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REV 11

Wireless
Semiconductor Solutions
RF and IF Device Data



"Creating the World of Tomorrow with Technology Today."

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Wireless Semiconductor Solutions RF and IF Device Data

FOREWORD

This publication includes technical information for the several product families that comprise the Motorola portfolio of Wireless Semiconductor RF and IF Products. The product families include bipolar, LDMOS, MOSFET RF Power, and gallium arsenide chip technologies in a variety of ceramic and plastic surface mount packages. Discrete components, hybrid modules, and integrated circuits provide different levels of complexity in an effort to provide solutions for our customers' needs.

All devices are in alphanumeric order in the *Device Index* of this book. Just turn to the appropriate page for technical details of the known device. Complete device specifications are provided in the form of *Data Sheets* which are categorized by product type into six chapters for easy reference. *Selector Guides* by product family are provided at the beginning of the book as well as in the beginning of each chapter to enable quick comparisons of performance characteristics and to aid you in identifying devices that meet your functional performance requirements of frequency, output power, gain, or other parameters.

Chapters on Tape and Reel Options, Packaging Information, Applications and Product Literature include additional information to aid you in the design process.

Applications assistance is only a phone call away — call the nearest Semiconductor Sales office or 1-800-521-6274. Please refer to our section on *On–line Access to Wireless Semiconductor Data* so that you will always have easy access to the most current information available on Motorola's Wireless Semiconductor product portfolio.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

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ABOUT THIS REVISION

The Wireless Semiconductor Solutions RF and IF Device Data Book is contained in two volumes. This edition encompasses a considerable number of changes that have occurred since our last printing. Some devices have been removed from this book due to package changes or new technology replacements and many new devices have been added.

Application Notes, Engineering Bulletins and Article Reprints of special interest to designers of RF and IF equipment are available on the Motorola Semiconductor Product Sector Web site or are available through the Motorola Literature Distribution Center. Phone and fax numbers for ordering literature are listed on the back cover of this book and in our Accessing Data On–line section. See Chapter Ten for a complete listing of Application Literature.

For Cross Reference information on Motorola replacement devices, please consult your local Distributor or Motorola Sales Office. See Chapter Eleven in this data book for a complete listing of Motorola Distributor and Worldwide Sales Offices.

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Chapter One

Wireless Semiconductor Solutions RF and IF Selector Guide

While Motorola is a worldwide leader in semiconductor products, there is not a category in which the selection is more diverse, or more complete, than in products designed for RF system applications. From MOS, bipolar power and signal transistors to integrated circuits, Motorola's RF components cover the entire spectrum from HF to microwave to personal communications. Yet, product expansion continues — not only to keep pace with the progressive needs of the industry, but to better serve the needs of designers for a reliable and comprehensive source of supply.

How to Use This Selector Guide

The RF Monolithic Integrated Circuits and the RF/IF Integrated Circuits products in this guide are divided into three major functional categories: RF Front End ICs, RF/IF Subsystem ICs and Frequency Synthesis. Each of these categories is further subdivided based on circuit functionality. This structure differentiates highly integrated subsystem ICs from fundamental circuit building blocks and discrete transistors.

The Small Signal Transistors, Medium Power Transistors, Power MOSFETs, Power Bipolar Transistors, Power Amplifier Modules and CATV Distribution Amplifiers are FIRST divided into major categories by power level. SECOND, within each category parts are listed by frequency band, except for small signal and medium power transistors, which are divided by application. Small signal transistor applications are low noise, linear amplifiers, switches, and oscillators. THIRD, within a frequency band, transistors are further grouped by operating voltage and, finally, output power.

To Replace Devices in an Existing Design

Call your local Motorola Sales Office or Distributor to determine Motorola's closest replacement device.

Applications Assistance

Applications assistance is only a phone call away — call the nearest Semiconductor Sales office or 1-800-521-6274.

Access Data On–Line!

Use the Motorola SPS Internet to access Motorola Semiconductor Product data at http://mot–sps.com or http://mot–sps.com/rf/. The SPS Internet provides you with instant access to data sheets, selector guide information, package outlines, on–line technical support and much more.

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RF Front End ICs

Motorola's RF Front End integrated circuit devices provide an integrated solution for the personal communications market. These devices are available in plastic SO–8, SO–16, SOT–143, TSSOP–16, TSSOP–16EP, Micro–8, TSSOP–20EP, LQFP–48 or PFP–16 packages.

Evaluation Boards

Evaluation boards are available for RF Front End Integrated Circuits. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

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RF Front End ICs

RFICs

Downconverters

Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	LNA Gain dB (Typ)	LNA NF dB (Typ)	Mixer Conv. Gain dB (Typ)	Mixer NF dB (Typ)	Case No./ Package	System Applicability
MC13142[18b]	DC to 1800	2.7 to 6.5	13.5	17	1.8	–3.0	12	751B/ SO–16	ISM, Cellular, PCS

Upconverters/Exciters

Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current mA (Typ)	Conv. Gain dB (Typ)	Output IP3 dBm (Typ)	Case No./ Package	System Applicability
MRFIC0954[18b]	800 to 1000	2.7 to 5.0	65	5.0	31	28	948M/ TSSOP–20EP	CDMA, TDMA, ISM
MRFIC1813[18b]	1700 to 2000	2.7 to 4.5	25	0.1	15	11	948C/ TSSOP–16	DCS1800, PCS
MRFIC1854[18b]	1700 to 2000	2.7 to 5.0	70	5.0	31	23	948M/ TSSOP–20EP	CDMA, TDMA, PCS

Power Amplifiers

Device	Freq. Range MHz	Supply Volt. Range Vdc	Saturated P_{out} dBm (Typ)	PAE % (Typ)	Gain P_{out}/P_{in} dB (Typ)	Case No./ Package	System Applicability
MRFIC0917[18e]	800 to 1000	2.7 to 5.5	34.5	45	22.5	978/PFP–16	GSM
MRFIC0919[18b]★	800 to 1000	3.0 to 5.5	35.3	48	32.3	948L/ TSSOP–16EP	GSM
MRFIC1817[18e]	1700 to 2000	2.7 to 5.0	33.5	42	30.5	978/PFP–16	DCS1800, PCS
MRFIC1818[18e]	1700 to 2000	2.7 to 6.0	34.5	42	31.5	978/PFP–16	DCS1800, PCS
MRFIC1819[18b]★	1700 to 2000	3.0 to 5.0	33	40	27	948L/ TSSOP–16EP	DCS1800, PCS
MRFIC1856[18b]★	800 to 1000	3.0 to 5.6	32	50	32	948M/ TSSOP–20EP	TDMA, CDMA, AMPS
	1700 to 2000		30	35	30		TDMA, CDMA, PCS

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

★New Product

RF Building Blocks

Amplifiers

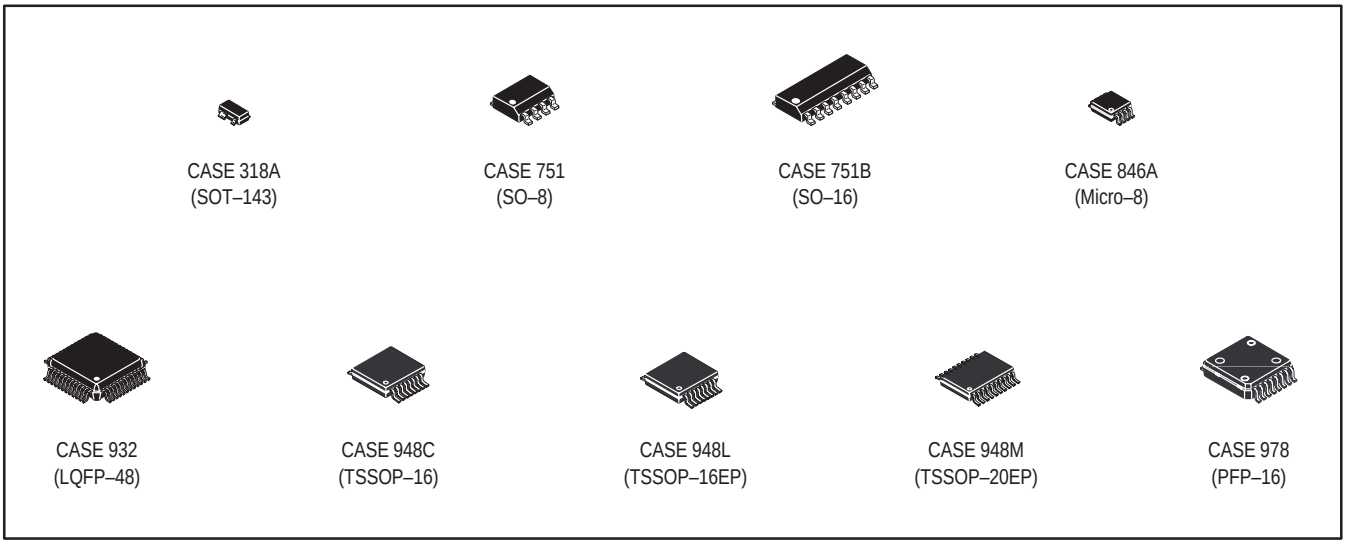
Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current μA (Typ)	Small Signal Gain dB (Typ)	Output IP3 dBm (Typ)	NF dB (Typ)	Case No./ Package	System Applicability
MC13144[18b]	100 to 2000	1.8 to 6.0	8.5	1	17	12	1.4	751/SO–8	ISM, PCS, Cellular
MRFIC0915[18c]	100 to 2500	2.7 to 5.0	2.0	–	16.2	4.0	1.9	318A/ SOT–143	ISM, PCS, Cellular
MRFIC0916[18c]	100 to 2500	2.7 to 5.0	4.7	–	18.5	11	1.9	318A/ SOT–143	ISM, PCS, Cellular
MRFIC0930DM[18b]	800 to 1000	2.7 to 4.5	8.5	20	19	10	1.7	846A/ Micro–8	GSM, AMPS, ISM
MRFIC1501[18b]	1000 to 2000	3.0 to 5.0	5.9	–	18	10	1.1	751/SO–8	GPS
MRFIC1808DM[18b]	1700 to 2100	2.7 to 4.5	5.0	8.0	18	13	1.6	846A/ Micro–8	DCS1800, PCS
MRFIC1830DM[18b]	1700 to 2100	2.7 to 4.5	9.0	20	18.5	8.5	2.1	846A/ Micro–8	DCS1800, PCS

Mixers

Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current μA (Typ)	Conv. Gain dB (Typ)	Input IP3 dBm (Typ)	Case No./ Package	System Applicability
MC13143[18b]	DC to 2400	1.8 to 6.0	4.1	–	–2.6	16	751/SO–8	ISM, PCS, Cellular

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

RF Front End Integrated Circuit Packages



RF/IF Subsystems

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RF/IF Subsystems

Cordless Phone Subsystem ICs

Device	V_{CC}	I_{CC} (Typ)	Dual Conversion Receiver	Universal Dual PLL	Compander and Audio Interface	CVSD Compatible	Low Battery Detect	Notes	Suffix/ Case No.
MC13109A	2.0 to 5.5 V	Active Mode 6.7 mA Inactive Mode 40 µA	✓	✓	✓	–	✓	CT–0	FB/848B, FTA/932
MC13110A	2.7 to 5.5 V	Active Mode 8.5 mA Inactive Mode 15 µA	✓	✓	✓	–	✓	CT–0	FB/848B FTA/932
MC13111A	2.7 to 5.5 V	Active Mode 8.5 mA Inactive Mode 15 µA	✓	✓	✓	–	✓	CT–0	FB/848B, FTA/932
MC13145	2.7 to 6.5 V	Active Mode 27 mA Inactive Mode 10 µA	✓	–	–	✓	–	Receiver with coilless demod CT–900	FTA/932
MC13146	2.7 to 6.5 V	Active Mode 18 mA Inactive Mode 10 µA	–	–	–	✓	–	Transmitter with VCO CT–900	FTA/977
MC33410	2.7 to 5.5 V	Active Mode 13 mA Inactive Mode 10 µA	✓	✓	–	✓	✓	Digital Baseband CT–900	FTA/932
MC33411A MC33411B	2.7 to 5.5 V	Active Mode 15 mA Inactive Mode 10 µA	✓	✓	✓	–	✓	Analog Baseband CT–900	FTA/932

GPS Subsystem ICs

Device	RF Freq (MHz)	IF Freq (MHz)	V_{CC} (V)	I_{CC} (mA) (Typ)	Dual Conversion Receiver	Dual Loop PLL	Limiting Amplifier	Variable Gain IF Amplifier	Case No.
MRFIC1502	1575	9.5	4.5 to 5.5	52	✓	✓	–	–	932
MRFIC1504	1575	4.1	2.7 to 3.3	28	✓	✓	✓	✓	932

Receivers

Device	V_{CC}	I_{CC} (Typ)	Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Case No.
MC2800	1.1 to 3.0 V	1.5 mA	–110 dBm	75 MHz	455 kHz	–	✓	>1.2 kb	Pager Applications	FTA/873C
MC3356	3.0 to 9.0 V	20 mA	30 µV	150 MHz	10.7 MHz	✓	–	500 kb	Includes front end mixer/L.O.	DW/751D

Receivers (continued)

Device	V_{CC}	I_{CC} (Typ)	Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Case No.
MC3361B	2.0 to 8.0 V	3.9 mA	2.6 µV	60 MHz	455 kHz	✓	–	>4.8 kb	Squelch and Scan	D/751B
MC3361C	2.0 to 8.0 V	2.8 mA				✓	–			D/751B
MC3371	2.0 to 9.0 V	3.6 mA	1.0 µV	100 MHz			✓ 60 dB		RSSI	D/751B, DTB/948F
MC3372									RSSI, Ceramic Quad Detector/Resonator	
MC3374	1.1 to 3.0 V	1.6 mA	0.5 µV	75 MHz		–	–		Low Battery Detect	FTB/873
MC13135	2.0 to 6.0 V	4.0 mA	1.0 µV	200 MHz	10.7 MHz/ 455 kHz	–	✓ 70 dB	>4.8 kb	Voltage Buffered RSSI, LC Quad Detector	DW/751E, P/724
MC13136									Voltage Buffered RSSI, Ceramic Quad Detector	DW/751E
MC13150	2.5 to 6.0 V	1.7 mA	2.0 µV	500 MHz		✓	✓ 110 dB	>9.6 kb	Coilless Detector with Adjustable Bandwidth	FTB/873, FTA/977
MC13156	2.0 to 6.0 V	5.0 mA	2.0 µV	500 MHz	21.4 MHz	–	✓ 80 dB	500 kb	CT–2 FM/Demodulator	DW/751E, FB/873
MC13158	2.0 to 6.0 V	6.0 mA		500 MHz				>1.2 Mb	FM IF/Demodulator with split IF for DECT	FTB/873

IFs

Device	V_{CC}	I_{CC} (Typ)	Sensitivity (Typ)	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Case No.
MC13055	3.0 to 12 V	20 mA	20 µV	40 MHz	✓	✓	2.0 Mb	Wideband Data IF, includes data shaper	D/751B
MC13155	3.0 to 6.0 V	7.0 mA	1.0 mV	250 MHz	–		10 Mb	Video Speed FM IF	D/751B

Transmitters

Device	V_{CC}	I_{CC} (Typ)	P_{out}	Max RF Freq Out	Max Mod Freq	Notes	Suffix/ Case No.
MC13176	2.0 to 5.0 V	40 mA	10 dBm	1.0 GHz	5.0 MHz	$f_{out} = 32 \times f_{ref}$, includes power down function, AM/FM Modulation	D/751B

Miscellaneous Functions

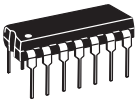
ADCs/DACs

Device	Function	I/O Format	Resolution	Number of Analog Channels	On–Chip Oscillator	Other Features	Suffix/ Case No.
MC144110	DAC	Serial	6 Bits	6	–	Emitter–Follower Outputs	DW/751D
MC144111				4			DW/751G
MC145050	ADC		10 Bits	11	–	Successive Approximation	P/738, DW/751D
MC145051					✓		
MC145053				5			P/646, D/751A

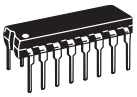
Encoders/Decoders

Device	Function	Number of Address Lines	Maximum Number of Address Codes	Number of Data Bits	Operation	Suffix/ Case No.
MC145026	Encoder	Depends on Decoder	Depends on Decoder	Depends on Decoder	Simplex	P/648, D/751B
MC145027	Decoder	5	243	4	Simplex	P/648, DW/751G
MC145028		9	19,683	0	Simplex	

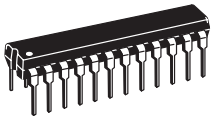
RF/IF Subsystems Packages



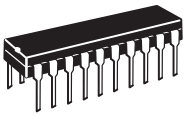
CASE 646
P SUFFIX
(DIP–14)



CASE 648
P SUFFIX
(DIP–16)



CASE 724
P SUFFIX
(DIP–24)



CASE 738
P SUFFIX
(DIP–20)



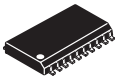
CASE 751
D SUFFIX
(SO–8)



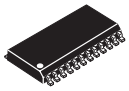
CASE 751A
D SUFFIX
(SO–14)



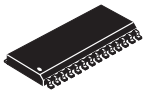
CASE 751B
D SUFFIX
(SO–16)



CASE 751D
DW SUFFIX
(SO–20L)



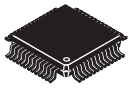
CASE 751E
DW SUFFIX
(SO–24L)



CASE 751F
DW SUFFIX
(SO–28L)



CASE 751G
DW SUFFIX
(SO–16W)



CASE 848B
FB SUFFIX
(QFP–52)



CASE 873
FB, FTB SUFFIX
(LQFP–32)



CASE 873C
FTA SUFFIX
(LQFP–32)



CASE 932
FTA SUFFIX
(LQFP–48)



CASE 948D
DT SUFFIX
(TSSOP–20)



CASE 948F
DTB SUFFIX
(TSSOP–16)



CASE 977
FTA SUFFIX
(LQFP–24)

Frequency Synthesis

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Frequency Synthesis

Single PLL Synthesizers

Maximum Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Features	Device	Suffix/ Case
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Parallel Interface	MC145151–2	DW/751F
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Parallel Interface, Uses External Dual–Modulus Prescaler	MC145152–2	DW/751F
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Serial Interface	MC145157–2	DW/751G
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Serial Interface, Uses External Dual–Modulus Prescaler	MC145158–2	DW/751G
100 @ 3.0 V 185 @ 4.5 V	2.7 to 5.5	2 @ 3 V 6 @ 5 V	Serial Interface, Auxiliary Reference Divider, Evaluation Kit – MC145170EVK	MC145170–2	P/648, D/751B, DT/948C
1000	2.7 to 5.5	4.25	4–Line Parallel Interface	MC12181	D/751B
1100	2.7 to 5.5	7 @ 5 V	Serial Interface, Standby, Auxiliary Reference Divider, Evaluation Kit – MC145191EVK	MC145193(46a)	F/751J, DT/948D
2000	2.7 to 5.5	4 @ 3 V	Serial Interface, Standby, Auxiliary Reference Device, Evaluation Kit – MC145202EVK	MC145202–1(46a)	F/751J, DT/948D
2500	2.7 to 5.5	9.5	Serial Interface	MC12210	D/751B, DT/948E
2800	4.5 to 5.5	3.5	Fixed Divider	MC12179	D/751

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

Dual PLL Synthesizers

Maximum Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Phase Detector	Device	Suffix/ Case
60 @ 3.0 V both loops	2.5 to 5.5	3 @ 3 V	Serial Interface, Standby	MC145162	P/648, D/751B
85 @ 3.0 V both loops	2.5 to 5.5	3 @ 3 V	Serial Interface, Standby	MC145162–1	D/751B
550, 60	1.8 to 3.6	3	10 MHz Serial Interface, Multiple Standby Modes, Dual 8–Bit DACs, Voltage Multiplier for Phase Detectors (See Note).	MC145181	FTA/873C
1100 both loops	2.7 to 5.5	12	Serial Interface, Standby, Evaluation Kit – MC145220EVK	MC145220	F/803C, DT/948D
1200, 550	1.8 to 3.6	4	10 MHz Serial Interface, Multiple Standby Modes, Dual 8–Bit DACs, Voltage Multiplier for Phase Detectors (See Note).	MC145225	FTA/873C
2200, 550	1.8 to 3.6	5	10 MHz Serial Interface, Multiple Standby Modes, Dual 8–Bit DACs, Voltage Multiplier for Phase Detectors (See Note).	MC145230	FTA/873C

NOTE: The MC145230EVK development system may be used with the MC145181, MC145225, or MC145230. The MC145230 is soldered to a tested board; MC145181, MC145225 and MC145230 device samples are included. The user must supply the VCOs for the MC145181.

PLL Building Blocks

Prescalers

Frequency (MHz)	Divide Ratios	Single or Dual Modulus	Supply Voltage (V)	Supply Current (mA)	Features	Device	Suffix/ Case
1100	64/65, 128/129	Dual	2.7 to 5.5	2.0 max	Low Power	MC12052A	D/751
1100	64/65, 128/129	Dual	2.7 to 5.5	2.5 max	Low Power, Standby	MC12053A	D/751
1100	126/128, 254/256	Dual	2.7 to 5.5	2.0 max	Low Power	MC12058	D/751
1100	10,20,40,80	Single	4.5 to 5.5	5.0 max		MC12080	D/751
1100	2, 4, 8	Single	2.7 to 5.5	4.5 max	Standby	MC12093	D/751
2000	64/65, 128/129	Dual	2.7 to 5.5	2.6 max	Low Power	MC12054A	D/751
2500	2, 4	Single	2.7 to 5.5	14 max	Standby	MC12095	D/751
2800	64, 128, 256	Single	4.5 to 5.5	11.5 max		MC12079	D/751
2800	64, 128	Single	4.5 to 5.5	14.5 max		MC12089	D/751

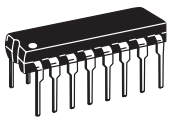
Voltage Control Oscillators

Frequency (MHz)	Supply Voltage (V)	Features	Device	Suffix/ Case
1300	2.7 to 5.5	Two high drive open collector outputs (Q, QB), Adjustable output amplitude, Low drive output for prescaler	MC12149	D/751

Phase–Frequency Detectors

Frequency (MHz)	Supply Voltage (V)	Features	Device	Suffix/ Case
800 (Typ)	4.75 to 5.5	MECL10H compatible	MCH12140	D/751
800 (Typ)	4.2 to 5.5	100K ECL compatible	MCK12140	D/751

RF/IF Integrated Circuits Packages



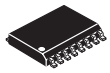
CASE 648
P SUFFIX
(DIP–16)



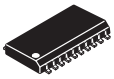
CASE 751
D SUFFIX
(SO–8)



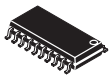
CASE 751B
D SUFFIX
(SO–16)



CASE 751G
DW SUFFIX
(SO–16W)



CASE 751J
F SUFFIX
(SO–20)



CASE 803C
F SUFFIX
(SO–20)



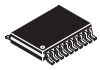
CASE 873C
FTA SUFFIX
(LQFP–32)



CASE 948C
DT SUFFIX
(TSSOP–16)



CASE 948D
DT SUFFIX
(TSSOP–20)



CASE 948E
DT SUFFIX
(TSSOP–20)

Motorola RF Discrete Transistors

Motorola offers the most extensive group of RF Discrete Transistors offered by any semiconductor manufacturer anywhere in the world today.
From Bipolar to FET, from Low Power to High Power, the user can choose from a variety of packages. They include plastic and ceramic that are microstrip circuit compatible or surface mountable. Many are designed for automated assembly equipment.
Major sub–headings are Small Signal, Medium Power, Power MOSFETs and Bipolar Transistors.

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Packages	1.1–27

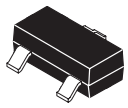
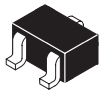
Motorola RF Small Signal Transistors

Motorola's broad line of RF Small Signal Transistors includes NPN Silicon Bipolar Transistors characterized for low noise amplifiers, mixers, oscillators, multipliers, non–saturated switches and low–power drivers.

These devices are available in a variety of package types. Most of these transistors are fully characterized with s–parameters.

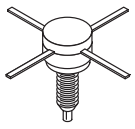
Plastic Packages

Table 1. Plastic

Device	Gain–Bandwidth @ f_T Typ GHz	Gain–Bandwidth @ I_C mA	NF_{min} @ f Typ dB	NF_{min} @ f MHz	Gain @ f Typ dB	Gain @ f MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	Maximum Ratings I_C mA	Package
Case 318–08/6 — SOT–23									
MMBR941LT1(18c)	8.0	15	2.1	2000	8.5	2000	10	50	
MMBR941LT3(18d)	8.0	15	2.1	2000	8.5	2000	10	50	
MMBR941BLT1(18c)	8.0	15	2.1	2000	8.5	2000	10	50	
MMBR951LT1(18c)	8.0	30	2.1	2000	7.5	2000	10	100	
Case 419 — SC–70/SOT–323									
MRF947T1(18c,d)	8.0	15	2.1	2000	10.5	1500	10	50	
MRF947T3(18d)	8.0	15	2.1	2000	10.5	1500	10	50	
MRF947AT1(18c)	8.0	15	2.1	2000	10.5	1500	10	50	
MRF947BT1(18c,d)	8.0	15	2.1	2000	10.5	1500	10	50	
MRF957T1(18c)	9.0	30	2.0	2000	9.0	1500	10	100	
MRF1047T1(18c)	12	15	1.0	1000	13	1000	5.0	45	
Case 463/1 — SC–90/SC–75									
MRF949T1(18c)	9.0	15	1.5	1000	14	1000	–	50	
MRF959T1(18c)	9.0	30	1.6	1000	8.0	1000	–	100	

Ceramic SOE Case

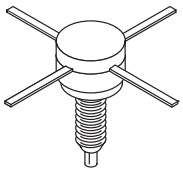
Table 2. Ceramic SOE Case

Device	Gain–Bandwidth @ f_T Typ GHz	Gain–Bandwidth @ I_C mA	NF @ f Typ dB	NF @ f MHz	Gain @ f Typ dB	Gain @ f MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	Maximum Ratings I_C mA	Package
Case 244A/1									
MRF587	5.5	90	3.0	500	13	500	15	200	

(17)PNP

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

RF Small Signal Transistors Packages



CASE 244A
STYLE 1



CASE 318–08
STYLE 6
(SOT–23)



CASE 419
(SC–70/SOT–323)



CASE 463
STYLE 1
(SC–90/SC–75)

Motorola RF Medium Power Transistors

RF Medium Power Transistors are used in portable transmitter applications and low voltage drivers for higher power devices. They can be used for analog cellular, GSM and the newer digital handheld cellular phones. GaAs, LDMOS and Bipolar devices are available. RF Medium Power Transistors are supplied in Motorola's high performance PLD line of surface mount power RF packages. Other applications include talkback pagers, wireless modems and LANs, cable modems, highspeed drivers and instrumentation.

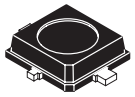
Discrete Wireless Transmitter Devices

Device	Freq. MHz	V_{DD} V	Typical Output Power dBm	Typical Drain Eff. %	Typical Gain dB	Semiconductor Technology	Case No./ Package
MRF9382T1 (18f, 46a)	900	6.0	36.5	65	10.5	LDMOS	449/PLD–1
MRF9482T1 (18f, 46a)	900	4.8	36.0	65	10	LDMOS	449/PLD–1

(18) Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

(46) To be introduced: a) 1Q00 b) 2Q00 c) 3Q00

RF Medium Power Transistors Packages



CASE 449
(PLD–1)

Motorola RF High Power Transistors

RF Power MOSFETs

Motorola RF Power MOSFETs are constructed using a planar process to enhance manufacturing repeatability. They are *N–channel field effect transistors* with an oxide insulated gate which controls vertical current flow.

Compared with bipolar transistors, RF Power FETs exhibit higher gain, higher input impedance, enhanced thermal stability and lower noise. The FETs listed in this section are specified for operation in RF Power Amplifiers and are grouped by frequency range of operation and type of application. Arrangement within each group is first by order of voltage then by increasing output power.

Table 1. 2 to 150 MHz HF/SSB – Vertical MOSFETs

For military and commercial HF/SSB fixed, mobile and marine transmitters.

Device	Frequency Band(37)	P_{out} Watts	Gain (Typ) @ 30 MHz dB	Typical IMD d_3 dB	Typical IMD d_{11} dB	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB							
MRF171A	U	2–225	30	20	–32	—	1.52	211–07/2
V_{DD} = 50 Volts, Class AB							
MRF148A	U	2–225	30	18	–35	–60	1.5	211–07/2
MRF150	U	2–150	150	17	–32	–60	0.6	211–11/2
MRF154	U	2–100	600	17	–25	—	0.13	368/2
MRF157	U	2–100	600	20	–25	—	0.13	368/2

Table 2. 2 to 225 MHz VHF AM/FM – Vertical MOSFETs

For VHF military and commercial aircraft radio transmitters.

Device	Frequency Band(37)	P_{out} Watts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB						
MRF134	U	30–225	5	14/150	55	10	211–07/2
MRF136	U	30–225	15	16/150	60	3.2	211–07/2
MRF171A	U	30–225	45	19.5/150	65	1.52	211–07/2
MRF173	U	30–225	80	13/150	65	0.8	211–11/2
MRF174	U	30–225	125	11.8/150	60	0.65	211–11/2
MRF141	U	2–175	150	10/175	55	0.6	211–11/2
MRF141G	U	2–175	300	13/175	55	0.35	375/2
V_{DD} = 50 Volts, Class AB						
MRF151	U	2–175	150	13/175	45	0.6	211–11/2
MRF151G	U	2–175	300	16/175	55	0.35	375/2

(37)M = Matched Frequency Band; U = Unmatched Frequency Band.

Table 3. 30 to 512 MHz VHF/UHF AM/FM

For VHF/UHF military and commercial aircraft radio transmitters.

Device	Frequency Band(37)		P_{out} Watts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB – Vertical MOSFETs							
MRF158	U	30–512	2	17.5/500	52	13.2	305A/2
MRF160	U	30–512	4	17/500	55	7.2	249/3
MRF166C	U	30–512	20	16/500	55	2.5	319/3
MRF166W	U	30–512	40	16/500	55	1.0	412/1
MRF177	U	100–400	100	12/400	60	0.65	744A/2
MRF275L	U	150–512	100	8.8/500	55	0.65	333/2
MRF275G	U	150–512	150	11.2/500	55	0.44	375/2

Table 4. Mobile – To 520 MHz

Designed for broadband VHF & UHF commercial and industrial applications. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 12.5/7.5 volt mobile, portable and base station operation.

Device	Frequency Band(37)		P_{out} Watts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Package/Style
VHF & UHF, V_{DD} = 7.5 Volts, Class AB, Land Mobile Radio – LDMOS Die							
MRF1511T1(18f,46a)	U	136–175	8	11.5/175	55	2.0	466/1
MRF1517T1(18f,46a)	U	430–520	8	11/520	55	2.0	466/1
VHF & UHF, V_{DD} = 7.5/12.5 Volts, Class AB, Land Mobile Radio – LDMOS Die							
MRF1513T1(18f,46a)	U	400–520	3	11/520	55	2.0	466/1
VHF & UHF, V_{DD} = 12.5 Volts, Class AB, Land Mobile Radio – LDMOS Die							
MRF1518T1(18f,46a)	U	400–520	8	11/520	55	2.0	466/1

Table 5. Broadcast – To 1.0 GHz – Lateral MOSFETs

Device	Frequency Band(37)		P_{out} Watts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	IMD dBc	Package/Style
470 – 1000 MHz, V_{DD} = 28 Volts, Class AB – LDMOS Die								
MRF373	U	470–1000	60	14.7/860	54	1.0	—	360B/1
MRF373S	U	470–1000	60	14.7/860	54	0.75	—	360C/1
MRF372(9)	M	470–1000	180 PEP	14.0/860	35	0.4	–30	375B/2
MRF374	U	470–1000	100 PEP	13.5/860	36	0.5	–31	375F/2
470 – 1000 MHz, V_{DD} = 50 Volts, Class AB – LDMOS Die								
MRF376(9)	M	470–1000	240	14/860	55	0.3	—	375B/2

(9)In development.

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

(37)M = Matched Frequency Band; U = Unmatched Frequency Band.

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

Table 6. Cellular – To 1.0 GHz – Lateral MOSFETs

Device	Frequency Band(37)		P_{out} Watts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Package/Style
800 – 1.0 GHz, V_{DD} = 26 Volts, Class AB – LDMOS Die							
MRF6522–5R1(18a,46a)	U	960	5 CW	18/960	53	15	458A/1
MRF6522–10R1(18a,46a)	U	960	10 CW	17.5/960	55	6.0	458A/1
MRF6522–70(18i)★	M	921–960	70 CW	16/921–960	58	1.1	465D/1
MRF187	M	880	85 PEP	13/880	33	0.7	465/1
MRF187S	M	880	85 PEP	13/880	33	0.7	465A/1
MRF9085(46a)	M	880	85 PEP	17/880	38	0.7	465/1
MRF9085S(46a)	M	880	85 PEP	17/880	38	0.7	465A/1
MRF9180(46a)	M	880	180 PEP	17/880	38	0.4	375D/2
800 – 1.0 GHz, V_{DD} = 28 Volts, Class AB – LDMOS Die							
MRF181SR1(18a,46a)	U	945	8 PEP	17/945	35	3.6	458/1
MRF181ZR1(18a,46a)	U	945	8 PEP	17/945	35	3.6	458A/1
MRF182	U	945	30 CW	14/945	58	1.75	360B/1
MRF182S(18a)	U	945	30 CW	14/945	58	1.75	360C/1
MRF183	U	945	45 PEP	13.5/945	38	1.5	360B/1
MRF183S(18a)	U	945	45 PEP	13.5/945	38	1.5	360C/1
MRF9045(46a)	U	945	45 PEP	18/945	42	1.3	360B/1
MRF9045S(46a)	U	945	45 PEP	18/945	42	1.3	360C/1
MRF9045M(46a)	U	945	45 PEP	16/945	40	TBD	1265/–
MRF184	U	945	60 CW	13.5/945	60	1.1	360B/1
MRF184S(18a)	U	945	60 CW	13.5/945	60	1.1	360C/1
MRF185(3)	M	960	85 CW	14/960	53	0.7	375B/2
MRF186(3)	M	945	120 PEP	12/945	35	0.6	375B/2

Table 7. PCS and 3G – To 2.1 GHz – Lateral MOSFETs

Device	Frequency Band(37)		P_{out} Watts	Class	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Package/Style
1805 – 1990 MHz, V_{DD} = 26 Volts – LDMOS Die (GSM1800, GSM1900 and PCS TDMA)								
MRF18060A★	M	1805–1880	60 CW	AB	13/1805–1880	45	0.97	465/1
MRF18060AS★	M	1805–1880	60 CW	AB	13/1805–1880	45	0.97	465A/1
MRF18060B★	M	1930–1990	60 CW	AB	13/1930–1990	45	0.97	465/1
MRF18060BS★	M	1930–1990	60 CW	AB	13/1930–1990	45	0.97	465A/1
MRF18090A★	M	1805–1880	90 CW	AB	13.5/1805–1880	52	0.7	465B/1
MRF18090AS★	M	1805–1880	90 CW	AB	13.5/1805–1880	52	0.7	465C/1
MRF18090B★	M	1930–1990	90 CW	AB	13.5/1930–1990	45	0.7	465B/1
MRF18090BS★	M	1930–1990	90 CW	AB	13.5/1930–1990	45	0.7	465C/1
1.9 GHz, V_{DD} = 26 Volts – LDMOS Die (PCS CDMA)								
MRF19030(46a)	M	1930–1990	30 PEP	AB	13/1990	36	1.2	465E/1
MRF19030S(46a)	M	1930–1990	30 PEP	AB	13/1990	36	1.2	465F/1
MRF19045(46a)	M	1930–1990	45 PEP	AB	14/1990	37	0.84	465E/1
MRF19045S(46a)	M	1930–1990	45 PEP	AB	14/1990	37	0.84	465F/1
MRF19060★	M	1930–1990	60 PEP	AB	12.5/1990	36	0.97	465/1
MRF19060S★	M	1930–1990	60 PEP	AB	12.5/1990	36	0.97	465A/1

(3)Internal Impedance Matched Push-Pull Transistors

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

(37)M = Matched Frequency Band; U = Unmatched Frequency Band.

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

★New Product

Table 7. PCS and 3G – To 2.1 GHz – Lateral MOSFETs (continued)

Device	Frequency Band(37)	P_{out} Watts	Class	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Package/Style
1.9 GHz, V_{DD} = 26 Volts – LDMOS Die (PCS CDMA) (continued)							
MRF19090★	M	1930–1990	90 PEP	AB	11.5/1990	35	0.65	465B/1
MRF19090S(18a)★	M	1930–1990	90 PEP	AB	11.5/1990	35	0.65	465C/1
MRF19085(46a)	M	1930–1990	90 PEP	AB	12.5/1990	37	0.64	465/1
MRF19085S(46a)	M	1930–1990	90 PEP	AB	12.5/1990	37	0.64	465A/1
MRF19120(3,46a)	M	1930–1990	120 PEP	AB	11.8/1990	34.5	0.45	375D/2
MRF19120S(3,46a)	M	1930–1990	120 PEP	AB	11.8/1990	34.5	0.45	375E/2
MRF19125(46a)	M	1930–1990	125 PEP	AB	12.5/1990	35	0.53	465B/1
MRF19125S(46a)	M	1930–1990	125 PEP	AB	12.5/1990	35	0.53	465C/1
2.0 GHz, V_{DD} = 26 Volts – LDMOS Die							
MRF281SR1(18a,46a)	U	1930–2000	4 PEP	A, AB	13.6/2000	41	8.75	458/1
MRF281ZR1(18a,46a)	U	1930–2000	4 PEP	A, AB	13.6/2000	41	8.75	458A/1
MRF282SR1(18a,46a)	U	1930–2000	10 PEP	A, AB	12.5/2000	34	2.9	458/1
MRF282ZR1(18a,46a)	U	1930–2000	10 PEP	A, AB	12.5/2000	34	2.9	458A/1
MRF284	U	1930–2000	30 PEP	A, AB	10.5/2000	35	2.0	360B/1
MRF284SR1(18a)	U	1930–2000	30 PEP	A, AB	10.5/2000	35	2.0	360C/1
MRF286(46a)	M	1930–2000	60 PEP	A, AB	10.5/2000	31	0.73	465/1
MRF286S(46a)	M	1930–2000	60 PEP	A, AB	10.5/2000	31	0.73	465A/1
2.1 GHz, V_{DD} = 28 Volts – LDMOS Die (W–CDMA, UMTS)							
MRF21030(46a)	M	2110–2170	30 PEP	AB	13.5/2170	33	1.2	465E/1
MRF21030S(46a)	M	2110–2170	30 PEP	AB	13.5/2170	33	1.2	465F/1
MRF21060★	M	2110–2170	60 PEP	AB	12.5/2170	34	1.02	465/1
MRF21060S★	M	2110–2170	60 PEP	AB	12.5/2170	34	1.02	465A/1
MRF21090(46a)	M	2110–2170	90 PEP	AB	11.7/2170	33	0.65	465B/1
MRF21090S(46a)	M	2110–2170	90 PEP	AB	11.7/2170	33	0.65	465C/1
MRF21120(3,46a)	M	2110–2170	120 PEP	AB	11.3/2170	35	0.45	375D/2
MRF21120S(3,46a)	M	2110–2170	120 PEP	AB	11.3/2170	35	0.45	375E/2
MRF21125(26,46a)	M	2110–2170	125 PEP	AB	12/2170	34	0.53	465B/1
MRF21125S(26,46a)	M	2110–2170	125 PEP	AB	12/2170	34	0.53	465C/1
MRF21180(3,46a)	M	2110–2170	160 PEP	AB	11.3/2170	33	0.39	375D/2
MRF21180S(3,46a)	M	2110–2170	160 PEP	AB	11.3/2170	33	0.39	375E/2

(3)Internal Impedance Matched Push-Pull Transistors

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

(26)W–CDMA = 20 W P_{out}, 13 dB Gain, 18% Efficiency, 2.1125–2.1675 GHz.

(37)M = Matched Frequency Band; U = Unmatched Frequency Band.

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

RF Power Bipolar Transistors

Motorola's broad line of bipolar RF power transistors are characterized for operation in RF power amplifiers. Typical applications are in base stations, military and commercial landmobile, avionics and marine radio transmitters. Groupings are by frequency band and type of application. Within each group, the arrangement of devices is by major supply voltage rating, then in the order of increasing output power. All devices are NPN polarity except where otherwise noted.

UHF Transistors

Table 1. 100 – 500 MHz Band

Designed for UHF military and commercial aircraft radio transmitters.

Device	Frequency Band(37)		P_{out} Watts	Gain (Min)/Freq. dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class C						
MRF392(3)	M	100–400	125	8/400	0.65	744A/1
MRF393(3)	M	100–512	100	7.5/500	0.65	744A/1

900 MHz Transistors

Table 2. 900 – 960 MHz Band

Designed specifically for the 900 MHz mobile radio band, these devices offer superior gain, ruggedness, stability and broadband operation. Devices are for mobile and base station applications.

Device	Frequency Band(37)		P_{out} Watts	Class	Gain (Min)/Freq. dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 24 Volts — Si Bipolar							
MRF858S	U	840–900	3.6 (CW)	A	11/900	6.9	319A/2
MRF897(3)	M	900	30	AB	10/900	1.7	395B/1
MRF897R(3)	M	900	30	AB	10.5/900	1.7	395E/1
MRF898(2)	M	850–900	60 (CW)	C	7/900	1	333A/1
V_{CC} = 26 Volts — Si Bipolar							
MRF6409	M	921–960	20	AB	10/960	3.8	319/2
MRF6414	M	921–960	50	AB	8.5/960	1.3	333A/2
MRF899(3)	M	900	150	AB	8/900	0.8	375A/1

1.5 GHz Transistors

Table 3. 1600 – 1640 MHz Band

Device	Frequency Band(37)		P_{out} Watts	Class	Gain (Min)/Freq. dB/MHz	η Eff. (Min) %	θ_{JC} °C/W	Package/Style
MRF16006	M	1600–1640	6	C	7.4/1600	40	6.8	395C/2
MRF16030	M	1600–1640	30	C	7.5/1600	40	1.7	395C/2

(2)Internal Impedance Matched

(3)Internal Impedance Matched Push-Pull Transistors

(37)M = Matched Frequency Band; U = Unmatched Frequency Band.

Microwave Transistors

Table 4. L–Band Long Pulse Power

These products are designed for pulse power amplifier applications in the 960–1215 MHz frequency range. They are capable of handling up to 10 μs pulses in long pulse trains resulting in up to a 50% duty cycle over a 3.5 millisecond interval. Overall duty cycle is limited to 25% maximum. The primary applications for devices of this type are military systems, specifically JTIDS and commercial systems, specifically Mode S. Package types are hermetic.

Device	Frequency Band(37)		P_{out} Watts	Gain (Min) @ 1215 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts — Class C Common Base						
MRF10005	M	960–1215	5	8.5	8	336E/1
V_{CC} = 36 Volts — Class C Common Base						
MRF10031	M	960–1215	30	10	3	376B/1
MRF10120	M	960–1215	120	8	0.6	355C/1
V_{CC} = 50 Volts — Class C Common Base						
MRF10150	M	1025–1150	150	10(7)	0.25	376B/1
MRF10350	M	1025–1150	350	9(7)	0.11	355E/1
MRF10502	M	1025–1150	500	9(7)	0.12	355J/1

Linear Transistors

The following sections describe a wide variety of devices specifically characterized for linear amplification. Included are medium power and high power parts covering frequencies to 2.0 GHz.

Table 5. UHF Ultra Linear For TV Applications

The following device has been characterized for ultra–linear applications such as low–power TV transmitters in Band IV and Band V and features diffused ballast resistors and an all–gold metal system to provide enhanced reliability and ruggedness.

Device	Frequency Band(37)		P_{out} Watts	Gain (Typ)/Freq. Small Signal Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class AB						
TPV8100B	M	470–860	100(11)	9.5/860	0.7	398/1

Table 6. Microwave Linear for PCN Applications

The following devices have been developed for linear amplifiers in the 1.5–2 GHz region and have characteristics particularly suitable for PDC, PCS or DCS1800 base station applications.

Device	Frequency Band(37)		P_{out} Watts	Class	Gain (Typ)/Freq. dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 26 Volts–Bipolar Die							
MRF6404(16)	M	1860–1900	30	AB	8.2/1880	1.4	395C/1
MRF20030R	M	2000	30	AB	11/2000	1.4	395C/1
MRF20060R	M	2000	60	AB	9.8/2000	0.7	451/1
MRF20060RS	M	2000	60	AB	9.8/2000	0.7	451A/1

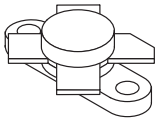
(7)Typical @ 1090 MHz

(11)Output power (Min) at 1 dB compression in Class AB

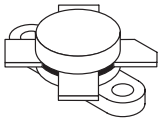
(16)Formerly known as “TP4035”

(37)M = Matched Frequency Band; U = Unmatched Frequency Band.

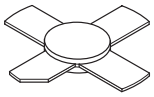
RF Power MOSFETs and Bipolar Transistors Packages



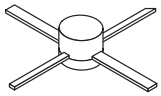
CASE 211–07
STYLE 2
(.380″ FLANGE)



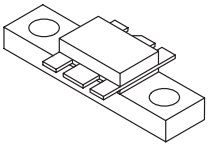
CASE 211–11
STYLE 2
(.500″ FLANGE)



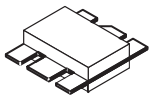
CASE 249–06
STYLE 3



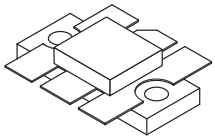
CASE 305A
STYLE 1, 2
(.204″ PILL)



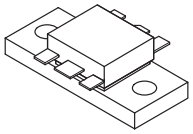
CASE 319
STYLE 1, 2, 3
(CS–12)



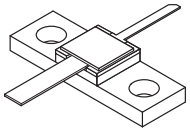
CASE 319A
STYLE 2



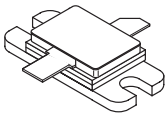
CASE 333
STYLE 2



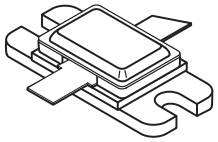
CASE 333A
STYLE 1, 2
(MAAC PAC)



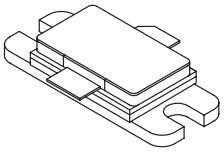
CASE 336E
STYLE 1



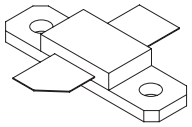
CASE 355C
STYLE 1



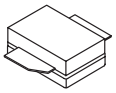
CASE 355E
STYLE 1



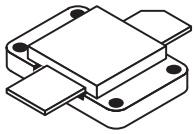
CASE 355J–02
STYLE 1



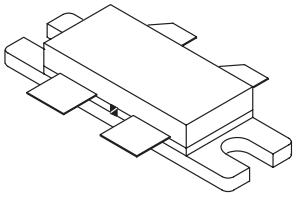
CASE 360B
STYLE 1
(Micro 250)



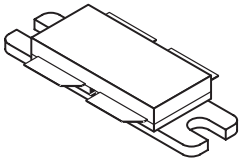
CASE 360C
STYLE 1
(Micro 250S)



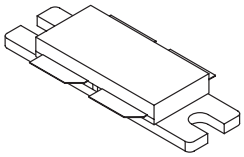
CASE 368
STYLE 2
(HOG PAC)



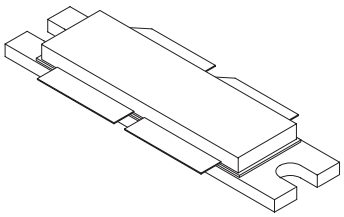
CASE 375
STYLE 2



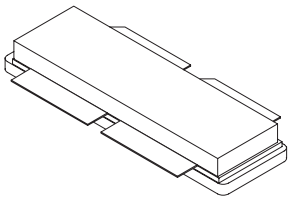
CASE 375A
STYLE 1



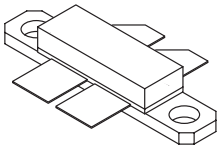
CASE 375B
STYLE 2
(Micro 860)



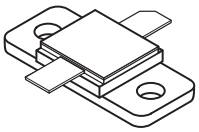
CASE 375D
STYLE 2



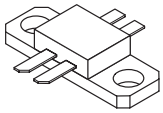
CASE 375E
STYLE 2



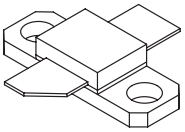
CASE 375F
STYLE 1



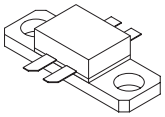
CASE 376B
STYLE 1



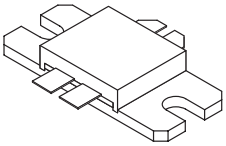
CASE 395B
STYLE 1



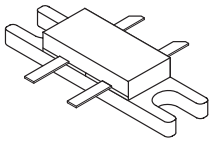
CASE 395C
STYLE 1, 2



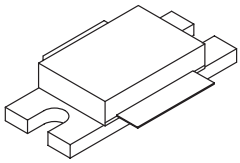
CASE 395E
STYLE 1



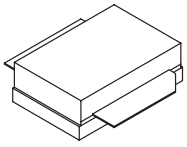
CASE 398
STYLE 1



CASE 412
STYLE 1



CASE 451
STYLE 1



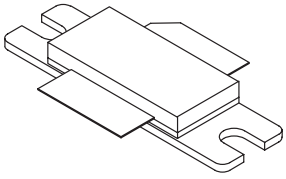
CASE 451A
STYLE 1



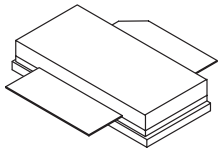
CASE 458
STYLE 1
(Micro 200S)



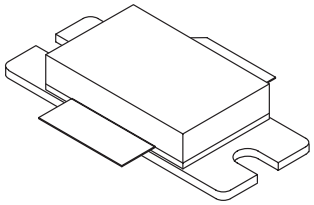
CASE 458A
STYLE 1
(Micro 200Z)



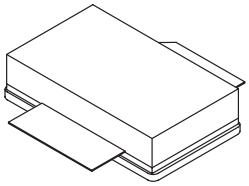
CASE 465
STYLE 1



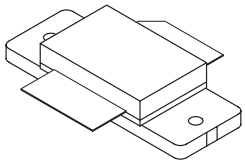
CASE 465A
STYLE 1



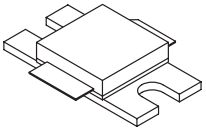
CASE 465B
STYLE 1



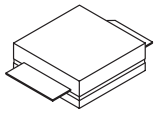
CASE 465C
STYLE 1



CASE 465D
STYLE 1



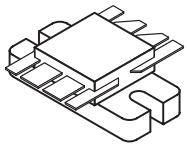
CASE 465E
STYLE 1



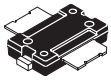
CASE 465F
STYLE 1



CASE 466
STYLE 1
PLASTIC
(PLD 1.5)



CASE 744A
STYLE 1, 2



CASE 1265
PLASTIC
(TO–270)

Motorola RF Amplifier Modules

Motorola's RF portfolio includes many hybrid designs optimized to perform either in narrowband base station transmitter applications, or in broadband linear amplifiers. Motorola modules feature two or more active transistors (LDMOS, GaAs, or Bipolar die technology) and their associated 50 ohm matching networks. Circuit substrate and metallization have been selected for optimum performance and reliability. For PA designers, hybrid modules offer the benefits of small and less complex system designs, in less time and at a lower overall cost.

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Packages	1.1–32

Motorola RF Amplifier Modules/ICs

Complete amplifiers with 50 ohm input and output impedances are available for all popular base station transmitter systems, including GSM and CDMA, covering frequencies from 800 MHz up to 2.2 GHz.

Base Stations

Designed for applications such as macrocell drivers and microcell output stage, these class AB amplifiers are ideal for GSM base station systems at 900, 1800 and 1900 MHz, with power requirements up to 16 watts.

Table 1. Base Stations

Device	Frequency MHz	P_{out} Watts	Gain (Min) dB	Supply Voltage Volts	Class	System Application	Die Technology	Package/Style
MHVIC910L(46b)	921–960	10	22	26	AB	GSM900	LDMOS–IC	978/–
MHW1810–1	1805–1880	10	24	26	AB	GSM1800	LDMOS	301AW/1
MHW1810–2	1805–1880	10	32	26	AB	GSM1800	LDMOS	301AW/1
MHW1815	1805–1880	15	30	26	AB	GSM1800	Silicon Bipolar	301AK/1
MHW1910–1	1930–1990	10	24	26	AB	GSM1900	LDMOS	301AW/1
MHW1915	1930–1990	15	29	26	AB	GSM1900	Silicon Bipolar	301AK/1

Table 2. Base Station Drivers

These 50 ohm amplifiers are recommended for modern multi–tone CDMA, TDMA and UMTS base station pre–driver applications. Their high third–order intercept point, tight phase and gain control, and excellent group delay characteristics make these devices ideal for use in high–power feedforward loops.

Ultra–Linear (for CDMA, W–CDMA, TDMA, Analog) – Class A (Silicon Bipolar Die)

Device	Frequency Band MHz	V_{CC} (Nom.) Volts	I_{CC} (Nom.) mA	Gain (Nom.) dB	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept (Typ) dBm	NF (Typ) dB	Case/ Style
MHL9128	800–960	28	400	20	0.5	31	43	7.5	448/1

Ultra–Linear (for CDMA, W–CDMA, TDMA, Analog) – Class A (LDMOS Die) – Lateral MOSFETs

Device	Frequency Band MHz	V_{DD} (Nom.) Volts	I_{DD} (Nom.) mA	Gain (Nom.) dB	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept (Typ) dBm	NF (Typ) dB	Case/ Style
MHL9838★	800–925	28	770	31	.1	39	50	3.7	301AP/1
MHL9236	800–960	26	550	30.5	.1	34	47	3.5	301AP/1
MHL9236M	800–960	26	550	30.5	.1	34	47	3.5	301AP/2
MHL9318★	860–900	28	500	17.5	.1	35.5	49	3.0	301AS/1
MHL19338★	1900–2000	28	500	30	.1	36	46	4.2	301AP/1
MHL19936(46b)	1900–2000	28	1400	30	.2	41	51	4.2	301AY/1
MHL21336(46a)	2100–2200	26	500	30	.15	35	45	4.5	301AP/1

Ultra–Linear (for CDMA, W–CDMA, TDMA, Analog) – Class A – GaAs FET

MHL9025(46b)	790–920	15	330	21.5	.25	31.5	48	2.5	438F/1

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

★New Product

Wideband Linear Amplifiers

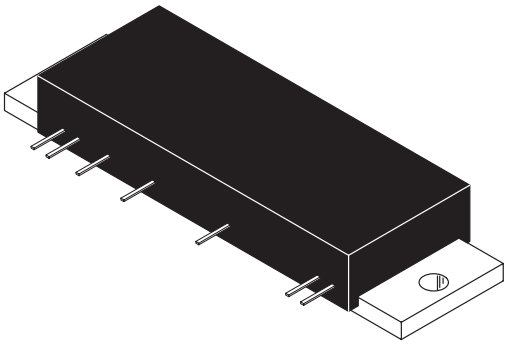
Table 1. Standard 50 Ohm Linear Hybrid

This series of RF linear hybrid amplifier has been optimized for wideband, 50 ohm applications. These amplifiers were designed for multi–purpose RF applications where linearity, dynamic range and wide bandwidth are of primary concern. The MHL series utilizes a new case style that provides microstrip input and output connections.

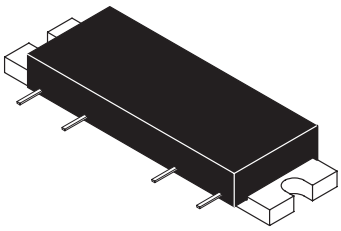
Device	Frequency Band MHz	V_{CC} (Nom.) Volts	I_{CC} (Nom.) mA	Gain/Freq. (Typ) dB/MHz	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept Point/Freq. (Typ) dBm/MHz	NF/Freq. (Typ) dB/MHz	Case/ Style
MHL8115	40–1000	15	700	17.5/900	1	30	41.5/1000	8.5/1000	448/2
MHL8118	40–1000	28	400	17.5/900	1	30	41.5/1000	8.5/1000	448/1

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

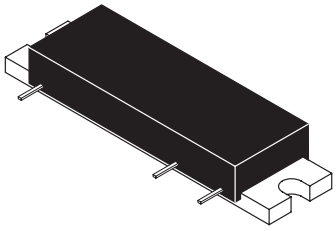
RF Amplifier Modules Packages



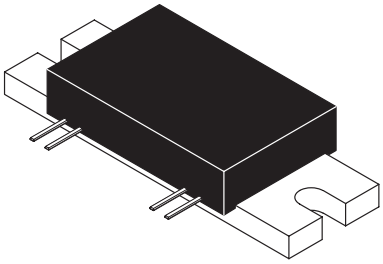
CASE 301AK
STYLE 1



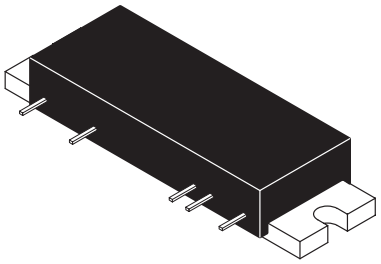
CASE 301AP
STYLE 1, 2



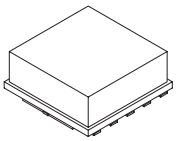
CASE 301AS
STYLE 1



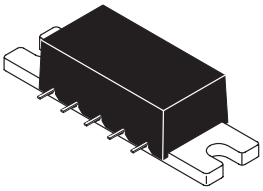
CASE 301AW
STYLE 1



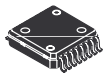
CASE 301AY
STYLE 1



CASE 438F
STYLE 1



CASE 448
STYLE 1, 2



CASE 978

Motorola RF CATV Distribution Amplifiers

Motorola Hybrids are manufactured using the latest generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels.

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Motorola RF CATV Distribution Amplifiers

Motorola Hybrids are manufactured using the latest generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels.

Forward Amplifiers

40–1000 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 1000 MHz dB Max	Package/ Style
			Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 152 CH	Cross Modulation dB 152 CH		
MHW9182B★	18.5	152	+38	–63(40)	–61	–61	7.5	714Y/1
MHW9242A★	24	152	+38	–61(40)	–61	–59	8.0	714Y/1

40–860 MHz Hybrids

Device	Gain dB Typ @ 50 MHz	Frequency MHz	V_{CC} Volts	2nd Order IMD @ V_{out} = 50 dBmV/ch Max	DIN45004B @ f=860 MHz dBμV Min	Noise Figure @ 860 MHz dB Max	Package/ Style
CA901	17	40 – 860	24	–60	120	8.0	714P/2
CA901A	17	40 – 860	24	–64	120	8.0	714P/2
Power Doubling Hybrids							
CA922	17	40 – 860	24	–63	123	9.5	714P/2
CA922A	17	40 – 860	24	–67	123	9.5	714P/2

40–860 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 860 MHz dB Max	Package/ Style
			Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 128 CH	Cross Modulation FM = 55.25 MHz dB 128 CH		
MHW8182B	18.5	128	+38	–64(40)	– 66	– 65	7.5	714Y/1
MHW8222B(46b)	21.9	128	+38	–59(40)	– 64	– 63	7.0	1302/1
MHW8242B★	24	128	+38	–62(40)	– 64	– 60	7.5	714Y/1
MHW8272A	27.2	128	+38	–64(40)	– 64	– 62	7.0	714Y/1
MHW8292	29	128	+38	–56(40)	– 60	– 60	7.0	714Y/1

(40)Composite 2nd Order; V_{out} = +38 dBmV/ch

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

★New Product

40–860 MHz Hybrids, V_{CC} = 24 Vdc, Class A (continued)

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB, 128 CH	Cross Modulation FM = 55.25 MHz dB, 128 CH	Noise Figure @ 860 MHz dB Max	Package/ Style
Power Doubling Hybrids								
MHW8185L(21)	18.5	128	+40	–62(39)	– 63	– 64	8.5*	714Y/1
MHW8185LR(28)	18.5	128	+40	–62(39)	– 63	– 64	8.5*	714Y/2
MHW8185	18.8	128	+40	–62(39)	– 64	– 64	8.0	714Y/1
MHW8185R(14)	18.8	128	+40	–62(39)	– 64	– 64	8.0	714Y/2
MHW8205L(22)	19.5	128	+40	–60(39)	– 63	– 64	8.5*	714Y/1
MHW8205	19.8	128	+40	–60(39)	– 63	– 64	8.0	714Y/1
MHW8205R(24)	19.8	128	+40	–60(39)	– 63	– 64	8.0	714Y/2
MHW8205LR(29,46b)	19.8	128	+40	–60(39)	– 63	– 64	8.5*	714Y/2

*@ 870 MHz

40–750 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB, 110 CH	Cross Modulation FM = 55.25 MHz dB, 110 CH	Noise Figure @ 750 MHz dB Max	Package/ Style
MHW7182B	18.5	110	+40	–63(39)	– 66	– 64	6.5	714Y/1
MHW7222A	21.5	110	+40	–57(39)	– 60	– 60	7.0	714Y/1
MHW7222B(46b)	21.9	110	+40	–60(39)	– 61	– 60	6.5	1302/1
MHW7242B★	24	110	+40	–62(39)	– 63	– 58	7.0	714Y/1
MHW7272A	27.2	110	+40	–64(39)	– 64	– 60	6.5	714Y/1
MHW7292	29	110	+40	–60(39)	– 60	– 60	6.5	714Y/1
Power Doubling Hybrids								
MHW7185CL(23)	18.5	110	+44	–64(36)	–61	–63	7.5	714Y/1
MHW7185C	18.8	110	+44	–64(36)	–62	–63	7.5	714Y/1
MHW7205CL(27)	19.5	110	+44	–63(36)	–61	–62	7.5	714Y/1
MHW7205C	19.8	110	+44	–63(36)	–61	–62	7.5	714Y/1

(14)Mirror Amplifier Version of MHW8185
(21)Low DC Current Version of MHW8185; Typical I_{CC} @ Vdc = 24 V is 365 mA.
(22)Low DC Current Version of MHW8205; Typical I_{CC} @ Vdc = 24 V is 365 mA.
(23)Low I_{CC} Version of MHW7185C; Typical I_{CC} @ Vdc = 24 V is 365 mA.
(24)Mirror Amplifier Version of MHW8205
(27)Low I_{CC} Version of MHW7205C; Typical I_{CC} @ Vdc = 24 V is 365 mA.
(28)Mirror Amplifier Version of MHW8185L
(29)Mirror Amplifier Version of MHW8205L
(36)Composite 2nd order; V_{out} = +44 dBmV/ch
(39)Composite 2nd order; V_{out} = +40 dBmV/ch
(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00
★New Product

40–550 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 550 MHz dB Max	Package/ Style
			Output Level	2nd Order Test	Composite Triple Beat dB	Cross Modulation dB		
			dBmV	dB	77 CH	77 CH		
MHW6182T(46b)	18.2	77	+44	–72(35)	–58	–57	7.0	1302/1
MHW6222T(46b)	22	77	+44	–66(35)	–57	–57	6.0	1302/1
MHW6272T(46b)	27	77	+44	–64(35)	–57	–57	6.5	1302/1
MHW6342T	34.5	77	+44	–64(35)	–57	–57	6.5	1302/1
Power Doubling Hybrids								
MHW6185T(46b)	18.5	77	+44	–65(36)	–65	–68	7.5	1302/1

Reverse Amplifiers

5–200 MHz Hybrids, V_{CC} = 24 Vdc, Class A – 22 CH, 26 CH

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications						Noise Figure @ 175 MHz dB Max	Package/ Style
			Output Level	2nd Order Test(30)	Composite Triple Beat dB		Cross Modulation dB			
			dBmV	dB	22 CH	26 CH	22 CH	26 CH		
MHW1224	22	22	+50	–72	–69	–68.5(19)	–62	–62(19)	5.5	714Y/1
MHW1244	24	22	+50	–72	–68	–67.5(19)	–61	–61(19)	5.0	714Y/1

5–200 MHz Hybrids, V_{CC} = 24 Vdc, Class A – 6 CH, 10 CH

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications							Noise Figure @ 200 MHz dB Max	Package/ Style
			Output Level	2nd Order Test dB		Composite Triple Beat dB		Cross Modulation dB			
			dBmV	6 CH	10 CH	6 CH	10 CH	6 CH	10 CH		
MHW1224LA(34,46b)	22	6,10	50	TBD	TBD	–74	TBD	–64	TBD	4.9	1302/1
MHW1254LA(34,46b)	25	6,10	50	TBD	TBD	–75	TBD	–65	TBD	6.1	1302/1
MHW1304LA(34,46b)	30	6,10	50	TBD	TBD	–74	TBD	–64	TBD	4.9	1302/1
MHW1354LA(34,46b)	35	6,10	50	TBD	TBD	–73	TBD	–63	TBD	5.8	1302/1

(19)Typical
(30)Channels 2 and A @ 7
(34)Specifications are preliminary.
(35)Channels 2 and M30 @ M39
(36)Composite 2nd order; V_{out} = +44 dBmV/ch
(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

CATV Distribution: Reverse Amplifiers (continued)

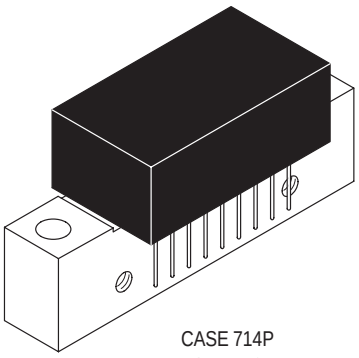
Low Current Amplifiers — 5–50 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	I_{DC} mA Max	Maximum Distortion Specifications				Noise Figure @ 50 MHz dB Max	Package/ Style
				Output Level dBmV	2nd Order Test(30) dB	Composite Triple Beat dB 4 CH	Cross Modulation dB 4 CH		
MHW1254L	25	4	135	+50	–70	–70	–62	4.5	714Y/1
MHW1304L	30	4	135	+50	–70	–66	–57	4.5	714Y/1

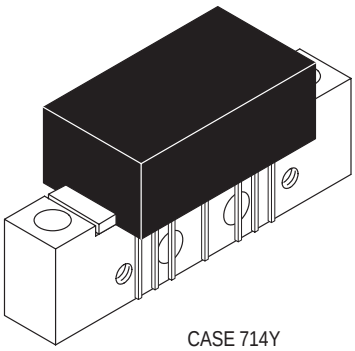
(19)Typical

(30)Channels 2 and A @ 7

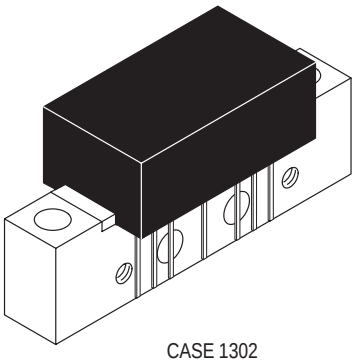
RF CATV Distribution Amplifiers Packages



CASE 714P
STYLE 2



CASE 714Y
STYLE 1, 2



CASE 1302
STYLE 1

Chapter Two
RF Front End ICs

Section One 2.1–0
RF Front End ICs – Selector Guide

Section Two 2.2–0
RF Front End ICs – Data Sheets

Section One
Selector Guide

RF Front End ICs

Motorola's RF Front End integrated circuit devices provide an integrated solution for the personal communications market. These devices are available in plastic SO–8, SO–16, SOT–143, TSSOP–16, TSSOP–16EP, Micro–8, TSSOP–20EP, LQFP–48 or PFP–16 packages.

Evaluation Boards

Evaluation boards are available for RF Front End Integrated Circuits. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

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RF Front End ICs	2.1–1
RFICs	2.1–2
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Upconverters/Exciters	2.1–2
Power Amplifiers	2.1–2
RF Building Blocks	2.1–3
Amplifiers	2.1–3
Mixers	2.1–3
Packages	2.1–4

RF Front End ICs

RFICs

Downconverters

Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	LNA Gain dB (Typ)	LNA NF dB (Typ)	Mixer Conv. Gain dB (Typ)	Mixer NF dB (Typ)	Case No./ Package	System Applicability
MC13142[18b]	DC to 1800	2.7 to 6.5	13.5	17	1.8	–3.0	12	751B/ SO–16	ISM, Cellular, PCS

Upconverters/Exciters

Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current mA (Typ)	Conv. Gain dB (Typ)	Output IP3 dBm (Typ)	Case No./ Package	System Applicability
MRFIC0954[18b]	800 to 1000	2.7 to 5.0	65	5.0	31	28	948M/ TSSOP–20EP	CDMA, TDMA, ISM
MRFIC1813[18b]	1700 to 2000	2.7 to 4.5	25	0.1	15	11	948C/ TSSOP–16	DCS1800, PCS
MRFIC1854[18b]	1700 to 2000	2.7 to 5.0	70	5.0	31	23	948M/ TSSOP–20EP	CDMA, TDMA, PCS

Power Amplifiers

Device	Freq. Range MHz	Supply Volt. Range Vdc	Saturated P_{out} dBm (Typ)	PAE % (Typ)	Gain P_{out}/P_{in} dB (Typ)	Case No./ Package	System Applicability
MRFIC0917[18e]	800 to 1000	2.7 to 5.5	34.5	45	22.5	978/PFP–16	GSM
MRFIC0919[18b]★	800 to 1000	3.0 to 5.5	35.3	48	32.3	948L/ TSSOP–16EP	GSM
MRFIC1817[18e]	1700 to 2000	2.7 to 5.0	33.5	42	30.5	978/PFP–16	DCS1800, PCS
MRFIC1818[18e]	1700 to 2000	2.7 to 6.0	34.5	42	31.5	978/PFP–16	DCS1800, PCS
MRFIC1819[18b]★	1700 to 2000	3.0 to 5.0	33	40	27	948L/ TSSOP–16EP	DCS1800, PCS
MRFIC1856[18b]★	800 to 1000	3.0 to 5.6	32	50	32	948M/ TSSOP–20EP	TDMA, CDMA, AMPS
	1700 to 2000		30	35	30		TDMA, CDMA, PCS

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

★New Product

RF Building Blocks

Amplifiers

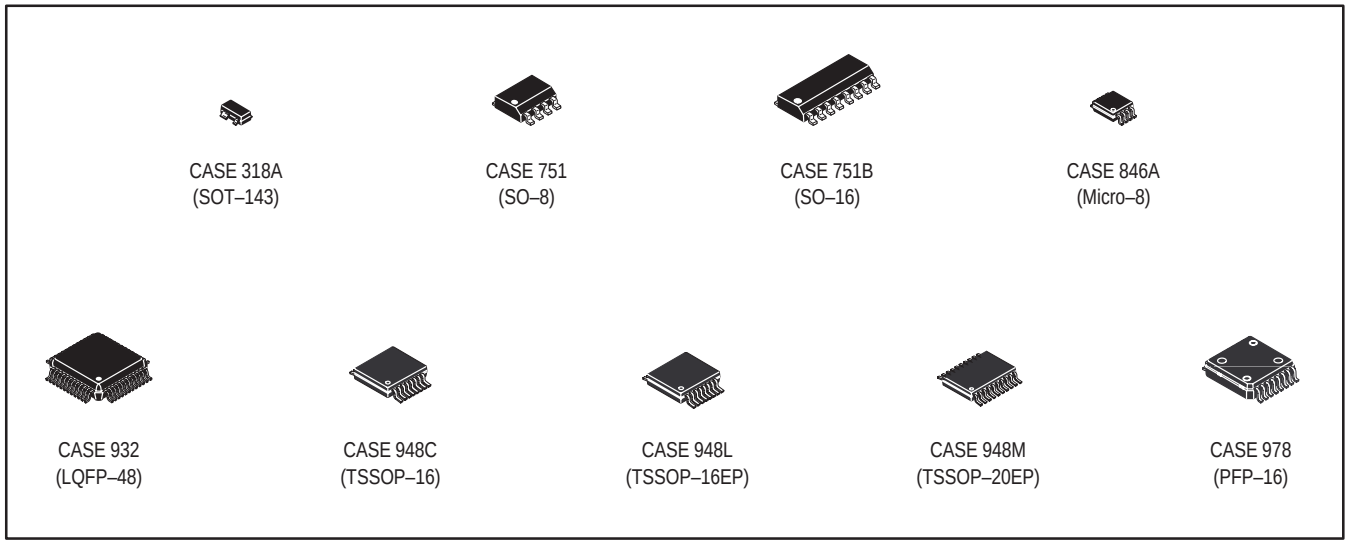
Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current μA (Typ)	Small Signal Gain dB (Typ)	Output IP3 dBm (Typ)	NF dB (Typ)	Case No./ Package	System Applicability
MC13144[18b]	100 to 2000	1.8 to 6.0	8.5	1	17	12	1.4	751/SO–8	ISM, PCS, Cellular
MRFIC0915[18c]	100 to 2500	2.7 to 5.0	2.0	–	16.2	4.0	1.9	318A/ SOT–143	ISM, PCS, Cellular
MRFIC0916[18c]	100 to 2500	2.7 to 5.0	4.7	–	18.5	11	1.9	318A/ SOT–143	ISM, PCS, Cellular
MRFIC0930DM[18b]	800 to 1000	2.7 to 4.5	8.5	20	19	10	1.7	846A/ Micro–8	GSM, AMPS, ISM
MRFIC1501[18b]	1000 to 2000	3.0 to 5.0	5.9	–	18	10	1.1	751/SO–8	GPS
MRFIC1808DM[18b]	1700 to 2100	2.7 to 4.5	5.0	8.0	18	13	1.6	846A/ Micro–8	DCS1800, PCS
MRFIC1830DM[18b]	1700 to 2100	2.7 to 4.5	9.0	20	18.5	8.5	2.1	846A/ Micro–8	DCS1800, PCS

Mixers

Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current μA (Typ)	Conv. Gain dB (Typ)	Input IP3 dBm (Typ)	Case No./ Package	System Applicability
MC13143[18b]	DC to 2400	1.8 to 6.0	4.1	–	–2.6	16	751/SO–8	ISM, PCS, Cellular

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

RF Front End Integrated Circuit Packages



Section Two

RF Front End ICs – Data Sheets

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RFICs	
Downconverters	
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MRFIC1813	2.2–95
MRFIC1854	2.2–139
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MRFIC0919	2.2–55
MRFIC1817	2.2–108
MRFIC1818	2.2–116
MRFIC1819	2.2–124
MRFIC1856	2.2–148
MRFIC2006	2.2–149
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MRFIC0916	2.2–39
MRFIC0930	2.2–65
MRFIC1501	2.2–81
MRFIC1808	2.2–88
MRFIC1830	2.2–134
Mixers	
MC13143	2.2–16

MOTOROLA

MC13142

Advance Information

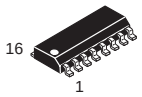
Low Power DC – 1.8 GHz LNA, Mixer and VCO

The MC13142 is intended to be used as a first amplifier, voltage controlled oscillator and down converter for RF applications. It features wide band operation, low noise, high gain and high linearity while maintaining low current consumption. The circuit consists of a Low Noise Amplifier (LNA), a Voltage Controlled Oscillator (VCO), a buffered oscillator output, a mixer, an Intermediate Frequency amplifier (IF_{amp}) and a dc control section. The wide mixer IF bandwidth allows this part also to be used as an up converter and exciter amplifier.

- Wide RF Bandwidth: DC–1.8 GHz
- Wide LO Bandwidth: DC–1.8 GHz
- Wide IF Bandwidth: DC–1.8 GHz
- Low Power: 13 mA @ V_{CC} = 2.7 – 6.5 V
- High Mixer Linearity: $P_{i1.0\ dB}$ = 3.0 dBm
- Linearity Adjustment Increases IP_{3in} Up to 20 dBm
- Single–Ended 50 Ω Mixer Input
- Double Balanced Mixer Operation
- Open Collector Mixer Output
- Single Transistor Oscillator with Collector, Base and Emitter Pinned Out
- Buffered Oscillator Output

LOW POWER DC – 1.8 GHz LNA, MIXER and VCO

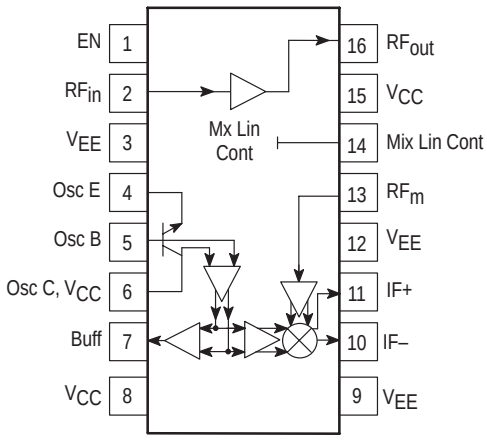
SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS

SO–16



This device contains 176 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13142D	T_A = –40° to +85°C	SO–16

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	7.0	Vdc
Operating Supply Voltage Range	V_{CC}	2.7 to 6.5	Vdc

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 V, T_A = 25°C, LO_{in} = –10 dBm @ 950 MHz, IF @ 50 MHz.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Disable) Pin 15 with Pin 1 @ 0 V Pin 10 and 11 with Pin 1 @ 0 V Pin 6 with Pin 1 @ 0 V	I_{CC_Total} I_{CC_15} I_{CC_Mix} I_{CC_6}	–230 –110 –20 –100	– – – –	230 110 20 100	µA
Supply Current (Enable) Pin 15 with Pin 1 @ 3.0 V Pin 10 with Pin 1 @ 3.0 V Pin 6 with Pin 1 @ 3.0 V	I_{CC_Total} I_{CC_15} I_{CC_Mix} I_{CC_6}	8.25 1.0 1.25 6.0	13.5 – – –	26 4.5 7.5 14	mA
Amplifier Gain (50 Ω Insertion Gain)	S_{21}	6.5	12	13	dB
Amplifier Reverse Isolation	S_{12}	–	–33	–	dB
Amplifier Input Match	$\Gamma_{in\ amp}$	–	–10	–	dB
Amplifier Output Match	$\Gamma_{out\ amp}$	–	–15	–	dB
Amplifier 1.0 dB Gain Compression	$Pin_{–1.0\ dB}$	–18	–15	–8.0	dBm
Amplifier Input Third Order Intercept	$IP3_{in}$	–	–5.0	–	dBm
Amplifier Noise Figure (Application Circuit)	NF	1.0	1.8	4.0	dB
Amplifier Gain @ N.F.	G_{NF}	–	17	–	dB
Mixer Voltage Conversion Gain (R_P = R_L = 800 Ω)	VG_C	–	9.0	–	dB
Mixer Power Conversion Gain (R_P = R_L = 800 Ω)	PG_C	–7.0	–3.0	–2.0	dB
Mixer Input Match	$\Gamma_{in\ M}$	–	–20	–	dB
Mixer SSB Noise Figure	NF_{SSBM}	–	12	–	dB
Mixer 1.0 dB Gain Compression	$Pin_{–1.0\ dBM}$	–	3.0	–	dBm
Mixer Input Third Order Intercept	$IP3_{InM}$	–	–1.0	–	dBm
Oscillator Buffer Drive (50 Ω)	P_{VCO}	–19.5	–16	–12	dBm
Oscillator Phase Noise @ 25 kHz Offset	N_Φ	–	–90	–	dBc/Hz
RF_{in} Feedthrough to RF_m	$P_{RFin–RFm}$	–	–35	–	dB
RF_{out} Feedthrough to RF_m	$P_{RFout–RFm}$	–	–35	–	dB
LO Feedthrough to IF	$P_{LO–IF}$	–	–35	–	dBm
LO Feedthrough to RF_{in}	$P_{LO–RFin}$	–	–35	–	dBm
LO Feedthrough to RF_m	$P_{LO–RFm}$	–	–35	–	dBm
Mixer RF Feedthrough to IF	$P_{RFm–IF}$	–	–25	–	dB
Mixer RF Feedthrough to RF_{in}	$P_{RFm–RFin}$	–	–25	–	dB

CIRCUIT DESCRIPTION

General

The MC13142 is a low power LNA, double–balanced Mixer, and VCO. This device is designated for use as the frontend section in analog and digital FM systems such as Digital European Cordless Telephone (DECT), PHS, PCS, Cellular, UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services and 902 to 928 MHz cordless telephones. It features a mixer linearity control to preset or auto program the mixer dynamic range, an enable function and a wideband IF so the IC may be used either as a down converter or an up converter. Further details are covered in the Pin by Pin Description which shows the equivalent internal circuit and external circuit requirements.

Current Regulation/Enable

Temperature compensating voltage independent current regulators are controlled by the enable function in which “high” powers up the IC.

Low Noise Amplifier (LNA)

The LNA is internally biased at low supply current (approximately 2.0 mA emitter current) for optimal noise figure and gain. The LNA output is biased internally with a 600 Ω resistor to V_{CC}. Input and output matching may be achieved at various frequencies using few external components. Matching the LNA for Maximum stable gain (MSG) yields noise performance within a few tenths of a dB of the minimum noise figure.

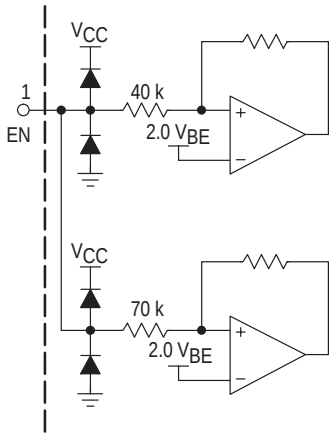
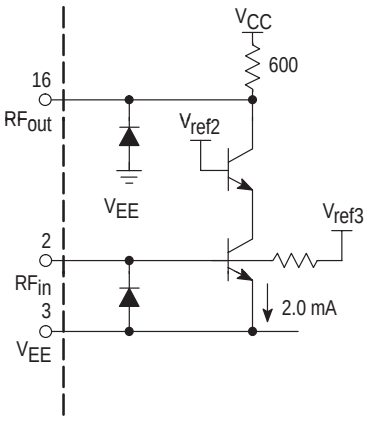
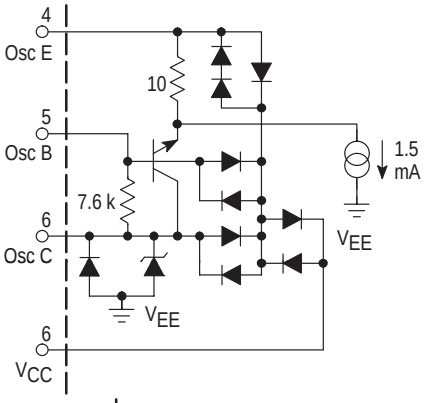
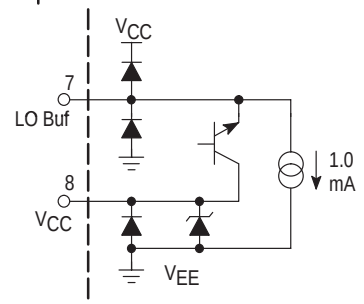
Mixer

The mixer is a double–balanced four quadrant multiplier biased class AB allowing for programmable linearity control via an external current source. An input third order intercept point of 20 dBm may be achieved. All 3 ports of the mixer are designed to work up to 1.8 GHz. The mixer has a 50 Ω single–ended RF input and open collector differential IF outputs. An on–board Local Oscillator transistor has the emitter, base and collector pinned out to implement a low phase noise VCO in various configurations. Additionally, a buffered LO output is provided for operation with a frequency synthesizer. The linear gain of the mixer is approximately 0 dB with a SSB noise figure of 12 dB in the IF output circuit configuration shown in the application example.

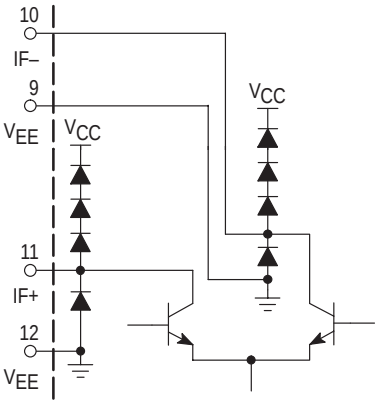
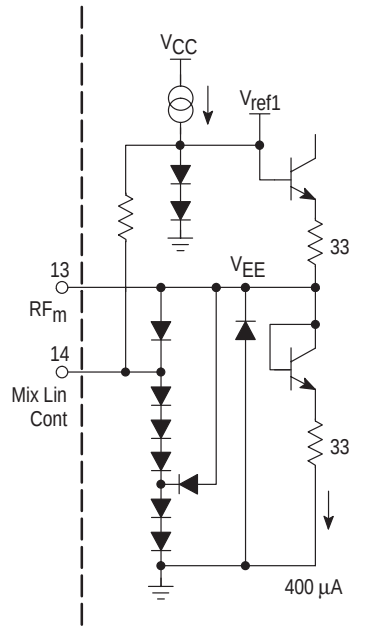
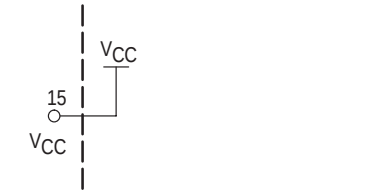
Local Oscillator

The on–chip transistor operates with coaxial transmission line or LC resonant elements to over 2.0 GHz. Biasing is done with a temperature compensated current source in the emitter and a collector to base internal resistor of 7.6 kΩ; however, an RFC from V_{CC} to base is recommended. The application circuit shows a voltage controlled Clapp oscillator operating at center frequency of 975 MHz.

PIN FUNCTION DESCRIPTION

Pin 16 Pin SOIC	Symbol	Equivalent Internal Circuit (20 Pin LQFP)	Description
1	EN		**Enable, E Osc** In SO–16, both enables, (for the Oscillator/LO Buffer and LNA/Mixer) are bonded to Pin 1. Enable by pulling up to V_{CC} or to greater than 2.0 V_{BE}.
2	RF_{in}		**RF Input** The input is the base of an NPN low noise amplifier. Minimum external matching is required to optimize the input return loss and gain.
3	V_{EE}		**V_{EE} – Negative Supply** V_{EE} pin is taken to an ample dc ground plane through a low impedance path. The path should be kept as short as possible. A two sided PCB is implemented so that ground returns can be easily made through via holes.
16	RF_{out}		**RF Output** The output is from the collector of the LNA; it is internally biased with a 600 Ω resistor to V_{CC}. As shown in the 926 MHz application receiver the output is conjugately matched with a shunt L, and series L and C network.
4 5 6	Osc E Osc B Osc C		**On–Board VCO Transistor** The transistor has the emitter, base and collector + V_{CC} pins available. Internal biasing which is compensated for stability over temperature is provided. It is recommended that the base pin is pulled up to V_{CC} through an RFC chosen for the particular oscillator center frequency. The application circuit shows a modified Colpitts or Clapp oscillator configuration and its design is discussed in detail in the application section.
6 8	V_{CC} V_{CC}		**Supply Voltage (V_{CC})** Two V_{CC} pins are provided for the Local Oscillator and LO Buffer Amplifier. The operating supply voltage range is from 2.7 Vdc to 6.5 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as feasible to minimize inductive reactances along the trace. V_{CC} should be decoupled to V_{EE} at the IC pin as shown in the component placement view.
7	LO Buff		**Local Oscillator Buffer** This is a buffered output providing –16 dBm (50 Ω termination) to drive the f_{in} pin of a PLL synthesizer. Impedance matching to the synthesizer may be necessary to deliver the optimal signal and to improve the phase noise performance of the VCO.

PIN FUNCTION DESCRIPTION (continued)

Pin 16 Pin SOIC	Symbol	Equivalent Internal Circuit (20 Pin LQFP)	Description
9, 12	V_{EE}		**V_{EE}, Negative Supply** These pins are V_{EE} supply for the mixer IF output. In the application PC board these pins are tied to a common V_{EE} trace with other V_{EE} pins.
10, 11	IF–, IF+		**IF Output** The IF is a differential open collector configuration which designed to use over a wide frequency range for up conversion as well as down conversion. Differential to single–ended circuit configuration and matching options are discussed in the application section. 6.0 dB of additional Mixer gain can be achieved by conjugately matching at the desired IF frequency.
13	RF_m		**Mixer RF Input** The mixer input impedance is broadband 50 Ω for applications up to 1.8 GHz. It easily interfaces with a RF ceramic filter as shown in the application schematic.
14	Mix Lin Cont		**Mixer Linearity Control** The mixer linearity control circuit accepts approximately 0 to 2.3 mA control current to set the dynamic range of the mixer. An Input Third Order Intercept Point, IIP3 of 20 dBm may be achieved at 2.3 mA of control current (approximately 7.0 mA of additional supply current).
15	V_{CC}		**V_{CC}, Power Supply**

APPLICATIONS INFORMATION

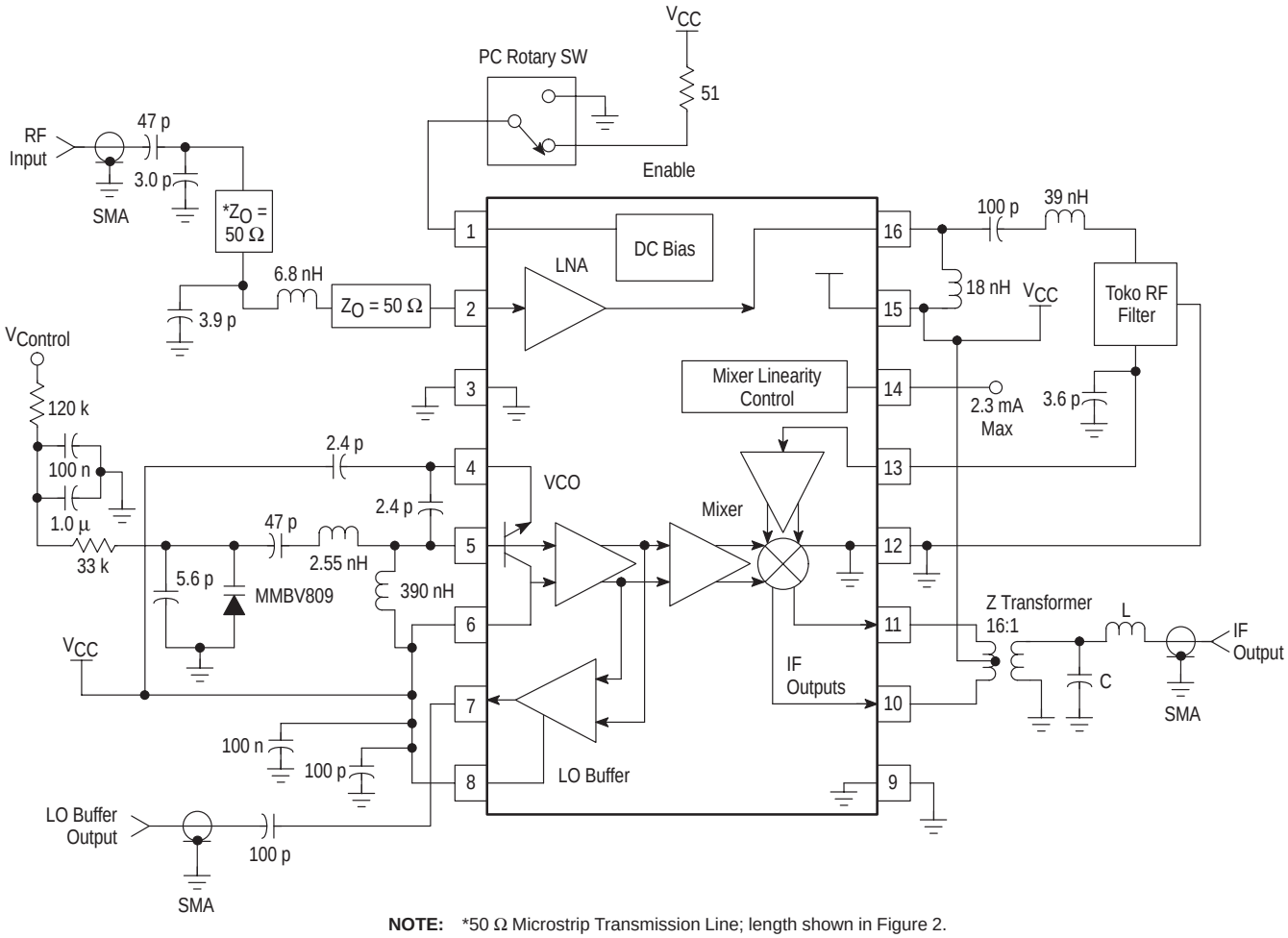
Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The PC board accommodates all SMT components on the circuit side (see Circuit Side Component Placement View). This evaluation board will be discussed and referenced in this section.

Component Selection

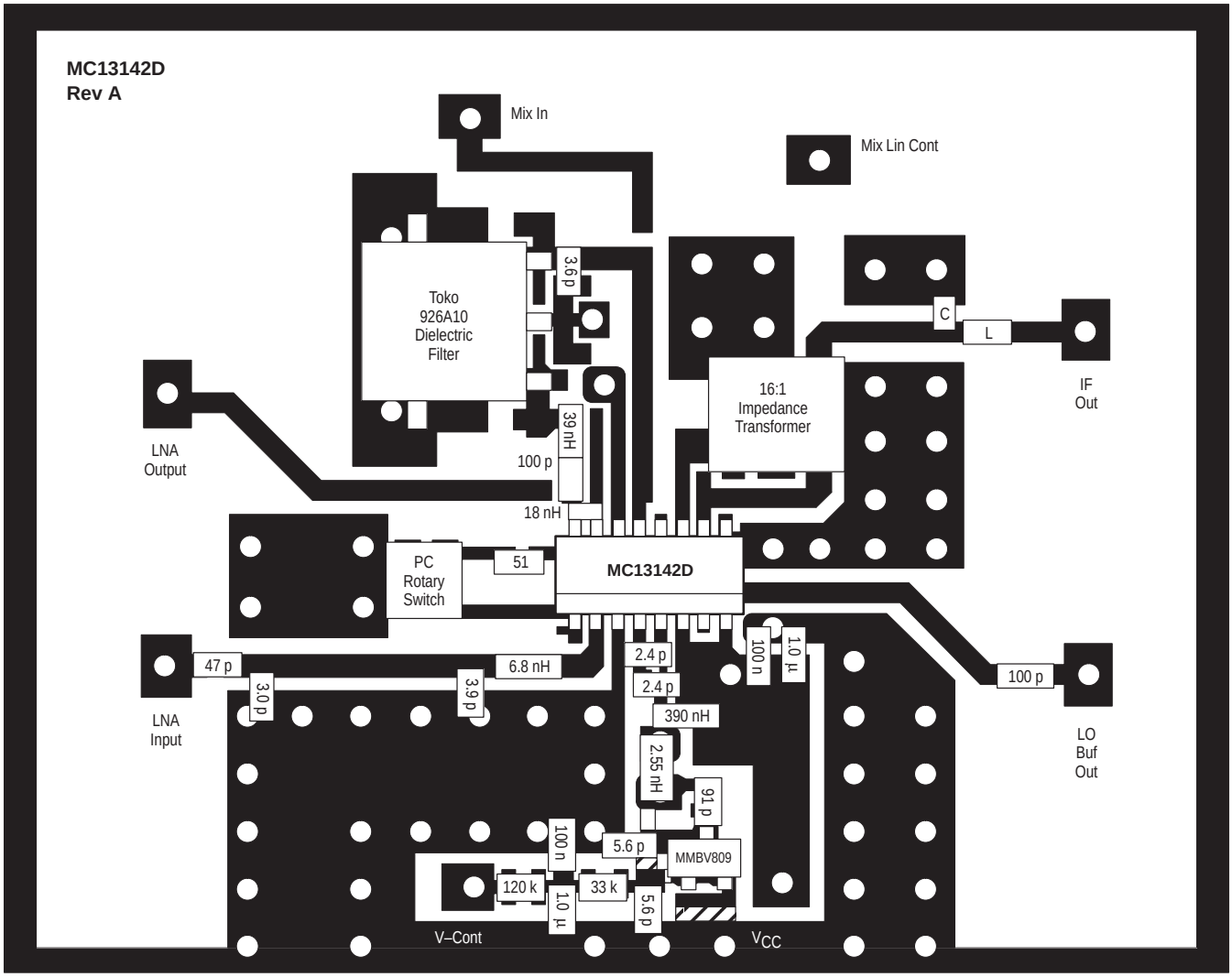
The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers. The circuit side placement view is illustrated for the components specified in the application circuit. The application circuit schematic specifies particular components that were used to achieve the results given and specified in the tables but alternate components of the same Q and value should give equivalent results.

Figure 1. Application Circuit
(926.5 MHz)



NOTE: *50 Ω Microstrip Transmission Line; length shown in Figure 2.

Figure 2. 900 MHz Circuit Side Component Placement View



NOTES: The PCB is laidout for the 4DFA (2 pole SMD type) and 4DFB (3 pole SMD type) filters which are available for applications in cellular and GSM,GPS (1.2–1.5 GHz), DECT, PHS and PCS (1.8–2.0 GHz) and ISM Bands (902–928 MHz and 2.4–2.5 GHz). In the component placement shown above, the 926.5 MHz dielectric type image filter is used (Toko Part # 4DFA–926A10).

The PCB also accommodates a surface mount SAW filter in an eight or six pin ceramic package for the cellular base and handset frequencies. Recommended manufacturers are Siemens and Murata.

Traces are provided on the PCB to evaluate the LNA and mixer separately. The component placement view shows external circuit components used for the 926.5 MHz application circuit. Note: some traces must be cut to accommodate placement of components; likewise some traces must be shorted. The voltage controlled oscillator is shown with the varactor referenced to V_{EE} ground. The PCB is modified as shown to do this.

16:1 broadband impedance transformer is mini circuits part #TX16–R3T; it is in the leadless surface mount “TX” package. Components L and C comprise a low pass filter used to provide narrowband matching at a given IF frequency. For example at 49 MHz C = 36 p and L = 330 nH.
The microstrip trace on the ground side of the PCB is intended for a microstrip resonator; it is cut free when using a lump inductor as done above.

Input Matching/Components

It is desirable to use a RF ceramic or SAW filter before the mixer to provide image frequency rejection. The filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 3.0 to 5.0 dB insertion loss. The PC board layout accommodates both ceramic and SAW RF filters which are offered by various suppliers such as Siemens, Toko and Murata.

Interface matching between the LNA, RF filter and the mixer will be required. The interface matching networks shown in the application circuit are designed for 50 Ω interfaces.

In the application circuit, the LNA is conjugately matched to 50 Ω input and output for 3.0 to 5.0 Vdc V_{CC}. 17 dB gain and 1.8 dB noise figure is typical at 926 MHz. The mixer measures 0 dB gain and 12 dB noise figure as shown in the application circuit. Typical insertion loss of the Toko ceramic filter is 3.0 dB. Thus, the overall gain of the frontend receiver is 14 dB with a 3.3 dB noise figure.

System Noise Considerations

The block diagram shows the cascaded noise stages of the MC13142 in the frontend receiver subsystem; it represents the application circuit. In the cascaded noise analysis the system noise equation is:

Fsystem = F1 + [(F2 –1)/G1] + [(F3–1)]/[(G1)(G2)]

where:

F1 = the Noise Factor of the MC13142 LNA
G1 = the Gain of the LNA
F2 = the Noise factor of the RF Ceramic Filter
G2 = the Gain of the Ceramic Filter
F3 = the Noise factor of the Mixer

Note: the above terms are defined as linear relationships and are related to the log form for gain and noise figure by the following:

$F = \text{Log}^{-1}$ [(NF in dB)/10] and similarly
$G = \text{Log}^{-1}$ [(Gain in dB)/10].

Calculating in terms of gain and noise factor yields the following:

F1 = 1.51; G1 = 50.11
F2 = 1.99; G2 = 0.5
F3 = 15.85

Thus, substituting in the equation for system noise factor:

Fsystem = 2.12; NFsystem = 3.3 dB

Figure 3. Frontend Subsystem Block Diagram for Noise Analysis

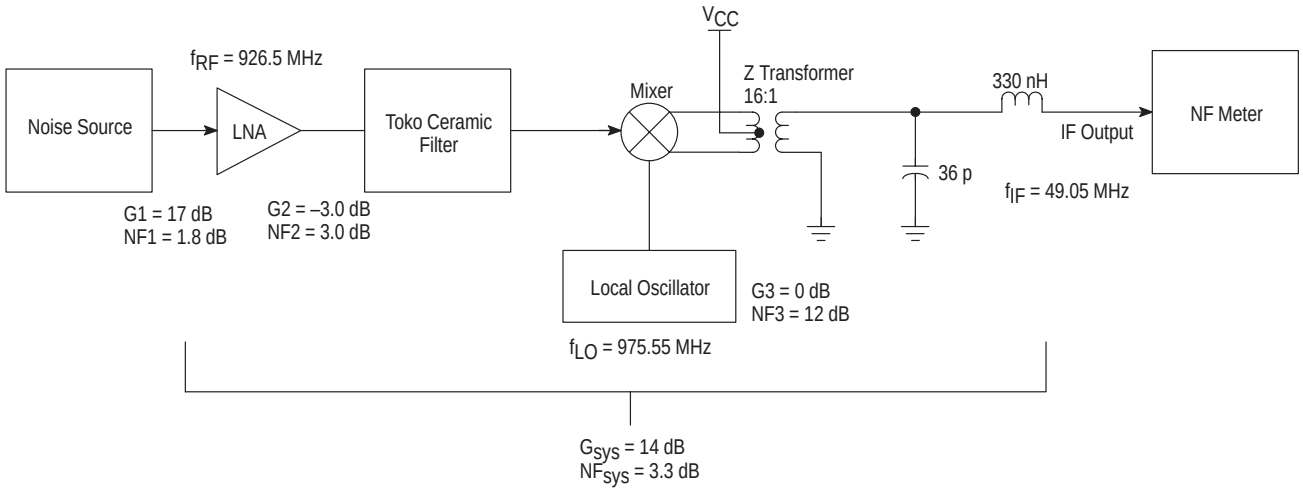
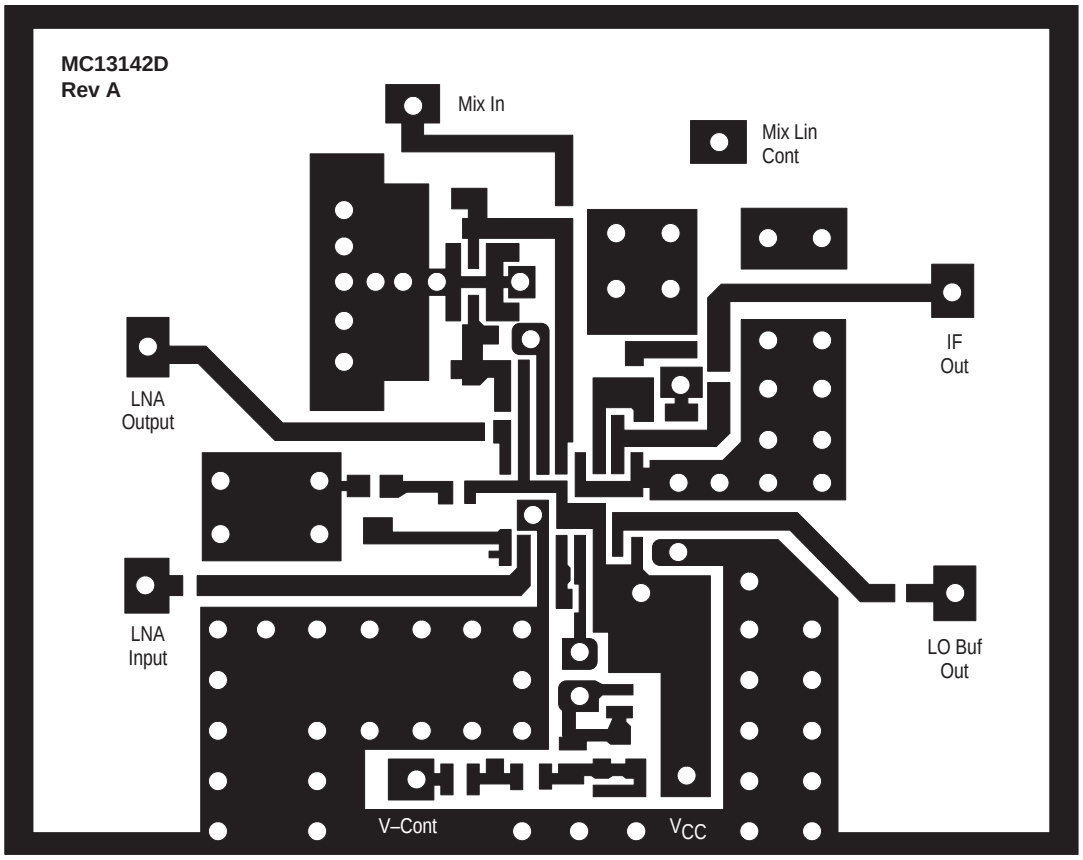
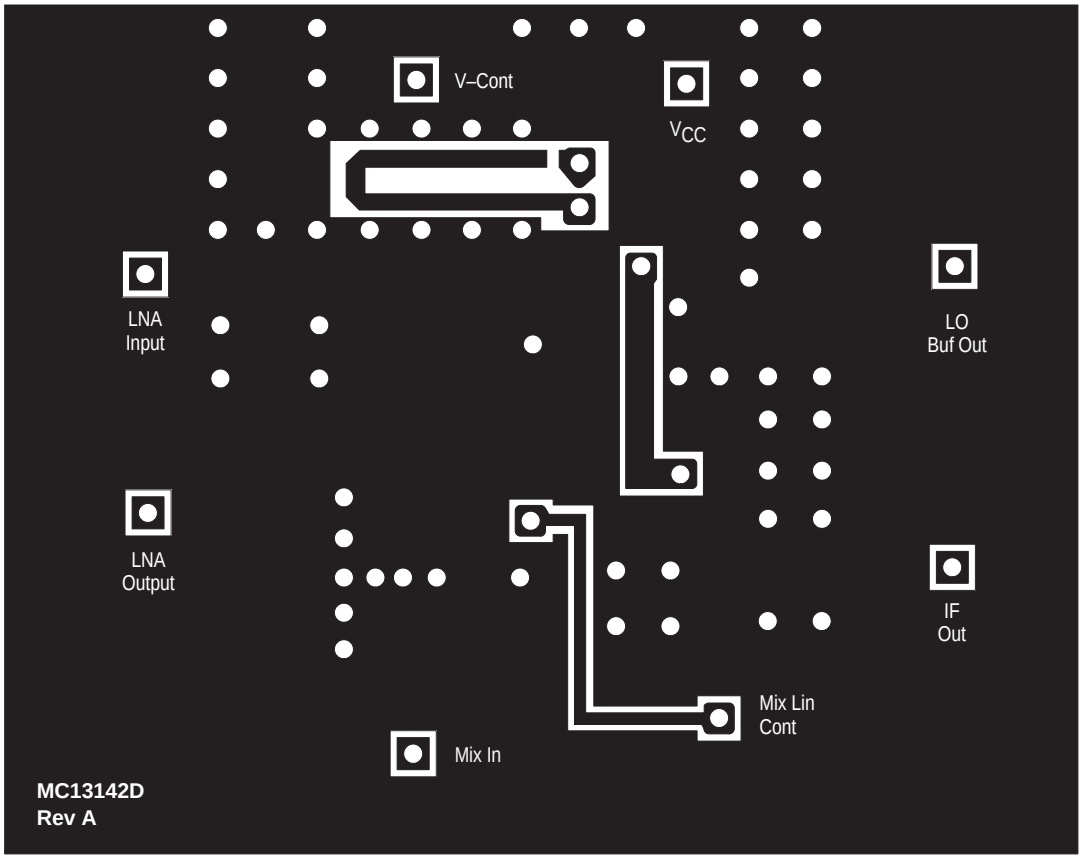


Figure 4. Circuit Side View



NOTES: Critical dimensions are 50 mil centers lead to lead in SO–16 footprint.
Also line widths to labeled ports excluding V_{CC} are 50 mil (0.050 inch).
FR4 PCB, 1/32 inch.

Figure 5. Ground Side View



NOTES: FR4 PCB, 1/32 inch.

1.9 GHz FRONT–END FOR WIRELESS SYSTEMS

This application is applicable to both Analog and Digital systems. With the correct VCO tuning and the appropriate filter, it will do the front–end for DECT, PHS or PCS. The MC13142D is available in a SOIC 16 pin package. The part requires minimal external components, leading to a low cost system. A circuit board layout with a circuit diagram to evaluate the IC is shown. Except for the PLL control, all the wireless systems front–ends will look the same and have the same basic performance characteristic as the test circuit.

Circuit Operation:

LNA Input/Output

An LC filter is incorporated before the LNA to provide some selectivity. In addition to selectivity, its other function is to match the antenna impedance (50 Ω) to the LNA input for best gain and sensitivity (low noise figure). The network reflects about a 200 Ω source impedance to the device.

The output circuit is a pie network consisting of; the LNA output capacity, the inductance (the bond wire, package pin and L2), and the input capacity of the dielectric filter, along with some added shunt. A 2.4 pF with Toko 4DFA 2 pole filter. The 2.4 pF is for matching the in–band filter impedance to the LNA output and has little effect on tuning.

Both networks are tuned to band center by adjusting L1 and L2. L1 and L2, as well as L3, are short length of wire formed in a half loop. Once the correct length is determined in centering the tuning range, adjustment is accomplished by moving the loop toward or away from some conductive surface such as a ground plane.

The dielectric filter is referenced to the dc supply which lessen the parts count and adds distributive capacity for high frequency bypassing. DC feed to the LNA is through a low value resistor (220 to 330 Ω) tapped at the filter input, so as not to load the circuit unnecessarily. There is a small voltage drop across the resistor, as well as some signal loss. The signal loss is about 0.73 dB for a 220 Ω resistor and less for larger values. If one can not afford the voltage drop, an inductor could replace the resistor at a somewhat increased cost.

Mixer

Looking from the dielectric filter's output, the Mixer input is 50 Ω in series with an inductor. This inductor consists of the printed circuit run, the package pin and bond wire, all in series. It is modified, to some extent, by the package pin distributive capacity, but overall at the bandpass frequency remains inductive. Matching the filter impedance to the Mixer input only requires a capacitor with a value that, when placed in series, will resonate with this inductor at the filter bandpass frequency.

The single–ended input signal is converted internally into balanced current signals. The two signals drive the two low impedance inputs (emitters) of a Gilbert Cell. They appear as

current sources to the Cell and can be programmed (via Pin 15) for more current. The current is often adjusted for minimum third order response. In this Fixture it is fixed biased for most conversion gain.

The Mixer circuit is balanced where both oscillator and RF are suppressed. This provides IF signals at Pins 9 and 10 which are equal in amplitude and 180 degrees out of phase. To realize a positive gain one needs to reflect a higher impedance from the load impedance (50 Ω for this fixture) to the Mixer output or outputs. Maximum signal transfer would require a balance to unbalance network. Center tapped tuned transformers can perform this function but are quite expensive. If one can afford 3.0 dB less signal, a simple LC circuit at one of the outputs will work well. The other output is unused and bypassed to ground.

The most gain is realized when no shunt capacity is added and L4 is selected to resonate with the terminal capacity. Adding shunt capacity will lower the gain and increase the circuit's bandwidth. A small value series capacitor C4 to the 50 Ω output will control the reflected impedance and complete the circuit. L4 and C4 will vary in value depending on the IF frequency.

VCO

The base of the device is the source for driving both the Gilbert cell and prescaler buffer stages. Because of this, the oscillator device will operate and drive the Mixer only in the grounded collector configuration. Additional dc bias is added through a 1.3 kΩ resistor (tapped for minimum VCO loading) to reduce the off–set between base and supply.

The external circuit is a modified Colpitts where the capacitance between base and emitter (Pins 4 and 5), along with a capacitor from emitter to ac ground, forms the circuit capacity and the feedback that sustains oscillations. The effective circuit inductance (looking from the top of the circuit, the transistor base) consist of L3 in series with varactor diode D1 and a blocking capacitor. This circuit must appear inductive for the VCO to operate properly. If the capacity is too small, the feedback ratio is reduced and the VCO can cease oscillating. When it becomes to large, it will not vary the frequency due to the limiting effect of the series loop capacitance.

In this application, the VCO is not required to cover a large tuning range. Limiting the tuning range to no more than is required to cover the band (making allowance for temperature and aging effects) will result in a VCO less susceptible to on board noise sources. To assure oscillation while controlling the tuning range the varactor (plus series capacitor) minimum capacity is chosen to be about equal to the capacity from Pin 5 (transistor base) to RF ground. The maximum tuning ratio could be no greater than 1.41 because the circuit capacity could only double whatever the upper value capacity the varactor attained. An upper limit on the varactor capacity along with the effects of the series capacitor reduces the VCO tuning range to about 1.2 times. The varactors chosen for the test fixtures were Loral KV2111.

The VCO buffer, as most emitter follower circuits, has the potential of generating a parasitic oscillation. When a collector is RF bypassed, a tuned LC circuit is formed consisting of the bypass capacitor, bond wire plus package pin inductance and the device effective output capacity. If the base is low impedance, there is normally enough distributive collector to emitter capacity for the device to oscillate in the common base mode. A simple fix without affecting the buffer otherwise, is to place a small value series resistor in the collector lead. This will lower the Q of the circuit where it cannot sustain oscillations. Without the series resistor at Pin 8 or some other damping element, the buffer will oscillate.

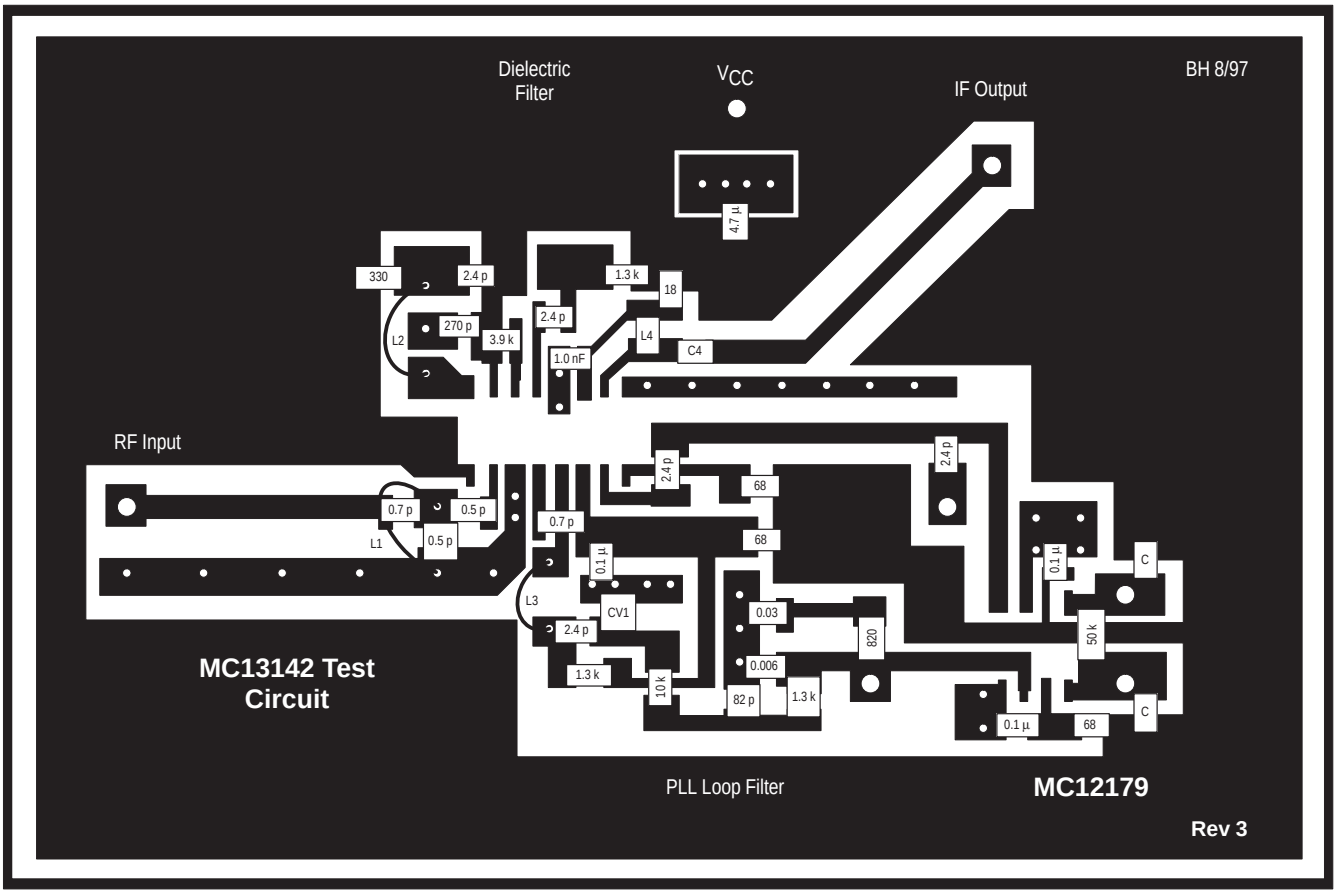
PLL

A phase lock loop is added to the test board to evaluate the VCO. The MC12179 multiplies the crystal reference frequency by 256 to obtain lock. In a frequency agile system, the MC12210 would control the VCO and its reference derived from a crystal. The crystal frequency would be selected to coincide with the required VCO frequencies and channels spacing requirements.

Expected Performance

As stated earlier, the MC13142 performance in any of the systems should mirror the performance obtained in the test fixture. Fixture power gains of 15 dBm and noise figures of 5.5 dB are typical. The Mixer current can be varied to enhances battery life as well as alter its output characteristic for peak performance of a desired or undesired response.

Figure 6. 1.9 GHz Circuit Component Placement View



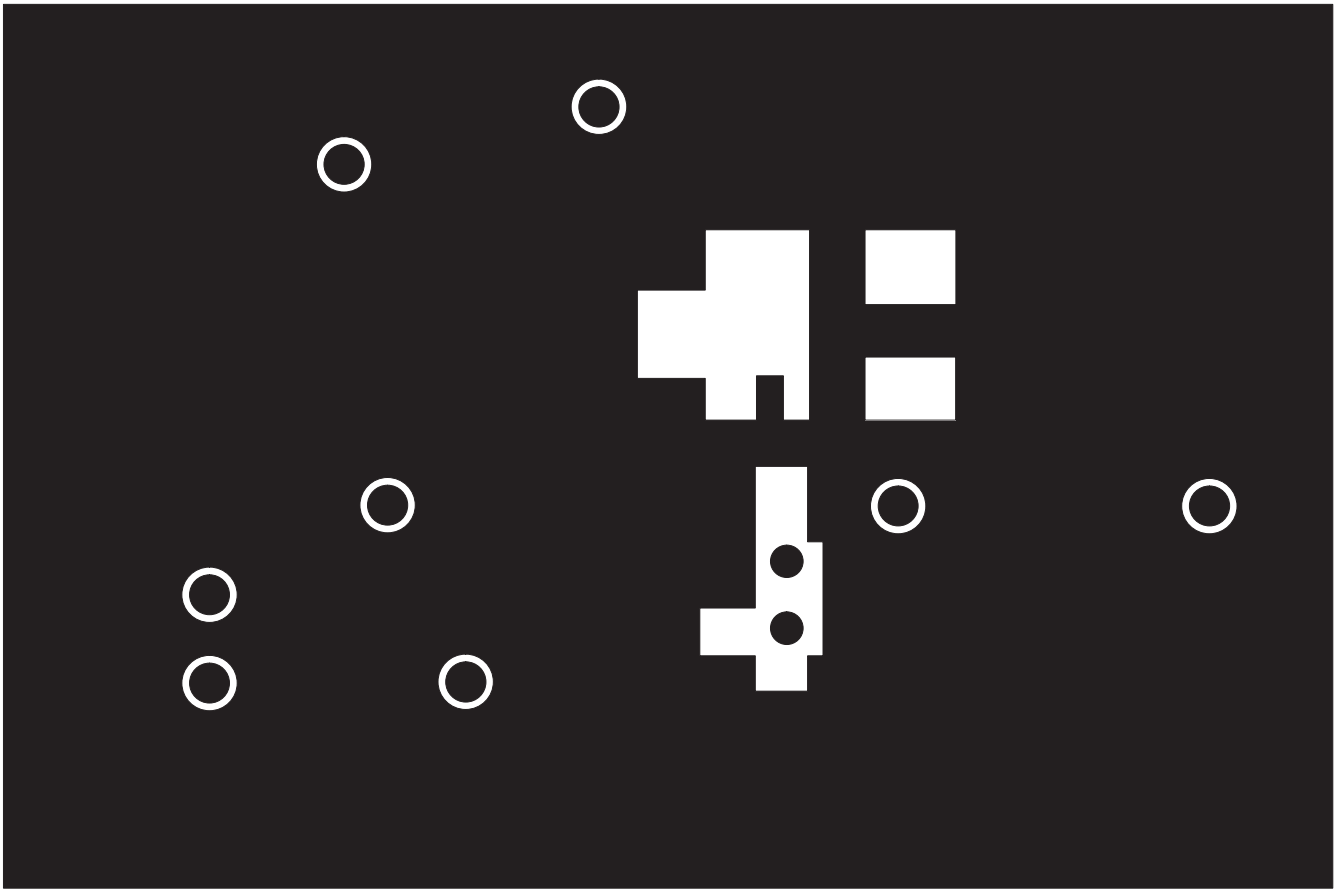
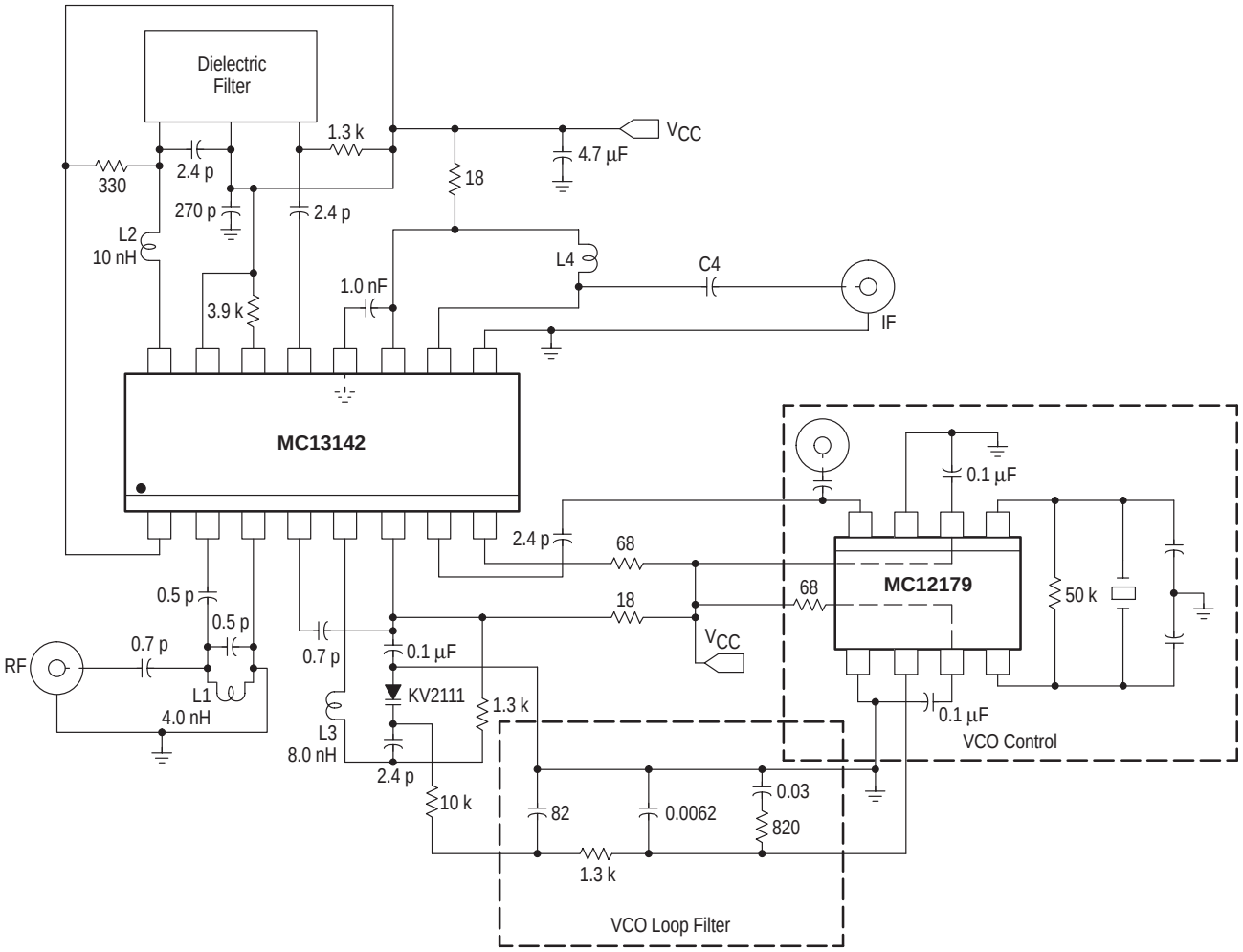


Figure 7. 1.9 GHz Application Circuit



MOTOROLA

Ultra Low Power DC – 2.4 GHz Linear Mixer

The MC13143 is a high compression linear mixer with single–ended RF input, differential IF output and differential LO inputs which consumes as little as 1.8 mW. A new circuit topology is used to achieve a high third order intermodulation intercept point, high linearity and high 1.0 dB output compression point while maintaining a linear 50 Ω input impedance. It is designed for Up or Down conversion anywhere from dc to 2.4 GHz.

Ultra Low Power: 1.0 mA @ V_{CC} = 1.8 to 6.5 V

- Wide Input Bandwidth: DC–2.4 GHz
- Wide Output Bandwidth: DC–2.4 GHz
- Wide LO Bandwidth: DC–2.4 GHz
- High Mixer Linearity: $P_{i1.0\ dB}$ = 3.0 dBm

Linearity Adjustment of up to IP_{3in} = 20 dBm

- 50 Ω Mixer Input
- Single–Ended Mixer Input
- Double Balanced Mixer Operation
- Differential Open Collector Mixer Output

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13143D	T_A = –40 to 85°C	SO–8

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

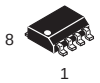
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}(max)	7.0	Vdc
Junction Temperature	T_{Jmax}	150	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C

NOTE: ESD data available upon request.

MC13143

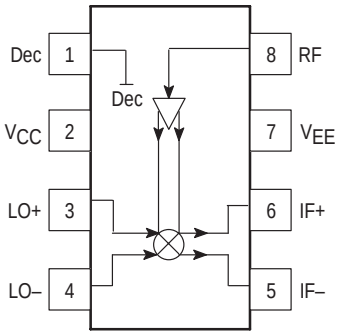
ULTRA LOW POWER DC – 2.4 GHz LINEAR MIXER

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

This device contains 29 active transistors.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	1.8	–	6.0	Vdc

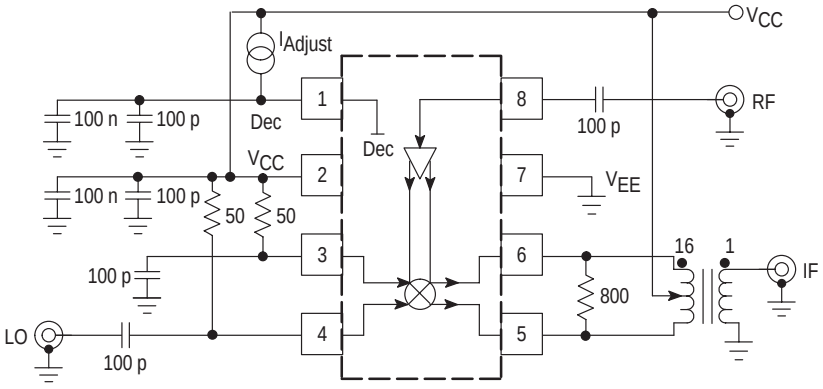
DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.0 V, f_{RF} = 1.0 GHz, Pin = –25 dBm.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Lin Control Current = 0)	I_{CC1}	–	1.0	–	mA
Supply Current (Lin Control Current = 1.6 mA)	I_{CC2}	–	4.1	–	mA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.0 V, f_{RF} = 1.0 GHz, Pin = –25 dBm.)

Characteristic	Symbol	Min	Typ	Max	Unit
Mixer Voltage Conversion Gain (R_P = R_L = 800 Ω)	VG_C	–	9.0	–	dB
Mixer Power Conversion Gain (R_P = R_L = 800 Ω)	PG_C	–3.5	–2.6	–1.5	dB
Mixer Input Return Loss	Γin_{mx}	–	–20	–	dB
Mixer SSB Noise Figure	NF_{SSB}	–	14	15	dB
Mixer 1.0 dB Compression Point (Mx Lin Control Current = 1.6 mA)	$Pin_{–1.0\ dB}$	–1	0	–	dBm
Mixer Input Third Order Intercept Point (d_f = 1.0 MHz, $I_{control}$ = 1.6 mA)	$IP3_{in}$	–	16	–	dBm
LO Drive Level	LO_{in}	–	–5.0	–	dBm
LO Leakage to Mixer IF Outputs	$P_{LO–IF}$	–	–33	–25	dB
Mixer Input Feedthrough Output	$P_{RFm–IF}$	–	–25	–	dB
LO Leakage to Mixer Input	$P_{LO–RFm}$	–	–40	–25	dB
Mixer Input Leakage to LO	$P_{RFm–LO}$	–	–35	–	dB

Figure 1. Test Circuit



TYPICAL PERFORMANCE CURVES

Figure 2. Power Conversion Gain and Supply Current versus Supply Voltage

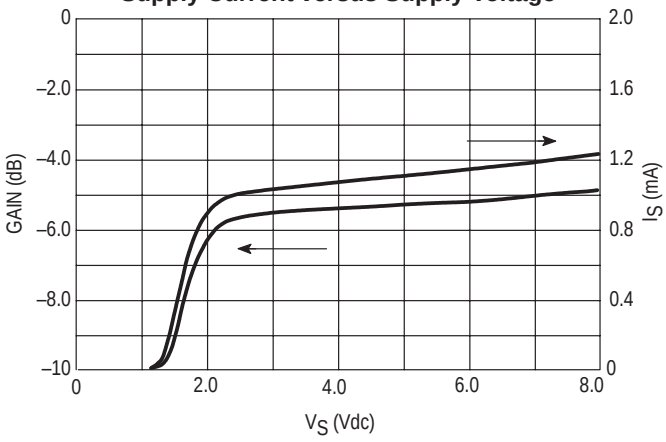


Figure 3. Noise Figure and Gain versus LO Power

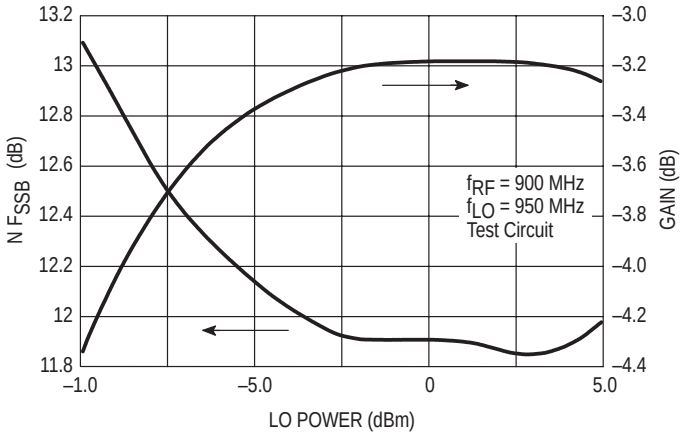


Figure 4. Mixer Input Return Loss versus RF Input Frequency

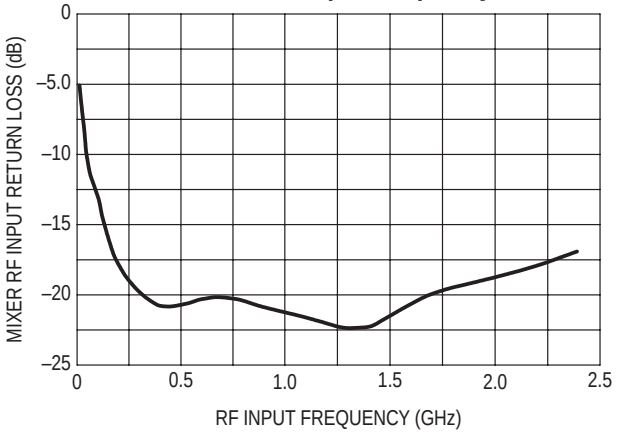


Figure 5. Power Conversion Gain and Supply Current versus RF Input Power

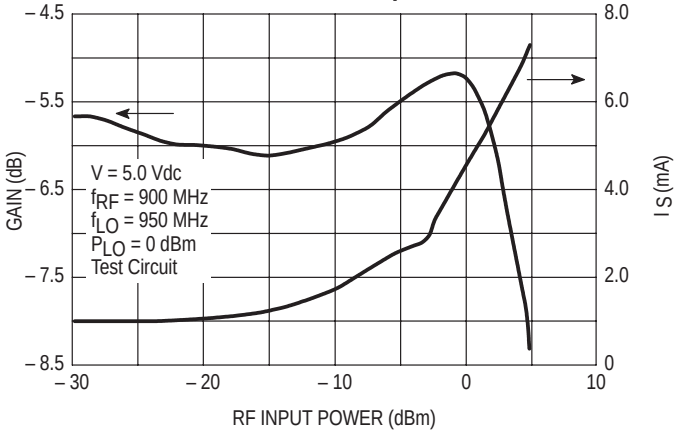


Figure 6. Noise Figure and Gain versus RF Frequency

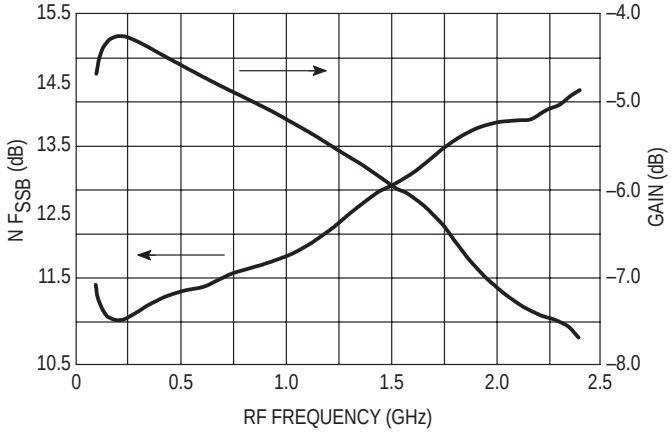


Figure 7. IIP3, Gain, Supply Current versus Mixer Linearity Control Current

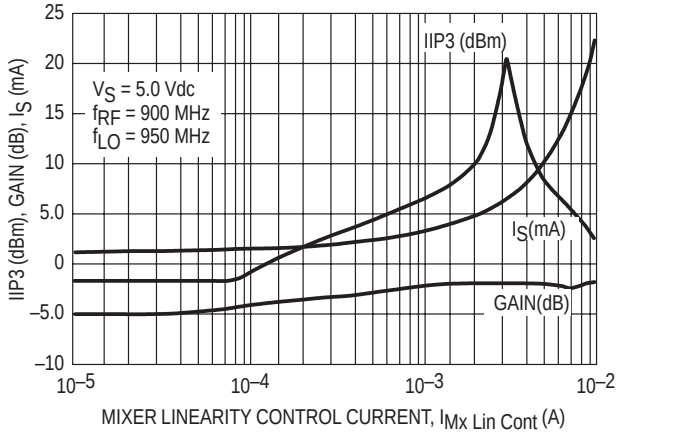


Table 1. Mixer Scattering Parameters
(V_{DD} = 3.0 V, T_A = 25°C, Mixer Enable = 3.0 V, 50 Ω System)

f (MHz)	RF Input S_{11}		IF Input S_{11}		LO Input S_{11}	
	$\|S_{11}\|$	ϕ	$\|S_{11}\|$	ϕ	$\|S_{11}\|$	ϕ
50	0.343	178.00	0.951	–1.73	0.420	–178.56
100	0.344	174.95	0.932	–2.81	0.436	–179.65
150	0.344	173.59	0.923	–3.81	0.445	178.10
200	0.339	172.00	0.913	–4.04	0.452	176.53
250	0.339	169.86	0.894	–4.43	0.452	174.69
300	0.338	167.81	0.874	–4.49	0.454	173.45
350	0.334	165.65	0.865	–3.83	0.461	171.72
400	0.329	163.54	0.857	–2.79	0.462	169.68
500	0.310	159.65	0.881	–1.19	0.453	165.85
600	0.287	157.53	0.912	–1.85	0.451	162.65
700	0.271	162.46	0.938	–3.58	0.435	160.21
800	0.274	164.71	0.948	–5.39	0.437	159.31
900	0.292	165.39	0.953	–7.24	0.445	156.21
1000	0.308	164.23	0.953	–9.35	0.441	153.57
1100	0.312	162.28	0.951	–11.39	0.429	151.50
1200	0.318	161.86	0.944	–13.30	0.437	152.31
1300	0.330	158.99	0.936	–15.62	0.455	148.48
1400	0.334	156.41	0.927	–17.82	0.473	146.94
1500	0.340	153.93	0.920	–21.62	0.490	141.96
1600	0.336	151.75	0.905	–26.05	0.493	140.27
1700	0.342	150.94	0.886	–30.44	0.495	134.93
1800	0.358	148.01	0.886	–36.09	0.497	133.41
1900	0.358	144.62	0.840	–41.80	0.506	129.67
2000	0.355	141.73	0.820	–46.92	0.510	126.17
2100	0.357	139.48	0.798	–53.04	0.511	122.55
2200	0.364	137.30	0.787	–59.14	0.516	119.69
2300	0.367	134.21	0.783	–63.19	0.520	116.45
2400	0.367	130.92	0.786	–67.03	0.511	111.51
2500	0.370	128.16	0.808	–69.65	0.494	109.01
2600	0.367	125.48	0.816	–73.04	0.483	107.63
2700	0.371	123.33	0.828	–73.38	0.487	107.26

CIRCUIT DESCRIPTION

General

The MC13143 is a double–balanced Mixer. This device is designated for use as the frontend section in analog and digital FM systems such as Wireless Local Area Network (LAN), Digital European Cordless Telephone (DECT), PHS, PCS, GPS, Cellular, UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services and 902 to 928 MHz cordless telephones. It features a mixer linearity control to preset or auto program the mixer dynamic range, an enable function and a wideband IF so the IC may be used either as a down converter or an up converter.

Current Regulation

Temperature compensating voltage independent current regulators provide typical supply current at 1.0 mA with no mixer linearity control current.

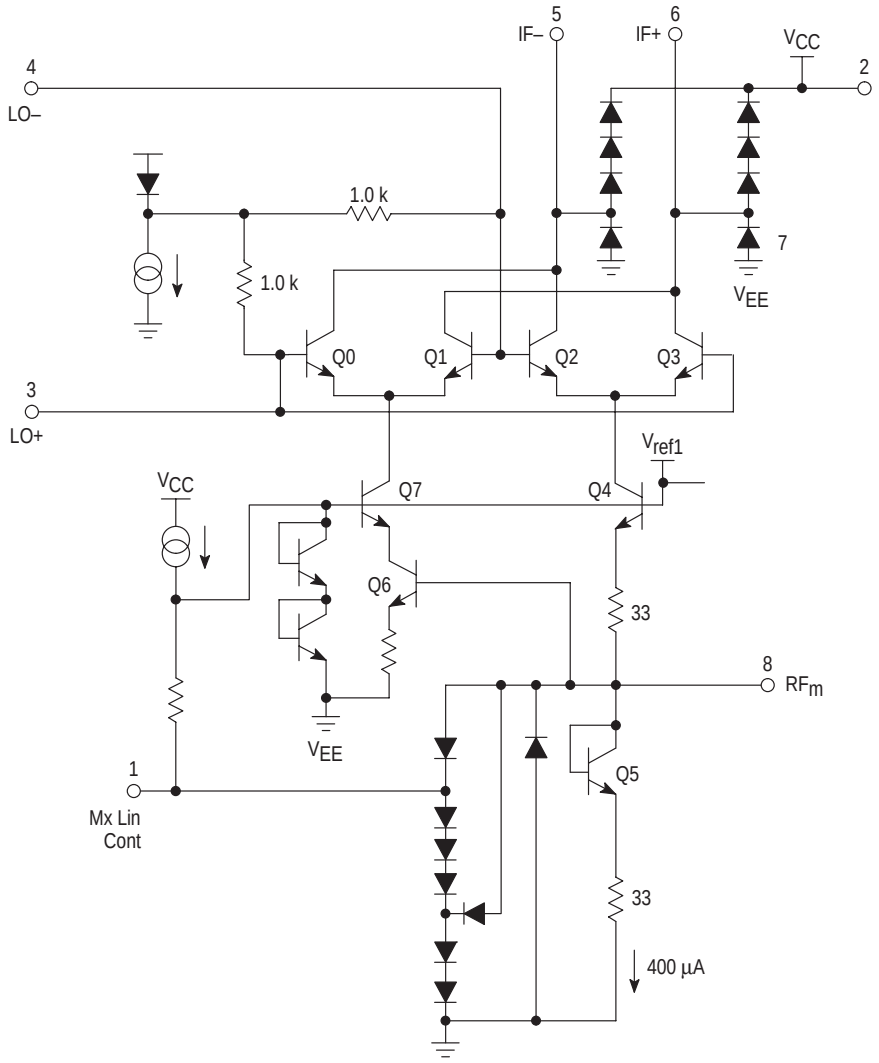
Mixer

The mixer is a unique and patented double–balanced four quadrant multiplier biased class AB allowing for programmable linearity control via an external current source. An input third order intercept point of 20 dBm may be achieved. All 3 ports of the mixer are designed to work up to 2.4 GHz. The mixer has a 50 Ω single–ended RF input and open collector differential IF outputs (see Internal Circuit Schematic for details). The linear gain of the mixer is approximately –5.0 dB with a SSB noise figure of 12 dB.

Local Oscillator

The local oscillator has differential input configuration that requires typically –10 dBm input from an external source to achieve the optimal mixer gain.

Figure 8. MC13143 Internal Circuit*



NOTE: * The MC13143 uses a unique and patented circuit topology.

APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The PC board is laid out to accommodate all SMT components on the circuit side (see Circuit Side Component Placement View).

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers. The circuit side placement view is illustrated for the components specified in the application circuit. The Component Placement View specifies particular components that were used to achieve the results shown in the typical curves and tables.

Mixer Input

The mixer input impedance is broadband 50 Ω for applications up to 2.4 GHz. It easily interfaces with a RF ceramic filter as shown in the application schematic.

Mixer Linearity Control

The mixer linearity control circuit accepts approximately 0 to 2.3 mA control current. An Input Third Order Intercept Point, IIP3 of 20 dBm may be achieved at 2.3 mA of control current (approximately 7.0 mA of additional supply current).

Local Oscillator Inputs

The differential LO inputs are internally biased at V_{CC} – 1.0 V_{BE}; this is suitable for high voltage and high gain operation.

For low voltage operation, the inputs are taken to V_{CC} through 51 Ω.

IF Output

The IF is a differential open collector configuration which is designed to use over a wide frequency range for up conversion as well as down conversion.

Input/Output Matching

It is desirable to use a RF ceramic or SAW filter before the mixer to provide image frequency rejection. The filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 3.0 to 5.0 dB insertion loss. The PC board layout accommodates both ceramic and SAW RF filters which are offered by various suppliers such as Siemens, Toko and Murata.

Interface matching between the RF input, RF filter and the mixer will be required. The interface matching networks shown in the application circuit are designed for 50 Ω interfaces.

Differential to single–ended circuit configuration is shown in the test circuit. 6.0 dB of additional mixer gain can be achieved by conjugately matching the output of the MiniCircuits transformer to 50 Ω at the desired IF frequency. With narrowband IF output matching the mixer performance is 3.0 dB gain and 12 dB noise figure (see Narrowband 49 and 83 MHz IF Output Matching Options). Typical insertion loss of the Toko ceramic filter is 3.0 dB. Thus, the overall gain of the circuit is 0 dB with a 15 dB noise figure.

Figure 9. Narrowband IF Output Matching with 16:1 Z Transformer and LC Network

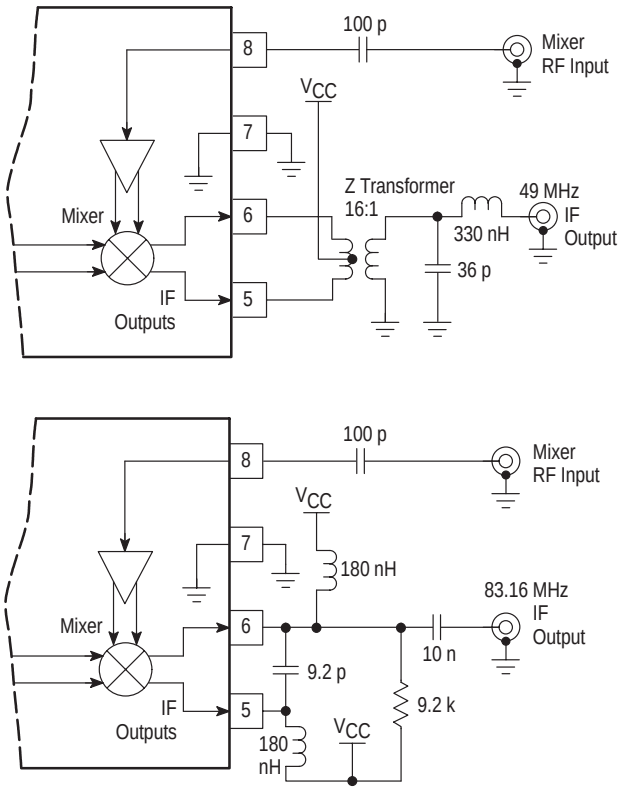
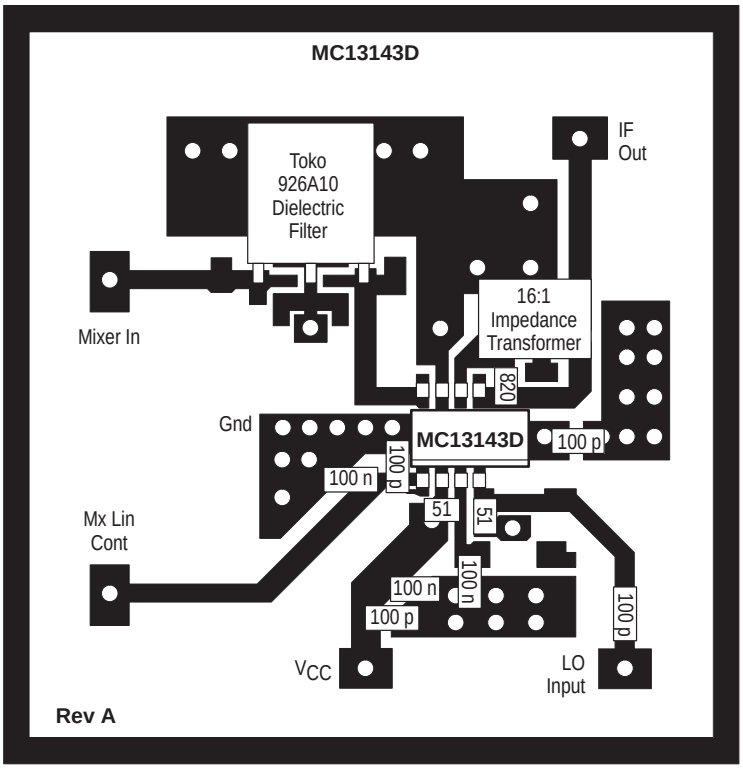


Figure 10. Circuit Side Component Placement View



NOTES: 926.5 MHz preselect dielectric filter is Toko part # 4DFA–926A10; the 4DFA (2 and 3 pole SMD type) filters are available for applications in cellular and GSM, GPS, DECT, PHS, PCS and ISM bands at 902–928 MHz, 1.8–1.9 GHz at 2.4–2.5 GHz.

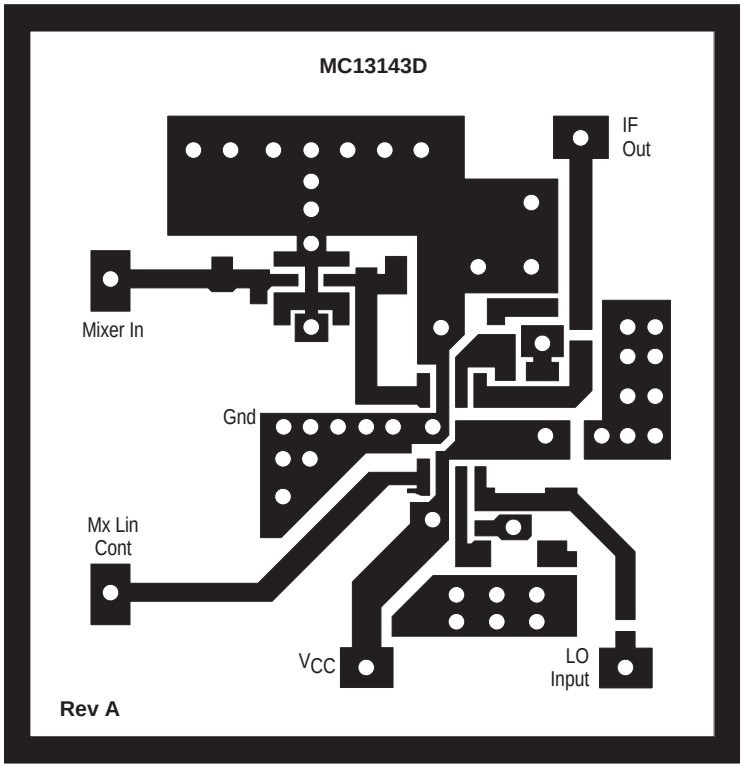
The PCB also accommodates a surface mount RF SAW filter in an eight or six pin ceramic package for the cellular base and handset frequencies. Recommended manufacturers are Siemens and Murata.

The PCB may also be used without a preselector filter; AC coupled to the mixer as shown in the test circuit schematic. All other external circuit components shown in the PCB layout above are the same as used in the test circuit schematic.

16:1 broadband impedance transformer is mini circuits part #TX16–R3T; it is in the leadless surface mount “TX” package. For a more selective narrowband match, a lowpass filter may be used after the transformer. The PCB is designed to accommodate lump inductors and capacitors in more selective narrowband matching of the mixer differential outputs to a single–ended output at a given IF frequency.

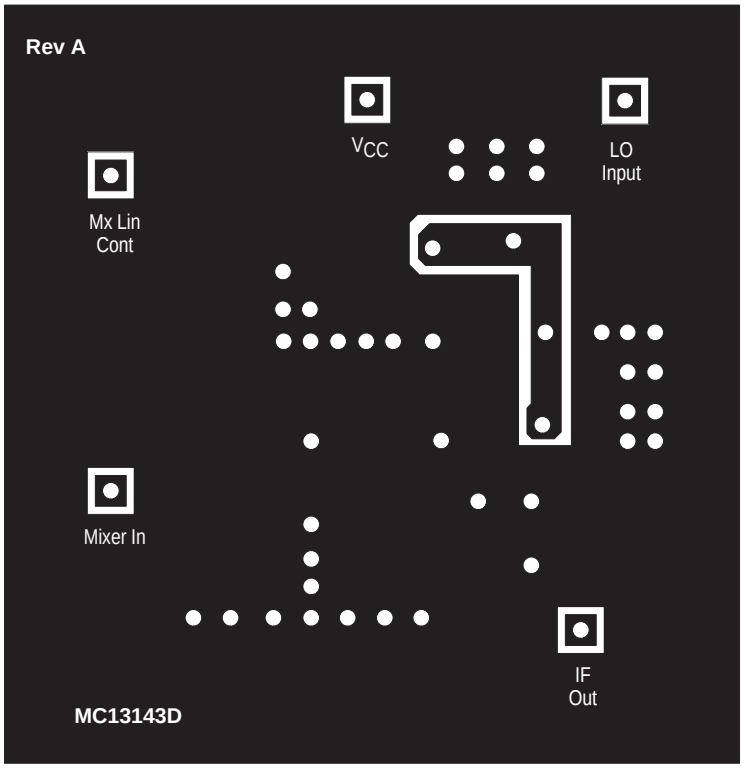
. The local oscillator may also be driven in a differential configuration using a coaxial transformer. Recommended sources are the Toko Balun transformers type B4F, B5FL and B5F (SMD component).

Figure 11. Circuit Side View



NOTES: Critical dimensions are 50 mil centers lead to lead in SO–8 footprint.
Also line widths to labeled ports excluding V_{CC} are 50 mil.

Figure 12. Ground Side View



MOTOROLA

MC13144

Advance Information

VHF - 2.0 GHz Low Noise Amplifier with Programmable Bias

The MC13144 is designed in the Motorola High Frequency Bipolar MOSIAC V™ wafer process to provide excellent performance in analog and digital communication systems. It includes a cascoded LNA usable up to 2.0 GHz and at 1.8 Vdc, with 2 bit digital programming of the LNA bias. Targeted applications are in the UHF Family Radio Services, UHF and 800 MHz Special Mobile Radio, 800 MHz Cellular and GSM, PCS, DECT and PHS at 1.8 to 2.0 GHz and Cordless Telephones in the 902 to 928 MHz band covered by FCC Title 47; Part 15. The MC13144 offers the following features:

- 17 dB Gain at 900 MHz
- 1.4 dB Noise Figure at 900 MHz
- 1.0 dB Compression Point of –7.0 dBm; Input Third Order Intercept Point of –5.0 dBm
- Low Operating Supply Voltage (1.8 to 6.0 Vdc)
- Programmable Bias with Enable 1 and Enable 2
- Enable 1 and Enable 2 Programmed High for Optimal Noise Figure and Gain Associated with NF
- Can Override Enable and Externally Program In Up to 15 mA

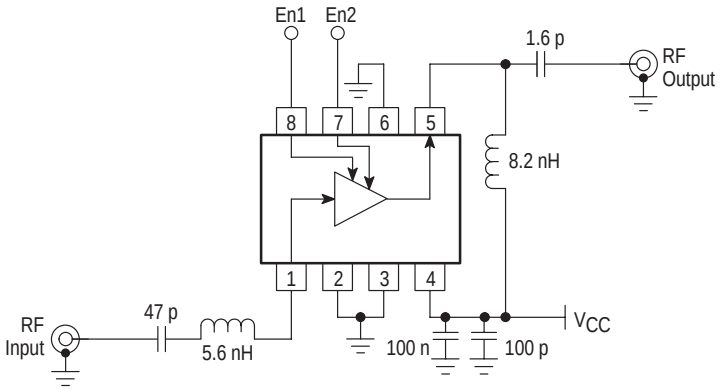
VHF – 2.0 GHz LOW NOISE AMPLIFIER WITH PROGRAMMABLE BIAS

SEMICONDUCTOR TECHNICAL DATA



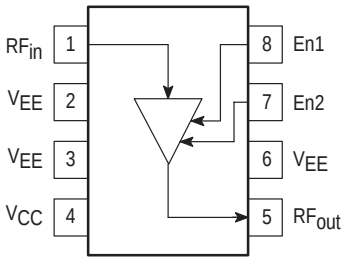
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Typical Application as 900 MHz Low Noise Amplifier



This device contains 67 active transistors.

PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13144D	T_A = – 40 to 85°C	SO–8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}(max)	7.0	Vdc
Junction Temperature	T_{Jmax}	150	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C

NOTES: 1. Devices should not be operated at or outside these values. The "Recommended Operating Conditions" provide for actual device operation.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	1.8	–	6.0	Vdc

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc; f_{RF} = 1.0 GHz; Pin = –25 dBm)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Power Down) (En1 = En2 = Low)	I_{CC0}	–	0.0001	20	μA
Supply Current (Power Up) (En1 = Low; En2 = High)	I_{CC1}	–	1.2	2.0	mA
Supply Current (Power Up) (En1 = High; En2 = Low)	I_{CC2}	–	3.4	5.0	mA
Supply Current (Power Up) (En1 = High; En2 = High)	I_{CC3}	–	8.2	12	mA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc; f_{RF} = 1.0 GHz; Pin = –25 dBm)

Characteristic	Symbol	Min	Typ	Max	Unit
Amplifier Gain (50 Ω Insertion Gain) (En1 = En2 = High)	$S_{21}{}^2$	–	12	–	dB
Amplifier Reverse Isolation (En1 = En2 = High)	S12	–	–35	–	dB
Amplifier Input Return Loss (En1 = En2 = High)	Γin_{amp}	–	–10	–	dB
Amplifier Output Return Loss (En1 = En2 = High)	Γout_{amp}	–	–15	–	dB
Input 3rd Order Intercept Point (En1 = En2 = High) df = 100 kHz df = 1.0 MHz	IIP3	 – –	 –11 –5.0	 – –	dBm
Amplifier Noise Figure (Figure 1; En1 = En2 = High)	NF	–	1.4	2.0	dB
Amplifier Gain @ NF (Figure 1; En1 = En2 = High)	G_{NF}	–	17	–	dB
Amplifier Gain (En1 = En2 = High)	G_{ain3}	14	17	–	dB
Amplifier Gain (En1 = High; En2 = Low)	G_{ain2}	10	13.3	–	dB
Amplifier Gain (En1 = Low; En2 = High)	G_{ain1}	6.0	9.2	–	dB

CIRCUIT DESCRIPTION

General

The MC13144 is a low noise amplifier with programmable bias. This device is designated for use in the front end section in analog and digital FM systems such as Wireless Local Area Network (LAN), Digital European Cordless Telephone (DECT), PHS, PCS, GPS, Cellular, UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services and 902 to 928 MHz cordless telephones.

Current Regulation/Enable

Temperature compensating voltage independent current regulation is digitally controlled by a 2–bit programmable bias/enable circuit.

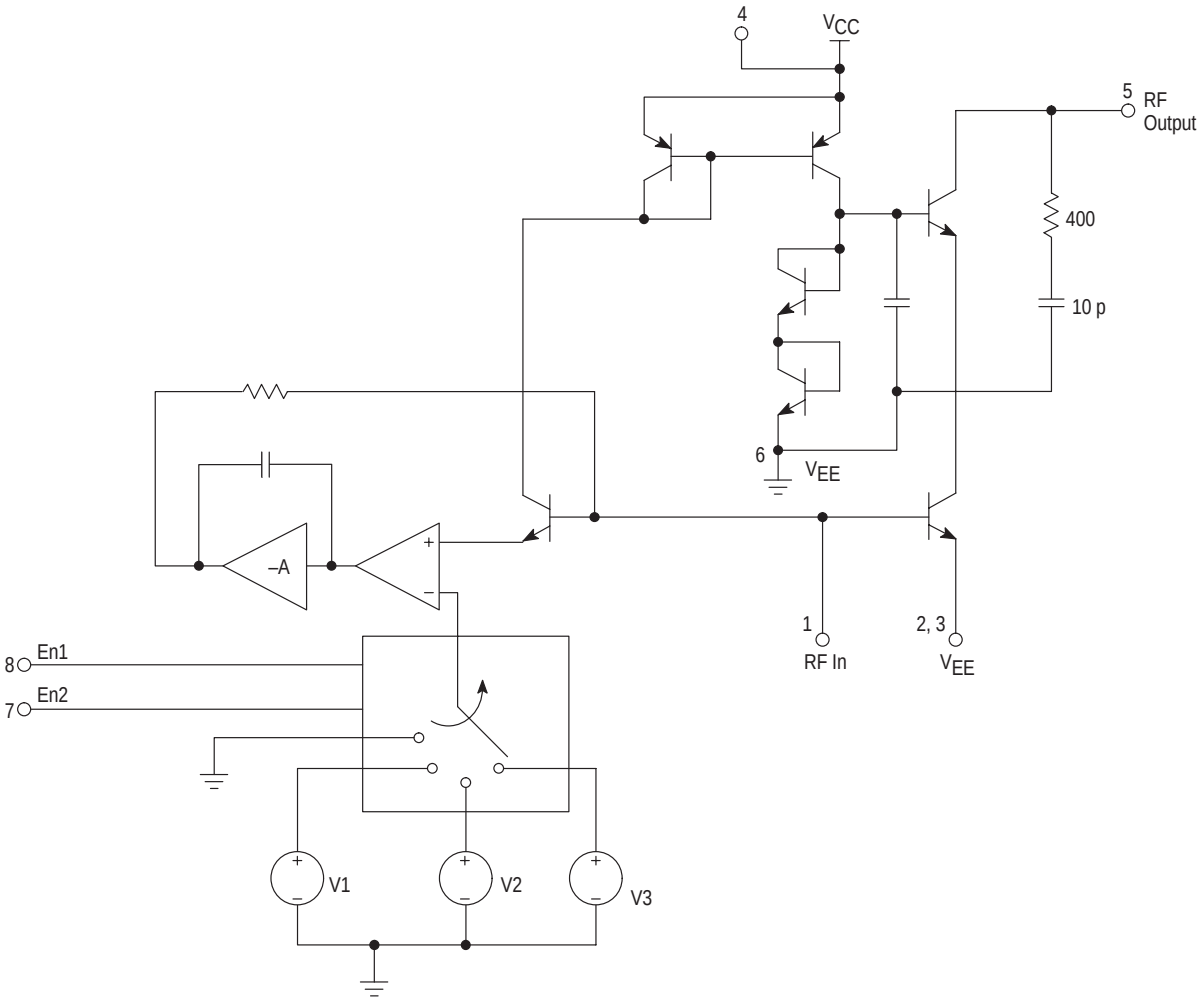
LNA

The LNA is a unique and patented cascode amplifier with digitally (2–bit) programmable bias (see Internal Circuit Schematic). Typical gain of the LNA is 17 dB for minimum noise figure of 1.4 dB at 900 MHz.

Programmable Bias/Enable Circuit

This unique circuit allows for 3 bias levels and a standby mode in which the LNA can be externally biased as desired.

Figure 1. MC13144 Internal Circuit*



NOTE: * The MC13144 uses a unique and patent pending circuit topology.

APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The PC board layout accommodates all SMT components on the circuit side (see Circuit Side Component Placement View).

Component Selection

The evaluation PC board is laid out for the 4DFA (2 pole SMD Type) and 4DFB (3 pole SMD Type) filters which are available for applications in Cellular and GSM, GPS (1.2 to 1.5 GHz), DECT, PHS and PCS (1.8 to 2.0 GHz) and ISM Bands (902 to 928 MHz and 2.4 to 2.5 GHz). In the 926.5 MHz Application Circuit, a ceramic deielectric filter is used (Toko part # 4DFA–926A10).

LNA Input/Output

The LNA input impedance is the base of a common emitter cascode amplifier. The LNA output is the collector of the cascode stage and it is loaded with a series resistor of 400 Ω and a capacitor of 10 pF to provide stability.

Digitally Programmable Bias/Enable

The LNA is enabled by a 2 bit (En1 and En2) programmable bias circuit. The internal circuit shows the comparator circuit which programs the internal regulator. The logic table below shows the bias and typical performance.

f = 900 mHz

I_{CC}/Gain	En2 Low	En2 High
En1 Low	0 mA/–22 dB	1.2 mA/9.2 dB
En1 High	3.4 mA/13 dB	8.2 mA/17 dB

f = 1900 mHz

I_{CC}/Gain	En2 Low	En2 High
En1 Low	0 mA/–22 dB	1.2 mA/7.5 dB
En1 High	3.4 mA/10 dB	8.2 mA/13 dB

Input/Output Matching

A typical application at 900 MHz yields 17 dB gain and 1.4 dB noise figure. In this circuit a series inductor of 5.6 nH is used to match the input and a shunt inductor of 8.2 nH which also serves as an RFC and a series capacitor of 0.9 p is used to match the LNA output to 50 Ω load impedance.

It may be desirable to use a RF ceramic or SAW filter after the LNA when driving a mixer to provide image frequency rejection. The image filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 3.0 to 5.0 dB insertion loss. Interface matching between the RF input, RF filter and the mixer is shown in Application Circuit and the Component Placement View.

A typical application at 1900 MHz yields 13 dB gain and 2.7 dB noise figure. In this circuit a series inductor of 5.6 nH and a series capacitor of 1.0 pF are used to match the input and a shut inductor of 2.0 nH and a series capacitor of 2.0 pF are used to match the LNA output to 50 Ω load impedance.

Figure 2. MC13144D Application Circuit
(926.5 MHz)

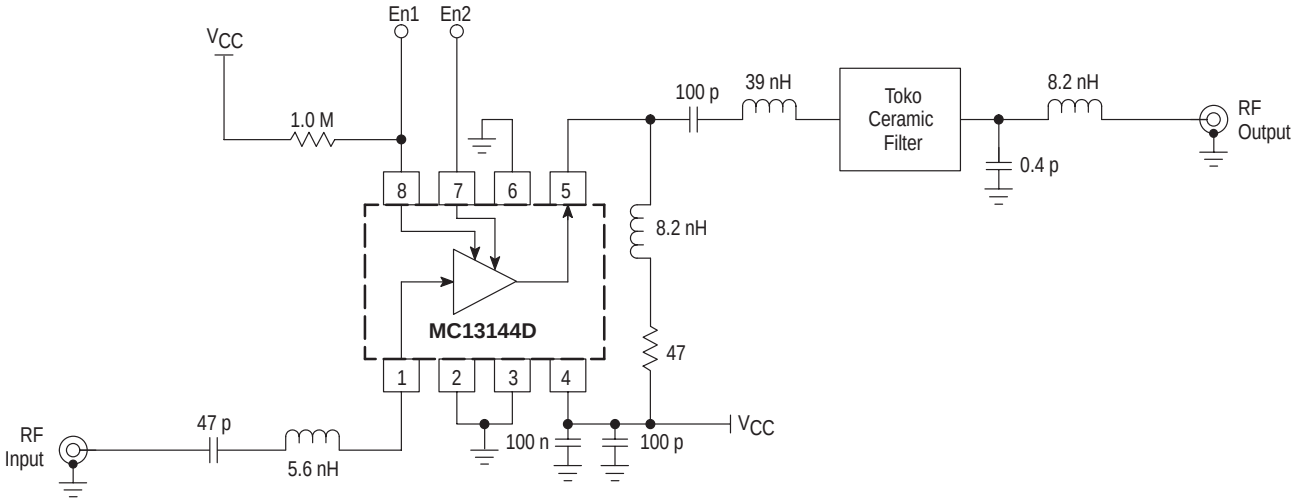


Figure 3. Typical S–Parameters VCC = 3.0 Vdc; En1 = En2 =1

Freq (MHz)	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
100	0.91	–11	4.2	143	0.00028	24	0.80	–10
125	0.92	–14	4.2	136	0.00033	71	0.79	–10
150	0.90	–16	4.2	127	0.0006	60	0.79	–11
175	0.89	–19	4.2	118	0.0011	80	0.78	–12
200	0.89	–22	4.0	108	0.0014	35	0.78	–13
250	0.88	–26	3.8	97	0.0015	39	0.78	–14
300	0.86	–32	4.1	77	0.0022	52	0.78	–17
350	0.85	–36	3.5	59	0.0017	65	.078	–19
400	0.84	–41	3.7	50	0.0024	68	0.79	–21
450	0.83	–46	3.7	26	0.0021	63	0.79	–24
500	0.81	–50	3.2	15	0.0028	56	0.79	–26
550	0.80	–55	3.5	–3.0	0.0027	51	0.80	–29
600	0.79	–59	3.1	–22	0.0038	46	0.81	–32
650	0.77	–63	3.0	–36	0.0057	30	0.82	–35
700	0.77	–67	2.8	–52	0.0067	32	0.83	–39
750	0.77	–72	2.5	–68	0.0095	26	0.83	–43
800	0.76	–77	2.2	–77	0.014	13	0.80	–49
850	0.74	–82	2.2	–86	0.019	12	0.75	–51
900	0.71	–85	2.3	–100	0.020	38	0.73	–51
950	0.69	–88	2.3	–117	0.021	55	0.74	–51
1000	0.67	–91	2.3	–132	0.020	72	0.76	–54
1100	0.67	–98	2.2	–163	0.022	87	0.76	–59
1200	0.66	–106	2.1	168	0.026	107	0.79	–65
1300	0.79	–72	1.9	136	0.030	134	0.64	–73
1400	0.64	–121	1.9	100	0.038	150	0.80	–80
1500	0.62	–128	1.9	74	0.053	170	0.81	–87
1600	0.61	–135	1.7	40	0.068	157	0.82	–96
1700	0.59	–145	1.5	7.0	0.076	120	0.81	–105
1800	0.58	–152	1.4	–24	0.092	97	0.80	–115
1900	0.54	–125	1.2	–57	0.11	59	0.74	–125
2000	0.47	–130	1.0	–79	0.093	195	0.68	–130

Figure 4. Circuit Side Component Placement View

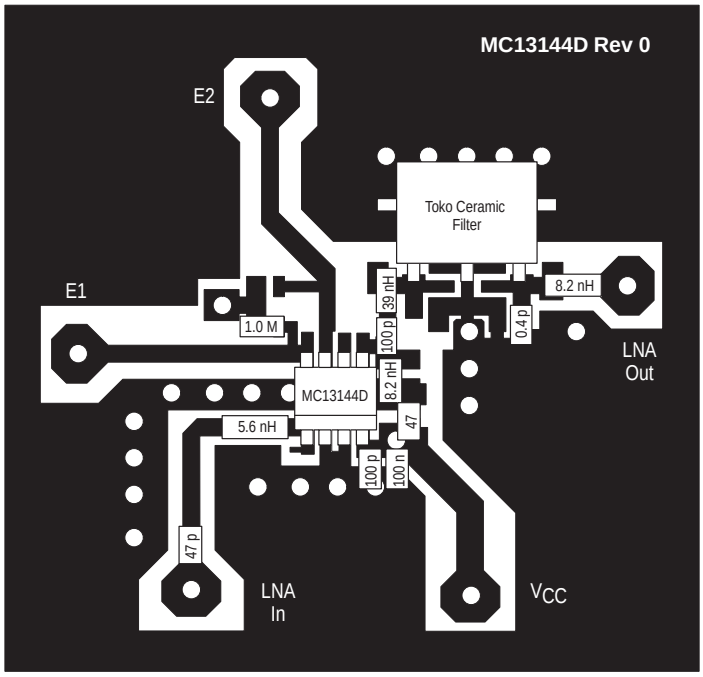
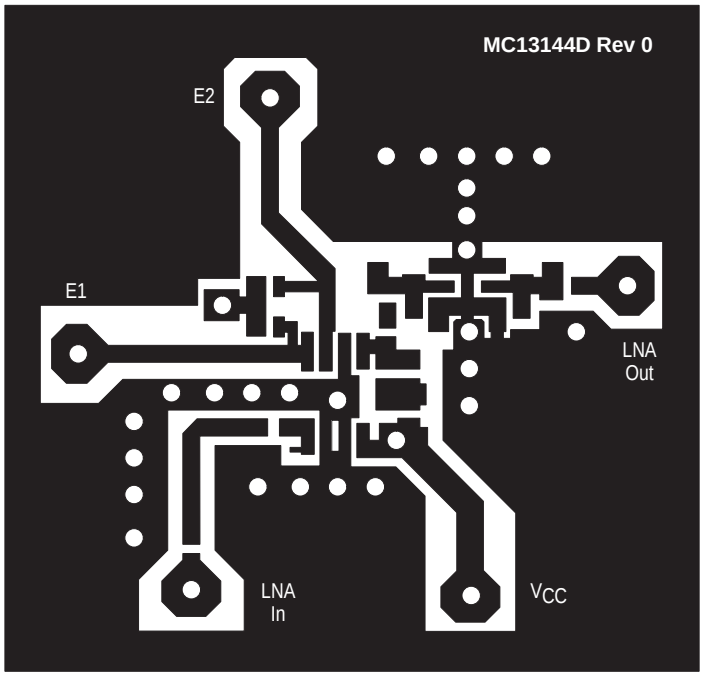
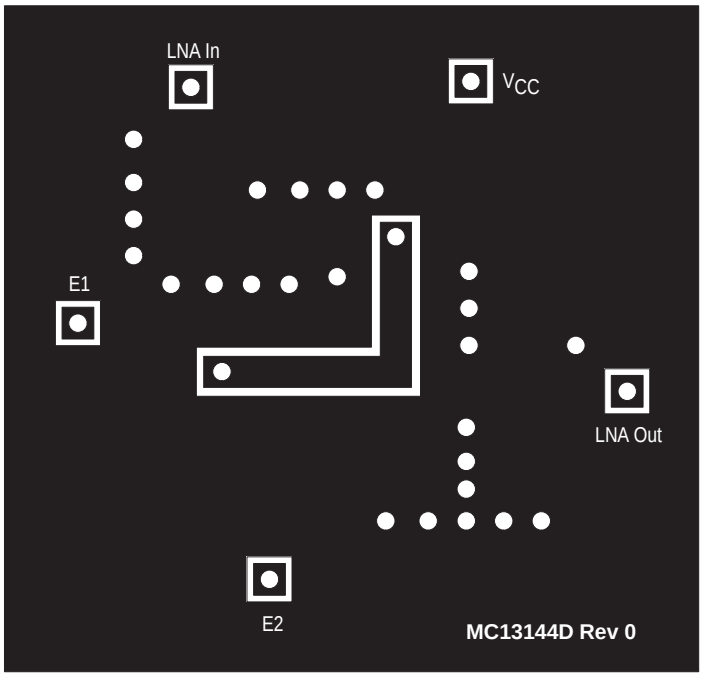


Figure 5. Circuit Side View



NOTES: Critical dimensions are 50 MIL centers lead to lead in SO–8 footprint.
Also line widths to labeled ports excluding V_{CC}, E1 and E2 are 50 MIL (0.050 inch).
FR4 PCB, 1/32 inch.

Figure 6. Ground Side View



NOTES: FR4 PCB, 1/32 inch.

The MRFIC Line

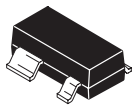
General Purpose RF Cascode Amplifier

MRFIC0915

100 to 2500 MHz
SILICON GENERAL PURPOSE
RF CASCODE AMPLIFIER

The MRFIC0915 is a cost–effective, high isolation cascode silicon monolithic amplifier in the industry standard SOT–143 surface mount package designed for general purpose RF applications. The device is a lower current version of the MRFIC0916 and is appropriate for VCOs, VCO buffers and amplifiers. On–chip bias circuitry sets the bias point while matching is accomplished off chip affording the maximum in application flexibility.

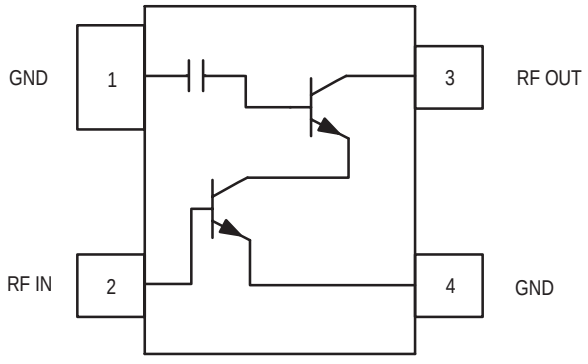
- Usable Frequency Range = 100 to 2500 MHz
- Good Small Signal Gain at V_{CC} = 2.7 Volts
  16.2 dB Typ at 850 MHz
  9.6 dB Typ at 1800 MHz
  5.8 dB Typ at 2400 MHz
- –4.6 dBm typical Output Power at 1 dB Gain Compression at 850 MHz, V_{CC} = 2.7 Volts
- 38 dB Typical Reverse Isolation at 850 MHz
- 2.5 mA Max Bias Current at V_{CC} = 2.7 Volts
- 2.7 to 5 Volt Supply
- Order MRFIC0915T1 for Tape and Reel.
  T1 Suffix = 3.000 Units per 8 mm, 7 inch Reel.
- Device Marking = 22



CASE 318A–05
(SOT–143)

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Limit	Unit
Supply Voltage	V_{CC}	6	Vdc
RF Input Power	P_{RF}	10	dBm
Power Dissipation	P_{DIS}	100	mW
Supply Current	I_{CC}	10	mA
Thermal Resistance, Junction to Case	$R_{\theta JC}$	250	°C/W
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Case Temperature	T_C	– 40 to +100	°C



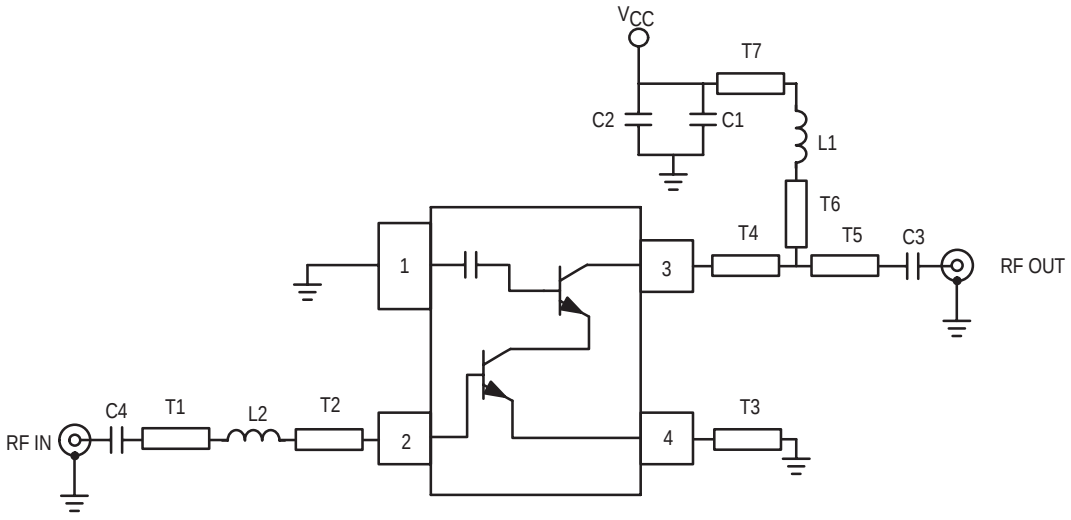
Pin Connections and Functional Block Diagram

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Frequency	f_{RF}	100 to 2500	MHz
Supply Voltage	V_{CC}	2.7 to 5	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V, T_A = 25°C)

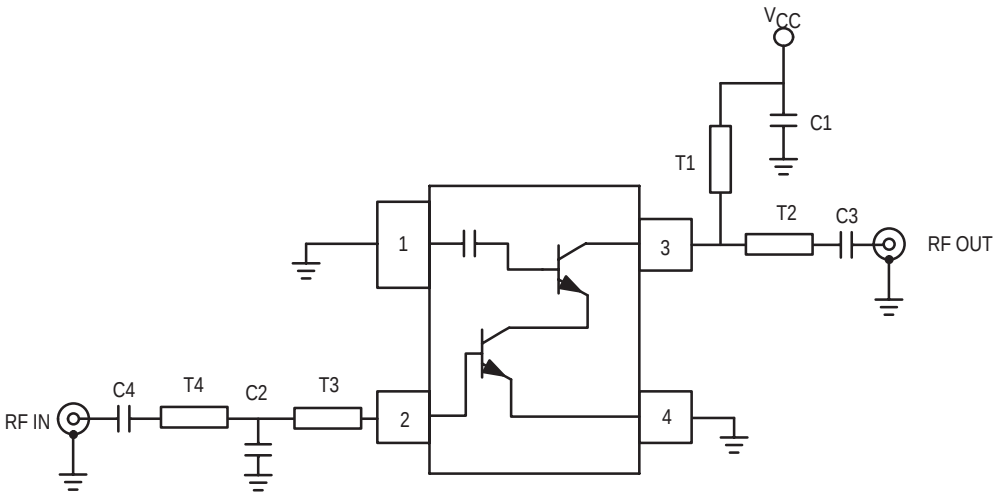
Characteristic	Min	Typ	Max	Unit
Small Signal Gain				
850 MHz	14.2	16.2	—	dB
1800 MHz	7.4	9.6	—	dB
2400 MHz	5	5.8	—	dB
Noise Figure				
850	—	1.9	—	dB
1800 MHz	—	3.6	—	dB
2400 MHz	—	5.5	—	dB
Power Output at 1dB Gain Compression				
850 MHz	—	–4.6	—	dBm
1800 MHz	—	–7.8	—	dBm
2400 MHz	—	–9.8	—	dBm
Output 3rd Order Intercept Point				
850 MHz	—	4	—	dBm
1800 MHz	—	1	—	dBm
2400 MHz	—	–1	—	dBm
Reverse Isolation				
850 MHz	—	38	—	dB
1800 MHz	—	33	—	dB
2400 MHz	—	29	—	dB
Supply Current	1.5	2.0	2.5	mA



C1	10 pF, NPO/COG	T1	50 Ω MICROSTRIP, 0.13”
C2	0.01 µF	T2	76 Ω MICROSTRIP, 0.072”
C3	1.4 pF, NPO/COG	T3	100 Ω MICROSTRIP, 0.035”
C4	12 pF, NPO/COG	T4	50 Ω MICROSTRIP, 0.048”
L1	8.2 nH	T5	50 Ω MICROSTRIP, 0.08”
L2	10 nH	T6	76 Ω MICROSTRIP, 0.062”
		T7	76 Ω MICROSTRIP, 0.07”

BOARD MATERIAL: FR4, ε_r = 4.45, THICKNESS = 0.014”

Figure 1. 850 MHz Applications Circuit Configuration



1.8 GHz DESCRIPTION		2.4 GHz DESCRIPTION	
C1	18 pF, NPO/COG	C1	12 pF, NPO/COG
C2	1.0 pF, NPO/COG	C2	1.2 pF, NPO/COG
C3	0.9 pF, NPO/COG	C3	0.7 pF, NPO/COG
C4	10 pF, NPO/COG	C4	10 pF, NPO/COG
T1	50 Ω MICROSTRIP, 0.41”	T1	50 Ω MICROSTRIP, 0.228”
T2	50 Ω MICROSTRIP, 0.076”	T2	50 Ω MICROSTRIP, 0.076”
T3	50 Ω MICROSTRIP, 0.528”	T3	50 Ω MICROSTRIP, 0.229”
T7	N/A	T4	50 Ω MICROSTRIP, 0.345

BOARD MATERIAL: FR4, ε_r = 4.45, THICKNESS = 0.014”

Figure 2. 1800 and 2400 MHz Applications Circuit Configuration

TYPICAL CHARACTERISTICS

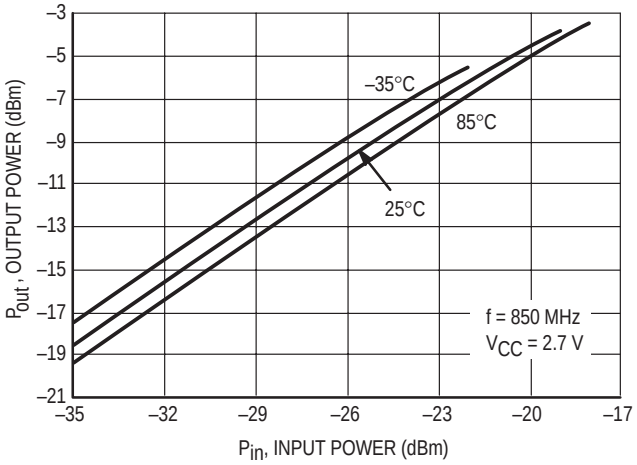


Figure 3. Output Power versus Input Power

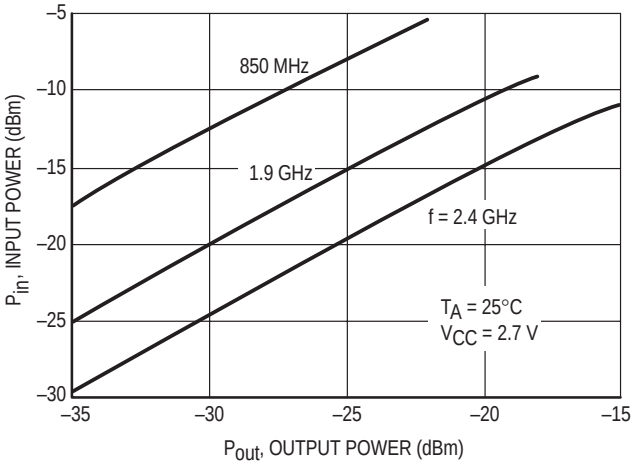


Figure 4. Output Power versus Input Power

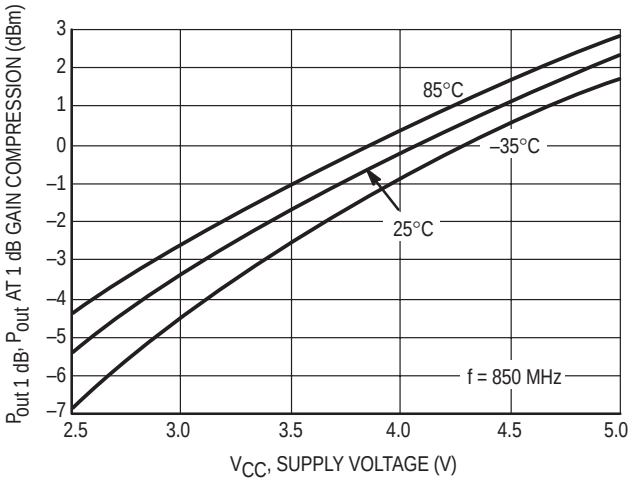


Figure 5. Output Power at 1 dB Gain Compression versus Supply Voltage

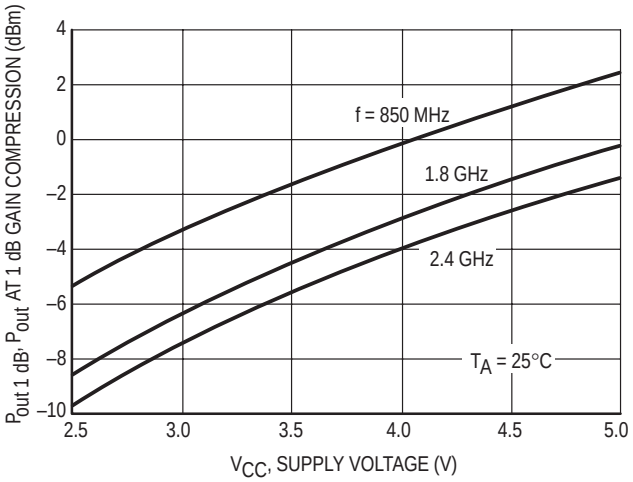


Figure 6. Output Power at 1 dB Gain Compression versus Supply Voltage

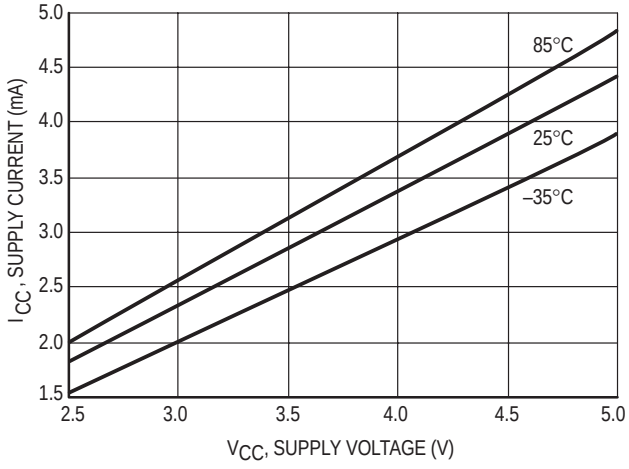


Figure 7. Supply Current versus Supply Voltage

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
100	0.91	–11	5.72	168	0.000	53	0.97	–3
200	0.90	–22	5.50	156	0.001	85	0.97	–7
300	0.86	–32	5.32	145	0.002	80	0.96	–10
400	0.82	–42	5.00	134	0.002	74	0.95	–13
500	0.75	–52	4.72	122	0.002	69	0.94	–16
600	0.70	–60	4.35	113	0.002	67	0.92	–18
700	0.66	–68	4.05	105	0.003	66	0.91	–21
800	0.63	–75	3.65	97	0.003	67	0.90	–24
900	0.57	–83	3.52	89	0.002	69	0.89	–26
1000	0.54	–90	3.28	82	0.002	73	0.87	–29
1100	0.50	–96	3.05	75	0.002	78	0.86	–32
1200	0.48	–103	2.81	69	0.002	92	0.85	–34
1300	0.45	–109	2.71	62	0.002	108	0.84	–37
1400	0.43	–114	2.53	56	0.002	129	0.83	–40
1500	0.41	–120	2.37	51	0.002	147	0.81	–42
1600	0.39	–125	2.28	45	0.003	160	0.80	–45
1700	0.38	–132	2.12	39	0.004	167	0.79	–48
1800	0.37	–137	2.00	34	0.005	113	0.78	–51
1900	0.36	–141	1.88	28	0.006	116	0.77	–53
2000	0.35	–146	1.78	23	0.008	–2	0.76	–56
2100	0.34	–150	1.71	18	0.010	–61	0.75	–59
2200	0.33	–155	1.65	12	0.012	–120	0.74	–62
2300	0.34	–159	1.51	7	0.013	–120	0.73	–65
2400	0.33	–161	1.51	2	0.016	–61	0.72	–69
2500	0.34	–167	1.39	–5	0.019	58	0.71	–73
2600	0.34	–171	1.32	–10	0.022	176	0.70	–77
2700	0.34	–173	1.26	–15	0.025	175	0.69	–80
2800	0.34	–176	1.20	–20	0.028	174	0.68	–83
2900	0.34	–119	1.14	–25	0.032	172	0.67	–86
3000	0.34	118	1.09	–30	0.036	170	0.66	–90

Table 1. S–Parameters (V_{CC} = 2.7 V, 50 Ω System)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
100	0.88	–12	8.65	167	0.001	48	0.97	–3
200	0.85	–23	8.23	154	0.001	93	0.97	–6
300	0.80	–34	7.73	142	0.002	82	0.96	–10
400	0.75	–44	7.15	131	0.002	73	0.95	–12
500	0.67	–53	6.56	119	0.002	68	0.93	–15
600	0.62	–60	5.99	111	0.002	66	0.92	–18
700	0.57	–67	5.47	102	0.002	63	0.91	–21
800	0.53	–74	5.02	95	0.002	65	0.90	–23
900	0.48	–80	4.67	88	0.002	66	0.88	–26
1000	0.44	–86	4.31	81	0.002	69	0.87	–29
1100	0.41	–92	3.98	75	0.001	79	0.86	–31
1200	0.38	–97	3.71	69	0.001	101	0.85	–34
1300	0.36	–102	3.49	63	0.001	139	0.84	–36
1400	0.34	–107	3.26	58	0.002	102	0.82	–39
1500	0.32	–111	3.07	53	0.003	–4	0.81	–42
1600	0.30	–116	2.89	49	0.004	–119	0.80	–44
1700	0.29	–122	2.72	43	0.005	–115	0.79	–47
1800	0.28	–126	2.56	38	0.007	–113	0.78	–50
1900	0.28	–130	2.42	33	0.008	–113	0.77	–53
2000	0.27	–134	2.30	29	0.010	–112	0.76	–55
2100	0.26	–137	2.20	24	0.012	–113	0.75	–58
2200	0.25	–141	2.08	19	0.014	–114	0.74	–61
2300	0.26	–146	1.98	14	0.017	–115	0.73	–64
2400	0.25	–147	1.90	10	0.019	–117	0.72	–68
2500	0.26	–153	1.79	5	0.022	–119	0.71	–72
2600	0.26	–157	1.71	0	0.025	59	0.70	–75
2700	0.27	–159	1.63	–5	0.028	177	0.69	–78
2800	0.27	–162	1.55	–9	0.032	175	0.68	–81
2900	0.27	–164	1.48	–14	0.036	173	0.67	–85
3000	0.27	–167	1.41	–18	0.040	171	0.66	–88

Table 2. S–Parameters (V_{CC} = 4.0 V, 50 Ω System)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
100	0.85	–12	11.04	166	0.00	39	0.97	–3
200	0.82	–24	10.44	152	0.00	94	0.97	–6
300	0.77	–35	9.79	140	0.00	82	0.96	–9
400	0.70	–44	8.95	128	0.00	74	0.96	–12
500	0.62	–53	8.16	117	0.00	69	0.94	–15
600	0.57	–59	7.34	109	0.00	64	0.93	–18
700	0.52	–66	6.70	100	0.00	63	0.92	–20
800	0.48	–72	6.02	93	0.00	65	0.90	–23
900	0.43	–77	5.58	86	0.00	68	0.89	–26
1000	0.39	–82	5.11	80	0.00	71	0.88	–28
1100	0.36	–87	4.71	75	0.00	81	0.87	–31
1200	0.34	–92	4.33	69	0.00	114	0.86	–33
1300	0.32	–95	4.08	63	0.00	152	0.84	–36
1400	0.30	–99	3.80	59	0.00	114	0.83	–38
1500	0.28	–104	3.54	54	0.00	–118	0.82	–41
1600	0.26	–108	3.35	49	0.00	–114	0.81	–44
1700	0.25	–113	3.13	44	0.01	–111	0.80	–47
1800	0.25	–117	2.96	40	0.01	–110	0.79	–49
1900	0.24	–120	2.79	35	0.01	–111	0.78	–52
2000	0.23	–123	2.64	31	0.01	–111	0.77	–55
2100	0.22	–126	2.52	26	0.01	–112	0.76	–58
2200	0.22	–130	2.40	22	0.01	–114	0.75	–61
2300	0.23	–135	2.25	18	0.02	–115	0.74	–64
2400	0.23	–136	2.19	13	0.02	–117	0.73	–67
2500	0.23	–142	2.05	8	0.02	–119	0.72	–71
2600	0.23	–146	1.96	4	0.02	–1	0.71	–74
2700	0.24	–149	1.87	0	0.03	177	0.70	–77
2800	0.24	–151	1.78	–4	0.03	175	0.69	–80
2900	0.25	–153	1.70	–9	0.03	173	0.68	–84
3000	0.25	–156	1.62	–13	0.04	171	0.68	–87

Table 3. S–Parameters (V_{CC} = 5.0 V, 50 Ω System)

V_{CC} (Volts)	f (GHz)	NF_{min} (dB)	Γ_0		R_N (Ω)
			MAG	∠ ϕ	
2.7	0.30	1.26	0.47	18	0.47
	0.50	1.48	0.42	29	0.44
	0.70	1.71	0.38	41	0.42
	0.90	1.96	0.34	53	0.41
	1.00	2.09	0.33	60	0.40
	1.50	2.82	0.27	94	0.38
	2.00	3.67	0.25	132	0.36
	2.40	4.43	0.25	165	0.36
4.0	0.30	1.27	0.37	18	0.37
	0.50	1.41	0.33	29	0.35
	0.70	1.56	0.30	40	0.33
	0.90	1.73	0.27	52	0.32
	1.00	1.82	0.25	59	0.31
	1.50	2.32	0.21	93	0.30
	2.00	2.91	0.20	133	0.29
	2.40	3.44	0.21	168	0.29
4.5	0.30	1.41	0.38	18	0.40
	0.50	1.53	0.34	26	0.38
	0.70	1.67	0.31	36	0.37
	0.90	1.83	0.27	46	0.36
	1.00	1.92	0.26	52	0.35
	1.50	2.42	0.20	85	0.33
	2.00	3.03	0.17	126	0.32
	2.40	3.61	0.16	165	0.34
5.0	0.30	1.36	0.33	18	0.35
	0.50	1.47	0.29	28	0.33
	0.70	1.60	0.26	40	0.32
	0.90	1.74	0.24	52	0.31
	1.00	1.82	0.22	58	0.30
	1.50	2.25	0.18	93	0.29
	2.00	2.78	0.17	133	0.28
	2.40	3.27	0.18	170	0.29

Table 4. Typical Noise Parameters (50 Ω System)

MOTOROLA

General Purpose RF Cascode Amplifier

The MRFIC0916 is a cost–effective, high isolation cascode silicon monolithic amplifier in the industry standard SOT–143 surface mount package designed for general purpose RF applications. On chip bias circuitry sets the bias point while matching is accomplished off chip affording the maximum in application flexibility.

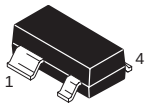
- Usable Frequency Range = 100 to 2500 MHz
- 18.5 dB typical gain at 850 MHz, V_{CC} = 2.7 V
- 2.3 dBm typical Output Power at 1.0 dB Gain Compression at 850 MHz, V_{CC} = 2.7 V
- 44 dB Typical Reverse Isolation at 850 MHz
- 5.6 mA Max Bias Current at V_{CC} = 2.7 V
- 2.7 to 5.0 V Supply

MRFIC0916

GENERAL PURPOSE RF CASCODE AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

Pin 1. Gnd
2. RF In
3. RF Out
4. Gnd

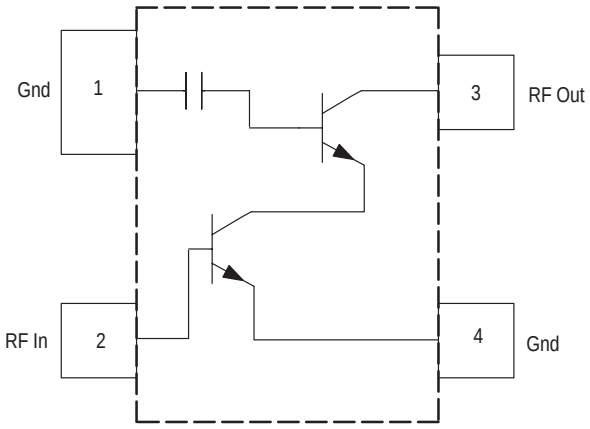


PLASTIC PACKAGE
CASE 318A
(SOT–143, Tape & Reel Only)

ORDERING INFORMATION

Device	Device Marking	Package
MRFIC0916T1	16	SOT–143

Functional Block Diagram



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	Vdc
RF Input Power	P_{RF}	10	dBm
Power Dissipation	P_{DIS}	100	mW
Supply Current	I_{CC}	20	mA
Thermal Resistance, Junction to Case	$R_{\theta JC}$	250	C/W
Storage Temperature Range	T_{stg}	–65 to 150	°C
Operating Case Temperature	T_C	–40 to 100	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
RF Frequency	f_{RF}	100	–	2500	MHz
Supply Voltage	V_{CC}	2.7	–	5.0	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V, T_A = 25°C, f_{RF} = 850 MHz, Tested in Circuit Shown in Figure 1, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Small Signal Gain		16.5	18.5	20.5	dB
Noise Figure		–	1.9	–	dB
Power Output at 1.0 dB Gaim Compression		0	2.3	–	dBm
Output 3rd Order Intercept Point		–	11	–	dBm
Reverse Isolation		–	44	–	dB
Supply Current		3.8	4.7	5.6	mA

Figure 1. 850 MHz Applications Circuit Configuration

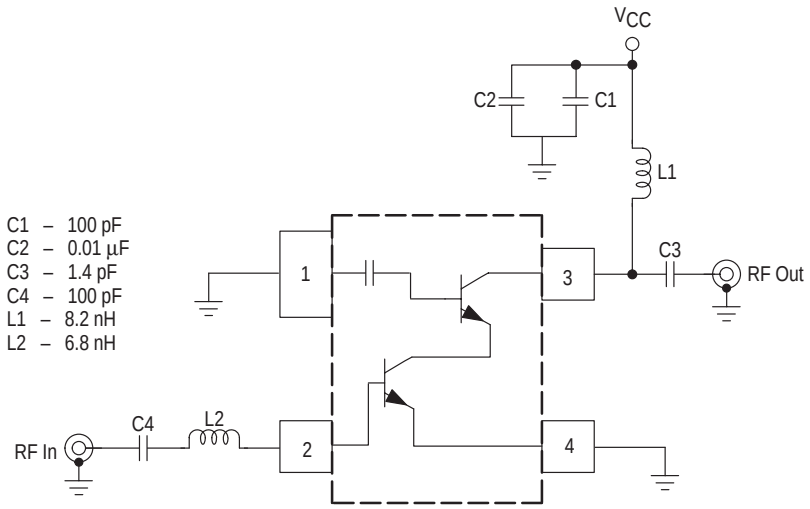


Figure 2. GU_{max} versus Frequency

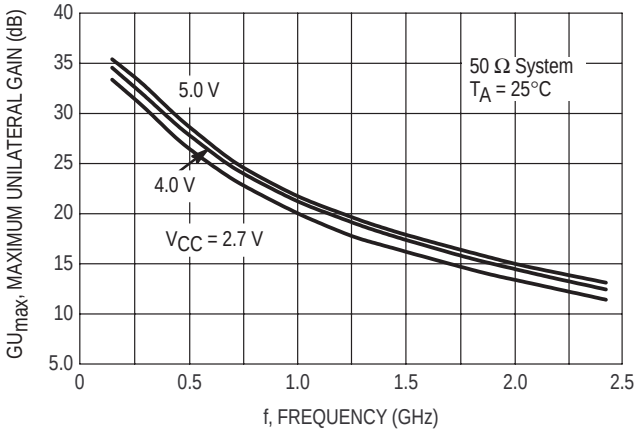


Figure 3. Output Power versus Input Power

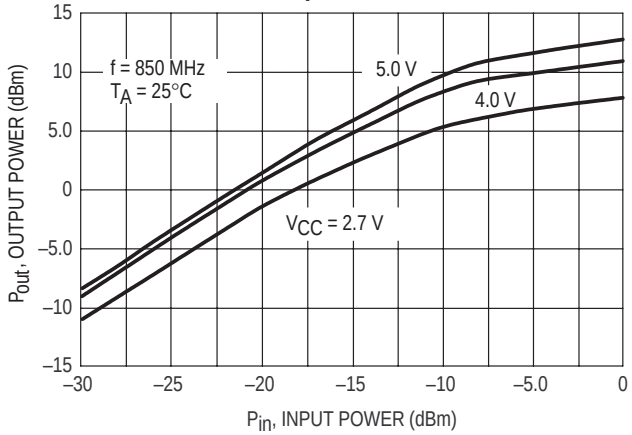


Figure 4. Supply Current versus Input Power

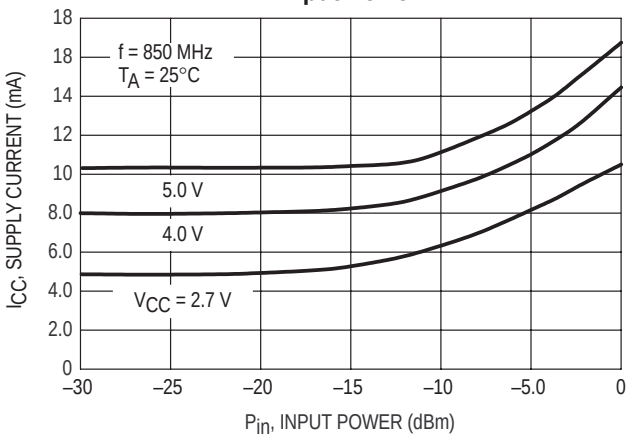


Table 1. Scattering Parameters
(V_{CC} = 2.7 V, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
100	0.806	–17.01	12.03	162.32	0.001	–0.14	0.956	–4.69
200	0.765	–33.28	11.18	145.74	0.001	71.58	0.948	–8.69
300	0.713	–47.99	10.18	130.99	0.002	69.67	0.945	–13.23
400	0.652	–61.35	9.06	118.01	0.003	64.61	0.930	–17.35
500	0.574	–70.94	8.06	106.50	0.003	62.93	0.904	–20.85
600	0.533	–81.00	7.09	96.50	0.003	61.94	0.891	–24.71
700	0.493	–89.33	6.36	87.60	0.003	63.16	0.875	–28.18
800	0.469	–97.65	5.62	79.57	0.003	66.33	0.857	–31.89
900	0.432	–103.64	5.16	72.38	0.002	80.79	0.845	–35.21
1000	0.409	–110.68	4.70	65.39	0.002	100.33	0.831	–38.86
1100	0.396	–116.17	4.29	58.75	0.002	127.72	0.815	–42.52
1200	0.383	–122.20	3.91	52.55	0.003	152.57	0.799	–45.77
1300	0.373	–126.00	3.66	46.34	0.004	164.39	0.789	–49.49
1400	0.369	–131.29	3.38	40.61	0.006	169.63	0.776	–53.23
1500	0.366	–134.46	3.14	35.29	0.008	172.81	0.762	–56.86
1600	0.366	–140.07	2.93	29.63	0.011	172.47	0.751	–60.74
1700	0.364	–143.07	2.75	23.86	0.013	172.79	0.738	–64.66
1800	0.368	–147.48	2.58	18.42	0.016	171.54	0.727	–68.29
1900	0.377	–148.91	2.42	13.15	0.020	170.15	0.719	–72.29
2000	0.381	–153.42	2.27	7.58	0.023	167.89	0.707	–76.58
2100	0.394	–155.23	2.15	2.46	0.027	165.86	0.695	–80.50
2200	0.396	–158.91	2.03	–3.00	0.032	163.46	0.685	–84.85
2300	0.416	–160.43	1.90	–8.32	0.037	161.00	0.672	–88.93
2400	0.424	–162.98	1.81	–13.30	0.042	158.00	0.662	–93.38
2500	0.434	–166.35	1.68	–18.45	0.047	155.58	0.654	–97.89

Table 2. Scattering Parameters
(V_{CC} = 4 V, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
100	0.744	–17.43	16.979	160.38	0.001	–2.89	0.955	–4.40
200	0.691	–33.58	15.442	142.46	0.001	83.36	0.950	–8.33
300	0.627	–47.53	13.633	127.28	0.002	76.39	0.946	–12.79
400	0.558	–59.50	11.851	114.52	0.002	70.12	0.931	–16.75
500	0.482	–67.02	10.284	103.51	0.002	67.02	0.907	–20.11
600	0.440	–75.50	8.957	94.12	0.002	66.00	0.895	–23.85
700	0.401	–81.87	7.930	85.95	0.002	68.71	0.880	–27.22
800	0.377	–88.89	7.003	78.57	0.002	73.50	0.863	–30.83
900	0.348	–93.11	6.348	71.96	0.002	90.55	0.852	–34.06
1000	0.328	–98.88	5.747	65.59	0.002	113.74	0.838	–37.62
1100	0.317	–103.27	5.223	59.57	0.002	146.45	0.822	–41.18
1200	0.306	–108.54	4.765	53.98	0.003	165.49	0.808	–44.34
1300	0.301	–111.30	4.425	48.39	0.004	175.51	0.798	–47.95
1400	0.297	–116.30	4.082	43.18	0.006	177.46	0.785	–51.59
1500	0.298	–118.89	3.790	38.32	0.008	179.45	0.771	–55.11
1600	0.298	–124.58	3.531	33.13	0.011	178.69	0.760	–58.88
1700	0.301	–127.19	3.300	28.02	0.014	178.02	0.748	–62.66
1800	0.305	–131.73	3.093	23.10	0.016	176.25	0.737	–66.16
1900	0.319	–133.16	2.901	18.34	0.020	174.44	0.729	–70.03
2000	0.324	–137.94	2.724	13.33	0.023	172.03	0.717	–74.16
2100	0.339	–140.09	2.575	8.67	0.027	169.82	0.706	–77.92
2200	0.342	–143.98	2.434	3.79	0.032	166.99	0.696	–82.07
2300	0.367	–146.00	2.278	–0.98	0.036	164.37	0.684	–86.04
2400	0.375	–148.75	2.166	–5.56	0.042	161.35	0.674	–90.25
2500	0.387	–152.75	2.020	–10.12	0.046	158.69	0.666	–94.64

Table 3. Scattering Parameters
(V_{CC} = 5 V, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
100	0.707	–17.56	20.04	159.03	0.001	–7.95	0.954	–4.25
200	0.648	–33.40	17.93	140.29	0.001	86.24	0.950	–8.15
300	0.579	–46.60	15.53	124.94	0.002	78.79	0.946	–12.54
400	0.509	–57.44	13.31	112.38	0.002	72.27	0.931	–16.42
500	0.438	–63.51	11.40	101.70	0.002	69.34	0.908	–19.68
600	0.397	–70.90	9.87	92.70	0.002	69.55	0.896	–23.35
700	0.363	–76.05	8.69	84.92	0.002	71.59	0.882	–26.64
800	0.340	–82.18	7.67	77.89	0.002	79.44	0.865	–30.20
900	0.316	–85.44	6.91	71.60	0.002	95.59	0.855	–33.36
1000	0.298	–90.52	6.24	65.56	0.001	121.55	0.841	–36.86
1100	0.290	–94.44	5.67	59.82	0.002	152.13	0.826	–40.37
1200	0.280	–99.17	5.17	54.53	0.003	169.84	0.811	–43.48
1300	0.277	–101.65	4.79	49.25	0.005	177.80	0.802	–47.02
1400	0.274	–106.49	4.42	44.27	0.006	–179.84	0.790	–50.59
1500	0.278	–109.07	4.10	39.65	0.008	–179.19	0.776	–54.04
1600	0.276	–114.88	3.82	34.68	0.011	–179.68	0.765	–57.73
1700	0.281	–117.46	3.56	29.88	0.013	179.47	0.753	–61.43
1800	0.285	–122.11	3.34	25.21	0.016	177.73	0.742	–64.85
1900	0.300	–123.94	3.14	20.70	0.019	175.80	0.734	–68.66
2000	0.305	–128.93	2.95	15.91	0.023	173.47	0.723	–72.71
2100	0.322	–131.48	2.78	11.50	0.027	171.04	0.712	–76.37
2200	0.324	–135.50	2.63	6.84	0.031	168.25	0.703	–80.42
2300	0.351	–138.04	2.47	2.33	0.036	165.47	0.691	–84.31
2400	0.358	–140.88	2.34	–2.05	0.041	162.71	0.681	–88.42
2500	0.371	–145.28	2.19	–6.40	0.046	160.19	0.674	–92.74

Table 4. Typical Noise Parameters
(50 Ω System)

V_{CC} (Volts)	f (GHz)	NF_{min} (dB)	Γ_0		R_N (Ω)
			MAG	∠ ϕ	
2.7	0.3	1.48	0.08	–145	0.18
	0.5	1.48	0.11	–52	0.23
	0.7	1.52	0.14	27	0.25
	0.9	1.61	0.17	93	0.21
	1.0	1.67	0.19	121	0.18
	1.5	2.16	0.26	–152	0.17
	2.0	2.94	0.33	–150	0.22
	2.4	3.78	0.38	150	0.26
4.0	0.3	1.66	0.07	114	0.24
	0.5	1.62	0.09	118	0.21
	0.7	1.62	0.12	124	0.19
	0.9	1.67	0.14	130	0.18
	1.0	1.71	0.15	133	0.17
	1.5	2.08	0.21	152	0.17
	2.0	2.72	0.27	175	0.19
	2.4	3.44	0.32	–164	0.232
4.5	0.3	1.85	0.14	149	0.20
	0.5	1.74	0.14	146	0.18
	0.7	1.69	0.14	144	0.17
	0.9	1.69	0.15	144	0.17
	1.0	1.71	0.16	145	0.17
	1.5	2.04	0.20	155	0.18
	2.0	2.71	0.26	175	0.20
	2.4	3.50	0.33	–161	0.24
5.0	0.3	1.83	0.10	133	0.27
	0.5	1.76	0.11	136	0.23
	0.7	1.73	0.13	141	0.20
	0.9	1.75	0.14	146	0.18
	1.0	1.78	0.15	148	0.17
	1.5	2.10	0.19	163	0.17
	2.0	2.71	0.25	–179	0.20
	2.4	3.42	0.30	–163	0.25

The MRFIC Line

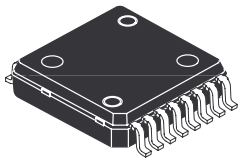
900 MHz GaAs Integrated Power Amplifier

MRFIC0917

900 MHz
GSM CELLULAR
INTEGRATED POWER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT

This integrated circuit is intended for GSM class IV handsets. The device is specified for 2.5 Watts output power and 43% minimum power added efficiency under GSM signal conditions at 3.6 Volt supply voltage. To achieve this superior performance, Motorola's planar GaAs MESFET process is employed. The device is packaged in the PFP–16 Power Flat Pack package which gives excellent thermal performance through a solderable backside contact.

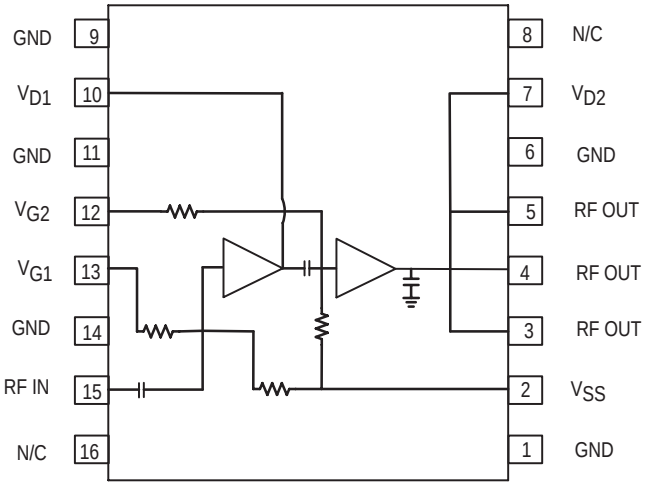
- Usable Frequency Range 800 to 1000 MHz
- Typical Output Power: 34.5 dBm @ 3.6 Volts
- 43% Minimum Power Added Efficiency
- Low Parasitic, High Thermal Dissipation Package
- Order MRFIC0917R2 for Tape and Reel.
  R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M0917



CASE 978–02
(PFP–16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage, Normal Conditions	V_{D1}, V_{D2}	6	Vdc
Supply Voltage under Load Stress	V_{D1}, V_{D2}	4.5	Vdc
RF Input Power	P_{in}	15	dBm
Gate Voltage	V_{SS}	–6	Vdc
Ambient Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	15	°C/W



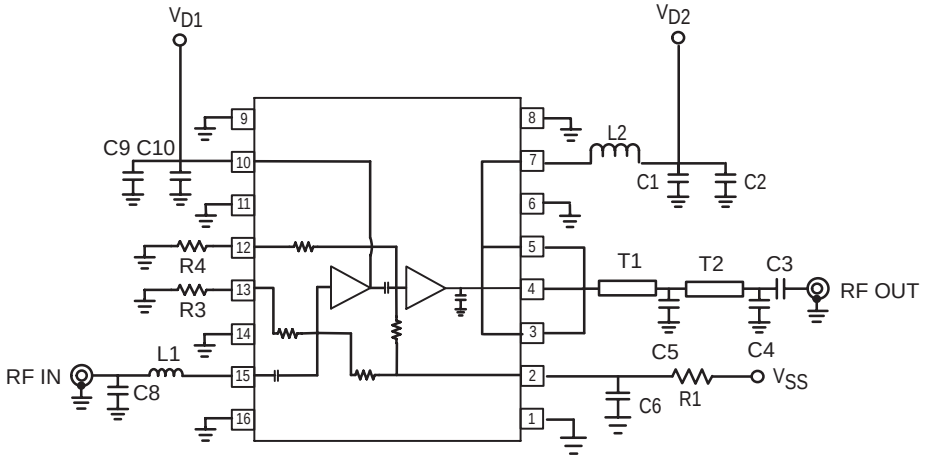
Pin Connections and Functional Block Diagram

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	V_{D1}, V_{D2}	2.7 to 5.5	Vdc
Gate Voltage	V_{SS}	–5 to –3	Vdc
RF Frequency Range	f_{RF}	800 to 1000	MHz
RF Input Power	P_{RF}	6 to 13	dBm

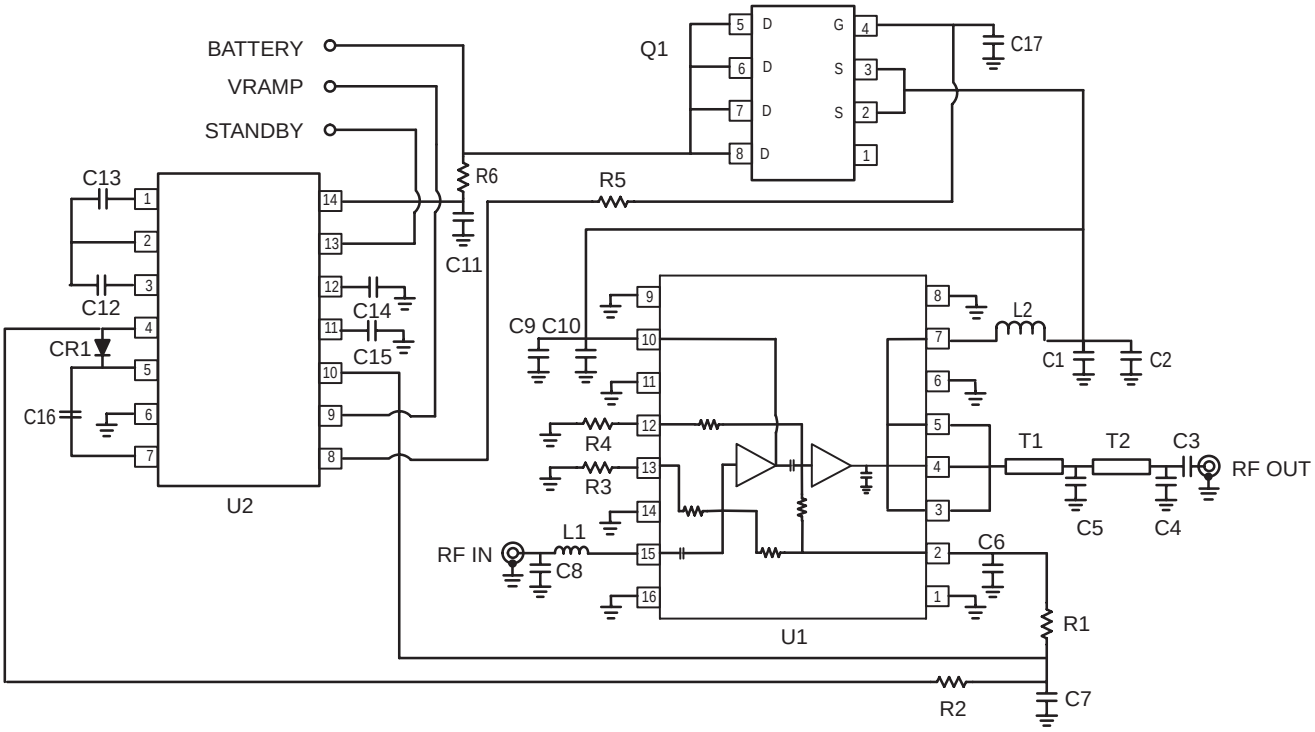
ELECTRICAL CHARACTERISTICS (V_{D1}, V_{D2} = 3.6 V, V_{SS} = –4 V, P_{in} = 12 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted. Measured in Circuit Configuration Shown in Figure 1.)

Characteristic	Min	Typ	Max	Unit
Frequency Range	880	—	915	MHz
Output Power	34	34.5	—	dBm
Power Added Efficiency	43	—	—	%
Input VSWR	—	2:1	—	VSWR
Harmonic Output 2nd 3rd	 — —	 — —	 –30 –35	dBc
Output Power at low voltage (V_{D1}, V_{D2} = 3.0 V)	32.5	33	—	dBm
Output Power, Isolation (V_{D1}, V_{D2} = 0 V)	—	–20	–15	dBm
Noise Power in 100 kHz, 925 to 960 MHz	—	—	–90	dBm
Stability – Spurious Output (P_{in} = 10 to 13 dBm, P_{out} = 5 to 34.5 dBm, Load VSWR = 6:1 at any Phase Angle, Source VSWR = 3:1, at any Phase Angle, V_{D1}, V_{D2} Adjusted for Specified P_{out})	—	—	–60	dBc
Load Mismatch Stress (P_{in} = 10 to 13 dBm, P_{out} = 5 to 34.5 dBm, Load VSWR = 10:1 at any Phase Angle, V_{D1}, V_{D2} Adjusted for Specified P_{out})	No Degradation in Output Power after Returning to Standard Conditions			
3 dB V_{DD} Bandwidth (V_{D1}, V_{D2} = 0 to 4.5 V)	1	—	—	MHz
Negative Supply Current	—	—	1	mA



C1, C3, C10	33 pF	C8	6.8 pF	R1, R3	330 Ω
C2, C6, C9	33 nF	L1	5.6 nH	R4	1 kΩ
C4	4.7 pF	L2	10 Turn MicroSpring,	T1	2 mm 30 Ω MICROSTRIP
C5	10 pF		Coilcraft 1606–10 or	T2	3.5 mm 30 Ω MICROSTRIP
			18 mm 50 Ω MICROSTRIP	BOARD MATERIAL	FR4

Figure 1. 900 MHz Reference Circuit



C1, C3, C10	33 pF	CR1	MMBD701LT1	R4	1 kΩ
C2, C6, C9	33 nF	L1	5.6 nH	R5	470 Ω
C4	4.7 pF	L2	10 Turn MicroSpring,	R6	22 Ω
C5	10 pF		Coilcraft 1606–10 or 18 mm	T1	2 mm 30 Ω MICROSTRIP
C7	220 nF		50 Ω MICROSTRIP	T2	3.5 mm 30 Ω MICROSTRIP
C8	6.8 pF	Q1	MMSF4N01HD	U1	MRFIC0917
C11 to C16	1 μF	R1, R3	330 Ω	U2	MC33169 (–4 V Version)
C17	0 to 5 nF Depending on control bandwidth	R2	100 Ω	BOARD MATERIAL	FR4

Figure 2. GSM Application Circuit Configuration with Drain Switch and MC33169 GaAs Power Amplifier Support IC

TYPICAL CHARACTERISTICS

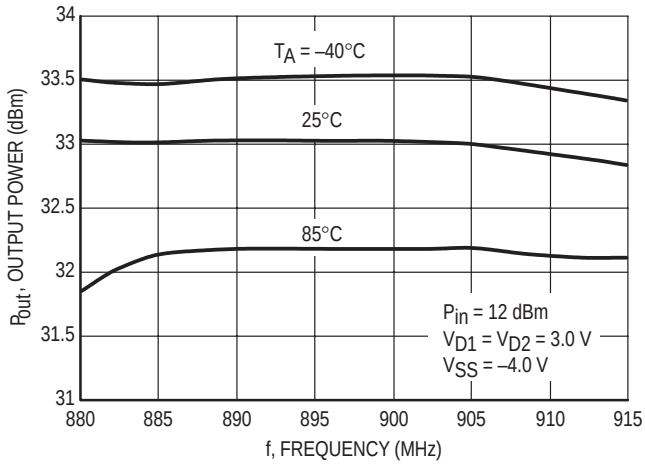


Figure 3. Output Power versus Frequency

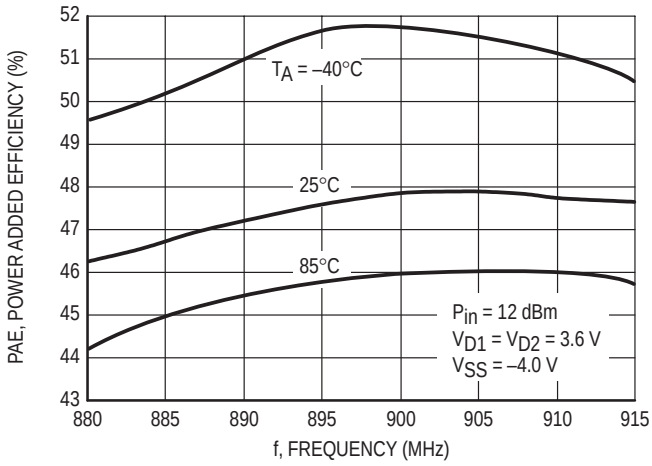


Figure 4. Power Added Efficiency versus Frequency

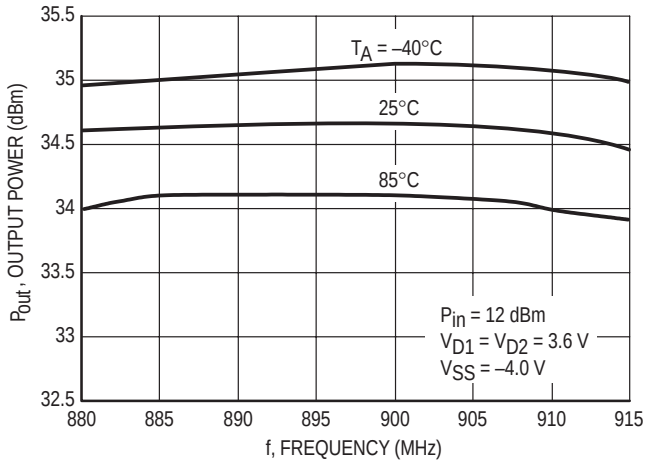


Figure 5. Output Power versus Frequency

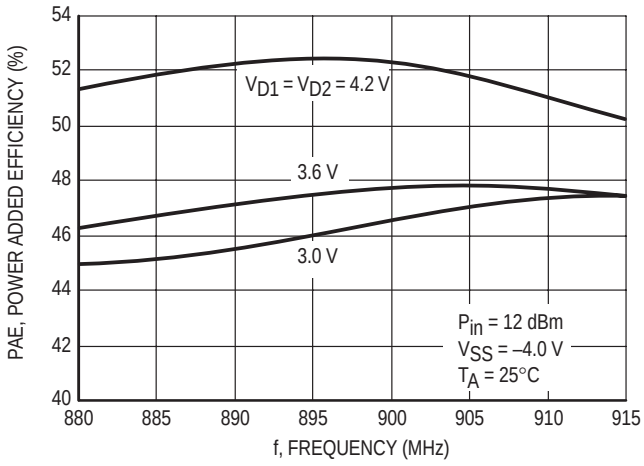


Figure 6. Power Added Efficiency versus Frequency

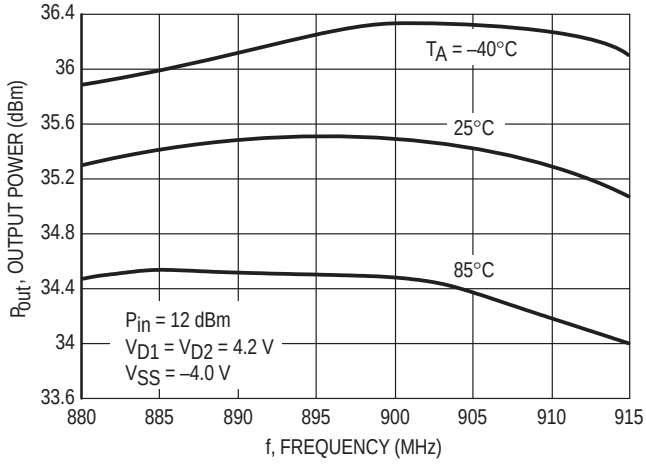


Figure 7. Output Power versus Frequency

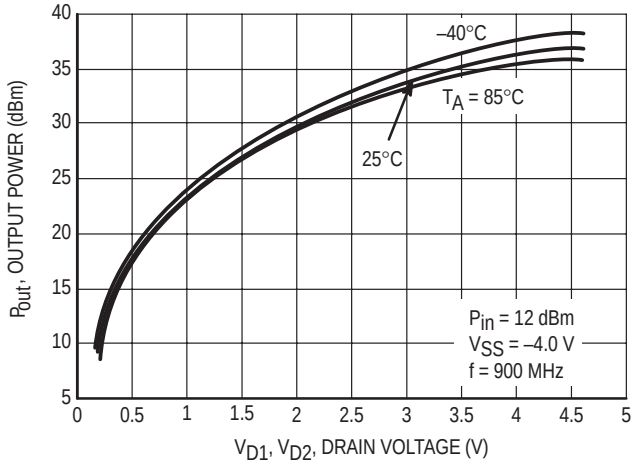


Figure 8. Output Power versus Drain Voltage

TYPICAL CHARACTERISTICS

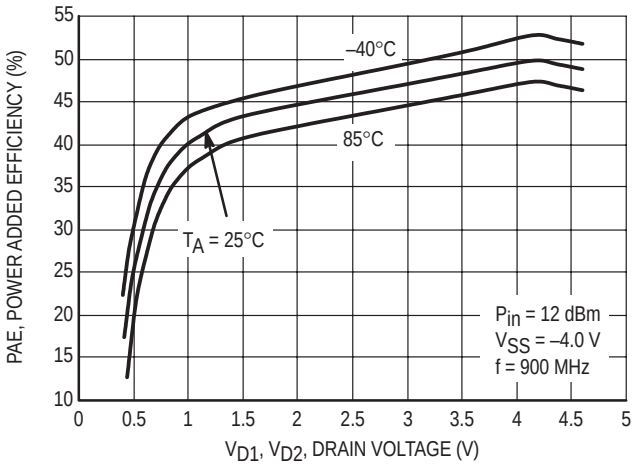


Figure 9. Power Added Efficiency versus Drain Voltage

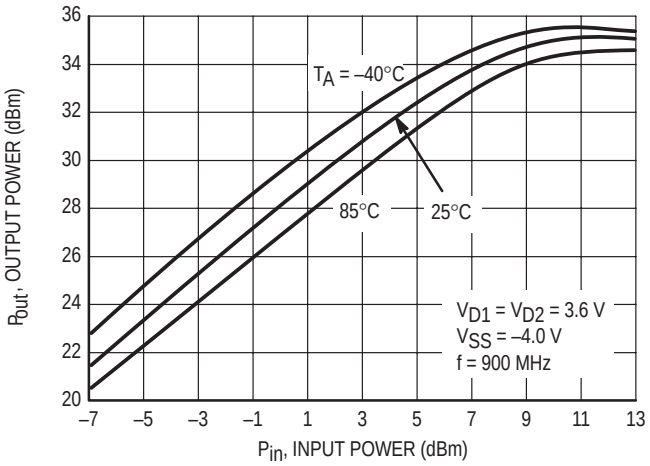


Figure 10. Output Power versus Input Power

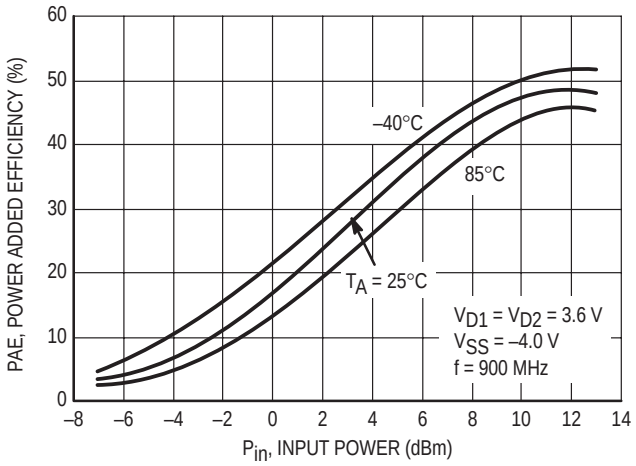


Figure 11. Power Added Efficiency versus Input Power

f	Z_{in} (Ω)		Z_{OL}^* (Ω)	
MHz	R	jX	R	jX
880	20.2	8.63	2.49	7.04
885	20.5	8.57	2.48	6.98
890	20.8	8.5	2.45	6.91
895	21.2	8.42	2.43	6.81
900	21.5	8.36	2.42	6.74
905	21.9	8.3	2.4	6.64
910	22.3	8.23	2.37	6.58
915	22.6	8.17	2.36	6.51

Table 1. Device Impedances Derived from Circuit Characterization

Table 2. Scattering Parameters

(V_{DD} = 3 V, V_{SS}, V_{G1}, V_{G2} Set for I_{DQ1}= 150 mA and I_{DQ2} = 750 mA, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
500	0.738	–86	12.71	–82	0.002	147	0.891	173
600	0.786	–83	5.05	–102	0.003	132	0.874	170
700	0.799	–113	11.56	–79	0.004	153	0.858	173
800	0.681	–115	8.44	–113	0.005	138	0.885	171
820	0.671	–116	7.93	–115	0.005	138	0.887	170
840	0.669	–117	7.54	–117	0.005	133	0.885	170
860	0.668	–118	7.30	–119	0.005	130	0.888	170
880	0.673	–119	7.18	–121	0.006	129	0.885	169
900	0.672	–120	7.07	–123	0.006	131	0.883	169
920	0.672	–122	6.90	–127	0.006	130	0.883	168
940	0.672	–123	6.65	–130	0.006	130	0.882	168
960	0.673	–124	6.37	–133	0.007	127	0.881	168
980	0.682	–126	6.10	–136	0.007	130	0.88	168
1000	0.679	–127	5.83	–138	0.006	123	0.881	167
1100	0.685	–134	4.81	–145	0.007	120	0.874	166
1200	0.705	–143	4.67	–152	0.008	121	0.868	165
1300	0.703	–152	4.06	–165	0.010	113	0.855	164
1400	0.704	–161	3.69	–175	0.011	106	0.838	163
1500	0.646	–174	3.19	160	0.011	86	0.826	166

Table 3. Scattering Parameters

(V_{DD} = 3.6 V, V_{SS}, V_{G1}, V_{G2} Set for I_{DQ1}= 150 mA and I_{DQ2} = 750 mA, 50 Ω System)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
500	0.737	–85	14.12	–84	0.002	135	0.887	174
600	0.792	–83	5.47	–103	0.002	130	0.866	170
700	0.799	–112	12.69	–80	0.004	157	0.853	174
800	0.687	–115	9.13	–115	0.005	131	0.881	171
820	0.681	–116	8.56	–117	0.005	131	0.882	171
840	0.680	–117	8.12	–119	0.005	132	0.882	170
860	0.678	–118	7.83	–121	0.005	131	0.883	170
880	0.680	–119	7.69	–123	0.005	129	0.882	170
900	0.681	–120	7.53	–125	0.006	133	0.882	169
920	0.680	–122	7.36	–129	0.006	127	0.879	169
940	0.681	–123	7.09	–132	0.006	130	0.878	169
960	0.681	–125	6.77	–135	0.006	121	0.878	168
980	0.688	–126	6.47	–137	0.006	123	0.878	168
1000	0.684	–128	6.18	–139	0.006	123	0.876	168
1100	0.690	–135	5.08	–147	0.007	116	0.870	166
1200	0.707	–143	4.90	–153	0.007	123	0.862	165
1300	0.701	–153	4.24	–167	0.009	112	0.852	164
1400	0.704	–162	3.83	–176	0.010	107	0.833	164
1500	0.643	–174	3.26	160	0.010	84	0.828	167

Table 4. Scattering Parameters

(V_{DD} = 4.2 V, V_{SS}, V_{G1}, V_{G2} Set for I_{DQ1}= 150 mA and I_{DQ2} = 750 mA, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
500	0.740	–85	15.59	–86	0.002	139	0.880	174
600	0.798	–84	5.71	–103	0.002	135	0.859	171
700	0.802	–112	13.82	–81	0.004	154	0.851	174
800	0.694	–116	9.82	–116	0.005	137	0.879	171
820	0.688	–116	9.20	–119	0.005	132	0.883	171
840	0.684	–117	8.70	–121	0.004	137	0.877	171
860	0.688	–119	8.37	–123	0.005	133	0.879	170
880	0.684	–120	8.20	–125	0.005	129	0.879	170
900	0.686	–121	8.03	–127	0.005	127	0.879	169
920	0.685	–123	7.82	–131	0.006	130	0.879	169
940	0.682	–124	7.53	–134	0.005	127	0.875	169
960	0.687	–126	7.18	–137	0.006	126	0.874	169
980	0.694	–127	6.84	–139	0.006	124	0.875	168
1000	0.686	–129	6.53	–141	0.006	123	0.873	168
1100	0.692	–137	5.34	–149	0.006	116	0.866	167
1200	0.704	–145	5.12	–155	0.007	122	0.861	165
1300	0.698	–154	4.41	–168	0.009	113	0.847	165
1400	0.695	–163	3.94	–178	0.010	104	0.835	164
1500	0.638	–175	3.34	159	0.009	84	0.828	167

APPLICATIONS INFORMATION

Design Philosophy

The MRFIC0917 is a two–stage Integrated Power Amplifier designed for use in cellular phones, especially for those used in GSM Class IV, 3.6 V operation. Due to the fact that the input, output and some of the interstage matching is accomplished off chip, the device can be tuned to operate anywhere within the 800 to 1000 MHz frequency range.

This capability makes the MRFIC0917 suitable for portable cellular applications such as:

- 3.6 V 900 MHz DAMPS
- 3.6 V 900 MHz PDC

RF Circuit Considerations

The MRFIC0917 can be tuned by changing the values and/or positions of the appropriate external components. Refer to Figure 2, a typical GSM Class IV applications circuit.

The input match is a shunt–C, series–L, low–pass structure and can be retuned as desired with the only limitation being the on–chip 12 pF blocking capacitor. For saturated applications such as GSM and analog cellular, the input match should be optimized at the rated RF input power.

Interstage matching can be optimized by changing the value and/or position of the decoupling capacitor on the V_{D1} supply line. Moving the capacitor closer to the device or reducing the value increases the frequency of resonance with the inductance of the device's wirebonds and leadframe pin.

Output matching is accomplished with a two–stage low–pass network as a compromise between bandwidth and harmonic rejection. Implementation is through chip capacitors mounted along a 30 or 50Ω microstrip transmission line. Values and positions are chosen to present a 2Ω loadline to the device while conjugating the device output parasitics. The network must also properly terminate the second and third harmonics to optimize efficiency and reduce harmonic output. When low–Q commercial chip capacitors are used for the shunt capacitors, loss can be reduced by mounting two capacitors in parallel to achieve the total value needed.

Loss in circuit traces must also be considered. The output transmission line and the bias supply lines should be at least 0.6 mm in width to accommodate the peak circulating currents which can be as high as 2 amperes. The bias supply line which supplies the output should include an RF choke of at least 8 nH, surface mount solenoid inductors or equivalent length of microstrip lines. Discrete inductors will usually give better efficiency and conserve board space.

The DC blocking capacitor required at the output of the device is best mounted at the 50Ω impedance point in the circuit where the RF current is at a minimum and the capacitor loss will have less effect.

Power Control Using the MC33169

The MC33169 is a dedicated GaAs power amplifier support IC which provides the –4 V required for V_{SS}, an N–MOS drain switch interface and driver and power supply sequencing. The MC33169 can be used for power control in applications where the amplifier is operated in saturation since the output power in non–linear operation is proportional to V_D^2. This provides a very linear and repeatable power control transfer function. This technique can be used open–loop to achieve 20–25 dB dynamic range over process and temperature variation. With careful design and selection of calibration points, this technique can be used for GSM phase II control where 29 dB dynamic range is required, eliminating the need for the complexity and cost of closed–loop control.

The transmit waveform ramping function required for systems such as GSM can be implemented with a simple Sallen and Key filter on the MC33169 control loop. The amplifier is then ramped on as the V_{RAMP} pin is taken from 0 V to 3 V. To implement the different power steps required for GSM, the V_{RAMP} pin is ramped between 0 V and the appropriate voltage between 0 V and 3 V for the desired output power.

For closed–loop configurations using the MC33169, MMSF4N01HD N–MOS switch and the MRFIC0917 provide a typical 1 MHz 3 dB loop bandwidth. The STANDBY pin must be enabled (3 V) at least 800 μs before the V_{RAMP} pin goes high and disabled (0 V) at least 20 μs before the V_{RAMP} pin goes low. This STANDBY function allows for the enabling of the MC33169 one burst before the active burst thus reducing power consumption.

Biasing Considerations

Gate bias is supplied to each stage separately through resistive division of the V_{SS} voltage. The top of each divider is brought out through pins 12 and 13 (V_{G2} and V_{G1} respectively) allowing gate biasing through use of external resistors or positive voltages. This allows setting the quiescent current of each stage separately.

For applications where the amplifier is operated close to saturation, such as GSM and analog cellular, the gate bias can be set with resistors. Variations in process and temperature will not affect amplifier performance significantly in these applications. The values shown in the Figure 1 will set quiescent currents of 100 to 200 mA for the first stage and 600 to 1200 mA for the second stage.

For linear modes of operation, the quiescent current must be more carefully controlled. For these applications, the V_G pins can be referenced to some tunable voltage which is set at the time of radio manufacturing. Less than 1.0 mA is required in the divider network so a DAC can be used as the voltage source. Typical settings for 3.6 V linear operation are 150 mA ±5% for the first stage, and 750 mA ±5% for the second stage.

Conclusion

The MRFIC0917 offers the flexibility in matching circuitry and gate biasing required for portable cellular applications. Together with the MC33169 support IC, the device offers an efficient system solution for TDMA applications such as GSM where saturated amplifier operation is used.

Evaluation Boards

Evaluation boards are available for RF Monolithic Integrated Circuits. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

MOTOROLA

MRFIC0919

Advance Information

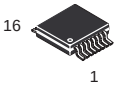
3.6 V GSM GaAs Integrated Power Amplifier

The MRFIC0919 is a single supply, RF power amplifier designed for the 2.0 W GSM900 handheld radio. The negative power supply is generated inside the chip using RF rectification, which avoids any spurious signal. A built in priority switch is provided to prevent Drain Voltage being applied on the RF lineup if not properly biased by the Negative Voltage. The device is packaged in the TSSOP–16EP package, with exposed backside pad, which allows excellent electrical and thermal performance through a solderable contact.

- Target 3.6 V Characteristics:
  - RF Input Power: 3.0 dBm
  - RF Output Power: 35.3 dBm Typical
  - Efficiency: 53% Typical
- Single Positive Supply Solution
- Negative Voltage Generator
- Positive Step–up Voltage Generator
- V_{SS} Check Switch for Gate–Drain Priority

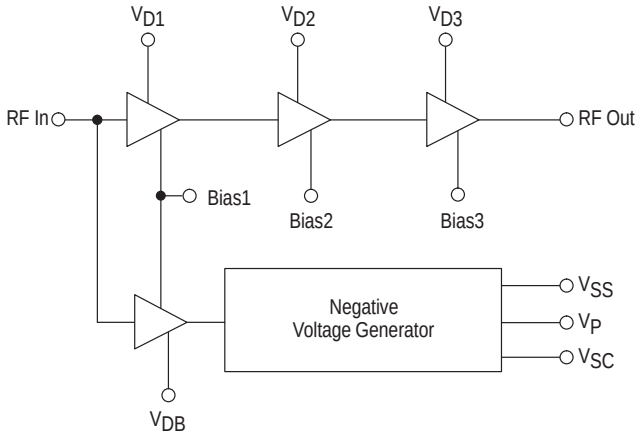
GSM 880 – 915 MHz
INTEGRATED
POWER AMPLIFIER

SEMICONDUCTOR
TECHNICAL DATA



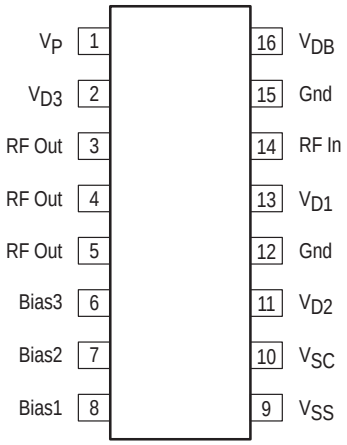
PLASTIC PACKAGE
CASE 948L
(TSSOP–16EP, Tape and Reel Only)

Simplified Block Diagram



This device contains 8 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temp Range	Package
MRFIC0919R2	T_A = –40 to 85°C	TSSOP–16EP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	$V_{D1, 2, 3}$	6.0	V
RF Input Power	P_{in}	12	dBm
RF Output Power	P_{out}	38	dBm
Operating Case Temperature Range	T_C	–40 to 85	°C
Storage Temperature Range	T_{stg}	–55 to 150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Contitions or Electrical Characteristics tables.
2. Meets Human Body Model (HBM) ≤250 V and Machine Model (MM) ≤60 V. This device is rated Moisture Sensitivity Level (MSL) 4. ESD data available upon request.
3. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DB}, $V_{D1, 2, 3}$	–	3.0 to 5.5	–	Vdc
Input Power	P_{in}	–	3.0 to 8.0	–	dBm

ELECTRICAL CHARACTERISTICS (V_{DB} = 3.6 V, $V_{D1, 2, 3}$ = 3.6 V, P_{in} = 3.0 dBm, Peak measurement at 12.5% duty cycle, 4.6 ms Period, T_A = 25°C, unless otherwise noted.)

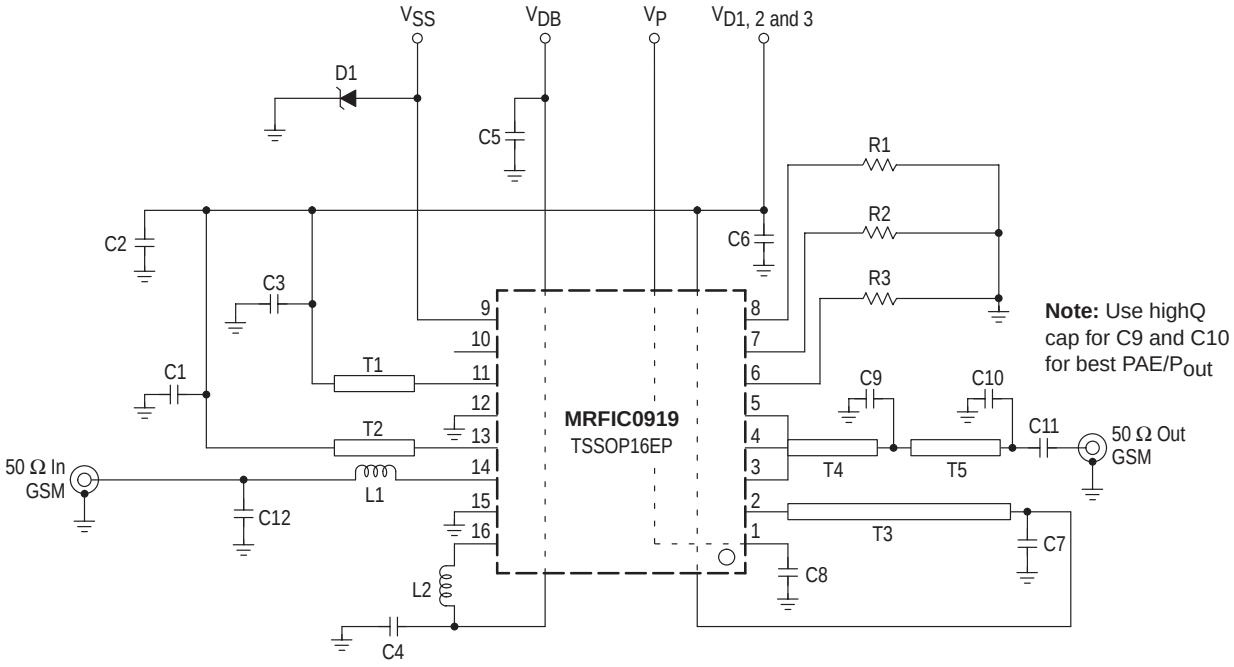
Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	880	–	915	MHz
Output Power	P_{out}	34.5	35.3	–	dBm
Power Added Efficiency	PAE	45	53	–	%
Output Power at Low Voltage ($V_{D1, 2, 3}$ = 3.0 V)	P_{out}	33	33.7	–	dBm
Harmonic Output $2f_0$ $\geq 3f_0$	 – –	 – –	 40 45	 35 40	dBc
Input Return Loss	|S11|	–	12	–	dB
Output Power Isolation (P_{in} = 8.0 dBm, V_{DB} = 3.0 V, $V_{D1, 2\&3}$ = 0 V)	P_{off}	–	–32	–	dBm
Noise Power in Rx band 925 to 960 MHz (100 kHz measurement bandwidth)	NP	–	–90	–	dBm
Negative Voltage (P_{in} = 3.0 dBm, V_{DB} = 3.0 V, $V_{D1, 2\&3}$ = 0 V)	V_{ss}	–4.85	–	–	V
Negative Voltage Setting Time (P_{in} = 3.0 dBm, VDB stepped from 0 to 3.0 V)	T_s	–	0.7	–	µs
Stability–Spurious Output (P_{out} = 5.0 to 35 dBm, Load VSWR 6:1 all phase angles, source VSWR = 3:1, at any phase angle, Adjust $V_{D1, 2\&3}$ for specified power)	P_{spur}	–	–	–60	dBc
Load Mismatch Stress (P_{out} = 5.0 to 35 dBm, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust $V_{D1, 2\&3}$ for specified power)	No Degradation in Output Power Before & After Test				
Positive Voltage (P_{in} = 3.0 dBm, V_{DB} = 3.0 V)	V_P	6.0	–	–	V

Table 1. Optimum Loads Derived from Circuit Characterization

f MHz	Z_{in} OHMS		Z_{OL}* OHMS	
	R	jX	R	jX
880	9.83	–75.84	1.79	2.34
885	9.88	–76.75	1.78	2.46
890	9.83	–77.65	1.76	2.57
895	9.82	–78.60	1.75	2.67
900	9.82	–79.50	1.74	2.80
905	9.79	–80.35	1.73	2.90
910	9.78	–81.23	1.71	3.00
915	9.75	–82.18	1.70	3.13

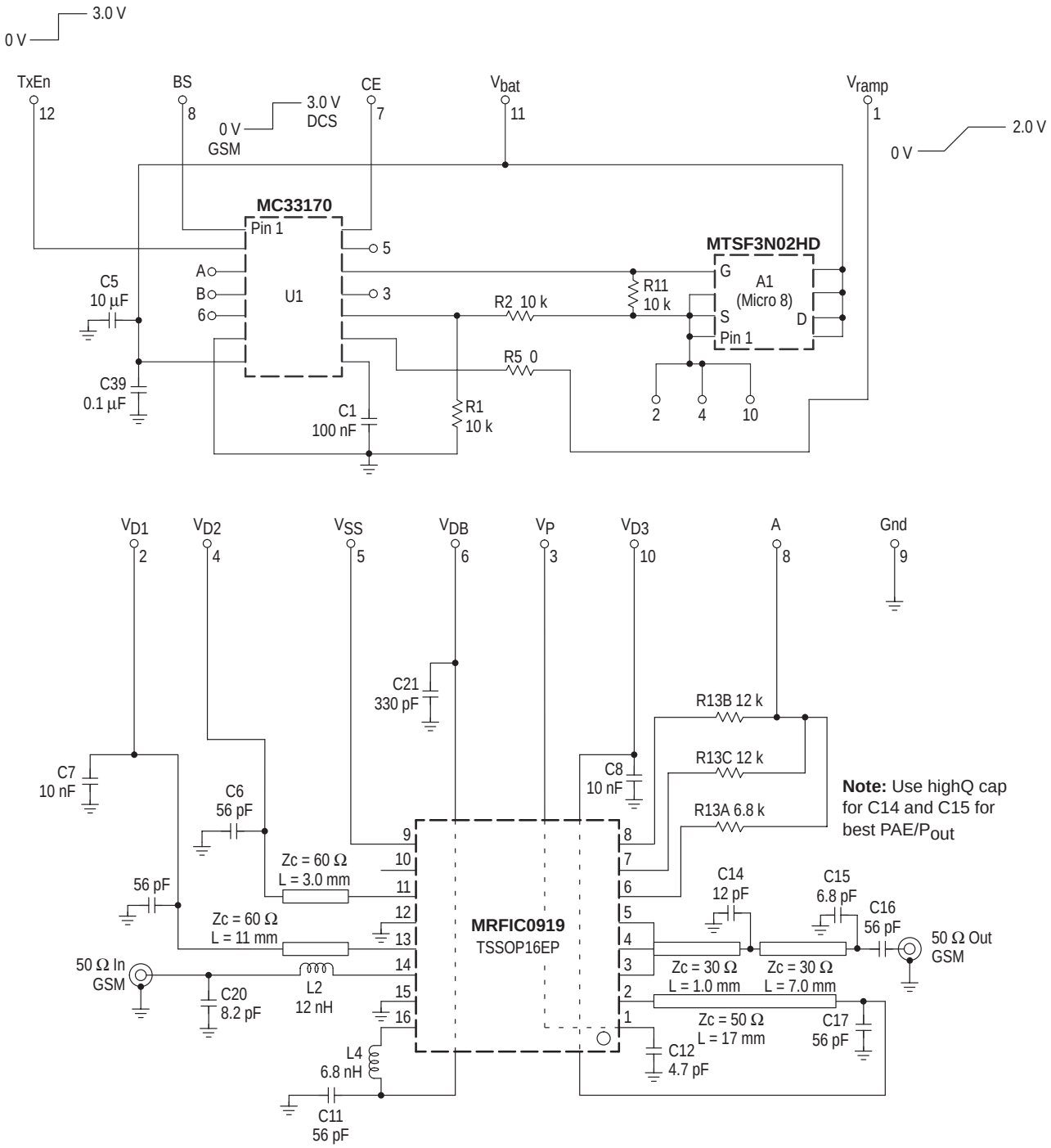
Z_{in} represents the input impedance of the device.
Z_{OL}* represents the conjugate of the optimum output load to present to the device.

Figure 1. Reference Circuit



C1, C3, C4, C7, C11	56 pF		R1, R2	12 k
C2, C6	10 nF		R3	6.8 k
C5	330 pF		T1	60 Ω Microstrip Line, L = 3.0 mm
C8	4.7 pF		T2	60 Ω Microstrip Line, L = 11 mm
C9	12 pF	AVX Accu–F	T3	50 Ω Microstrip Line, L = 17 mm
C10	6.8 pF	AVX Accu–F	T4	30 Ω Microstrip Line, L = 1.0 mm
C12	8.2 pF		T5	30 Ω Microstrip Line, L = 7.0 mm
L1	12 nH			
L2	6.8 nH			
D1	Zener 5.1 V	MMSZ4689T1		

Figure 2. 3.6 V GSM IPA MRFIC0919 Application Circuit



Note: I/O labels and pin numbers refer to demoboard connector pin out.

Figure 3. 3.6 V GSM & DCS IPA Dual–Band Application Circuit with Companion Chip & NMOS Switch

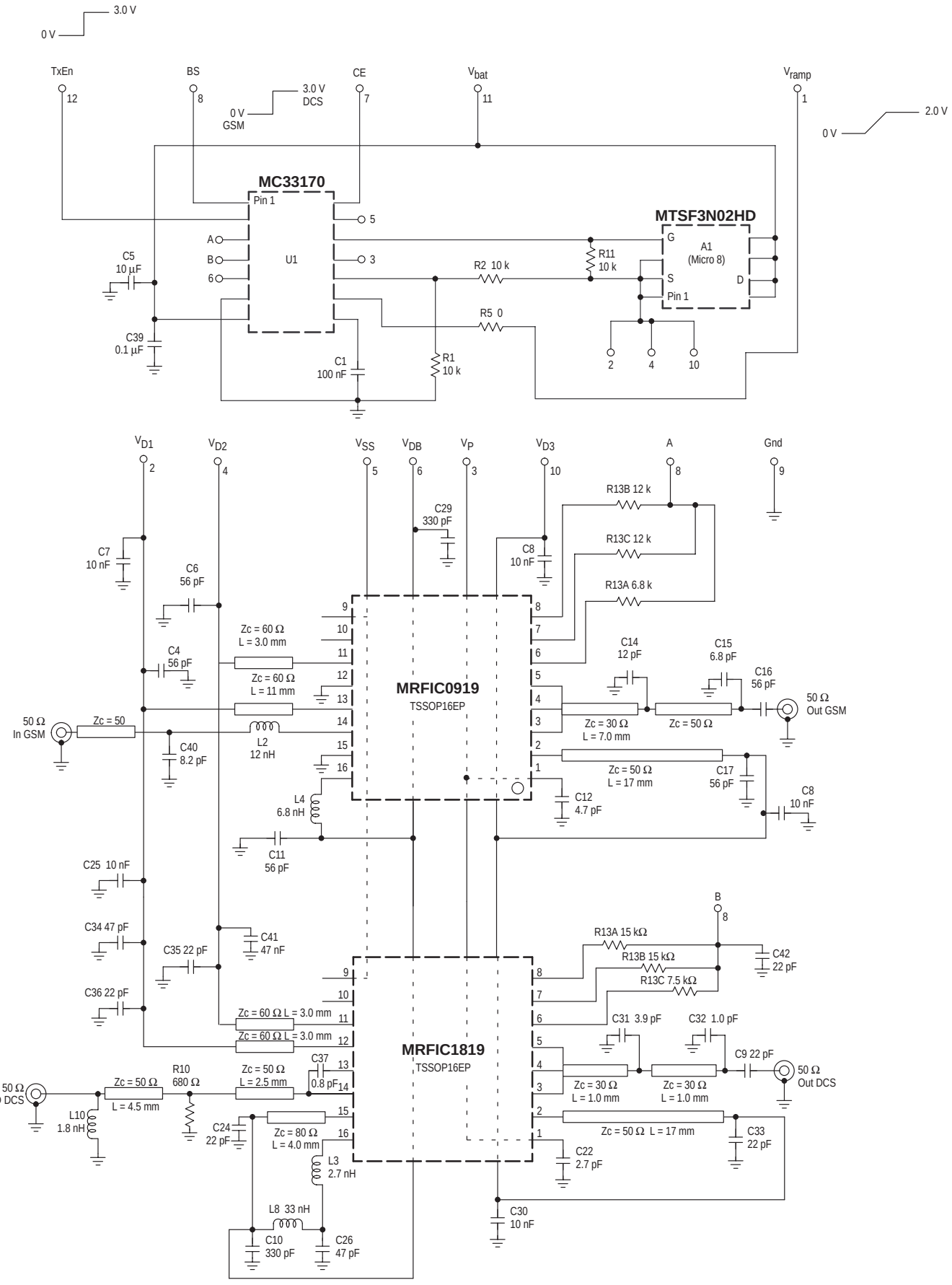


Figure 4. Output Power versus Frequency

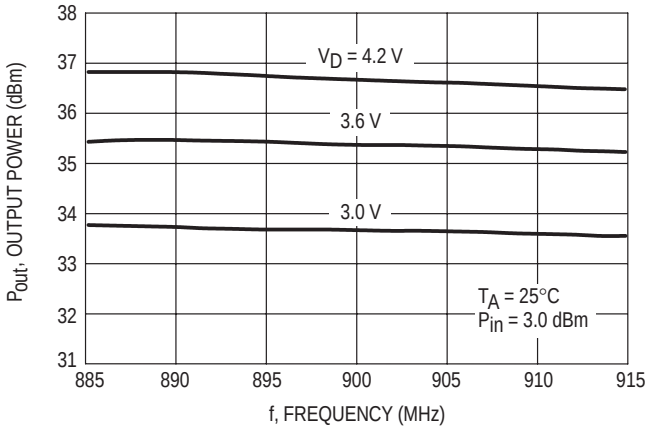


Figure 5. Power Added Efficiency versus Frequency

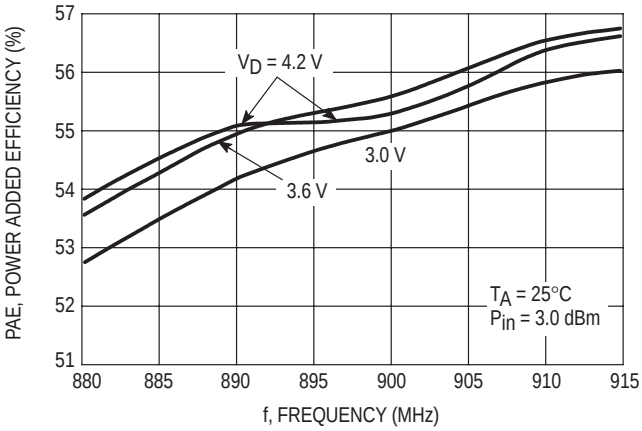


Figure 6. Output Power versus Frequency

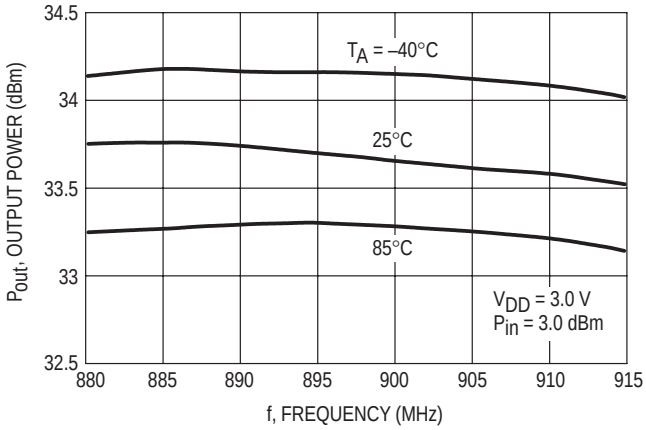


Figure 7. Output Power versus Frequency

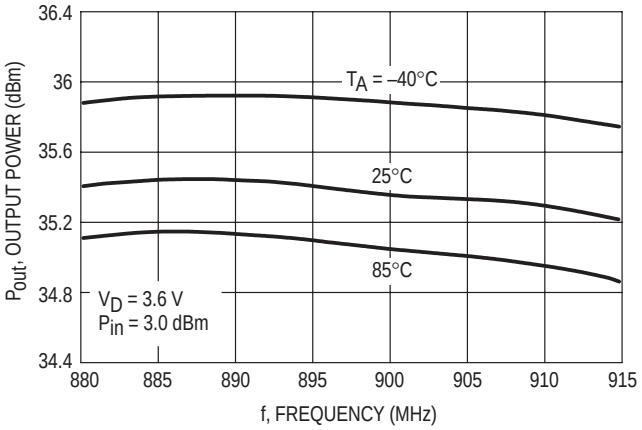


Figure 8. Output Power versus Frequency

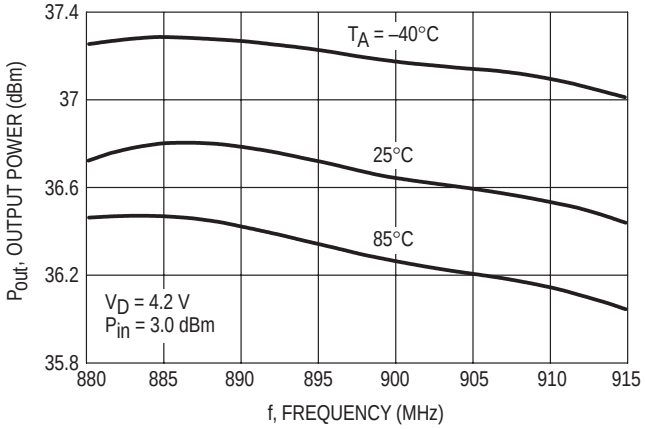


Figure 9. Power Added Efficiency versus Frequency

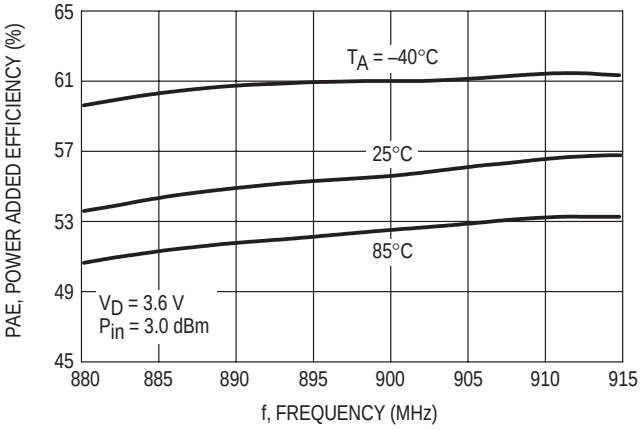


Figure 13. Output Power versus Drain Voltage

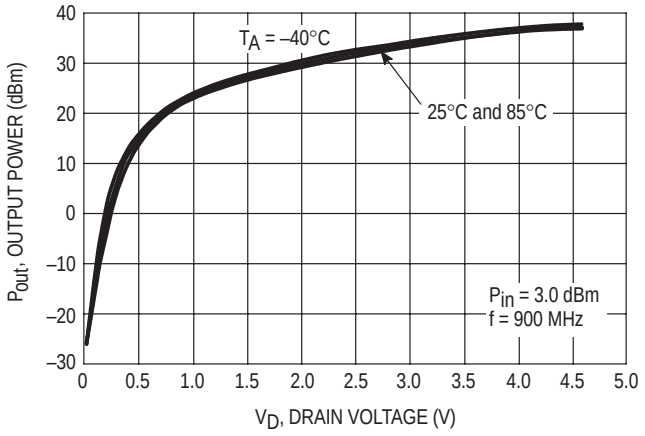


Figure 12. Power Added Efficiency versus Drain Voltage

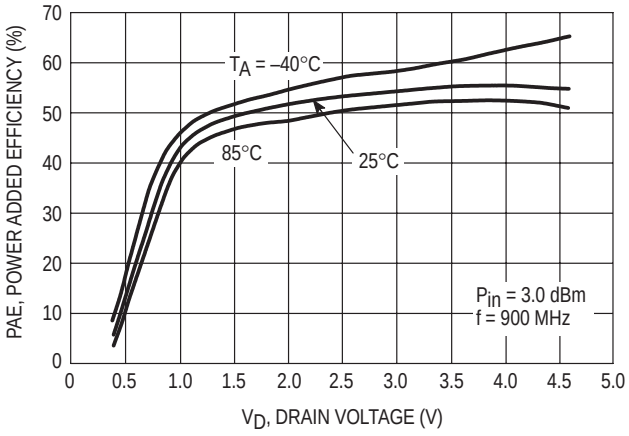


Figure 11. Positive Voltage Generator Output versus Drain Voltage

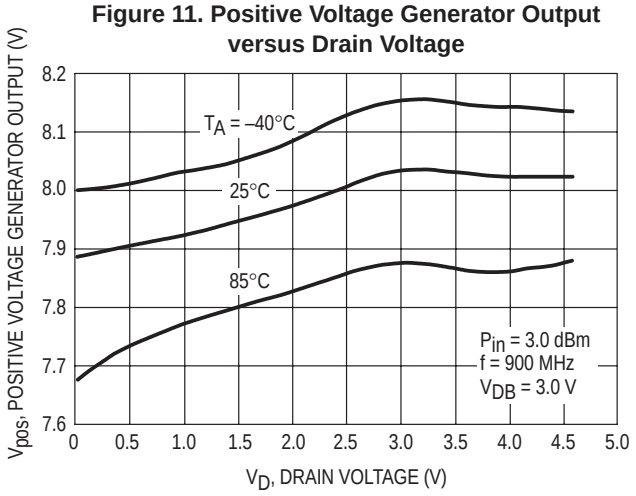


Figure 10. Positive Voltage Output versus Frequency

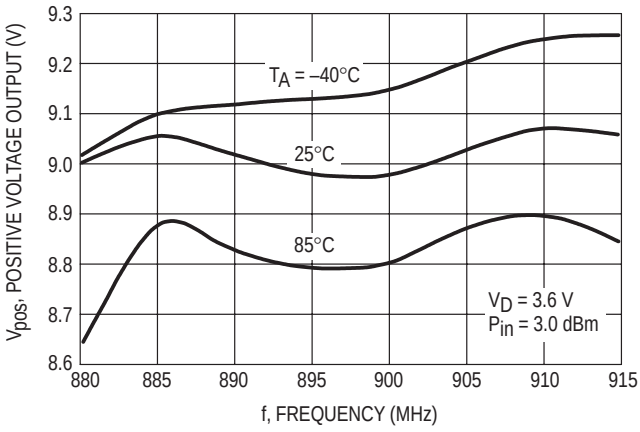


Figure 14. Second Harmonics versus Drain Voltage

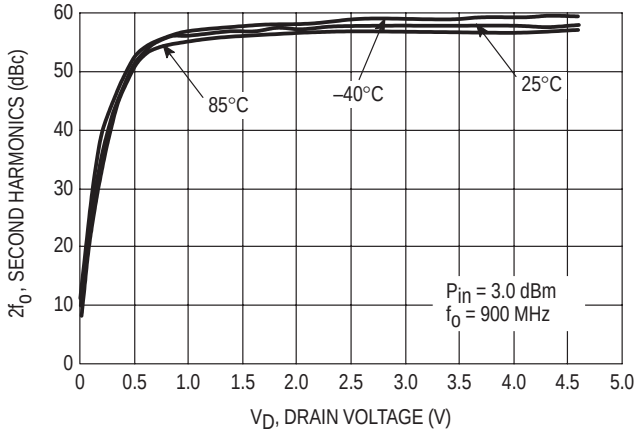
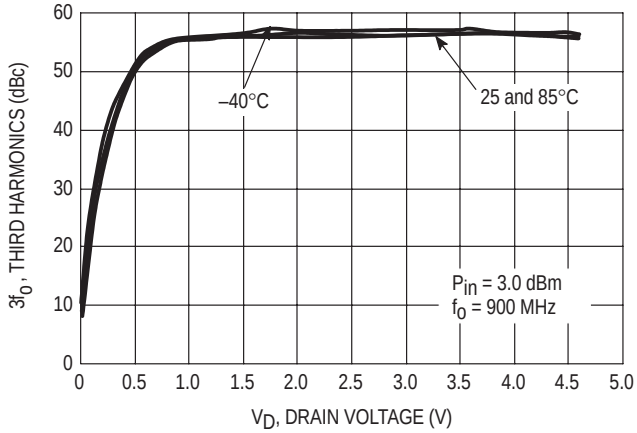


Figure 15. Third Harmonics versus Drain Voltage



APPLICATIONS INFORMATION

Design Philosophy

The MRFIC0919 is a high performance three stage GaAs IPA (Integrated Power Amplifier) designed for GSM handheld radios (880 to 915 MHz frequency band). With a 3.6 V battery supply, it delivers typically 35.3 dBm of Output Power with 53% Power Added Efficiency.

It features an internal Negative Voltage Generator based on RF rectification of the input carrier after its amplification by a dedicated buffer stage (see Internal Block Diagram). This method eliminates spurs found on the Output signal when using DC/DC converter type negative voltage generators, either on or off chip. The buffer also generates a step–up positive voltage which can be used to drive a N–MOS drain switch.

The RF input power is split internally to the 3 stage RF line–up (Q1,Q2 andQ3) and the Buffer. This arrangement allows separate operation of Voltage Generation and Power Amplification for maximum flexibility.

External Circuit Considerations

The MRFIC0919 can be tuned by changing the values and/or positions of the appropriate external components (see Figure 1. Reference Circuit). While tuning the RF line–up, it is recommended to apply external negative supply in order to prevent any damage to the power amplifier stages. Poor tuning on the input may not provide enough RF power to operate the negative voltage generator properly.

Input matching is a shunt–C, series–L low–pass structure and should be optimized at the rated RF Input power (e.g., 3.0 dBm). Since the Input line feeds both 1st stage and buffer, Input matching should be iterated with Buffer and Q1 drain matching. Note that a DC blocking capacitor is included on chip.

Buffer drain is supplied and matched through a discrete chip inductor. Its value is tuned to get the maximum output from voltage generator.

The step–up positive voltage available at Pin 1 is both decoupled and maximized by a small shunt capacitor. This positive voltage which is approximately twice the buffer drain voltage can be used to drive a N–MOS drain switch for best performance.

Q1 drain is supplied and matched through a printed microstrip line that could be replaced by a discrete chip inductor as well. Its length (or equivalent inductor value) is tuned by sliding the RF decoupling capacitor along to get the maximum gain on the first stage. Make sure when laying out the PCB to put enough ground pads and vias close to the microstrip lines to help for this fine tuning.

Q2 is supplied through a printed microstrip line that contributes also to the interstage matching in order to provide optimum drive to the final stage. The line length is very small so replacing it with a discrete inductor is not practical.

Q3 drain is feed via a printed line that must handle the high supply current of that stage (2.0 to 3.0 Amp peak) without significant voltage drop. This line can be buried in an inner layer to save PCB space or be a discrete RF choke.

Output matching is accomplished with a two stage low–pass network. Easy implementation is achieved with shunt capacitors mounted along a 30 Ω microstrip transmission line. Value and position are chosen to reach a load line of 1.8 Ω while conjugating the device output parasitics. The network must also properly terminate the second and third harmonic to optimize efficiency and reduce harmonic level. Use of high Q capacitor for the output matching circuit is recommended in order to get the best Output Power and Efficiency performance.

Biasing Considerations

The internally generated negative voltage is clamped by an external Zener diode in order to eliminate variation linked to Input power or Buffer supply. This negative voltage is used by three independent bias circuits to set the proper quiescent current of all stages. Each bias circuit is equivalent to a current source sinking its value from the bias pin. When the bias pins are grounded, nominal quiescent current and operating point of each RF stage are selected.

Q1 and Buffer share the Bias1 (0.25 mA) while Q2 and Q3 have dedicated Bias2 (0.25 mA) and Bias3 (0.5 mA) respectively. It is also possible to reference those bias pins to higher voltage than Gnd by using a series resistor that drops the equivalent voltage.

If those pins are left open, the corresponding stages are pinched–off. Thus the bias pins can be used as a means to select the MRFIC0919 or MRFIC1819 in a dual band configuration. The MRFIC1819 is the partner device to the MRFIC0919 and is designed for DCS1800/PCS1900 applications.

Table 2. Pin Function Description

Pin	Symbol	Description
1	V_P	Positive voltage output
2	V_{D3}	Third stage drain supply
3	RF Out	RF output
4	RF Out	RF output
5	RF Out	RF output
6	Bias3	Third stage bias
7	Bias2	Second stage bias
8	Bias1	Buffer and first stage bias
9	V_{SS}	Negative voltage output
10	V_{SC}	Negative voltage check
11	V_{D2}	Second stage drain supply
12	Gnd	Tied to ground externally
13	V_{D1}	First stage drain supply
14	RF In	RF input
15	Gnd	Tied to ground externally
16	V_{DB}	Buffer stage drain supply

V_{SC} is an open drain internal FET switch which is biased through the negative voltage. Consequently, this pin is high impedance when negative voltage is okay and low impedance (about 40 Ω) when negative voltage is missing.

Operation Procedure

The MRFIC0919 is a standard MESFET GaAs Power Amplifier, presence of a negative voltage to bias the RF line–up is essential in order to avoid any damage to the parts. Due to the fact that the negative voltage is generated through rectification of the RF input signal, a minimum input power

level is needed for correct operation of the demoboard. The following procedure will guaranty safe operation for doing the RF measurements.

Note: make sure that Bias1 (pin 8) is connected to ground or will have equivalent potential for nominal biasing of Buffer stage.

1. Apply RF input power (RF In) >3.0 dBm.
2. Apply V_{DB} = 3.0 to 5.0 V.
3. Check that Vss reaches approximatively –5.1 V (settling of the negative voltage).
4. Apply $V_{D1,2\&3}$ 0 to 5.0 V.
5. Measure RF output power and relevant parameters.

Proceed in the reverse order to switch off the Power Amplifier.

Control Considerations

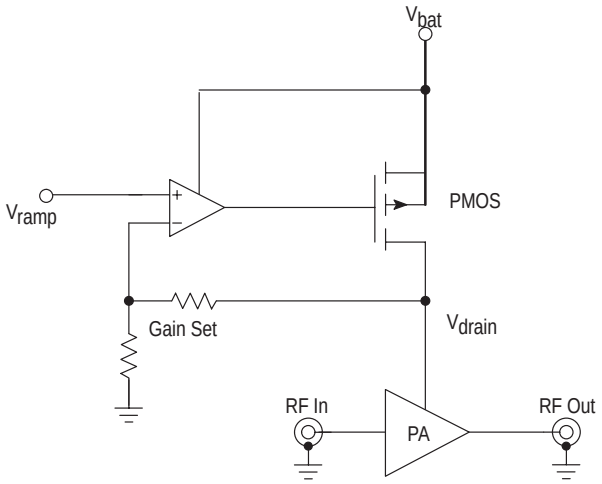
MRFIC0919 application uses the drain control technique developed for our previous range of GaAs IPAs (refer to application note AN1599). This method relies on the fact that for an RF amplifier operating in satuaration mode, the RF output power is proportional to the square of the Amplifier drain voltage: P_{out}(Watt)=k*Vd(Volt)*Vd(Volt).

In the proposed application circuit (see figure 2: application circuit), a PMOS FET is used to switch the IPA drain and vary the drain supply voltage from 0 to battery voltage. As the PMOS FET has a non linear behavior, an OpAmp is included in the application. This OpAmp is linearizing the PMOS by sensing its drain output and gives a true linear relationship between the Control voltage and the RF output voltage.

The obtained power control transfer function is so linear and repeatable than it can be used to predict the output power within a dynamic of 25 to 30 dB over frequency and temperature range. This so called “open–loop” arrangement eliminates the need for coupler and detector required for the classical but complex closed–loop control and consequently reduces the Insertion Loss from Power Amplifier to the Antenna.

The following block diagram shows the principle of operation as implemented in the application circuit of Figure 2. The OpAmp is connected as an inverter to compensate the negative gain of the PMOS switch.

Figure 16. Drain Control through PMOS Switch



NOTE: The positive voltage generated by the Buffer stage can be used to supply the OpAmp and make it possible to drive a NMOS switch as a voltage follower. Doing so, the main advantage is to have a lower Rdson switch and better intrinsic linearity.

The following plot illustrates the ”open–loop” performance as far as temperature stability. The measured datas are displayed in a log–scale in order to have a good representation of both the dynamic and the linearity of control. The variation of P_{out} accross the frequency band are also very small (less than 1.0 dB ripple) and are kept to that small amount when controlling P_{out} through the Drain voltage.

Figure 17. P_{out} versus V_D

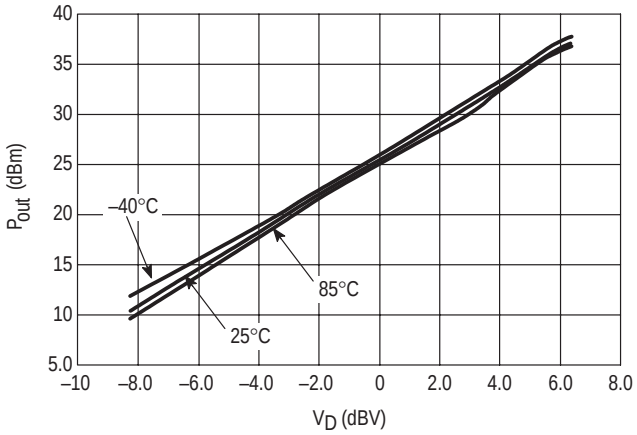
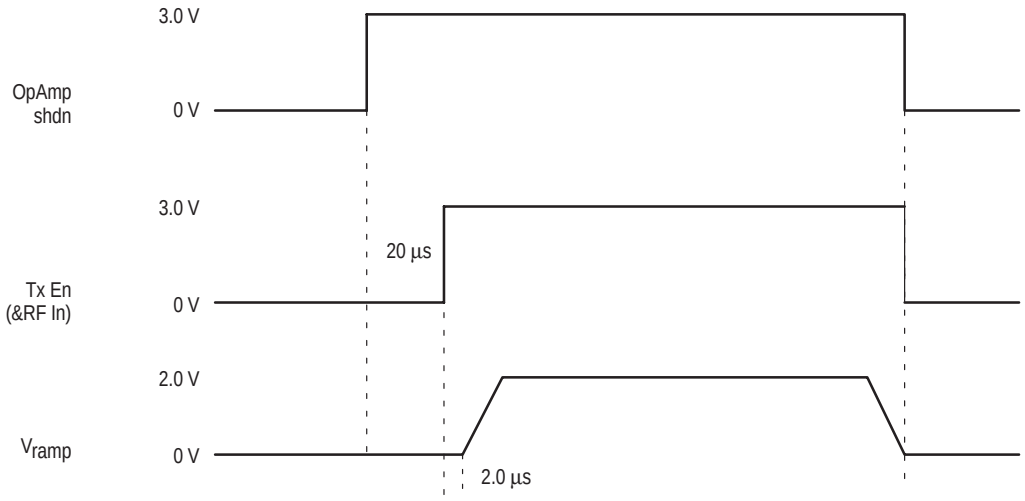


Figure 18. Timing Guide



Burst mode

Use Figure 18 as a guide line to perform burst mode measurements with the complete application circuit of Figure 2. Notice that the V_{SC} pin is connected to V_{ramp} (through a resistor) and act as a pull down when negative voltage is missing so that drain voltage is not applied to the RF line–up.

– Bursting the OpAmp with its Pin 8 (shdn) is not mandatory during a call as the OpAmp current consumption is very small (1.0 to 2.0 mA). This pin is mainly used for the idle mode of the radio. In any case, the wake–up time of the OpAmp is very short.

– V_{ramp} can be applied soon after Tx EN since the internal negative voltage generator settles in less than 2.0 µs.

– Tx EN signal can be used to switch the input power (using a driver or attenuator) in order to provide higher isolation for on/off burst dynamic.

References (Motorola application notes)

AN1599 – Power Control with the MRFIC0913 GaAs Integrated Power Amplifier and MC33169 Support IC.

AN1602 – 3.6 V and 4.8 V GSM/DCS1800 Dual Band PA Application with DECT capability Using Standard Motorola RFIC's.

MOTOROLA

MRFIC0930

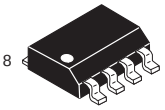
900 MHz GaAs Low Noise Amplifier with Gain Control

Designed primarily for use in 900 MHz wireless communication systems such as GSM, AMPS, and Industrial, Scientific, and Medical (ISM) band applications. The MRFIC0930 is a two–stage low noise amplifier with an integrated step attenuator and is packaged in a low–cost SO–8 package. The MRFIC0930DM is packaged in the smaller Micro–8 package. The attenuator is controlled by a V_{gain} Pin. The LNA can be turned off during transmit mode to save current by using the Rx Enable Pin. The amplifier can be matched to optimize gain or noise figure with simple off–chip input matching.

- Usable Frequency Range = 800 to 1000 MHz
- 19 dB Typ Gain
- Gain Attenuation = 18 dB (Typ)
- 1.7 dB Typ Noise Figure
- Simple Off–chip Matching for Maximum Gain/Noise Figure Flexibility
- High Reverse Isolation = 41 dB (Typ)
- Low Power Consumption = 24 mW (Typ)
- Single Bias Supply = 2.7 to 4.5 V
- Low Standby Current = 20 μA (Typ)
- Low Cost Surface Mount Plastic Package

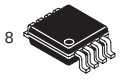
900 MHz GaAs
LOW NOISE AMPLIFIER
WITH GAIN CONTROL

SEMICONDUCTOR
TECHNICAL DATA



(Scale 2:1)

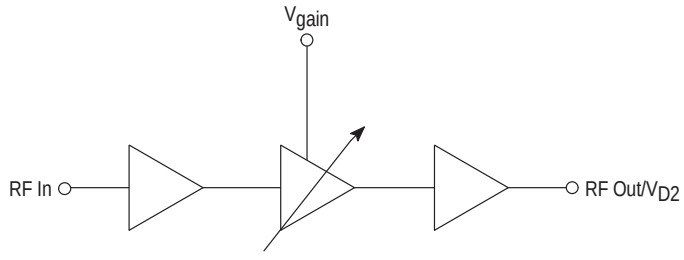
PLASTIC PACKAGE
CASE 751
(SO–8, Tape & Reel Only)



(Scale 2:1)

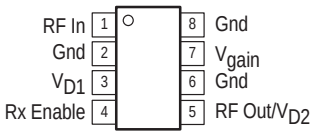
DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8, Tape & Reel Only)

Simplified Block Diagram



This device contains 12 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temp Range	Package
MRFIC0930R2	T_A = –30 to 70°C	SO–8* Tape & Reel
MRFIC0930DMR2		Micro–8** Tape & Reel

*2,500 Units per 16 mm, 13 inch reel.
**2,500 Units per 12 mm, 13 inch reel.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{D1}, V_{D2}	5.5	Vdc
RF Input Power	P_{RF}	3	dBm
Gain Control Voltage	V_{gain}	5.5	Vdc
Enable Voltage	RX Enable	5.5	Vdc
Storage Temperature Range	T_{stg}	–65 to 150	°C
Operating Ambient Temperature	T_A	–30 to 70	°C

NOTES: 1. Meets Human Body Model (HBM) ≤750 V and Machine Model (MM) ≤100 V.
2. ESD data available upon request.

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min	Typ	Max	Unit
RF Frequency	f_{RF}	800	–	1000	MHz
Supply Voltage	V_{D1}, V_{D2}	2.7	–	4.5	Vdc
V_{gain}, High Gain	V_{gain}	–	3.0	–	Vdc
V_{gain}, Low Gain	V_{gain}	–	0	–	Vdc
Rx Enable Voltage, On	Rx Enable	2.7	–	V_{D1}, V_{D2}	Vdc
Rx Enable Voltage, Off	Rx Enable	0	–	0.2	Vdc

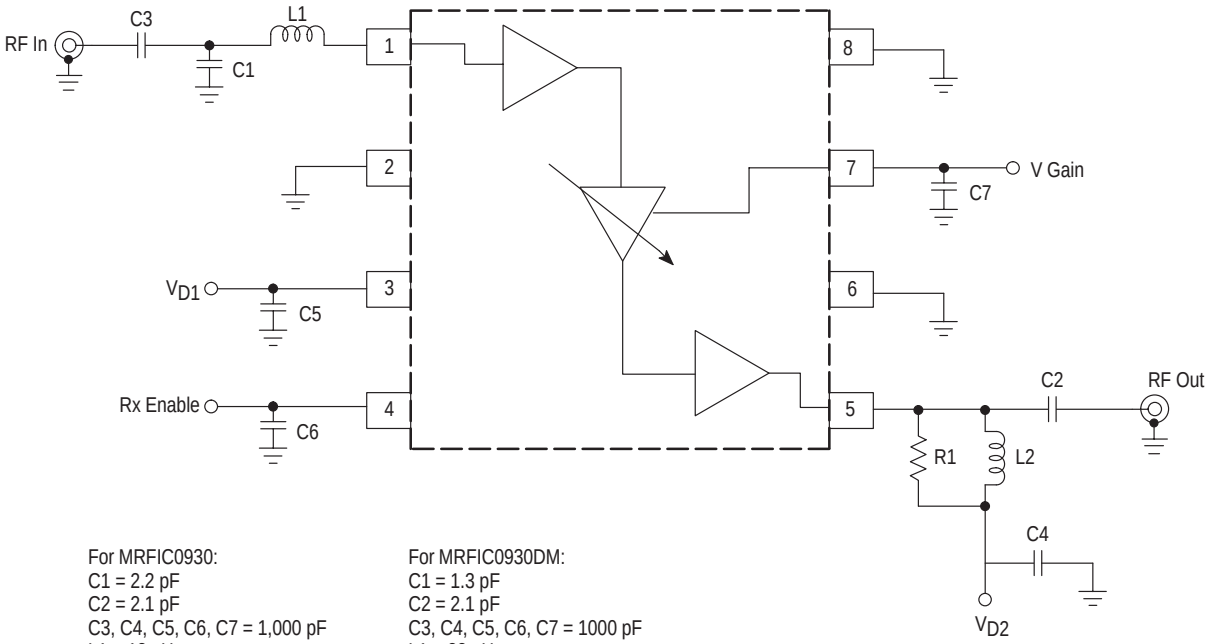
NOTE: To bias, apply V_{D1} and V_{D2} before Rx Enable.

ELECTRICAL CHARACTERISTICS (V_{D1}, V_{D2} = 2.8 V, T_A = 25°C, RF = 940 MHz, Rx Enable = 2.8 V, V Gain = 2.8 V, RF In = –30 dBm, unless otherwise noted. Tested in Circuit Shown in Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
RF Gain MRFIC0930 MRFIC0930DM	S_{21}	 17 17.5	 19 19	 21 21.5	dB
RF Gain (V_{gain} = 0 V)	S_{21}	–	0.8	4.0	dB
SSB Noise Figure [Note]	NF	–	1.7	3.0	dB
SSB Noise Figure (V_{gain} = 0 V) [Note]	NF	–	10.4	–	dB
RF Input 3rd Order Intercept Point [Note]	IIP3	–12	–9.0	–	dBm
RF Input 3rd Order Intercept Point (V_{gain} = 0 V) [Note]	IIP3	–7.0	–5.7	–	dBm
Input 1.0 dB Gain Compression [Note]	P_{1dB}	–21.5	–20.8	–	dBm
Input 1.0 dB Gain Compression (V_{gain} = 0 V) [Note]	P_{1dB}	–16	–11	–	dBm
Reverse Isolation (S_{12})	S_{12}	–	41	–	dB
Input Return Loss	S_{11}	–	15	–	dB
Input Return Loss (V_{gain} = 0 V)	S_{11}	–	15	–	dB
Output Return Loss	S_{22}	–	15	–	dB
Output Return Loss (V_{gain} = 0 V)	S_{22}	–	12	–	dB
Supply Current Rx Mode	I_D	–	8.5	12	mA
Supply Current Standby Mode (Rx Enable = 0 V)	I_D	–	20	200	μA

NOTE: Guaranteed by design.

Figure 1. 900 MHz Test Circuit



For MRFIC0930:
C1 = 2.2 pF
C2 = 2.1 pF
C3, C4, C5, C6, C7 = 1,000 pF
L1 = 18 nH
L2 = 10 nH
R1 = 220 Ω

For MRFIC0930DM:
C1 = 1.3 pF
C2 = 2.1 pF
C3, C4, C5, C6, C7 = 1000 pF
L1 = 22 nH
L2 = 8.2 nH
R1 = 180 Ω

TYPICAL CHARACTERISTICS

(For SO–8 Packaged MRFIC0930)

Figure 2. Reverse Isolation versus Frequency

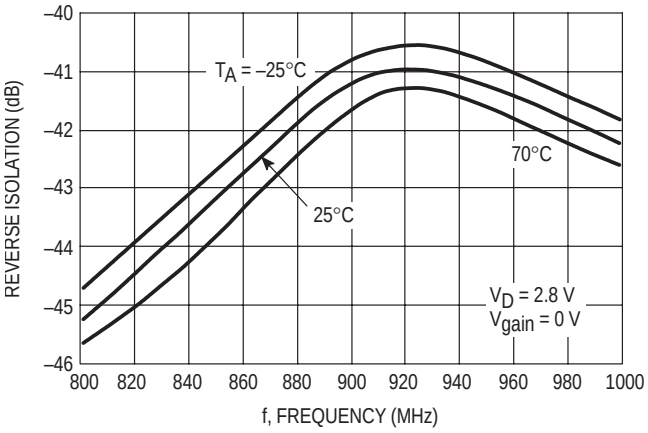


Figure 3. Reverse Isolation versus Frequency

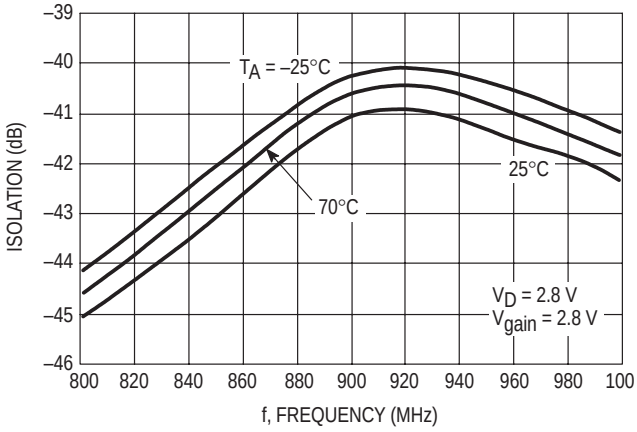


Figure 4. Gain versus Frequency

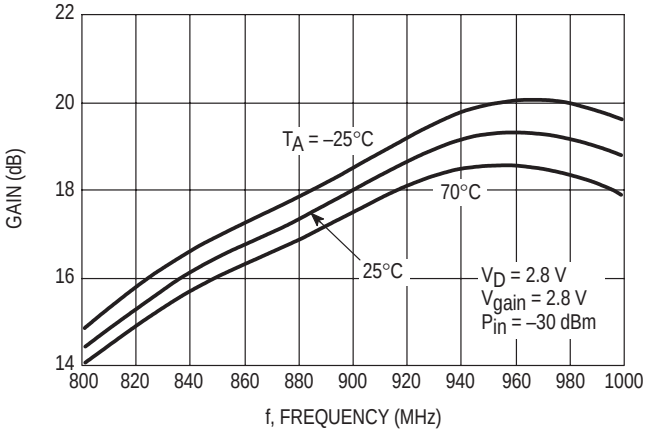


Figure 5. Gain Attenuation versus Frequency

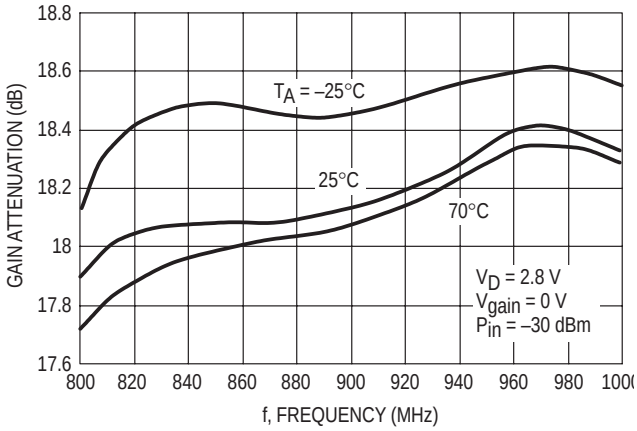


Figure 6. Gain versus Frequency

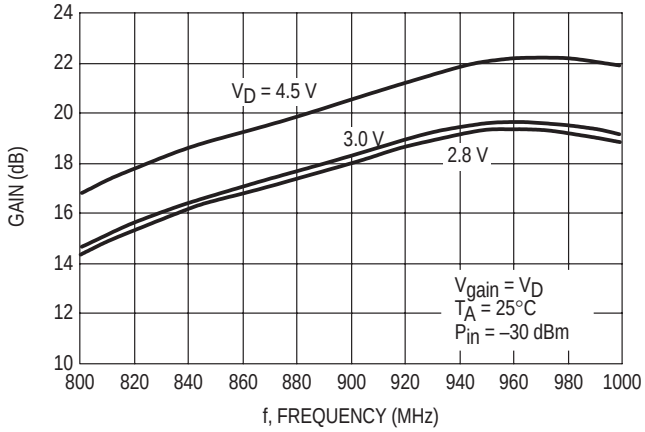
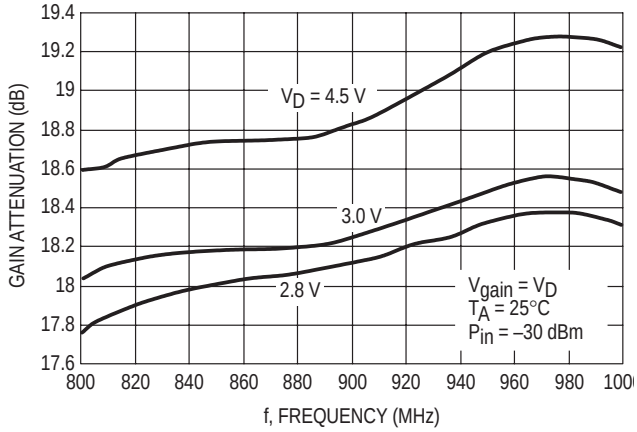


Figure 7. Gain Attenuation versus Frequency



TYPICAL CHARACTERISTICS

(For SO–8 Packaged MRFIC0930)

Figure 8. Input Power versus Output Power

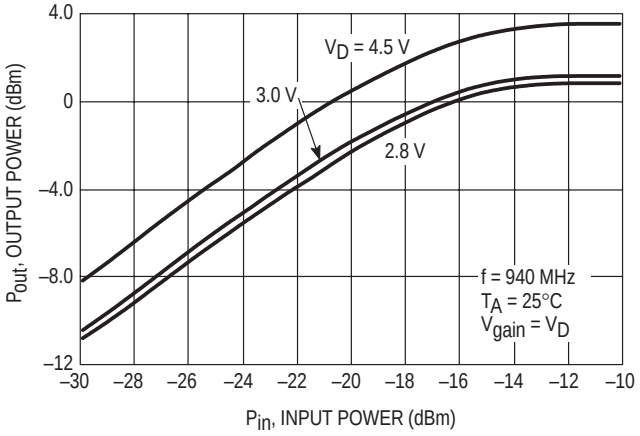


Figure 9. Input Power versus Output Power

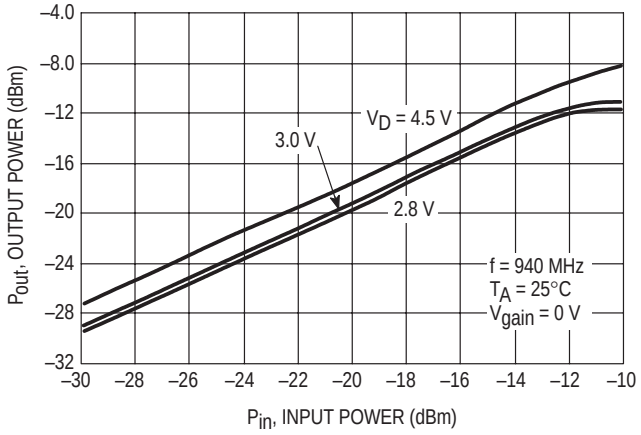


Figure 10. Input Power versus Output Power

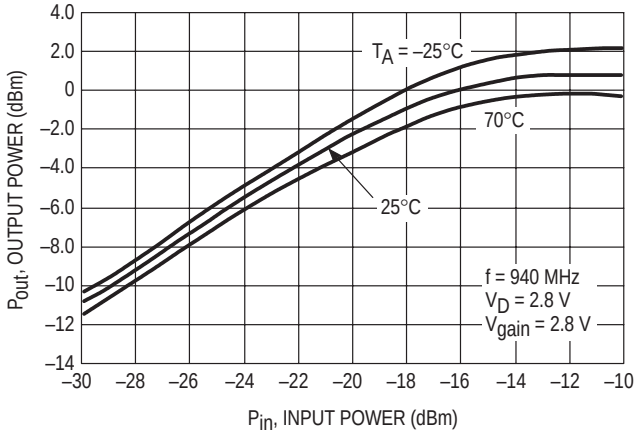


Figure 11. Input Power versus Output Power

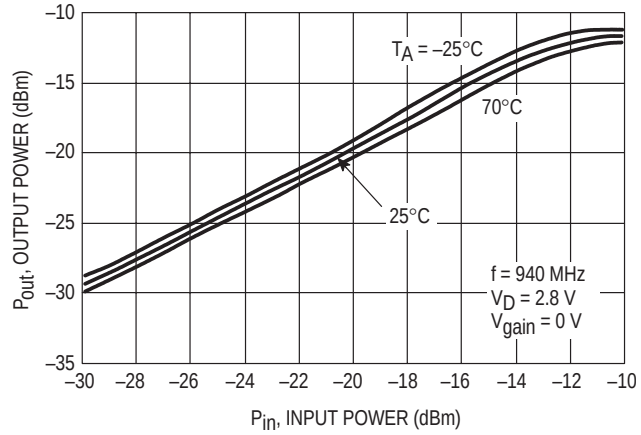


Figure 12. Noise Figure versus Frequency

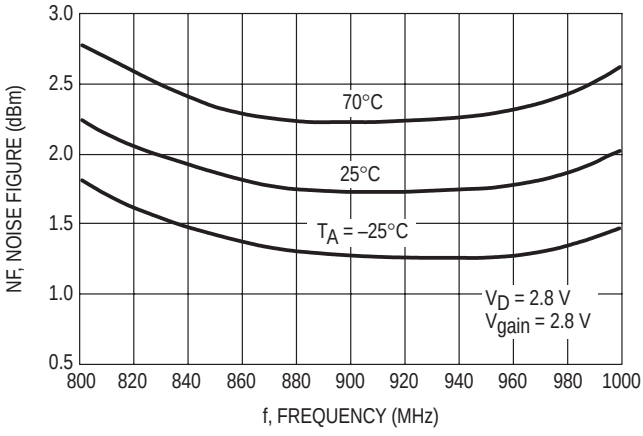
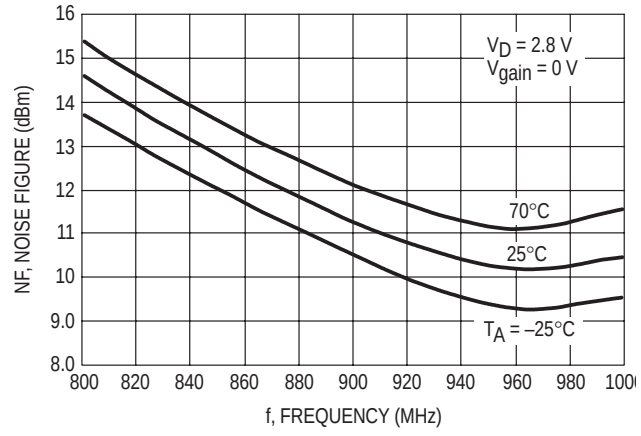


Figure 13. Noise Figure versus Frequency



TYPICAL CHARACTERISTICS

(For Micro–8 Packaged MRFIC0930DM)

Figure 14. Reverse Isolation versus Frequency

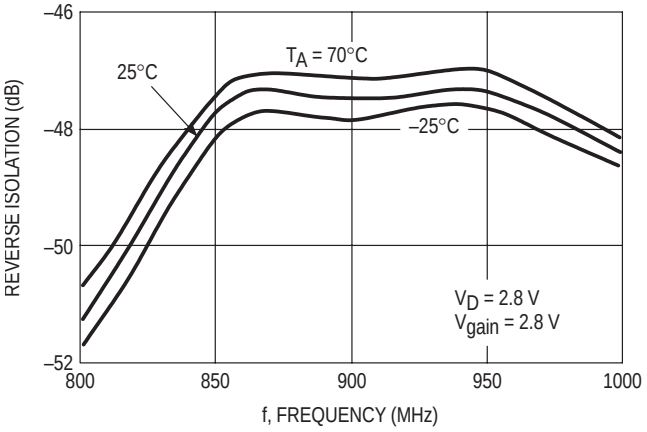


Figure 15. Reverse Isolation versus Frequency

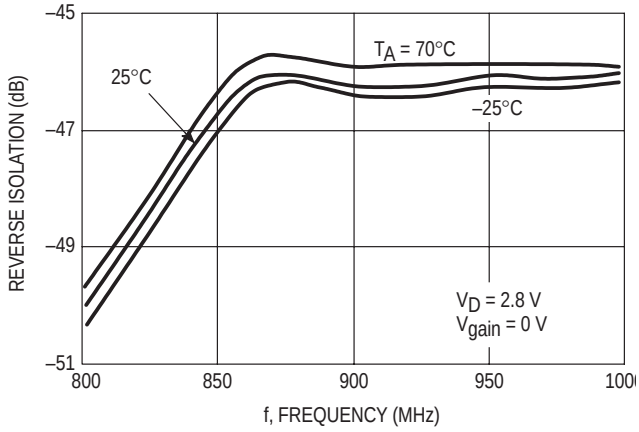


Figure 16. Gain versus Frequency

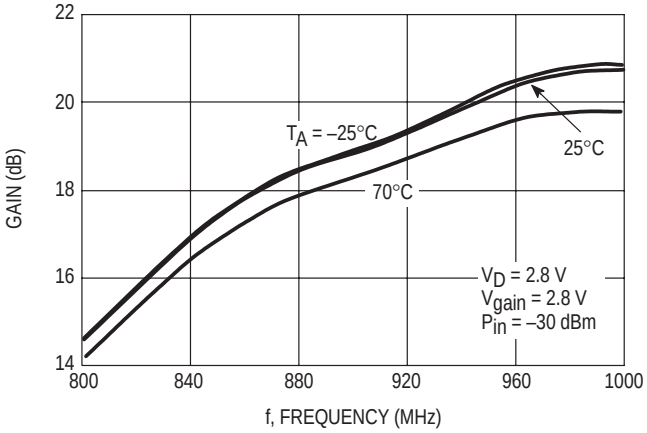


Figure 17. Gain Attenuation versus Frequency

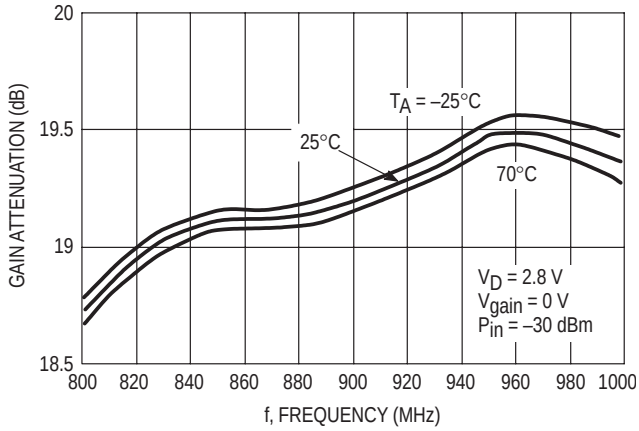


Figure 18. Gain versus Frequency

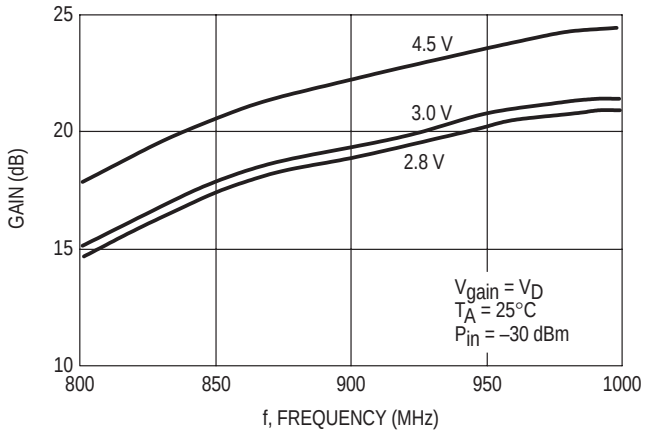
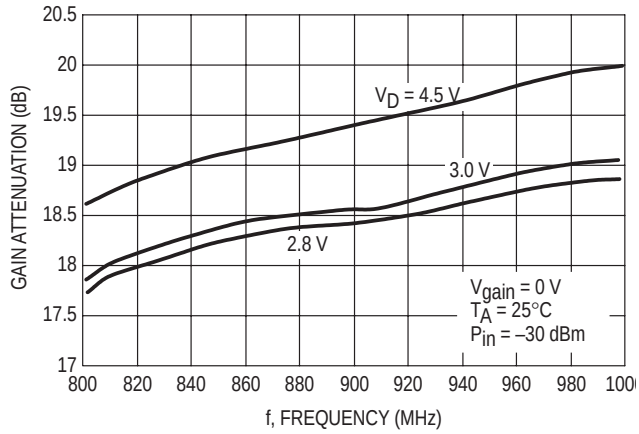


Figure 19. Gain Attenuation versus Frequency



TYPICAL CHARACTERISTICS

(For Micro–8 Packaged MRFIC0930DM)

Figure 20. Input Power versus Output Power

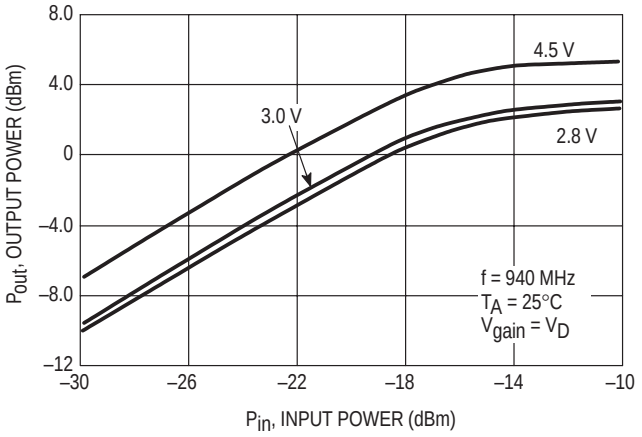


Figure 21. Input Power versus Output Power

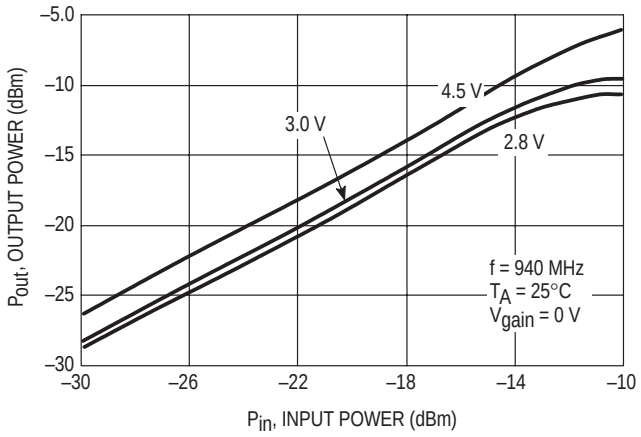


Figure 22. Input Power versus Output Power

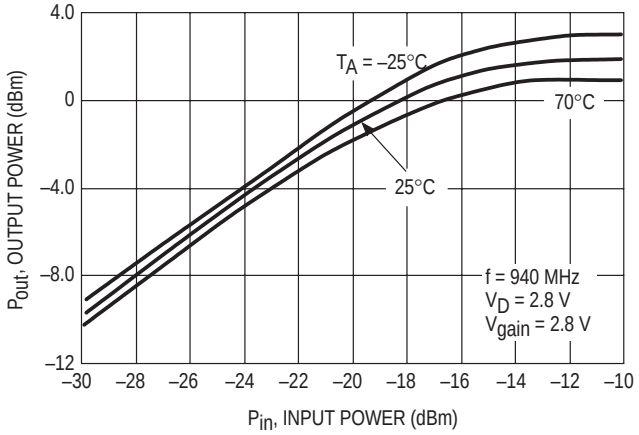


Figure 23. Input Power versus Output Power

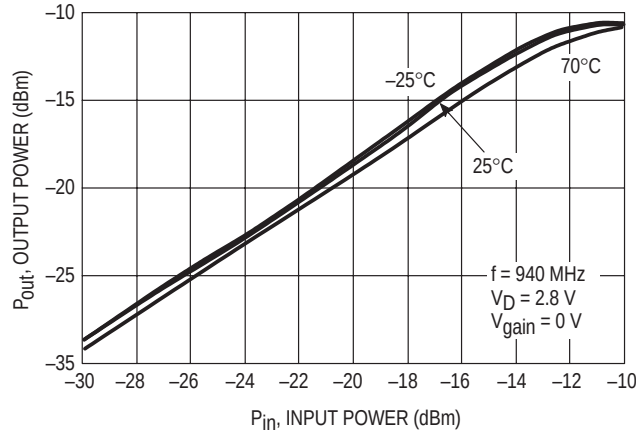


Figure 24. Noise Figure versus Frequency

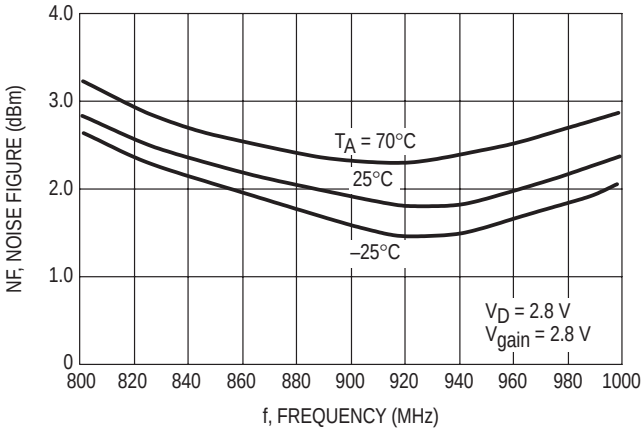
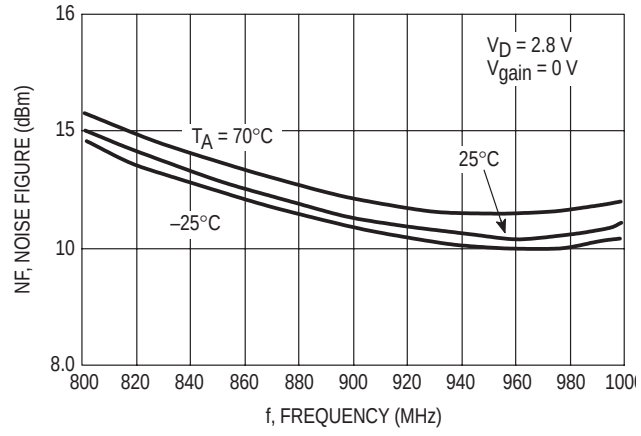


Figure 25. Noise Figure versus Frequency



MOTOROLA

MRFIC0954

Advance Information

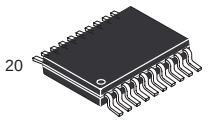
800 MHz CDMA Upmixer/Exciter

The MRFIC0954 is an integrated upmixer and exciter amplifier designed specifically for dual–mode CDMA/AMPS digital cellular radios. The exciter amplifier incorporates a temperature compensated linear gain control. The design utilizes Motorola's RF BiCMOS1 process to yield superior performance in a cost effective monolithic device.

- Designed for Dual–Mode Operation
  - Total Supply Current CDMA Mode = 55 mA Typical
  - Total Supply Current FM Mode = 35 mA Typical
- 30 dB Dynamic Range Gain Control on Exciter
- Upmixer Output IP_3 = 11 dBm Typical
- Exciter Output IP_3 = 28 dBm Typical
- Supply Voltage Range = 2.7 to 3.6 V
- Cascaded Adjacent Channel Power (P_{out} = 6.0 dBm)
  - @ 885 kHz Offset = –60 dBc Typical
  - @ 1.98 MHz Offset = –72 dBc Typical

800 MHz
DUAL–MODE CDMA/AMPS
UPMIXER/EXCITER

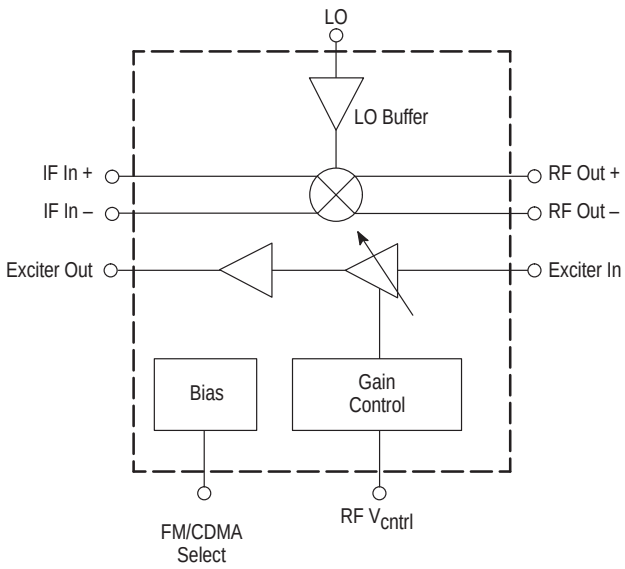
SEMICONDUCTOR
TECHNICAL DATA



(Scale 2:1)

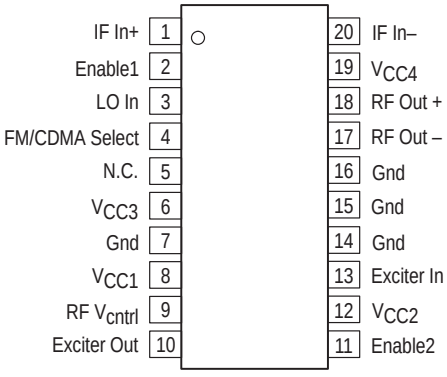
PLASTIC PACKAGE
CASE 948M
(TSSOP–20EP, Tape & Reel Only)

Simplified Block Diagram



This device contains 305 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temp Range	Package
MRFIC0954R2	T_A = –40 to 85°C	TSSOP–20EP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	5.0	V
IF Input	IF In+, IF In–	10	dBm
LO Input	LO	10	dBm
Operating Temperature	T_A	–40 to 85	°C
Storage Temperature	T_{stg}	–65 to 150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions and Electrical Characteristics tables or Pin Descriptions section.
2. Meets Human Body Model (HBM) ≤50 V and Machine Model (MM) ≤40 V. This device is rated Moisture Sensitivity Level (MSL) 4. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	–	3.6	V
RF Frequency Range	f_{RF}	800	–	960	MHz
IF Frequency Range	f_{IF}	70	–	250	MHz
LO Frequency Range	f_{LO}	600	–	1200	MHz
Gain Control Voltage Range	V_{cntrl}	0.1	–	1.7	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V, P_{LO} = –15 dBm @ 967 MHz, P_{IF} = –21 dBm (differential) @ 130 MHz, V_{Enable} = $V_{TxEnable}$ = 2.4 V, T_A = 25°C, Test Circuit in Figure 1, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CASCADE PERFORMANCE (Filter included between RF Out and Exciter input. Filter has an insertion loss of 4.0 dB) For CDMA mode FM/CDMA Select = 2.7 V. For FM mode FM/CDMA Select = 0 V.					
Output Power	P_{out}				dBm
CDMA Mode (V_{cntrl} = 1.7 V)		6.0	10	–	
FM Mode (P_{IF} = –12 dBm (differential))		11	14	–	
Dynamic Range (RF_{Vcntrl} = 0.1 to 1.7 V)	DR	25	38	–	dB
Adjacent Channel Power (CDMA Mode, P_{out} = 6.0 dBm, P_{IF} = –21 dBm (differential))	ACPR				dBc
@ 885 kHz Offset		–	–60	–52	
@ 1.98 MHz Offset		–	–72	–62	
Supply Current	I_{CC}				mA
CDMA Mode, P_{IF} = –21 dBm (differential), P_{out} = 6.0 dBm (set by V_{cntrl})		–	55	70	
FM Mode, P_{IF} = –12 dBm (differential), P_{out} = 11 dBm (set by V_{cntrl})		–	35	50	
MIXER SECTION					
Conversion Gain	GC	–	7.0	–	dB
Noise Figure	NF	–	15	–	dB
Output Third Order Intercept Point	OIP3	–	11	–	dBm
EXCITER SECTION					
Gain (No Attenuation)	GC	–	28	–	dB
Noise Figure	NF	–	5.0	–	dB
AGC Dynamic Range	DR	25	38	–	dB
Output Third Order Intercept Point	OIP3	–	25	–	dBm

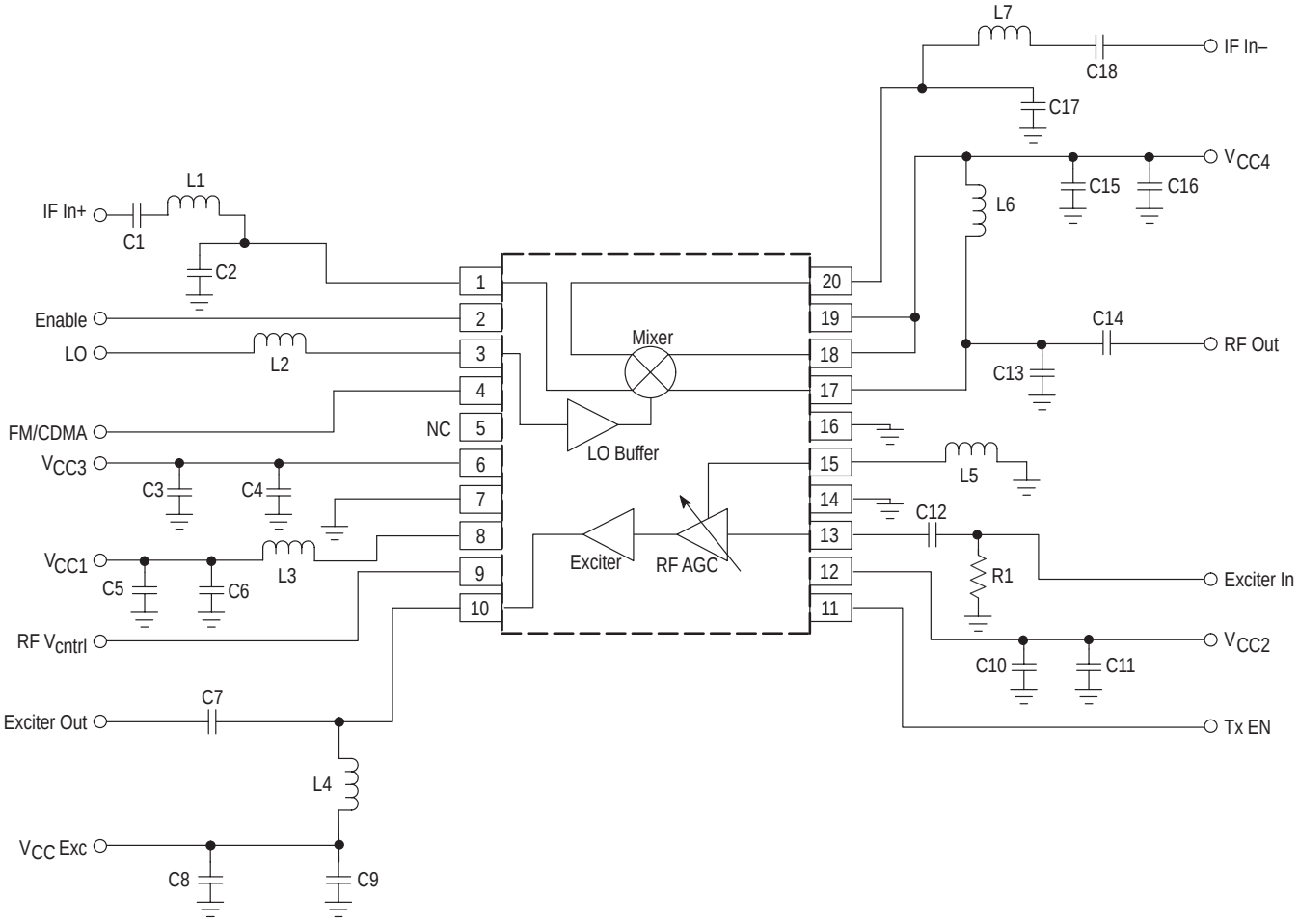
PIN FUNCTION DESCRIPTION

Pin	Function	Description	Voltage On (V)	Voltage Off (V)
1	IF In+	Mixer IF input pin. Input impedance is 500 Ω.	–24 dBm (Typ)	
2	Enable 1 (See Table 3)	Enable pin. A logic ″High″ (>2.4 V) enables entire chip and ″Low″ (<0.4 V) **disables chip.**	2.4 to 3.6	0 to 0.4
3	LO In	Mixer LO input pin.	–15 dBm (Typ)	
4	FM/CDMA Select	FM/CDMA select pin. Logic ″High″ (>2.4 V) selects CDMA mode for increased linearity and output power. ″Low″ (<0.4 V) selects FM mode for reduced current consumption.		
5	N.C.	No Connection		
6	V_{CC3}	Supply Voltage.	2.7 to 3.6	
7	Gnd	Ground connection.	–	
8	V_{CC1}	Supply Voltage	2.7 to 3.6	
9	RF AGC Control Voltage	RF AGC control pin. A 30 dB dynamic range can be acheived by adjusting voltage from 0.1 V (low gain) to 1.7 V (high gain).	0.1 to 1.7	
10	Exciter Out	RF exciter amplifier output pin.	–	
11	Enable 2 (See Table 3)	Tx Enable pin. A logic ″High″ (>2.4 V) enables Tx path and ″Low″ (<0.4 V) **disables Tx path except LO Buffer**.	2.4 to 3.6	0 to 0.4
12	V_{CC2}	Supply Voltage	2.7 to 3.6	
13	Exciter In	RF exciter amplifier input pin.	–	
14	Gnd	Ground connection.	–	
15	Gnd	Ground connection.	–	
16	Gnd	Ground connection.	–	
17	RF Out–	Mixer RF output pin.		
18	RF Out+	Mixer RF output pin.		
19	V_{CC4}	Supply Voltage	2.7 to 3.6	
20	IF In–	Mixer IF input pin. Input impedance is 500 Ω.	–24 dBm (Typ)	

Table 1. Enable Truth Table

Enable 1	Enable 2	Mode
0	0	Disabled
0	1	Not Applicable
1	0	Standby Mode: Disables mixer/exciter, except LO buffer
1	1	Tx Enabled

Figure 1. Applications Circuit



C1, C18	1.0 nF	L1, L7	220 nH
C2, C17	4.7 pF	L2	15 nH
C3 , C5, C8, C11, C16	10 nF	L3 , L4, L6	6.8 nH
C4, C6, C9, C10, C12, C15	100 pF	L5	1.0 nH
C7	4.3 pF		
C13	1.6 pF	R1	100 Ω
C14	1.3 pF		

NOTES: 1. IF ports matched to 50 Ω for testing purposes.
2. L3 and C6 form part of RFAGC/Exciter interstage match.
3. L5 can be varied to change gain.

Figure 2. Gain versus Frequency (FM Mode)

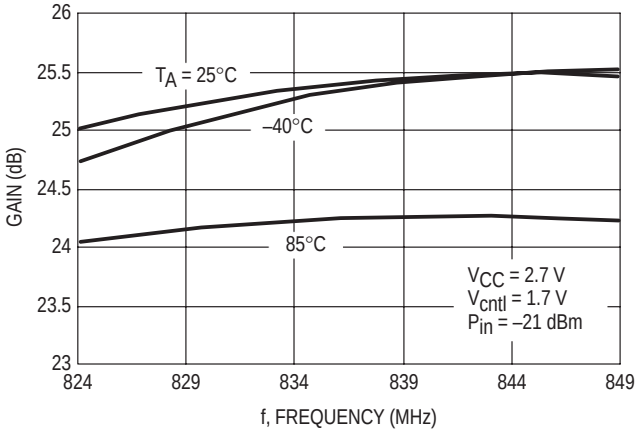


Figure 3. Gain versus Frequency (CDMA Mode)

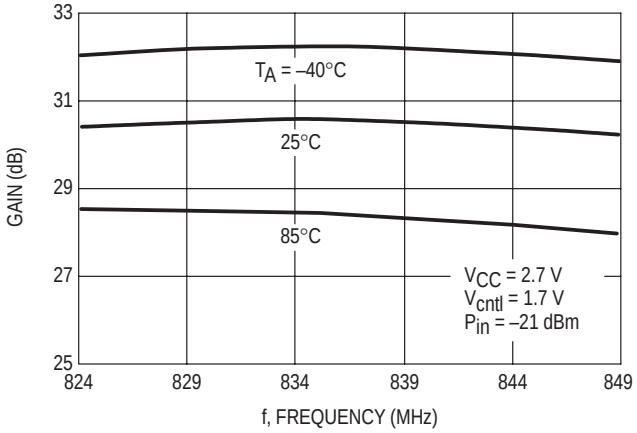


Figure 4. Gain versus LO Power (FM Mode)

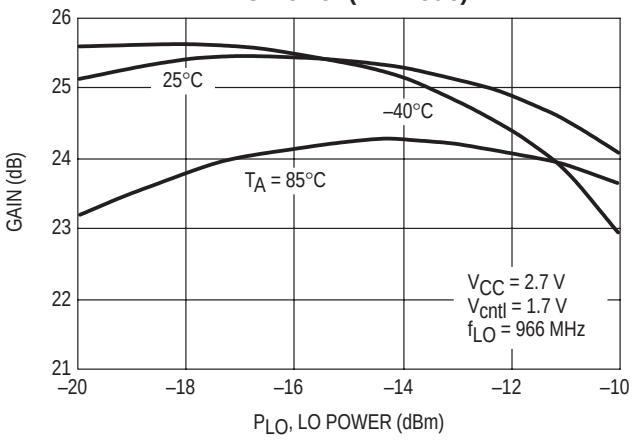


Figure 5. Gain versus LO Power (CDMA Mode)

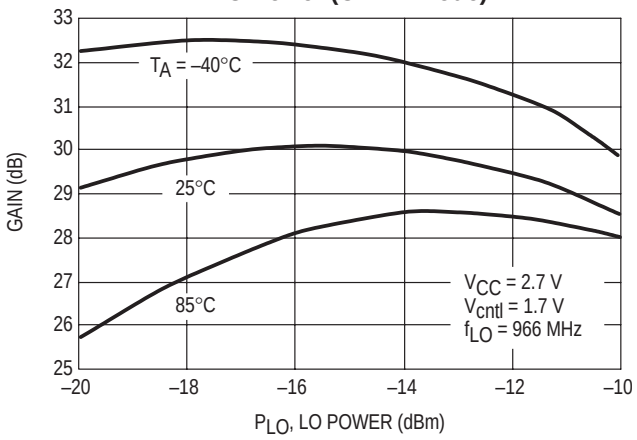


Figure 6. LO Feedthrough versus Control Voltage (FM Mode)

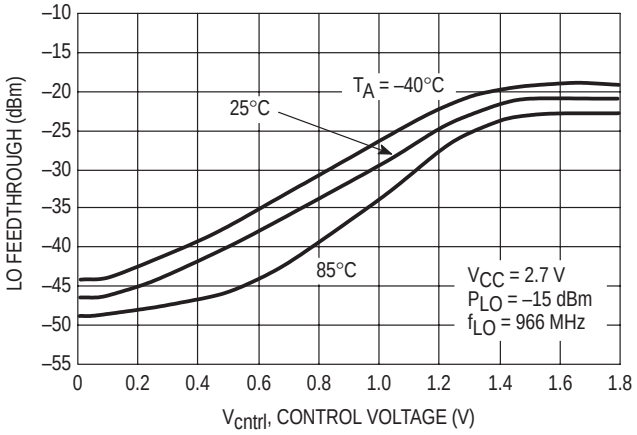


Figure 7. LO Feedthrough versus Control Voltage (CDMA Mode)

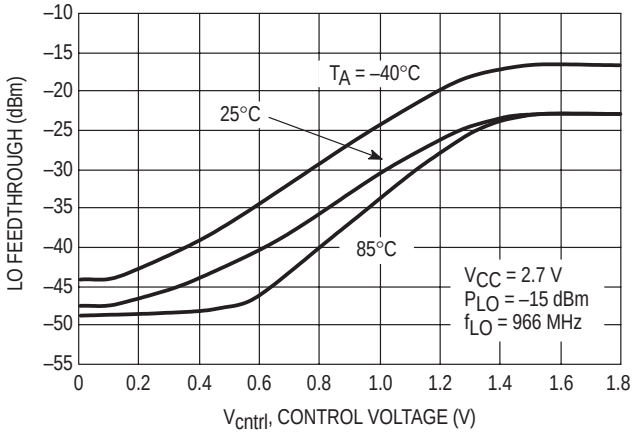


Figure 8. Output Power versus Control Voltage (FM Mode)

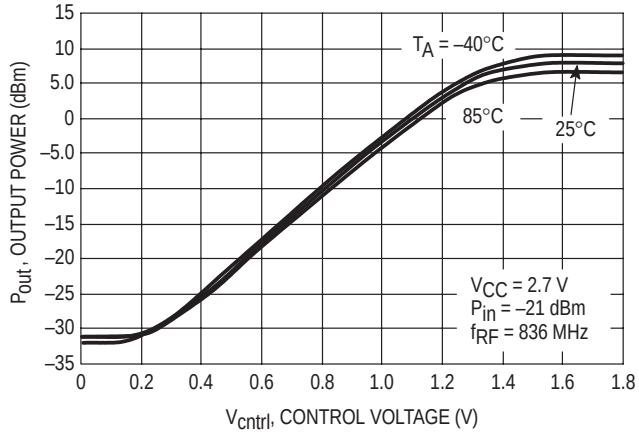


Figure 9. Output Power versus Control Voltage (CDMA Mode)

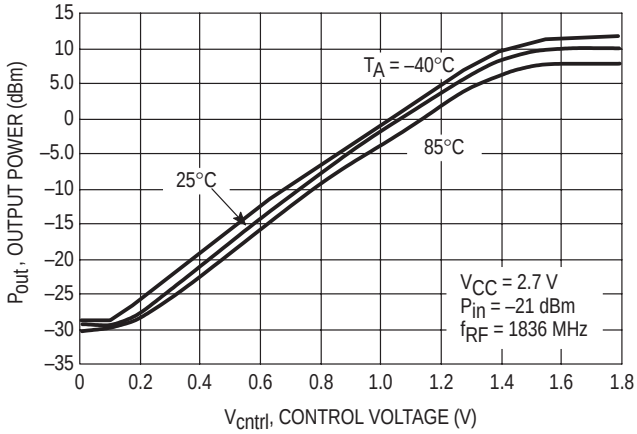


Figure 10. Adjacent Channel Power versus Control Voltage (CDMA Mode)

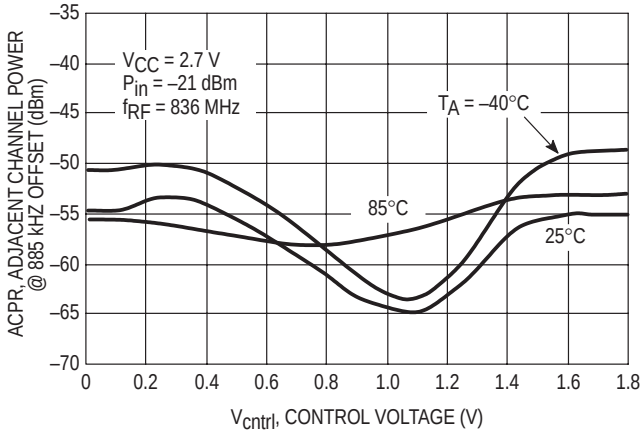
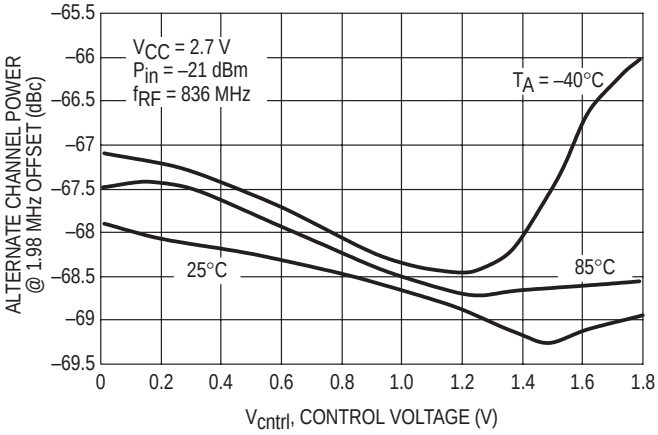


Figure 11. Alternate Channel Power versus Control Voltage (CDMA Mode)



APPLICATIONS INFORMATION

Design Philosophy

The MRFIC0954 has three operating states, enable, standby, and disable. These states are controlled by the truth table shown in Table 3. The device is fully operational during the enable state and the bias level can be selected. A high bias current for CDMA or a lower bias current for Analog (or CDMA at lower powers) can be selected via the FM/CDMA pin. In the high current CDMA mode, the quiescent current is increased to maximize the linearity of the device. In the lower current bias, the quiescent current is optimized for efficiency in the Analog mode. This lower bias point is also useful in lower power CDMA operation. The standby mode can be used to reduce current consumption during Voice Activity Factoring. In the standby mode, the LO buffer remains on to prevent VCO pulling and the bandgap reference bias circuit remains on to assure rapid device turn on. Current consumption in standby mode is 10 mA typical. The disable mode is used to turn the MRFIC0954 completely off. Leakage current in this mode is only a few microamps.

The mixer is a double–balanced “Gilbert–cell” design with a balanced LO buffer amplifier. The input and output of the mixer are differential. However, the linearity is high enough to tie one output to V_{CC} and use the other as a single–ended output. Used this way it provides around 7.0 dB of gain and typically draws 20 mA quiescent current in CDMA mode and 16 mA in Analog Mode. An external filter is required between the mixer and RF AGC amplifier to reduce RX band noise.

Figure 1 shows the applications circuit for the MRFIC0954. In this circuit, the IF ports of the mixer have been matched to 50 Ω for testing purposes. In the actual application, the differential IF ports of the mixer would be impedance matched to an IF SAW filter. The differential impedance of the mixer IF ports is 1600 Ω. The RF output of the mixer is configured as a single ended output. DC current to the open collector output of the mixer is provided by inductor, L6 (6.8 nH). Inductor L6 is also part of the matching circuit with C13 (1.6 pF), C14 (1.3 pF) and C15 (100 p).

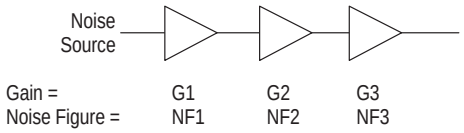
The RF AGC amplifier is a single–ended cascode design employing the standard “current steering” method of gain control. It’s ground is brought out through pin number 15 so inductance can be added to degenerate the gain for a lower noise floor. With 2.0 to 3.0 nH of external inductance, the maximum gain is around 13 dB. It typically draws 9.0 mA quiescent current in CDMA mode and 3.0 mA in Analog mode. The RF V_{cntrl} signal is buffered with an on–chip OpAmp then preconditioned with temperature compensation and dB/V linearization before being applied to the RF AGC amplifier.

Inductor L3 (6.8 nH) and capacitor C6 (100 pF) are for the interstage match between the RF AGC and the exciter amplifier.

The exciter amplifier is a simple common emitter design. It is grounded directly to the exposed pad which results in 12 dB of gain. It typically draws 24 mA bias current in CDMA mode and 8.0 mA in Analog mode. Inductor L4 (6.8 nH), capacitor C7 (4.3 pF), and C9 (100 pF) provide the output matching. L4 also provides a DC current path for the open collector output.

Noise Power Considerations

In CDMA systems, the handset is required to dynamically adjust its output power to specific levels. This requires a dynamic range of as much as 90 dB from the transmitter. Another key performance specification in CDMA systems is the output noise power, both in band and out of band. Noise power specifications has caused the noise figure of the transmitter to become an important system consideration. The cascaded noise figure of the transmitter can be analyzed with the same equation used in receiver analysis. The only difference is the noise source is from the transmitter (modulator) instead of the atmosphere.



$$NF_{cascaded} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2}$$

This equation above shows that the cascaded noise figure is better if the gain is higher and the noise figure is lower for the stages close to the noise source. For this reason, it is advantageous to implement some of the gain control of a CDMA transmitter in the RF section. The MRFIC0954 integrates a RF AGC amplifier after the upmixer to improve the overall noise figure of the transmitter.

If better noise figure from the mixer is required, the mixer RF output can be operated differentially with the addition of a balun. Operating the mixer differentially will provide some noise cancellation and reduce the noise figure by 5.0 dB. Shown below is a lumped element balun that is effective in the cellular transmit band of 824 to 849 MHz.

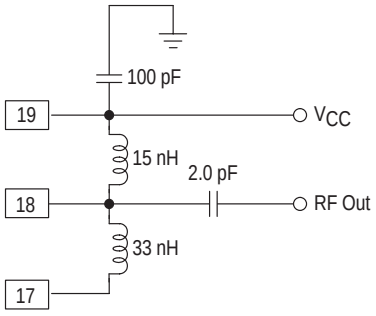


Table 2. Scattering Parameters for Exciter Amplifier
(V_{DD} = 2.7 V, T_A = 25°C, RF V_{cntrl} = 1.8 V, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$	$\lvert S_{21} \rvert$	$\angle\phi$	$\lvert S_{12} \rvert$	$\angle\phi$	$\lvert S_{22} \rvert$	$\angle\phi$
800	0.523	–31.46	18.463	–102.56	0.001	153.19	0.341	–26.37
810	0.522	–31.83	18.964	–107.12	0.001	152.15	0.360	–33.06
820	0.519	–31.84	19.412	–111.84	0.001	152.18	0.379	–39.48
830	0.515	–31.96	20.017	–121.57	0.001	143.30	0.413	–52.61
840	0.513	–31.90	20.214	–126.53	0.002	139.87	0.428	–58.96
850	0.512	–31.78	20.330	–131.59	0.001	140.14	0.445	–65.36
860	0.513	–31.62	20.228	–141.98	0.001	143.83	0.468	–77.72
870	0.510	–31.64	19.962	–147.12	0.002	140.02	0.476	–83.97
880	0.510	–31.45	19.593	–152.09	0.002	147.69	0.478	–89.94
890	0.514	–31.41	18.768	–161.40	0.002	139.58	0.486	–100.64
900	0.515	–31.50	18.161	–166.11	0.002	141.12	0.491	–105.67
910	0.514	–31.58	17.585	–170.50	0.002	124.24	0.489	–110.70
920	0.515	–31.83	16.353	–178.79	0.002	125.97	0.485	–119.67
930	0.517	–31.96	15.718	177.30	0.002	128.36	0.489	–124.16
940	0.518	–32.29	15.070	173.39	0.002	125.66	0.484	–128.24
950	0.517	–32.88	13.708	166.70	0.002	112.00	0.473	–135.30
960	0.518	–32.81	13.090	163.84	0.002	117.04	0.468	–138.41

Table 3. Scattering Parameters for Upmixer
(V_{DD} = 2.7 V, T_A = 25°C, 50 Ω System)

f	IF In+		IF In–		f	RF Out (Pin 17)	
(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$	$\lvert S_{11} \rvert$	$\angle\phi$	(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$
70	0.886	–5.66	0.885	–5.12	800	0.488	–60.15
80	0.883	–5.79	0.882	–5.29	810	0.487	–60.56
90	0.884	–6.15	0.881	–5.73	820	0.487	–61.04
100	0.879	–6.26	0.878	–5.74	830	0.488	–61.82
110	0.881	–6.74	0.881	–6.19	840	0.490	–62.20
120	0.877	–7.20	0.878	–6.43	850	0.487	–62.85
130	0.880	–7.23	0.879	–6.64	860	0.491	–63.72
140	0.876	–7.89	0.876	–7.20	870	0.492	–64.03
150	0.876	–8.11	0.875	–7.28	880	0.493	–64.38
160	0.878	–8.51	0.877	–7.57	890	0.497	–65.56
170	0.879	–8.84	0.879	–8.07	900	0.501	–65.98
180	0.877	–9.28	0.880	–8.26	910	0.503	–66.50
190	0.876	–9.81	0.878	–8.81	920	0.504	–68.66
200	0.876	–10.15	0.877	–9.21	930	0.504	–69.70
210	0.875	–10.52	0.876	–9.44	940	0.502	–69.91
220	0.877	–10.83	0.880	–9.78	950	0.503	–71.15
230	0.877	–11.58	0.877	–10.41	960	0.502	–70.74
240	0.878	–11.59	0.877	–10.41			
250	0.881	–12.29	0.879	–10.85			

f	LO In		f	LO In		f	LO In	
(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$	(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$	(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$
600	0.820	–18.93	810	0.802	–24.40	1020	0.785	–30.28
610	0.819	–19.00	820	0.800	–24.55	1030	0.784	–30.09
620	0.817	–19.35	830	0.802	–24.75	1040	0.786	–30.63
630	0.815	–19.60	840	0.804	–25.22	1050	0.786	–30.91
640	0.820	–19.87	850	0.804	–25.13	1060	0.784	–31.10
650	0.814	–20.06	860	0.802	–25.86	1070	0.780	–31.60
660	0.813	–20.49	870	0.799	–26.14	1080	0.783	–31.85
670	0.816	–20.61	880	0.801	–26.36	1090	0.782	–31.99
680	0.815	–20.82	890	0.797	–26.72	1100	0.775	–32.54

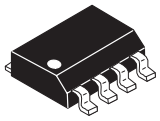
The MRFIC Line
GPS GaAs Low Noise Amplifier

MRFIC1501

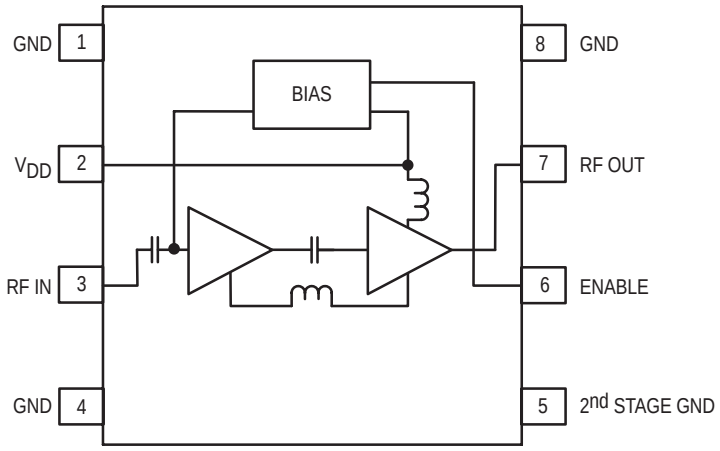
1.6 GHz GaAs LOW NOISE AMPLIFIER

The MRFIC1501 is a low cost yet high performance two–stage, low–noise amplifier designed primarily for use in Global Positioning Satellite System (GPS) and other L–band satellite receivers. The broadband nature of the design makes the device applicable to a variety of L–band applications where high performance at reasonable current and cost are required. Supply current is minimized through a current sharing DC cascode circuit configuration. Supply voltage can be applied to either the V_{DD} pin or the RF output pin for remote antenna applications. The integrated circuit requires minimal off-chip matching while allowing for maximum flexibility in optimizing gain and noise figure. An ENABLE pin is provided to allow for a reduced supply current standby mode. The design employs Motorola's low cost planar self–aligned MESFET process to assure repeatable characteristics at minimal cost.

- Usable Frequency Range = 1 to 2 GHz
- 18 dB Typ Gain at V_{DD} = 5 Volts
- 1.1 dB Typ Noise Figure at V_{DD} = 5 Volts
- Simple Off-chip Matching for Maximum Gain/Noise Figure Flexibility
- Single Bias Supply = 3 to 5 Volts
- Low Power Consumption = 30 mW (Typ) at 5 Volts
- Low Cost Surface Mount Plastic Package
- Order MRFIC1501R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M1501



CASE 751–06
(SO-8)



Pin Connections and Functional Block Diagram

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

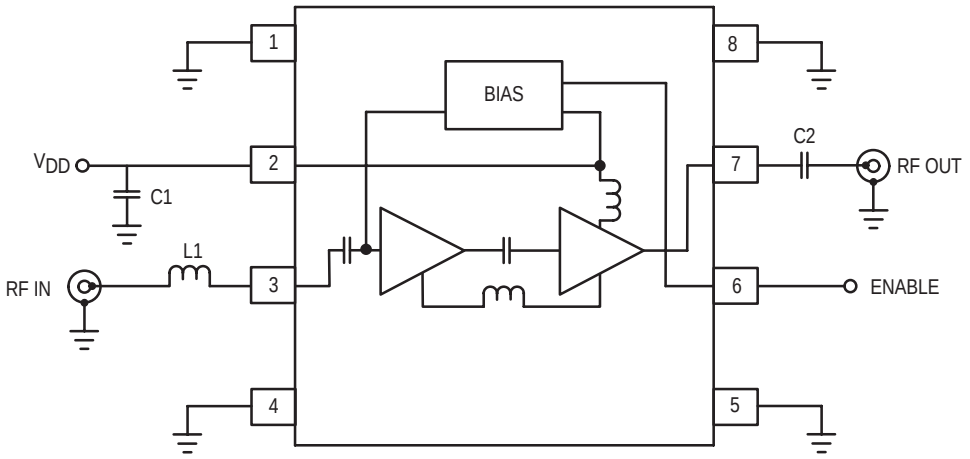
Ratings	Symbol	Limit	Unit
Supply Voltage	V_{DD}	6	Vdc
RF Input Power	P_{RF}	3	dBm
ENABLE Voltage	ENABLE	6	Vdc
V_{DD} Current Sourcing (With Supply Connected to Pin 7)	I_{PIN2}	20	mA
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to + 100	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Frequency	f_{RF}	1 to 2	GHz
ENABLE “ON” (Device Operational) Voltage	ENABLE	$V_{DD} \pm 0.5$	Vdc
ENABLE “OFF” (Device in Standby Mode) Voltage	ENABLE	0 to 0.5	Vdc
Supply Voltage	V_{DD}	3 to 5	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, RF = 1.575 GHz, ENABLE = 5 V, Circuit Configuration Shown in Figure 1)

Characteristic	Min	Typ	Max	Unit
RF Gain	17	18	—	dB
SSB Noise Figure	—	1.1	—	dB
RF Output 3rd Order Intercept Point	—	10	—	dBm
Output 1 dB Gain Compression	—	0	—	dBm
Reverse Isolation (s_{12})	—	30	—	dB
Input Return Loss	—	10	—	dB
Output Return Loss	—	10	—	dB
Supply Current	—	5.9	7.5	mA



C1, C2 – 22 pF
L1 – 11 nH (Implemented in Microstrip)

Figure 1. Applications Circuit Configuration

TYPICAL CHARACTERISTICS

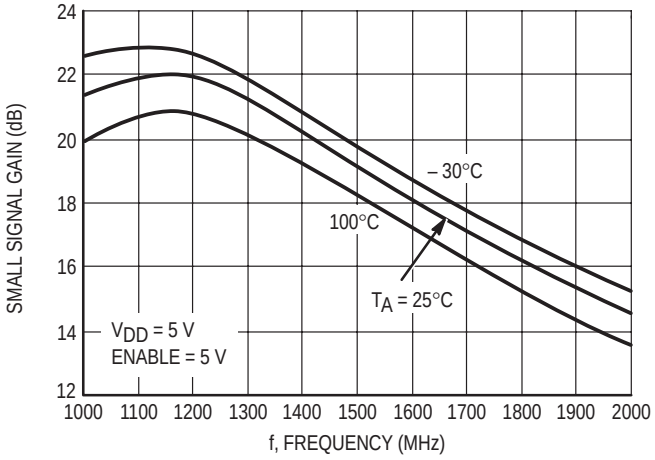


Figure 2. Small Signal Gain versus Frequency

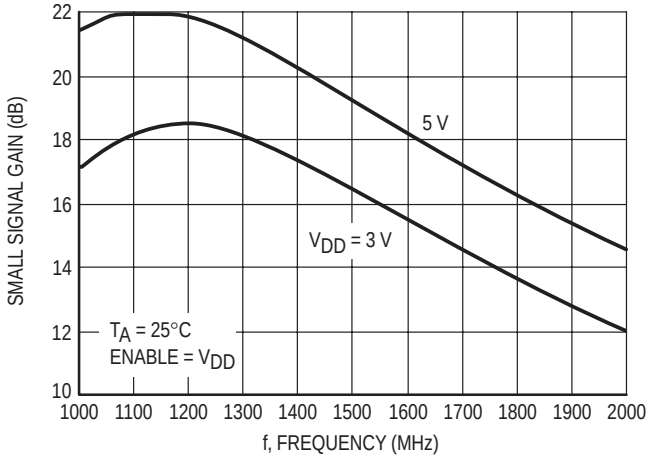


Figure 3. Small Signal Gain versus Frequency

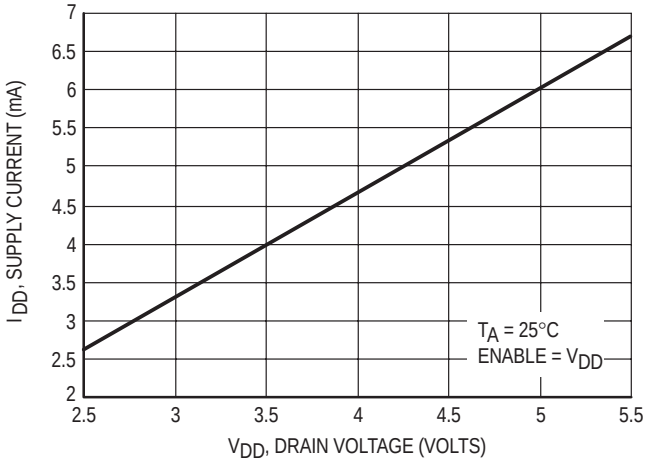


Figure 4. Drain Current versus Drain Voltage

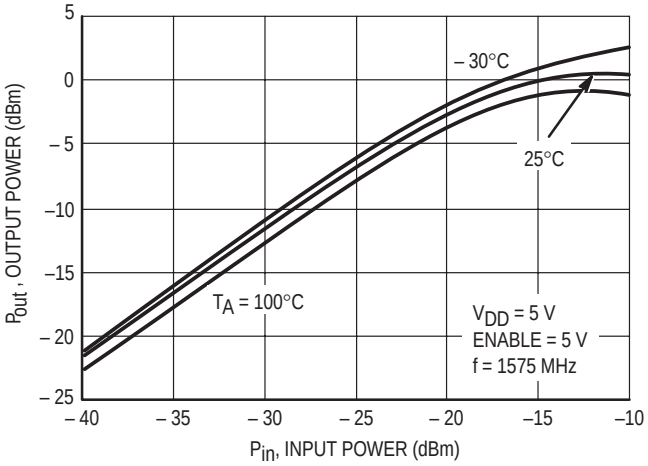


Figure 5. Output Power versus Input Power

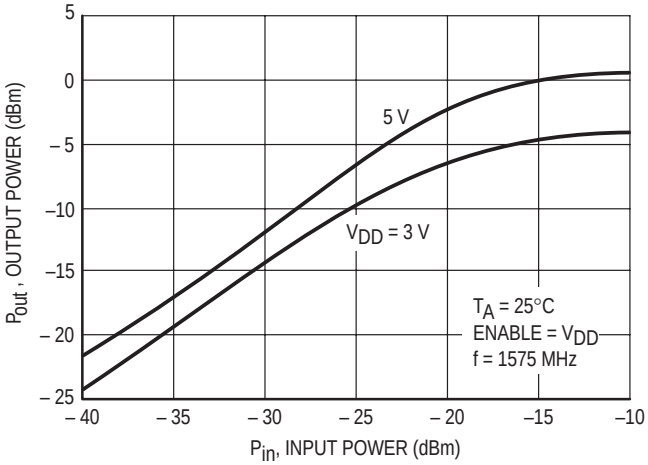


Figure 6. Output Power versus Input Power

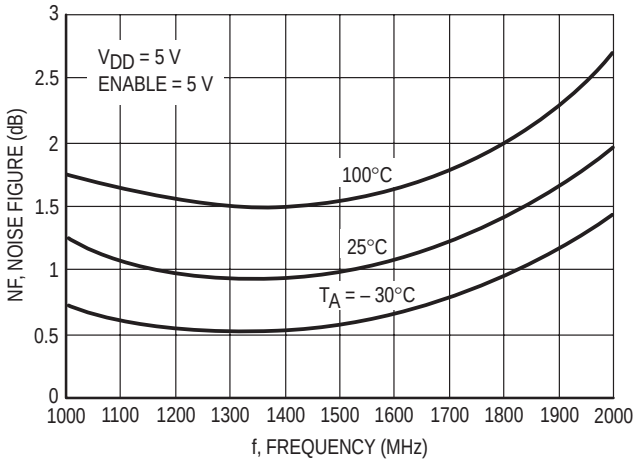


Figure 7. Noise Figure versus Frequency

TYPICAL CHARACTERISTICS

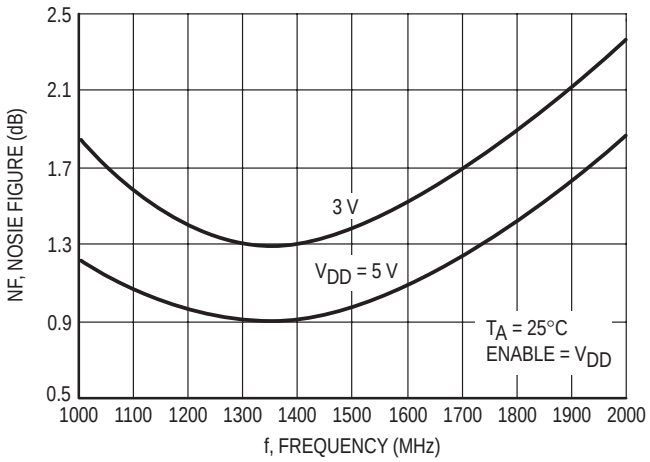


Figure 8. Noise Figure versus Frequency

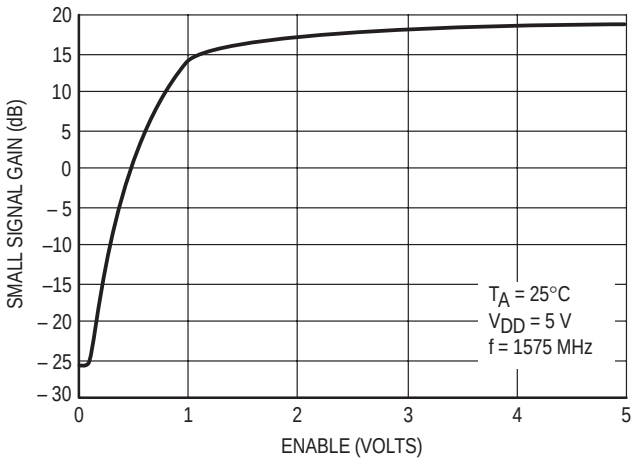


Figure 9. Gain versus ENABLE Voltage

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

The circuit configuration employs a DC cascode arrangement which allows current sharing between two FETs. This gives excellent noise figure at reduced supply current. Since GPS applications often require the downconverter to be remotely mounted at the antenna, the output is DC coupled so that the drain voltage can be supplied through the coax feed. The V_{DD} pin can actually supply other components in the equipment at less than 20 mA of current. On–chip bias circuitry tracks changes in device threshold voltage and temperature and is externally controlled through the ENABLE pin. This feature allows for a low current standby mode or for gain reduction. Refer to Figure 9 for control characteristics.

CIRCUIT CONSIDERATIONS

As shown in Figure 1, impedance matching of the MRFIC1501 is quite simple. Through use of an on–chip source inductor in the first stage, Γ_{opt} and and Γ_{in}^{*} are approximately equal. A single inductor at the input will give good input match and noise figure. This inductor can be implemented with a high impedance microstrip line or a chip inductor.

As with all RF active circuit designs, bypassing the supply pin is recommended. Layout and ground via location is important. Vias should be located as close as possible to ground pins and the ground side of off–chip components.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” to the device type. For a complete list of currently available boards and ones in development for newly introduced products, please consult your local Motorola Distributor or Sales Office.

Table 1. Scattering Parameters (V_{DD} = 3 Volts, ENABLE = 3 Volts, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
795	0.958	–28.07	3.218	28.76	0.011	179.98	0.358	21.08
825	0.959	–29.71	3.448	23.95	0.011	176.45	0.336	15.36
855	0.954	–31.16	3.534	18.42	0.012	172.43	0.311	9.65
870	0.951	–32.04	3.535	16.03	0.011	171.06	0.297	6.67
900	0.945	–33.63	3.502	11.26	0.012	166.26	0.273	1.19
930	0.935	–35.48	3.528	6.47	0.013	166.48	0.250	–5.16
960	0.932	–37.28	3.689	2.07	0.014	164.19	0.227	–11.04
990	0.921	–39.03	3.867	–2.41	0.016	163.33	0.203	–18.26
1020	0.912	–40.69	3.954	–7.56	0.018	160.39	0.181	–25.17
1050	0.901	–42.28	3.975	–12.01	0.019	158.58	0.158	–33.18
1080	0.892	–44.16	4.039	–16.73	0.020	154.26	0.138	–40.98
1110	0.879	–46.05	4.154	–21.72	0.021	151.91	0.119	–49.98
1140	0.865	–47.91	4.296	–27.64	0.022	147.91	0.101	–58.85
1170	0.846	–49.35	4.320	–32.73	0.022	147.32	0.086	–71.10
1200	0.825	–51.34	4.224	–36.64	0.022	147.46	0.077	–87.14
1230	0.800	–51.92	4.125	–40.14	0.026	152.91	0.070	–118.39
1260	0.798	–52.57	4.224	–42.75	0.029	141.81	0.053	–155.35
1290	0.782	–53.50	4.371	–47.81	0.030	135.50	0.051	169.35
1320	0.775	–55.70	4.554	–53.11	0.031	132.76	0.049	140.94
1350	0.758	–57.05	4.525	–57.58	0.030	128.85	0.052	126.02
1380	0.742	–58.70	4.501	–61.64	0.031	125.89	0.061	114.60
1410	0.721	–60.03	4.511	–66.70	0.030	123.70	0.073	105.25
1440	0.703	–60.76	4.538	–71.38	0.031	121.40	0.083	97.32
1470	0.686	–61.48	4.553	–75.65	0.030	119.75	0.095	89.55
1500	0.668	–62.72	4.497	–79.44	0.031	116.74	0.107	82.70
1530	0.652	–63.71	4.436	–83.00	0.031	115.52	0.119	77.82
1560	0.633	–63.91	4.437	–87.36	0.030	115.29	0.132	72.37
1575	0.629	–64.01	4.458	–89.76	0.030	114.23	0.139	69.33
1590	0.621	–63.94	4.474	–91.54	0.030	112.50	0.147	66.71
1620	0.604	–64.46	4.477	–95.21	0.031	112.56	0.159	62.76
1650	0.586	–63.98	4.425	–98.51	0.030	111.63	0.172	58.00
1680	0.576	–64.45	4.330	–102.11	0.031	108.93	0.185	54.00
1710	0.559	–64.36	4.264	–105.61	0.030	106.34	0.198	50.85
1740	0.549	–64.02	4.227	–108.90	0.030	106.33	0.208	47.46
1770	0.538	–63.89	4.219	–112.08	0.030	106.56	0.222	43.54
1800	0.527	–63.69	4.172	–114.95	0.029	104.83	0.233	40.56
1830	0.523	–63.58	4.046	–118.53	0.030	104.72	0.244	37.76
1860	0.511	–62.83	3.965	–121.26	0.028	102.55	0.256	34.88
1890	0.503	–62.92	3.925	–124.29	0.029	103.12	0.266	32.47
1920	0.495	–62.26	3.917	–126.71	0.029	102.20	0.275	29.95
1950	0.485	–60.97	3.843	–129.24	0.029	102.70	0.283	27.89
1980	0.479	–60.47	3.759	–132.13	0.029	101.50	0.290	25.95
2010	0.474	–59.93	3.631	–135.13	0.027	98.87	0.300	24.27

Table 2. Scattering Parameters (V_{DD} = 4 Volts, ENABLE = 4 Volts, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
900	0.927	–34.45	4.901	4.43	0.011	167.24	0.210	–4.75
930	0.915	–36.30	4.962	–0.21	0.012	166.66	0.185	–12.35
960	0.908	–38.22	5.164	–4.86	0.013	165.06	0.160	–20.80
990	0.895	–39.78	5.383	–9.68	0.015	161.65	0.135	–30.56
1020	0.883	–41.42	5.485	–14.72	0.016	158.86	0.112	–42.22
1050	0.869	–43.05	5.514	–19.31	0.017	158.43	0.092	–55.71
1080	0.858	–44.69	5.573	–24.34	0.018	155.12	0.078	–73.31
1110	0.840	–46.48	5.695	–29.10	0.019	151.63	0.068	–94.03
1140	0.822	–48.23	5.813	–35.10	0.020	149.83	0.063	–115.86
1170	0.804	–49.58	5.817	–40.03	0.020	149.25	0.066	–136.79
1200	0.783	–51.19	5.741	–43.83	0.020	149.99	0.077	–153.70
1230	0.750	–51.37	5.625	–47.36	0.023	155.59	0.102	–172.32
1260	0.753	–51.39	5.762	–49.92	0.026	144.73	0.114	165.51
1290	0.747	–52.29	5.894	–55.24	0.028	137.19	0.122	150.89
1320	0.741	–54.09	6.078	–60.53	0.028	134.63	0.123	139.00
1350	0.727	–55.80	5.998	–65.01	0.028	131.72	0.129	131.12
1380	0.709	–57.17	5.957	–68.70	0.028	128.11	0.137	124.50
1410	0.692	–58.13	5.921	–73.18	0.027	126.13	0.144	117.65
1440	0.676	–59.05	5.928	–77.75	0.027	126.40	0.153	111.32
1470	0.661	–59.68	5.909	–81.80	0.028	122.94	0.162	105.05
1500	0.641	–60.62	5.821	–85.30	0.027	122.00	0.169	98.79
1530	0.628	–61.62	5.715	–88.81	0.028	119.28	0.179	93.52
1560	0.613	–61.52	5.686	–93.11	0.028	119.11	0.190	87.97
1575	0.606	–61.90	5.667	–95.29	0.028	119.48	0.196	85.31
1590	0.599	–61.76	5.667	–97.03	0.029	117.97	0.201	82.57
1620	0.587	–62.04	5.635	–100.45	0.028	117.17	0.209	78.01
1650	0.570	–61.74	5.550	–103.32	0.027	117.04	0.222	73.51
1680	0.560	–62.07	5.423	–106.67	0.028	114.76	0.233	69.07
1710	0.543	–62.20	5.318	–110.16	0.028	112.28	0.243	65.48
1740	0.534	–61.92	5.250	–113.26	0.028	113.29	0.253	61.42
1770	0.527	–61.70	5.212	–116.15	0.028	112.91	0.264	58.10
1800	0.516	–61.84	5.146	–118.66	0.029	113.11	0.274	54.22
1830	0.511	–61.24	4.991	–121.89	0.027	112.07	0.285	50.97
1860	0.501	–60.19	4.848	–124.80	0.027	111.64	0.295	47.95
1890	0.491	–60.35	4.783	–127.80	0.027	110.45	0.304	45.16
1920	0.484	–59.86	4.747	–130.12	0.028	109.45	0.315	42.60
1950	0.474	–58.58	4.697	–132.44	0.028	109.35	0.323	40.11
1980	0.471	–58.40	4.605	–134.97	0.028	111.10	0.329	38.15
2010	0.462	–57.51	4.407	–138.30	0.026	108.25	0.339	35.69

Table 3. Scattering Parameters (V_{DD} = 5 Volts, ENABLE = 5 Volts, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
900	0.909	–35.17	6.271	–1.16	0.011	168.82	0.163	–11.03
930	0.892	–37.01	6.337	–6.08	0.011	165.10	0.137	–21.39
960	0.882	–38.73	6.583	–10.74	0.012	163.68	0.109	–33.61
990	0.869	–40.38	6.808	–15.88	0.014	161.24	0.088	–49.68
1020	0.855	–41.71	6.927	–21.01	0.015	160.19	0.072	–71.47
1050	0.840	–43.22	6.925	–25.76	0.016	157.93	0.065	–98.66
1080	0.828	–44.84	6.996	–30.74	0.017	156.01	0.067	–124.50
1110	0.807	–46.50	7.081	–35.59	0.018	152.69	0.076	–144.89
1140	0.791	–47.98	7.172	–41.40	0.019	151.04	0.088	–161.86
1170	0.769	–49.03	7.150	–45.93	0.019	150.32	0.103	–174.42
1200	0.745	–50.40	7.082	–49.82	0.018	149.54	0.120	178.54
1230	0.716	–49.79	6.940	–53.44	0.021	156.21	0.149	168.88
1260	0.726	–49.58	7.070	–56.18	0.024	146.99	0.165	154.85
1290	0.724	–50.16	7.183	–61.43	0.025	140.13	0.175	144.80
1320	0.721	–52.48	7.285	–66.39	0.027	136.54	0.177	136.23
1350	0.707	–54.20	7.176	–70.78	0.025	133.27	0.183	130.59
1380	0.690	–55.55	7.102	–74.39	0.026	131.27	0.191	124.77
1410	0.675	–56.53	7.006	–78.73	0.026	129.73	0.198	119.51
1440	0.660	–57.13	6.962	–82.74	0.026	127.44	0.204	113.76
1470	0.646	–57.73	6.936	–86.50	0.026	126.66	0.212	108.23
1500	0.629	–58.40	6.822	–89.92	0.026	124.54	0.219	102.92
1530	0.618	–59.69	6.687	–93.31	0.026	122.48	0.227	98.15
1560	0.601	–59.69	6.606	–97.38	0.026	121.63	0.235	93.28
1575	0.594	–59.80	6.573	–99.55	0.027	122.68	0.243	90.64
1590	0.592	–59.78	6.548	–101.29	0.027	122.13	0.246	88.16
1620	0.577	–60.13	6.477	–104.22	0.027	120.48	0.254	84.10
1650	0.562	–59.69	6.366	–106.82	0.027	119.01	0.263	79.24
1680	0.552	–60.13	6.218	–110.11	0.027	118.15	0.272	75.16
1710	0.543	–60.34	6.094	–113.45	0.026	117.67	0.282	71.64
1740	0.529	–59.65	6.000	–116.40	0.027	118.05	0.291	67.99
1770	0.523	–59.54	5.945	–119.10	0.026	116.25	0.301	64.28
1800	0.515	–59.87	5.845	–121.60	0.027	117.55	0.311	60.73
1830	0.507	–59.61	5.676	–124.69	0.027	116.91	0.320	57.22
1860	0.497	–58.77	5.488	–127.65	0.027	115.88	0.330	54.18
1890	0.491	–58.79	5.414	–130.43	0.027	114.66	0.339	51.39
1920	0.478	–58.39	5.376	–132.53	0.028	117.05	0.348	48.34
1950	0.472	–57.29	5.324	–134.66	0.029	114.84	0.356	45.85
1980	0.466	–56.94	5.193	–137.20	0.028	114.82	0.363	43.87
2010	0.461	–56.18	4.972	–140.40	0.027	114.81	0.372	41.56

Table 4. Noise Parameters (V_{DD} = 5 Volts, ENABLE = 5 Volts, 50 Ω System)

f (MHz)	NF_{min} (dB)	Γ_0		R_N
		MAG	∠ ϕ	
1.000	0.8	0.859	26.36	0.98
1.575	1.0	0.793	43.87	0.70
2.000	1.3	0.713	55.80	0.56

MOTOROLA

MRFIC1808

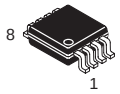
1.9 GHz GaAs Low Noise Amplifier

Designed primarily for use in wireless Personal Communication Systems (PCS) applications such as Digital European Cordless Telephone (DECT), Japan's Personal Handy System (PHS) and the emerging North American systems as a preamp for discrete or integrated downmixers. The MRFIC1808DM is a two–stage low noise amplifier in a low–cost Micro–8 package. The amplifier can be matched to optimize gain or noise figure with simple off–chip input matching. The design employs a novel stacked MESFET design which reuses bias current for the highest gain at minimal current. A CMOS compatible Rx Enable pin allows for very low standby current while the system is in transmit mode.

- Usable Frequency Range = 1.7 to 2.1 GHz
- 18 dB Typ Gain
- 1.6 dB Typ Noise Figure
- Simple Off–chip Matching for Maximum Gain/Noise Figure Flexibility
- High Reverse Isolation = 32 dB (Typ)
- Single Bias Supply = 2.7 to 4.5 V
- Low Standby Current = 8 μA (Typ)
- Low Cost Surface Mount Plastic Package
- Device Marking = M1808

1.9 GHz GaAs
LOW NOISE AMPLIFIER

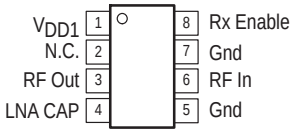
SEMICONDUCTOR
TECHNICAL DATA



(Scale 2:1)

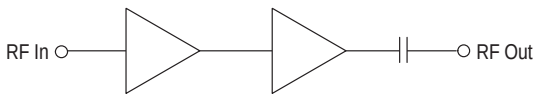
DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8, Tape & Reel Only)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



This device contains 5 active transistors.

ORDERING INFORMATION

Device	Operating Temp Range	Package
MRFIC1808DMR2	T_A = –30 to 85°C	Micro–8

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	5.5	Vdc
RF Input Power	P_{RF}	3.0	dBm
Enable Voltage	Rx Enable	5.5	Vdc
Storage Temperature Range	T_{stg}	–65 to 150	°C
Operating Ambient Temperature	T_A	–30 to 85	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions or Electrical Characteristics tables.
2. Meets Human Body Model (HBM) ≤500 V and Machine Model (MM) ≤200 V.
3. ESD data available upon request.

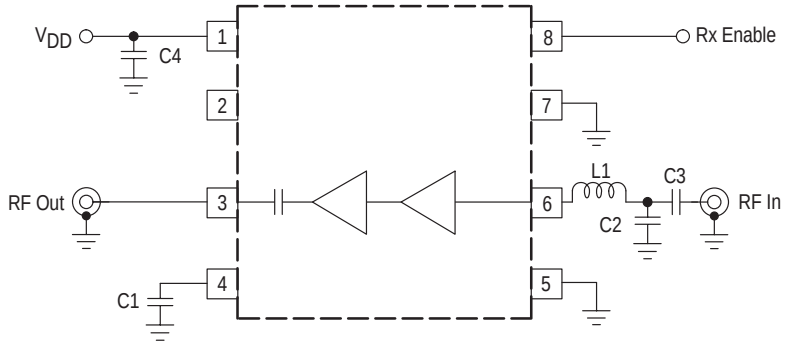
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
RF Frequency	f_{RF}	1.7	–	2.1	GHz
Supply Voltage	V_{DD}	2.7	–	4.5	Vdc
Rx Enable Voltage, ON	Rx Enable	2.7	–	V_{DD}	Vdc
Rx Enable Voltage, OFF	Rx Enable	0	–	0.2	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 3.0 V, T_A = 25°C, RF = –30 dBm @ 1.9 GHz, Rx Enable = 3.0 V, unless otherwise noted. Tested in Circuit Shown in Figure 1)

Characteristic	Symbol	Min	Typ	Max	Unit
RF Gain	–	16	18	–	dB
SSB Noise Figure	–	–	1.6	–	dB
RF Output 3rd Order Intercept Point	–	–	13	–	dBm
Output 1 dB Gain Compression	–	–3.0	1.0	–	dBm
Reverse Isolation (s_{12})	–	–	–34	–	dB
Input Return Loss	–	–	–12	–	dB
Output Return Loss	–	–	–15	–	dB
Supply Current, Rx Mode	–	–	5.0	7.5	mA
Supply Current, Standby Mode (Rx Enable = 0 V)	–	–	–	50	μA

Figure 1. Applications Circuit Configuration



C1 1.4 pF
C2 1.4 pF
C3, C4 22 pF
L1 4.7 nH

TYPICAL CHARACTERISTICS

Figure 2. Supply Current versus Voltage

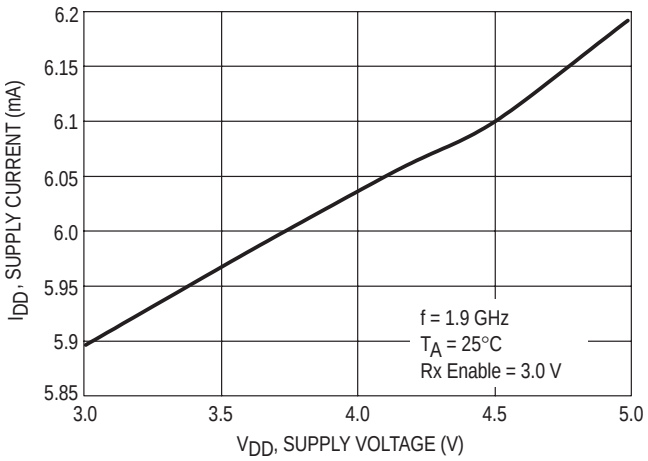


Figure 3. Output Power versus Input Power

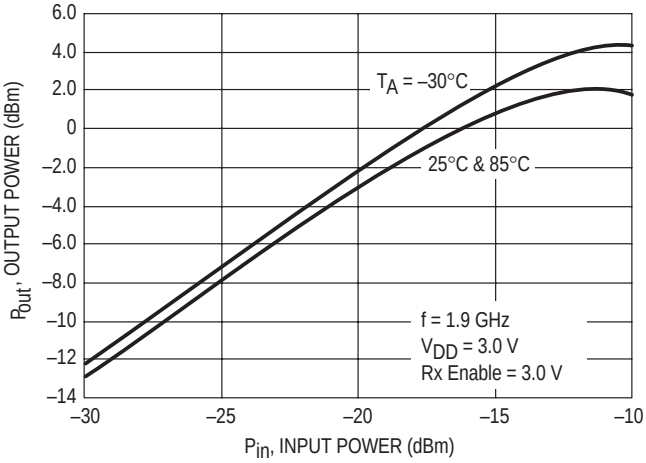


Figure 4. Output Power versus Input Power

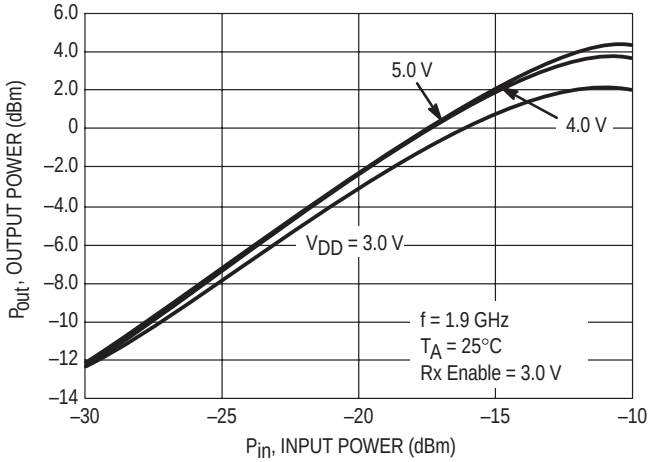


Figure 5. Gain versus Frequency

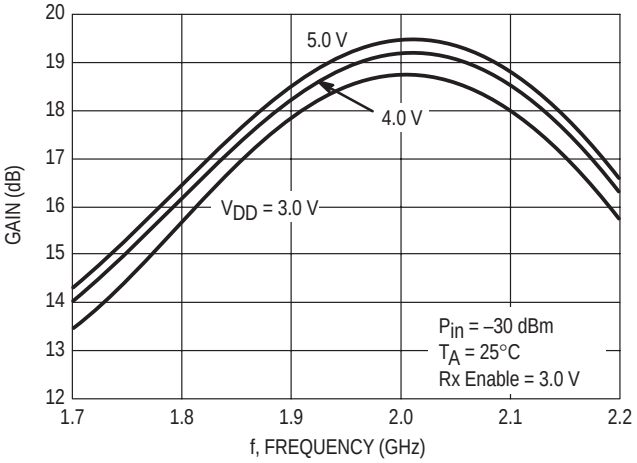


Figure 6. Gain versus Frequency

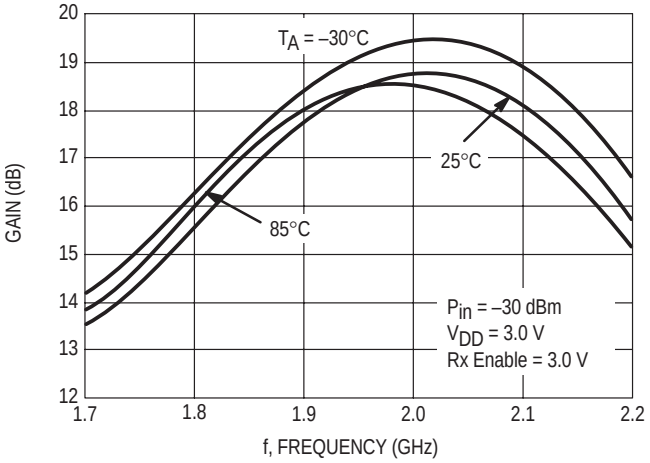
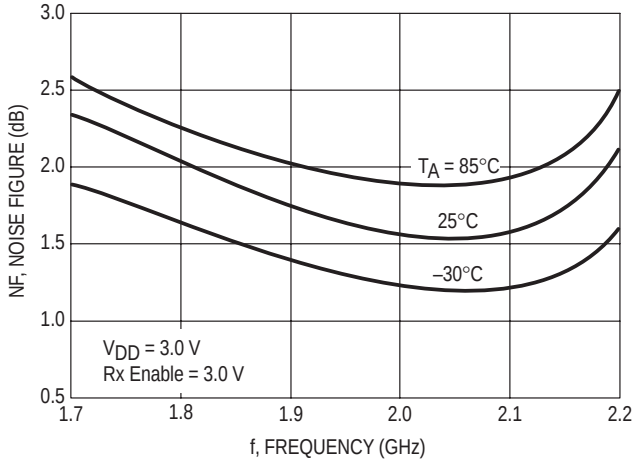


Figure 7. Noise Figure versus Frequency



TYPICAL CHARACTERISTICS

Figure 8. Reverse Isolation versus Frequency

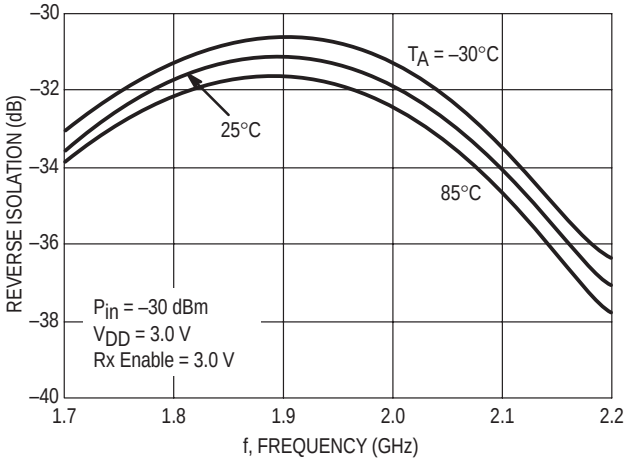


Figure 9. Reverse Isolation versus Frequency

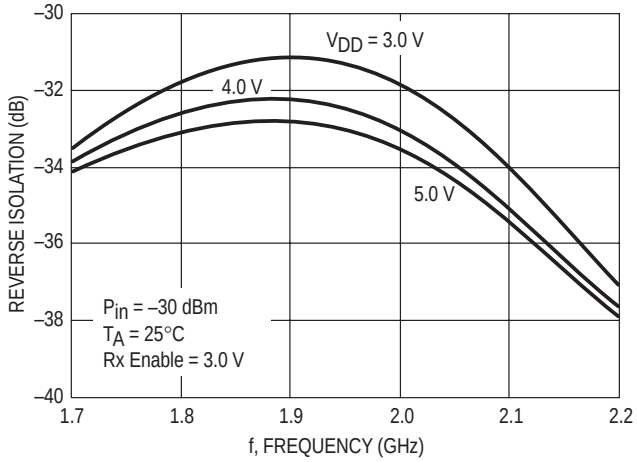


Table 1. Scattering Parameters

(V_{DD} = 3.0 V, T_A = 25°C, Rx Enable = 3.0 V, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
1500	0.907	–42	2.91	153	0.012	87	0.793	–60
1530	0.913	–43	3.11	148	0.012	85	0.765	–62
1560	0.920	–44	3.32	144	0.013	83	0.735	–64
1590	0.927	–45	3.55	139	0.013	80	0.701	–66
1620	0.935	–46	3.78	135	0.013	76	0.665	–67
1650	0.943	–47	4.02	130	0.013	73	0.627	–69
1680	0.951	–48	4.26	125	0.013	70	0.586	–70
1710	0.959	–49	4.49	119	0.012	67	0.544	–70
1740	0.967	–50	4.72	114	0.012	63	0.500	–70
1770	0.975	–52	4.94	109	0.012	59	0.458	–70
1800	0.982	–53	5.17	104	0.011	56	0.418	–68
1830	0.988	–55	5.38	98	0.011	52	0.382	–65
1860	0.993	–56	5.58	93	0.011	48	0.351	–60
1890	0.997	–58	5.76	87	0.010	44	0.329	–54
1920	0.999	–59	5.92	82	0.009	40	0.317	–48
1950	1.002	–61	6.07	76	0.008	35	0.317	–40
1980	1.004	–62	6.19	71	0.008	30	0.327	–34
2010	1.004	–64	6.29	65	0.007	25	0.346	–28
2040	1.003	–65	6.37	60	0.006	19	0.371	–24
2070	1.002	–67	6.43	55	0.005	11	0.401	–21
2100	0.999	–68	6.50	50	0.004	2	0.433	–20
2130	0.996	–70	6.55	45	0.004	–10	0.467	–19
2160	0.994	–71	6.61	40	0.003	–29	0.499	–19
2190	0.991	–73	6.67	35	0.003	–52	0.530	–19
2220	0.989	–74	6.70	31	0.003	–80	0.560	–20
2250	0.984	–76	6.70	26	0.003	–100	0.589	–21
2280	0.981	–77	6.66	21	0.004	–113	0.615	–22
2310	0.975	–79	6.59	16	0.005	–122	0.639	–23
2340	0.968	–80	6.51	13	0.006	–130	0.661	–25
2370	0.960	–82	6.48	9	0.007	–135	0.681	–26
2400	0.953	–83	6.47	5	0.008	–140	0.698	–28
2430	0.944	–84	6.48	2	0.009	–145	0.714	–30
2460	0.937	–86	6.50	–2	0.011	–149	0.727	–31
2490	0.929	–87	6.52	–7	0.012	–154	0.739	–33
2520	0.922	–88	6.49	–11	0.013	–158	0.750	–34
2550	0.915	–90	6.43	–15	0.014	–161	0.758	–36
2580	0.908	–91	6.33	–19	0.015	–163	0.766	–38

Table 2. Scattering Parameters

(V_{DD} = 4.0 V, T_A = 25°C, Rx Enable = 3.0 V, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
1500	0.893	–42	3.20	151	0.012	87	0.797	–60
1530	0.899	–43	3.42	147	0.012	85	0.770	–62
1560	0.906	–44	3.65	143	0.012	82	0.740	–64
1590	0.914	–45	3.90	138	0.012	80	0.707	–65
1620	0.921	–46	4.15	134	0.013	77	0.671	–67
1650	0.929	–47	4.41	129	0.013	73	0.633	–68
1680	0.936	–48	4.67	124	0.013	70	0.593	–70
1710	0.945	–49	4.93	119	0.012	67	0.551	–70
1740	0.953	–50	5.18	113	0.012	63	0.507	–71
1770	0.960	–52	5.43	108	0.012	60	0.465	–70
1800	0.967	–53	5.66	103	0.011	57	0.424	–68
1830	0.973	–55	5.89	97	0.011	53	0.387	–66
1860	0.979	–56	6.11	92	0.011	50	0.355	–61
1890	0.982	–58	6.32	87	0.010	46	0.330	–56
1920	0.985	–59	6.51	81	0.009	43	0.317	–49
1950	0.987	–61	6.68	75	0.008	39	0.314	–42
1980	0.988	–62	6.81	70	0.008	32	0.322	–35
2010	0.989	–64	6.92	65	0.007	26	0.339	–29
2040	0.988	–65	7.02	60	0.006	20	0.364	–25
2070	0.986	–67	7.09	54	0.005	13	0.394	–22
2100	0.984	–68	7.17	49	0.005	4	0.425	–20
2130	0.980	–70	7.23	44	0.004	–7	0.459	–19
2160	0.978	–71	7.30	40	0.003	–21	0.491	–18
2190	0.975	–73	7.35	35	0.003	–39	0.524	–19
2220	0.972	–74	7.39	30	0.002	–69	0.554	–19
2250	0.968	–76	7.38	25	0.003	–93	0.584	–20
2280	0.964	–77	7.34	20	0.004	–109	0.611	–21
2310	0.958	–79	7.26	16	0.004	–118	0.635	–23
2340	0.950	–80	7.18	12	0.005	–126	0.658	–24
2370	0.942	–82	7.14	8	0.007	–133	0.678	–26
2400	0.934	–83	7.14	4	0.008	–138	0.695	–28
2430	0.927	–84	7.15	1	0.009	–145	0.712	–29
2460	0.920	–85	7.16	–3	0.010	–150	0.726	–31
2490	0.912	–87	7.17	–8	0.011	–154	0.738	–33
2520	0.905	–88	7.14	–12	0.012	–158	0.749	–34
2550	0.897	–89	7.07	–16	0.013	–161	0.758	–36
2580	0.891	–91	6.95	–20	0.014	–163	0.766	–38

Table 3. Scattering Parameters

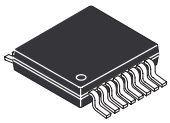
(V_{DD} = 5.0 V, T_A = 25°C, Rx Enable = 3.0 V, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
1500	0.876	–42	3.50	150	0.012	87	0.799	–59
1530	0.883	–43	3.73	146	0.012	85	0.773	–61
1560	0.891	–44	3.98	141	0.012	83	0.744	–63
1590	0.898	–45	4.25	137	0.012	80	0.712	–65
1620	0.906	–46	4.52	132	0.012	77	0.677	–67
1650	0.914	–47	4.80	127	0.012	74	0.640	–68
1680	0.921	–48	5.08	122	0.012	71	0.600	–69
1710	0.928	–49	5.36	117	0.012	67	0.559	–70
1740	0.936	–51	5.63	112	0.012	64	0.517	–70
1770	0.944	–52	5.90	107	0.012	60	0.475	–70
1800	0.950	–53	6.16	102	0.011	57	0.435	–69
1830	0.956	–55	6.41	96	0.011	54	0.397	–66
1860	0.961	–56	6.66	91	0.010	50	0.365	–62
1890	0.965	–58	6.89	85	0.010	47	0.339	–57
1920	0.967	–59	7.10	80	0.009	43	0.323	–51
1950	0.968	–61	7.29	74	0.009	39	0.318	–44
1980	0.969	–62	7.44	69	0.008	35	0.323	–37
2010	0.970	–64	7.56	64	0.007	29	0.338	–31
2040	0.969	–66	7.66	58	0.006	24	0.361	–26
2070	0.966	–67	7.75	53	0.006	18	0.389	–23
2100	0.963	–69	7.84	48	0.005	10	0.420	–21
2130	0.960	–70	7.91	43	0.004	0	0.453	–19
2160	0.957	–72	7.98	38	0.003	–15	0.485	–19
2190	0.954	–73	8.04	34	0.003	–34	0.517	–19
2220	0.951	–75	8.08	29	0.002	–59	0.547	–20
2250	0.946	–76	8.07	24	0.003	–83	0.576	–21
2280	0.942	–78	8.02	19	0.003	–104	0.603	–22
2310	0.936	–79	7.93	14	0.004	–116	0.629	–23
2340	0.928	–81	7.84	10	0.005	–125	0.652	–24
2370	0.920	–82	7.80	7	0.006	–132	0.672	–26
2400	0.912	–83	7.79	3	0.007	–138	0.690	–28
2430	0.904	–84	7.79	–1	0.008	–143	0.707	–29
2460	0.896	–86	7.81	–5	0.009	–148	0.720	–31
2490	0.889	–87	7.81	–9	0.010	–152	0.733	–33
2520	0.882	–88	7.78	–13	0.011	–155	0.744	–34
2550	0.874	–89	7.69	–17	0.012	–158	0.754	–36
2580	0.869	–91	7.56	–21	0.013	–161	0.762	–38

The MRFIC Line
1.9 GHz GaAs Upconverter

MRFIC1813

1.9 GHz UPMIXER AND EXCITER AMPLIFIER

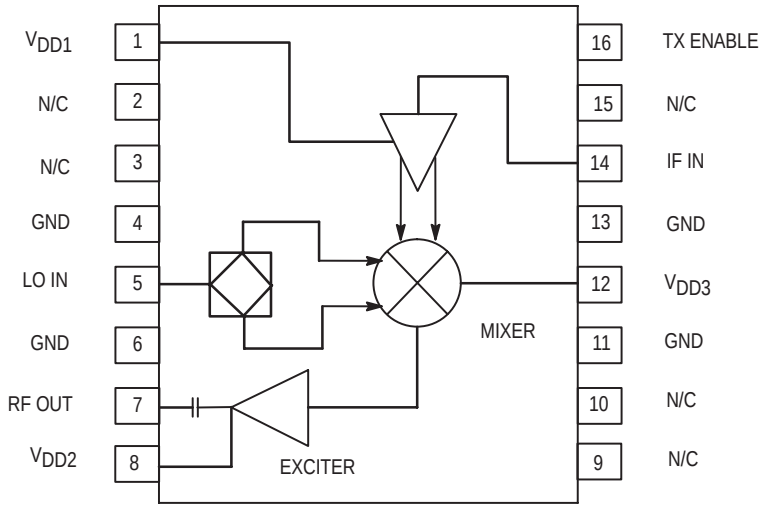


CASE 948C–03
(TSSOP–16)

Designed primarily for use in wireless Personal Communication Systems (PCS) applications such as Digital European Cordless Telephone (DECT), Japan's Personal Handy System (PHS) and the emerging North American systems. The MRFIC1813 is also applicable to 2.4 GHz ISM equipment. The device combines a balanced upmixer and a transmit exciter amplifier in a low-cost TSSOP–16 package. Minimal off-chip matching is required while allowing for maximum flexibility and efficiency. The mixer is optimized for low–side injection and provides more than 12 dB of conversion gain with over 0 dBm output at 1 dB gain compression. Image filtering is implemented off-chip to allow maximum flexibility. A CMOS compatible ENABLE pin allows standby operation where the current drain is less than 250 μA.

Together with other devices from the MRFIC180X or the MRFIC240X series, this GaAs IC family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone or 2.4 GHz ISM band equipment.

- Usable Frequency Range = 1.7 to 2.5 GHz
- 15 dB Typ IF to RF Conversion Gain
- 3 dBm Power Output Typ, 0 dBm Minimum at 1 dB Gain Compression
- Simple Off-chip Matching for Maximum Flexibility
- Low Power Consumption = 75 mW (Typ)
- Single Bias Supply = 2.7 to 4.5 Volts
- Low LO Power Requirement = – 5 dBm (Typ)
- Low Cost Surface Mount Plastic Package
- Order MRFIC1813R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1813



Pin Connections and Functional Block Diagram

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

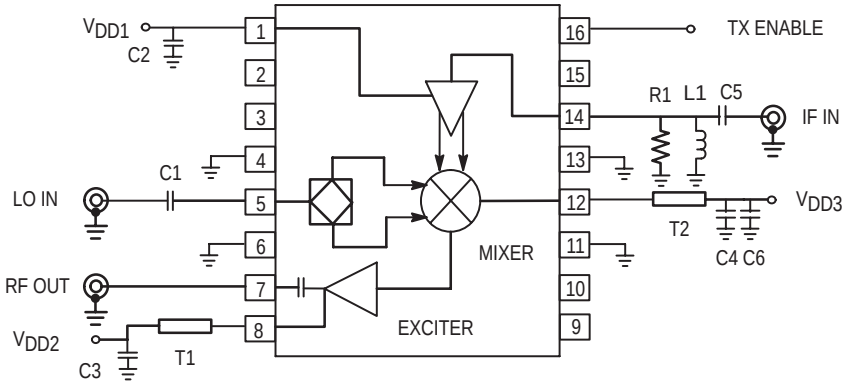
Ratings	Symbol	Limit	Unit
Supply Voltage	V_{DD1}, V_{DD2}, V_{DD3}	5.5	Vdc
IF Input Power	P_{IF}	3	dBm
LO Input Power	P_{LO}	3	dBm
Enable Voltage	TX ENABLE	5.5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to +85	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Output Frequency	f_{RF}	1.7 to 2.5	GHz
LO Input Frequency	f_{LO}	1.5 to 2.4	GHz
IF Input Frequency	f_{IF}	70 to 350	MHz
Supply Voltage	V_{DD}	2.7 to 4.5	Vdc
TX Enable Voltage, ON	TX ENABLE	2.7 to V_{DD}	Vdc
TX Enable Voltage, OFF	TX ENABLE	0 to 0.2	Vdc

ELECTRICAL CHARACTERISTICS ($V_{DD1,2,3}$, TX ENABLE= 3 V, T_A = 25°C, f_{LO} = 1.65 GHz @ – 5 dBm, f_{IF} = 250 MHz @ –15 dBm)

Characteristic	Min	Typ	Max	Unit
IF to RF Small Signal Conversion Gain (P_{RF} = –35 dBm)	12	15	—	dB
RF Output 1 dB Gain Compression	0	3	—	dBm
RF Output 3rd Order Intercept	—	11	—	dBm
LO Feedthrough to RF Port	—	–15	–10	dBm
Noise Figure	—	11	—	dB
Lower Sideband Output Power at RF Port	—	–10	–6	dBm
Supply Current TX Mode	—	25	35	mA
Supply Current Standby Mode (TX ENABLE = 0 V, LO Off)	—	100	250	μA
TX Enable Current	—	3	—	μA



C1, C2, C3, C4 15 pF
C6 1 μF
R1 300 Ω
T1, T2 MICROSTRIP, Z_0 = 73 Ω, θ = 29° @ 1.9 GHz
BOARD MATERIAL – GLASS/EPOXY, ε_r = 4.45,
DIELECTRIC THICKNESS = 0.018 INCH

IF Frequency	L1	C5
110 MHz	180 nH	12 pF
250 MHz	68 nH	5.6 pF
350 MHz	39 nH	3.9 pF

Figure 1. Applications Circuit Configuration

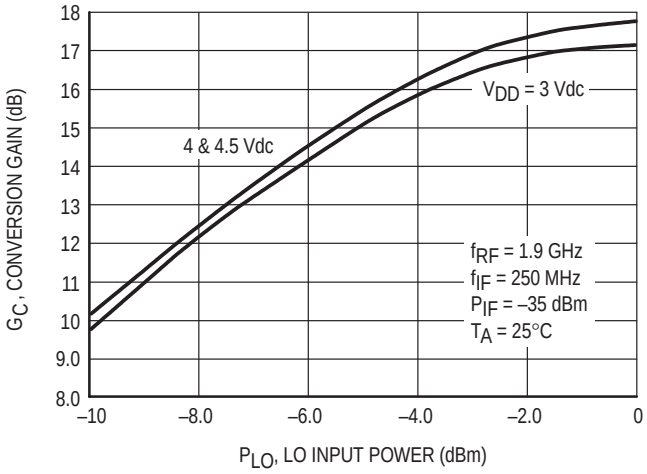


Figure 2. Conversion Gain versus LO Power

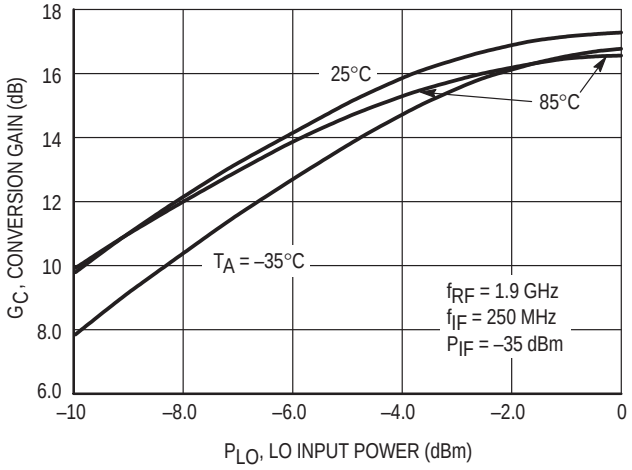


Figure 3. Conversion Gain versus LO Power

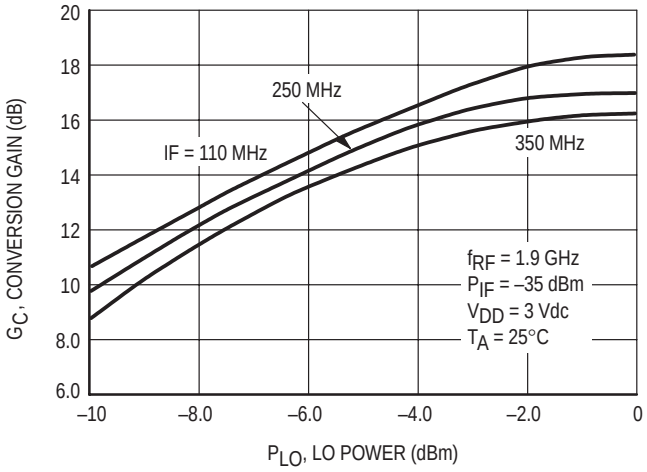


Figure 4. Conversion Gain versus LO Power

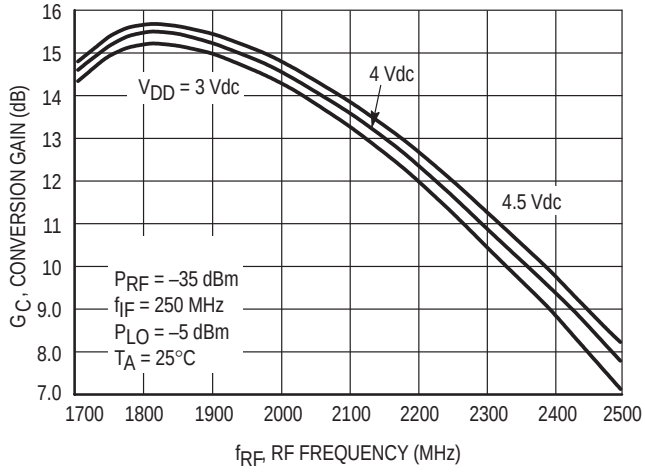


Figure 5. Conversion Gain versus RF Frequency

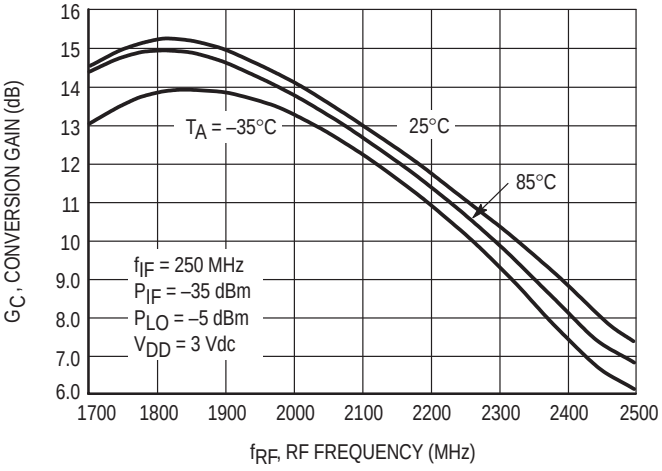


Figure 6. Conversion Gain versus RF Frequency

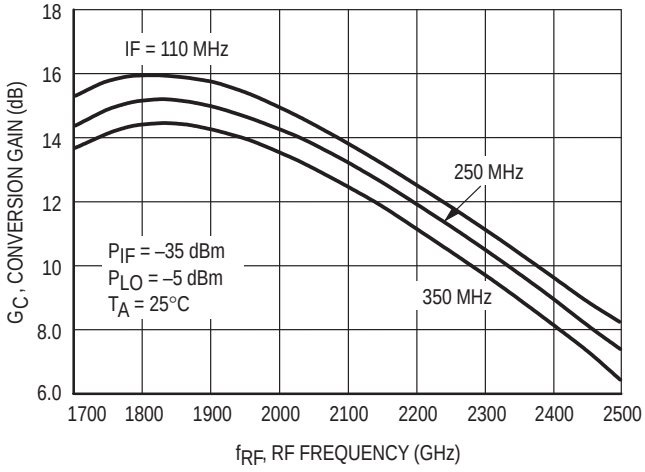


Figure 7. Conversion Gain versus RF Frequency

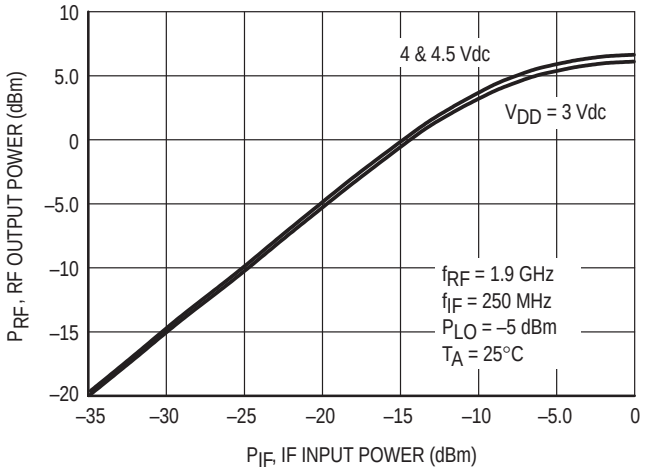


Figure 8. RF Output versus Input Power

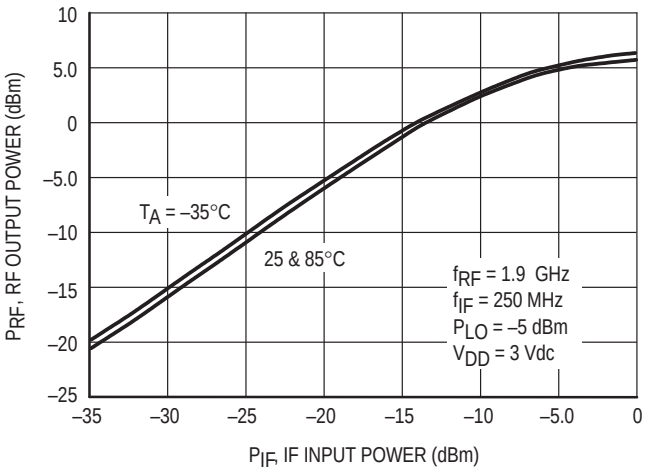


Figure 9. RF Output Power versus IF Input Power

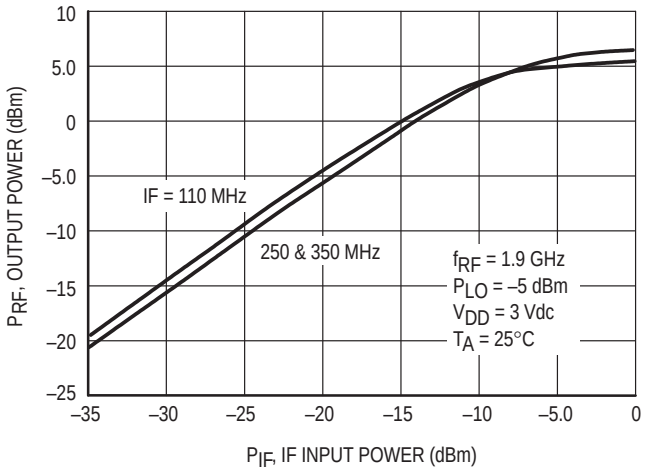


Figure 10. RF Output versus IF Input Power

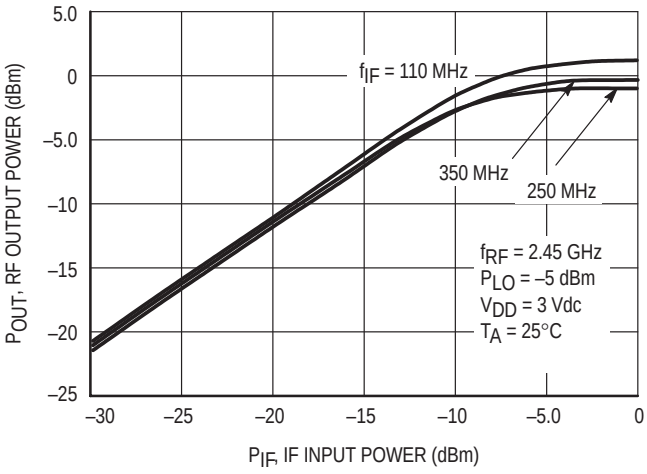


Figure 11. Output Power versus IF Input Power

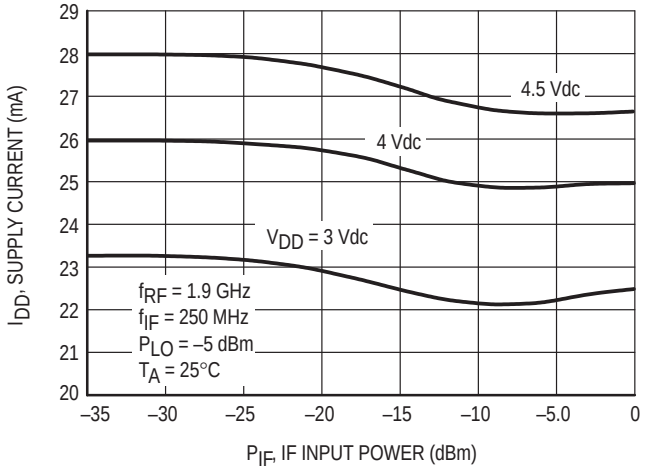


Figure 12. Supply Current versus IF Input Power

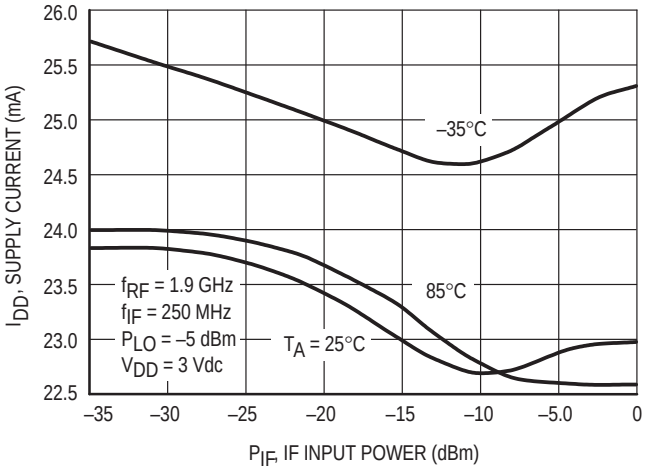


Figure 13. Supply Current versus IF Input Power

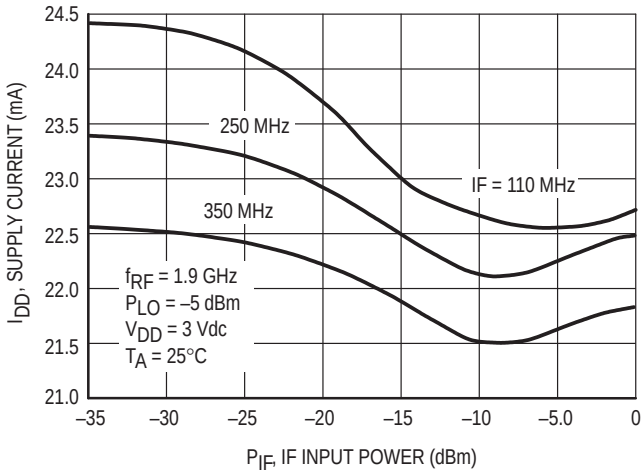


Figure 14. Supply Current versus IF Input Power

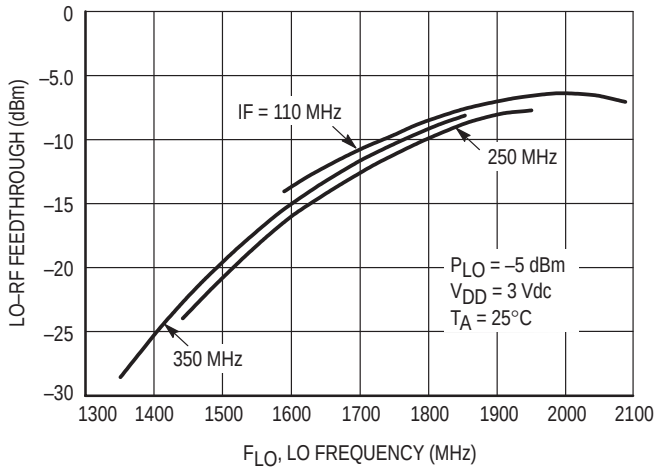


Figure 15. LO to RF Feedthrough versus LO Frequency

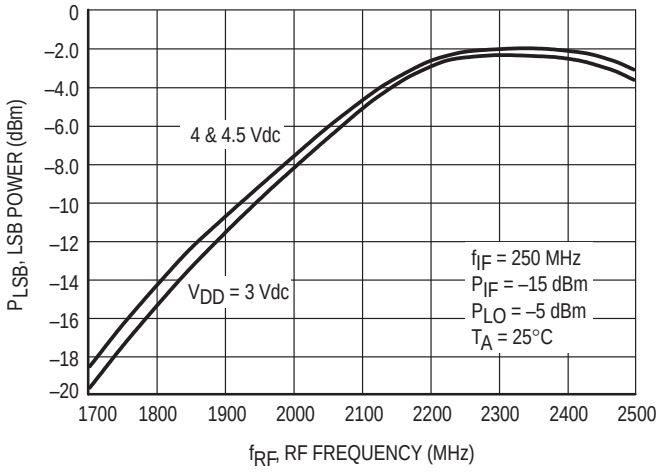


Figure 16. Lower Side Band Power versus RF Frequency

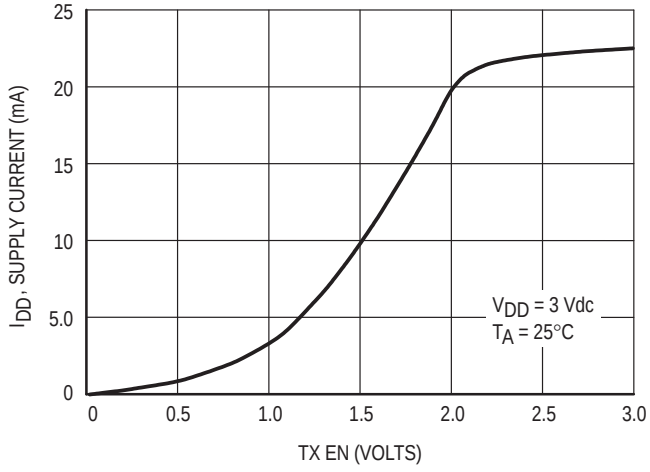


Figure 17. Supply Current versus Transmit Enable Voltage

f	IF Input		LO Input		RF Output (1)	
(MHz)	R	jX	R	jX	R	jX
70	8.3	–452.4				
100	7.3	–318.5				
150	7.1	–211.3				
200	6.6	–156.4				
250	6.5	–123.1				
300	6.1	–100.7				
350	5.7	–84.2				
1100			62.5	3.1		
1200			58.1	4.3		
1300			53.7	4.7		
1400			50.2	4.2		
1500			47.3	3.9		
1600			44.4	3.2		
1700			42.0	1.6	30.4	33.6
1800			40.6	0.5	42.6	16.9
1900			39.6	–0.7	49.1	2.3
2000			38.7	–2.2	40.6	14.2
2100			38.2	–3.6	33.8	17.7
2200			38.4	–5.1	33.3	15.7
2300			38.9	–6.5	32.9	13.7
2400			39.5	–7.8	29.6	13.2
2500					27.4	11.9

(1) Includes T1 shown in Figure 1.

Table 1. Port Impedances versus Frequency (V_{D1}, V_{D2}, V_{D3}, TX EN = 3 Vdc)

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

The MRFIC1813 combines a single–balanced MESFET mixer with an exciter amplifier. It is usable for transmit frequencies from 1.7 to 2.5 GHz and IF frequencies from 70 to 350 MHz. The design is optimized for low–side local oscillator injection in hetrodyne transmit applications.

Minimal off–chip matching is required while allowing for flexibility and performance optimization. An active balun is employed at the IF port which gives good balance down to at least 70 MHz. A passive splitter is used at the LO input to complete the single–balanced configuration.

CIRCUIT CONSIDERATIONS

Figure 1 shows the application circuit used to gather the data presented in the characterization curves. As shown in Table 1, the IF port impedance is very high. Three hundred ohms was chosen for R1 to shunt the IF port as a compromise of gain and bandwidth. A 50 Ω resistor can be used and L1 and C5 eliminated to provide a broadband match. The conversion gain is reduced to about 8 dB. Microstrip inductors T1 and T2 combine with inductance internal to the device to form RF chokes. Some tuning of the RF output can be achieved with T1.

As with all RF devices, circuit layout is important. Controlled impedance lines should be used for all RF and IF interconnects. As shown in Figure 1, power supply by–passing should be used to avoid device instability. Ground vias should be included near all ground connections indicated in the schematic. Off–chip components should be mounted as close to the IC leads as possible.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” to the device type. For a complete list of currently available boards and one in development for newly introduced products, please contact your local Motorola Distributor or Sales Office.

MOTOROLA

MRFIC1814

1.9 GHz GaAs Downconverter

Designed primarily for use in wireless Personal Communication Systems (PCS) applications such as Digital European Cordless Telephone (DECT), Japan's Personal Handy System (PHS), and the emerging North American systems. The MRFIC1814 includes a low noise amplifier and downmixer in a low-cost TSSOP–16 package. The integrated circuit requires minimal off-chip matching while allowing for the maximum in flexibility and efficiency. The mixer is optimized for low–side injection and offers reasonable intercept point as well as high efficiency with 8.0 dB of conversion gain. Image filtering is implemented off-chip to allow maximum flexibility. CMOS compatible ENABLE pins allow standby operation where the current drain is less than 0.1 mA.

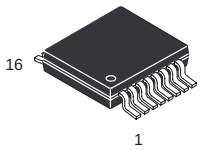
Together with the rest of the MRFIC18XX series, this GaAs IC family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

- Usable Frequency Range = 1.8 to 2.0 GHz
- 17 dB Typ Gain, 2.5 dB Typ Noise Figure LNA
- 8.0 dB Typ Gain, 10 dB Typ Noise Figure Mixer
- –5.5 dBm Typ Mixer Input Intercept Point
- Simple LO/IF Off-chip Matching for Maximum Flexibility
- Low Power Consumption = 39 mW (Typ)
- Single Bias Supply = 2.7 to 4.5 V
- Low LO Power Requirement = –5.0 dBm (Typ)
- Low Cost Surface Mount Plastic Package

NOT RECOMMENDED FOR NEW DESIGN
DEVICE TO BE PHASED OUT.
No replacement available.

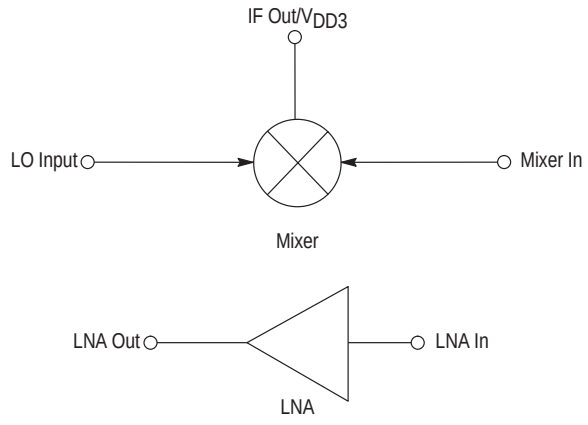
1.8 GHz LOW NOISE AMPLIFIER AND DOWNMIXER

SEMICONDUCTOR TECHNICAL DATA

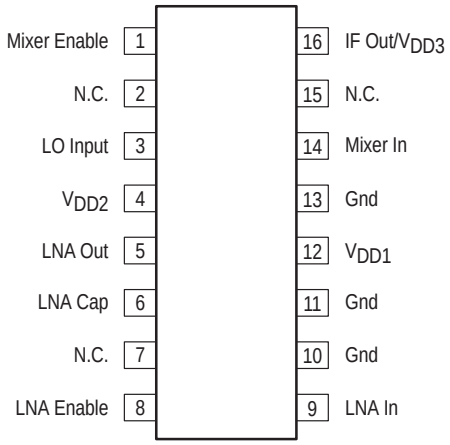


PLASTIC PACKAGE
CASE 948C
(TSSOP–16)

Functional Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MRFIC1814	T_A = – 40° to +85°C	TSSOP–16
MRFIC1814R2		TSSOP–16 Tape & Reel*

*2,500 Units per 16 mm, 13 inch reel.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	5.5	Vdc
LNA Input Power	LNA_{In}	10	dBm
LO Input Power	P_{LO}	10	dBm
Enable Voltage	Enable	5.5	Vdc
Storage Temperature Range	T_{stg}	–65 to 150	°C
Operating Ambient Temperature	T_A	–30 to 85	°C

NOTES: 1. Meets Human Body Model (HBM) ≤100 V.
2. ESD data available upon request.

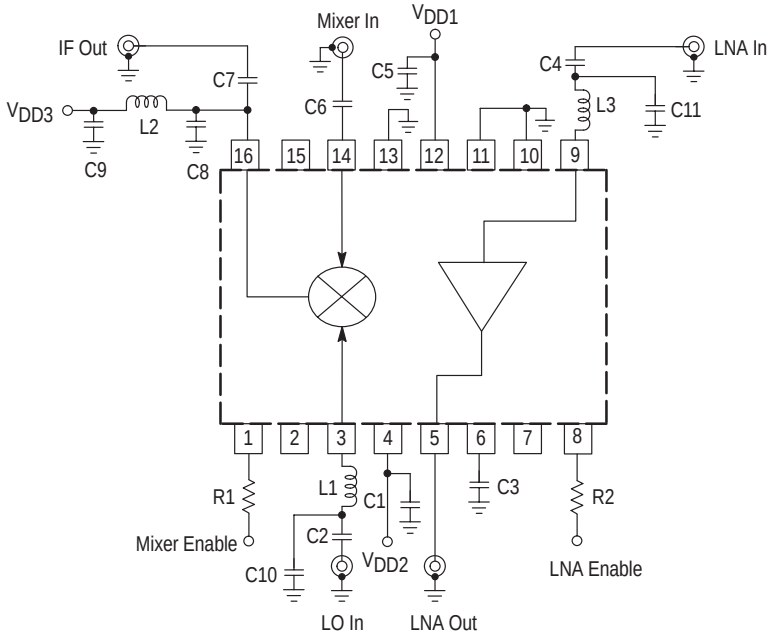
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min	Typ	Max	Unit
RF Input Frequency	f_{RF}	1.8	–	2.0	GHz
Mixer LO Frequency	f_{LO}	1.5	–	1.8	GHz
IF Output Frequency	f_{IF}	70	–	300	MHz
Supply Voltage	V_{DD}	2.7	–	4.5	Vdc
Enable Voltage, On	Mixer, LNA Enable	2.7	–	V_{DD}	Vdc
Enable Voltage, Off	Mixer, LNA Enable	0	–	0.2	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 3.0 V, T_A = 25°C, LO = 1.65 GHz @ –5.0 dBm, RF = 1.9 GHz @ –30 dBm, Mixer & LNA Enable = 3.0 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
LNA Gain (LNA Enable = 3.0 V)	–	14	17	–	dB
LNA Gain (LNA Enable = 0 V)	–	–	–19	–	dB
LNA Noise Figure	–	–	2.5	–	dB
LNA Input 3rd Order Intercept	–	–	–7.0	–	dBm
LNA Output 1.0 dB Gain Compression Point	–	–6.0	–3.0	–	dBm
Mixer Conversion Gain (into 50 Ω)	–	5.0	8.0	–	dB
Mixer Noise Figure	–	–	10	–	dB
Mixer Input 3rd Order Intercept	–	–	–5.0	–	dBm
Mixer Output 1.0 dB Gain Compression Point	–	–8.5	–5.5	–	dBm
Total Supply Current (Enable Voltages = 3.0 V, LO Off)	–	–	10	17	mA
Total Supply Current (Enable Voltages = 3.0 V, LO On)	–	–	13	–	mA
Standby Mode Current (Enable Voltages = 0 V, LO Off)	–	–	0.05	0.25	mA

Figure 1. Applications Circuit Configuration for 250 MHz IF



C1, C2, C4	15 pF	C11	1.6 pF
C3	3.0 pF	L1	4.7 nH
C5	30 pF	L2	10 nH
C6, C8	10 pF	L3	3.9 nH
C7	12 pF	R1, R2	10 kΩ
C9	560 pF	Board Material Glass/Epoxy, ε_r = 4.45,	
C10	3.6 pF	0.018 Inch Dielectric Thickness	

Figure 2. Equivalent IF Output Circuit

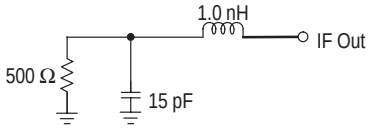


Figure 3. LNA Gain versus Frequency

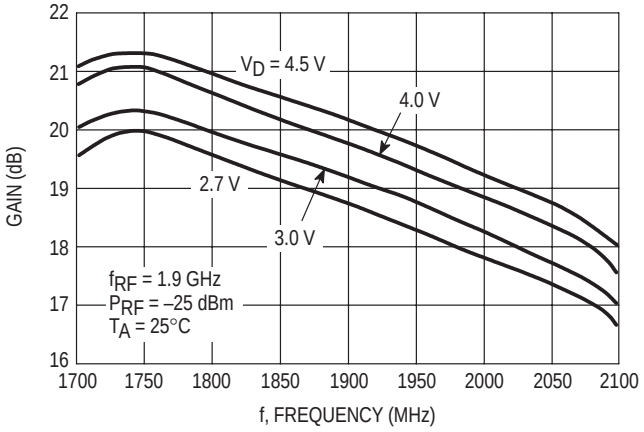


Figure 4. LNA Input 1.0 dB Compression versus Frequency

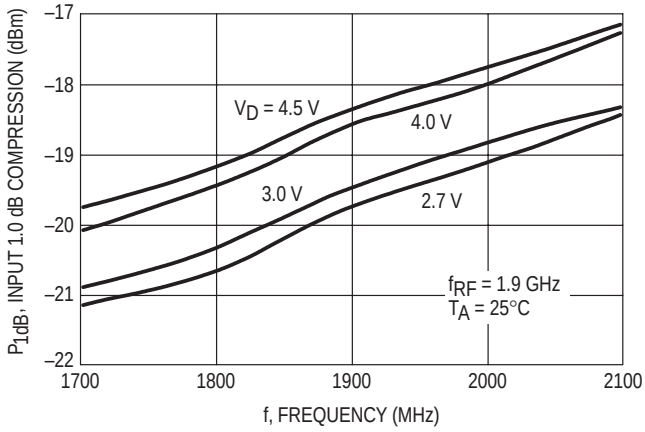


Figure 5. LNA Gain versus Frequency

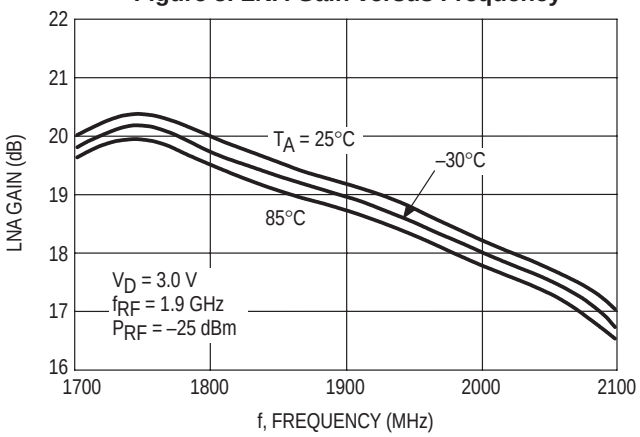


Figure 6. LNA Input 1.0 dB Compression versus Frequency

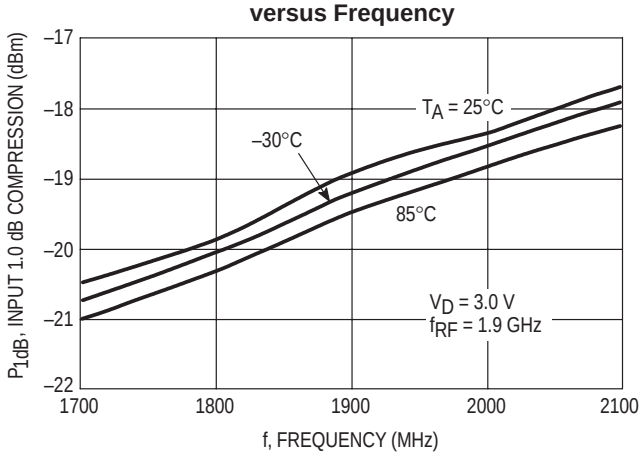


Figure 7. LNA Output Power versus Input Power

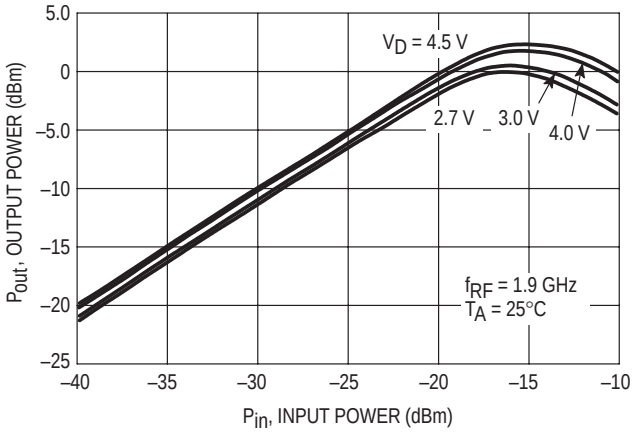


Figure 8. LNA Output Power versus Input Power

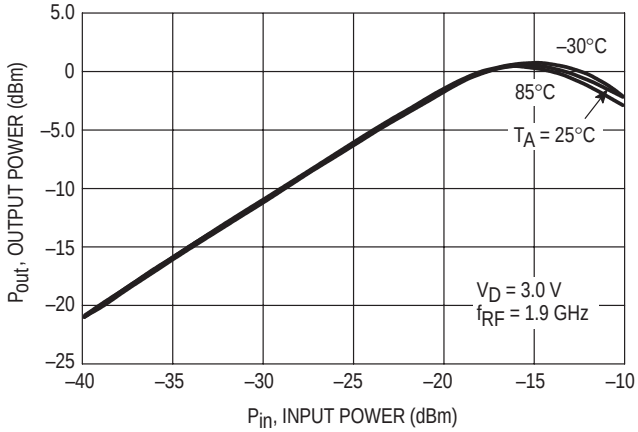


Figure 9. LNA Noise Figure versus Frequency

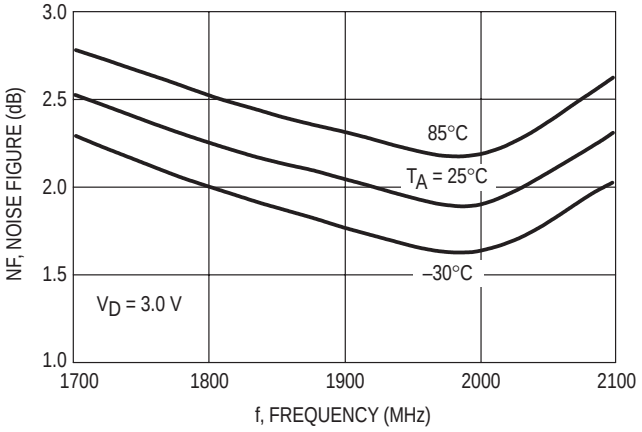


Figure 10. Mixer Noise Figure versus Frequency

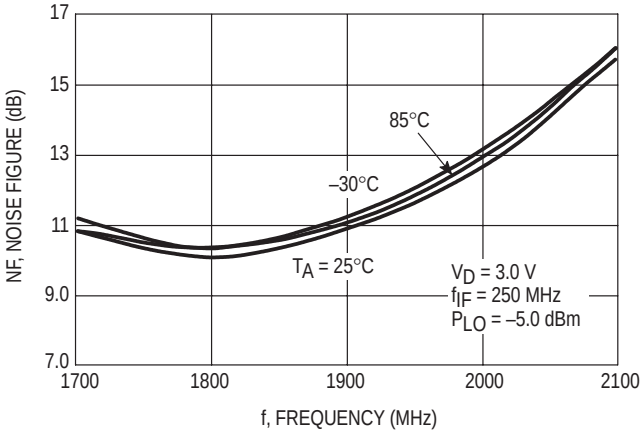


Figure 11. Mixer Noise Figure versus Frequency

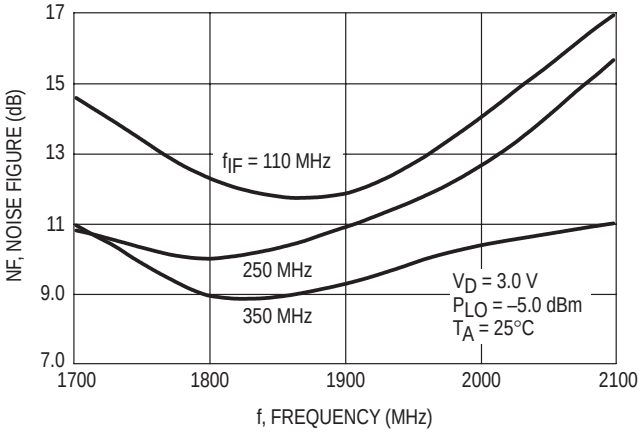


Figure 12. Mixer Conversion Gain versus LO Power

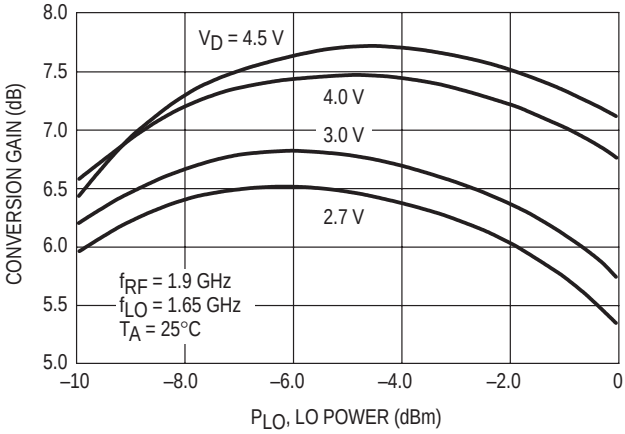


Figure 13. Mixer Conversion Gain versus LO Power

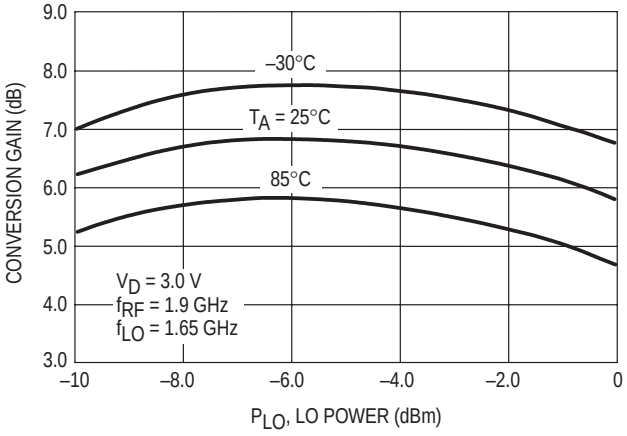


Figure 14. Mixer Conversion Gain versus Frequency

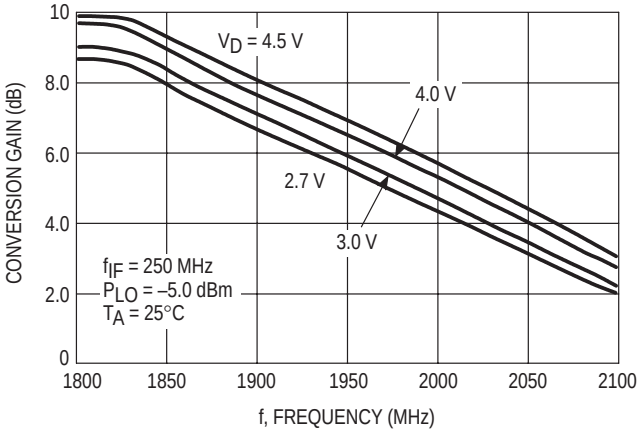


Figure 15. Mixer Conversion Gain versus Frequency

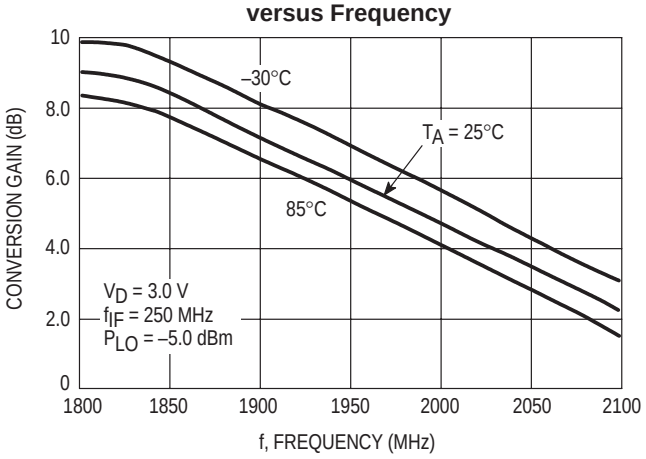


Figure 16. Mixer Conversion Gain versus Frequency

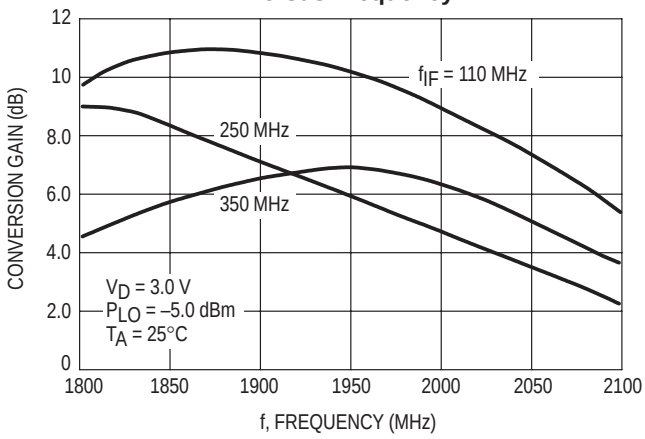


Figure 17. Mixer IF Output Power versus RF Input Power

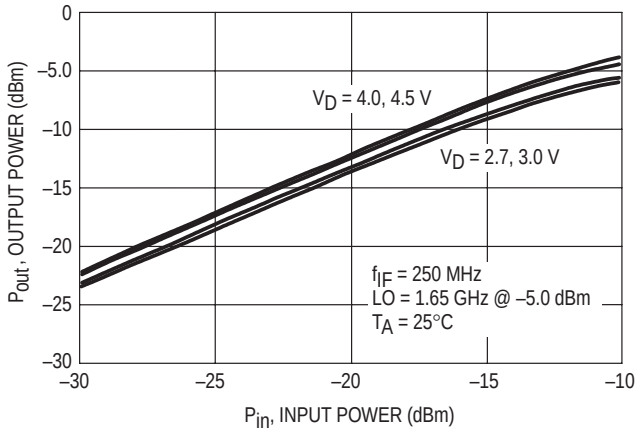


Figure 18. Mixer IF Output Power versus RF Input Power

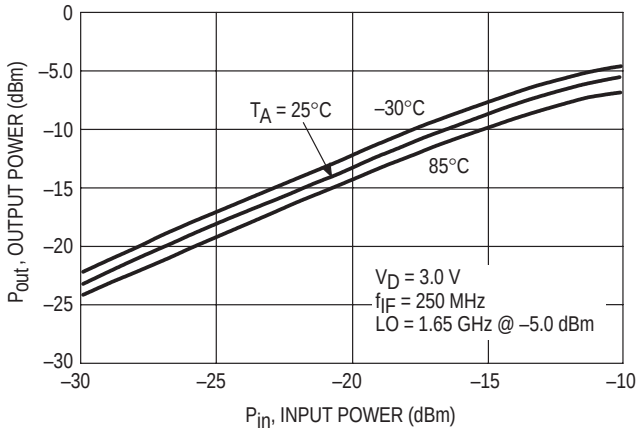


Figure 19. Mixer IF Output Power versus RF Input Power

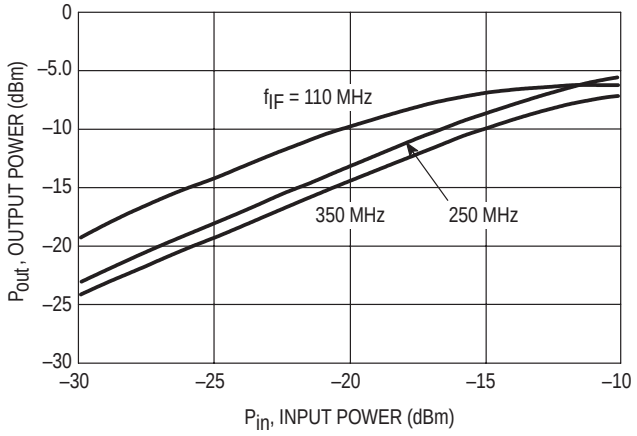


Figure 20. Total Supply Current versus Enable Voltage

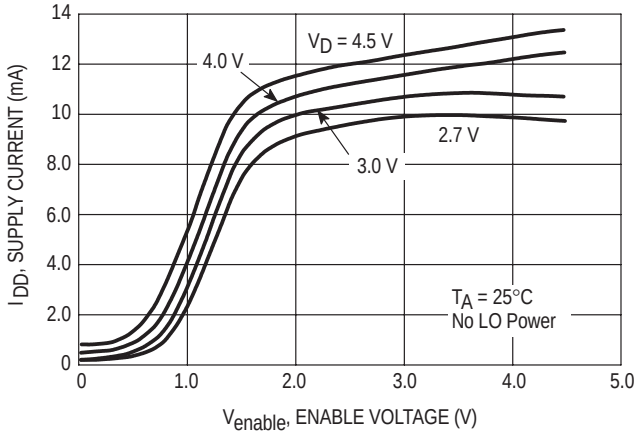


Table 1. LNA Scattering Parameters (V_{DD} = 3.0 V, T_A = 25°C, LNA Enable = 3.0 V)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$	$\lvert S_{21} \rvert$	$\angle\phi$	$\lvert S_{12} \rvert$	$\angle\phi$	$\lvert S_{22} \rvert$	$\angle\phi$
1500	0.840	–89	4.895	38.19	0.008	131.86	0.801	–55.13
1550	0.795	–92.72	5.028	29	0.009	125.54	0.779	–57.71
1600	0.734	–97.70	5.201	19.79	0.011	114.47	0.748	–60.9
1650	0.688	–101.46	5.467	12.99	0.012	106.9	0.721	–63.74
1700	0.636	–105.06	5.709	4.67	0.013	100.19	0.692	–66.43
1750	0.573	–109.56	5.903	–5.79	0.015	92.43	0.649	–70.51
1800	0.533	–113.79	6.072	–13.79	0.017	85.88	0.612	–73.59
1850	0.491	–117.18	6.214	–22.09	0.019	78.74	0.571	–77.53
1900	0.425	–121.18	6.184	–32.5	0.022	71.31	0.514	–82.96
1950	0.385	–124.25	6.273	–39.57	0.024	66.54	0.467	–86.74
2000	0.348	–128.09	6.325	–48.49	0.027	60.7	0.421	–91.62
2050	0.311	–133.47	6.131	–60.1	0.03	51.68	0.354	–98.9
2100	0.279	–139.87	5.913	–66.79	0.032	45.56	0.297	–105.36
2150	0.245	–145.18	5.830	–73.36	0.035	39.82	0.247	–112.36
2200	0.208	–150.93	5.668	–83.28	0.039	32.36	0.181	–126.37
2250	0.193	–158.52	5.466	–90.54	0.042	25	0.135	–145.26
2300	0.172	–168.94	5.208	–97.77	0.046	17.74	0.099	–174.55
2350	0.147	171.81	4.803	–105.55	0.048	9.32	0.101	136.35
2400	0.138	160.56	4.632	–111	0.05	4.19	0.136	111.97
2450	0.145	148.43	4.414	–117.57	0.054	–2.18	0.183	96.68
2500	0.165	127.94	3.989	–125.47	0.058	–13.07	0.248	81.44

Table 2. Mixer RF Port Scattering Parameters (V_{DD} = 3.0 V, T_A = 25°C, Mixer Enable = 3.0 V)

f	S_{11}		f	S_{11}		f	S_{11}	
(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$	(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$	(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$
1500	0.294	117.08	1900	0.259	47.33	2300	0.196	–5.66
1550	0.295	110.75	1950	0.241	40.96	2350	0.192	–11.74
1600	0.296	104.68	2000	0.228	34.34	2400	0.186	–19.36
1650	0.294	96.78	2050	0.225	29.79	2450	0.177	–25.26
1700	0.297	87.62	2100	0.214	21.41	2500	0.174	–33.39
1750	0.292	75.6	2150	0.204	13.8	–	–	–
1800	0.283	65.13	2200	0.205	10.5	–	–	–
1850	0.271	55.11	2250	0.206	1.34	–	–	–

Table 3. Mixer LO Port Scattering Parameters (V_{DD} = 3.0 V, T_A = 25°C, Mixer Enable = 3.0 V)

f	S_{11}		f	S_{11}		f	S_{11}	
(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$	(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$	(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$
1500	0.281	–85.60	1900	0.149	–103.02	2300	0.089	161.65
1550	0.265	–87.18	1950	0.134	–108.65	2350	0.108	148.38
1600	0.243	–89.74	2000	0.123	–115.69	2400	0.124	142.34
1650	0.235	–91.48	2050	0.114	–125.16	2450	0.139	137.15
1700	0.221	–93.04	2100	0.102	–132.09	2500	0.155	131.10
1750	0.205	–94.56	2150	0.094	–143.46	–	–	–
1800	0.186	–96.12	2200	0.082	–161.69	–	–	–
1850	0.171	–98.21	2250	0.081	177.29	–	–	–

MOTOROLA

1800 MHz GaAs Integrated Power Amplifier

Designed specifically for application in Pan European digital 1.0 watt DCS1800/PCS1900 handheld radios, the MRFIC1817 is specified for 32 dBm output power with power gain over 27 dB from a 3.6 V supply. To achieve this superior performance, Motorola's planar GaAs MESFET process is employed. The device is packaged in the PFP–16 Power Flat Package which gives excellent thermal and electrical performance through a solderable backside contact while allowing the convenience and cost benefits of reflow soldering.

- Minimum Output Power Capabilities
  - 32 dBm @ 3.6 V
  - 30 dBm @ 3.0 V
- Typical Volt Characteristics
  - RF Input Power = 5.0 dBm
  - RF Output Power = 33.5 dBm
  - Typical PAE = 42%
- Low Current required from Negative Supply –2.0 mA max
- Guaranteed Stability and Ruggedness
- Device Marking = M1817

MAXIMUM RATINGS (T_A = 25°C, Z_O = 50 Ω, unless otherwise noted)

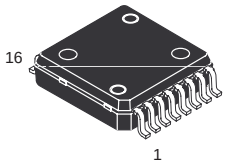
Rating	Symbol	Value	Unit
DC Positive Supply Voltage	$V_{D1, 2, 3}$	6.0	Vdc
DC Negative Supply Voltage	V_{SS}	–5.0	Vdc
RF Input Power	P_{in}	10	dBm
RF Output Power	P_{out}	35	dBm
Operating Case Temperature Range	T_C	–35 to 85	°C
Storage Temperature Range	T_{stg}	–55 to 150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W

NOTES: 1. ESD data available upon request.
2. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.

MRFIC1817

1700 TO 1900 MHz DCS1800/PCS1900 GaAs IPA

SEMICONDUCTOR TECHNICAL DATA



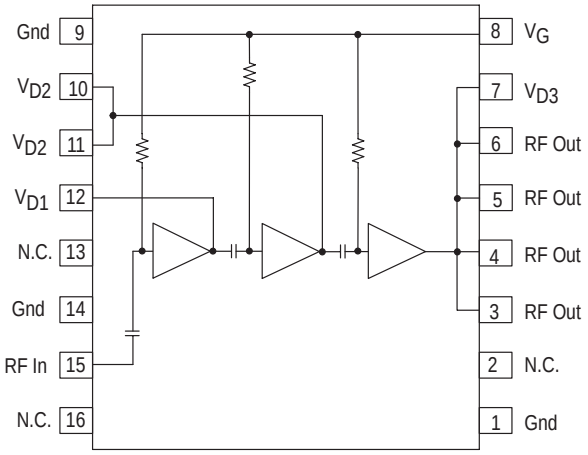
(Scale 2:1)

PLASTIC PACKAGE
CASE 978
(PFP–16, Tape & Reel Only)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MRFIC1817R2	T_C = –35° to 85°C	PFP–16

Pin Connections and Functional Block Diagram



RECOMMENDED OPERATING RANGES

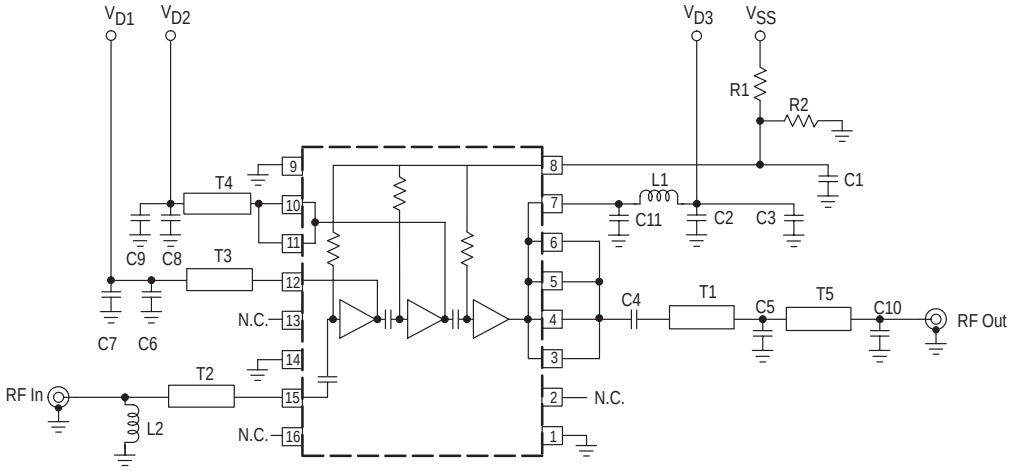
Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{D1, 2, 3}$	2.7	–	5.0	Vdc
Gate Voltage	V_{SS}	–3.5	–	–4.5	Vdc
RF Frequency Range	f_{RF}	1700	–	1900	MHz
RF Input Power	P_{RF}	0	–	6.0	dBm

ELECTRICAL CHARACTERISTICS ($V_{D1, 2, 3}$ = 3.6 V, V_{SS} = –4 V, P_{in} = 5.0 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted. Measured in Reference Circuit Shown in Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range		1710	–	1785	MHz
Output Power		32	33.5	–	dBm
Power Added Efficiency		35	42	–	%
Output Power (PCS 1900 Tuning f = 1850 to 1910 MHz)		–	33.5	–	dBm
Power Added Efficiency (PCS 1900 Tuning f = 1850 to 1910 MHz)		–	42	–	%
Input VSWR		–	2:1	–	VSWR
Harmonic Output (2nd and 3rd)		–	–35	–30	dBc
Output Power at Low voltage (V_{D1}, V_{D2}, V_{D3} = 3.0 V)		30	32	–	dBm
Output Power Isolation (V_{D1}, V_{D2}, V_{D3} = 0 V)		–	–40	–30	dBm
Noise Power (In 100 kHz, 1805 to 1880 MHz)		–	–85	–80	dBm
Stability – Spurious Output (P_{in} = 5 dBm, P_{out} = 0 to 33 dBm, Load VSWR = 6:1 at any Phase Angle, Source VSWR = 3:1, at any Phase Angle) (1)		–	–	–60	dBc
Load Mismatch stress (P_{out} = 33 dBm, Load VSWR = 10:1 at any Phase Angle) (1)		No Degradation in Output Power after Returning to Standard Conditions			
3 dB V_{DD} Bandwidth		–	2.0	–	MHz
Negative Supply Current		–	0.7	2.0	mA

NOTES: 1. Adjust $V_{D1, 2, 3}$ (0 to 3.6 V) for specified P_{out}; Duty Cycle = 12.5%, Period = 4.6 ms.

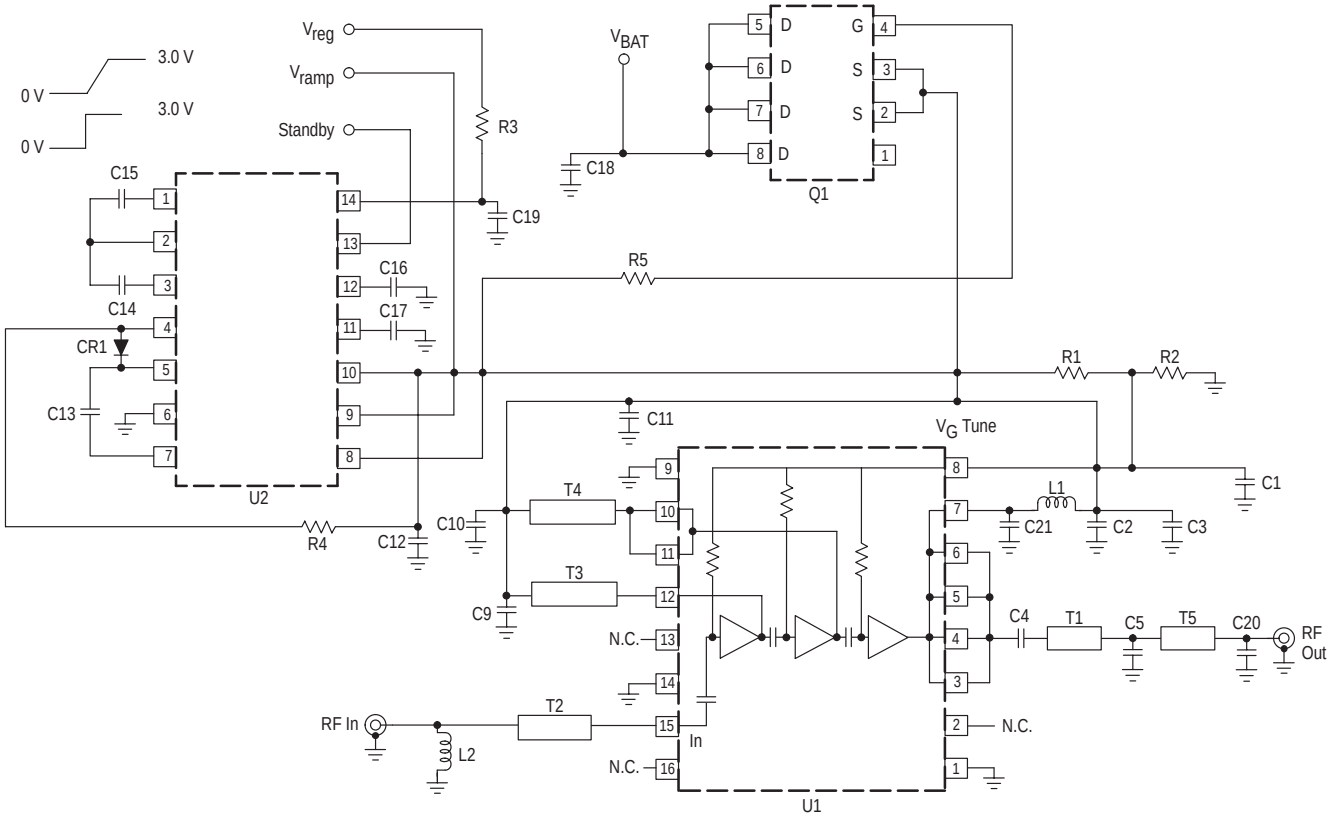
Figure 1. Reference Circuit Configuration



C1	1 nF	L1	18 nH, Coilcraft or 20 mm 50 Ω Microstrip Line	T2	6 mm 50 Ω Microstrip Line
C2, C6, C8	22 pF, NPO/COG			T3	5 mm 40 Ω Microstrip Line
C3, C7, C9	47 nF	L2	1.8 nH, Toko 2012	T4	1 mm 40 Ω Microstrip Line
C4	5.6 pF, AVX0603 ACCUF	R1	2.7 KΩ	T5	5.5 mm 50 Ω Microstrip Line
C5	3.9 pF, AVX0603 ACCUF	R2	2.2 KΩ	Board Material: Glass/Epoxy, ε_r = 4.45, Thickness = 0.5 mm	
C10, C11	1 pf	T1	2.5 mm 50 Ω Microstrip Line		

NOTE: For PCS 1900 tuning the following values are changed.
C5 = 2.7 pF, AVX0603 ACCUF
L2 = 1.5 nH, Toko 2012
T3 = 1 mm 50 Ω Microstrip Line

Figure 2. DCS1800/PCS1900 Applications Circuit Configuration



C1	6.8 nF	C20, C21	1.0 pF	R4	100 Ω
C2, C9,		CR1	MMBD701LT1	R5	470 Ω
C10	22 pF, 0603 NPO/COG	L1	18 nH, Coilcraft or 20 mm	T1	0.5 mm 30 Ω Microstrip Line
C3, C11	47 nF		50 Ω Microstrip Line	T2	5.0 mm 50 Ω Microstrip Line
C4	5.6 pF, AVX0603 ACCUF	L2	1.8 nH, Toko 2012	T3	8.0 mm 50 Ω Microstrip Line
C5	3.9 pF, AVX0603 ACCUF	Q1	MMSF4N01HD	T4	1.0 mm 50 Ω Microstrip Line
C12	220 nF	R1	2.7 kΩ	T5	5.5 mm 50 Ω Microstrip Line
C13, C16,		R2	3.0 kΩ	U1	MRFIC1817
C17, C19	1.0 µF	R3	22 Ω	U2	MC33169 (–4 V Version)
C14, C15	1.0 µF			Board Material: Glass/Epoxy, ε_r = 4.45, Thickness = 0.5 mm	
C18	1.0 µF				

NOTE: For PCS1900 applications, the following component values are changed:
L2 = 1.5 nH Toko 2012
C4 = 6.8 pF, AVX0603 ACCUF
C5 = 2.7 pF, AVX0603 ACCUF
C20 = Not Used
T1 = 0.5 mm 50 Ω Microstrip Line
T2 = 5.0 mm 50 Ω Microstrip Line
T3 = 1.0 mm 40 Ω Microstrip Line

TYPICAL CHARACTERISTICS

Figure 3. Output Power versus Frequency

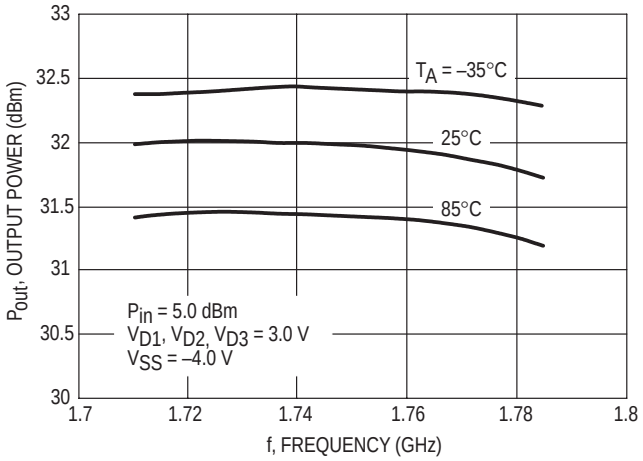


Figure 4. Power Added Efficiency versus Frequency

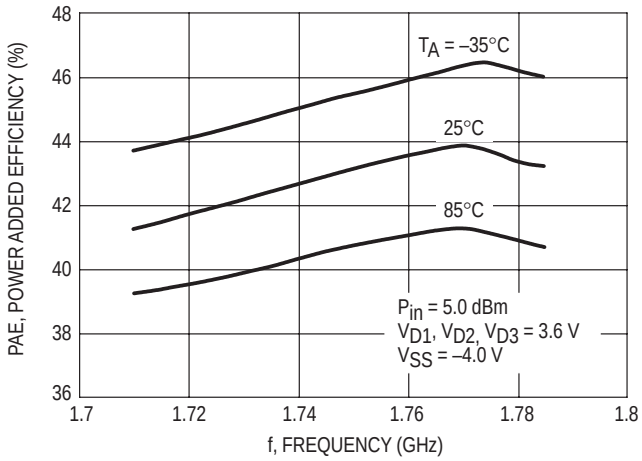


Figure 5. Output Power versus Frequency

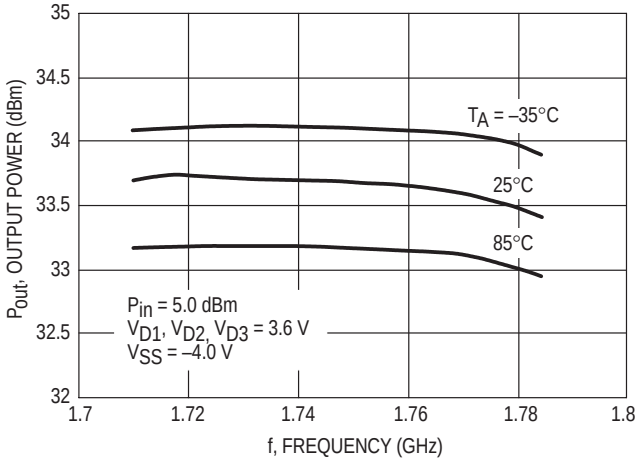


Figure 6. Power Added Efficiency versus Frequency

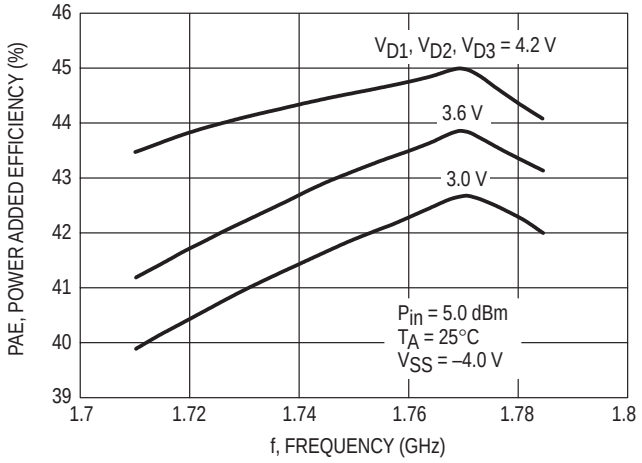


Figure 7. Output Power versus Frequency

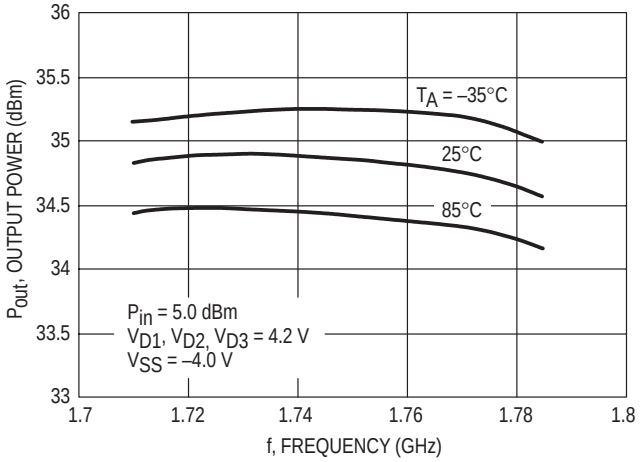
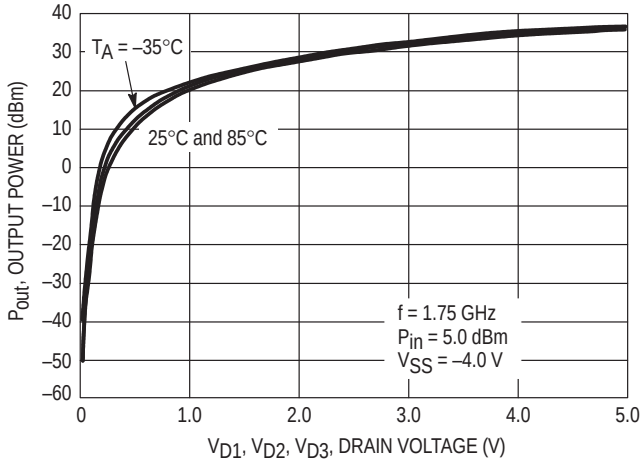


Figure 8. Output Power versus Drain Voltage



TYPICAL CHARACTERISTICS

Figure 9. Power Added Efficiency versus Drain Voltage

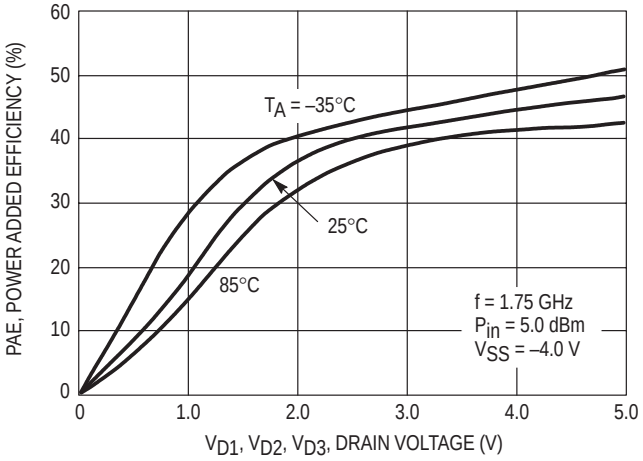


Figure 10. Output Power versus Input Power

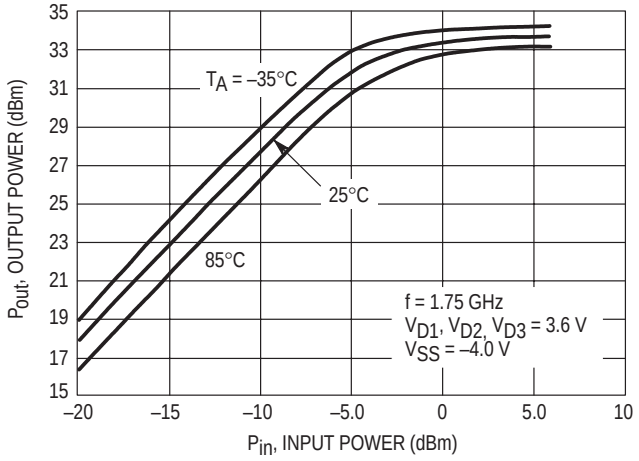


Figure 11. Power Added Efficiency versus Input Power

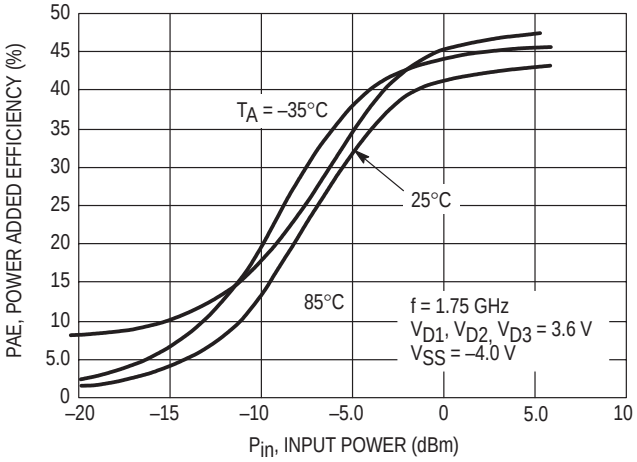


Figure 12. Second Harmonic versus Drain Voltage

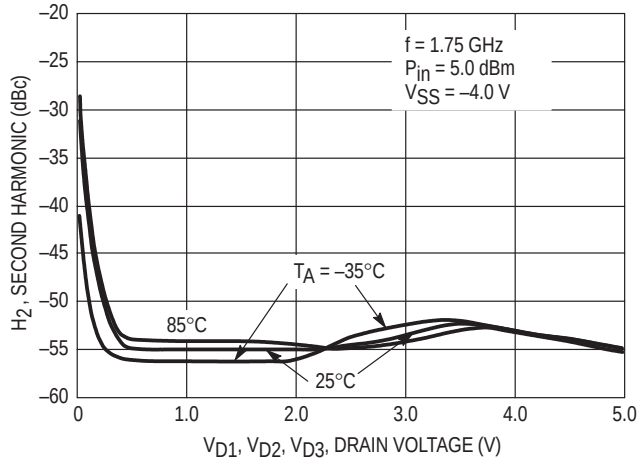


Figure 13. Third Harmonic versus Drain Voltage

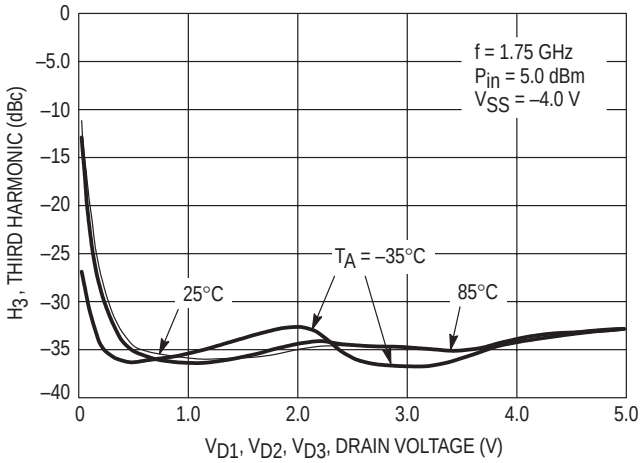
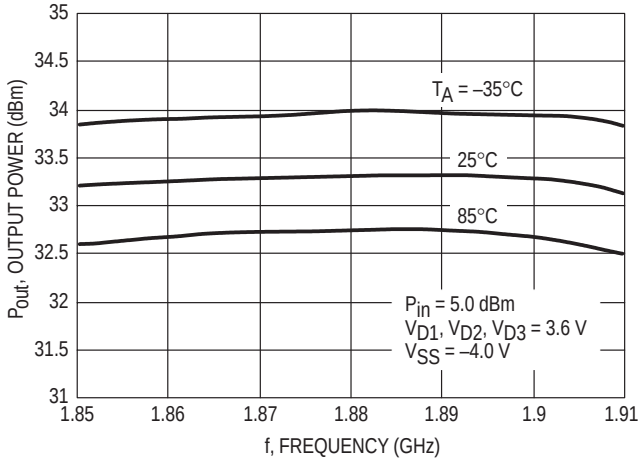


Figure 14. Output Power versus Frequency – PCS Band



Typical Characteristics

Figure 15. Power Added Efficiency versus Frequency – PCS Band

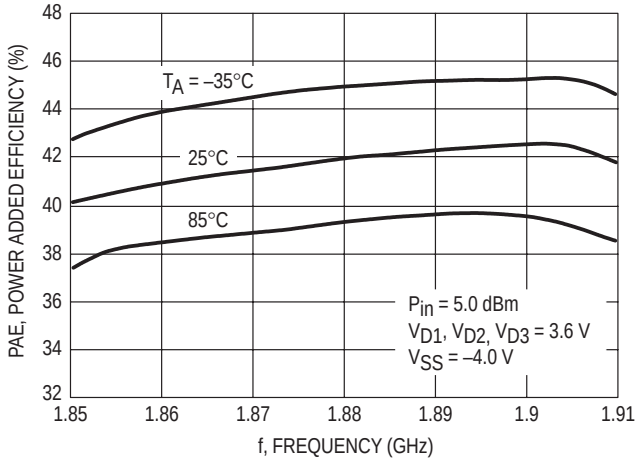


Table 1. Optimum Loads Derived from Circuit Characterization

f	Z_{in} OHMS		Z_{OL}* OHMS	
MHz	R	jX	R	jX
1710	7.77	–34.15	4.89	9.50
1720	7.84	–34.37	4.87	9.34
1730	7.87	–34.67	4.86	9.18
1740	8.07	–34.79	4.78	8.94
1750	8.24	–35.05	4.77	8.70
1760	8.39	–35.22	4.73	8.51
1770	8.44	–35.56	4.70	8.32
1780	8.52	–35.79	4.67	8.12
1785	8.57	–35.82	4.65	7.95

Z_{in} represents the input impedance of the device.
Z_{OL}* represents the conjugate of the optimum output load to present to the device.

Table 2. Optimum Loads Derived from Circuit Characterization – PCS Band

f	Z_{in} OHMS		Z_{OL}* OHMS	
MHz	R	jX	R	jX
1850	3.97	–39.68	7.49	3.07
1860	3.94	–40.31	7.42	2.81
1870	4.09	–40.65	7.38	2.51
1880	4.04	–40.92	7.31	2.28
1890	4.18	–41.21	7.28	2.02
1900	4.27	–41.48	7.28	1.73
1910	4.26	–41.71	7.23	1.56

Z_{in} represents the input impedance of the device.
Z_{OL}* represents the conjugate of the optimum output load to present to the device.

APPLICATIONS INFORMATION

Design Philosophy

The MRFIC1817 is a 3–stage integrated power amplifier designed for use in cellular phones, especially for those used in DCS1800 (PCN) 3.6 V operation. With matching circuit modifications, it is also applicable for use in DCS1900 (PCS) equipment. Due to the fact that the input, output and some of the interstage matching is accomplished off–chip, the device can be tuned to operate anywhere within the 1500 to 2000 MHz frequency range. Typical performance at different battery voltages is:

- 33.5 dBm @ 3.6 V
- 32.0 dBm @ 3 V

This capability makes the MRFIC1817 suitable for portable cellular applications such as:

- 3 V and 3.6 V DCS1800 Class I and II
- 3 V and 3.6 V PCS tag5

RF Circuit Considerations

The MRFIC1817 can be tuned by changing the values and/or positions of the appropriate external components. Refer to Figure 2, a typical DCS1800 Class I applications circuit. The input match is a shunt–L, series–C, high–pass structure and can be retuned as desired with the only limitation being the on–chip 6 pF blocking capacitor. For saturated applications such as DCS1800 and PCS1900, the input match should be optimized at the rated RF input power. Interstage matching can be optimized by changing the value and/or position of the decoupling capacitor on the V_{D1} and V_{D2} supply lines. Moving the capacitor closer to the device or reducing the value increases the frequency of resonance with the inductance of the device's wirebonds and leadframe pin. Output matching is accomplished with a low–pass network as a compromise between bandwidth and harmonic rejection. Implementation is through high Q capacitors mounted along a 50 Ω microstrip transmission line. Values and positions are chosen to present a 2 W loadline to the device while conjugating the device output parasitics. The network must also properly terminate the second and third harmonics to optimize efficiency and reduce harmonic output. All components used in this application are low–Q commercial chip capacitors, except for the output load line. Loss in circuit traces must also be considered. The output transmission line and the bias supply lines should be at least 0.6 mm in width to accommodate the peak circulating currents which can be as high as 2 amperes under worst case conditions. The bias supply line which supplies the output should include an RF choke of at least 18 nH, surface mount solenoid inductors or quarter wave microstrip lines. Discrete inductors will usually give better efficiency and conserve board space.

Biasing Considerations

Gate bias lines are tied together and connected to the V_{SS} voltage, allowing gate biasing through use of external resistors or positive voltages. This allows setting the quiescent current of all stage in the same time while saving some board space. For applications where the amplifier is operated close to saturation, such as with TDMA amplifiers, the gate bias can be set with resistors. Variations in process and tempera–ture will not affect amplifier performance significantly in these applications. The values shown in the Figure 1 will set quiescent currents of 20 to 40 mA for the first stage, 150 to 300 mA for the second stage, and 400 to 800 mA for the final stage. For linear modes of operation which are required for CDMA amplifiers, the quiescent current must be more carefully controlled. For these applications, the V_G pins can be referenced to some tunable voltage which is set at the time of radio manufacturing. Less than 1 mA is required in the divider network so a DAC can be used as the voltage source.

Power Control Using the MC33169

The MC33169 is a dedicated GaAs power amplifier support IC which provides the –4 V required for V_{SS}, an N–MOS drain switch interface and driver and power supply sequencing. The MC33169 can be used for power control in applications where the amplifier is operated in saturation since the output power in non–linear operation is proportional to V_{D2}. This provides a very linear and repeatable power control transfer function. This technique can be used open loop to achieve 40–45 dB dynamic range over process and temperature variation. With careful design and selection of calibration points, this technique can be used for DCS1800 control where 30 dB dynamic range is required, eliminating the need for the complexity and cost of closed–loop control. The transmit waveform ramping function required for systems such as DCS1800 can be implemented with a simple Sallen and Key filter on the MC33169 control loop. The amplifier is then ramped on as the V_{RAMP} pin is taken from 0 V to 3 V. To implement the different power steps required for DCS1800, the V_{RAMP} pin is ramped between 0 V and the appropriate voltage between 0 V and 3 V for the desired output power. For closed–loop configurations using the MC33169, MMSF4N01HD N–MOS switch and the MRFIC1817 provide a typical 1 MHz 3 dB loop bandwidth. The STANDBY pin must be enabled (3 V) at least 800 μs before the V_{RAMP} pin goes high and disabled (0 V) at least 20 ms before the V_{RAMP} pin goes low. This STANDBY function allows for the enabling of the MC33169 one burst before the active burst thus reducing power consumption.

Conclusion

The MRFIC1817 offers the flexibility in matching circuitry and gate biasing required for portable cellular applications. Together with the MC33169 support IC, the device offers an efficient system solution for TDMA applications such as DCS1800 where saturated amplifier operation is used.

For more information about the power control using the MC33169, refer to application note AN1599, "Power Control with the MRFIC0913 GaAs Integrated Power Amplifier and MC33169 Support IC."

Evaluation Boards

Two versions of the MRFIC1817 evaluation board are available. Order MRFIC1817DCSTF for the 1.8 GHz version and order MRFIC1817PCSTF for the 1.9 GHz version. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

MOTOROLA

MRFIC1818

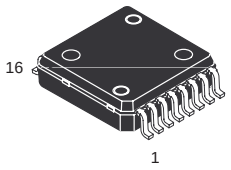
1800 MHz GaAs Integrated Power Amplifier

Designed specifically for application in Pan European digital 1.0 watt DCS1800 handheld radios, the MRFIC1818 is specified for 33 dBm output power with power gain over 30 dB from a 4.8 V supply. With minor tuning changes, the MRFIC1818 can be used for PCS1900 as well as PCS CDMA. To achieve this superior performance, Motorola's planar GaAs MESFET process is employed. The device is packaged in the PFP–16 Power Flat Package which gives excellent thermal and electrical performance through a solderable backside contact while allowing the convenience and cost benefits of reflow soldering.

- Minimum Output Power Capabilities
  - 33 dBm @ 4.8 V
  - 32 dBm @ 4.0 V
- Specified 4.8 V Characteristics
  - RF Input Power = 3.0 dBm
  - RF Output Power = 33 dBm
  - Minimum PAE = 35%
- Low Current required from Negative Supply – 2.0 mA max
- Guaranteed Stability and Ruggedness
- Device Marking = M1818

1700 – 1900 MHz MMIC DCS1800/PCS1900 INTEGRATED POWER AMPLIFIER

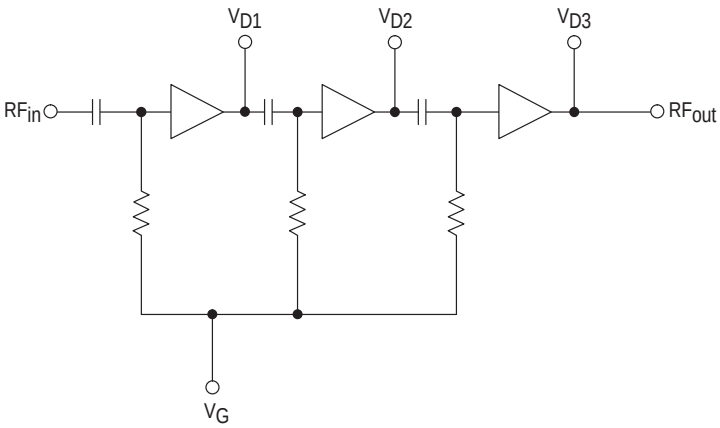
SEMICONDUCTOR TECHNICAL DATA



(Scale 2:1)

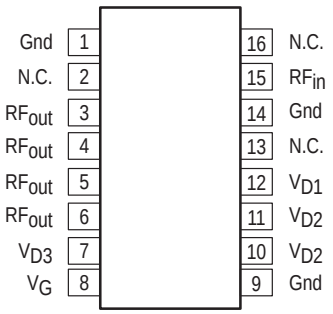
PLASTIC PACKAGE
CASE 978
(PFP–16, Tape & Reel Only)

Simplified Block Diagram



This device contains 3 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temp Range	Package
MRFIC1818R2	T_C = –40 to 85°C	PFP–16 Tape & Reel*

*1,500 units per 16 mm, 13 inch reel.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Positive Supply Voltage	$V_{D1, 2, 3}$	7.5	Vdc
DC Negative Supply Voltage	V_{SS}	–5.0	Vdc
RF Input Power	P_{in}	10	dBm
RF Output Power	P_{out}	36	dBm
Operating Case Temoperature Range	T_C	–40 to 85	°C
Storage Temperature Range	T_{stg}	–55 to 150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W

NOTE: ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{D1, 2, 3}$	2.7	–	6.0	Vdc
Gate Voltage	V_{SS}	–3.5	–	–4.5	Vdc
RF Frequency Range	f_{RF}	1700	–	1900	MHz
RF Input Power	P_{RF}	0	–	6.0	dBm

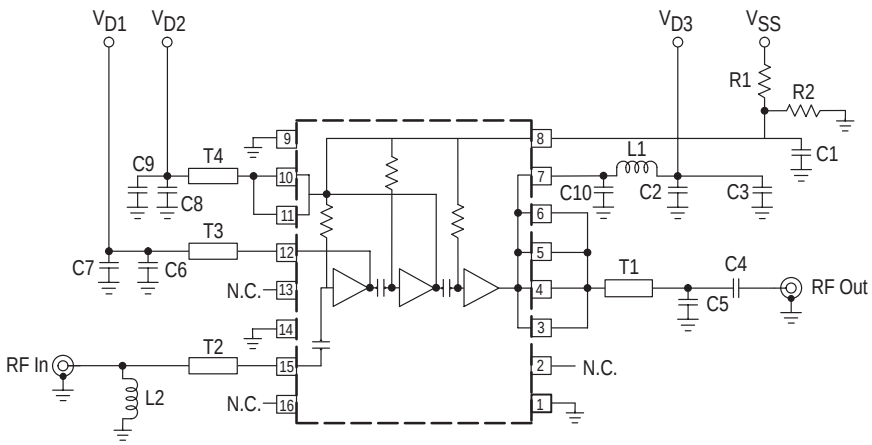
ELECTRICAL CHARACTERISTICS

($V_{D1, 2, 3}$ = 4.8 V, V_{SS} = –4.0 V, P_{in} = 3.0 dBm, Peak measurement at 12.5% duty cycle, 4.6 ms Period, T_A = 25°C, unless otherwise noted. Measured in reference circuit shown in Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range		1710	–	1785	MHz
Output Power		33	34.5	–	dBm
Power Added Efficiency		35	42	–	%
Output Power (Tuned for PCS Band, 1850 to 1910 MHz)		–	34.5	–	dBm
Power Added Efficiency (Tuned for PCS Band, 1850 to 1910 MHz)		–	42	–	%
Input VSWR		–	2:1	–	VSWR
Harmonic Output (2nd and 3rd)		–	–35	–30	dBc
Output Power at low voltage (V_{D1}, V_{D2}, V_{D3} = 4.0 V)			33	–	dBm
Output Power, Isolation (V_{D1}, V_{D2}, V_{D3} = 0 V)		–	–40	–35	dBm
Noise Power (in 100 kHz, 1805 to 1880 MHz)		–	–85	–80	dBm
Stability–Spurious Output (P_{in} = 5.0 dBm, P_{out} = 0 to 33 dBm, Load VSWR 6:1 at any Phase Angle, Source VSWR = 3:1, at any Phase Angle) [Note]		–	–	–60	dBc
Load Mismatch Stress (P_{out} = 5.0 to 35 dBm, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust $V_{D1, 2\&3}$ for specified power)		No Degradation in Output Power After Returning to Standard Conditions			
3.0 dB V_{DD} Bandwidth		–	2.0	–	MHz
Negative Supply Current		–	0.7	2.0	mA

NOTE: Adjust $V_{D1, 2, 3}$ (0 to 4.8 V) for specified P_{out}; Duty Cycle = 12.5%, Period = 4.6 ms.

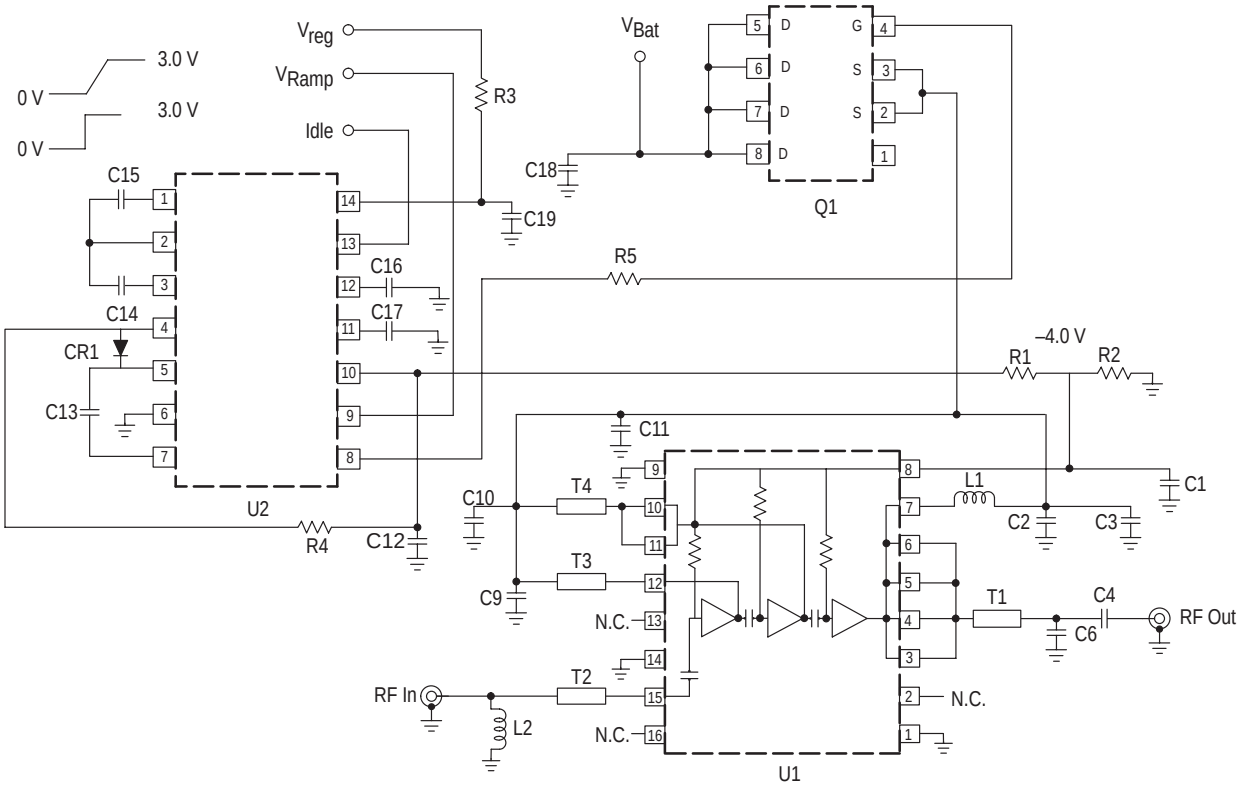
Figure 1. Reference Circuit Configuration



C1	6.8 nF	C5	3.9 pF, NPO/COG	T1	1.4 mm 25 Ω Microstrip Line
C2, C6, C8	22 pF, NPO/COG	L1	18 nH, Coilcraft	T2	5.0 mm 50 Ω Microstrip Line
C3, C7, C9	47 nF	L2	1.8 nH, Toko 2012	T3	4.0 mm 50 Ω Microstrip Line
C4	27 pF, NPO/COG	R1, R2 = 2.7 KΩ		T4	0.5 mm 50 Ω Microstrip Line
C10	0.5 pF			Board Material: Glass/Epoxy, ε_r = 4.45, Thickness = 0.5 mm	

NOTE: For PCS/DCS1900 applications,
the following components are used.
C5 = 2.7 pF, 0603 NPO/COG
L2 = 1.5 nH, Toko 2012
T3 = 1.0 mm 50 Ω Microstrip Line

Figure 2. DCS1800 Applications Circuit Configuration



C1 6.8 nF
C2, C9, C10 22 pF, 0603 NPO/COG
C3, C11 47 nF
C4 27 pF, 0603 NPO/COG
C6 3.9 pF, 0603 NPO/COG
C12 220 nF
C13, C16, C17, C19 1.0 μF
C14, C15 1.0 μF
C18 1.0 μF
CR1 MMBD701LT1
L1 18 nH, Coilcraft or 20 mm 50 Ω Microstrip Line
L2 1.8 nH, Toko 2012 or 5.0 mm 50 Ω Line
Q1 MMSF4N01HD
R1, R2 2.7 kΩ
R3, R4 100 Ω
R5 470 Ω
T1 2.0 mm 25 Ω Microstrip Line
T2 5.0 mm 50 Ω Microstrip Line
T3 8.0 mm 40 Ω Microstrip Line
T4 1.0 mm 40 Ω Microstrip Line
U1 MRFIC1818
U2 MC33169 (–4.0 V Version)
Board Material: Glass/Epoxy, ε_r = 4.45, Thickness = 0.5 mm

NOTE: For PCS/DCS1900 applications, the following component values are changed:
C6 = 2.7 pF, 0603 NPO/COG
L2 = 1.5 nH, Toko 2012
T3 = 1.0 mm 50 Ω Microstrip Line

TYPICAL CHARACTERISTICS

Figure 3. Output Power versus Frequency

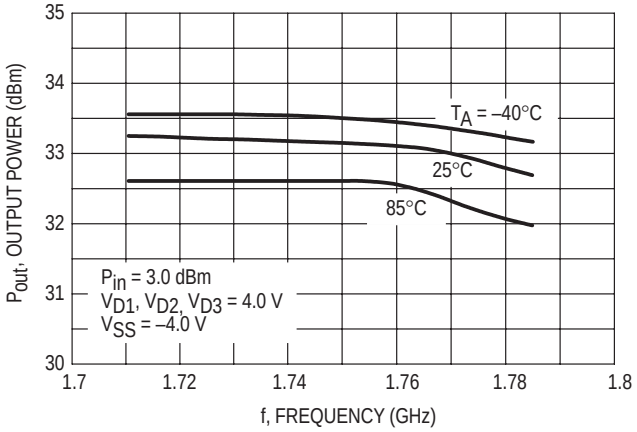


Figure 4. Power Added Efficiency versus Frequency

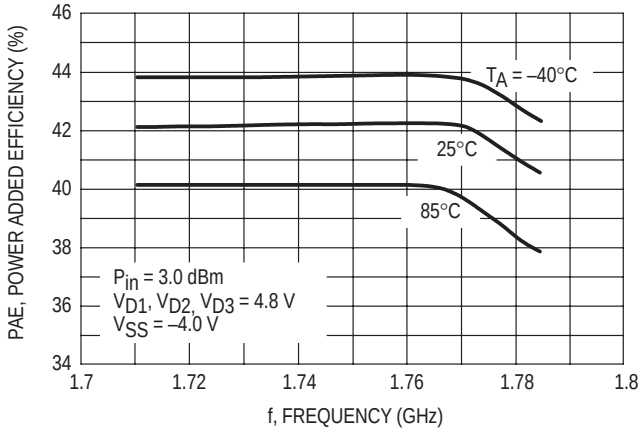


Figure 5. Output Power versus Frequency

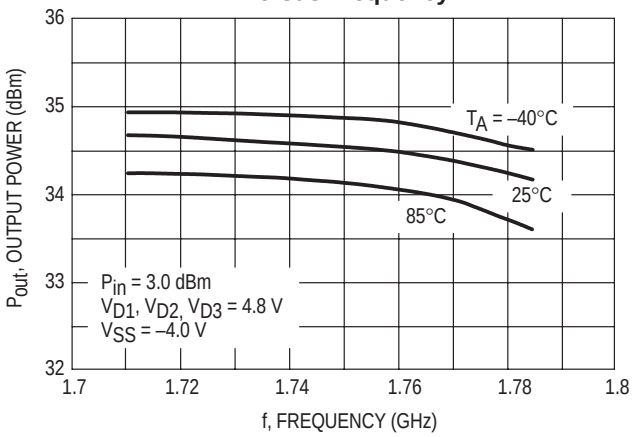


Figure 6. Power Added Efficiency versus Frequency

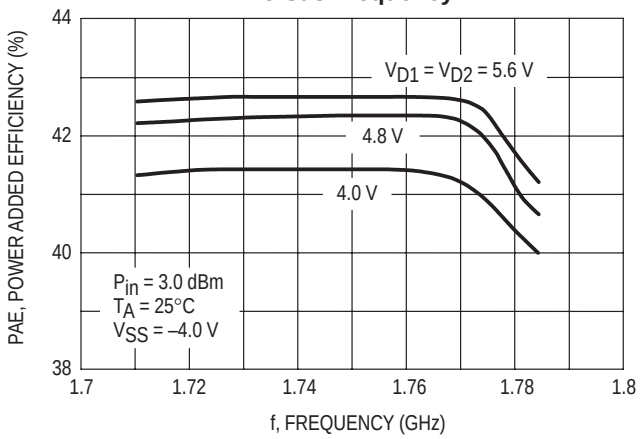


Figure 7. Output Power versus Frequency

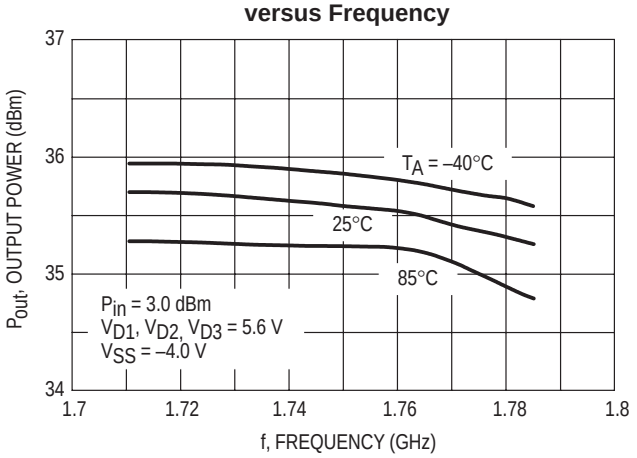
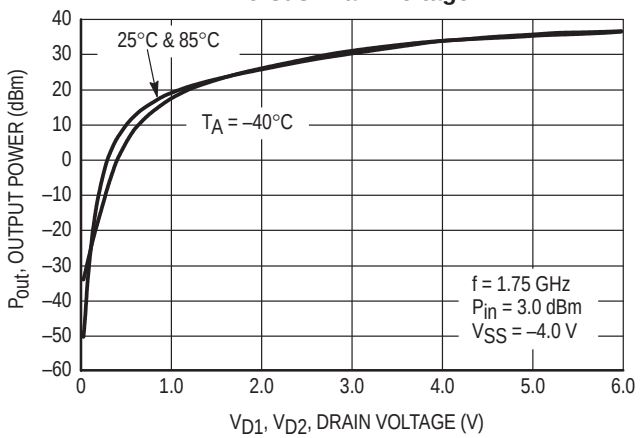


Figure 8. Output Power versus Drain Voltage



TYPICAL CHARACTERISTICS

Figure 9. Power Added Efficiency versus Drain Voltage

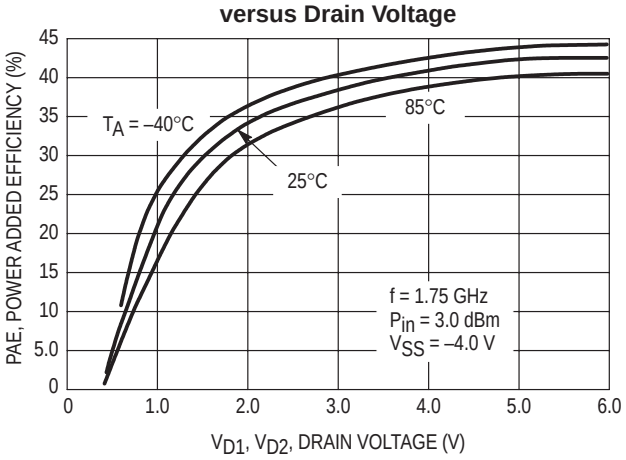


Figure 10. Output Power versus Input Power

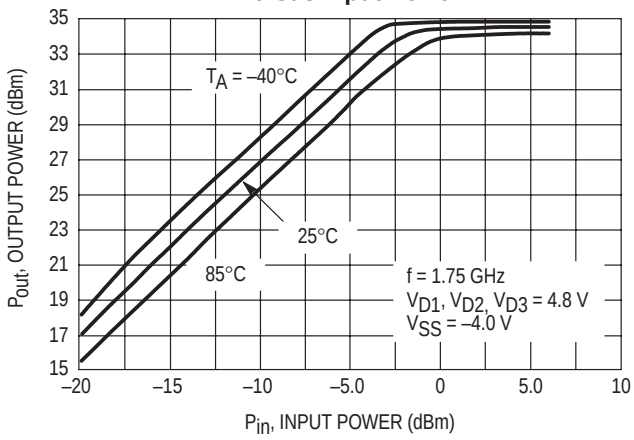


Figure 11. Power Added Efficiency versus Input Power

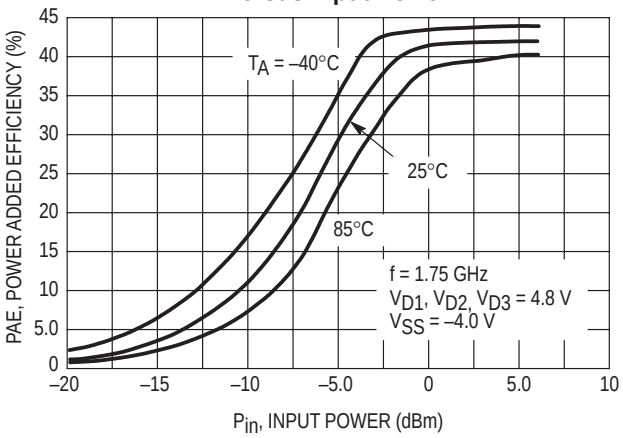


Figure 12. Second Harmonic versus Drain Voltage

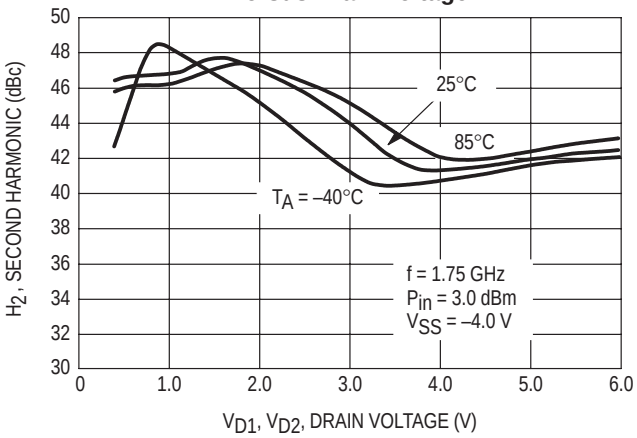


Figure 13. Third Harmonic versus Drain Voltage

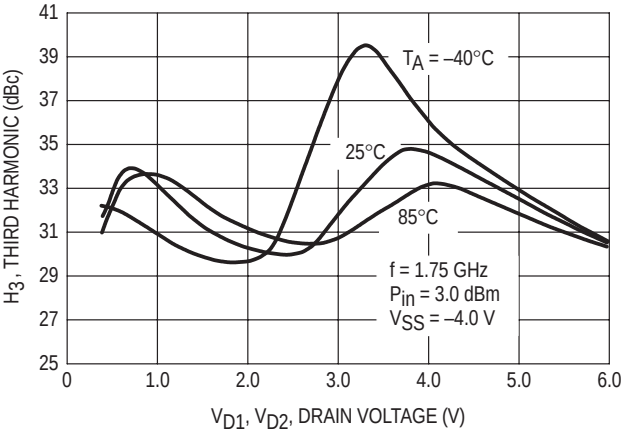
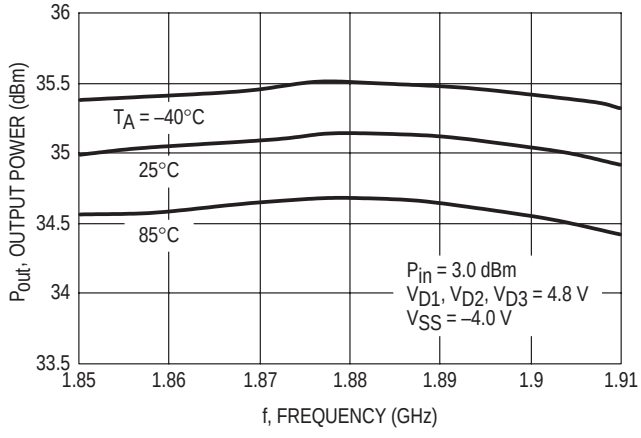


Figure 14. Output Power versus Frequency – PCS Band



TYPICAL CHARACTERISTICS

Figure 15. Power Added Efficiency versus Frequency – PCS Band

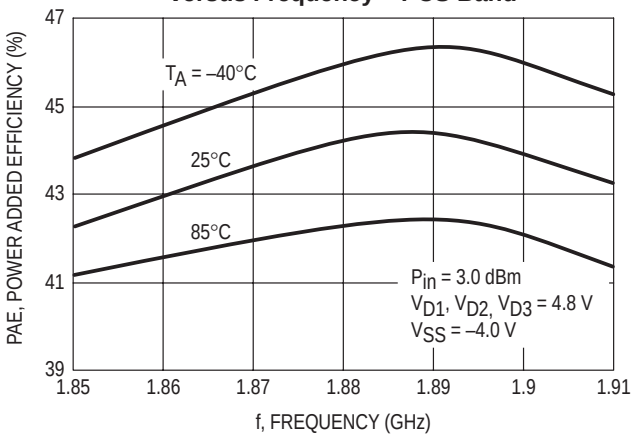


Figure 16. CDMA ACPR at 885 kHz Offset versus Output Power

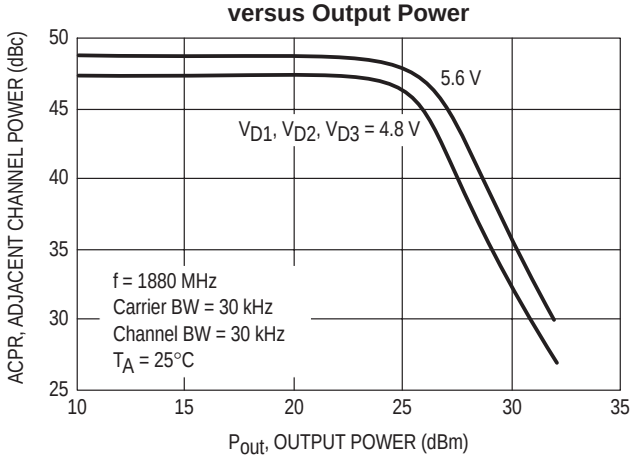


Figure 17. CDMA ACPR at 1980 kHz Offset versus Output Power

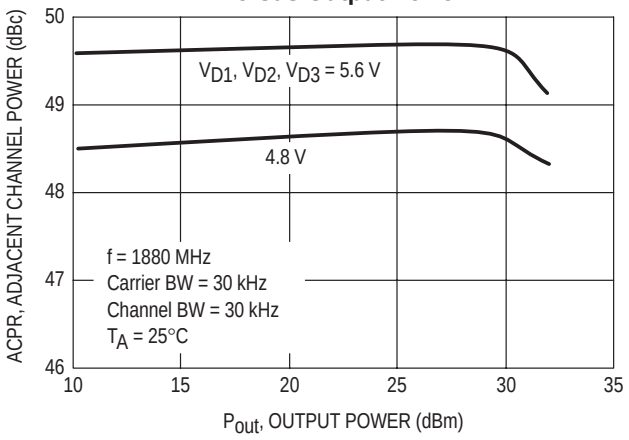


Table 1. Optimum Loads Derived from Circuit Characterization

f MHz	Z_{in} OHMS		Z_{OL}* OHMS	
	R	jX	R	jX
1710	9.19	–30.10	6.00	3.80
1720	9.35	–29.60	5.96	3.71
1730	9.50	–29.30	5.88	3.60
1740	9.65	–29.10	5.80	3.46
1750	9.60	–29.00	5.75	3.33
1760	9.42	–28.79	5.67	3.20
1770	9.11	–28.60	5.60	3.07
1780	8.77	–28.30	5.51	2.93
1785	8.54	–28.15	5.45	2.79

Z_{in} represents the input impedance of the device.
Z_{OL}* represents the conjugate of the optimum output load to present to the device.

Table 2. Optimum Loads Derived from Circuit Characterization – PCS Board

f MHz	Z_{in} OHMS		Z_{OL}* OHMS	
	R	jX	R	jX
1850	3.92	–43.30	7.70	0.39
1860	4.01	–43.56	7.64	0.23
1870	4.08	–43.78	7.57	0.15
1880	4.19	–44.00	7.51	0.07
1890	4.29	–44.29	7.50	–0.04
1900	4.31	–44.49	7.44	–0.06
1910	4.37	–44.81	7.35	–0.19

Z_{in} represents the input impedance of the device.
Z_{OL}* represents the conjugate of the optimum output load to present to the device.

APPLICATIONS INFORMATION

Design Philosophy

The MRFIC1818 is a 3–stage Integrated Power Amplifier designed for use in cellular phones, especially for those used in DCS1800 (PCN) 4.8 V operation. With matching circuit modifications, it is also applicable for use in DCS1900 (PCS) equipment. Due to the fact that the input, output and some of the interstage matching is accomplished off chip, the device can be tuned to operate anywhere within the 1500 to 2000 MHz frequency range. Typical performance at different battery voltages is:

- 36 dBm @ 6.0 V
- 34.5 dBm @ 4.8 V
- 32.0 dBm @ 3.6 V

This capability makes the MRFIC1818 suitable for portable cellular applications such as:

- 6V and 4.8 V DCS1800 Class I
- 6V and 4.8 V PCS tag5
- 3.6 V DCS1800 Class II

RF Circuit Considerations

The MRFIC1818 can be tuned by changing the values and/or positions of the appropriate external components. Refer to Figure 2, a typical DCS1800 Class I applications circuit. The input match is a shunt–L, series–C, High–pass structure and can be retuned as desired with the only limitation being the on–chip 6.0 pF blocking capacitor. For saturated applications such as DCS1800 and DCS1900, the input match should be optimized at the rated RF input power. Interstage matching can be optimized by changing the value and/or position of the decoupling capacitor on the V_{D1} and V_{D2} supply lines. Moving the capacitor closer to the device or reducing the value increases the frequency of resonance with the in–ductance of the device's wirebonds and leadframe pin. Output matching is accomplished with a one–stage low– pass network as a compromise between bandwidth and harmonic rejection. Implementation is through chip capacitors mounted along a 30 or 50 Ω microstrip transmission line. Values and positions are chosen to present a 2.5 W loadline to the device while conjugating the device output parasitics. The network must also properly terminate the second and third harmonics to optimize efficiency and reduce harmonic output. Low–Q commercial chip capacitors are used for the shunt capacitors, as shown in Figure 2. Loss in circuit traces must also be considered. The output transmission line and the bias supply lines should be at least 0.6 mm in width to accommodate the peak circulating currents which can be as high as 2.0 amperes under worst case conditions. The bias supply line which supplies the output should include an RF choke of at least 18 nH, surface mount solenoid inductors or quarter wave microstrip lines. Discrete inductors will usually give better efficiency and conserve board space. The dc blocking capacitor required at the output of the device is best mounted at the 50 Ω impedance point in the circuit where the RF current is at a minimum and the capacitor loss will have less effect.

Biasing Considerations

Gate bias lines are tied together and connected to the V_{SS} voltage, allowing gate biasing through use of external resistors or positive voltages. This allows setting the quiescent current of all stage in the same time while saving some board space. For applications where the amplifier is operated close to saturation, such as TDMA amplifiers, the gate bias can be set with resistors. Variations in process and tempera–ture will not affect amplifier performance significantly in these applications. The values shown in the Figure 1 will set quies–cent currents of 20 to 40 mA for the first stage, 150 to 300 for the second stage and 400 to 800 mA for the final stage. For linear modes of operation which are required for CDMA amplifiers, the quiescent current must be more carefully controlled. For these applications, the V_G pins can be referenced to some tunable voltage which is set at the time of radio manufacturing. Less than 1.0 mA is required in the divider network so a DAC can be used as the voltage source.

Power Control Using the MC33169

The MC33169 is a dedicated GaAs power amplifier support IC which provides the –4.0 V required for V_{SS}, an N–MOS drain switch interface and driver and power supply sequencing. The MC33169 can be used for power control in applications where the amplifier is operated in saturation since the output power in non–linear operation is proportional to V_{D2}. This provides a very linear and repeatable power control transfer function. This technique can be used open loop to achieve 40 to 45 dB dynamic range over process and temperature variation. With careful design and selection of calibration points, this technique can be used for DCS1800 control where 30 dB dynamic range is required, eliminating the need for the complexity and cost of closed–loop control. The transmit waveform ramping function required for systems such as DCS1800 can be implemented with a simple Sallen and Key filter on the MC33169 control loop. The amplifier is then ramped on as the V_{Ramp} pin is taken from 0 V to 3.0 V. To implement the different power steps required for DCS1800, the V_{Ramp} pin is ramped between 0 V and the appropriate voltage between 0 V and 3.0 V for the desired output power. For closed–loop configurations using the MC33169, MMSF4N01HD N–MOS switch and the MRFIC1818 provide a typical 1.0 MHz 3.0 dB loop bandwidth. The STANDBY pin must be enabled (3.0 V) at least 800 μs before the V_{Ramp} pin goes high and disabled (0 V) at least 20 μs before the V_{Ramp} pin goes low. This STANDBY function allows for the enabling of the MC33169 one burst before the active burst thus reducing power consumption.

Conclusion

The MRFIC1818 offers the flexibility in matching circuitry and gate biasing required for portable cellular applications. Together with the MC33169 support IC, the device offers an efficient system solution for TDMA applications such as DCS1800 where saturated amplifier operation is used.

For more information about the power control using the MC33169, refer to application note AN1599, "Power Control with the MRFIC0913 GaAs Integrated Power Amplifier and MC33169 Support IC."

Evaluation Boards

Two versions of the MRFIC1818 evaluation board are available. Order MRFIC1818DCSTF for the 1.8 GHz version and order MRFIC1818PCSTF for the 1.9 GHz version. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

MOTOROLA

MRFIC1819

Advance Information

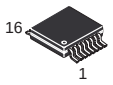
3.6 V 1800 MHz GaAs Integrated Power Amplifier

The MRFIC1819 is a single supply, RF power amplifier designed for the 1W DCS1800/PCS1900 handheld radio. The negative power supply is generated inside the chip using RF rectification, which avoids any spurious signal. A built in priority switch is provided to prevent Drain Voltage being applied on the RF lineup if not properly biased by the Negative Voltage. The device is packaged in the TSSOP–16EP package, with exposed backside pad, which allows excellent electrical and thermal performance through a solderable contact.

- Target 3.6 V Characteristics:
  - RF Input Power: 6.0 dBm
  - RF Output Power: 33 dBm Typical
  - Efficiency: 41% Typical
- Single Positive Supply Solution
- Negative Voltage Generator
- Positive Step–Up Voltage Generator
- V_{SS} Check Switch for Gate–Drain Priority

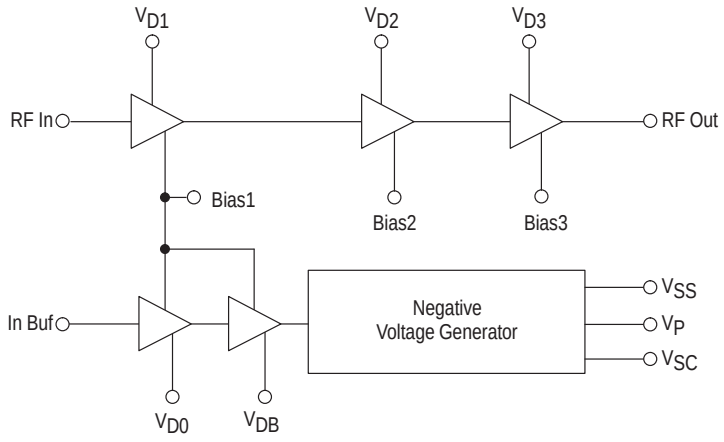
INTEGRATED RF POWER AMPLIFIER DCS1800/PCS1900

SEMICONDUCTOR TECHNICAL DATA



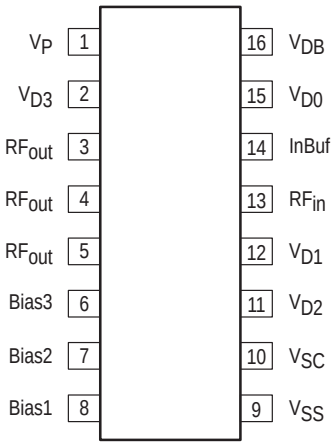
PLASTIC PACKAGE
CASE 948L
(TSSOP–16EP, Tape and Reel Only)

Simplified Block Diagram



This device contains 9 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temp Range	Package
MRFIC1819R2	T_A = –40 to 85°C	TSSOP–16EP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	$V_{D1, 2, 3}$	6.0	V
RF Input Power	P_{in}	12	dBm
RF Output Power	P_{out}	36	dBm

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Contitions or Electrical Characteristics tables.
2. Meets Human Body Model (HBM) ≤250 V and Machine Model (MM) ≤60 V. This device is rated Moisture Sensitivity Level (MSL) 4. ESD data available upon request.
3. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{D0}, V_{DB}, $V_{D1, 2, 3}$	3.0	–	5.0	Vdc
Input Power	P_{in}	5.0	–	10	dBm
Input Frequency	f_{RF}	1700	–	1900	MHz
Operating Case Temperature Range	T_C	–40	–	85	°C
Storage Temperature Range	T_{stg}	–55	–	150	°C

ELECTRICAL CHARACTERISTICS ($V_{D0} = V_{DB} = 3.6$ V, $V_{D1, 2, 3} = 3.6$ V, $P_{in} = 6.0$ dBm, Peak measurement at 12.5% duty cycle, 4.6 ms Period, $T_A = 25°C$, unless otherwise noted.)

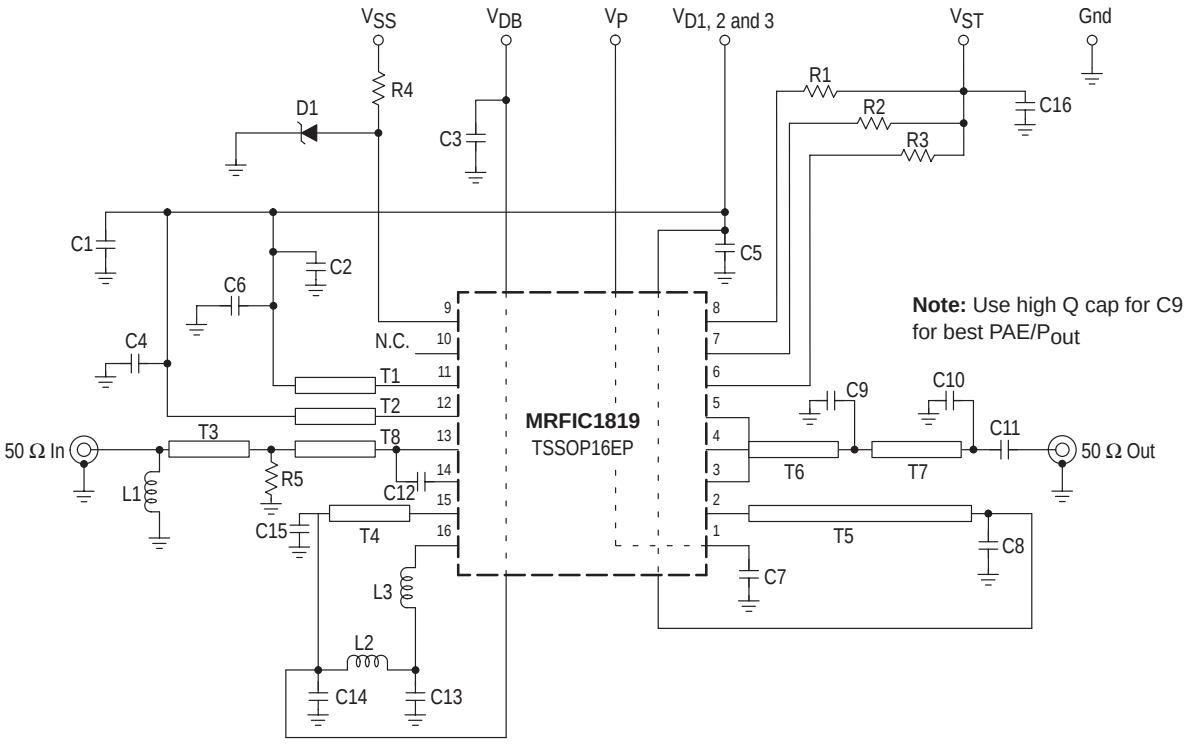
Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1710	–	1785	MHz
Output Power	P_{out}	32	33	–	dBm
Power Added Efficiency	PAE	35	41	–	%
Output Power (Tuned for PCS Band 1850 to 1910 MHz)	P_{out}	–	33	–	dBm
Power Added Efficiency (Tuned for PCS Band 1850 to 1910 MHz)	PAE	–	41	–	%
Output Power at low voltage ($V_{D0} = V_{DB} = 3.0$ V, $V_{D1, 2, 3} = 3.0$ V)	P_{out}	30.5	31	–	dBm
Harmonic Output $2f_0$ $3f_0$	–	 – –	 –45 –35	 –40 –30	dBc
Input Return Loss	|S11|	–	12	–	dB
Output Power Isolation ($P_{in} = 10$ dBm, $V_{D0} = V_{DB} = 3.0$ V, $V_{D1, 2\&3} = 0$ V)	P_{off}	–	–30	–	dBm
Noise Power (In 100 kHz, 1805 to 1880 MHz)		–	–90	–	dBm
Negative Voltage ($P_{in} = 6.0$ dBm, $V_{D0} = V_{DB} = 3.0$ V)	V_{SS}	–4.85	–	–	V
Negative Voltage Setting Time ($P_{in} = 6.0$ dBm, VD0 = V_{DB} stepped from 0 to 3.0 V)	T_S	–	0.7	–	µs
Positive Voltage ($P_{in} = 6.0$ dBm,$V_{D0} = V_{DB} = 3.0$ V)	V_P	5.7	6.6	–	V
Stability–Spurious Output ($P_{out} = 0$ to 33 dBm, Load VSWR 6:1 all phase angles, source VSWR = 3:1, at any phase angle, Adjust $V_{D1, 2\&3}$ for specified power)	P_{spur}	–	–	–60	dBc
Load Mismatch Stress ($P_{out} = 3$ to 33 dBm, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust $V_{D1, 2\&3}$ for specified power)	No Degradation in Output Power Before & After Test				

Table 1. Optimum Loads Derived from Circuit Characterization

f MHz	Z_{in} OHMS		Z_{OL}* OHMS	
	R	jX	R	jX
1710	14.51	–66.87	5.88	3.30
1720	14.67	–67.40	5.86	3.20
1730	14.82	–68.07	5.79	3.10
1740	15.08	–68.73	5.74	2.93
1750	15.30	–69.29	5.67	2.75
1760	15.55	–69.80	5.59	2.58
1770	15.80	–70.30	5.53	2.46
1780	16.00	–70.89	5.44	2.28
1790	16.16	–71.20	5.42	2.25

Z_{in} represents the input impedance of the device.
Z_{OL}* represents the conjugate of the optimum output load to present to the device.

Figure 1. Reference Circuit



C1,C2	47 nF	R4	1.0 kΩ
C3,C14	330 pF	R5	680 Ω
C4,C6,C8,C11,		L1	1.8 nH
C15,C16	22 pF	L2	33 nH
C5	10 nF	L3	2.7 nH
C7	2.7 pF	D1	Zener 5.1 V MMSZ4689T1
C9	3.9 pF AVX Accu–F	T1, T2	60 Ω Microstrip Line, L = 3.0 mm
C10	1.0 pF	T3	50 Ω Microstrip Line, L = 4.5 mm
C12	0.8 pF	T4	80 Ω Microstrip Line, L = 4.0 mm
C13	47 pF	T5	50 Ω Microstrip Line, L = 17 mm
R1,R2	15 kΩ	T6,T7	30 Ω Microstrip Line, L = 1.0 mm
R3	7.5 kΩ	T8	50 Ω Microstrip Line, L = 2.5 mm

Figure 2. 3.6 V DCS Application Circuit

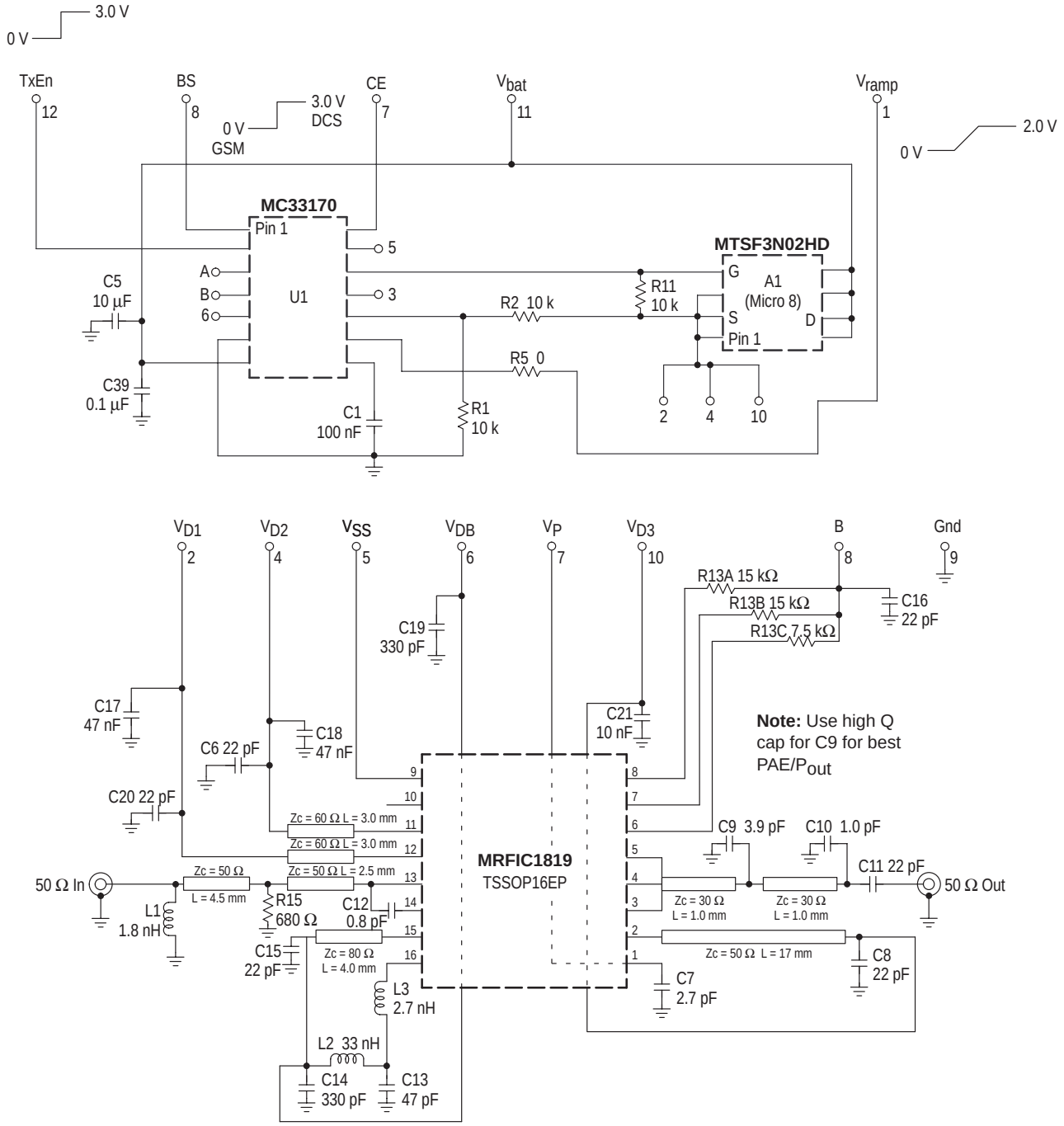


Figure 3. 3.6 V GSM & DCS IPA Dual–Band Application Circuit with Companion Chip & NMOS Switch

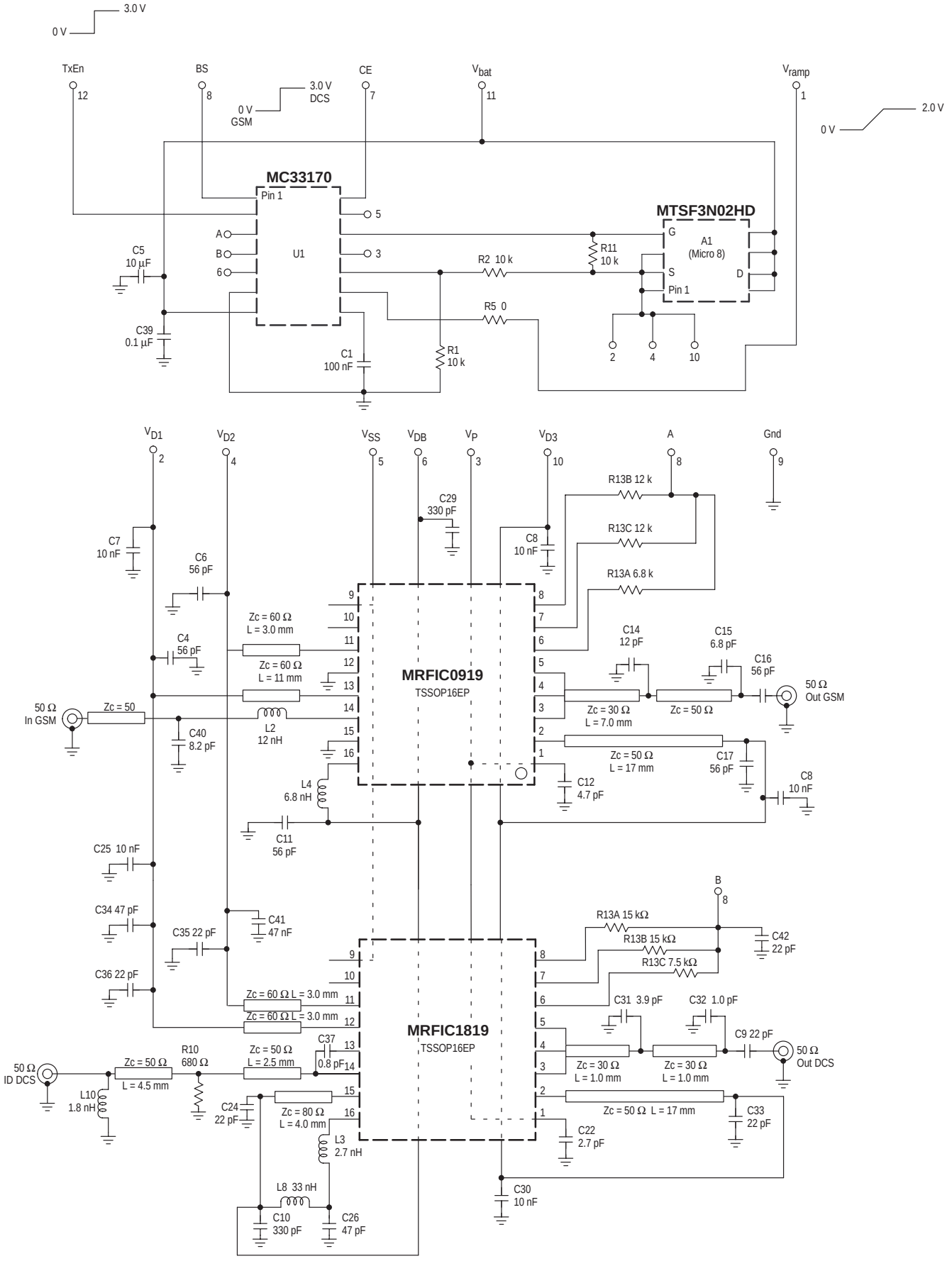


Figure 4. Output Power versus Frequency

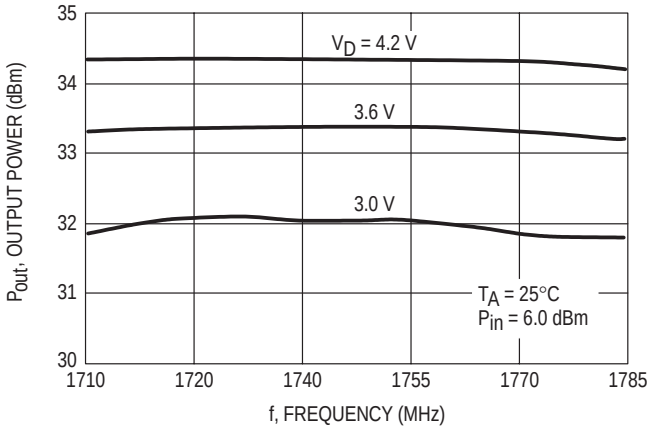


Figure 5. Power Added Efficiency versus Frequency

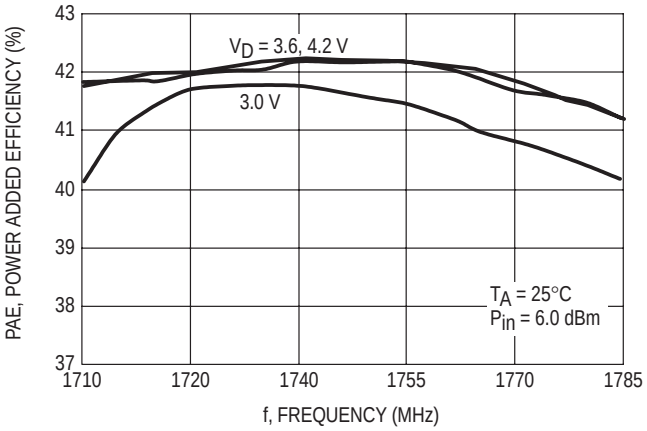


Figure 6. Output Power versus Frequency

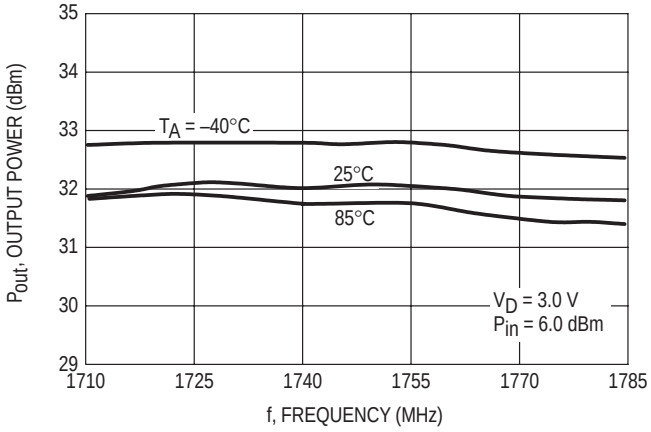


Figure 7. Output Power versus Frequency

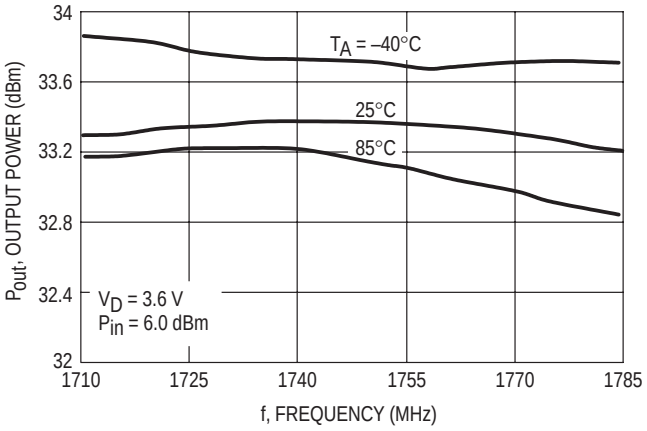


Figure 8. Output Power versus Frequency

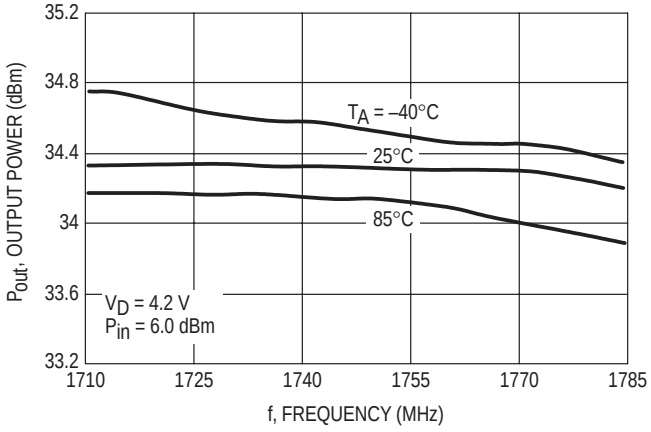


Figure 9. Power Added Efficiency versus Frequency

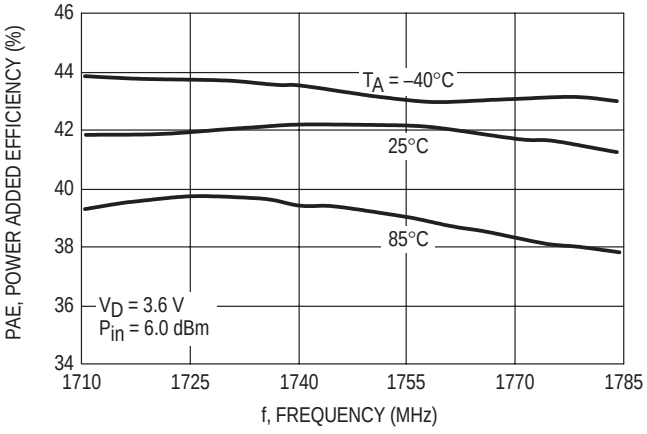


Figure 10. Output Power versus Drain Voltage

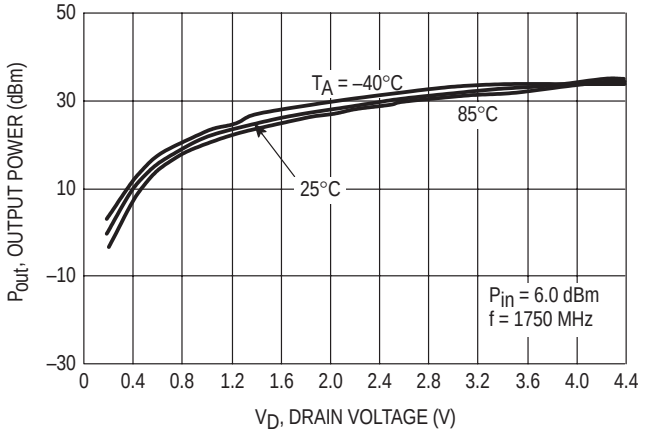


Figure 11. Power Added Efficiency versus Drain Voltage

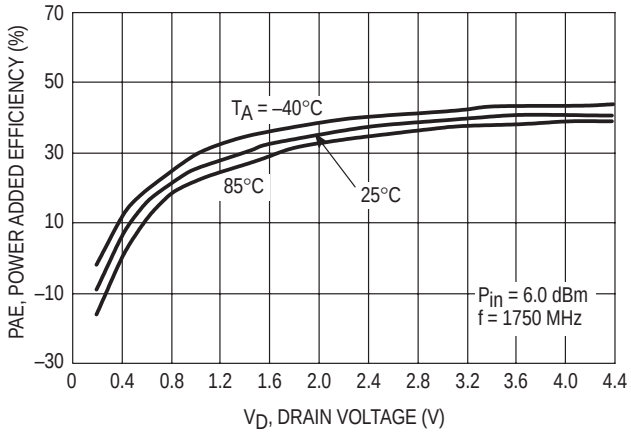


Figure 12. Positive Voltage Generator Output versus Drain Voltage

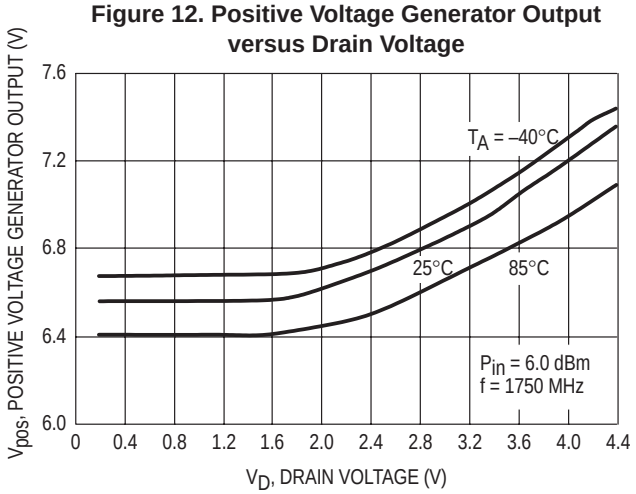
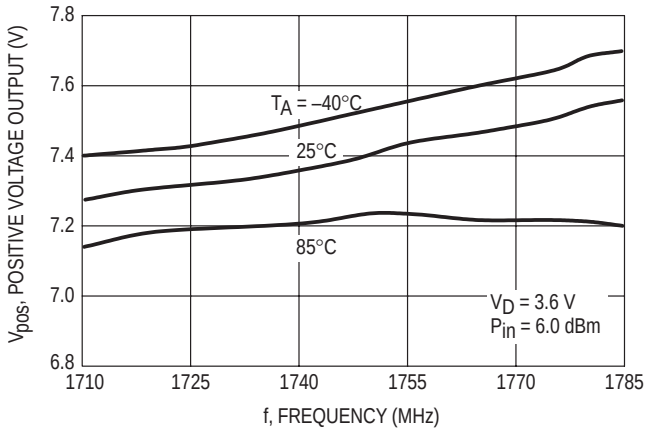


Figure 13. Positive Voltage Output versus Frequency



APPLICATIONS INFORMATION

Design Philosophy

The MRFIC1819 is a high performance three stage GaAs IPA (Integrated Power Amplifier) designed for DCS/PCS handheld radios (1710–1785 MHz DCS frequency band, 1850–1910 MHz PCS frequency band). With a 3.6 V battery supply, it delivers typically 33 dBm of Output Power with 41% Power Added Efficiency.

It features an internal Negative Voltage Generator based on RF rectification of the input carrier after its amplification by two dedicated buffer stages (see Internal Block Diagram). This method eliminates spurs found on the Output signal when using dc/dc converter type negative voltage generators, either on or off chip. The buffer also generates a step–up positive voltage which can be used to drive a N–MOS drain switch.

The RF input power is split **externally** (different from MRFIC0919) to the 3 stage RF line–up (Q1, Q2 and Q3) and the Buffer amplifier (Q0, QB). This arrangement allows separate operation of Voltage Generation and Power Amplification for maximum flexibility.

External Circuit Considerations

The MRFIC1819 can be tuned by changing the values and/or positions of the appropriate external components (see Figure 1: Reference Circuit). While tuning the RF line–up, it is recommended to apply external negative supply in order to prevent any damage to the power amplifier stages. Poor tuning on the input may not provide enough RF power to operate the negative voltage generator properly.

Input matching is a shunt–L, series–L high–pass structure and should be optimized at the rated RF Input power (e.g. 6.0 dBm). However, broadband matching is easier with a parallel 680 Ω resistor. This part can be removed to get operation to a lower input power (e.g. 5.0 dBm). Since the Input line feeds both 1st stage and buffer, Input matching should be iterated with Buffer and Q1 drain matching. Note that a dc blocking capacitor is included on chip.

RF input signal is fed to buffer amplifier using C12 capacitor (Figure 1). The value of this capacitor determines the power split between RF line–up and buffer amplifier. C12 has been tuned to get the best trade–off between RF gain and negative voltage on Pin 9.

First stage buffer amplifier is tuned with a short 80 Ω microstrip line which may be replaced by a chip inductor (T4 on Figure 1). Second stage buffer amplifier is supplied and matched through a discrete chip inductor. Those two elements are tuned to get the maximum output from voltage generator. The overall typical buffer current is about 50 mA; however, the negative generator needs a settling time of 2.0 µsec (see burst mode paragraph). During this transcient period of time, both stages are biased to IDSS which is about 200 mA each.

The step–up positive voltage available at Pin 1 is both decoupled and maximised by a small shunt capacitor. This positive voltage which is approximately twice the buffer drain voltage can be used to drive a NMOS drain switch for best performances.

Q1 drain is supplied and matched through a printed microstrip line that could be replaced by a discrete chip inductor as well. Its length (or equivalent inductor value) is tuned by sliding the RF decoupling capacitor along to get the maximum gain on the first stage.

Q2 is supplied through a printed microstrip line that contributes also to the interstage matching in order to provide optimum drive to the final stage.

The line length for Q1 and Q2 is small , so replacing it with a discrete inductor is not practical.

Q3 drain is fed via a printed line that must handle the high supply current of that stage (2.0 Amp peak) without significant voltage drop. This line can be buried in an inner layer to save PCB space or be a discrete RF choke.

Output matching is accomplished with a two stages low–pass network. Easy implementation is achieved with shunt capacitors mounted along a 2.0 mm 30 Ω microstrip transmission line. Value and position are chosen to reach a load line of 5.5 Ω while conjugating the device output parasitics. The network must also properly terminate the second and third harmonic to optimize efficiency and reduce harmonic level. Use of high Q capacitor for the first output matching capactor circuit is recommended in order to get the best Output Power and Efficiency performance.

NOTE: The choice of output matching capacitors type and supplier will affect H2 and H3 level and efficiency, because of serie resonnant frequency.

Biasing Considerations

The internally generated negative voltage is clamped by an external Zener diode in order to eliminate variation linked to Input power or Buffer supply. This negative voltage is used by three independent bias circuits to set the proper quiescent current of all stages. Each bias circuitry is equivalent to a current source sinking its value from the bias pin. When the bias pins are set to 3.0 V, nominal quiescent current and operating point of each RF stage are selected.

Q1 and Buffer share the Bias1 (0.25 mA) while Q2 and Q3 have dedicated Bias2 (0.25 mA) and Bias3 (0.5 mA) respectively. It is also possible to reference those bias pins to Gnd by changing series resistors R1, R2, R3 (Fig. 1) that drops the 3.0 V.

If those pins are left opened, the corresponding stages are pinched–off. Thus the bias pins can be used as a mean to select the MRFIC1819 or the MRFIC0919 in a dual band configuration. The MRFIC0919 is the partner device to the MRFIC1819 and is designed for GSM900 applications.

Table 2. Pin Function Description

Pin	Symbol	Description
1	V_P	Positive voltage output
2	V_{D3}	Third stage drain supply
3	RF Out	RF output
4	RF Out	RF output
5	RF Out	RF output
6	Bias3	Third stage bias
7	Bias2	Second stage bias
8	Bias1	Buffer and first stage bias
9	V_{SS}	Negative voltage output
10	V_{SC}	Negative voltage check
11	V_{D2}	Second stage drain supply
12	V_{D1}	First stage drain supply
13	RF In	RF input
14	In Buf	Buffer RF input
15	V_{D0}	First buffer stage drain supply
16	V_{DB}	Buffer stage drain supply

Vsc is an open drain internal FET switch which is biased through the negative voltage. Consequently, this pin is high impedance when negative voltage is okay and low impedance (about 40 Ω) when negative voltage is missing.

Operation Procedure

The MRFIC1819 is a standard MESFET GaAs Power Amplifier, presence of a negative voltage to bias the RF line–up is essential in order to avoid any damage to the parts. Due to the fact that the negative voltage is generated through rectification of the RF input signal, a minimum input power level is needed for correct operation of the demoboard. The following procedure will guaranty safe operation for doing the RF measurements.

Note: make sure that Bias1 (Pin 8 of demoboard Figure 2) is connected 3.0 V or will have equivalent potential for nominal biasing of Buffer stage.

6. Apply RF input power (RF In) > 6.0 dBm.
7. Apply V_{DB} = 3.0 to 5.0 V.
8. Check that V_{SS} reaches approximatively –5.1 V (settling of the negative voltage) (Pin 9).
9. Apply $V_{D1,2\&3}$=0 to 5.0 V.
10. Measure RF output power and relevant parameters.

Proceed in the reverse order to switch off the Power Amplifier.

Control Considerations

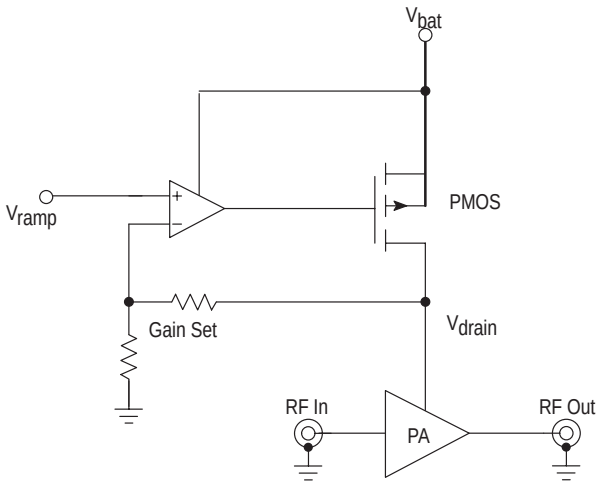
MRFIC01819 application uses the drain control technique developed for our previous range of GaAs IPAs (refer to application note AN1599). This method relies on the fact that for an RF amplifier operating in saturation mode, the RF output power is proportional to the square of the Amplifier drain voltage: Pout(Watt)=k*Vd(Volt)*Vd(Volt).

In the proposed application circuit (see Figure 2: application circuit), a PMOS FET is used to switch the IPA drain and vary the drain supply voltage from 0 to battery voltage. As the PMOS FET has a non linear behavior, an OpAmp is included in the application. This OpAmp is linearizing the PMOS by sensing its drain output and gives a true linear relationship between the Control voltage and the RF output voltage.

The obtained power control transfer function is so linear and repeatable than it can be used to predict the output power within a dynamic of 25 to 30 dB over frequency and temperature range. This so called “open–loop” arrangement eliminates the need for coupler and detector required for the classical but complex closed–loop control and consequently reduces the Insertion Loss from Power Amplifier to the Antenna.

The following block diagram shows the principle of operation as implemented in the application circuit of Figure 2. The OpAmp is connected as an inverter to compensate the negative gain of the PMOS switch.

Figure 14. Drain Control through PMOS Switch



NOTE: The positive voltage generated by the Buffer stage can be used to supply the OpAmp and make it possible to drive a NMOS switch as a voltage follower. Doing so, the main advantage is to have a lower Rdson switch and better intrinsic linearity.

In Figure 15, the plot illustrates the “open–loop” performance regarding temperature stability. The measured datas are diplayed in a log–log scale in order to have a good representation of both the dynamic and the linearity of control. The variation of Pout accross the frequency band are also very small (less than 1.0 dB ripple) and are kept to that small amount when controlling Pout through the Drain voltage.

Figure 15. Temperature Stability of the Open Loop Control

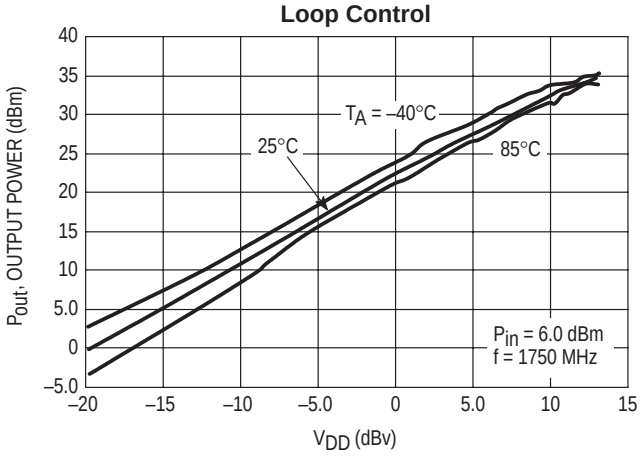
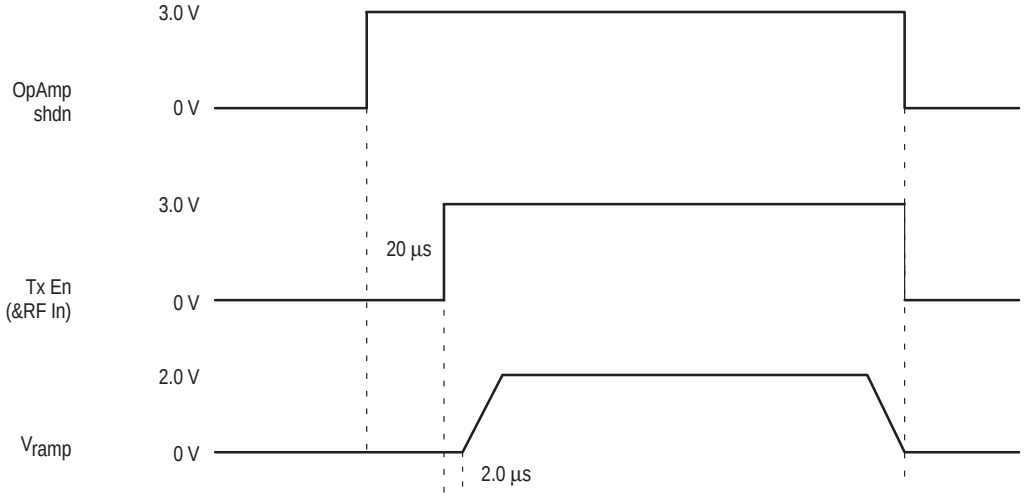


Figure 16. Timing Guide



Burst mode

Use Figure 18 as a guide line to perform burst mode measurements with the complete application circuit of Figure 2. Notice that the V_{SC} pin is connected to V_{ramp} (through a resistor) and acts as a pull down when negative voltage is missing so that drain voltage is not applied to the RF line–up.

– Bursting the OpAmp with its Pin 8 (shdn) is not mandatory during a call as the OpAmp current consumption is very small (1.0 to 2mA). This pin is mainly used for the idle mode of the radio. In any case, the wake–up time of the OpAmp is very short.

– V_{ramp} can be applied soon after Tx EN since the internal negative voltage generator settles in less than 2.0 µs.

– Tx EN signal can be used to switch the input power (using a driver or attenuator) in order to provide higher isolation for on/off burst dynamic.

References (Motorola application notes)

AN1599 – Power Control with the MRFIC0913 GaAs Integrated Power Amplifier and MC33169 Support IC.

AN1602 – 3.6 V and 4.8 V GSM/DCS1800 Dual Band PA Application with DECT capability Using Standard Motorola RFIC's.

MOTOROLA

MRFIC1830

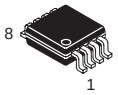
1.8 – 1.9 GHz GaAs Low Noise Amplifier with Gain Control

Designed primarily for use in 1.8 to 1.9 GHz wireless Personal Communication Systems (PCS) such as DCS1800, PCS1900, PHS, and DECT. The MRFIC1830 is a two–stage low noise amplifier with an integrated step attenuator and is packaged in a low–cost Micro–8 package. The attenuator is controlled by a CMOS compatible V_{gain} pin. The LNA can be turned off during transmit mode to save current by using the CMOS compatible Receive Enable pin. The amplifier can be matched to optimize gain or noise figure with simple off–chip input matching.

- Usable Frequency Range = 1800 to 2000 MHz
- 19 dB Typ Gain at 1.8 GHz and 17.5 dB at 1.9 GHz
- Gain Attenuation = 19.5 dB (Typ)
- 2.1 dB Typ Noise Figure for DCS and 2.3 dB for PCS
- Simple Off–chip Matching for Maximum Gain/Noise Figure Flexibility
- High Reverse Isolation = 38 dB (Typ)
- Low Power Consumption = 30 mW (Typ)
- Single Bias Supply = 2.7 to 4.5 V
- Low Standby Current = 20 μA (Typ)
- Low Cost Surface Mount Plastic Package
- Device Marking = M1830

DCS/PCS GaAs LOW NOISE AMPLIFIER WITH GAIN CONTROL

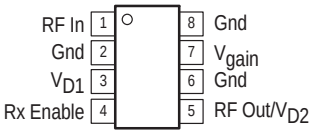
SEMICONDUCTOR TECHNICAL DATA



(Scale 2:1)

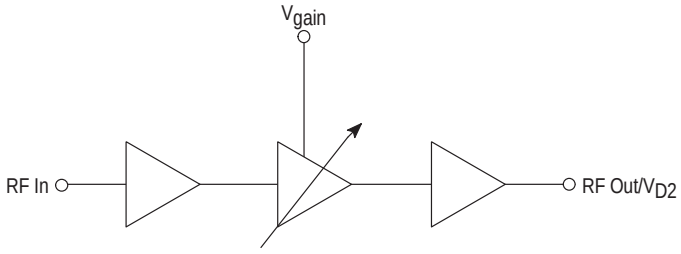
DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8, Tape & Reel Only)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



This device contains 12 active transistors.

ORDERING INFORMATION

Device	Operating Temp Range	Package
MRFIC1830DMR2	T_A = –30 to 70°C	Micro–8 Tape & Reel*

*2,500 Units per 12 mm, 13 inch reel.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Symbol	Limit	Unit
Supply Voltage	V_{D1}, V_{D2}	5.5	Vdc
RF Input Power	P_{RF}	3	dBm
Gain Control Voltage	V_{gain}	5.5	Vdc
Enable Voltage	Rx Enable	5.5	Vdc
Storage Temperature Range	T_{stg}	– 65 to 150	°C
Operating Ambient Temperature	T_A	– 20 to 70	°C

NOTES: 1. Meets Human Body Model (HBM) ≤250 V and Machine Model ≤50 V.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

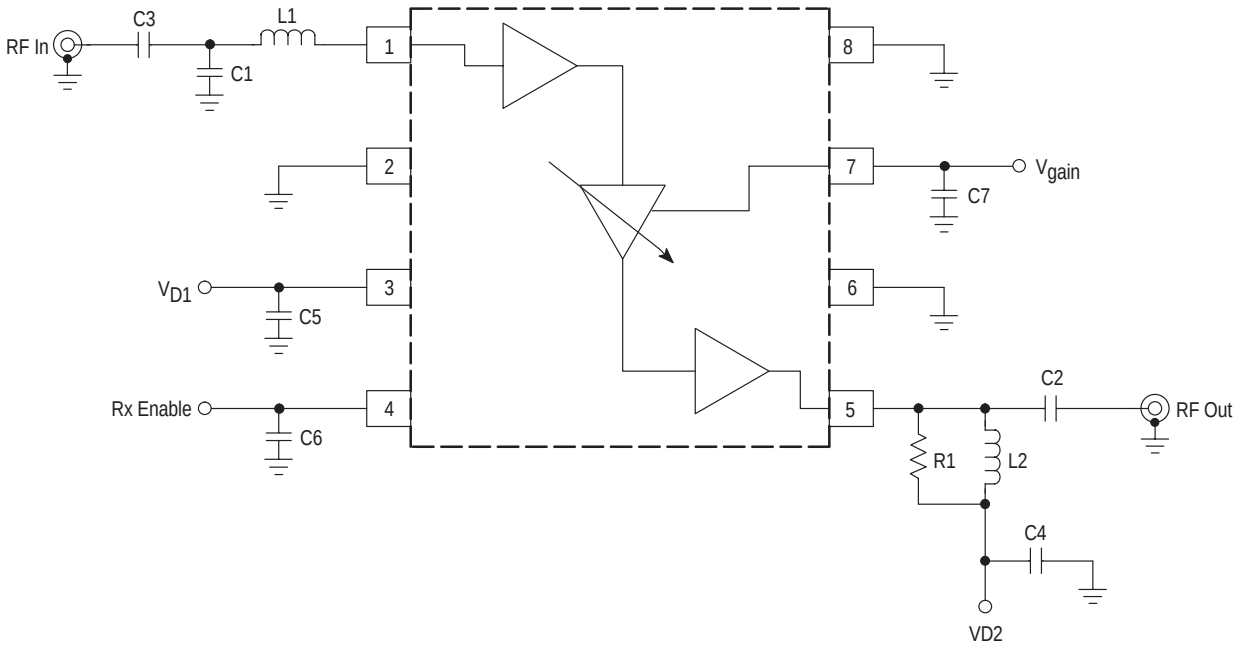
Parameter	Symbol	Min	Typ	Max	Unit
RF Frequency (DCS) DCS PCS	f_{RF}	 1.8 1.93	 – –	 1.88 1.99	GHz
Supply Voltage	V_{D1}, V_{D2}	2.7	–	4.5	Vdc
V Gain, High Gain	V_{gain}	–	3.0	–	Vdc
V Gain, Low Gain	V_{gain}	–	0	–	Vdc
Rx Enable Voltage, On	Rx Enable	2.7	–	V_{D1}, V_{D2}	Vdc
Rx Enable Voltage, Off	Rx Enable	0	–	0.2	Vdc

ELECTRICAL CHARACTERISTICS ($V_{D1, D2}$ = 2.8 V, T_A = 25°C, RF = 1840 MHz (1960 MHz for PCS), RF In = –30 dBm, Rx Enable = 2.8 V, V_{gain} = 2.8 V, unless otherwise noted. Tested in circuit shown in Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
RF Gain DCS PCS	–	 17 –	 19 17.5	 21 –	dB
RF Gain (V_{gain} = 0 V) (DCS and PCS)	–	–	–0.5	2.5	dB
SSB Noise Figure (DCS) [Note] DCS PCS	–	 – –	 2.1 2.3	 3.0 –	dB
SSB Noise Figure (V_{gain} = 0 V) (DCS and PCS) [Note]	–	–	9.5	20	dB
RF Input 3rd Order Intercept Point [Note] DCS and PCS V_{gain} = 0 V (DCS and PCS)	–	 –12 –7.0	 –9.0 –1.0	 – –	dBm
Input 1.0 dB Gain Compression [Note] DCS and PCS V_{gain} =0 V (DCS and PCS)	–	 –21.5 –16	 –20 –13	 – –	dBm
Reverse Isolation (S_{12}) V_{gain} = 3.0 V V_{gain} = 0 V	–	 – –	 38 47	 – –	dB
Input Return Loss V_{gain} = 3.0 V V_{gain} = 0 V	–	 – –	 15 12	 – –	dB
Output Return Loss V_{gain} = 3.0 V V_{gain} = 0 V	–	 – –	 12 12	 – –	dB
Supply Current Rx Mode	–	–	9.0	12	mA
Supply Current Standby Mode (Rx Enable = 0 V)	–	–	20	200	μA

NOTE: Guaranteed by design.

Figure 1. 1.9 GHz Test Circuit



DCS (1.8 – 1.88 GHz)	**PCS (1.93 – 1.99 GHz)**
C1 = Not Used	C1 = 1.0 pF
C2 = 1.5 pF	C2 = 1.3 pF
C3, C4, C5, C6, C7 = 1.0 kpF	C3, C4, C5, C6, C7 = 1.0 kpF
L1 = 5.6 nH	L1 = 5.6 nH
L2 = 2.2 nH	L2 = 2.2 nH
R1 = 390 Ω	R1 = 390 Ω

Figure 2. Reverse Isolation versus Frequency

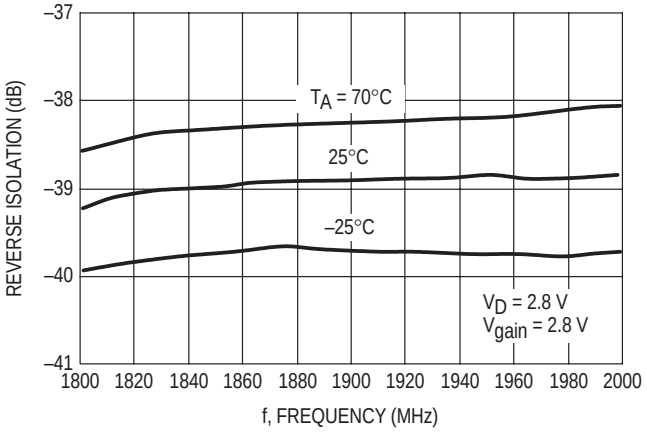


Figure 3. Reverse Isolation versus Frequency

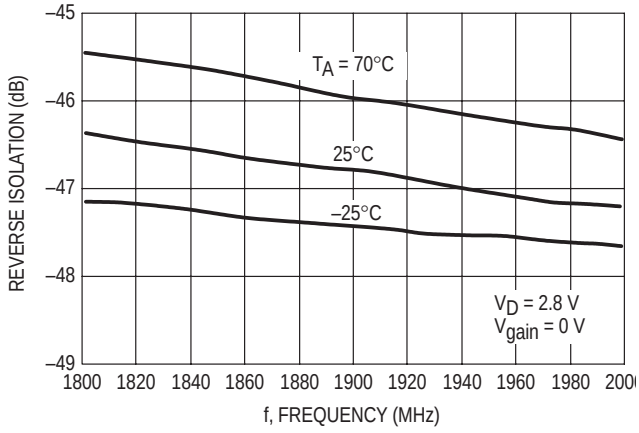


Figure 4. Gain versus Frequency

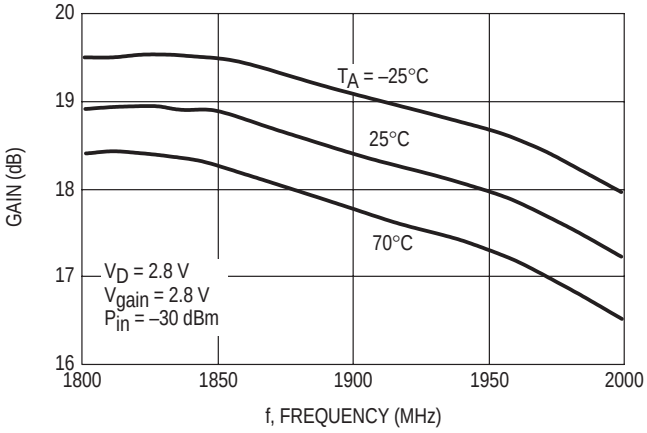


Figure 5. Gain Attenuation versus Frequency

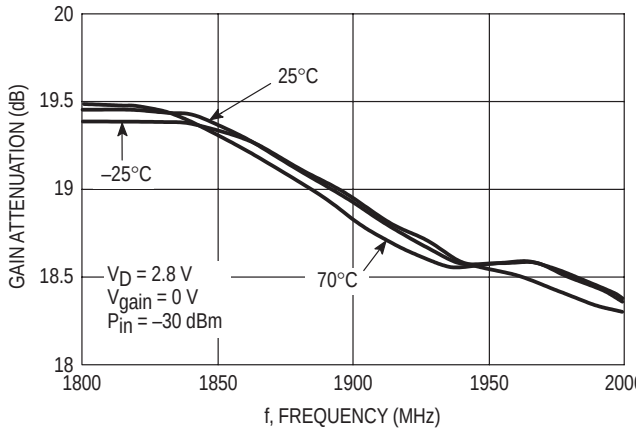


Figure 6. Gain versus Frequency

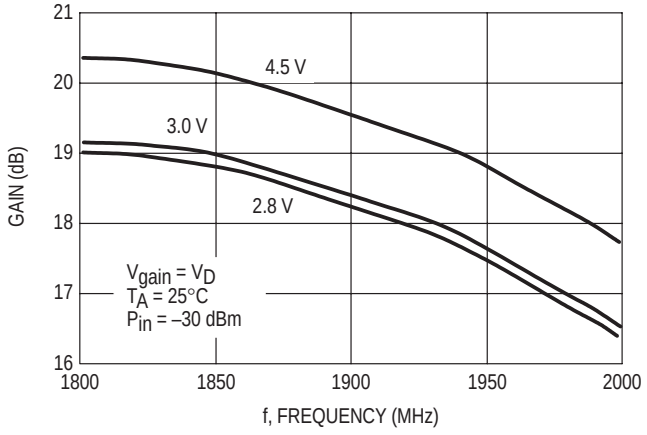


Figure 7. Gain Attenuation versus Frequency

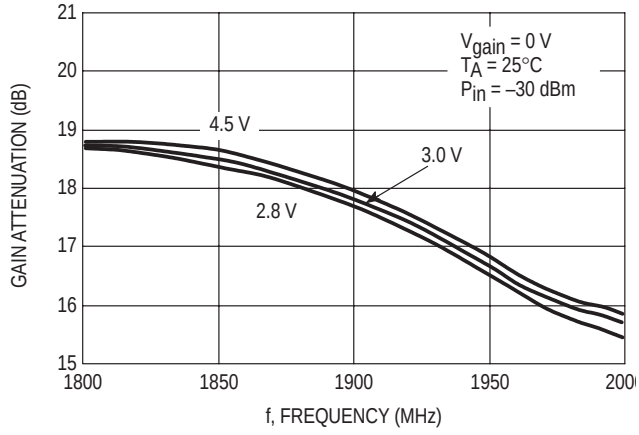


Figure 8. Input Power versus Output Power

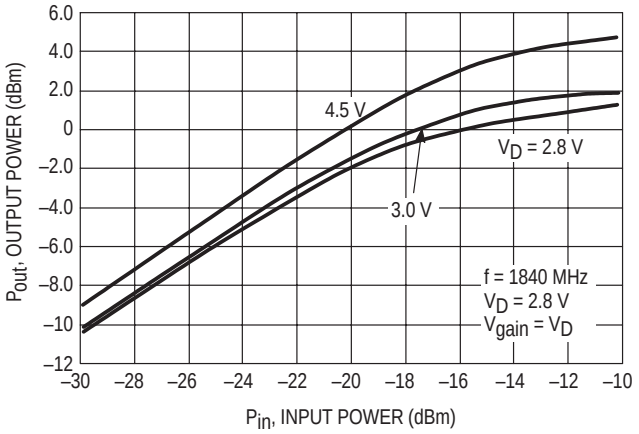


Figure 9. Input Power versus Output Power

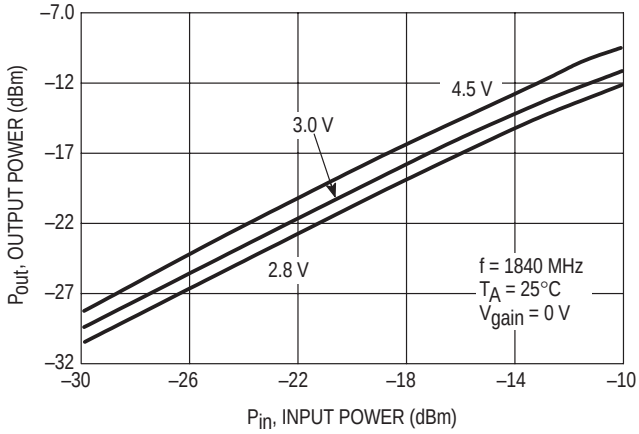


Figure 10. Input Power versus Output Power

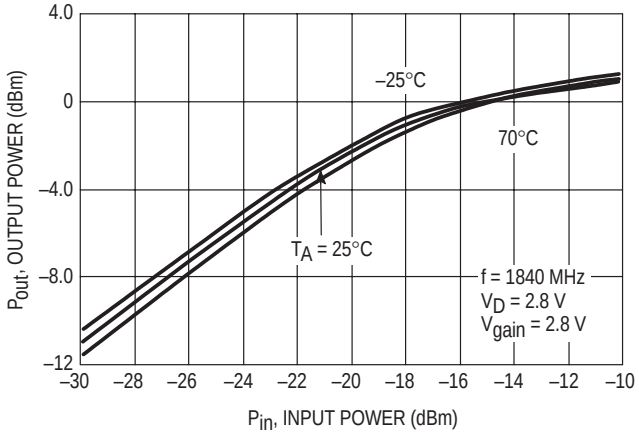


Figure 11. Input Power versus Output Power

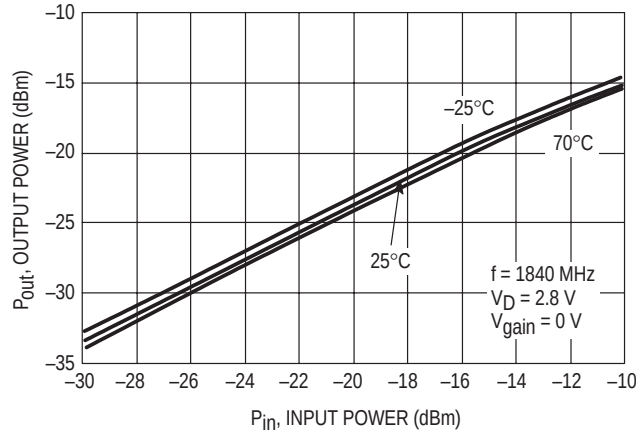


Figure 12. Noise Figure versus Frequency

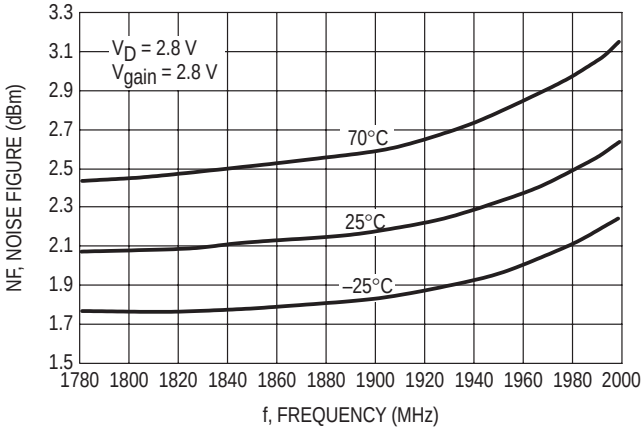
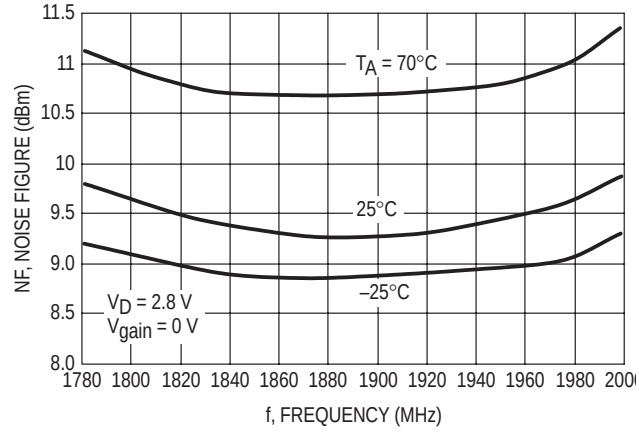


Figure 13. Noise Figure versus Frequency



MOTOROLA

MRFIC1854

Advance Information

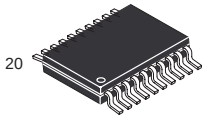
1.9 GHz CDMA Upmixer/Exciter

The MRFIC1854 is an integrated upmixer and exciter amplifier designed specifically for PCS CDMA digital cellular radios. The exciter amplifier incorporates a temperature compensated linear gain control and selectable bias to reduce power consumption. The design utilizes Motorola's RF BiCMOS1 process to yield superior performance in a cost effective monolithic device.

- Total Supply Current CDMA Mode = 55 mA Typical
- 65 dB Dynamic Range Gain Control
- Upmixer Output IP3 = 6.0 dBm Typical
- Exciter Output IP3 = 22 dBm Typical
- Supply Voltage Range = 2.7 to 3.6 V
- Adjacent Channel Power (ACPR) @ 1.25 MHz Offset (P_{out} = 3.0 dBm) = –58 dBc Typical

1.9 GHz CDMA UPMIXER/EXCITER

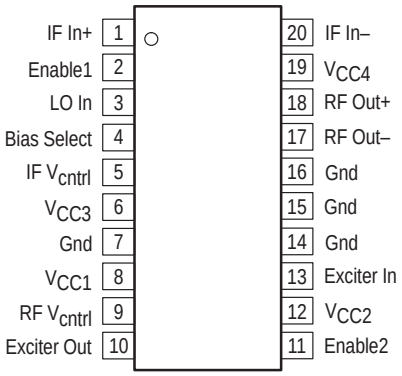
SEMICONDUCTOR TECHNICAL DATA



(Scale 2:1)

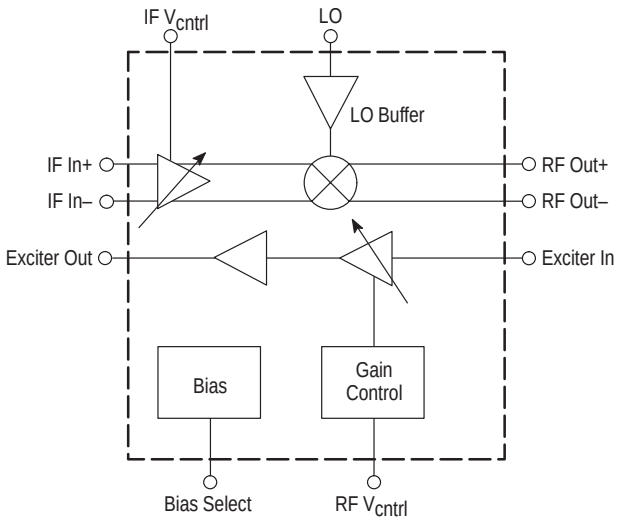
PLASTIC PACKAGE
CASE 948M
(TSSOP–20EP, Tape & Reel Only)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



This device contains 305 active transistors.

ORDERING INFORMATION

Device	Operating Temp Range	Package
MRFIC1854R2	T_A = –40 to 85°C	TSSOP–20EP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	5.0	V
IF Input	IF In+, IF In–	10	dBm
LO Input	LO	10	dBm
Operating Temperature	T_A	–40 to 85	°C
Storage Temperature	T_{stg}	–65 to 150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions and Electrical Characteristics tables or Pin Descriptions section.
2. Meets Human Body Model (HBM) ≤50 V and Machine Model (MM) ≤40 V. This device is rated Moisture Sensitivity Level (MSL) 4. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	–	3.6	V
RF Frequency Range	f_{RF}	1700	–	2000	MHz
IF Frequency Range	f_{IF}	70	–	250	MHz
LO Frequency Range	f_{LO}	1500	–	2100	MHz
Gain Control Voltage Range	IF V_{cntrl}, RF V_{cntrl}	0.1	–	1.7	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 V, P_{LO} = –13 dBm @ 2010 MHz, P_{IF} = –27 dBm (differential) @ 130 MHz, $V_{Enable1}$ = $V_{Enable2}$ = 2.4 V, T_A = –40 to 85°C, Test Circuit in Figure 1, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CASCADE PERFORMANCE (Filter included between RF Out and Exciter input. Filter insertion loss is 4.0 dB)					
Output Power (V_{ctrl} = 1.7 V)	P_{out}	3.0	5.0	–	dBm
Dynamic Range (V_{ctrl} = 0.1 to 1.7 V)	DR	50	65	–	dB
Adjacent Channel Power @ 1.25 MHz Offset High Current (Bias Select = 0.4 V, P_{out} = 3.0 dBm (set by V_{ctrl}))	ACPR	 –52	 –58	 –	dBc
Supply Current High Current (Bias Select = 0.4 V) Low Current (Bias Select = 2.4 V)	I_{CC}	 – –	 55 35	 80 50	mA
MIXER SECTION					
Conversion Gain	G_C	–	16	–	dB
Noise Figure	NF	–	12	–	dB
Output Third Order Intercept Point	OIP3	–	6.0	–	dBm
IF AGC Dynamic Range	DR_{IF}	25	38	–	dB
EXCITER SECTION					
Gain (No Attenuation)	G	–	24	–	dB
Noise Figure	NF	–	5.0	–	dB
Output Third Order Intercept Point	OIP3	–	22	–	dBm
RF AGC Dynamic Range	DR_{RF}	25	38	–	dB

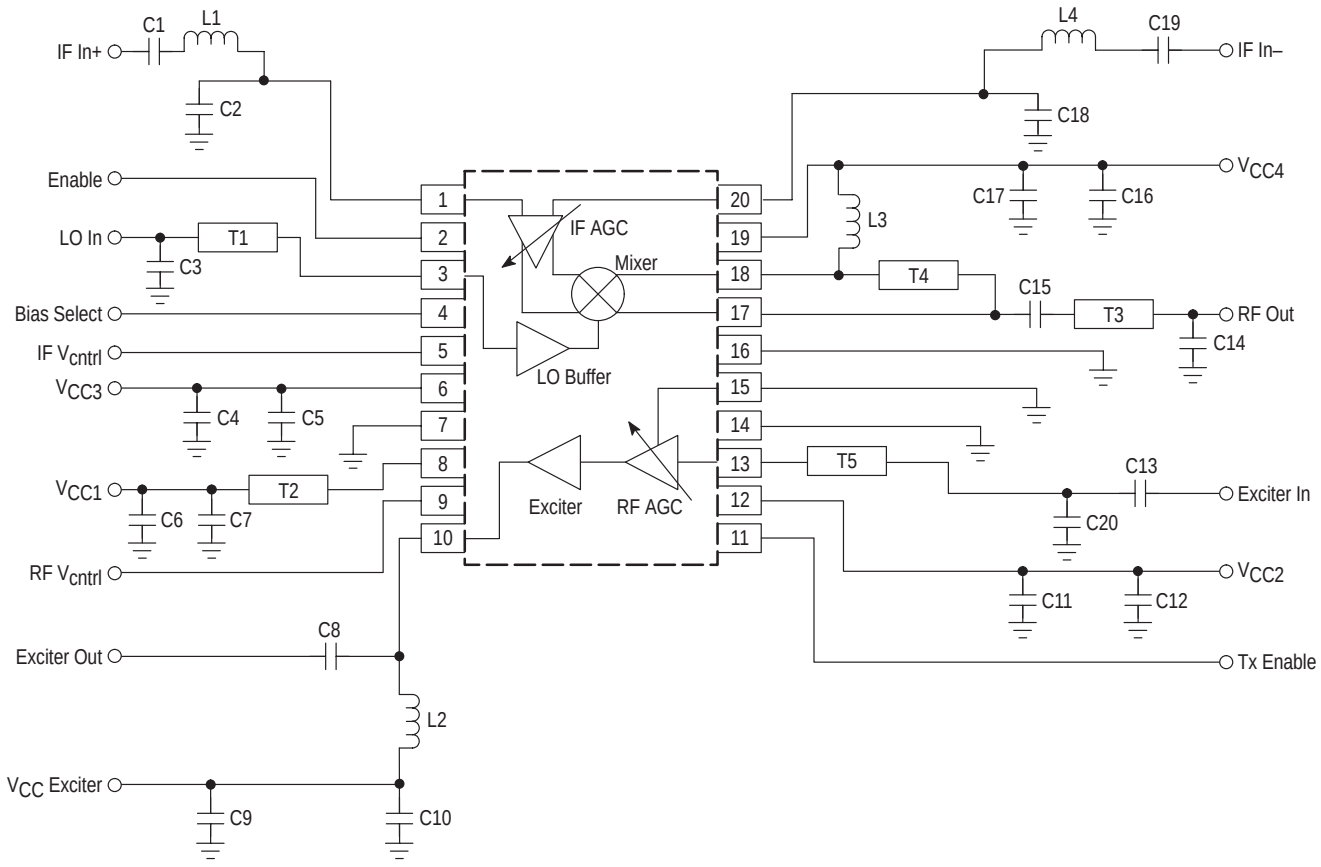
PIN FUNCTION DESCRIPTION

Pin	Function	Description	Voltage On (V)	Voltage Off (V)
1	IF In+	Mixer IF input pin. Input impedance is 500 Ω.	–33 dBm (Typ)	
2	Enable 1 (See Table 3)	Enable pin. A logic ″High″ (>2.4 V) enables entire chip and ″Low″ (<0.4 V) **disables chip.**	2.4 to 3.6	0 to 0.4
3	LO In	Mixer LO input pin.	–13 dBm (Typ)	
4	Bias Select	Bias select pin. Logic ″Low″ (<0.4 V) selects higher current bias for increased linearity and output power. ″High″ (>2.4 V) selects lower bias for reduced current consumption.		
5	IF AGC Control Voltage	IF AGC gain control pin. A 30 dB dynamic range can be acheived by adjusting voltage from 0.1 V (low gain) to 1.7 V (high gain).	0.1 to 1.7	
6	V_{CC3}	Supply Voltage.	2.7 to 3.6	
7	Gnd	Ground connection.	–	
8	V_{CC1}	Supply Voltage	2.7 to 3.6	
9	RF AGC Control Voltage	RF AGC control pin. A 30 dB dynamic range can be acheived by adjusting voltage from 0.1 V (low gain) to 1.7 V (high gain).	0.1 to 1.7	
10	Exciter Out	RF exciter amplifier output pin.	–	
11	Enable 2 (See Table 3)	Tx Enable pin. A logic ″High″ (>2.4 V) enables Tx path and ″Low″ (<0.4 V) **disables Tx path except LO Buffer**.	2.4 to 3.6	0 to 0.4
12	V_{CC2}	Supply Voltage	2.7 to 3.6	
13	Exciter In	RF exciter amplifier input pin.	–	
14	Gnd	Ground connection.	–	
15	Gnd	Ground connection.	–	
16	Gnd	Ground connection.	–	
17	RF Out–	Mixer RF output pin.		
18	RF Out+	Mixer RF output pin.		
19	V_{CC4}	Supply Voltage	2.7 to 3.6	
20	IF In–	Mixer IF input pin. Input impedance is 500 Ω.	–33 dBm (Typ)	

Table 1. Enable Truth Table

Enable 1	Enable 2	Mode
0	0	Disabled
0	1	Not Applicable
1	0	Standby Mode: Disables mixer/exciter, except LO buffer
1	1	Tx Enabled

Figure 1. Application Circuit



C1, C19	1.0 nF	L1, L4	220 nH
C2, C18	4.7 pF	L2	10 nH
C3	1.7 pF	L3	18 nH
C4, C6, C9, C12, C16	10 nF	T1	50 Ω Microstrip, L = 670 mils
C5, C8, C10, C11, C13, C15, C17	30 pF	T2	50 Ω Microstrip, L = 150 mils
C7	47 pF	T3	50 Ω Microstrip, L = 400 mils
C14	3.6 pF	T4	50 Ω Stripline, L = λ/2 @ 1880 MHz
C20	1.0 pF	T5	50 Ω Microstrip, L = 350 mils

NOTES: 1. IF ports matched to 50 Ω for testing purposes.
2. Microstrip line and C7 form part of RF AGC/Exciter interstage match.
3. Er = 4.45 and board thickness = 18 mils.

Figure 2. Gain versus Frequency (Low Current Mode)

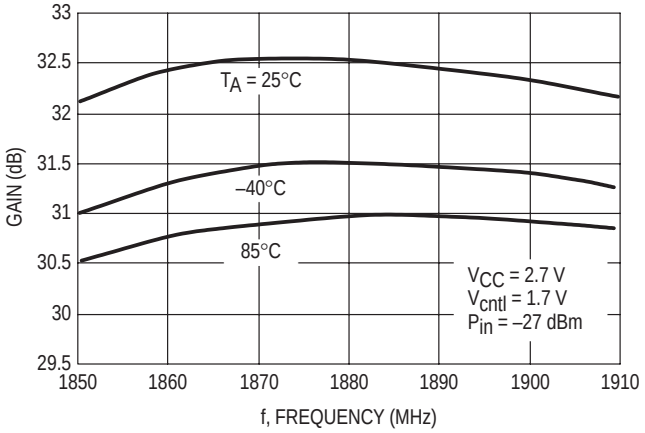


Figure 3. Gain versus Frequency (High Current Mode)

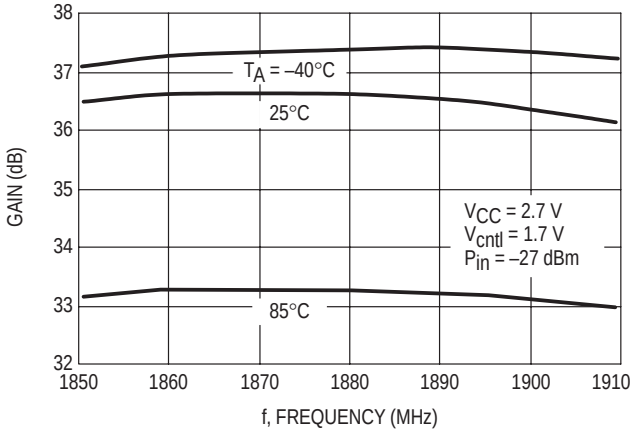


Figure 4. Gain versus LO Power (Low Current Mode)

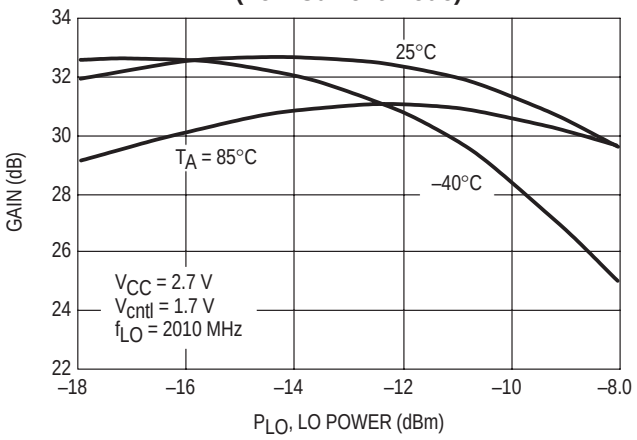


Figure 5. Gain versus LO Power (High Current Mode)

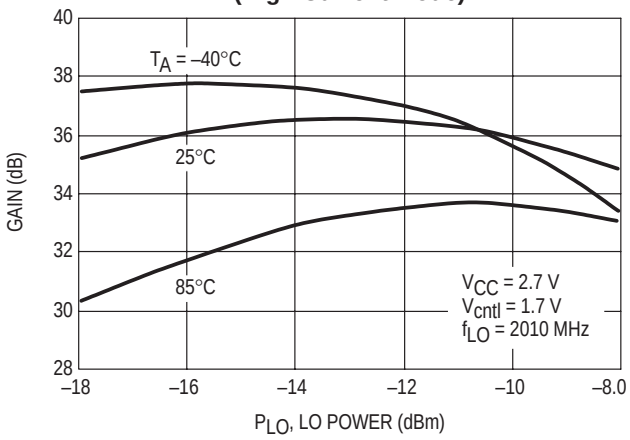


Figure 6. LO Feedthrough versus Control Voltage (Low Current Mode)

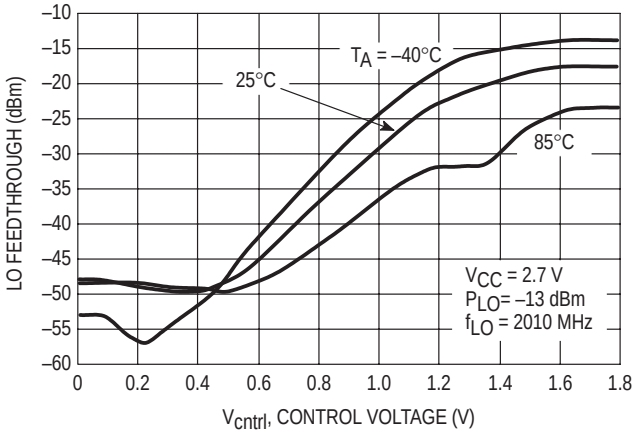


Figure 7. LO Feedthrough versus Control Voltage (High Current Mode)

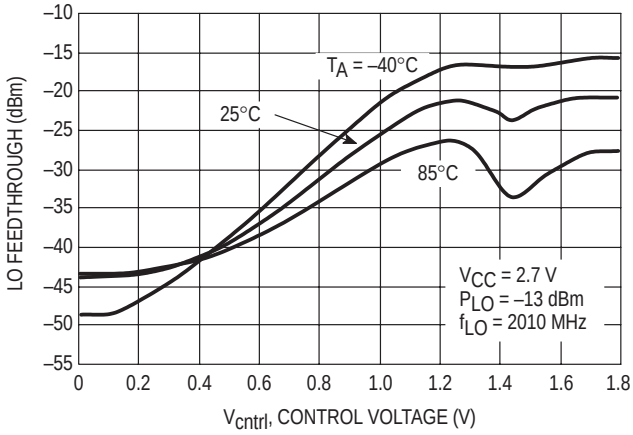


Figure 8. Output Power versus Control Voltage (Low Current Mode)

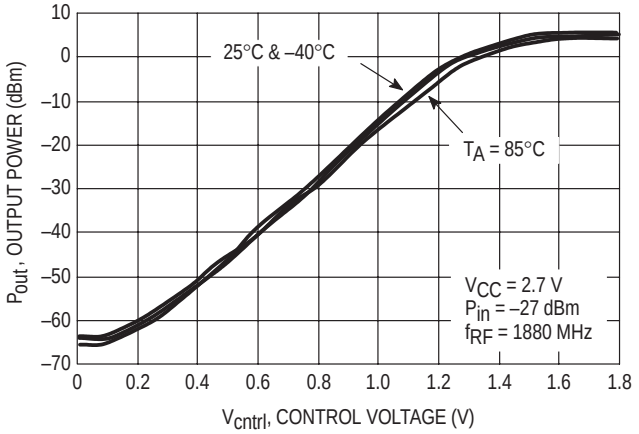


Figure 9. Output Power versus Control Voltage (High Current Mode)

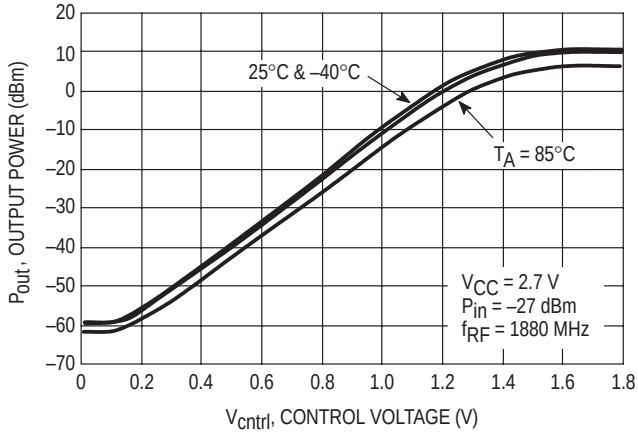
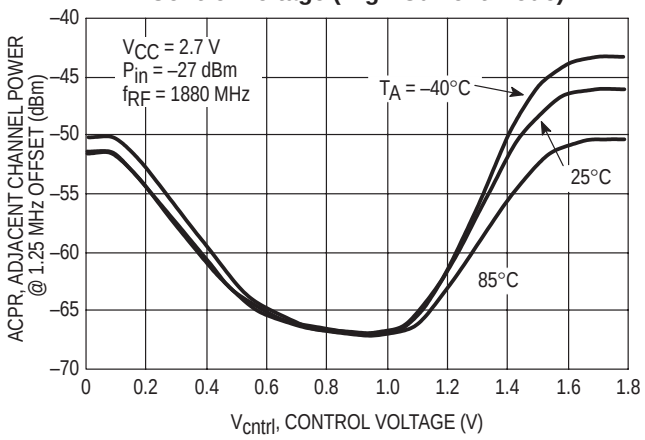


Figure 10. Adjacent Channel Power versus Control Voltage (High Current Mode)



APPLICATION INFORMATION

Design Philosophy

The MRFIC1854 has three operating states, enable, standby, and disable. These states are controlled by the truth table shown in Table 3. The device is fully operational during the enable state and the bias level can be selected. A high bias current for maximum power CDMA or a lower bias current for CDMA at lower powers can be selected via the Bias Select pin. In the high current CDMA mode, the quiescent current is increased to maximize the linearity of the device. In the lower current bias state, the quiescent current is reduced to save current during lower power CDMA operation. The standby mode can be used to reduce current consumption during Voice Activity Factoring. In the standby mode, the LO buffer remains on to prevent VCO pulling and the bandgap reference bias circuit remains on to assure rapid device turn on. Current consumption in standby mode is 10 mA typical. The disable mode is used to turn the MRFIC1854 completely off. Leakage current in this mode is only a few microamps.

The mixer is a double–balanced “Gilbert–cell” design with a balanced LO buffer amplifier. The input and output of the mixer are differential. The IF AGC is a differential amplifier that uses the “current steering” method for gain control. The IF AGC/mixer combination has 16 dB of gain and typically draws 20 mA quiescent current in the CDMA mode. An external filter is required between the mixer and RF AGC amplifier to reduce RX band noise.

Figure 1 shows the applications circuit for the MRFIC1854. In this circuit, the IF ports of the IF AGC have been matched to 50 Ω for testing purposes. In the actual application, the differential IF ports of the mixer would be impedance matched to an IF SAW filter. The differential impedance of the IF ports is 1600 ohms. The RF output of the mixer is configured as a differential output. A stripline balun is used to convert the RF output to single ended. DC current to the open collector output of the mixer is provided by inductor, L3 (18 nH) and transmission line, T4. Transmission lines T3 and T4, and capacitors C15 (30 pF) and C14 (3.6 pF) form the balun/output match for the mixer.

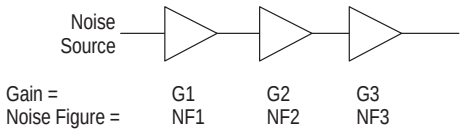
The RF AGC amplifier is a single–ended cascode design employing the standard “current steering” method of gain control. It’s ground is brought out through pin number 15 so inductance can be added to degenerate the gain for a lower noise floor. The maximum gain is around 13 dB. It typically draws 9.0 mA quiescent current in CDMA mode. The RF V_{cntrl} signal is buffered with an on–chip OpAmp then preconditioned with temperature compensation and dB/V linearization before being applied to the RF AGC amplifier.

Transmission line T2 and capacitor C7 (47 pF) are for the interstage match between the RF AGC and the exciter amplifier.

The exciter amplifier is a simple common emitter design. It is grounded directly to the exposed pad which results in 12 dB of gain. It typically draws 24 mA bias current in CDMA. Inductor L2 (10 nH), capacitor C8 (30 pF), and C10 (30 pF) provide the output matching. L2 also provides a DC current path for the open collector output.

Noise Power Considerations

In CDMA systems, the handset is required to dynamically adjust its output power to specific levels. This requires a dynamic range of as much as 90 dB from the transmitter. Another key performance specification in CDMA systems is the output noise power, both in band and out of band. Noise power specifications has caused the noise figure of the transmitter to become an important system consideration. The cascaded noise figure of the transmitter can be analyzed with the same equation used in receiver analysis. The only difference is the noise source is from the transmitter (modulator) instead of the atmosphere.



$$NF_{cascaded} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2}$$

This equation above shows that the cascaded noise figure is better if the gain is higher and the noise figure is lower for the stages close to the noise source. For this reason, it is advantageous to implement some of the gain control of a CDMA transmitter in the RF section. The MRFIC1854 integrates a RF AGC amplifier after the upmixer to improve the overall noise figure of the transmitter.

Table 2. Scattering Parameters for Exciter Amplifier
(V_{DD} = 2.7 V, T_A = 25°C, RF V_{cntrl} = 1.8 V, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$	$\lvert S_{21} \rvert$	$\angle\phi$	$\lvert S_{12} \rvert$	$\angle\phi$	$\lvert S_{22} \rvert$	$\angle\phi$
1700	0.319	–121.64	15.566	84.09	0.00476	–139.21	0.219	–12.29
1725	0.315	–123.78	16.291	76.55	0.00415	–126.71	0.222	–24.12
1750	0.310	–126.93	16.975	68.23	0.00406	–143.61	0.223	–35.58
1775	0.309	–130.34	17.590	56.64	0.00336	–143.09	0.237	–51.49
1800	0.304	–132.64	17.834	47.84	0.00406	–144.41	0.248	–64.80
1825	0.294	–137.08	17.944	35.98	0.00268	–141.85	0.271	–82.53
1850	0.286	–139.92	17.871	26.91	0.00411	–127.38	0.278	–94.74
1875	0.274	–141.87	17.591	17.93	0.00286	–132.49	0.298	–104.71
1900	0.261	–143.08	17.141	9.25	0.00351	–136.62	0.308	–114.83
1925	0.249	–145.61	16.374	–1.69	0.00447	–139.69	0.324	–128.42
1950	0.242	–146.86	15.738	–9.57	0.00322	–153.09	0.335	–137.57
1975	0.233	–148.86	15.046	–17.01	0.00411	–139.41	0.346	–146.12
2000	0.225	–149.74	14.132	–26.57	0.00490	–139.12	0.350	–155.24

Table 3. Scattering Parameters for Upmixer
(V_{DD} = 2.7 V, T_A = 25°C, IF V_{cntrl} = 1.8 V, 50 Ω System)

f	IF In+		IF In–		f	RF Out (Pin 17)	
(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$	$\lvert S_{11} \rvert$	$\angle\phi$	(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$
70	0.830	–2.07	0.832	–2.24	1700	0.815	–55.16
80	0.828	–2.73	0.830	–2.71	1725	0.814	–55.65
90	0.826	–3.01	0.828	–2.95	1750	0.814	–56.29
100	0.826	–3.21	0.827	–3.22	1775	0.817	–56.98
110	0.822	–3.57	0.825	–3.67	1800	0.820	–57.45
120	0.821	–3.74	0.823	–3.93	1825	0.823	–58.68
130	0.821	–3.93	0.823	–4.08	1850	0.825	–59.57
140	0.818	–4.25	0.820	–4.42	1875	0.826	–60.85
150	0.818	–4.54	0.821	–4.57	1900	0.825	–62.07
160	0.818	–4.61	0.820	–4.76	1925	0.815	–63.81
170	0.817	–4.85	0.819	–5.06	1950	0.807	–64.79
180	0.815	–5.12	0.819	–5.29	1975	0.794	–65.64
190	0.815	–5.26	0.819	–5.50	2000	0.782	–66.58
200	0.813	–5.45	0.816	–5.76			
210	0.815	–5.71	0.818	–6.15			
220	0.812	–5.82	0.816	–6.13			
230	0.811	–6.38	0.817	–6.54			
240	0.812	–6.54	0.814	–6.72			
250	0.810	–6.76	0.815	–6.98			

f	LO In		f	LO In		f	LO In	
(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$	(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$	(MHz)	$\lvert S_{11} \rvert$	$\angle\phi$
1500	0.708	–47.83	1725	0.677	–54.36	1950	0.624	–58.20
1525	0.704	–48.38	1750	0.670	–55.34	1975	0.623	–59.40
1550	0.702	–49.02	1775	0.654	–56.33	2000	0.612	–60.59
1575	0.696	–49.55	1800	0.641	–56.34	2025	0.605	–61.04
1600	0.694	–50.11	1825	0.636	–56.65	2050	0.599	–61.70
1625	0.691	–50.83	1850	0.631	–56.59	2075	0.592	–62.19
1650	0.688	–51.47	1875	0.630	–57.04	2100	0.588	–62.99
1675	0.691	–52.18	1900	0.626	–57.38			
1700	0.681	–53.42	1925	0.622	–57.84			

MOTOROLA

MRFIC1856

Product Preview

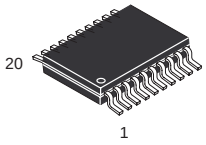
Dual–Band Dual Mode GaAs IPA

The MRFIC1856 is designed for dual–band subscriber equipment applications at 3.6 V in the 900 and 1800 MHz bands. The device incorporates two GaAs pHEMT amplifiers in one package allowing the most flexibility and highest performance while reducing board space. Target applications include dual–mode, dual–band handset for AMPS/DAMPS.

- Useable Frequency Range = 824 to 829 MHz AMPS/DAMPS and 1850 to 1910 MHz TDMA
- 3.6 V Operation
- 32 dBm Output Power AMPS
- 31 dBm Output Power DAMPS
- 30 dBm Output Power TDMA

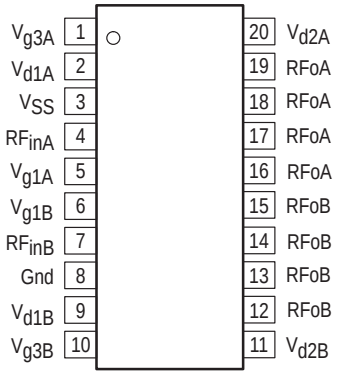
DUAL–BAND DUAL MODE GaAs IPA

SEMICONDUCTOR TECHNICAL DATA



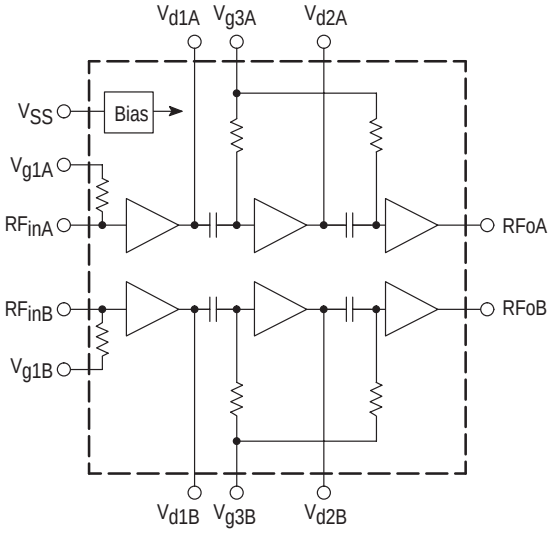
PLASTIC PACKAGE
CASE 948M
(TSSOP–20EP, Tape & Reel Only)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Operating Temp Range	Package
MRFIC1856R2	T_C = –35 to 100°C	TSSOP–20EP Tape & Reel*

*1,500 Units per 16 mm, 13 inch reel.

The MRFIC Line
900 MHz 2 Stage PA

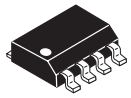
MRFIC2006

900 MHz 2 STAGE PA
SILICON MONOLITHIC
INTEGRATED CIRCUIT

The MRFIC2006 is an Integrated PA designed for linear operation in the 800 MHz to 1.0 GHz frequency range. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC2006 include CT-1 and CT-2 cordless telephones, remote controls, video and audio short range links, low cost cellular radios, and ISM band transmitters.

- 50 Ω Input and Output Impedance
- Typical Gain = 23 dB @ 900 MHz
- Bias Current Externally Adjustable
- Bias Pin can be used to Ramp or Disable
- Class A or AB Linear Operation
- Unconditionally Stable
- SO-8 Leaded Plastic Package
- Order MRFIC2006R2 for Tape & Reel.R2 Suffix
- Device Marking = M2006

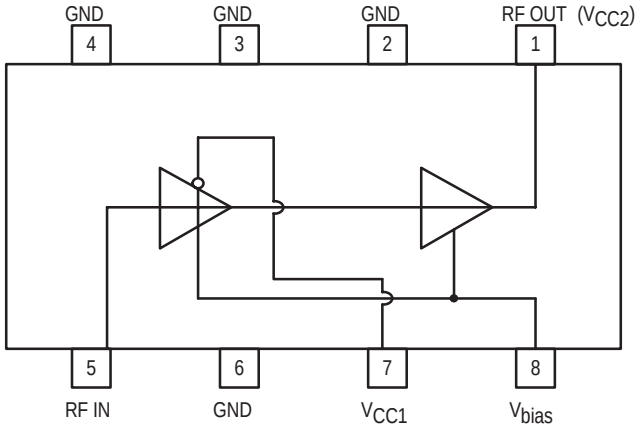
NOT RECOMMENDED FOR NEW DESIGN
DEVICE TO BE PHASED OUT.
No replacement available.



CASE 751-06
(SO-8)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Z_O = 50 Ω unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC1}, V_{CC2}	5.0	Vdc
Bias Voltage	V_{bias}	6.0	Vdc
Total Supply Current	I_{CC1}, I_{CC2}	100	mA
RF Output Power (V_{CC2} < 4.0 V)	P_{out}	+21	dBm
RF Output Power (4.0 V < V_{CC2} ≤ 5.0 V)	P_{out}	53 – 8 V_{CC2}	dBm
RF Input Power	P_{in}	+10	dBm
Operating Ambient Temperature	T_A	– 35 to + 85	°C
Storage and Junction Temperature	T_{stg}	– 65 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	63	°C/W



Pin Connections and Functional Block Diagram

REV 4
12/99

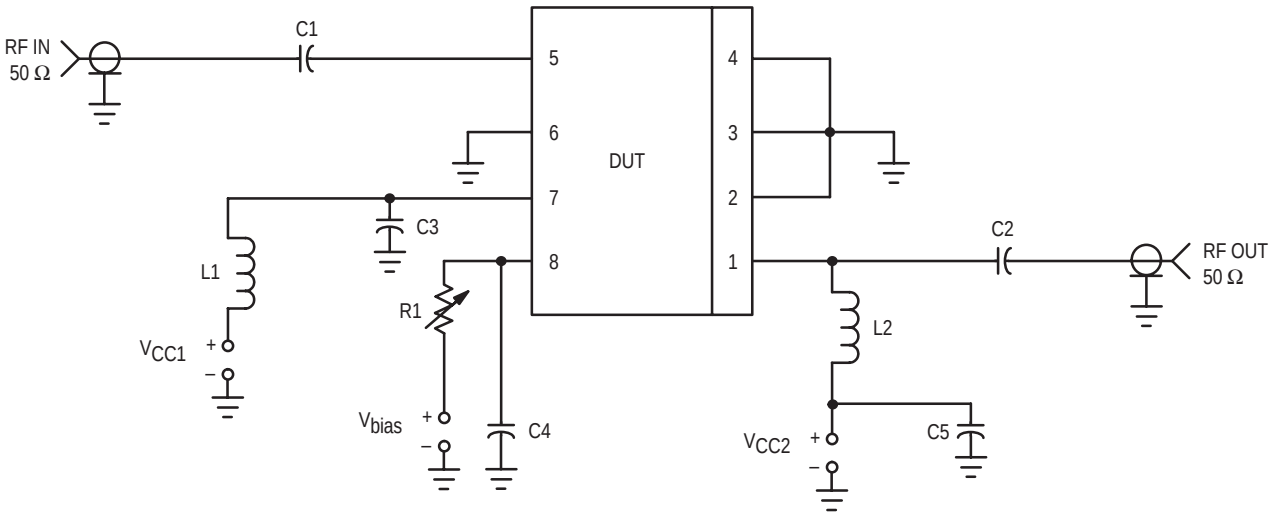
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage Ranges	V_{CC1}, V_{CC2}	1.8 to 4.0	Vdc
Bias Voltage Range	V_{bias}	0 to 5.0	Vdc
RF Frequency Range	f	500 to 1000	MHz

ELECTRICAL CHARACTERISTICS (V_{CC1}, V_{CC2}, V_{bias} = 3.0 V, T_A = 25°C, f = 900 MHz, Z_o = 50 Ω unless otherwise noted)

Characteristics (1)	Min	Typ	Max	Unit
Supply Current — Total	—	46	55	mA
I_{CC1}	—	14	—	mA
I_{CC2}	—	29	—	mA
I Bias	—	3.0	—	mA
Small Signal Gain	19	23	26	dB
Input Return Loss, RF IN Port	—	15	—	dB
Output Return Loss, RF OUT Port	—	15	—	dB
Reverse Isolation	—	35	—	dB
Output Power at 1.0 dB Gain Compression	+12	+15.5	—	dBm
3rd Order Intercept Point (Out)	—	+ 25	—	dBm
5th Order Intercept Point (Out)	—	+ 21	—	dBm

NOTE:
1. All electrical characteristics measured in test circuit schematic shown in Figure 1 below.



C1, C2 — 100 pF Chip Capacitor
C3, C5 — 1.0 nF Chip Capacitor
C4 — 10 nF Chip Capacitor
L1 — 150 nH Chip Inductor
L2 — 10 nH Chip Inductor

R1 — Resistor Optional
RF Connectors — SMA Type
Board Material — Epoxy/Glass ε_r = 4.5,
Dielectric Thickness = 0.014″ (0.36 mm)

Figure 1. Typical Biasing Configuration

Table 1. Scattering Parameters for 900 MHz Two – Stage PA

(V_{CC1}, V_{CC2}, V_{BIAS} = 3 V, I = 49 mA, T_A = 25°C, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
50	0.739	–16.67	3.785	51.56	0.003	–163.12	0.461	–89.23
100	0.702	–24.53	5.772	46.52	0.001	15.96	0.354	–117.30
150	0.671	–33.09	7.901	40.16	0.001	84.34	0.263	–144.77
200	0.649	–41.55	10.065	32.12	0.001	–165.89	0.208	–167.08
250	0.630	–49.79	12.287	23.06	0.002	–159.68	0.169	170.65
300	0.610	–58.60	14.576	12.25	0.002	171.75	0.136	145.40
350	0.592	–67.09	16.834	1.32	0.003	–160.23	0.113	113.52
400	0.567	–75.32	19.009	–10.72	0.005	–167.93	0.105	73.18
450	0.537	–83.69	20.901	–23.88	0.005	167.71	0.122	33.86
500	0.495	–91.79	22.237	–37.89	0.007	159.88	0.157	2.30
525	0.470	–95.35	22.626	–45.02	0.007	168.37	0.178	–10.93
550	0.448	–98.65	22.821	–52.22	0.010	162.65	0.196	–22.73
575	0.421	–101.69	22.834	–59.20	0.009	159.52	0.216	–32.62
600	0.397	–104.40	22.647	–66.13	0.010	155.15	0.233	–42.62
625	0.371	–106.50	22.299	–73.01	0.011	151.24	0.246	–50.98
650	0.349	–108.28	21.813	–79.43	0.011	148.14	0.258	–59.21
675	0.329	–109.85	21.204	–85.70	0.012	145.35	0.269	–66.61
700	0.310	–111.02	20.538	–91.62	0.012	140.66	0.273	–73.29
725	0.293	–111.65	19.824	–97.20	0.014	136.88	0.280	–79.97
750	0.278	–112.24	19.094	–102.54	0.014	136.98	0.281	–85.86
775	0.265	–112.60	18.334	–107.76	0.014	134.67	0.285	–91.50
800	0.252	–112.81	17.594	–112.54	0.016	133.71	0.284	–96.72
825	0.242	–113.50	16.880	–117.13	0.015	129.16	0.282	–102.24
850	0.233	–114.93	16.127	–122.44	0.017	131.80	0.281	–107.68
875	0.224	–115.32	15.438	–126.92	0.017	126.66	0.279	–112.88
900	0.216	–116.04	14.796	–130.89	0.017	127.06	0.275	–117.56
925	0.210	–116.66	14.165	–134.57	0.018	121.77	0.273	–120.85
950	0.203	–117.91	13.555	–138.19	0.019	122.40	0.269	–125.53
975	0.195	–118.87	13.009	–141.73	0.019	120.80	0.265	–129.73
1000	0.191	–120.47	12.515	–145.08	0.019	122.53	0.265	–132.68
1025	0.186	–122.39	12.004	–148.23	0.020	119.56	0.259	–137.22
1050	0.179	–124.03	11.517	–151.36	0.022	115.24	0.254	–140.85
1075	0.175	–126.22	11.063	–154.40	0.022	117.88	0.251	–144.69
1100	0.168	–128.77	10.634	–157.40	0.024	112.04	0.248	–148.25
1125	0.163	–131.41	10.228	–160.15	0.023	112.42	0.246	–151.75
1150	0.161	–133.93	9.841	–163.04	0.023	115.77	0.245	–155.28
1175	0.155	–136.68	9.479	–165.88	0.025	110.34	0.241	–158.69
1200	0.152	–140.85	9.125	–168.50	0.025	109.94	0.241	–161.95

TYPICAL CHARACTERISTICS

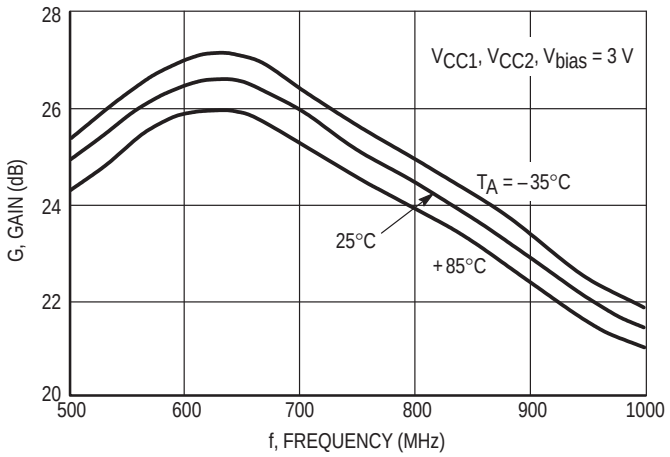


Figure 2. Gain versus Frequency

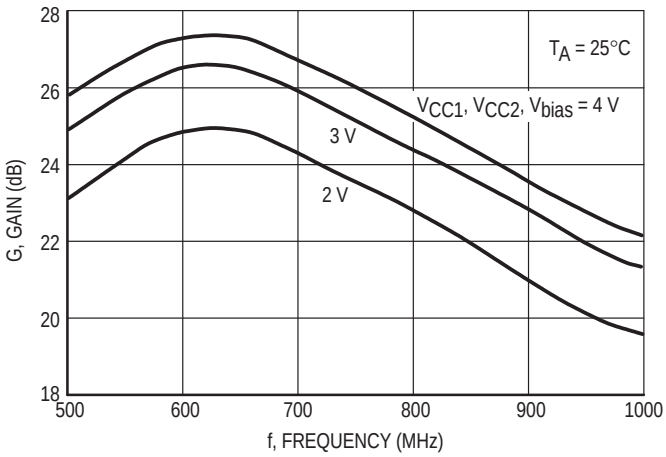


Figure 3. Gain versus Frequency

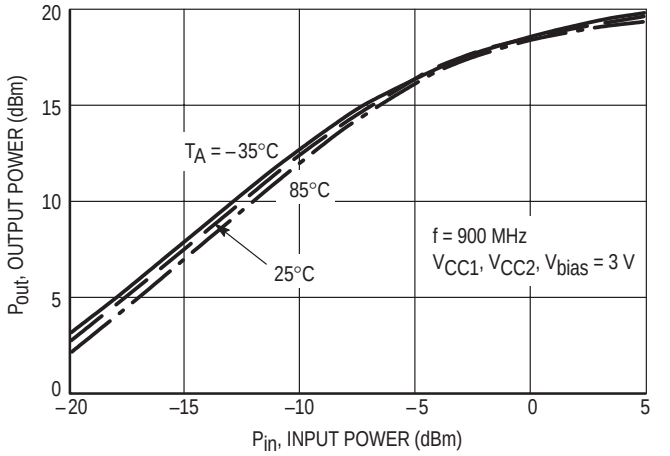


Figure 4. Output Power versus Input Power

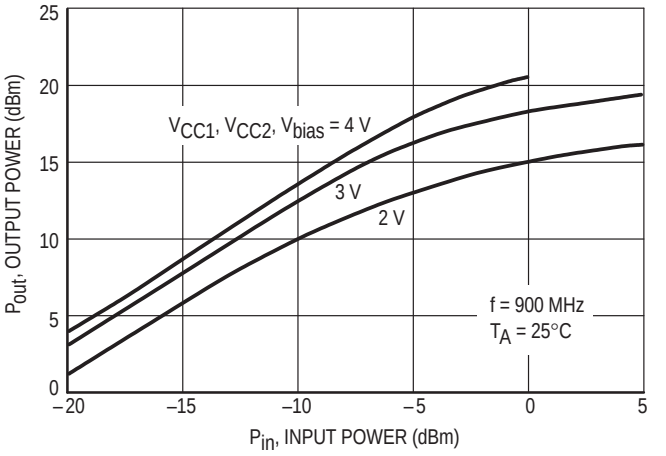


Figure 5. Output Power versus Input Power

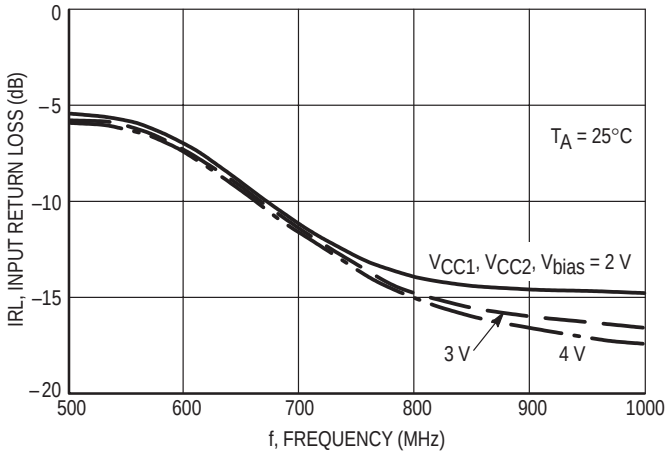


Figure 6. Input Return Loss versus Frequency

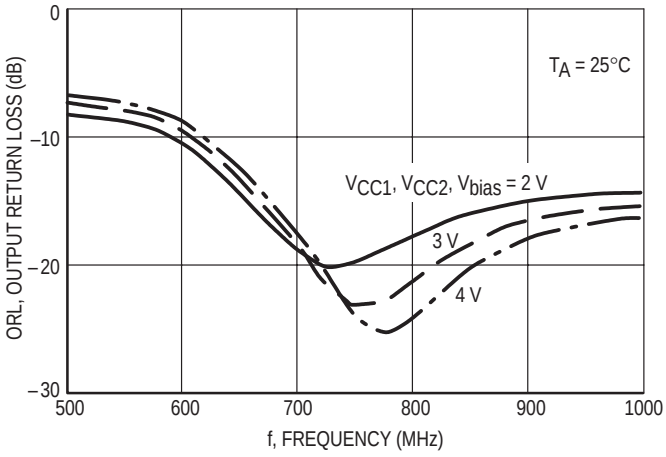


Figure 7. Output Return Loss versus Frequency

TYPICAL CHARACTERISTICS

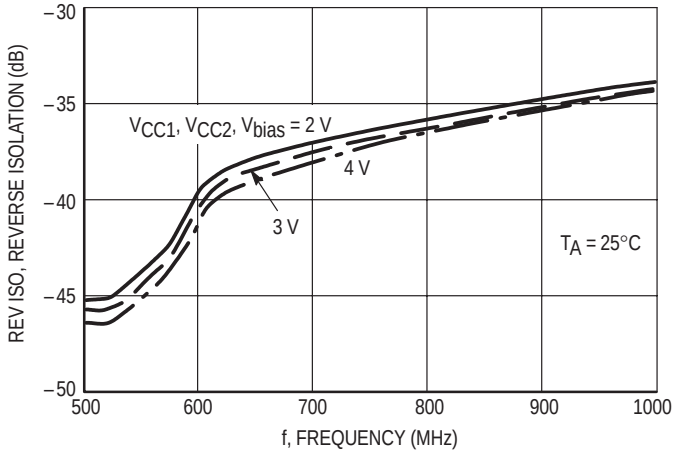


Figure 8. Reverse Isolation versus Frequency

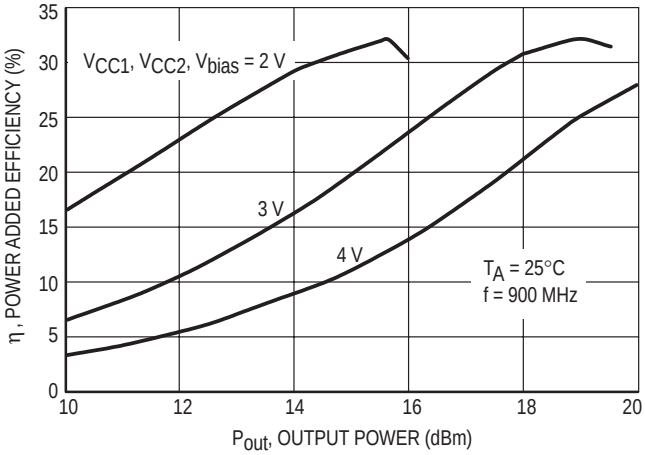


Figure 9. Power Added Efficiency versus Output Power

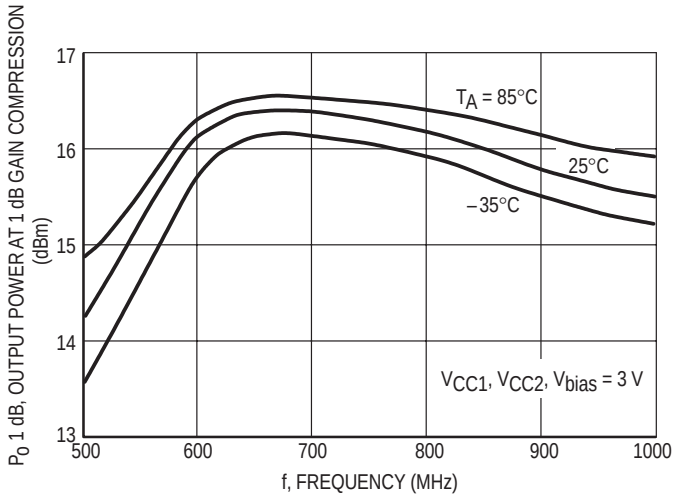


Figure 10. Output Power at 1 dB Gain Compression versus Frequency

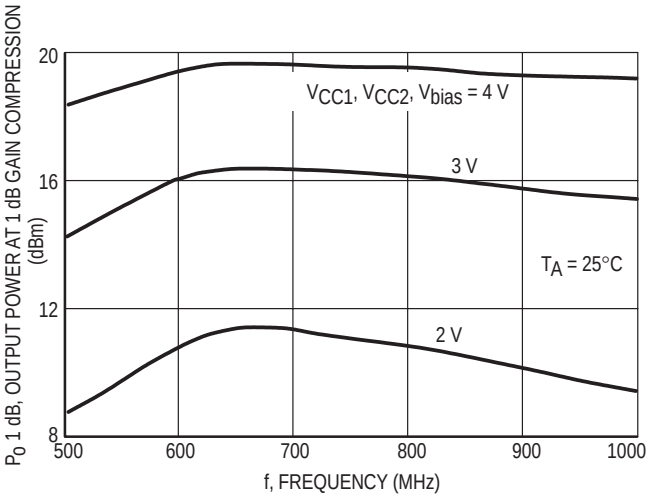


Figure 11. Output Power at 1 dB Gain Compression versus Frequency

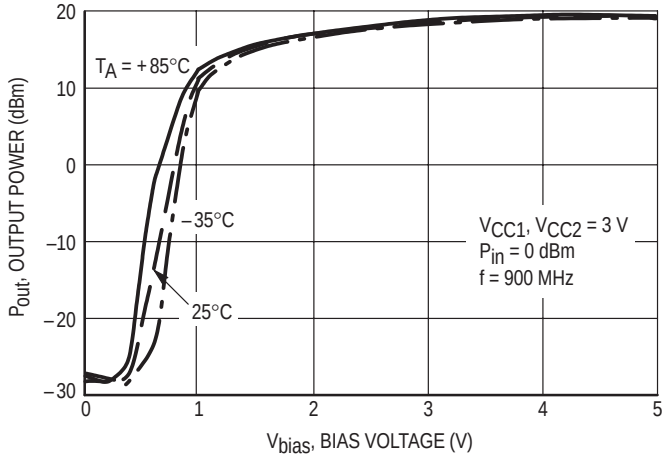


Figure 12. Output Power versus Bias Voltage

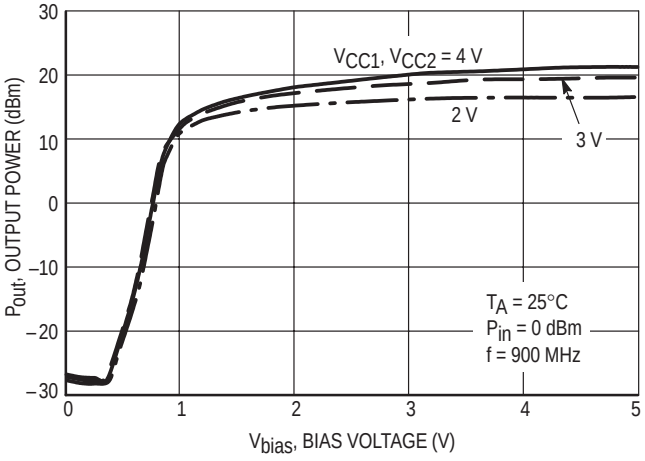


Figure 13. Output Power versus Bias Voltage

TYPICAL CHARACTERISTICS

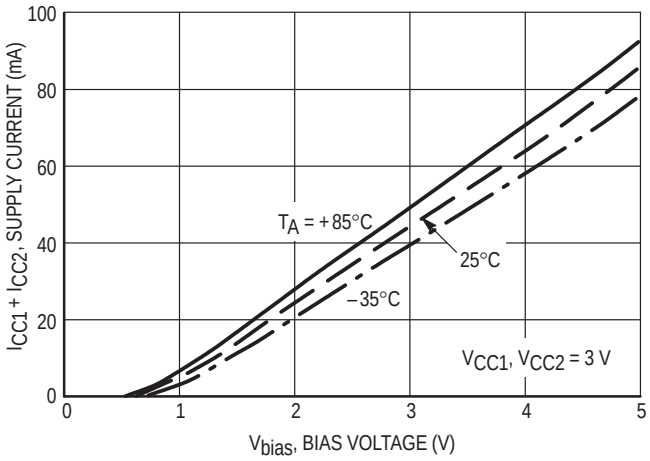


Figure 14. Supply Current versus Bias Voltage

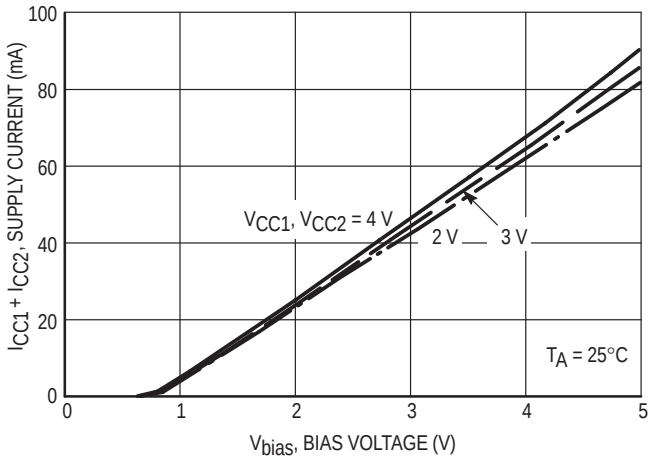


Figure 15. Supply Current versus Bias Voltage

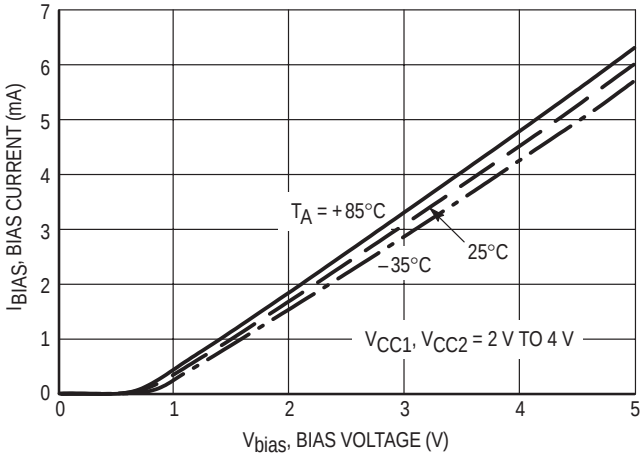


Figure 16. Bias Current versus Bias Voltage

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2006 was designed for low cost and flexibility. Low cost was achieved by minimizing external components and using an SOIC package. Flexibility was achieved by allowing the bias current to be externally adjustable resulting in a broad range of output power capability. The bias pin can be ramped to reduce AM splatter in TDD/TDMA systems and can be used to trim the RF output power.

THEORY OF OPERATION

The input port is internally matched to 50 ohms. Return loss is typically 15–16 dB in the 800–1000 MHz range. The output port is nearly 50 ohms but is an open collector and therefore requires an external bias inductor. Using an RF choke will result in a 11–12 dB output return loss. However, a 10 nH inductor will improve it to 15–20 dB. A 10 nH inductor is small enough in value to be printed on the board. DC blocks are required on the input and output. Values of 100 pF are recommended.

Supply decoupling must be done as close to the IC as possible. A 1000 pF capacitor is recommended. A series RF choke is recommended to keep the RF signal off the supply line. A 10 nF decoupling capacitor is recommended on the V_{bias} line but does not need to be very close to the IC.

The V_{bias} pin can be used several ways. Tying it directly to V_{CC} will maximize the bias current which will maximize linearity. Adding a series resistor will reduce the bias current which will improve efficiency. Figure 9 shows the efficiency versus output power with V_{bias} tied to V_{CC}. The series resistor will cause these curves to shift to the left. The RF output power can be trimmed by using a variable resistor. The V_{bias} pin can also be used to power down the IC or, in the case of TDD/TDMA systems, to ramp the IC. By applying a linear ramp voltage, such as the one provided by the MRFIC2004, it has been demonstrated to meet the CT2 Common Air Interface splatter specifications.

The MRFIC2006 is internally temperature compensated. For input powers of –5.0 to 0 dBm the output power temperature variation is typically less than 0.2 dB from –35 to +85°C.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

Chapter Three
RF/IF Subsystem ICs

Section One 3.1–0
RF/IF Subsystem ICs – Selector Guide

Section Two 3.2–0
RF/IF Subsystem ICs – Data Sheets

Section One
Selector Guide

RF/IF Subsystems

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Receivers	3.1–2
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Encoders/Decoders	3.1–4
Packages	3.1–5

RF/IF Subsystems

Cordless Phone Subsystem ICs

Device	V_{CC}	I_{CC} (Typ)	Dual Conversion Receiver	Universal Dual PLL	Compander and Audio Interface	CVSD Compatible	Low Battery Detect	Notes	Suffix/ Case No.
MC13109A	2.0 to 5.5 V	Active Mode 6.7 mA Inactive Mode 40 µA	✓	✓	✓	–	✓	CT–0	FB/848B, FTA/932
MC13110A	2.7 to 5.5 V	Active Mode 8.5 mA Inactive Mode 15 µA	✓	✓	✓	–	✓	CT–0	FB/848B FTA/932
MC13111A	2.7 to 5.5 V	Active Mode 8.5 mA Inactive Mode 15 µA	✓	✓	✓	–	✓	CT–0	FB/848B, FTA/932
MC13145	2.7 to 6.5 V	Active Mode 27 mA Inactive Mode 10 µA	✓	–	–	✓	–	Receiver with coilless demod CT–900	FTA/932
MC13146	2.7 to 6.5 V	Active Mode 18 mA Inactive Mode 10 µA	–	–	–	✓	–	Transmitter with VCO CT–900	FTA/977
MC33410	2.7 to 5.5 V	Active Mode 13 mA Inactive Mode 10 µA	✓	✓	–	✓	✓	Digital Baseband CT–900	FTA/932
MC33411A MC33411B	2.7 to 5.5 V	Active Mode 15 mA Inactive Mode 10 µA	✓	✓	✓	–	✓	Analog Baseband CT–900	FTA/932

GPS Subsystem ICs

Device	RF Freq (MHz)	IF Freq (MHz)	V_{CC} (V)	I_{CC} (mA) (Typ)	Dual Conversion Receiver	Dual Loop PLL	Limiting Amplifier	Variable Gain IF Amplifier	Case No.
MRFIC1502	1575	9.5	4.5 to 5.5	52	✓	✓	–	–	932
MRFIC1504	1575	4.1	2.7 to 3.3	28	✓	✓	✓	✓	932

Receivers

Device	V_{CC}	I_{CC} (Typ)	Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Case No.
MC2800	1.1 to 3.0 V	1.5 mA	–110 dBm	75 MHz	455 kHz	–	✓	>1.2 kb	Pager Applications	FTA/873C
MC3356	3.0 to 9.0 V	20 mA	30 µV	150 MHz	10.7 MHz	✓	–	500 kb	Includes front end mixer/L.O.	DW/751D

Receivers (continued)

Device	V_{CC}	I_{CC} (Typ)	Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Case No.
MC3361B	2.0 to 8.0 V	3.9 mA	2.6 µV	60 MHz	455 kHz	✓	–	>4.8 kb	Squelch and Scan	D/751B
MC3361C	2.0 to 8.0 V	2.8 mA				✓	–			D/751B
MC3371	2.0 to 9.0 V	3.6 mA	1.0 µV	100 MHz			✓ 60 dB		RSSI	D/751B, DTB/948F
MC3372									RSSI, Ceramic Quad Detector/Resonator	
MC3374	1.1 to 3.0 V	1.6 mA	0.5 µV	75 MHz		–	–		Low Battery Detect	FTB/873
MC13135	2.0 to 6.0 V	4.0 mA	1.0 µV	200 MHz	10.7 MHz/ 455 kHz	–	✓ 70 dB	>4.8 kb	Voltage Buffered RSSI, LC Quad Detector	DW/751E, P/724
MC13136									Voltage Buffered RSSI, Ceramic Quad Detector	DW/751E
MC13150	2.5 to 6.0 V	1.7 mA	2.0 µV	500 MHz		✓	✓ 110 dB	>9.6 kb	Coilless Detector with Adjustable Bandwidth	FTB/873, FTA/977
MC13156	2.0 to 6.0 V	5.0 mA	2.0 µV	500 MHz	21.4 MHz	–	✓ 80 dB	500 kb	CT–2 FM/Demodulator	DW/751E, FB/873
MC13158	2.0 to 6.0 V	6.0 mA		500 MHz				>1.2 Mb	FM IF/Demodulator with split IF for DECT	FTB/873

IFs

Device	V_{CC}	I_{CC} (Typ)	Sensitivity (Typ)	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Case No.
MC13055	3.0 to 12 V	20 mA	20 µV	40 MHz	✓	✓	2.0 Mb	Wideband Data IF, includes data shaper	D/751B
MC13155	3.0 to 6.0 V	7.0 mA	1.0 mV	250 MHz	–		10 Mb	Video Speed FM IF	D/751B

Transmitters

Device	V_{CC}	I_{CC} (Typ)	P_{out}	Max RF Freq Out	Max Mod Freq	Notes	Suffix/ Case No.
MC13176	2.0 to 5.0 V	40 mA	10 dBm	1.0 GHz	5.0 MHz	$f_{out} = 32 \times f_{ref}$, includes power down function, AM/FM Modulation	D/751B

Miscellaneous Functions

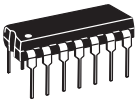
ADCs/DACs

Device	Function	I/O Format	Resolution	Number of Analog Channels	On–Chip Oscillator	Other Features	Suffix/ Case No.
MC144110	DAC	Serial	6 Bits	6	–	Emitter–Follower Outputs	DW/751D
MC144111				4			DW/751G
MC145050	ADC		10 Bits	11	–	Successive Approximation	P/738, DW/751D
MC145051					✓		
MC145053				5			P/646, D/751A

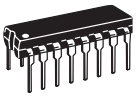
Encoders/Decoders

Device	Function	Number of Address Lines	Maximum Number of Address Codes	Number of Data Bits	Operation	Suffix/ Case No.
MC145026	Encoder	Depends on Decoder	Depends on Decoder	Depends on Decoder	Simplex	P/648, D/751B
MC145027	Decoder	5	243	4	Simplex	P/648, DW/751G
MC145028		9	19,683	0	Simplex	

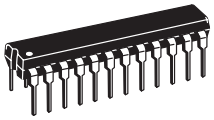
RF/IF Subsystems Packages



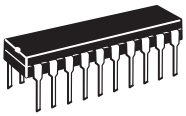
CASE 646
P SUFFIX
(DIP–14)



CASE 648
P SUFFIX
(DIP–16)



CASE 724
P SUFFIX
(DIP–24)



CASE 738
P SUFFIX
(DIP–20)



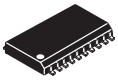
CASE 751
D SUFFIX
(SO–8)



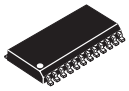
CASE 751A
D SUFFIX
(SO–14)



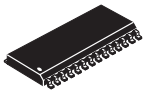
CASE 751B
D SUFFIX
(SO–16)



CASE 751D
DW SUFFIX
(SO–20L)



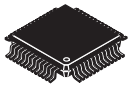
CASE 751E
DW SUFFIX
(SO–24L)



CASE 751F
DW SUFFIX
(SO–28L)



CASE 751G
DW SUFFIX
(SO–16W)



CASE 848B
FB SUFFIX
(QFP–52)



CASE 873
FB, FTB SUFFIX
(LQFP–32)



CASE 873C
FTA SUFFIX
(LQFP–32)



CASE 932
FTA SUFFIX
(LQFP–48)



CASE 948D
DT SUFFIX
(TSSOP–20)



CASE 948F
DTB SUFFIX
(TSSOP–16)



CASE 977
FTA SUFFIX
(LQFP–24)

Section Three

RF/IF Subsystems – Data Sheets

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MC13111A	3.2–104
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MC13146	3.2–196
MC33410	3.2–299
MC33411A, B	3.2–324
DRSEVS1	3.2–423
GPS Subsystems	
MRFIC1502	3.2–414
MRFIC1504	3.2–419
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MC2800	3.2–3
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MC3372	3.2–47
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MC13158	3.2–260
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MC13155	3.2–227
Transmitters	
MC13176	3.2–282

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MC144111	3.2–365
MC145050	3.2–388
MC145051	3.2–388
MC145053	3.2–401
Encoders/Decoders	
MC145026	3.2–371
MC145027	3.2–371
MC145028	3.2–371

MOTOROLA

MC2800

Advance Information

FSK FM IF Receiver BiCMOS

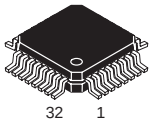
MC2800 is a high performance M–ary FSK FM IF Receiver for FLEX™ pagers. The circuit includes oscillator, mixer, IF amplifier, limiting IF circuitry, RSSI, quadrature discriminator, switchable bitrate filter, peak detector and A/D converter.

- 2/4 Level FSK Comparator and A/D Converter
- Fully Adaptive Data Slicer
- Coilless and Resonatorless Demodulator
- Current Consumption: 1.5 mA Typical
- Operating Voltage: V_{CC} = 1.1 to 3.0 V, V_{DD} = 1.1 to 3.0 V
- Input Bandwidth: 75 MHz
- Excellent Sensitivity: –110 dBm
- Switchable Bitrate Filter up to 6400 b/s Data Rate
- Start–up Time: 5.0 ms
- 1.0 V Regulator with Source Capability of 5.0 mA Typical
- RSSI Function
- Low Battery Detector
- Small Package 5 x 5 32–Pin LQFP

FLEX is a trademark of Motorola, Inc.

FSK FM IF RECEIVER
BiCMOS INTEGRATED CIRCUIT

SEMICONDUCTOR
TECHNICAL DATA

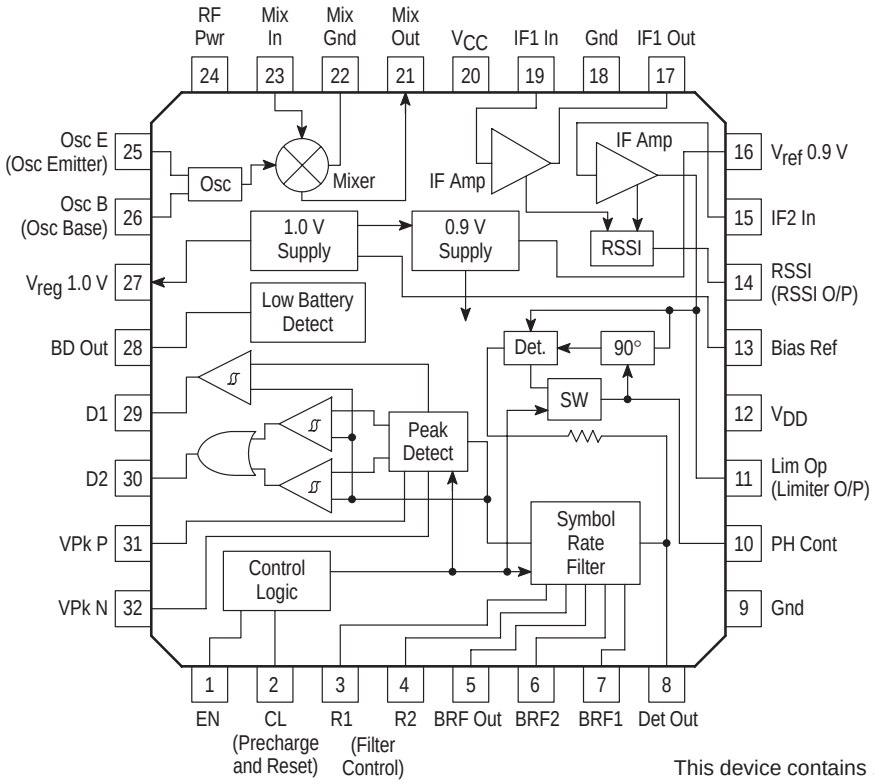


FTA SUFFIX
PLASTIC PACKAGE
CASE 873C
(LQFP–32)

ORDERING INFORMATION

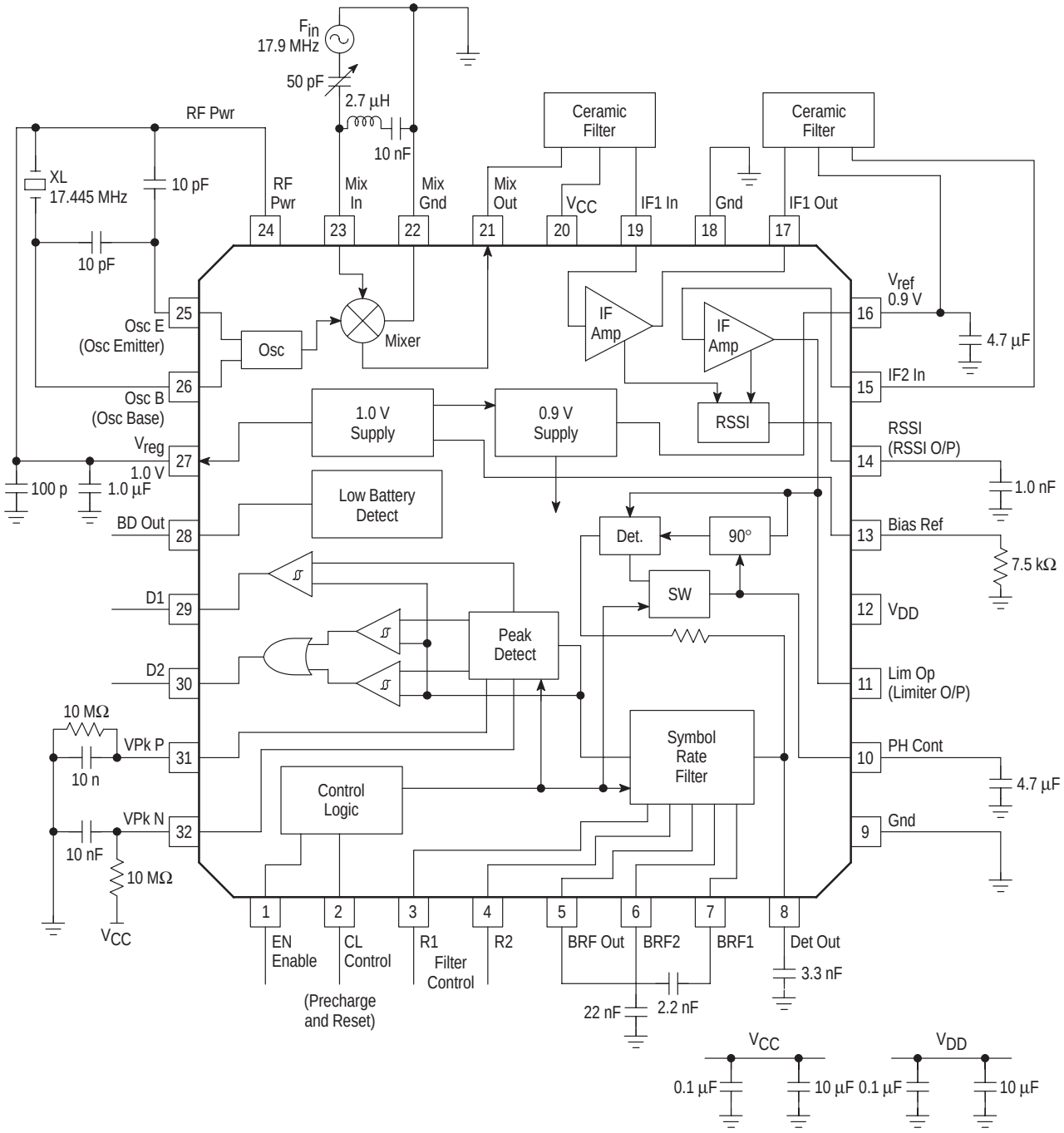
Device	Operating Temperature Range	Package
MC2800FTA	T_A = –10 to 75°C	LQFP–32

Representative Block Diagram



This device contains 1241 active transistors.

Figure 1. Typical Application Circuit for F_{in} = 17.9 MHz



MAXIMUM RATINGS

Rating	Condition	Symbol	Value	Unit
Power Supply Voltage	–	$V_{CC(max)}$ $V_{DD(max)}$	5.0 5.0	V
Junction Temperature	–	T_{JMAX}	150	°C
Storage Temperature	–	T_{stg}	–65 to 150	°C

NOTES: 1. Meets Human Body Model (HBM) ≤2000 V and Machine Model (MM) ≤200 V.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Condition	Symbol	Value	Unit
Power Supply Voltage 1	–	V_{CC}	1.1 to 3.0	V
Power Supply Voltage 2	[Note]	V_{DD}	1.1 to 3.0	V
Input Frequency at Mix In	–	f_{in}	10 to 75	MHz
Ambient Temperature Range	–	T_A	–10 to 75	°C

NOTE: V_{DD} is equal or greater than V_{CC}.

SYSTEM PERFORMANCE CHARACTERISTICS

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
Supply Voltage 1 [Note]	–	V_{CC}	1.1	1.4	3.0	V
Supply Voltage 2 [Note]	–	V_{DD}	1.1	1.8	3.0	V
Current 1	V_{CC} = 1.1 V	I_{CC}	–	1.5	1.7	mA
Current 2	V_{DD} = 1.8 V	I_{DD}	5.0	20	50	µA
Stand–By Current (“off”)	Disable (EN = “L”)	$I_{CC} + I_{DD}$	–	0	2.0	µA
Mixer Input Sensitivity	BER ≤ 1/100; f_{RF} = 17.9 MHz; Data Rate 6400 Bits/s; T_A = 25°C	Sens	–	–	–110	dBm
Detection Threshold for Battery “Low” Indicator	–	V_{th}	–	1.1	1.15	V
Ambient Temperature	–	T_A	–10	–	75	°C

NOTE: V_{DD} is equal or greater than V_{CC}.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 1.1 V, V_{DD} = 1.8 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
Total Current 1	Active (EN = “H”)	I_{CC}	–	1.5	1.7	mA
Total Current 2	Active (EN = “H”)	I_{DD}	5.0	20	50	µA
Total Current 3	Disable (EN = “L”)	$I_{CC} + I_{DD}$	–	–	2.0	µA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 1.1 V, V_{DD} = 1.1 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
MIXER (RF Pwr @ 1.0 V)						
Mixer Conversion Gain	Without Load With 1.5 kΩ Load (Ceramic Filter)	G_{max} G_{max}	– –	12 6.0	– –	dB
Maximum Input Level at Mix In	–	V_{im}	–	–15	–	dBm
Third Order Intercept Point	@ Mix In	IIP_3	–	–25	–	dBm
1.0 dB Gain Compression Level	@ Mix In	P_{1dB}	–	–35	–	dBm
Input Impedance	–	R_p	–	2.0	–	kΩ
Maximum Input Frequency	@ Mix In	f_{max}	75	–	–	MHz
Noise Figure @ Mix Out	Frequency = 17.9 MHz	NF1	–	12	–	dB

AC ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 1.1 V, V_{DD} = 1.1 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
OSCILLATOR (RF Pwr @ 1.0 V)						
Input Impedance (DC)	@ Osc B	R_{in}	–	15	–	kΩ
Signal Level at Osc B	–	$V_{Osc\ B}$	–	300	–	mVpp
IF AMP (First IF Amplifier)						
Gain	V_{CC} = 1.1 V; 455 kHz; AC Coupling	G_{IF1}	–	45	–	dB
Bandwidth		BW	–	25	–	kHz
Noise Figure		NF	–	18	–	dB
I/P Impedance		–	–	1.5	–	kΩ
O/P Impedance		–	–	1.5	–	kΩ
1.0 dB Compression		–	–	–70	–	dBm
IF AMP (Second IF Amplifier)						
Gain	V_{CC} = 1.1 V; 455 kHz; AC Coupling	G_{IF2}	–	69	–	dB
I/P Impedance		–	–	1.5	–	kΩ
Output Level		Lim Op	–	5.0	10	mVpp
RSSI						
Dynamic Range	–	–	40	–	–	dB
Output Impedance	@ RSSI	R_{rs}	–	50	–	kΩ
RSSI Output Voltage	–	V_{rs}	0	–	V_{CC}	V
RSSI Output Slope	@ RF_{in} = –80 dBm	V_{rs}	–	18	–	mV/dB
OVERALL WITH DETECTOR (@ BRF Out)						
12 dB Sensitivity (SINAD)	–	SINAD	–	–112	–	dBm
Recovered Audio	–	V_{au}	–	300	–	mVpp
Noise Output Level	Input Carrier Only	V_{no}	–	10	–	mVrms
CHARGE TIME						
Charge Time (See Figure 4)	CL = “L” to “H” EN = “H”	t_{ch}	–	5.0	6.0	ms
DATA COMPARATORS (D1, D2)						
Rise and Fall Time	f_{in} = 600 Hz	t_r, t_f	–	5.0	10	μs
Duty Cycle	D1, D2	–	–	50	–	%
Output High Voltage	R_L = 100 kΩ	V_{oh1}	V_{DD} – 0.3	–	–	V
Output Low Voltage	R_L = 100 kΩ	V_{ol1}	–	–	0.2	V
BIT RATE LOW PASS FILTER CUT–OFF FREQUENCY						
Cut–Off Frequency 1 (512 bps) [Note]	(R1, R2) = (0, 0)	f_{cl1}	350	410	480	Hz
Cut–Off Frequency 2 (1200 bps) [Note]	(R1, R2) = (1, 0)	f_{cl2}	820	960	1100	Hz
Cut–Off Frequency 3 (1600 bps) [Note]	(R1, R2) = (1, 1)	f_{cl3}	1100	1280	1480	Hz
Cut–Off Frequency 4 (3200 bps) [Note]	(R1, R2) = (0, 1)	f_{cl4}	2180	2560	2950	Hz

NOTE: Cut–off frequency is depending on the two external capacitors connected between BRF1, BRF Out, BRF2 and ground. The respective values are 2.2 nF ±1% and 22 nF ±1%.

AC ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 1.1 V, V_{DD} = 1.1 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
AUDIO OUTPUT (@ Det Out)						
Output Level 1	f_{dev} = ±4.5 kHz, f_{mod} = 600 Hz	V_{au1}	–	100	–	mVpp
Output Level 2	f_{dev} = ±4.8 kHz, f_{mod} = 800 Hz	V_{au2}	–	120	–	mVpp
Output Level 3	f_{dev} = ±4.8 kHz, f_{mod} = 1.6 kHz	V_{au3}	–	120	–	mVpp
BATTERY DETECT (Active Low)						
Threshold Voltage	–	V_{th}	–	1.1	1.15	V
Output High Voltage	R_L = 100 kΩ	V_{oh2}	V_{DD} – 0.3	–	–	V
Output Low Voltage	R_L = 100 kΩ	V_{ol2}	–	–	0.3	V
1.0 V VOLTAGE REGULATOR						
Output Voltage	No Load	V_{reg}	0.95	1.0	1.05	V
External Source Capability	V_{reg} = 0.95 V	I_{Smax}	–	5.0	–	mA
0.9 V VOLTAGE REGULATOR						
Output Voltage	No Load	V_{ref}	0.85	0.9	0.95	V
External Source Capability	V_{ref} = 0.9 V	I_{Smax}	–20	100	300	µA
INPUT PIN DC CHARACTERISTICS						
Input Voltage Low	R1, R2	V_{il1}	–	–	0.3	V
Input Voltage High	R1, R2	V_{ih1}	V_{DD} – 0.3	–	–	V
Input Voltage Low	CL	V_{il2}	–	–	0.3	V
Input Voltage High	CL	V_{ih2}	V_{DD} – 0.3	–	–	V
Input Voltage Low	EN	V_{il3}	–	–	0.3	V
Input Voltage High	EN	V_{ih3}	V_{DD} – 0.3	–	–	V

SYMBOL/BAUD RATE FILTER SELECTION

R1	R2	
L	L	512 POCSAG (Baud Per Second), 2 Levels
H	L	1200 POCSAG (Baud Per Second), 2 Levels
H	H	1600 FLEX (Symbol Per Second), 2/4 Levels
L	H	3200 FLEX (Symbol Per Second), 2/4 Levels

ENABLE (BATTERY SAVE FUNCTION)

Enable	
H	Active
L	Disable (Battery Saving)

CONTROL (CIRCUIT MODE FUNCTION)

Control	
H	Reset Mode
L	Normal Operation Mode

BD Out WITH 100 kΩ (LOW BATTERY DETECTOR)

BD Out	
H	Low Battery
L	–

D1 WITH 100 kΩ (D1)

D1	
H	Dev –4.8 kHz or Dev –1.6 kHz
L	Dev 1.6 kHz or Dev 4.8 kHz

D2 WITH 100 kΩ (D2)

D2	
H	Dev ±1.6 kHz
L	Dev ±4.8 kHz

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in the Block Diagram on page 1.

Oscillator

The oscillator is based on a transistor in common collector configuration. It requires two external capacitors and a crystal to form the tank circuit. External capacitors between base and emitter and from emitter to RF Pwr make the oscillator transistor to have a negative resistance for small signals which is the start–up condition for oscillation.

Mixer

The mixer consists of input v–to–i stage and upper switching stage driven from the oscillator. The LO drive is fed from the built–in oscillator. The mixer output is obtained at Mix Out.

IF Amplifier and Limiter

The first ceramic filter is to obtain the 455 kHz IF and to remove all other harmonics from the mixing process. The mixer output signal is then amplified in the first IF Amplifier. The signal is then fed into the second IF Amplifier through the second ceramic filter. The final IF signal can be monitored at the limiter output pin Lim Op.

RSSI function

The RSSI function is an indication of the strength of the incoming signal.

Demodulator

The limiter output @ 455 kHz is fed into the gyrator for carrier recovery and 90° phase shift. This LO signal is then mixed with the FSK signal fed by the IF Amp for demodulation. The demodulator output can be obtained at Det Out.

Bit–Rate Filter

The cut–off frequencies of the filter can be determined by the 2.2 nF external capacitor between Pins BRF Out and BRF1, and the 22 nF external capacitor at Pin BRF2. The filter bandwidth can be switched by Pins R1 and R2 for both POCSAG and FLEX requirements.

A/D Convertor

The A/D converter features a fully adaptive data slicer. The input to the converter at Pin BRF Out is initially peak–detected. Its peak and valley voltages are obtained at Pins VPk P and VPk N. Three threshold voltages at 1/6, 1/2 and 5/6 of the input signal level are determined dynamically regardless the actual peak–to–peak value. The final digital data are obtained at Pins D1 and D2 depending upon the 2 or 4 levels FSK signal.

Low Battery Detector

The battery low indicator senses the supply voltage and sets its output High when the voltage at input V_{CC} is less than V_{th} (typically 1.1 V).

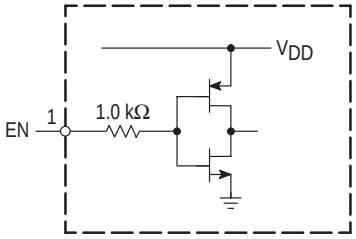
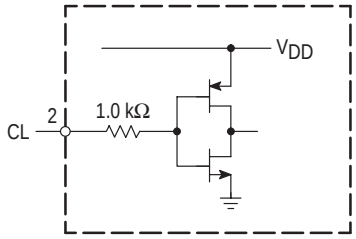
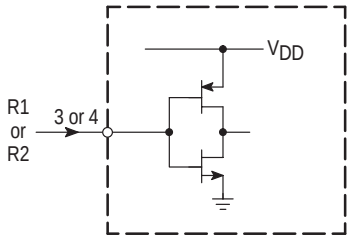
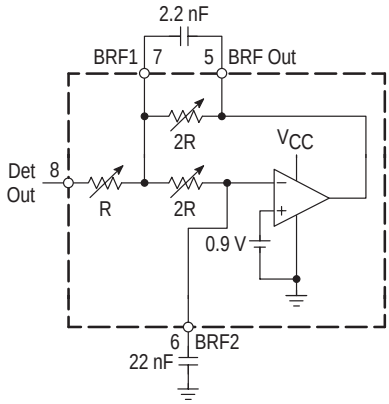
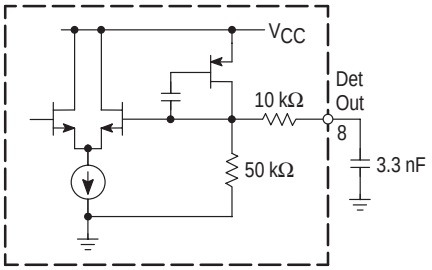
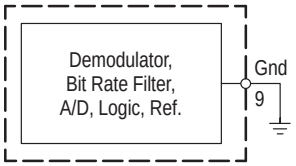
Band Gap Reference

The whole chip can be powered–up and powered–down by enabling and disabling the band gap reference via the Pin EN (Enable).

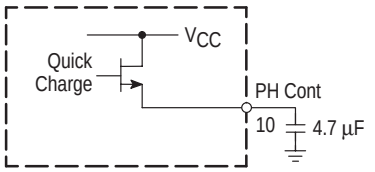
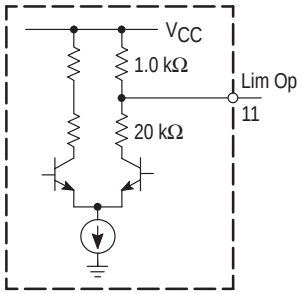
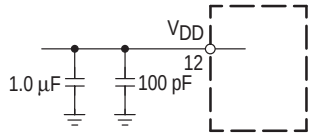
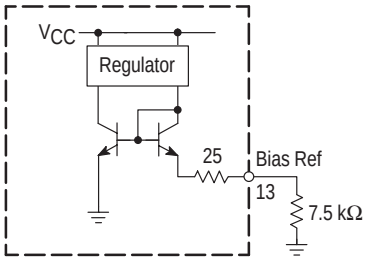
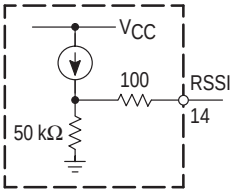
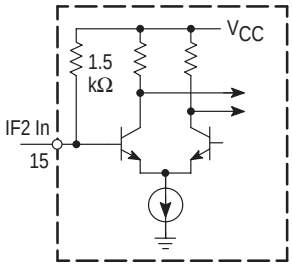
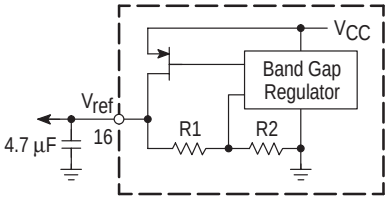
1.0 V Regulator

The 1.0 V voltage at Pin V_{reg} is used to supply the regulated voltage for the oscillator and the mixer. It can also be used to supply other external circuits.

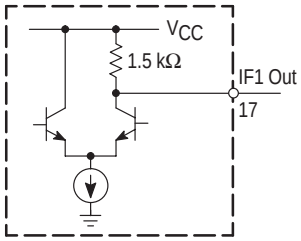
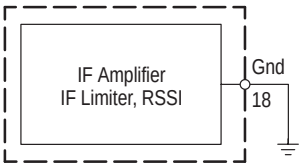
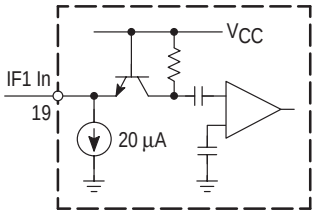
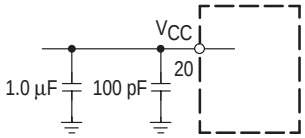
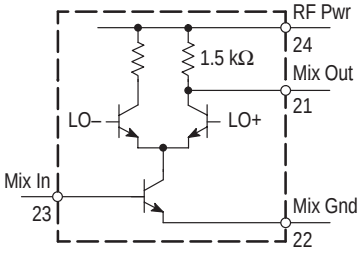
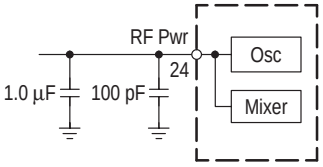
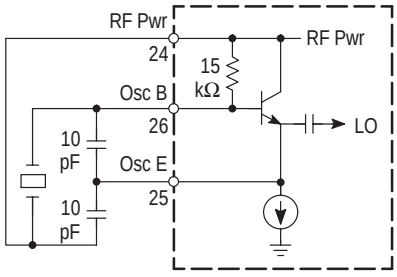
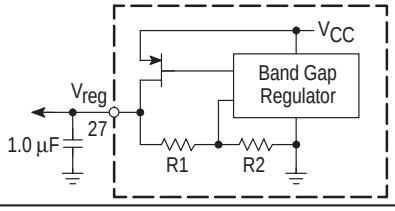
PIN FUNCTION DESCRIPTION

Pin	Symbol	Schematic (Excluding ESD)	Description
1	EN		Enables the circuit.
2	CL (Precharge and Reset)		This pin is used to precharge the circuit to accelerate the initial start–up process (particularly the 4.7 μF capacitor at Pin 10).
3 4	R1 R2		These pins are set to “high” or “low”. They are used for the selection of the filter’s symbol rate.
5	BRF Out		Symbol Rate Filter Output for connection of feedback capacitor. This is also the audio output before A/D.
6	BRF2		Symbol Rate Filter Input for connection of filter capacitor.
7	BRF1		Symbol Rate Filter Input.
8	Det Out		Audio output from FSK FM detector. This pin is also audio input for testing purposes (signal of 100 mVpp with DC offset of 0.9 V).
9	Gnd		Ground pin for IC covering Pins 1 through 13 and 27 through 32.

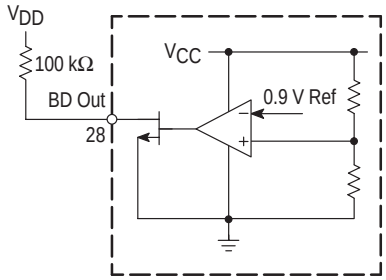
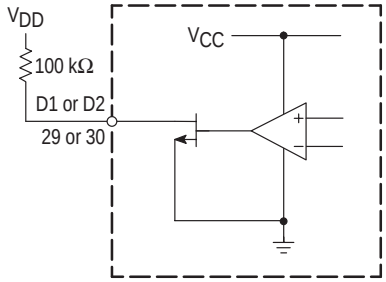
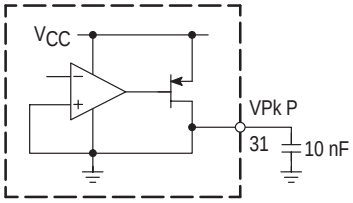
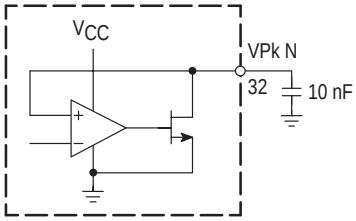
PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Schematic (Excluding ESD)	Description
10	PH Cont		This Phase Detector Control pin is connected to a 4.7 µF capacitor. It is precharged to 0.9 V during initial start–up (when the CTL signal is high).
11	Lim Op		IF Amp/Limiter Output (small signal 5.0 mVpp typical). (For test purpose only.)
12	V_{DD}		Digital Power Supply. V_{DD} can be greater or equal to V_{CC}.
13	Bias Ref		A 7.5 k resistor is connected to this pin for bias the reference of the gyrator filter included in the demodulator block.
14	RSSI		Receive Signal Strength Indicator. It should be decoupled with a small capacitor.
15	IF2 In		Signal input for second IF Amplifier/Limiter.
16	V_{ref} 0.9 V		0.9 V reference for internal use only. Minimum 4.7 µF capacitor required for decoupling. Not recommended for external use. (Do not draw current from it.)

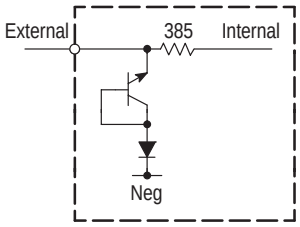
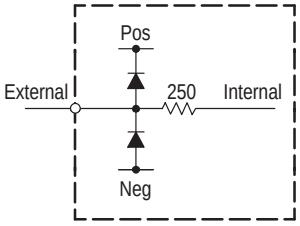
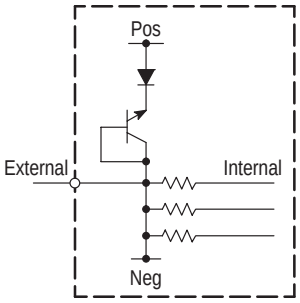
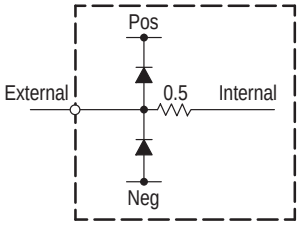
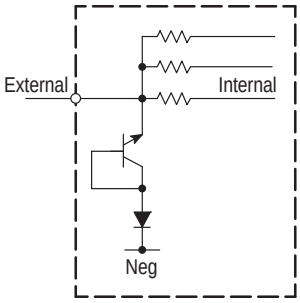
PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Schematic (Excluding ESD)	Description
17	IF1 Out		First IF Amplifier output.
18	Gnd		Ground pin for IC covering Pins 14 through 20.
19	IF1 In		First IF Amplifier input.
20	V_{CC}		Main Analog Power Supply for the circuit.
21	Mix Out		Mixer Output.
22	Mix Gnd		Ground pin for the RF Part.
23	Mix In		Mixer input relative to Pin 22.
24	RF Pwr		Power Supply for the RF part. It is not internally connected to the other Power Supply. It must be connected externally to V_{reg} 1.0 V, with the appropriate decoupling.
25 26	Osc E Osc B		These pins form the reference oscillator when connected to an external parallel–resonant crystal (17.445 MHz typical).
27	V_{reg} 1.0 V		1.0 V regulator output. Minimum 1.0 µF capacitor required for decoupling. It can supply up to 3.0 mA for external use.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Schematic (Excluding ESD)	Description
28	BD Out		Low Battery Detector Output (open collector requires external pull–up resistor typically at 100 kΩ.). It toggles with V_{CC} at 1.1 V typical.
29 30	D1 D2		Digital output of data slicers D1 and D2 (A/D converter). It is an open collector and requires an external pull–up resistor typically at 100 kΩ.
31	VPk P		Peak Detector Output voltage of peak. It can be monitored with a high impedance (FET) probe.
32	VPk N		Peak Detector Output voltage of valley. It can be monitored with a high impedance (FET) probe.

ESD PROTECTION SCHEMATIC

Pin	Symbol	Type	Schematic
1	EN	Digital Input (385 Ω)	
2	CL		
3	R1		
4	R2		
5	BRF Out	Analog Input/Output (250 Ω)	
6	BRF2		
7	BRF1		
8	Det Out		
9	Gnd	Gnd (0 Ω)	
10	PH Cont	Analog Output (0 Ω)	
11	Lim Op	Analog (250 Ω)	Same as Pin 5
12	V_{DD}	Power Input (High Voltage) (0 Ω)	
13	Bias Ref	Analog (250 Ω)	Same as Pin 5
14	RSSI	Analog (250 Ω)	Same as Pin 5
15	IF2 In	Analog (250 Ω)	Same as Pin 5
16	V_{ref} 0.9 V	Power (0 Ω)	Same as Pin 12
17	IF1 Out	Analog (250 Ω)	Same as Pin 5
18	Gnd	Gnd (0 Ω)	Same as Pin 9
19	IF1 In	Analog (250 Ω)	Same as Pin 5

ESD PROTECTION SCHEMATIC (continued)

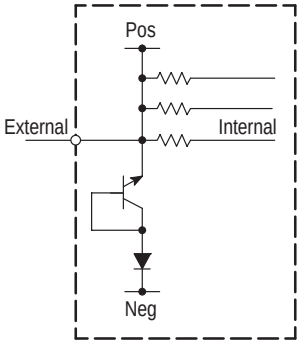
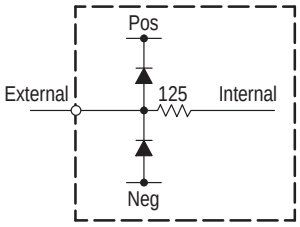
Pin	Symbol	Type	Schematic
20	V_{CC}	Supply Input (0 Ω)	
21	Mix Out	Analog (250 Ω)	Same as Pin 5
22	Mix Gnd	Gnd (0 Ω)	Same as Pin 9
23	Mix In	RF Input (125 Ω)	
24	RF Pwr	Supply (0 Ω)	Same as Pin 20
25	Osc E	Analog (250 Ω)	Same as Pin 5
26	Osc B	Analog (250 Ω)	Same as Pin 5
27	V_{reg} 1.0 V	Power (0 Ω)	Same as Pin 12
28	BD Out	Power (0 Ω)	Same as Pin 12
29	D1	Power (0 Ω)	Same as Pin 12
30	D2	Power (0 Ω)	Same as Pin 12
31	VPk P	Analog (250 Ω)	Same as Pin 5
32	VPk N	Analog (250 Ω)	Same as Pin 5

Figure 2. Data Slicer Operation

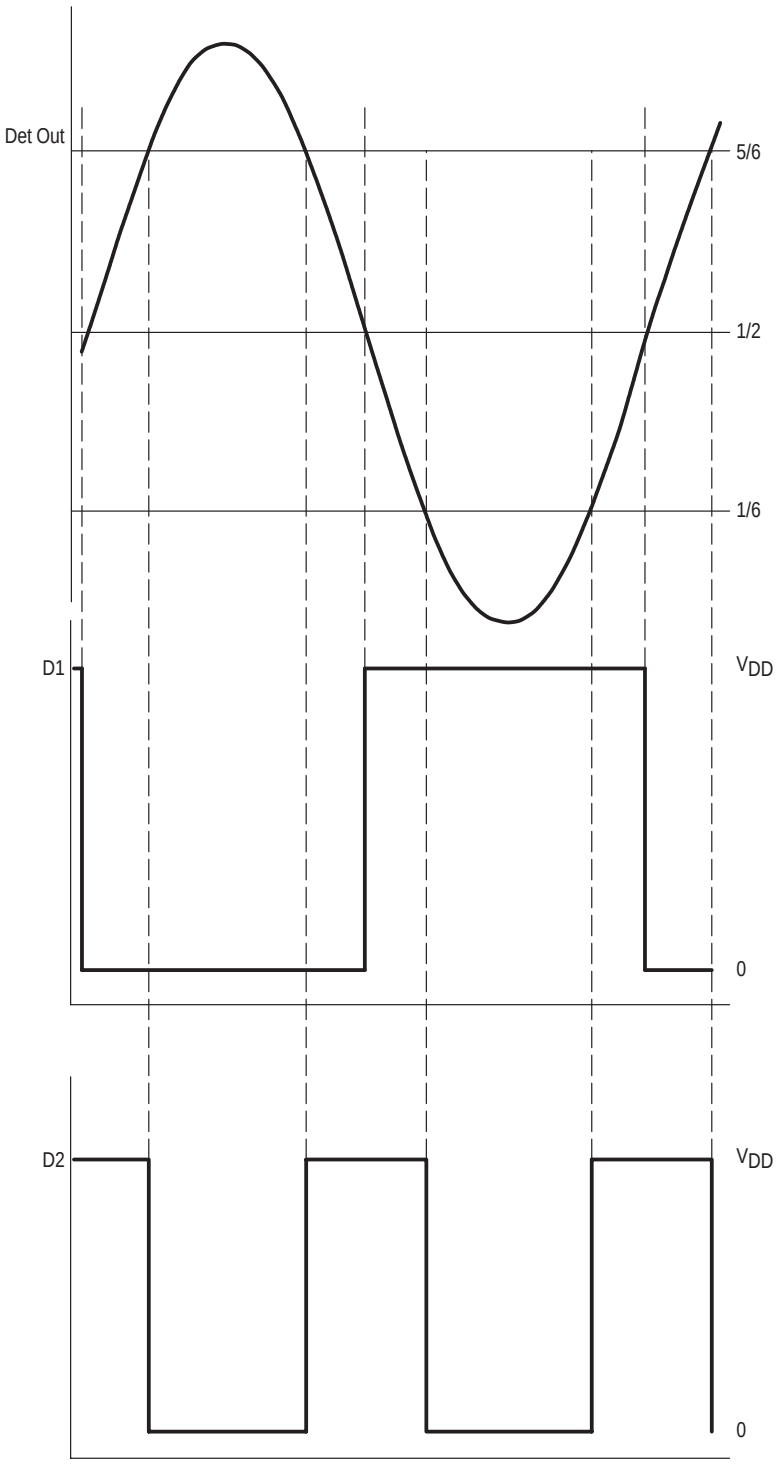


Figure 3. Typical BRF Response

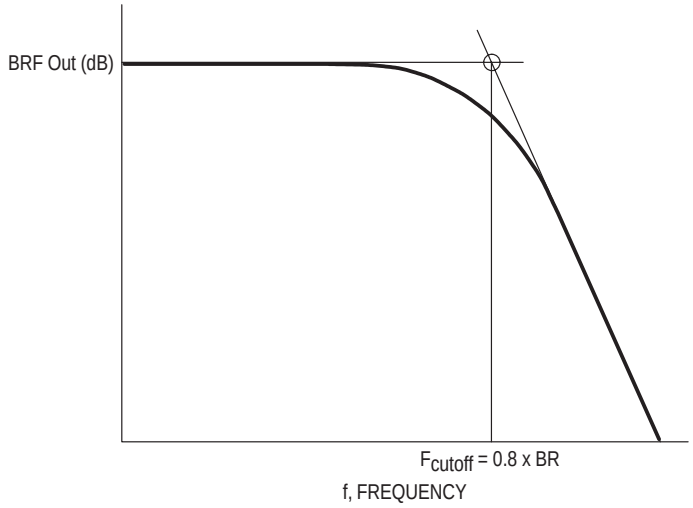


Figure 4. Start–Up Operation

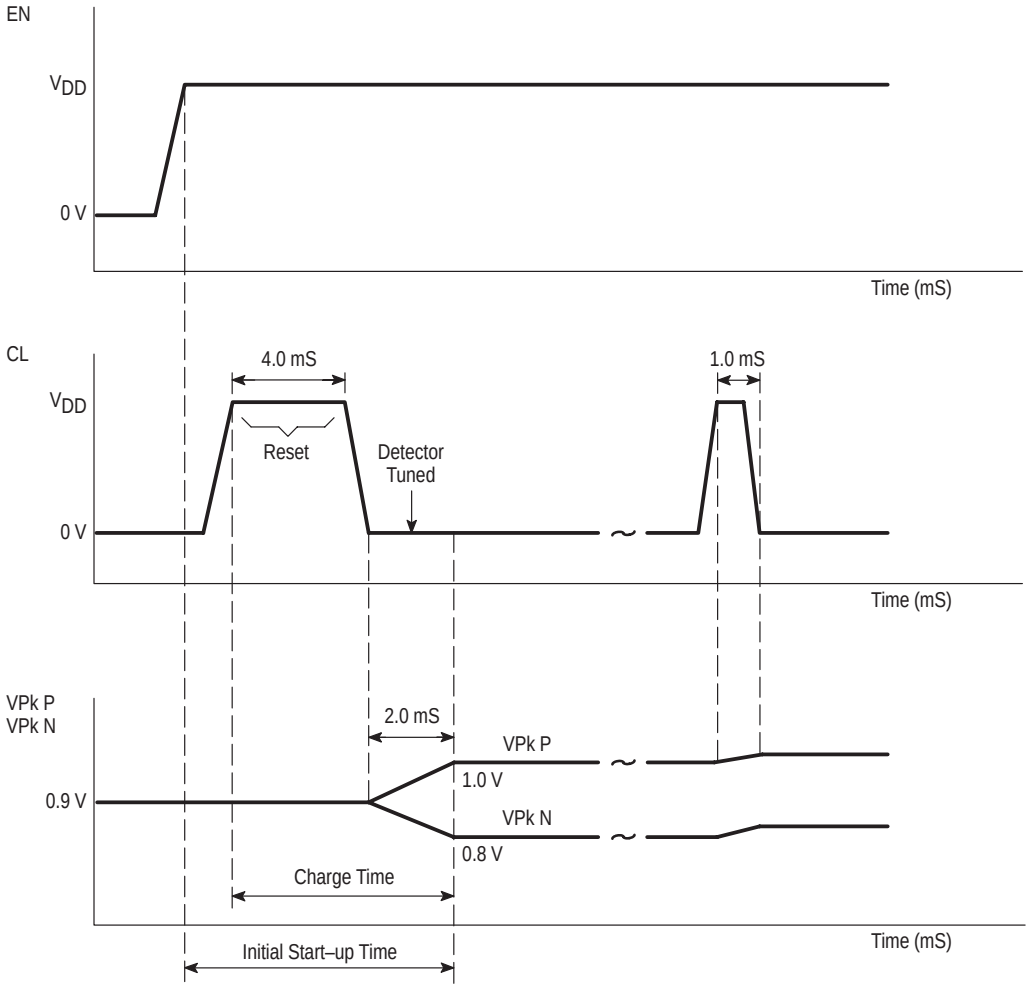
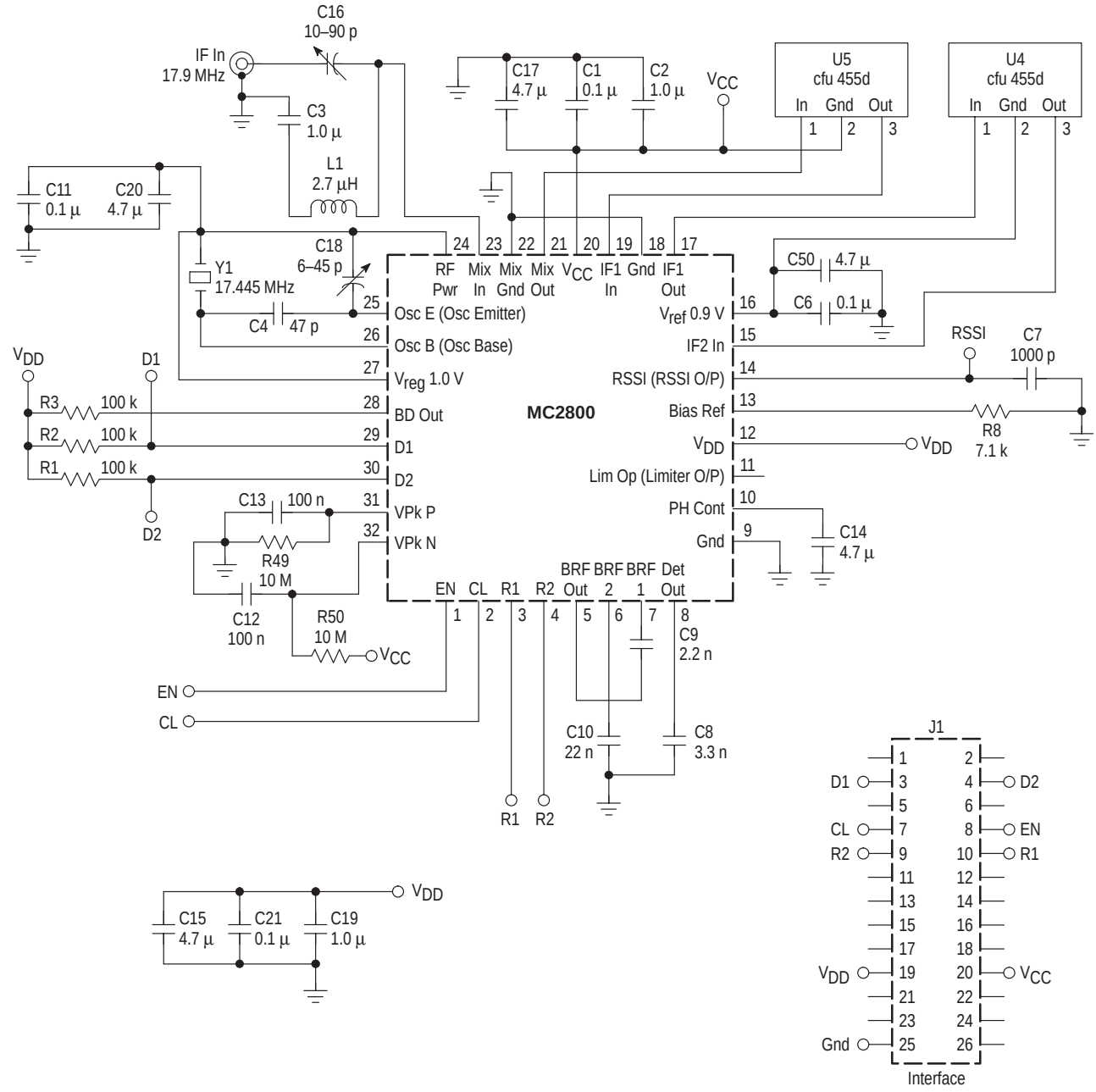


Figure 5. Schematics of MC2800 Demo Board (Two 455 kHz Ceramic Filters)



Capacitors	
C1,C6,C11,C12,C13,C21	0.1 µF
C2,C3,C19	1.0 µF
C4	47 pF
C7	1.0 nF
C8	3.3 nF
C9	2.2 nF
C10	22 nF
C14,C15,C17,C20,C50	4.7 µF
Variable capacitors	
C16	10 to 90 pF
C18	6.0 to 45 pF

Inductor	
L1	2.7 µH
Resistors	
R1,R2,R3	100 kΩ
R8	7.1 kΩ
R49,R50	10 MΩ
Ceramic filters (455 kHz)	
U4,U5	CFU455D
Crystal (17.445 MHz)	
Y1	1U0174450B2035BOX

MC2800 Application Board

The typical application circuit of MC2800 is shown in Figure 5. The performance of the system kit consisting of the MC2800, MC68175 and MC68HC705L32 is measured. The system has a typical sensitivity of –115 dBm @ Phase A. Table 1 shows the sensitivity measurements of the system at different symbol rates along with the Symbol Rate Filter (SRF) filter selections. The test input to the MC2800 is a single message of 12 characters. The first two columns of Table 1 show the SRF's R1 and R2 conditions during synchronization. The third and fourth columns show the R1 and R2 conditions during data sampling. In operation, the original digital baseband data is encoded by the Encoder Software in the computer before this encoded message is sent out via the Data Acquisition card (DAQ) to the signal generator HP8657B. The MC2800 receives the modulated signal from the HP8657B and then converts it into baseband data D1 and D2. When retrieving data from Pins D1 and D2, it is essential to observe the timing requirements for the EN and CL signals. This is illustrated in EN and CL Timing Requirements. The computer at the other end then retrieves the D1 and D2 data through the L32EVS board and displays it in the HC05 Pager Development Board. The test setup of this system measurement is shown in Figure 6.

With the input frequency at 17.9 MHz the input impedance of the mixer is measured to be 2.1k–j2.67 kΩ. The input impedance does not vary significantly with the supply voltage and frequency of interest. Figure 7 shows the input impedance of the mixer over a range of frequencies in the Smith Chart. From the Smith Chart, the matching network connecting between the 50 Ω signal generator and the MC2800 mixer is worked out to be consisting of a shunt inductor of 3.8 μH and a series capacitor of 19 pF. A varicap of 10 to 90 pF is selected for the series capacitor as this will make the fine tuning of the input stage easier. The other input to the mixer is internally connected to a Local Oscillator (LO). The LO has a Colpitts amplifier which amplifies the external crystal frequency of 17.445 MHz. The natural oscillation frequency of the crystal is not exactly 17.445 MHz, therefore the capacitor C4 is set to 47 pF and the varicap C18 is selected to have a range of 6.0 to 45 pF for making sure that the LO can oscillate at 17.445 MHz. The conversion voltage gain of the mixer is about 20 dB @ –110 dBm. Table 2 shows the mixer gain with different input signal levels. After the input signal is amplified and down converted to 455 kHz, it is then filtered before entering the amplifier 1st IF Amp. The voltage gain of this amplifier is measured to be 40 dB. This is shown in Figure 8. From the first stage of amplification the input signal strength is also detected and it can be monitored at the RSSI Pin. The relationship between the input signal strength and the RSSI output is shown in Figure 9. In applications where component cost is critical, the second 455 kHz ceramic filter may be replaced by an LC π network. This is shown in Figure 10. The 1.0 μF capacitors are used for blocking dc voltages. The network consisting of 560 pF capacitors and the 470 μH inductor acts as both a low pass filter centered at 455 kHz and a matching between the first amplifier output and the second amplifier input. The output resistance of the first amplifier is 1.1 kΩ and the input resistance of the second amplifier is 1.5 kΩ. Based on the setup as shown previously in Figure 6, the system performance of the MC2800 (one 455 kHz ceramic filter plus one LC network combination) together with the MC68175 and the MC68HC705L32 is measured and the test result is tabulated in Table 3.

Coming back to the device MC2800, the demodulator is coilless and it does not need any resonator. The external resistor connected to the pin Bias Ref is used to give the reference bias loop current for the demodulator. The frequency response of the demodulator is measured and it is shown in Figure 11. At the Demodulator Output (Det Out Pin) a capacitor is used to decouple the high frequency noise. Figure 12 shows the differences of the signal measured at this pin with different values of capacitors used. This highlights the importance in the selection of this capacitor value. If this value is too small then the SINAD will be very poor and hence the sensitivity will be very bad. If it is too big then the high frequency contents in the step input signal will be decoupled and this will make the decoding very difficult after analog to digital conversion. The SRF filter is a two pole active filter. The filter characteristics are plotted in Figure 14 and Figure 15 for which the selections of R1 = 0 and R2 = 1 are used during measurements. R1 and R2 are used to select the amount of resistors in the filter. The four level Data Slicer converts the analog signal into D1 and D2 digital outputs. This A–D conversion is best illustrated by the plots in Figures 16 and 17. A brief outline of the A–D conversion can be found in Data Slicer A/D Conversion. Figure 22 shows how the MC2800 is connected to the decoding device (MC68175) which is used after analog to digital conversion. The interface between the two devices is tabulated in Table 6. The operating procedure is also outlined.

Table 1. Test Result of the Typical MC2800 Demo Board with Different Symbol Rates (bps Means Bits Per Second and sps Means Symbols Per Second)

					6400 bps or 3200 sps	6400 bps or 3200 sps	3200 bps or 1600 sps	3200 bps or 1600 sps
					4 level	4 level	4 level	4 level
SRF Filter Control					Sensitivity (dBm)			
1600 sps R1	1600 sps R2	3200 sps R1	3200 sps R2		Phase A	Phase B	Phase A	Phase C
1	1	0	1		–112	–109	–112	–109

Figure 6. Test Equipment Setup

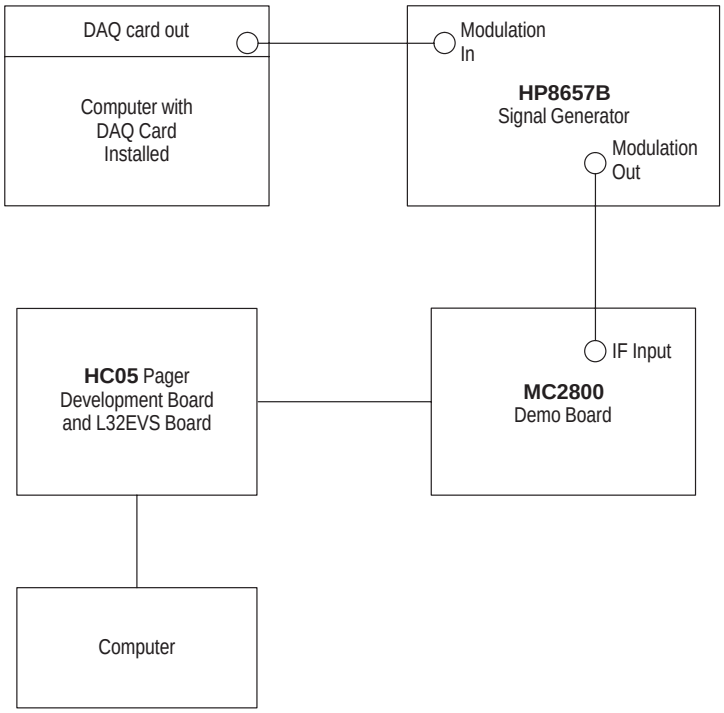


Figure 7. Input Impedence of MC2800 Mixer with Frequency Range 15 to 30 MHz

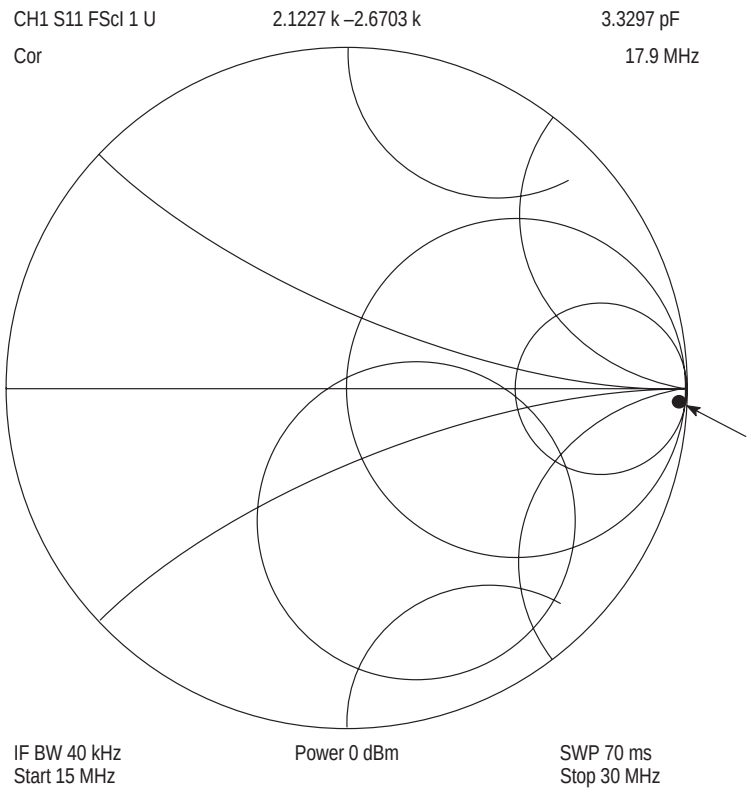


Table 2. Mixer Gain (with Matching Circuit)

Mixer Input (dBm)	–120	–110	–100	–90	–80	–70	–60	–50	–40	–30	–20	–10
Mixer Voltage Gain (dBm)	21.5	19.6	18.6	18	17.8	17.6	17.7	17.8	17.6	17.4	12.6	3.0
Mixer Power Gain (dBm)	6.7	4.75	3.83	3.21	3.0	2.79	2.9	2.99	2.87	2.64	–2.16	–11.7

Figure 8. 1st IF Amplifier Voltage Gain

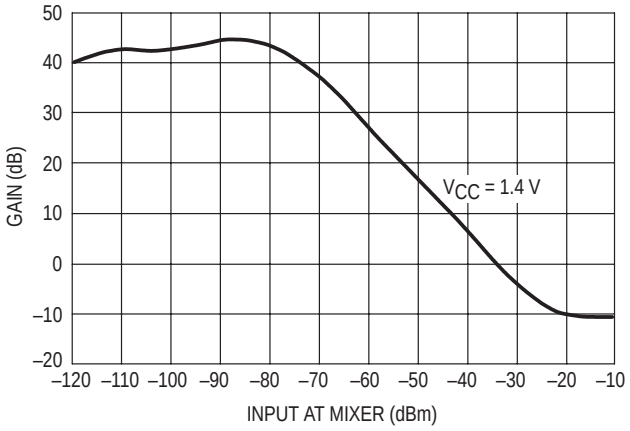


Figure 9. RSSI Output versus Mix In

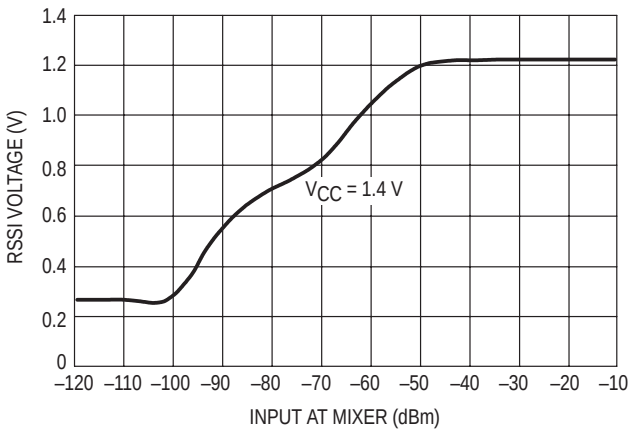
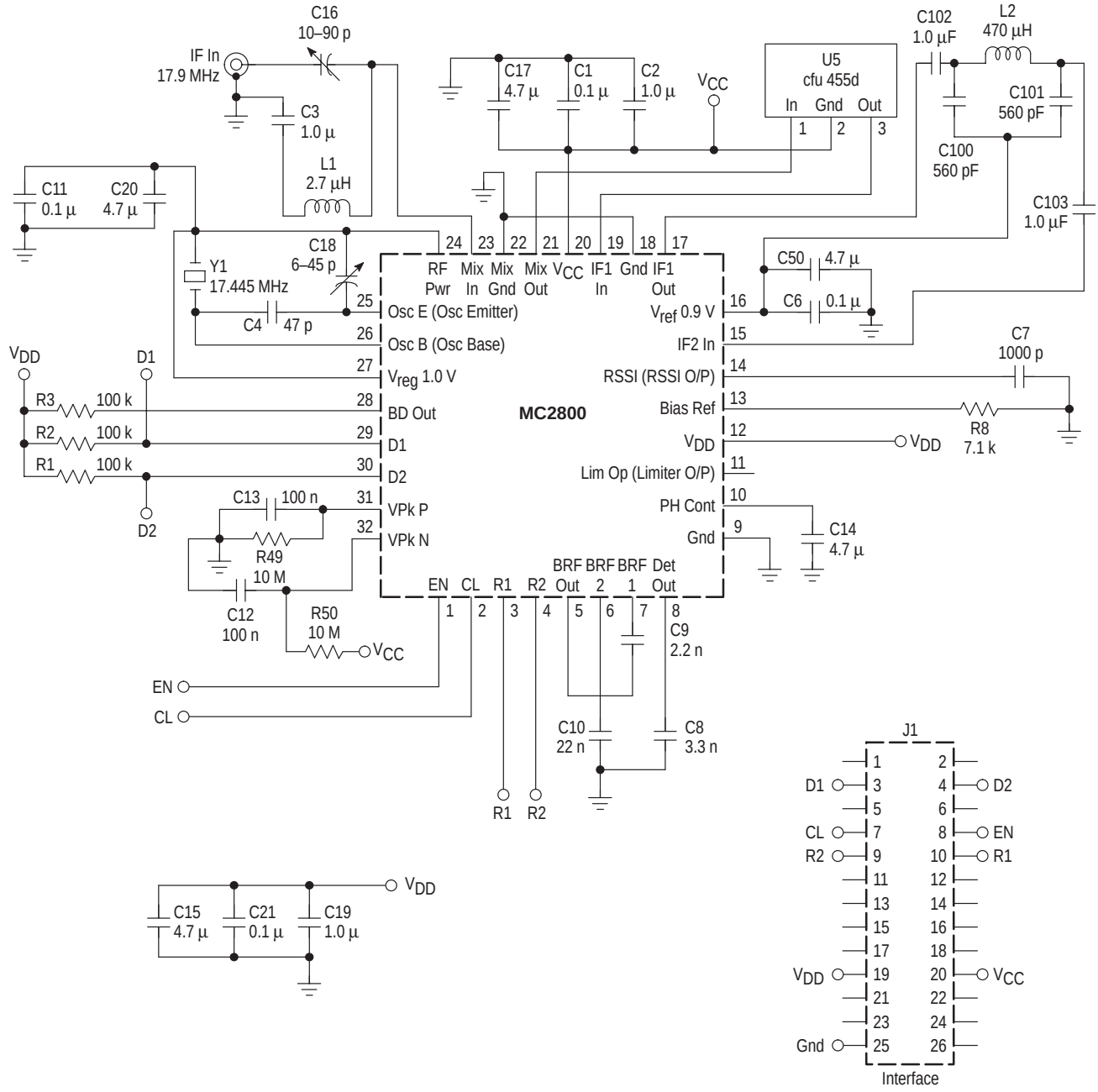


Figure 10. Schematics of MC2800 Demo Board (One 455 kHz Ceramic Filter)



Capacitors	
C1,C6,C11,C12,C13,C21	0.1 µF
C2,C3,C19,C102,C103	1.0 µF
C4	47 pF
C7	1.0 nF
C8	3.3 nF
C9	2.2 nF
C10	22 nF
C14,C15,C17,C20,C50	4.7 µF
Variable capacitors	
C16	10 to 90 pF
C18	6.0 to 45 pF
Capacitors	
C100,C101	560 pF

Inductors	
L1	2.7 µH
L2	470 µH
Resistors	
R1,R2,R3	100 kΩ
R8	7.1 kΩ
R49,R50	10 MΩ
Ceramic filter (455 kHz)	
U5	CFWC455D–TC
Crystal (17.445 MHz)	
Y1	1U0174450B2035BOX

Table 3. Test Result of the One 455 kHz Ceramic Demo Board

					6400 bps or 3200 sps	6400 bps or 3200 sps	3200 bps or 1600 sps	3200 bps or 1600 sps
					4 level	4 level	4 level	4 level
SRF Filter Control					Sensitivity (dBm)			
1600 sps R1	1600 sps R2	3200 sps R1	3200 sps R2		Phase A	Phase B	Phase A	Phase C
1	1	1	0		–108	–105	–108	–105

Figure 11. Demodulator Response at Det Out with Reference to Mixer Input

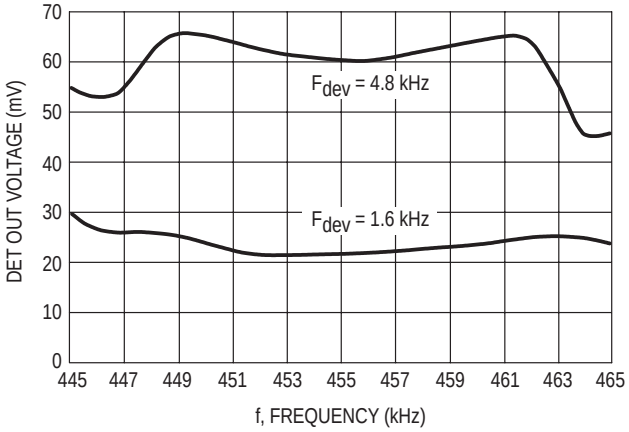


Figure 12. Det Out Characteristics with Different Capacitors (C = 20 nF)

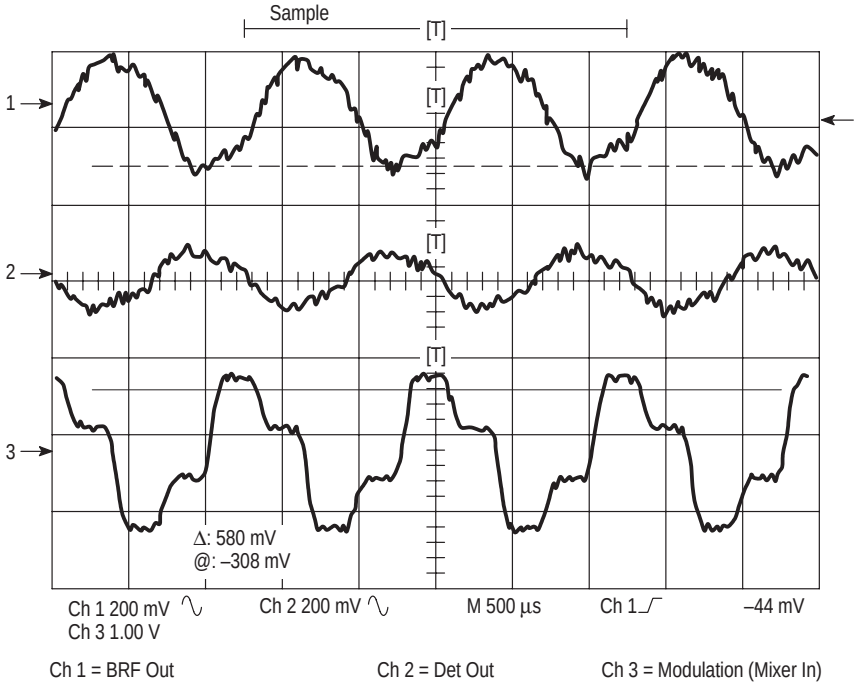


Figure 13. Det Out Characteristics with Different Capacitors (C = 3.3 nF)

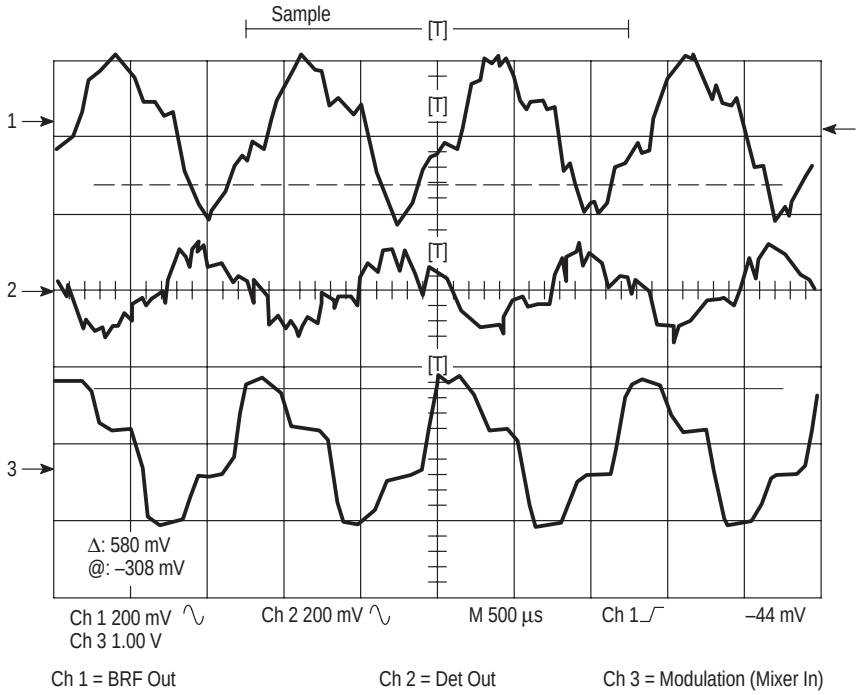


Figure 14. Symbol Rate Filter – Phase Response (R1 = 0, R2 = 1)

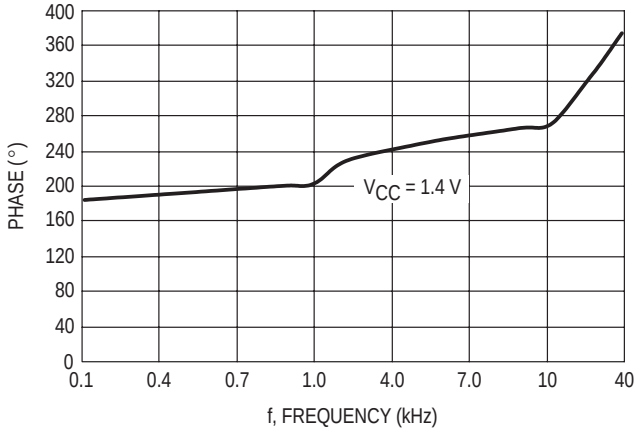


Figure 15. Symbol Rate Filter – Gain Response (R1 = 0, R2 = 1)

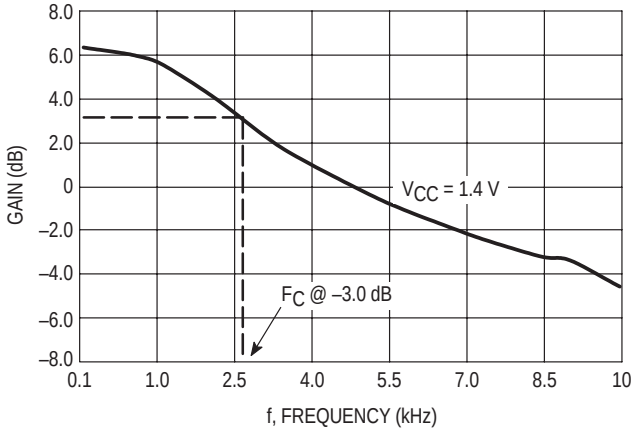


Figure 16. Modulation and Signal at BRF Out Pin

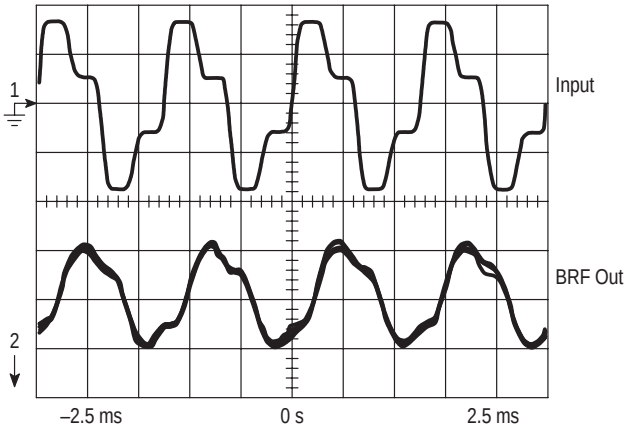
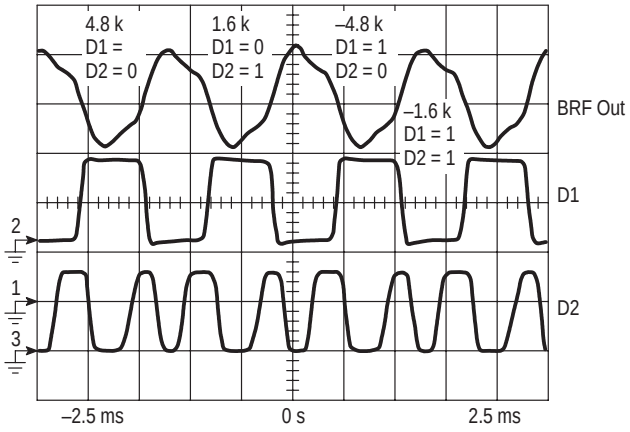


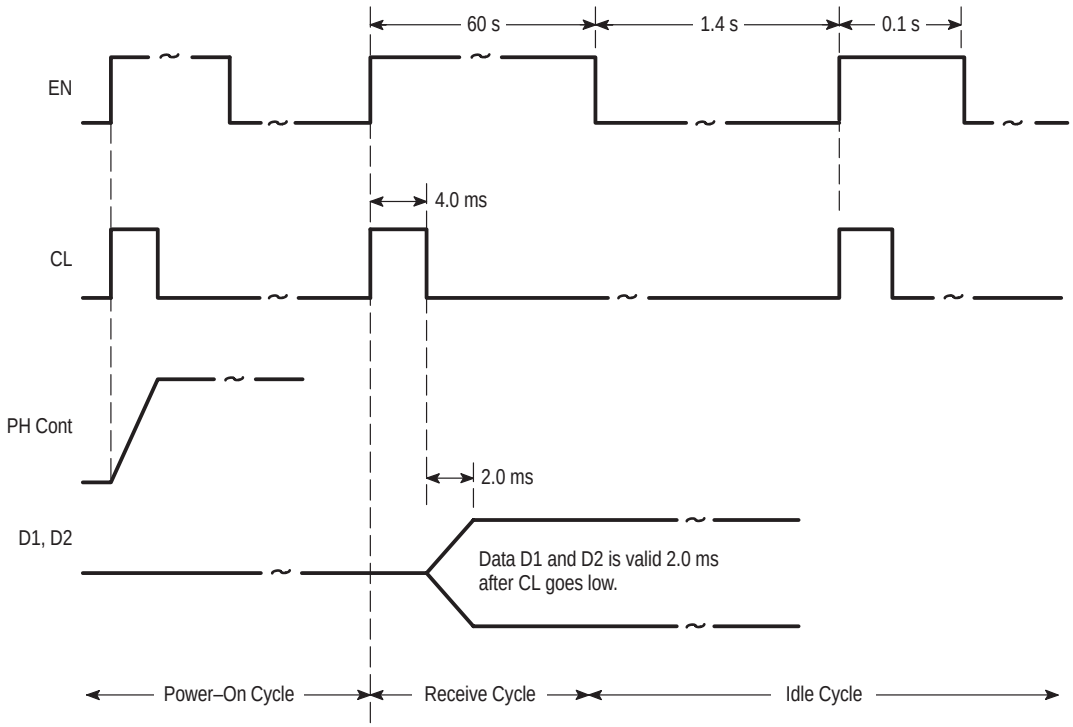
Figure 17. Digital D1 and D2 Outputs



EN and CL Timing Requirements

When power is first applied to the MC2800 the capacitor connecting to the Pin PH Cont is pre–charged to 0.9 V. The voltages at Pins EN and CL must be set to high during this Power On cycle of time. In the typical system application as shown in Figure 6 the voltage at Pin EN is pulled to high for a duration of 60 seconds at first. During this period the device MC2800 is enabled and data at Pins D1 and D2 is valid 6.0 ms after EN is high. When EN goes high, CL can also go high at the same instance without any delay. The purpose of pulling CL to high is to set up the voltages at Pins 31 and 32. It has been tried that 4.0 ms is adequate to get these pins to the correct voltages. However some delay must be allowed for the transient to die down after CL goes low. In application, it is observed that the data D1 and D2 will be valid 2.0 ms after CL goes low in this receive cycle. When there is no incoming message to receive, it is best to disable the MC2800 to save power. In this idle cycle, the MC2800 is disabled most of the time and it is enabled once every 1.5 s (or in some cases 1.875 s) to open the channel for the MCU to detect if there is any message coming in or not. These typical conditions are all illustrated in Figure 18.

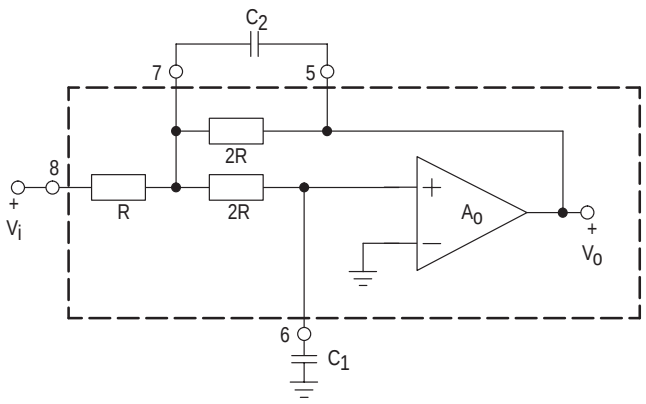
Figure 18. Timing of EN and CL



Low Pass Bit–Rate Filter

This section is a short description of the Architecture of the Bit–Rate Filter used in the MC2800.

Figure 19.



Based on the schematics described above, the equation of this filter is:

$$\frac{v_o}{v_i}(S) = \frac{-\frac{2A_o}{1+A_o}}{1 + s2RC_2 + \frac{2}{1+A_o}\left(1 + s4RC_1 + s^2 2R^2 C_1 C_2\right)}$$

$$= -\frac{\frac{2A_o}{3+A_o}}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)}$$

Assume A_o = 200, and $C_1 = 10C_2$, this equation can be simplified as:

$$p_1 = -\frac{0.44}{RC_2} \quad \text{and} \quad p_2 = -\frac{11.56}{RC_2}$$

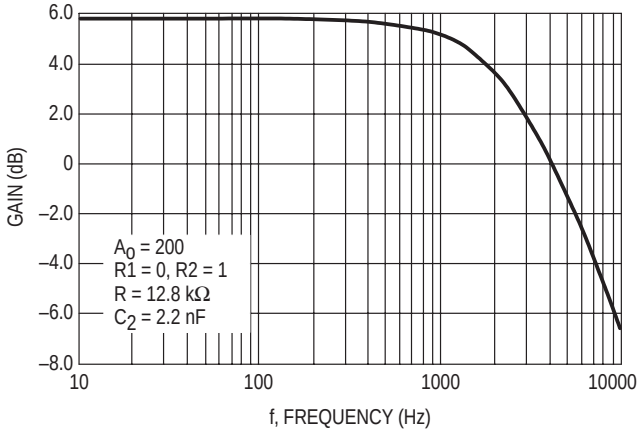
With the different combinations of R1, R2 to setup the Bit–Rate Filter, the cut–off frequencies has been defined according to the table below:

Table 4. Bit–Rate Filter Frequency Responses
(assume $C_1 = 10C_2$ = 22 nF)

R1	R2	R/kΩ	f_{p1}/Hz	f_{p2}/Hz
0	0	84.0	379	9.96 k
1	0	35.6	894	23.5 k
1	1	26.5	1.20 k	31.6 k
0	1	12.8	2.49 k	65.3 k

A typical frequency response of the bit–rate filter is shown in Figure 20.

Figure 20. Gain Response of the Bit–Rate Filter



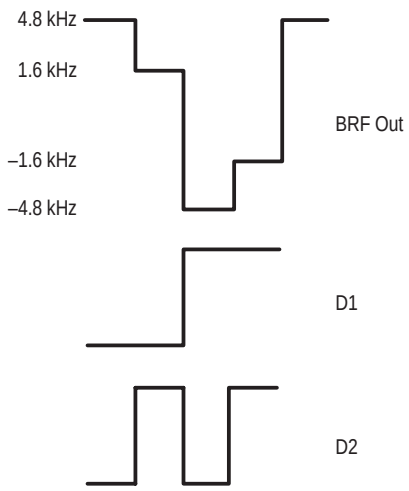
Data Slicer A/D Conversion

In the data slicer of the MC2800 there is a block of comparators which can compare four different kinds of input voltage levels. This “4 level” comparator compares the incoming signal (BRF Out) and then turns it into digital D1 and D2 outputs. This is shown graphically in Figure 21. The state table of D1 and D2 is shown in Table 5.

Table 5. State Table of D1 and D2

Frequency Deviation	D1	D2
4.8 kHz	0	0
1.6 kHz	0	1
–1.6 kHz	1	1
–4.8 kHz	1	0

Figure 21. D1 and D2 Outputs



MC2800 with HP8648

Figure 22. MC2800 Demo Board Test Circuit
(See Figures 5 and 10 for component list)

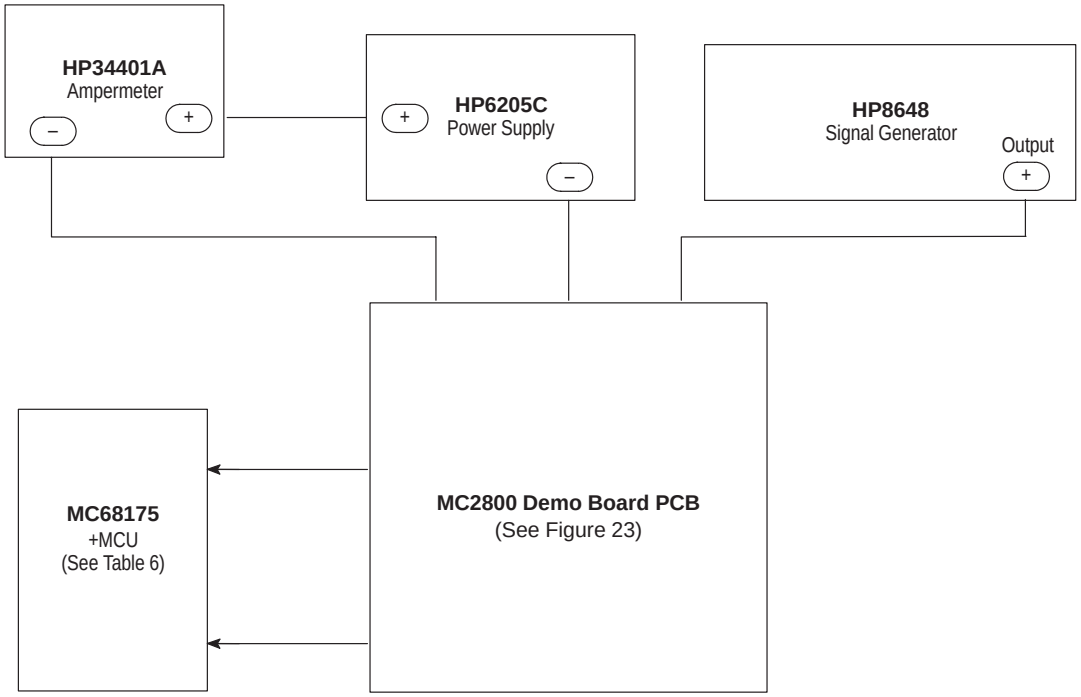
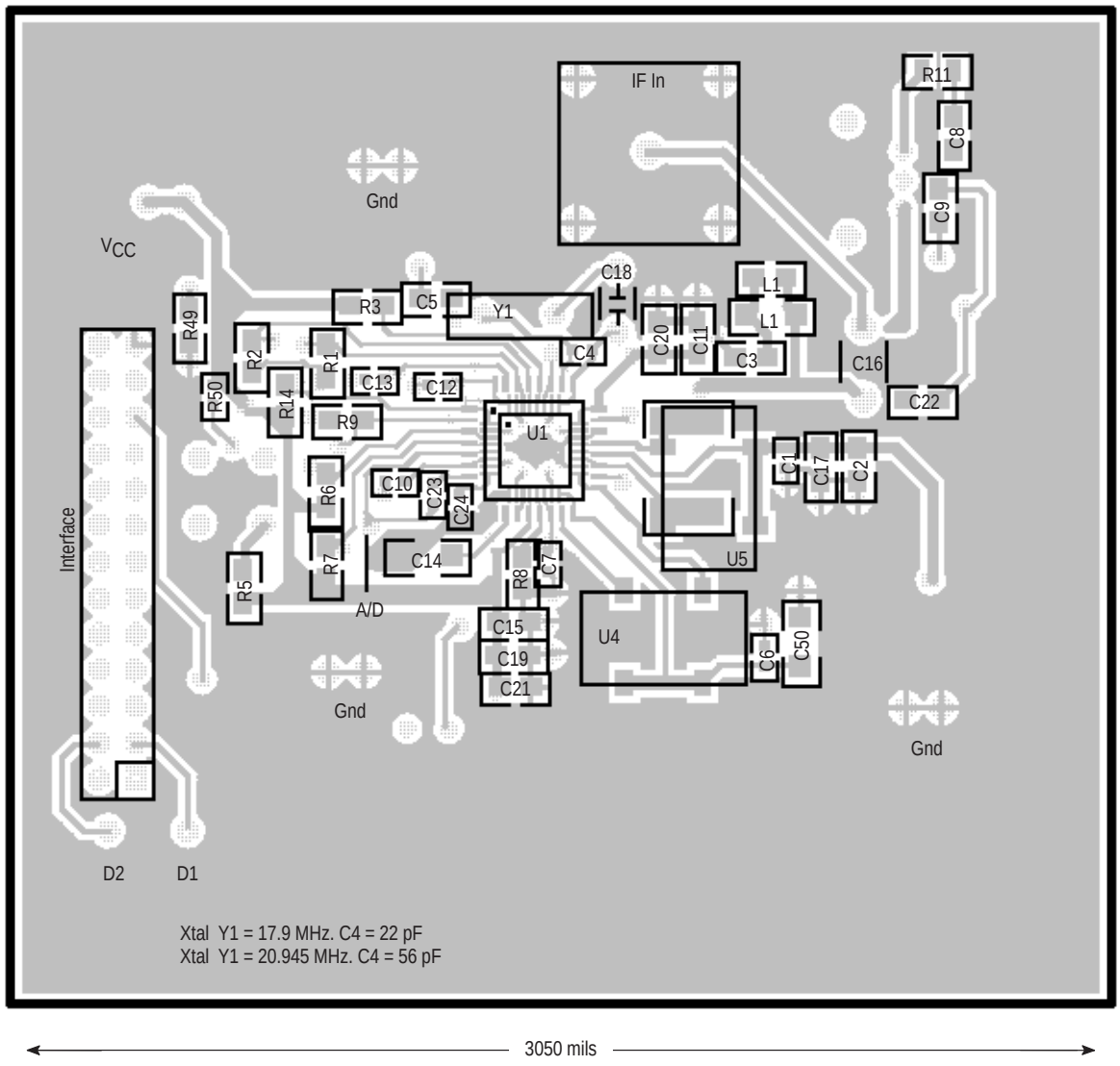


Figure 23. MC2800 Demo Board PCB (Top Layer)



C1,C6,C11,C21	0.1 µF	L1	2.7 µH
C2,C3,C5,C8,			
C9,C19,C22	1.0 µF	R1, R2, R3,	
C4	22 pF	R6, R7, R14	100 k
C7	1000 pF	R5, R11	2.0 k
C10	22 nF	R8	7.5 k
C12,C13	100 nF	R9	10 k
C14	22 µF	R49	10 M
C15,C17,C20,		R50	910 k
C50	4.7 µF		
C16	10 to 90 pF	U1	MC2800
C18	4 to 25 pF	U4,U5	CFWC455D–TC
C23	2.2 nF	Y1	17.445 MHz
C24	3.3 nF		

Table 6. Interface Between the MC2800 and the MC68175

MC2800 Pin No.	MC2800 Pin Description	Interface Connector Pin No.	MC68175 Pin No.	MC68175 Pin Description
30	D2	3	12	EXTS0
29	D1	4	11	EXTS1
2	CL	7	23	S0
1	EN	8	22	S1
4	R2	9	21	S2
3	R1	10	20	S3
12	V_{DD}	19	–	–
20	V_{CC}	20	–	–
14	RSSI	21	–	–
9, 18	Gnd	25	–	–

Operating Procedures

1. Connect up the circuit as shown in Figure 22.
2. Set the power supply to 1.4 V (typical value of an AA battery).
3. Set the HP8648A signal generator to the following:

FORMAT FLEX
POLARITY NORMAL FILTER ON

ROAMING MODE NONE

CYCLE 00 FRAME 000 PHASE A
COLLAPSE CYCLE 0

ADDRESS TYPE SHORT
ADDRESS1 2031715

PAGER CODE A0000001
DUMMY CALL OFF

IMMEDIATE STOP OFF
HEADER ON TERMINATOR ON

MODE SINGLE AMPLITUDE –110 dBm

MESSAGE NO.6 MESSAGE LENGTH 10
1234567890

VECTOR TYPE STANDARD

DATA RATE 6400/4
PAGER TYPE NUMERIC

4. Connect V_{DD} (Pin 19 of Interface Connector) to the digital voltage supply (usually 3.0 V).
5. Connect the MC2800 to the Flex decoder MC68175 as shown in Table 6. For example, Pin 1 of MC2800 is connected to Pin 22 of MC68175 via the Interface Connector Pin 8.
6. Program the MCU such that it can generate the timing for the EN and CL Pins as shown in Figure 18.

MOTOROLA

MC3356

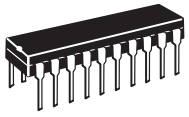
Wideband FSK Receiver

The MC3356 includes Oscillator, Mixer, Limiting IF Amplifier, Quadrature Detector, Audio Buffer, Squelch, Meter Drive, Squelch Status output, and Data Shaper comparator. The MC3356 is designed for use in digital data communciations equipment.

- Data Rates up to 500 kilobaud
- Excellent Sensitivity: – 3 dB Limiting Sensitivity
  30 μVrms @ 100 MHz
- Highly Versatile, Full Function Device, yet Few External Parts are Required
- Down Converter Can be Used Independently — Similar to NE602

WIDEBAND FSK RECEIVER

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 738

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

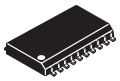
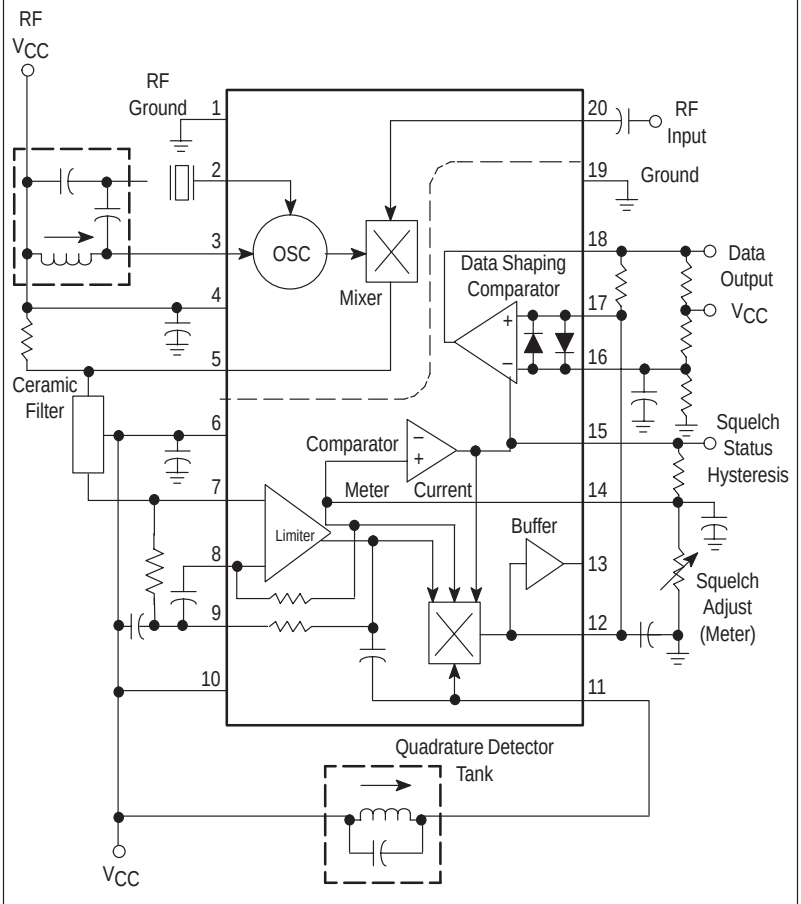
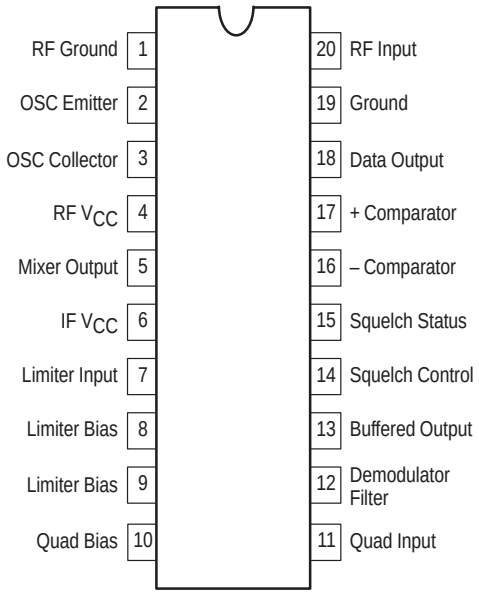


Figure 1. Representative Block Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3356DW	T_A = – 40 to +85°C	SO–20L
MC3356P		Plastic DIP

MAXIMUM RATINGS

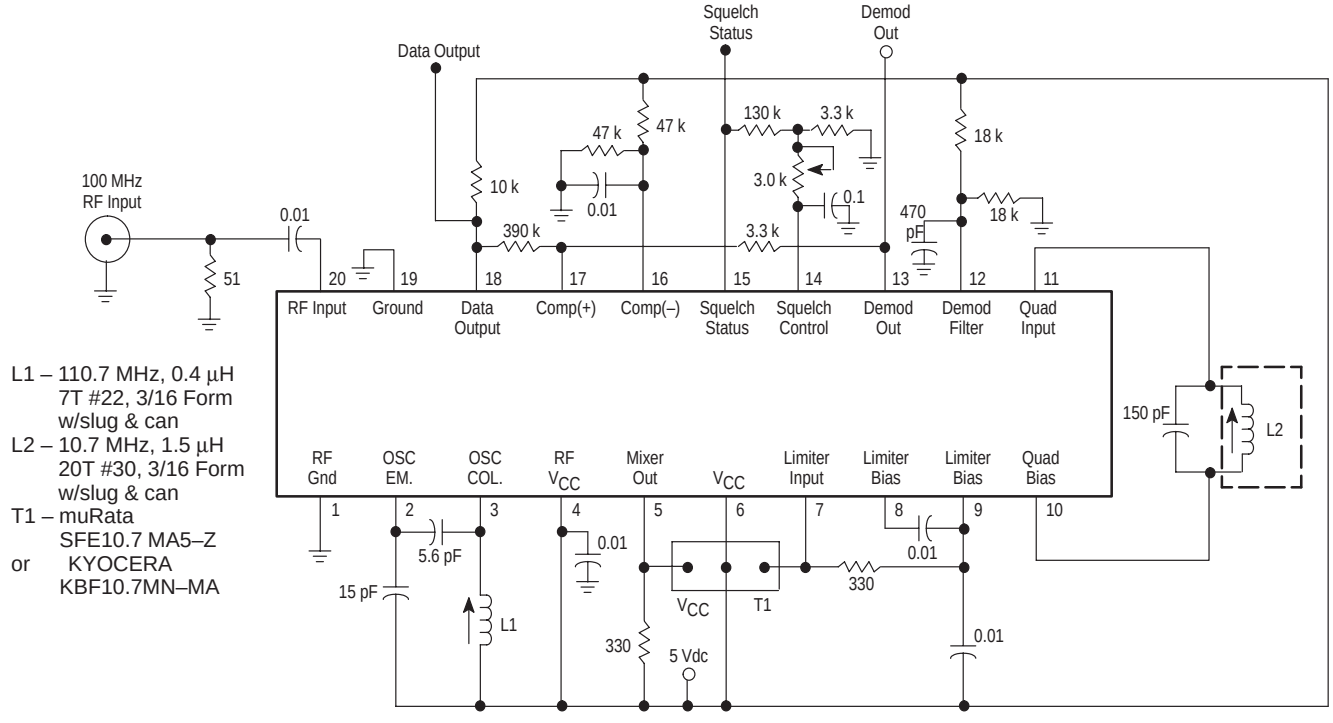
Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Power Supply Voltage Range (Pins 6, 10)	V_{CC}	3.0 to 9.0	Vdc
Operating RF Supply Voltage Range (Pin 4)	RF V_{CC}	3.0 to 12.0	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 100 MHz, f_{osc} = 110.7 MHz, Δf = ±75 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C, test circuit of Figure 2, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
Drain Current Total, RF V_{CC} and V_{CC}	–	20	25	mAdc
Input for – 3 dB limiting	–	30	–	µVrms
Input for 50 dB quieting $\left(\frac{S+N}{N}\right)$	–	60	–	µVrms
Mixer Voltage Gain, Pin 20 to Pin 5	2.5	–	–	
Mixer Input Resistance, 100 MHz	–	260	–	Ω
Mixer Input Capacitance, 100 MHz	–	5.0	–	pF
Mixer/Oscillator Frequency Range (Note 1)	–	0.2 to 150	–	MHz
IF/Quadrature Detector Frequency Range (Note 1)	–	0.2 to 50	–	MHz
AM Rejection (30% AM, RF V_{in} = 1.0 mVrms)	–	50	–	dB
Demodulator Output, Pin 13	–	0.5	–	Vrms
Meter Drive	–	7.0	–	µA/dB
Squelch Threshold	–	0.8	–	Vdc

NOTE: 1. Not taken in Test Circuit of Figure 2; new component values required.

Figure 2. Test Circuit



L1 – 110.7 MHz, 0.4 µH
7T #22, 3/16 Form
w/slug & can
L2 – 10.7 MHz, 1.5 µH
20T #30, 3/16 Form
w/slug & can
T1 – muRata
SFE10.7 MA5–Z
or KYOCERA
KBF10.7MN–MA

Figure 3. Output Components of Signal, Noise, and Distortion

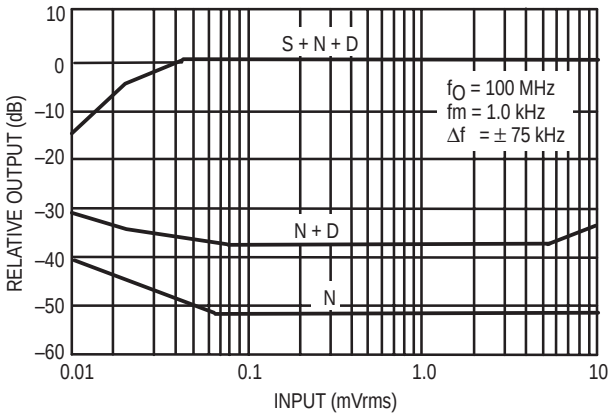
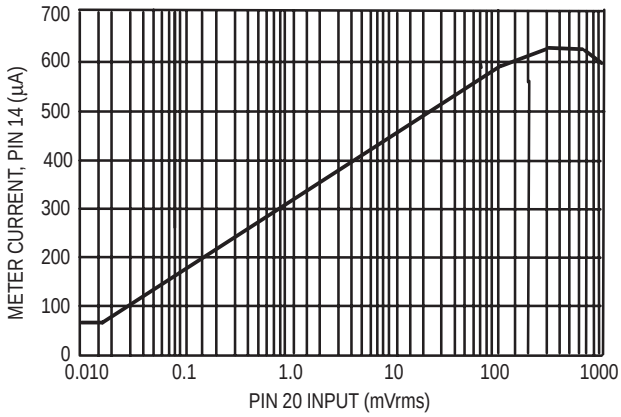


Figure 4. Meter Current versus Signal Input



GENERAL DESCRIPTION

This device is intended for single and double conversion VHF receiver systems, primarily for FSK data transmission up to 500 K baud (250 kHz). It contains an oscillator, mixer, limiting IF, quadrature detector, signal strength meter drive, and data shaping amplifier.

The oscillator is a common base Colpitts type which can be crystal controlled, as shown in Figure 1, or L–C controlled as shown in the other figures. At higher V_{CC}, it has been operated as high as 200 MHz. A mixer/oscillator voltage gain of 2 up to approximately 150 MHz, is readily achievable.

The mixer functions well from an input signal of 10 μVrms, below which the squelch is unpredictable, up to about 10 mVrms, before any evidence of overload. Operation up to 1.0 Vrms input is permitted, but non–linearity of the meter output is incurred, and some oscillator pulling is suspected. The AM rejection above 10 mVrms is degraded.

The limiting IF is a high frequency type, capable of being operated up to 50 MHz. It is expected to be used at 10.7 MHz in most cases, due to the availability of standard ceramic resonators. The quadrature detector is internally coupled to the IF, and a 5.0 pF quadrature capacitor is internally provided. The –3dB limiting sensitivity of the IF itself is approximately 50 μV (at Pin 7), and the IF can accept signals up to 1.0 Vrms without distortion or change of detector quiescent dc level.

The IF is unusual in that each of the last 5 stages of the 6 state limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 10 μV to 100 mVrms (see Figure 4).

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator (+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 30 μVrms. The 130 kΩ resistor shown in the test circuit provides a small amount of hysteresis. Its connection between the 3.3 k resistor to ground and the 3.0 k pot, permits adjustment of squelch level without changing the amount of hysteresis.

The squelch is internally connected to both the quadrature detector and the data shaper. The quadrature detector output, when squelched, goes to a dc level approximately equal to the zero signal level unsquelched. The squelch causes the data shaper to produce a high (V_{CC}) output.

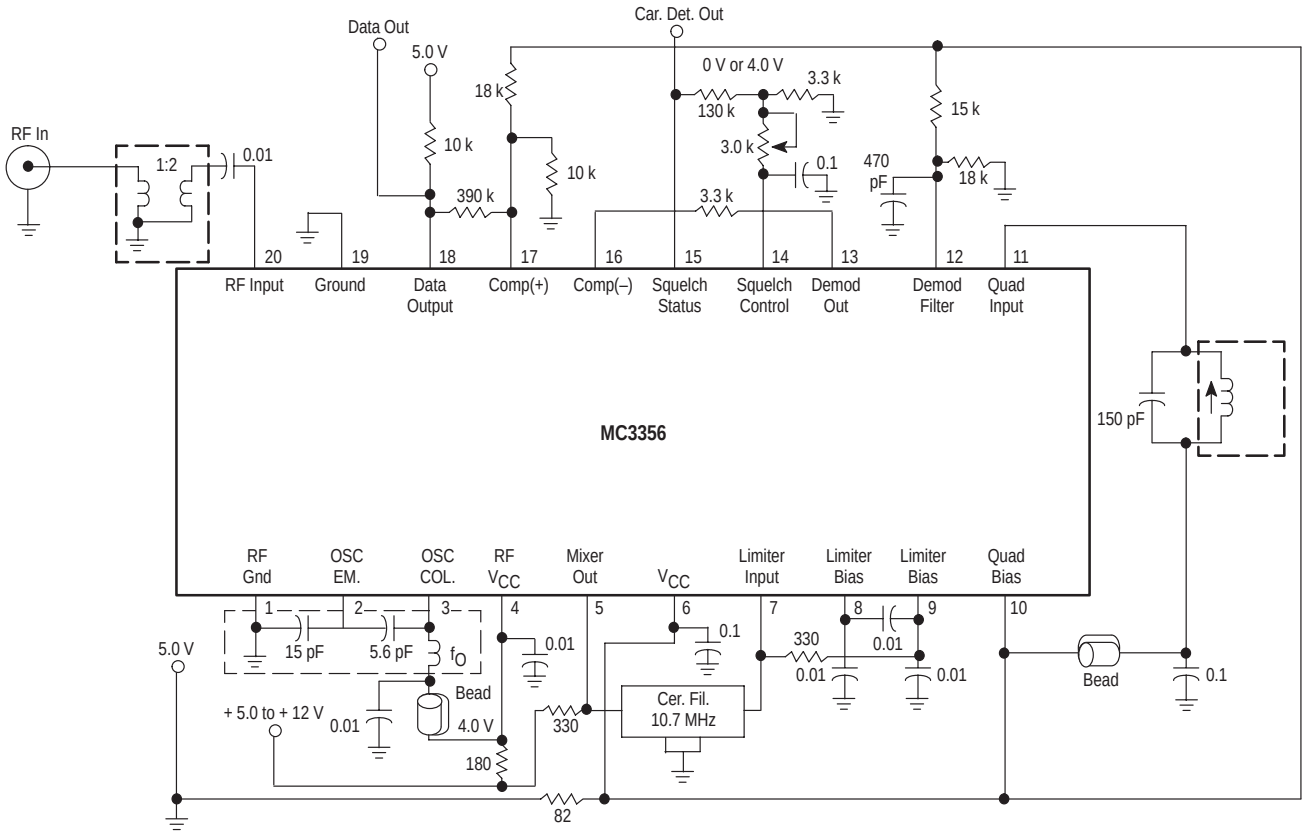
The data shaper is a complete ‘‘floating’’ comparator, with back to back diodes across its inputs. The output of the quadrature detector can be fed directly to either input of this amplifier to produce an output that is either at V_{CC} or V_{EE}, depending upon the received frequency. The impedance of the biasing can be varied to produce an amplifier which “follows” frequency detuning to some degree, to prevent data pulse width changes.

When the data shaper is driven directly from the demodulator output, Pin 13, there may be distortion at Pin 13 due to the diodes, but this is not important in the data application. A useful note in relating high/low input frequency to logic state: low IF frequency corresponds to low demodulator output. If the oscillator is above the incoming RF frequency, then high RF frequency will produce a logic low (input to (+) input of Data Shaper as shown in Figures 1 and 2).

APPLICATION NOTES

The MC3356 is a high frequency/high gain receiver that requires following certain layout techniques in designing a stable circuit configuration. The objective is to minimize or eliminate, if possible, any unwanted feedback.

Figure 5. Application with Fixed Bias on Data Shaper



APPLICATION NOTES (continued)

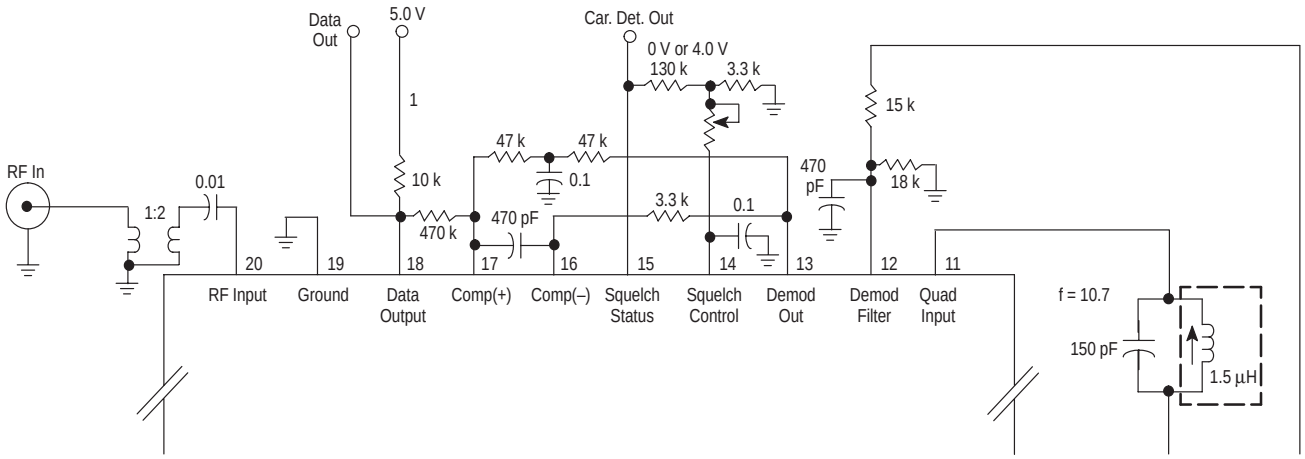
Shielding, which includes the placement of input and output components, is important in minimizing electrostatic or electromagnetic coupling. The MC3356 has its pin connections such that the circuit designer can place the critical input and output circuits on opposite ends of the chip. Shielding is normally required for inductors in tuned circuits.

The MC3356 has a separate V_{CC} and ground for the RF and IF sections which allows good external circuit isolation by minimizing common ground paths.

Note that the circuits of Figures 1 and 2 have RF, Oscillator, and IF circuits predominantly referenced to the plus supply rails. Figure 5, on the other hand, shows a suitable means of ground referencing. The two methods produce identical results when carefully executed. It is important to treat Pin 19 as a ground node for either approach. The RF input should be "grounded" to Pin 1 and then the input and the mixer/oscillator grounds (or RF V_{CC} bypasses) should be connected by a low inductance path to Pin 19. IF and detector sections should also have their bypasses returned by a **separate** path to Pin 19. V_{CC} and RF V_{CC} can be decoupled to minimize feedback, although the configuration of Figure 2 shows a successful implementation on a common 5.0 V supply. Once again, the message is: define a supply node and a ground node and return each section to those nodes by separate, low impedance paths.

The test circuit of Figure 2 has a 3 dB limiting level of 30 μV which can be lowered 6 db by a 1:2 untuned transformer at the input as shown in Figures 5 and 6. For applications that require additional sensitivity, an RF amplifier can be added, but with no greater than 20 db gain. This will give a 2.0 to 2.5 μV sensitivity and any additional gain will reduce receiver dynamic range without improving its sensitivity. Although the test circuit operates at 5.0 V, the mixer/oscillator optimum performance is at 8.0 V to 12 V. A minimum of 8.0 V is recommended in high frequency applications (above 150 MHz), or in PLL applications where the oscillator drives a prescaler.

Figure 6. Application with Self–Adjusting Bias on Data Shaper



APPLICATION NOTES (continued)

Depending on the external circuit, inverted or noninverted data is available at Pin 18. Inverted data makes the higher frequency in the FSK signal a “one” when the local oscillator is above the incoming RF. Figure 5 schematic shows the comparator with hysteresis. In this circuit the dc reference voltage at Pin 17 is about the same as the demodulated output voltage (Pin 13) when no signal is present. This type circuit is preferred for systems where the data rates can drop to zero. Some systems have a low frequency limit on the data rate, such as systems using the MC3850 ACIA that has a start or stop bit. This defines the low frequency limit that can appear in the data stream. Figure 5 circuit can then be changed to a circuit configuration as shown in Figure 6. In Figure 6 the reference voltage for the comparator is derived from the demodulator output through a low pass circuit where τ is much lower than the lowest frequency data rate. This and similar circuits will compensate for small tuning changes (or drift) in the quadrature detector.

Squelch status (Pin 15) goes high (squelch off) when the input signal becomes greater than some preset level set by the resistance between Pin 14 and ground. Hysteresis is added to the circuit externally by the resistance from Pin 14 to Pin 15.

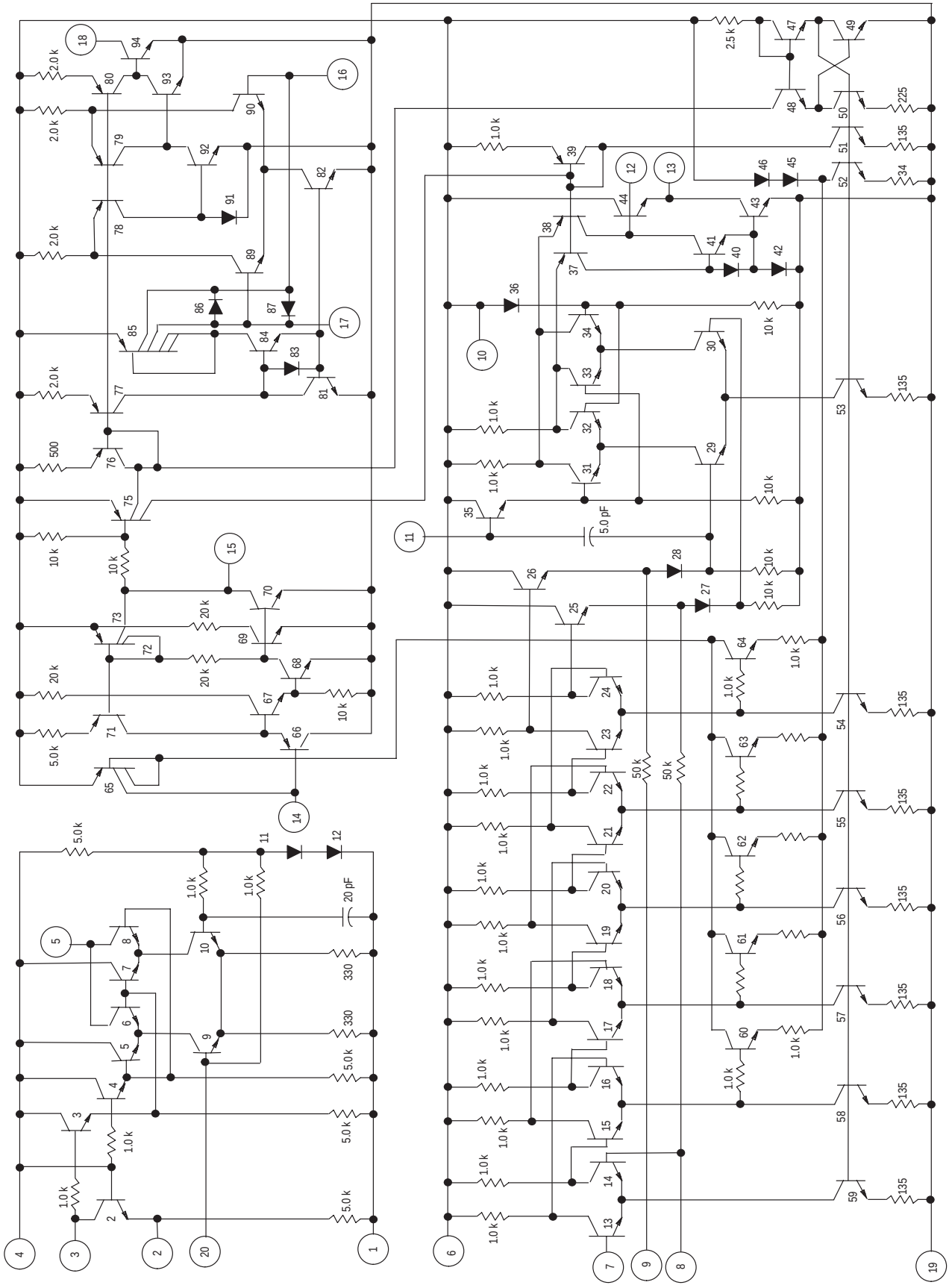


Figure 7. Internal Schematic

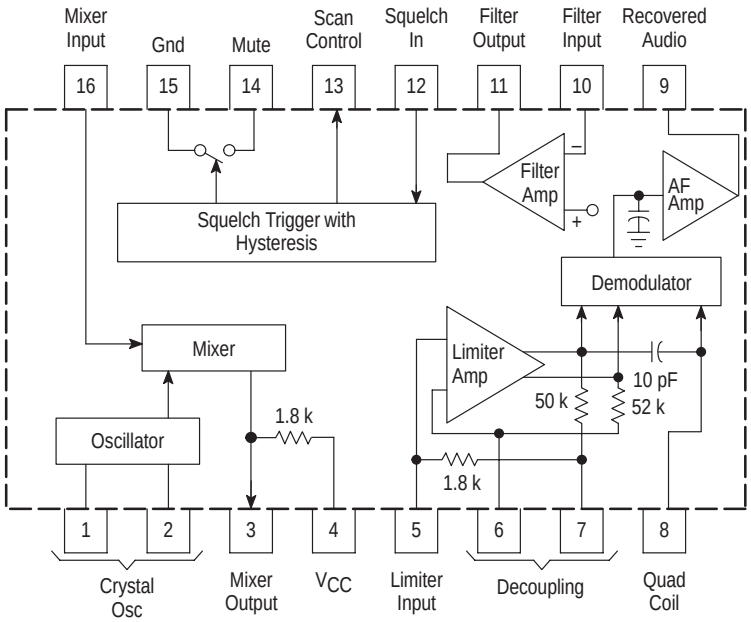
MOTOROLA

Low Power Narrowband FM IF

The MC3361B includes an Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control and Mute Switch. This device is designed for use in FM dual conversion communications equipment.

- Operates from 2.0 to 8.0 V Supply
- Low Drain Current 3.9 mA Typical @ V_{CC} = 4.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage –3.0 dB = 2.6 μV Typical
- Low Number of External Parts Required
- Operating Frequency Up to 60 MHz

Representative Block Diagram

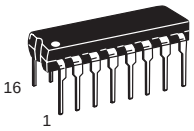


This device contains 92 active transistors.

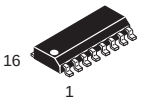
MC3361B

LOW POWER NARROWBAND FM IF

SEMICONDUCTOR TECHNICAL DATA

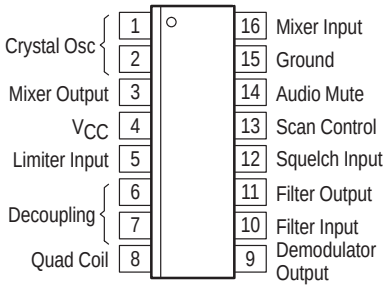


P SUFFIX
PLASTIC PACKAGE
CASE 648
Not Recommended for New Design



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3361BD	T_A = –30 to 70°C	SO–16
MC3361BP		Plastic DIP

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

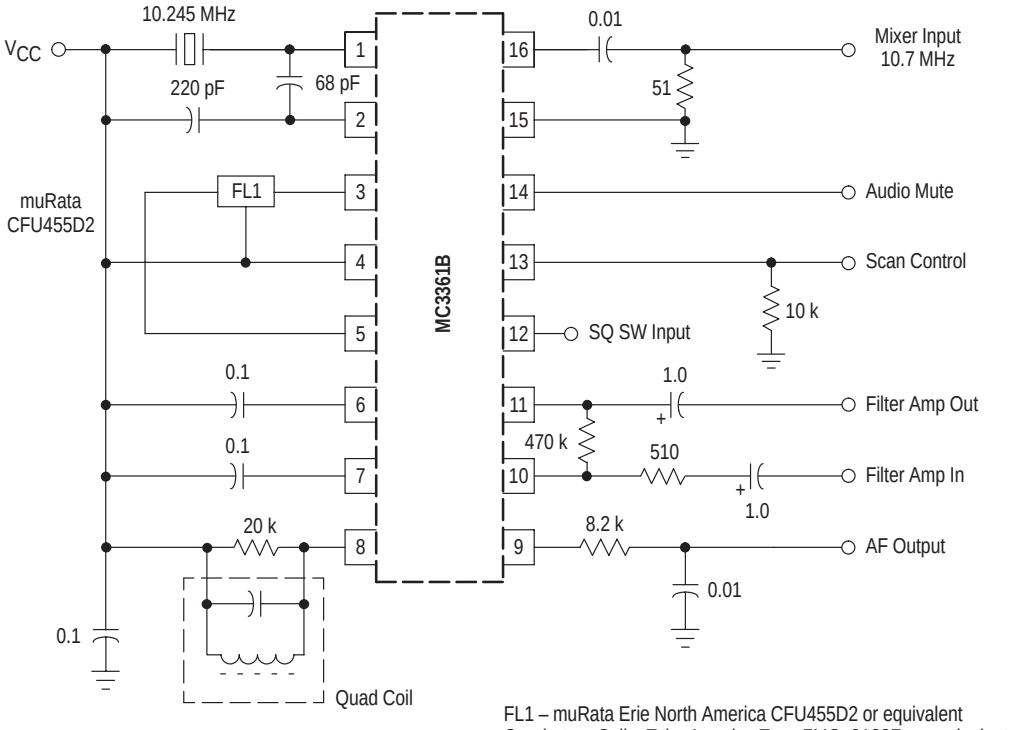
Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	10	Vdc
Operating Supply Voltage Range	4	V_{CC}	2.0 to 8.0	Vdc
Detector Input Voltage	8	–	1.0	V_{pp}
Input Voltage ($V_{CC} \geqslant$ 4.0 V)	16	V_{16}	1.0	V_{rms}
Mute Function	14	V_{14}	–0.5 to 5.0	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	–30 to 70	°C
Storage Temperature Range	–	T_{stg}	–65 to 150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, f_o = 10.7 MHz, $\Delta f = \pm$ 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current (No Signal)	4				mA
Squelch “Off”		2.9	3.9	4.9	
Squelch “On”		4.4	5.4	6.4	
Recovered Audio Output Voltage (V_{in} = 10 mVrms)	9	130	160	200	mVrms
Input Limiting Voltage (–3.0 dB Limiting)	16	–	2.6	6.0	μV
Total Harmonic Distortion	9	–	0.86	–	%
Recovered Output Voltage (No Input Signal)	9	60	120	250	mVrms
Drop Voltage AF Gain Loss	9	–3.0	–0.6	–	dB
Detector Output Impedance	–	–	450	–	Ω
Filter Gain (10 kHz) (V_{in} = 0.3 mVrms)	–	40	50	–	dB
Filter Output Voltage	11	1.0	1.3	1.6	Vdc
Mute Function Low	14	–	30	50	Ω
Mute Function High	14	1.0	11	–	MΩ
Scan Function Low (Mute “Off”) (V_{12} = 1.0 Vdc)	13	–	0	0.4	Vdc
Scan Function High (Mute “On”) (V_{12} = Gnd)	13	3.0	3.5	–	Vdc
Trigger Hysteresis	–	–	45	100	mV
Mixer Conversion Gain	3	–	28	–	dB
Mixer Input Resistance	16	–	3.3	–	kΩ
Mixer Input Capacitance	16	–	2.2	–	pF

Figure 1. Test Circuit



FL1 – muRata Erie North America CFU455D2 or equivalent
Quadrature Coil – Toko America Type 7MC–8128Z or equivalent
C – µF, unless noted

Figure 2. Audio Output, Distortion versus Supply Voltage

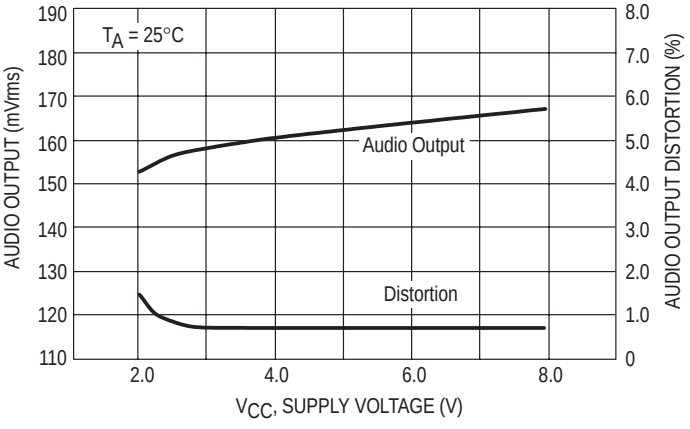
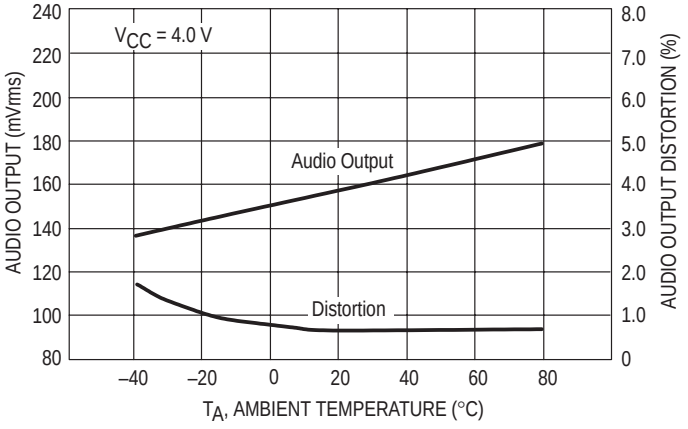


Figure 3. Audio Output, Distortion versus Temperature



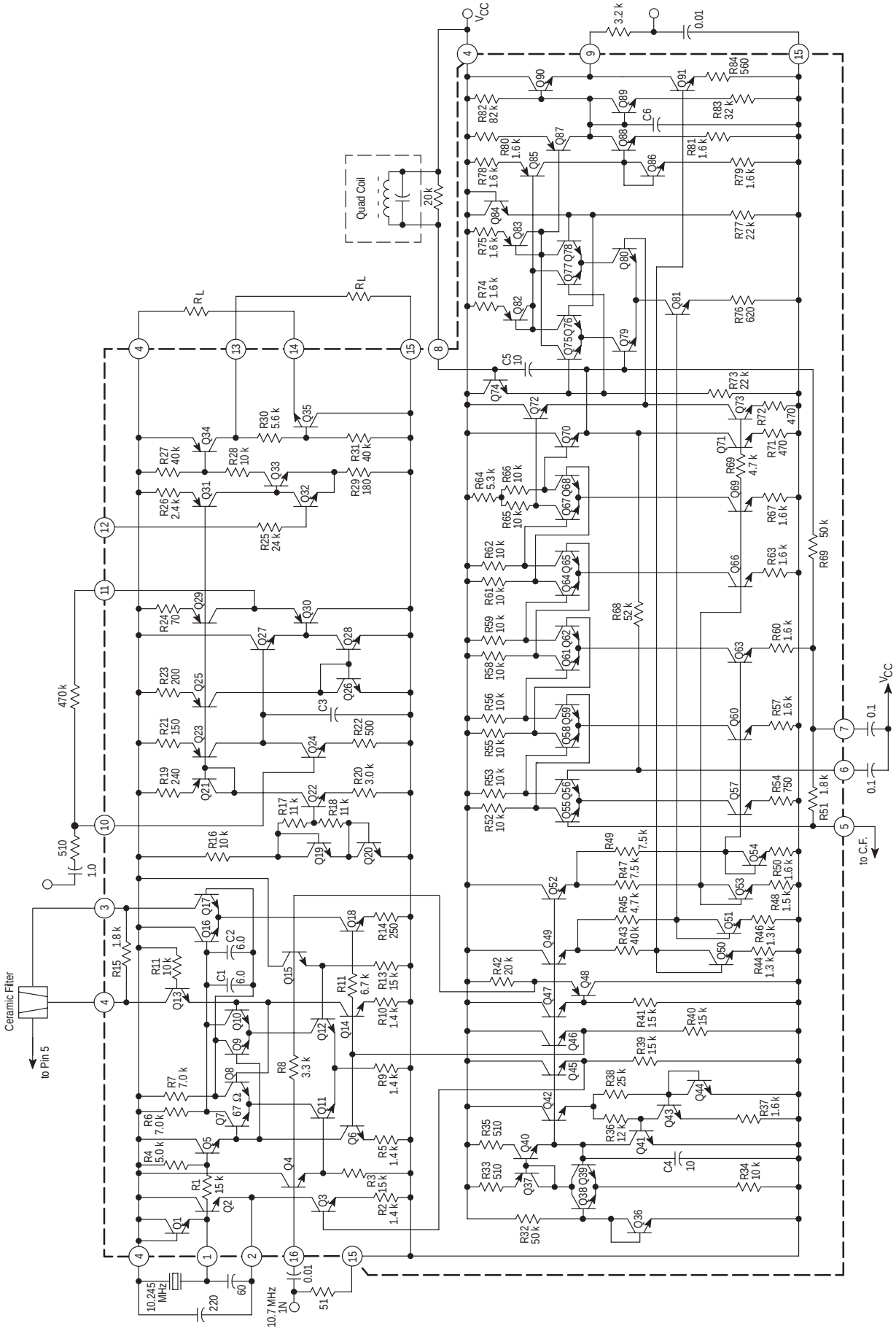


Figure 4. Low Voltage Low Power Narrowband FM IF

Figure 5. Input Limiting Voltage

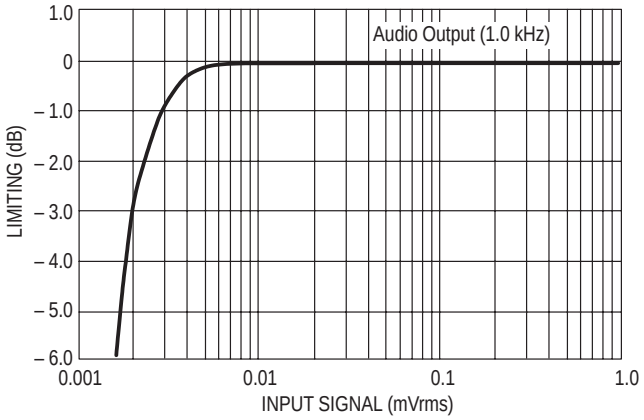


Figure 6. Overall Gain, Noise and AM Rejection

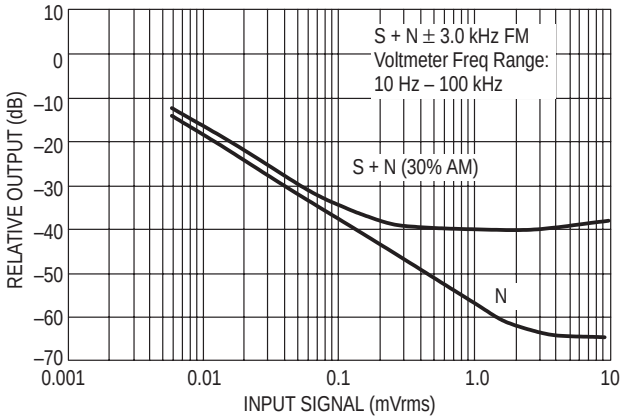


Figure 7. Filter Amp Response

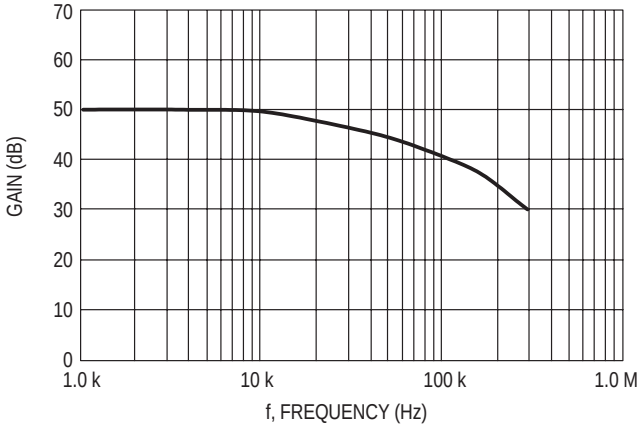


Figure 8. Filter Amp Gain

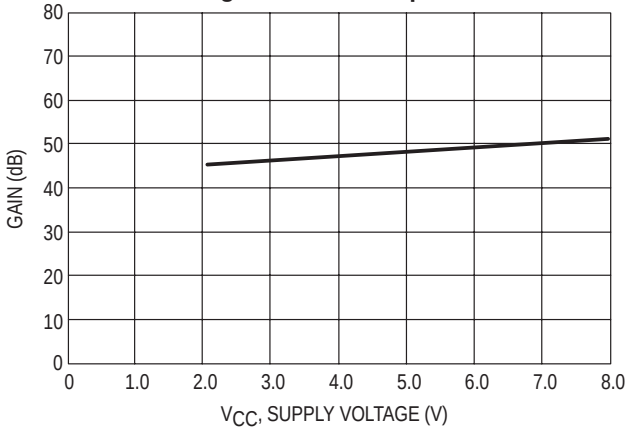


Figure 9. Supply Current

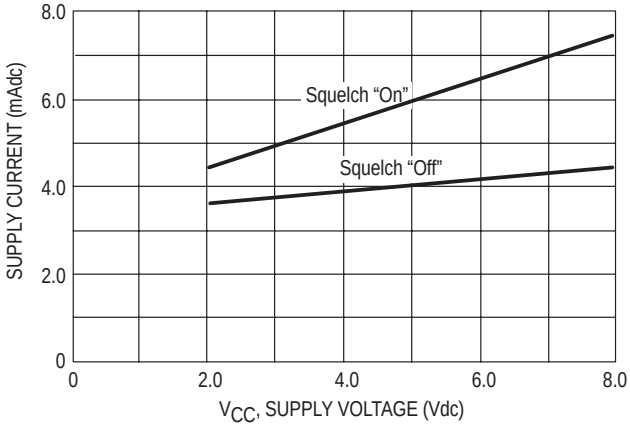
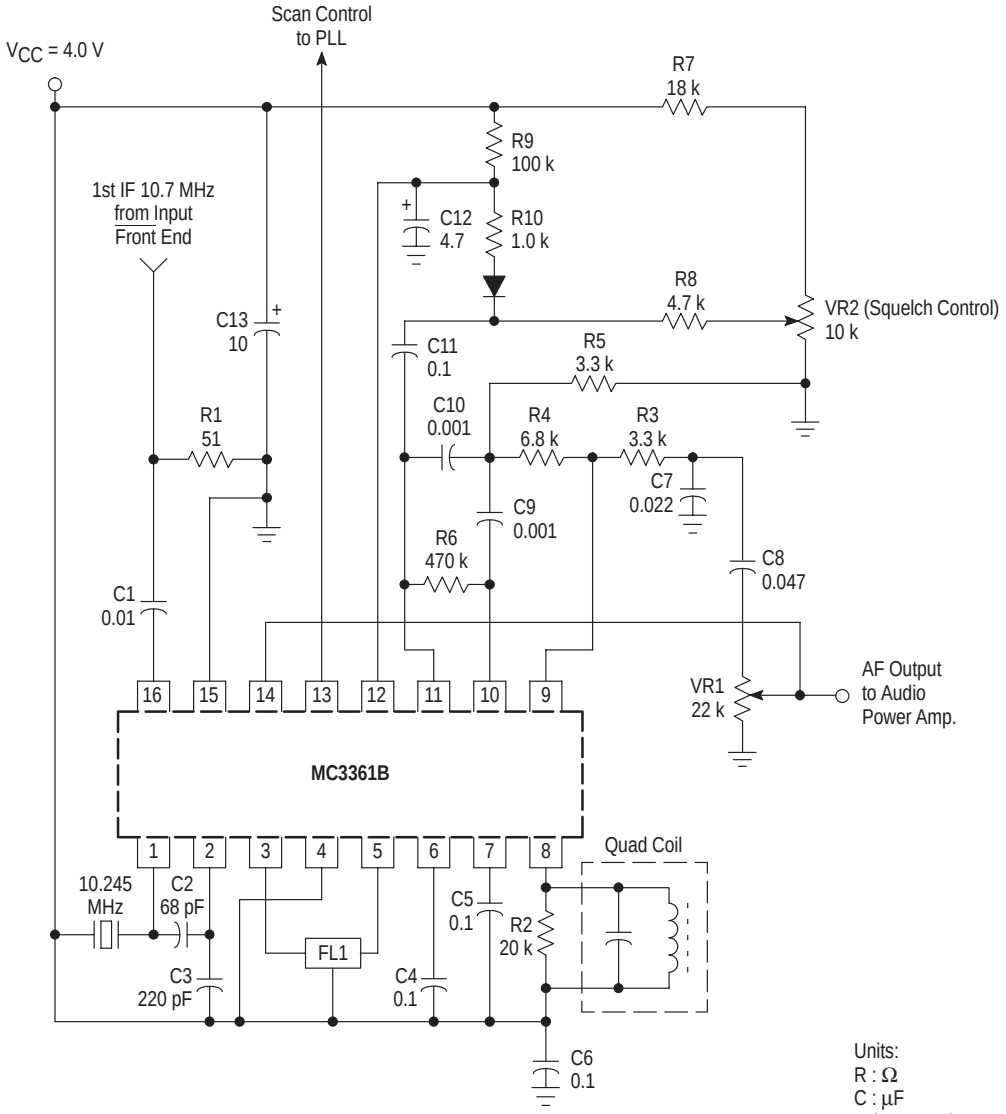


Figure 10. Simplified Application



FL1 – muRata Erie North America Type CFU455D2 or equivalent
Quadrature Coil – Toko America Type 7MC–8128Z or equivalent

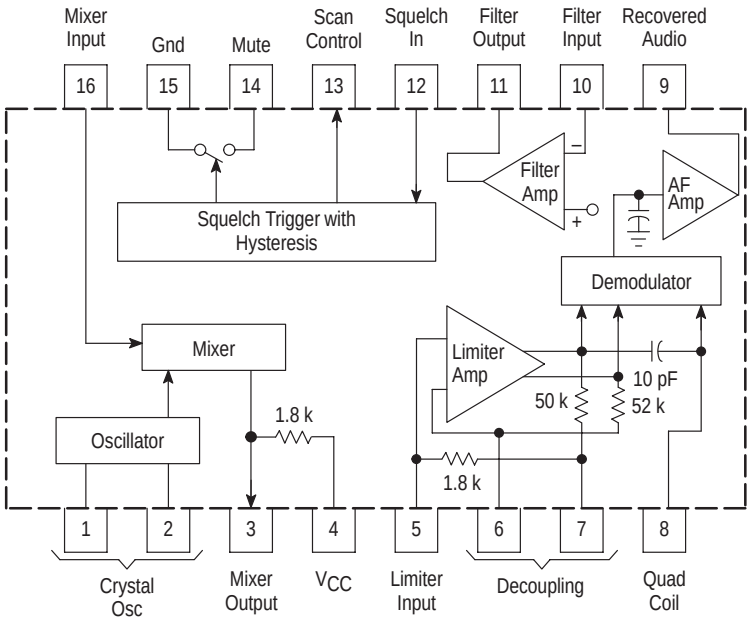
MOTOROLA

Low Power Narrowband FM IF

The MC3361C includes an Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control and Mute Switch. This device is designed for use in FM dual conversion communications equipment.

- Operates from 2.0 to 8.0 V Supply
- Low Drain Current 2.8 mA Typical @ V_{CC} = 4.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage –3.0 dB = 2.6 μV Typical
- Low Number of External Parts Required
- Operating Frequency Up to 60 MHz
- Full ESD Protection

Representative Block Diagram

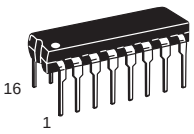


This device contains 92 active transistors.

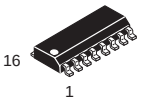
MC3361C

LOW POWER NARROWBAND FM IF

SEMICONDUCTOR TECHNICAL DATA

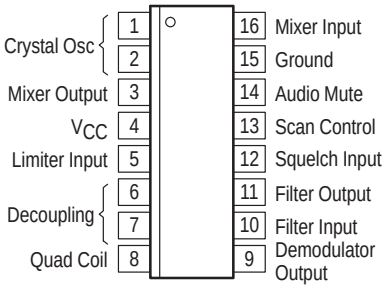


P SUFFIX
PLASTIC PACKAGE
CASE 648
Not Recommended For New Designs



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16, Tape & Reel Only)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3361CDR2	T_A = –30 to 70°C	SO–16

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

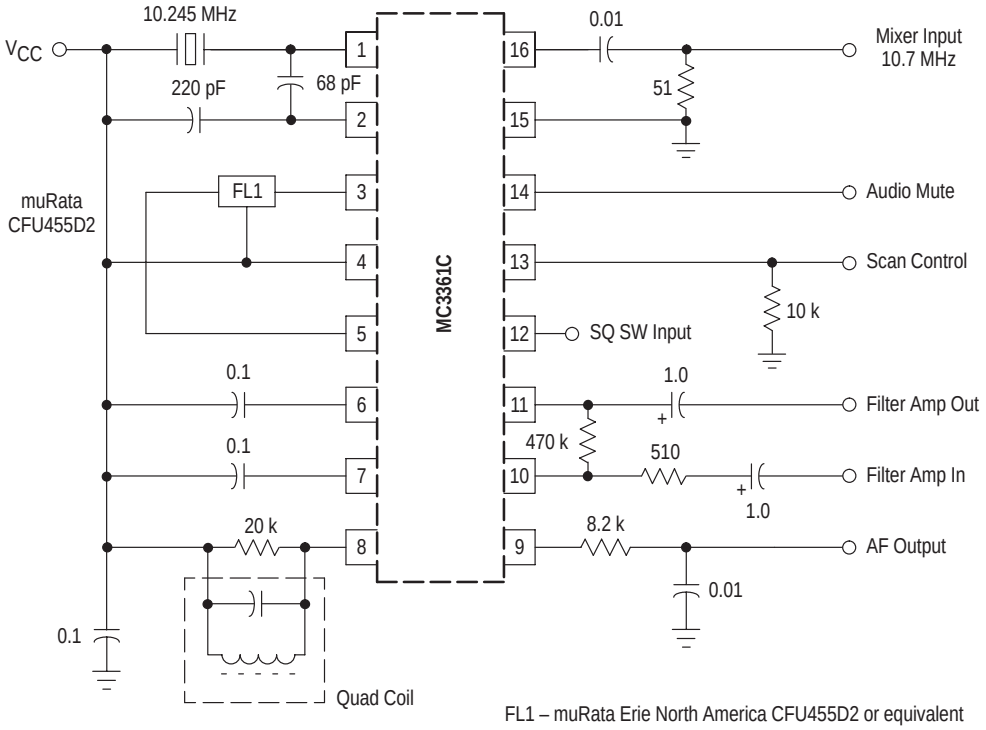
Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	10	Vdc
Operating Supply Voltage Range	4	V_{CC}	2.0 to 8.0	Vdc
Detector Input Voltage	8	–	1.0	Vp–p
Input Voltage ($V_{CC} \geqslant$ 4.0 V)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	–0.5 to 5.0	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	–30 to 70	°C
Storage Temperature Range	–	T_{stg}	–65 to 150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, f_o = 10.7 MHz, $\Delta f = \pm$ 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current (No Signal) Squelch “Off” Squelch “On”	4	 2.0 3.7	 2.8 5.2	 3.5 6.3	mA
Recovered Audio Output Voltage (V_{in} = 10 mVrms)	9	130	170	210	mVrms
Input Limiting Voltage (–3.0 dB Limiting)	16	–	2.6	6.0	μV
Total Harmonic Distortion	9	–	0.86	–	%
Recovered Output Voltage (No Input Signal)	9	60	190	350	mVrms
Drop Voltage AF Gain Loss	9	–3.0	–0.6	–	dB
Detector Output Impedance	–	–	450	–	Ω
Filter Gain (10 kHz) (V_{in} = 0.3 mVrms)	–	40	50	–	dB
Filter Output Voltage	11	0.5	0.7	0.9	Vdc
Mute Function Low	14	–	30	50	Ω
Mute Function High	14	1.0	11	–	MΩ
Scan Function Low (Mute “Off”) (V_{12} = 1.0 Vdc)	13	–	0	0.4	Vdc
Scan Function High (Mute “On”) (V_{12} = Gnd)	13	3.0	3.9	–	Vdc
Trigger Hysteresis	–	–	45	100	mV
Mixer Conversion Gain	3	–	28	–	dB
Mixer Input Resistance	16	–	3.3	–	kΩ
Mixer Input Capacitance	16	–	9.0	–	pF

Figure 1. Test Circuit



FL1 – muRata Erie North America CFU455D2 or equivalent

Quadrature Coil – Toko America Type 7MC–8128Z or equivalent

C – μF, unless noted

Figure 2. Audio Output, Distortion versus Supply Voltage

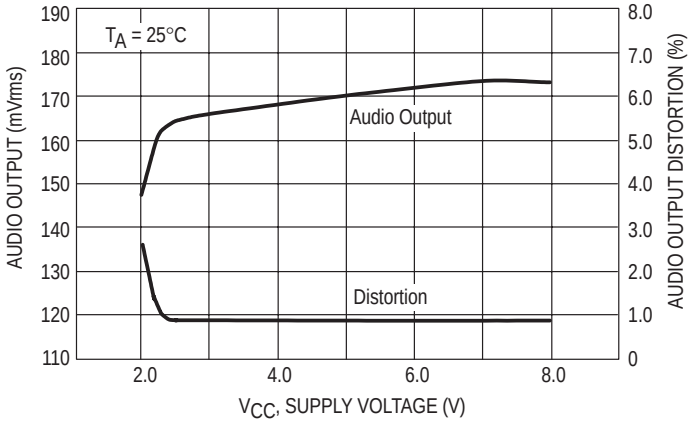
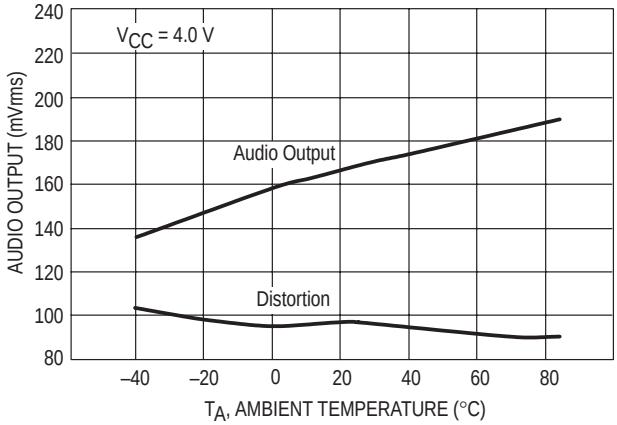


Figure 3. Audio Output, Distortion versus Temperature



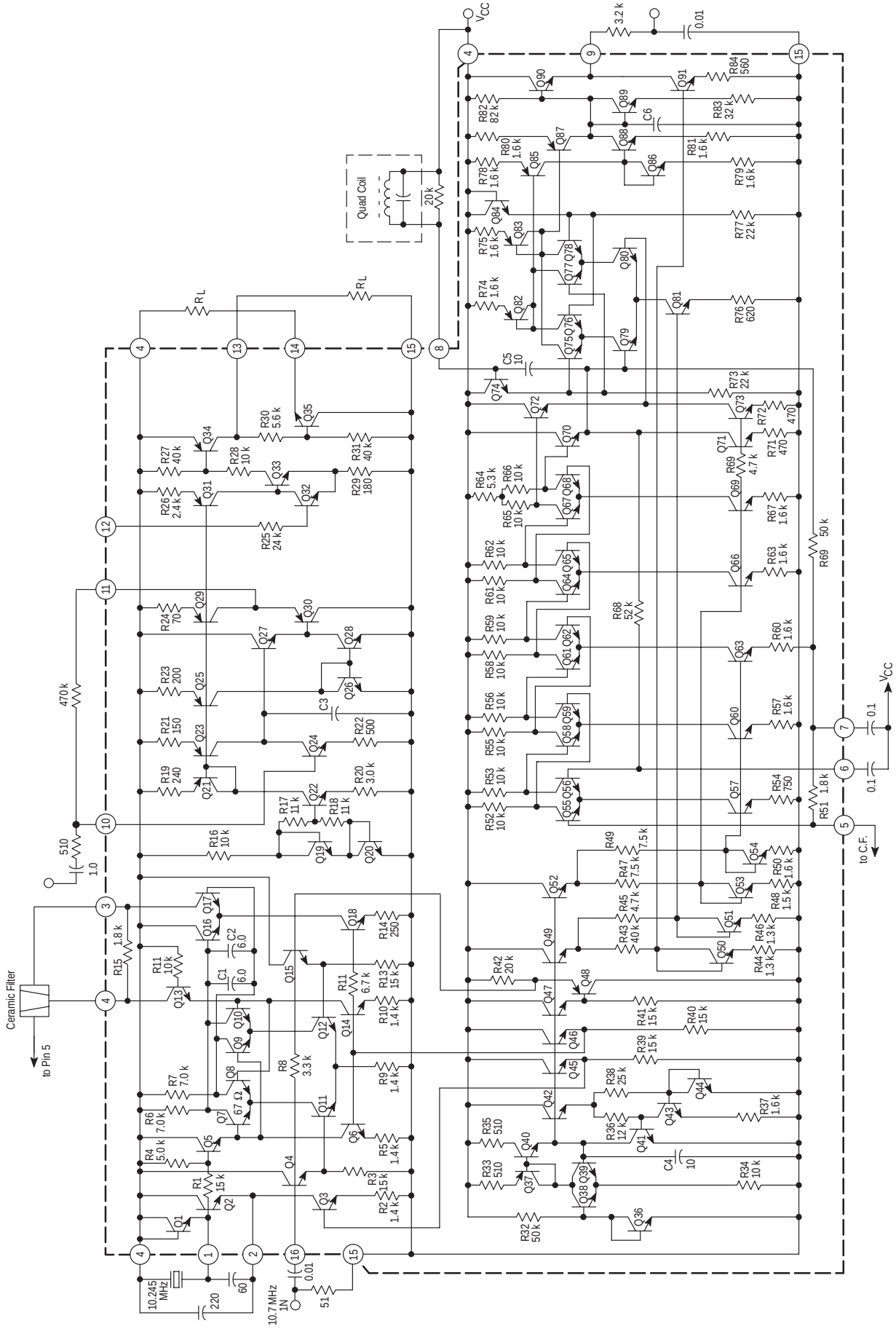


Figure 4. Low Voltage Low Power Narrowband FM IF

Figure 5. Input Limiting Voltage

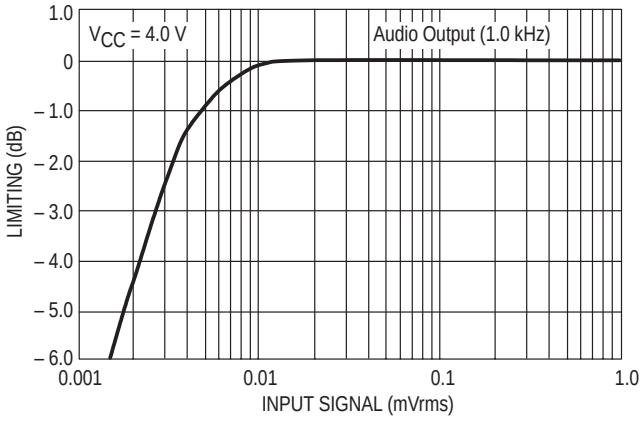


Figure 6. Overall Gain, Noise and AM Rejection

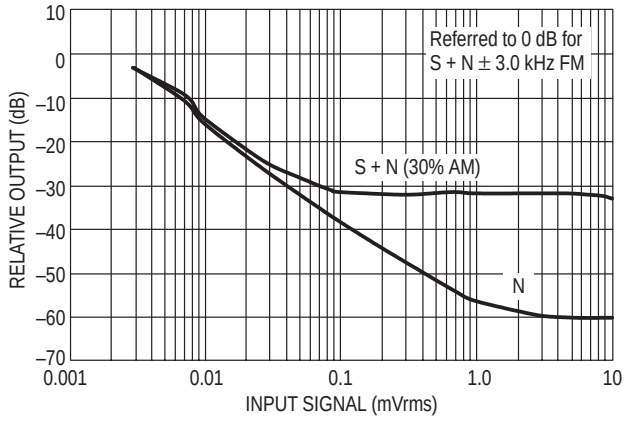


Figure 7. Filter Amp Response

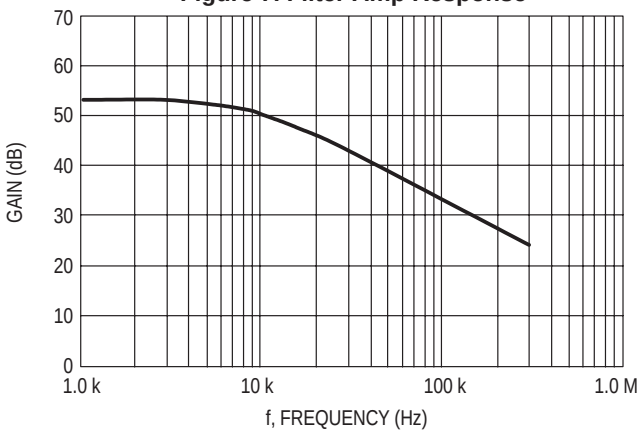


Figure 8. Filter Amp Gain

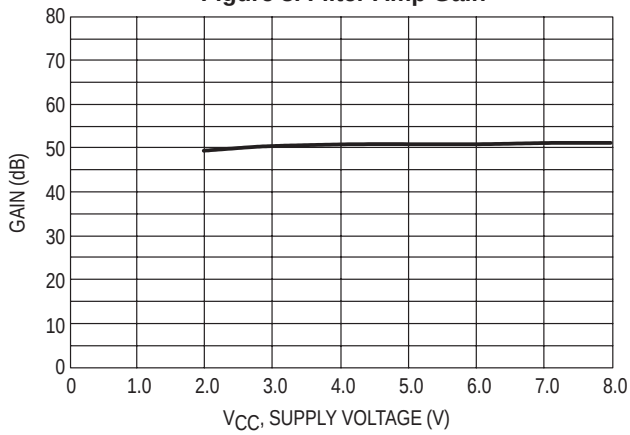


Figure 9. Supply Current

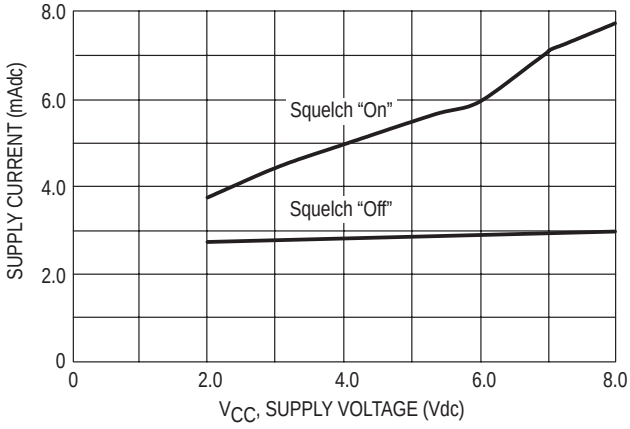
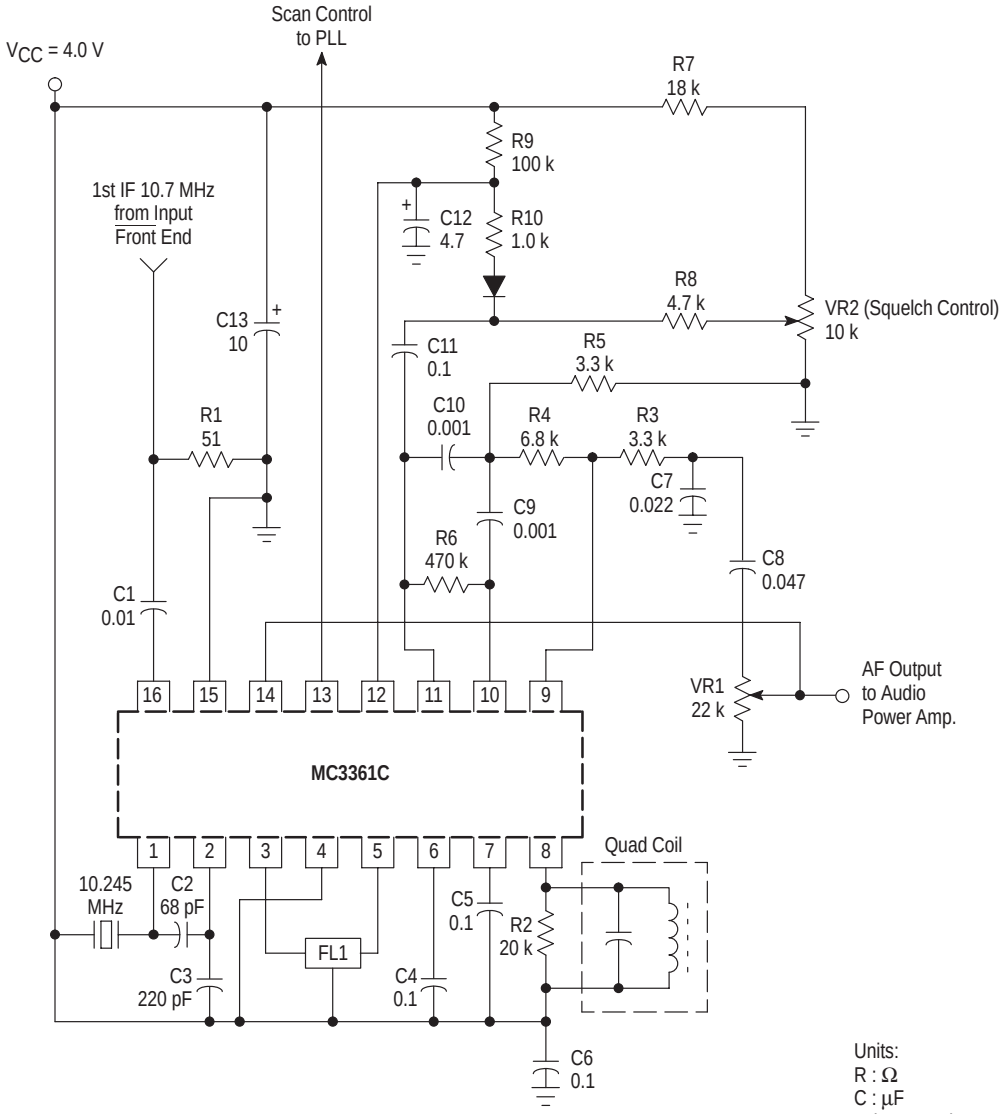


Figure 10. Simplified Application



FL1 – muRata Erie North America Type CFU455D2 or equivalent

Quadrature Coil – Toko America Type 7MC–8128Z or equivalent

MOTOROLA

MC3371
MC3372

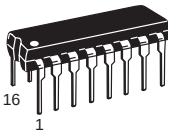
Low Power Narrowband FM IF

LOW POWER FM IF

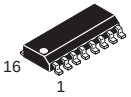
The MC3371 and MC3372 perform single conversion FM reception and consist of an oscillator, mixer, limiting IF amplifier, quadrature discriminator, active filter, squelch switch, and meter drive circuitry. These devices are designed for use in FM dual conversion communication equipment. The MC3371/MC3372 are similar to the MC3361/MC3357 FM IFs, except that a signal strength indicator replaces the scan function controlling driver which is in the MC3361/MC3357. The MC3371 is designed for the use of parallel LC components, while the MC3372 is designed for use with either a 455 kHz ceramic discriminator, or parallel LC components.

These devices also require fewer external parts than earlier products. The MC3371 and MC3372 are available in dual–in–line and surface mount packaging.

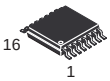
- Wide Operating Supply Voltage Range: V_{CC} = 2.0 to 9.0 V
- Input Limiting Voltage Sensitivity of –3.0 dB
- Low Drain Current: I_{CC} = 3.2 mA, @ V_{CC} = 4.0 V, Squelch Off
- Minimal Drain Current Increase When Squelched
- Signal Strength Indicator: 60 dB Dynamic Range
- Mixer Operating Frequency Up to 100 MHz
- Fewer External Parts Required than Earlier Devices



P SUFFIX
PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



DTB SUFFIX
PLASTIC PACKAGE
CASE 948F
(TSSOP–16)

MAXIMUM RATINGS

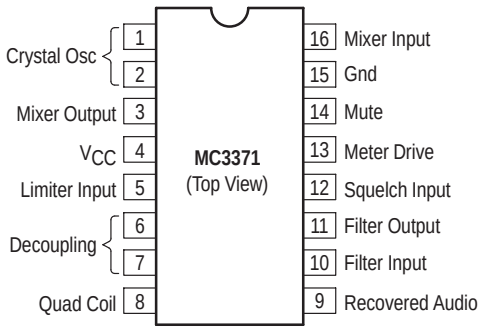
Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	10	Vdc
RF Input Voltage ($V_{CC} \geq$ 4.0 Vdc)	16	V16	1.0	Vrms
Detector Input Voltage	8	V8	1.0	Vpp
Squelch Input Voltage ($V_{CC} \geq$ 4.0 Vdc)	12	V12	6.0	Vdc
Mute Function	14	V_{14}	–0.7 to 10	V_{pk}
Mute Sink Current	14	I14	50	mA
Junction Temperature	–	T_J	150	°C
Storage Temperature Range	–	T_{stg}	–65 to +150	°C

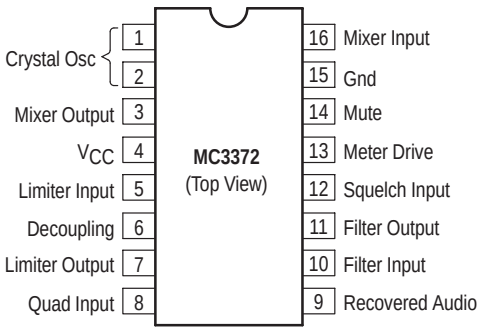
NOTES: 1. Devices should not be operated at these values. The "Recommended Operating Conditions" table provides conditions for actual device operation.
2. ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3371D	T_A = –30° to +70°C	SO–16
MC3371DTB		TSSOP–16
MC3371P		Plastic DIP
MC3372D		SO–16
MC3372DTB		TSSOP–16
MC3372P		Plastic DIP

PIN CONNECTIONS





RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Supply Voltage (@ T_A = 25°C) (–30°C ≤ T_A ≤ +75°C)	4	V_{CC}	2.0 to 9.0 2.4 to 9.0	Vdc
RF Input Voltage	16	V_{rf}	0.0005 to 10	mVrms
RF Input Frequency	16	f_{rf}	0.1 to 100	MHz
Oscillator Input Voltage	1	V_{local}	80 to 400	mVrms
Intermediate Frequency	–	f_{if}	455	kHz
Limiter Amp Input Voltage	5	V_{if}	0 to 400	mVrms
Filter Amp Input Voltage	10	V_{fa}	0.1 to 300	mVrms
Squelch Input Voltage	12	V_{sq}	0 or 2	Vdc
Mute Sink Current	14	I_{sq}	0.1 to 30	mA
Ambient Temperature Range	–	T_A	–30 to +70	°C

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, f_o = 58.1125 MHz, df = ±3.0 kHz, f_{mod} = 1.0 kHz, 50 Ω source, f_{local} = 57.6575 MHz, V_{local} = 0 dBm, T_A = 25°C, unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Input for 12 dB SINAD Matched Input – (See Figures 11, 12 and 13) Unmatched Input – (See Figures 1 and 2)	–	V_{SIN}	 – –	 1.0 5.0	 – 15	µVrms
Input for 20 dB NQS	–	V_{NQS}	–	3.5	–	µVrms
Recovered Audio Output Voltage V_{rf} = –30 dBm	–	AF_O	 120	 200	 320	mVrms
Recovered Audio Drop Voltage Loss Vrf = –30 dBm, V_{CC} = 4.0 V to 2.0 V	–	AF_{loss}	 –8.0	 –1.5	 –	dB
Meter Drive Output Voltage (No Modulation) V_{rf} = –100 dBm V_{rf} = –70 dBm V_{rf} = –40 dBm	13	M_{Drv} MV1 MV2 MV3	 – 1.1 2.0	 0.3 1.5 2.5	 0.5 1.9 3.1	Vdc
Filter Amp Gain R_S = 600 Ω , f_S = 10 kHz, V_{fa} = 1.0 mVrms	–	$A_{V(Amp)}$	 47	 50	 –	dB
Mixer Conversion Gain V_{rf} = –40 dBm, R_L = 1.8 kΩ	–	$A_{V(Mix)}$	 14	 20	 –	dB
Signal to Noise Ratio V_{rf} = –30 dBm	–	s/n	 36	 67	 –	dB
Total Harmonic Distortion V_{rf} = –30 dBm, BW = 400 Hz to 30 kHz	–	THD	 –	 0.6	 3.4	%
Detector Output Impedance	9	Z_O	–	450	–	Ω
Detector Output Voltage (No Modulation) V_{rf} = –30 dBm	9	DV_O	 –	 1.45	 –	Vdc
Meter Drive V_{rf} = –100 to –40 dBm	13	M_O	 –	 0.8	 –	µA/dB
Meter Drive Dynamic Range RF_{In} IF_{In} (455 kHz)	13	MVD	 – –	 60 80	 – –	dB
Mixer Third Order Input Intercept Point f1 = 58.125 MHz f2 = 58.1375 MHz	–	ITO_{Mix}	 –	 –22	 –	dBm
Mixer Input Resistance	16	R_{in}	–	3.3	–	kΩ
Mixer Input Capacitance	16	C_{in}	–	2.2	–	pF

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, T_A = 25°C, unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Drain Current (No Input Signal)	4					mA
Squelch Off, V_{sq} = 2.0 Vdc		Icc1	–	3.2	4.2	
Squelch On, V_{sq} = 0 Vdc		Icc2	–	3.6	4.8	
Squelch Off, V_{CC} = 2.0 to 9.0 V		dIcc1	–	1.0	2.0	
Detector Output (No Input Signal)	9	V9				Vdc
DC Voltage, V8 = V_{CC}			0.9	1.6	2.3	
Filter Output (No Input Signal)	11					Vdc
DC Voltage		V11	1.5	2.5	3.5	
Voltage Change, V_{CC} = 2.0 to 9.0 V		dV11	2.0	5.0	8.0	
Trigger Hysteresis	–	Hys	34	57	80	mV

Figure 1. MC3371 Functional Block Diagram and Test Fixture Schematic

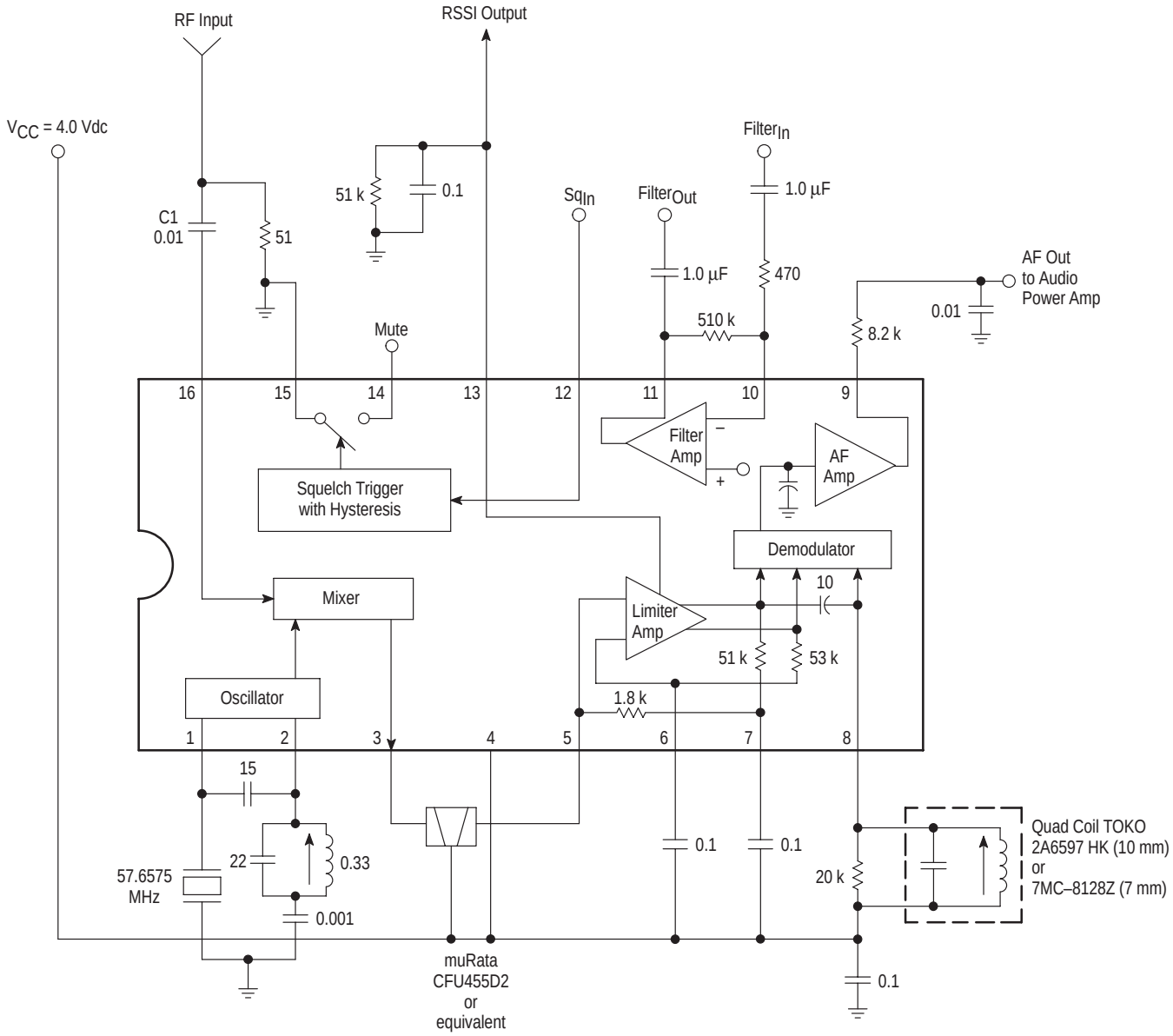
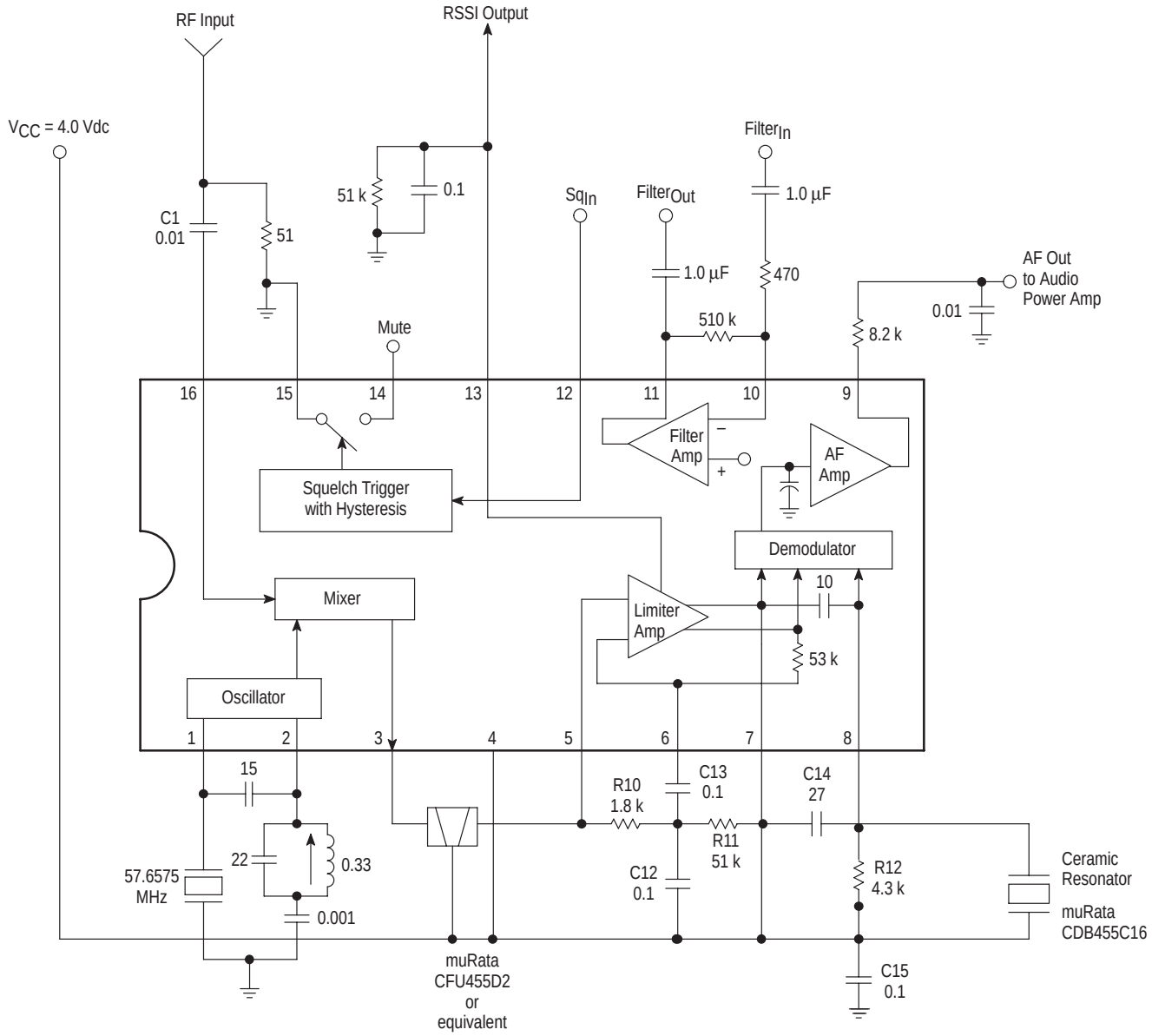


Figure 2. MC3372 Functional Block Diagram and Test Fixture Schematic



TYPICAL CURVES

(Unmatched Input)

Figure 3. Total Harmonic Distortion versus Temperature

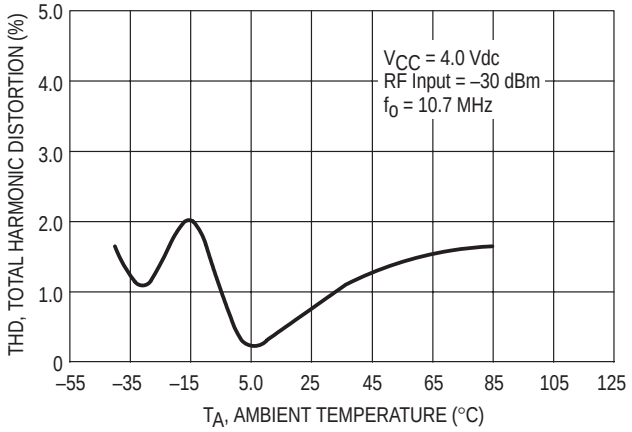


Figure 4. RSSI versus RF Input

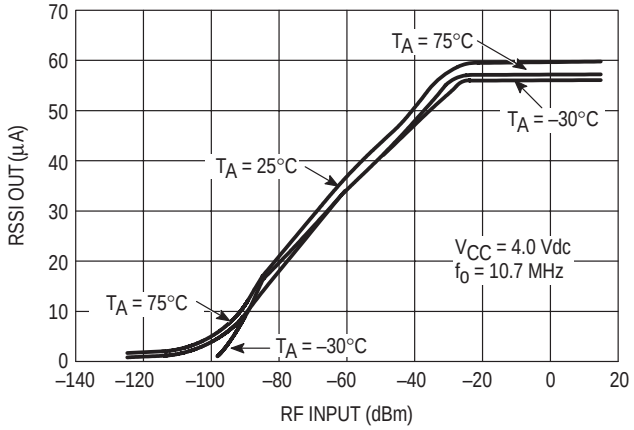


Figure 5. RSSI Output versus Temperature

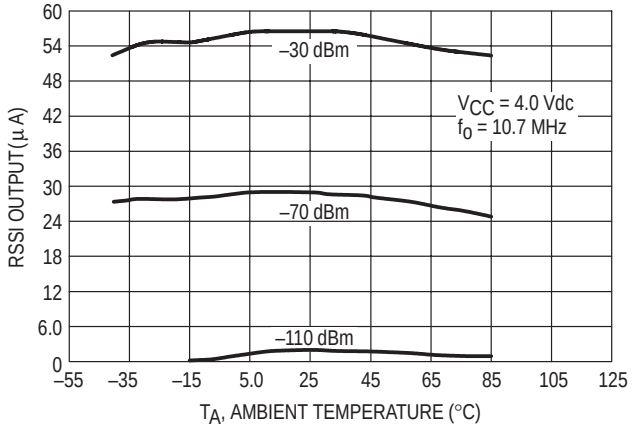


Figure 6. Mixer Output versus RF Input

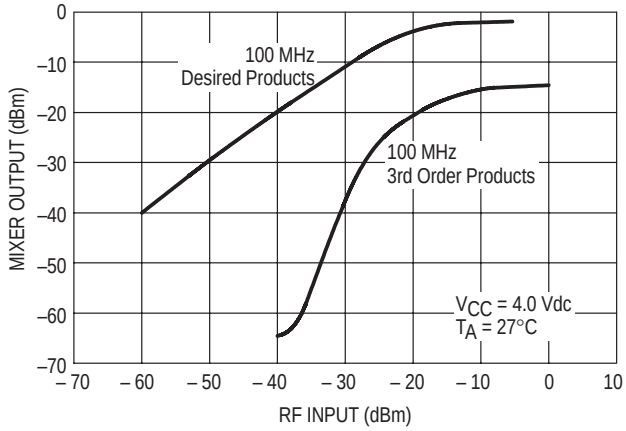


Figure 7. Mixer Gain versus Supply Voltage

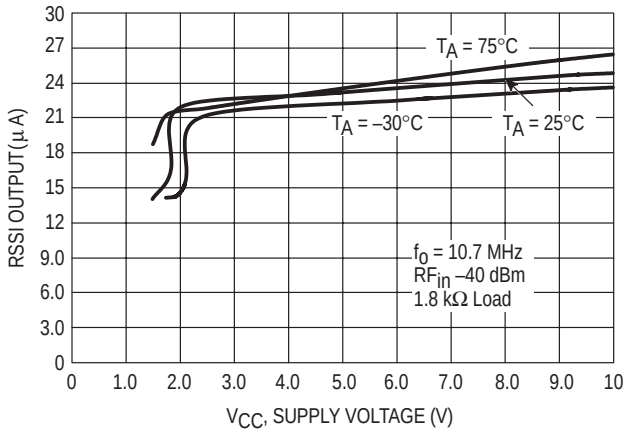
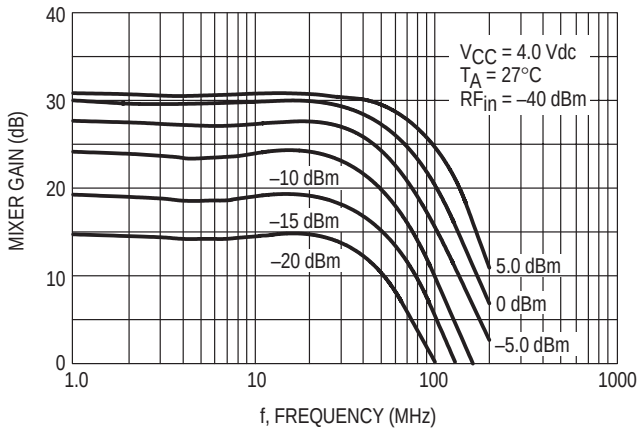
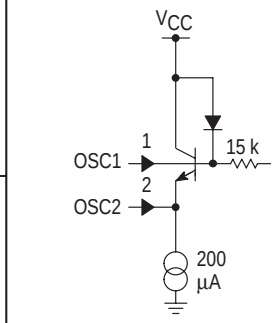
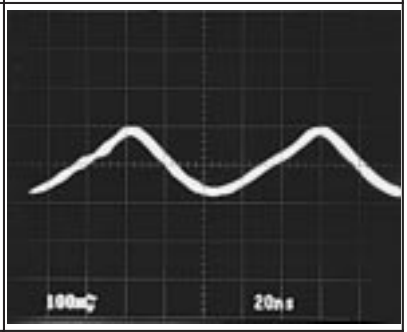
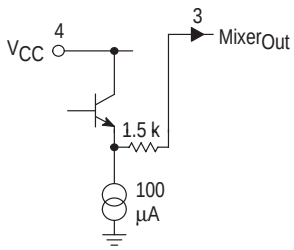
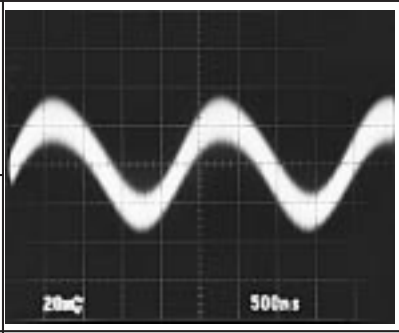
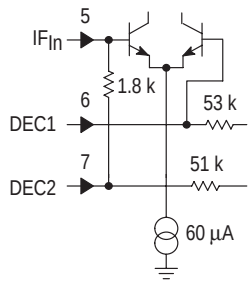
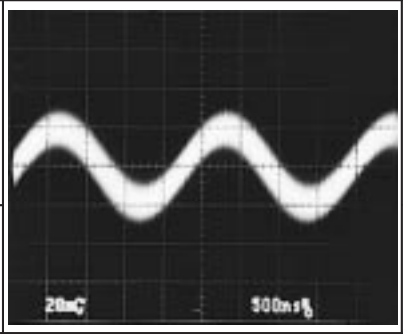
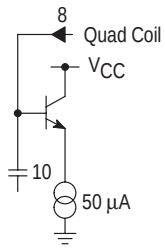
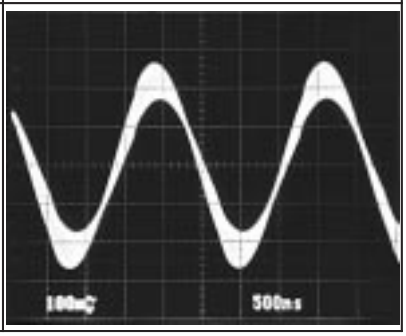


Figure 8. Mixer Gain versus Frequency



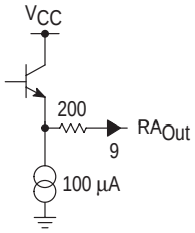
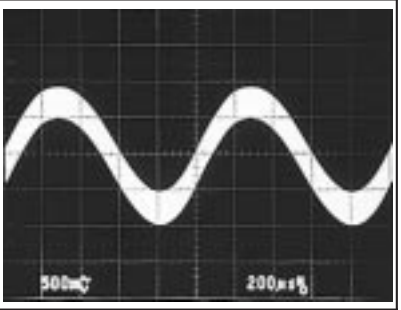
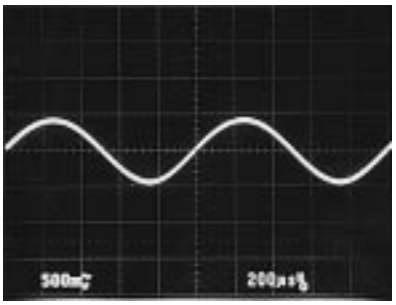
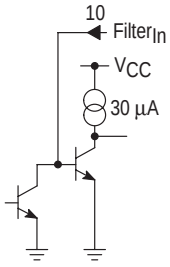
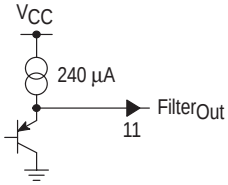
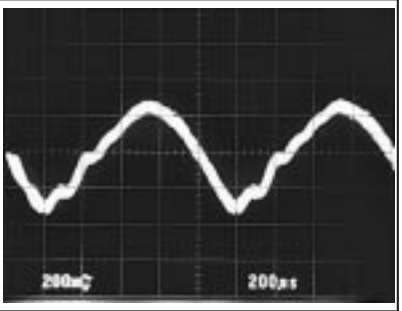
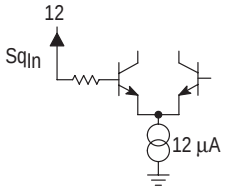
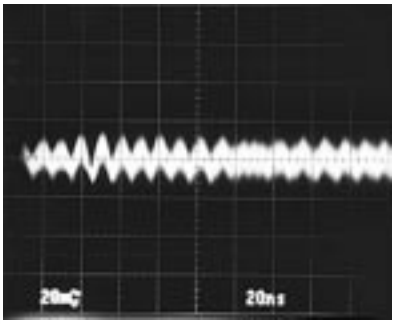
MC3371 PIN FUNCTION DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 11).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
1	OSC1		The base of the Colpitts oscillator. Use a high impedance and low capacitance probe or a “sniffer” to view the wave–form without altering the frequency. Typical level is 450 mVpp.	
2	OSC2		The emitter of the Colpitts oscillator. Typical signal level is 200 mVpp. Note that the signal is somewhat distorted compared to that on Pin 1.	
3	MX_{Out}		Output of the Mixer. Riding on the 455 kHz is the RF carrier component. The typical level is approximately 60 mVpp.	
4	V_{CC}		Supply Voltage –2.0 to 9.0 Vdc is the operating range. V_{CC} is decoupled to ground.	
5	IF_{In}		Input to the IF amplifier after passing through the 455 kHz ceramic filter. The signal is attenuated by the filter. The typical level is approximately 50 mVpp.	
6 7	DEC1 DEC2		IF Decoupling. External 0.1 µF capacitors connected to V_{CC}.	
8	Quad Coil		Quadrature Tuning Coil. Composite (not yet demodulated) 455 kHz IF signal is present. The typical level is 500 mVpp.	

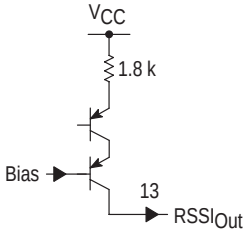
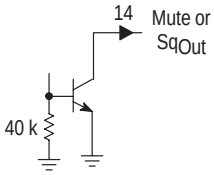
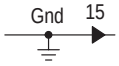
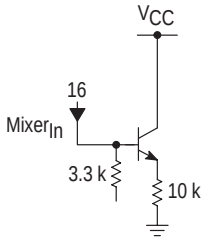
MC3371 PIN FUNCTION DESCRIPTION (continued)

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 11).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
9	RA		Recovered Audio. This is a composite FM demodulated output having signal and carrier component. The typical level is 1.4 Vpp.	
			The filtered recovered audio has the carrier component removed and is typically 800 mVpp.	
10	Fil_{In}		Filter Amplifier Input	
11	Fil_{Out}		Filter Amplifier Output. The typical signal level is 400 mVpp.	
12	Sq_{In}		Squelch Input. See discussion in application text.	

MC3371 PIN FUNCTION DESCRIPTION (continued)

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 μV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 11).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
13	RSSI		RSSI Output. Referred to as the Received Signal Strength Indicator or RSSI. The chip sources up to 60 μA over the linear 60 dB range. This pin may be used many ways, such as: AGC, meter drive and carrier triggered squelch circuit.	
14	MUTE		Mute Output. See discussion in application text.	
15	Gnd		Ground. The ground area should be continuous and unbroken. In a two–sided layout, the component side has the ground plane. In a one–sided layout, the ground plane fills around the traces on the circuit side of the board and is not interrupted.	
16	MIX_{In}		Mixer Input – Series Input Impedance: @ 10 MHz: 309 – j33 Ω @ 45 MHz: 200 – j13 Ω	

*Other pins are the same as pins in MC3371.

MC3372 PIN FUNCTION DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3372 at f_{RF} = 45 MHz (see Figure 13).

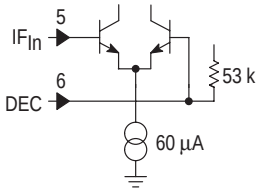
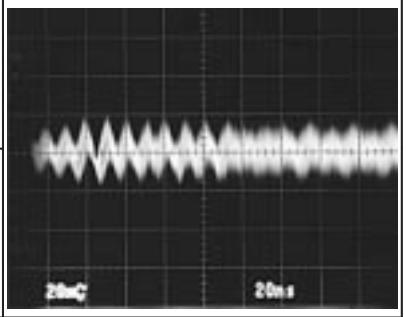
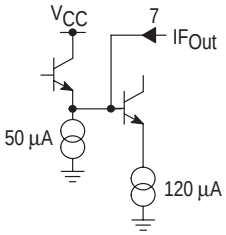
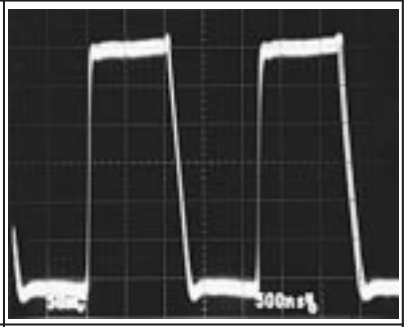
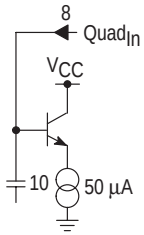
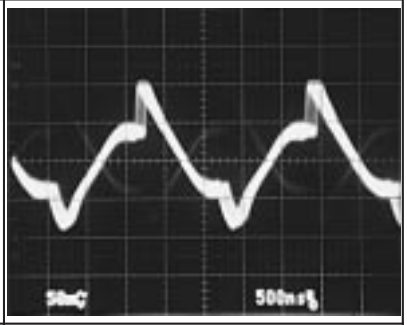
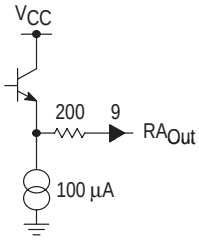
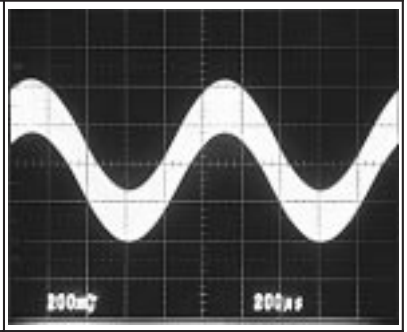
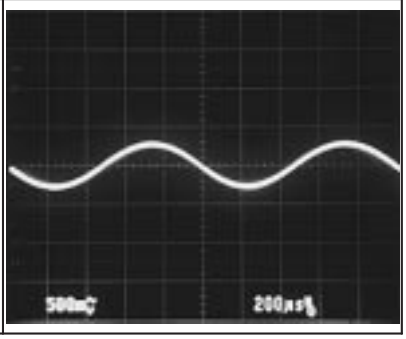
Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
5	IF_{In}		IF Amplifier Input	
6	DEC1		IF Decoupling. External 0.1 µF capacitors connected to V_{CC}.	
7	IF_{Out}		IF Amplifier Output Signal level is typically 300 mVpp.	
8	$Quad_{In}$		Quadrature Detector Input. Signal level is typically 150 mVpp.	
9	RA		Recovered Audio. This is a composite FM demodulated output having signal and carrier components. Typical level is 800 mVpp.	
			The filtered recovered audio has the carrier signal removed and is typically 500 mVpp.	

Figure 9. MC3371 Circuit Schematic

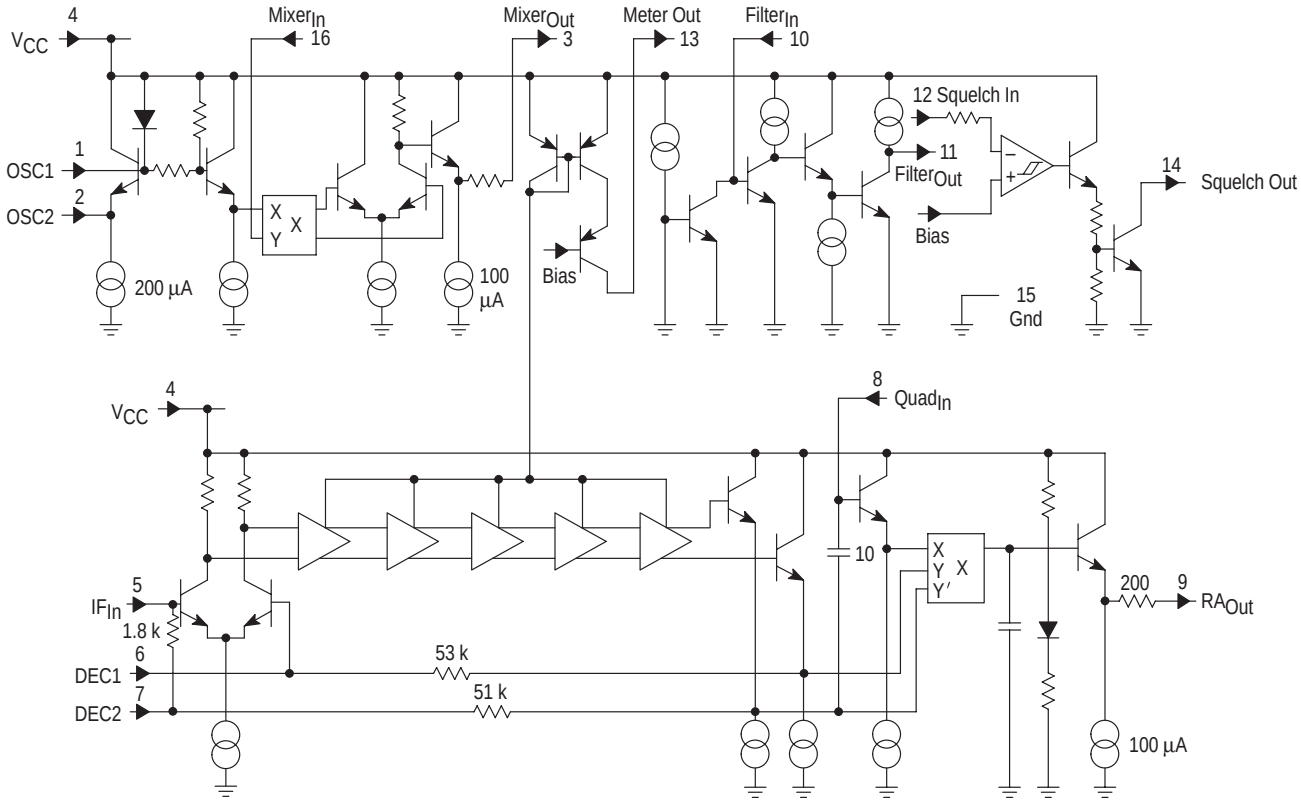
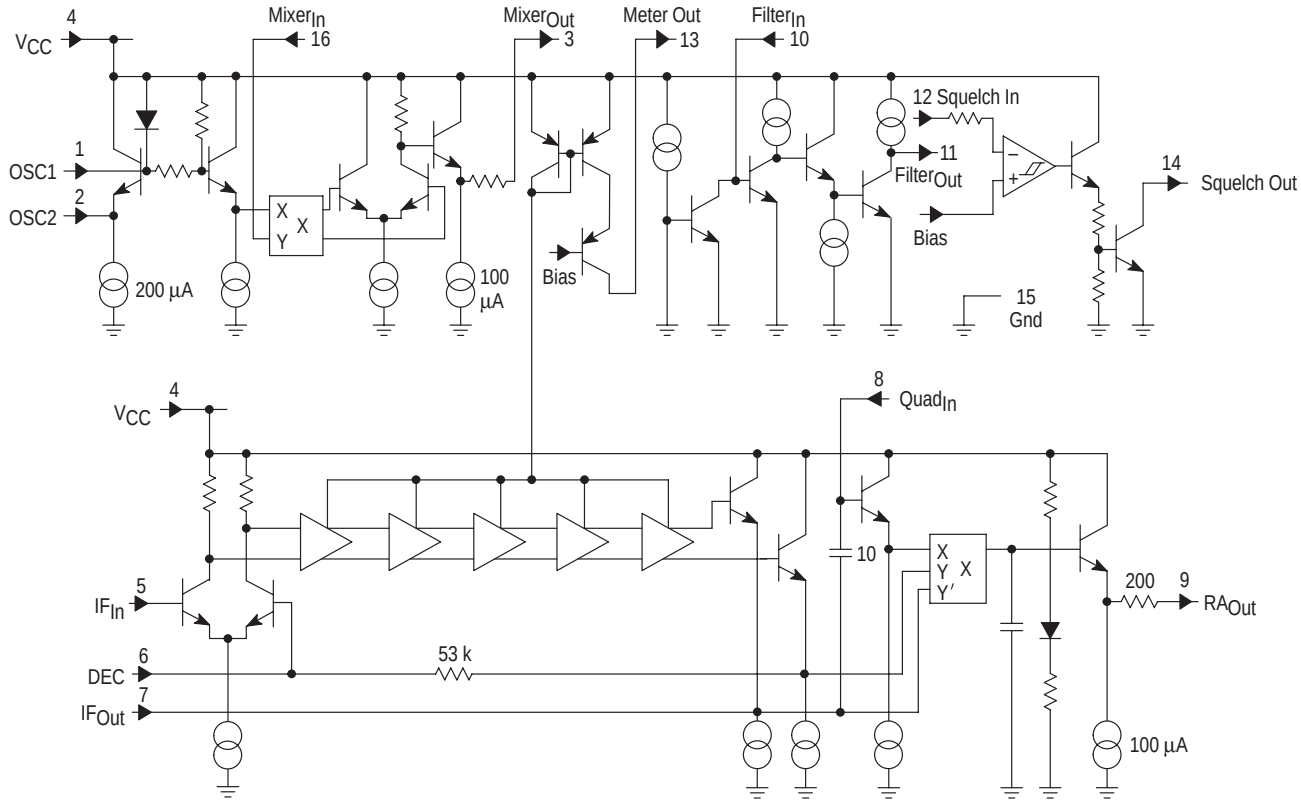


Figure 10. MC3372 Circuit Schematic



CIRCUIT DESCRIPTION

The MC3371 and MC3372 are low power narrowband FM receivers with an operating frequency of up to 60 MHz. Its low voltage design provides low power drain, excellent sensitivity, and good image rejection in narrowband voice and data link applications.

This part combines a mixer, an IF (intermediate frequency) limiter with a logarithmic response signal strength indicator, a quadrature detector, an active filter and a squelch trigger circuit. In a typical application, the mixer amplifier converts an RF input signal to a 455 kHz IF signal. Passing through an external bandpass filter, the IF signal is fed into a limiting amplifier and detection circuit where the audio signal is recovered. A conventional quadrature detector is used.

The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch switch is used to mute the audio when noise or a tone is present. The input signal level is monitored by a meter drive circuit which detects the amount of IF signal in the limiting amplifier.

APPLICATIONS INFORMATION

The oscillator is an internally biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1 and 2 respectively. This oscillator can be run under crystal control. For fundamental mode crystals use crystal characterized parallel resonant for 32 pF load. For higher frequencies, use 3rd overtone series mode type crystals. The coil (L2) and resistor RD (R13) are needed to ensure proper and stable operation at the LO frequency (see Figure 13, 45 MHz application circuit).

The mixer is doubly balanced to reduce spurious radiation. Conversion gain stated in the AC Electrical Characteristics table is typically 20 dB. This power gain measurement was made under stable conditions using a 50 Ω source at the input and an external load provided by a 455 kHz ceramic filter at the mixer output which is connected to the V_{CC} (Pin 4) and IF input (Pin 5). The filter impedance closely matches the 1.8 kΩ internal load resistance at Pin 3 (mixer output). Since the input impedance at Pin 16 is strongly influenced by a 3.3 kΩ internal biasing resistor and has a low capacitance, the useful gain is actually much higher than shown by the standard power gain measurement. The Smith Chart plot in Figure 17 shows the measured mixer input impedance versus input frequency with the mixer input matched to a 50 Ω source impedance at the given frequencies. In order to assure stable operation under matched conditions, it is necessary to provide a shunt resistor to ground. Figures 11, 12 and 13 show the input networks used to derive the mixer input impedance data.

Following the mixer, a ceramic bandpass filter is recommended for IF filtering (i.e. 455 kHz types having a bandwidth of ±2.0 kHz to ±15 kHz with an input and output impedance from 1.5 kΩ to 2.0 kΩ). The 6 stage limiting IF amplifier has approximately 92 dB of gain. The MC3371 and MC3372 are different in the limiter and quadrature detector circuits. The MC3371 has a 1.8 kΩ and a 51 kΩ resistor providing internal dc biasing and the output of the limiter is internally connected, both directly and through a 10 pF capacitor to the quadrature detector; whereas, in the MC3372 these components are not provided internally. Thus, in the MC3371, no external components are necessary to match the 455 kHz ceramic filter, while in the MC3372, external 1.8 kΩ and 51 kΩ biasing resistors are needed between Pins 5 and 7, respectively (see Figures 12 and 13).

In the MC3371, a parallel LCR quadrature tank circuit is connected externally from Pin 8 to V_{CC} (similar to the MC3361). In the MC3372, a quadrature capacitor is needed externally from Pin 7 to Pin 8 and a parallel LC or a ceramic discriminator with a damping resistor is also needed from Pin 8 to V_{CC} (similar to the MC3357). The above external quadrature circuitry provides 90° phase shift at the IF center frequency and enables recovered audio.

The damping resistor determines the peak separation of the detector and is somewhat critical. As the resistor is decreased, the separation and the bandwidth is increased but the recovered audio is decreased. Receiver sensitivity is dependent on the value of this resistor and the bandwidth of the 455 kHz ceramic filter.

On the chip the composite recovered audio, consisting of carrier component and modulating signal, is passed through a low pass filter amplifier to reduce the carrier component and then is fed to Pin 9 which has an output impedance of 450 Ω. The signal still requires further filtering to eliminate the carrier component, deemphasis, volume control, and further amplification before driving a loudspeaker. The relative level of the composite recovered audio signal at Pin 9 should be considered for proper interaction with an audio post amplifier and a given load element. The MC13060 is recommended as a low power audio amplifier.

The meter output indicates the strength of the IF level and the output current is proportional to the logarithm of the IF input signal amplitude. A maximum source current of 60 μA is available and can be used to drive a meter and to detect a carrier presence. This is referred to as a Received Strength Signal Indicator (RSSI). The output at Pin 13 provides a current source. Thus, a resistor to ground yields a voltage proportional to the input carrier signal level. The value of this resistor is estimated by (V_{CC}(Vdc) – 1.0 V)/60 μA; so for V_{CC} = 4.0 Vdc, the resistor is approximately 50 kΩ and provides a maximum voltage swing of about 3.0 V.

A simple inverting op amp has an output at Pin 11 and the inverting input at Pin 10. The noninverting input is connected to 2.5 V. The op amp may be used as a noise triggered squelch or as an active noise filter. The bandpass filter is designed with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal is checked for a tone signal or for the presence of noise above the normal audio band. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that the audio mute (Pin 14) is open or connected to ground. If Pin 12 is pulled down to 0.9 V or below by the noise or tone detector, Pin 14 is internally shorted to ground. There is about 57 mV of hyteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to the appropriate point in the audio path between Pin 9 and an audio amplifier. The voltage at Pin 14 should not be lower than –0.7 V; this can be assured by connecting Pin 14 to the point that has no dc component.

Another possible application of the squelch switch may be as a carrier level triggered squelch circuit, similar to the MC3362/MC3363 FM receivers. In this case the meter output can be used directly to trigger the squelch switch when the RF input at the input frequency falls below the desired level. The level at which this occurs is determined by the resistor placed between the meter drive output (Pin 13) and ground (Pin 15).

Figure 11. Typical Application for MC3371 at 10.7 MHz

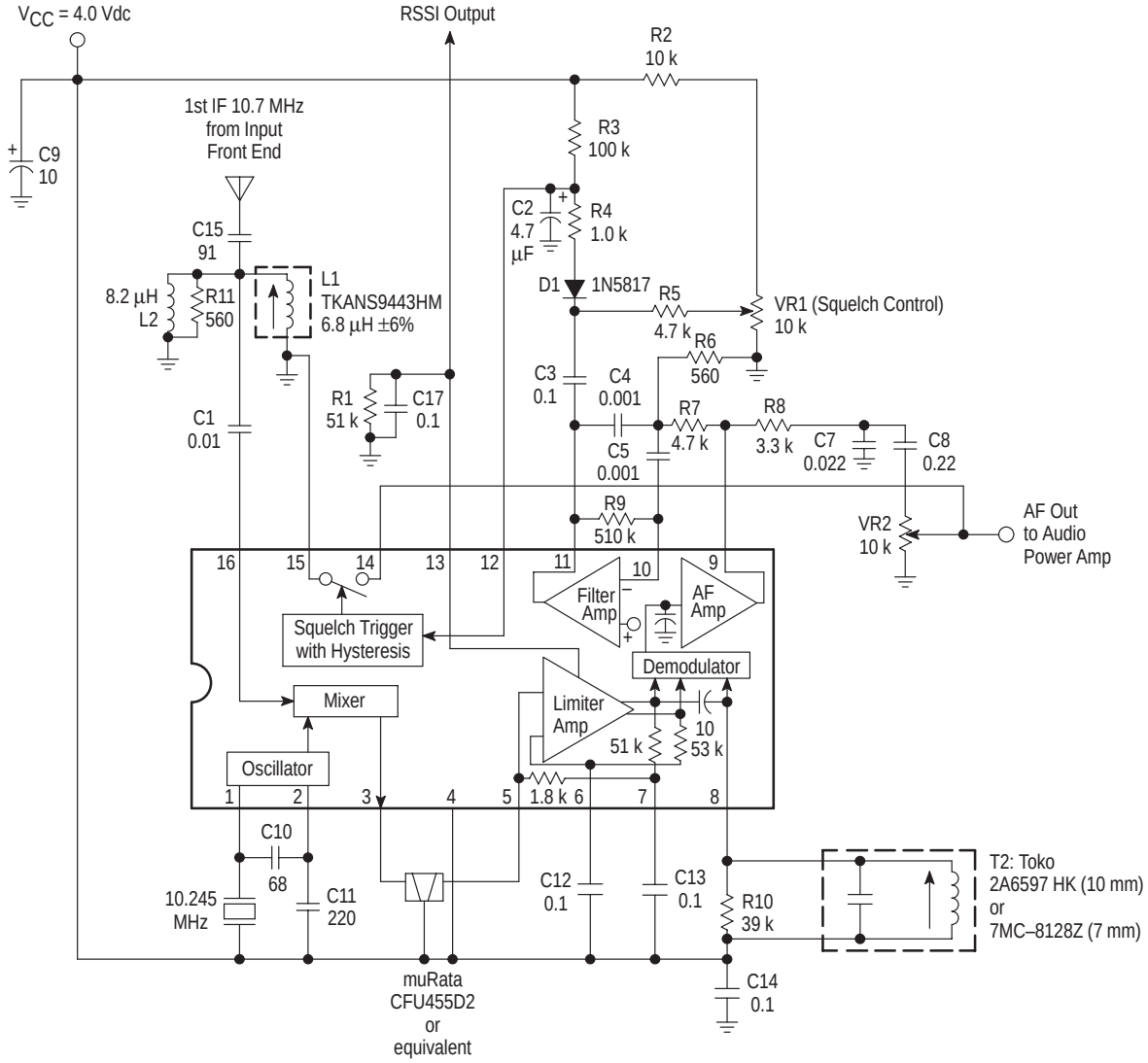


Figure 12. Typical Application for MC3372 at 10.7 MHz

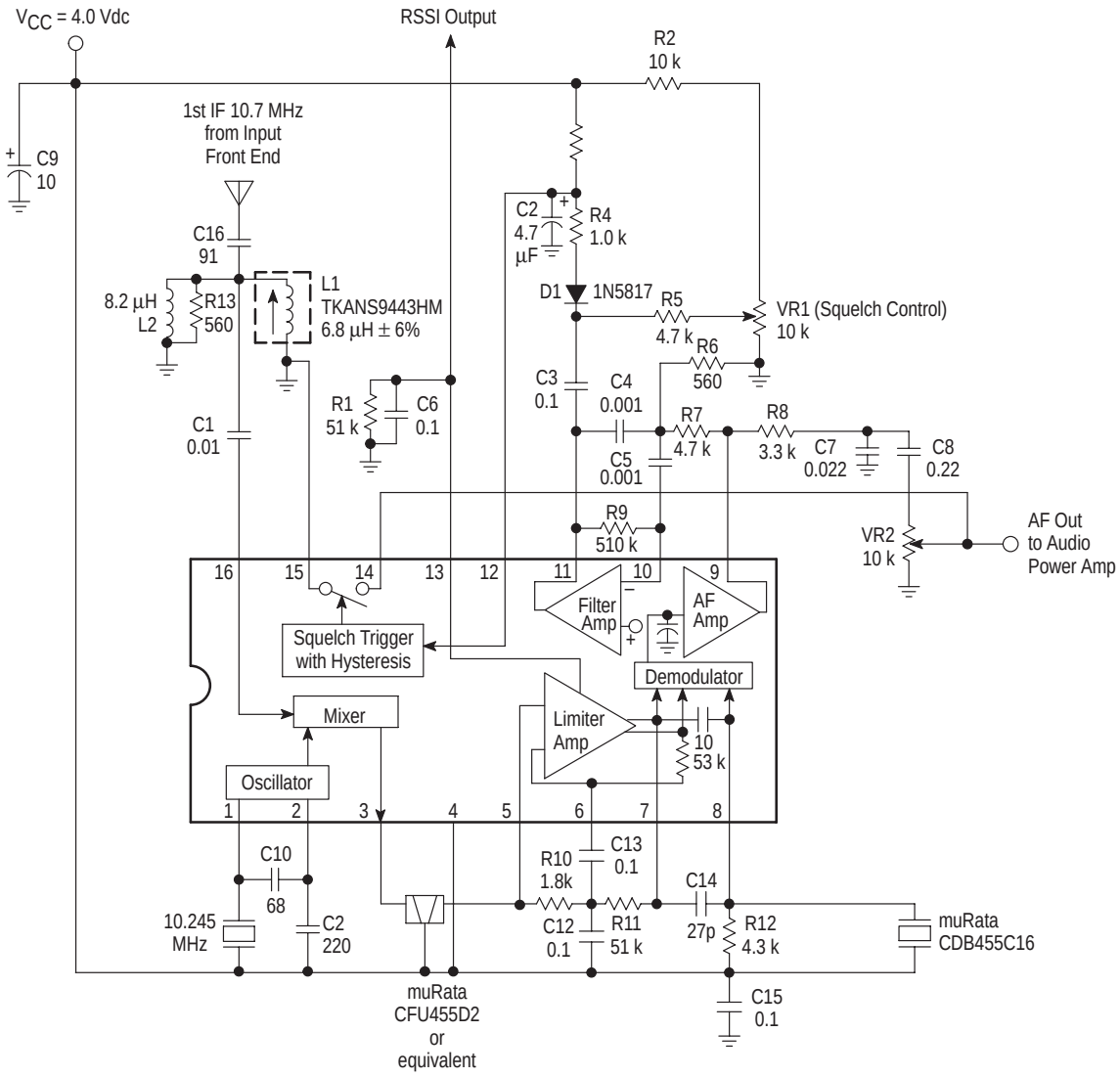


Figure 13. Typical Application for MC3372 at 45 MHz

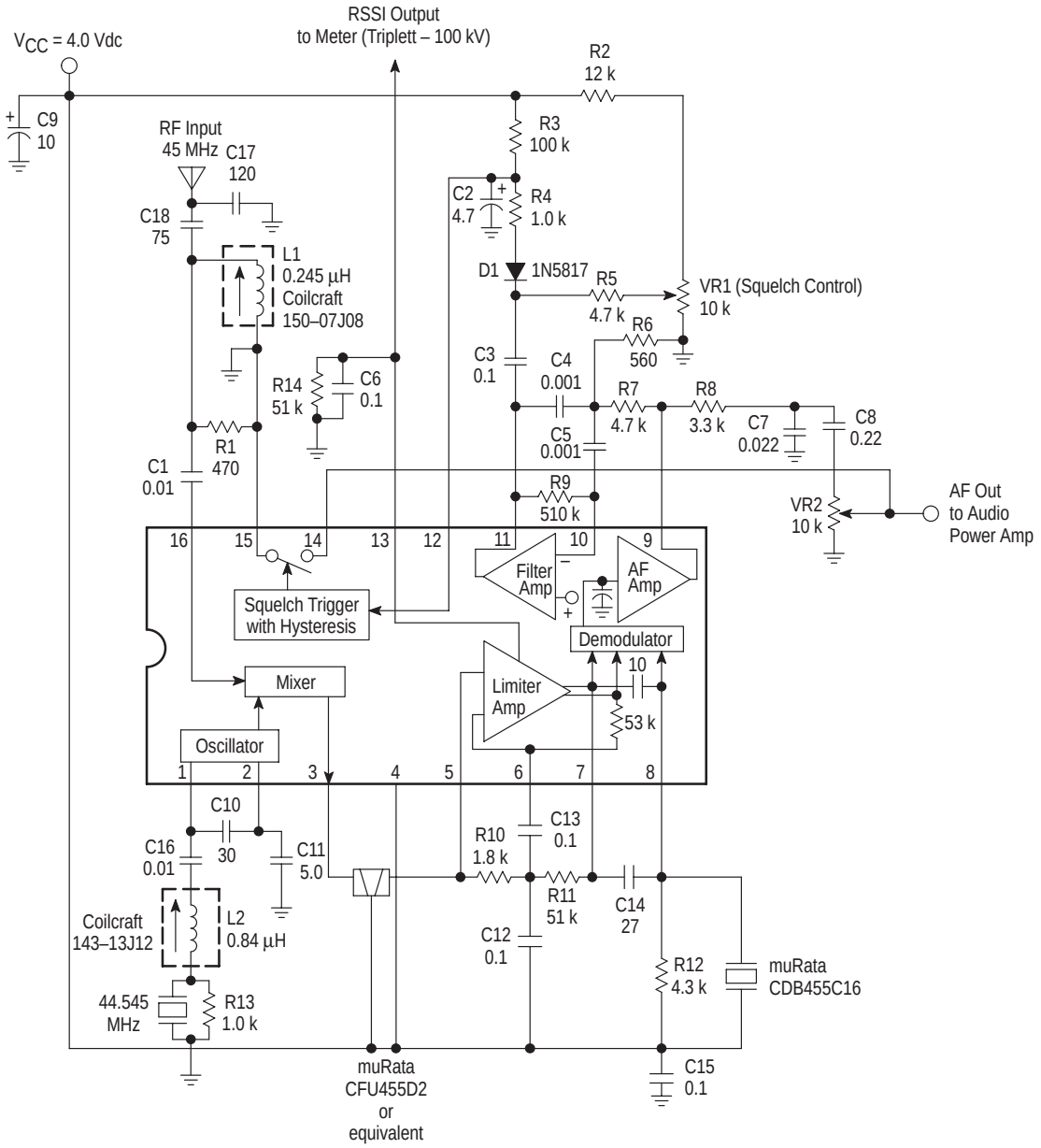


Figure 14. RSSI Output versus RF Input

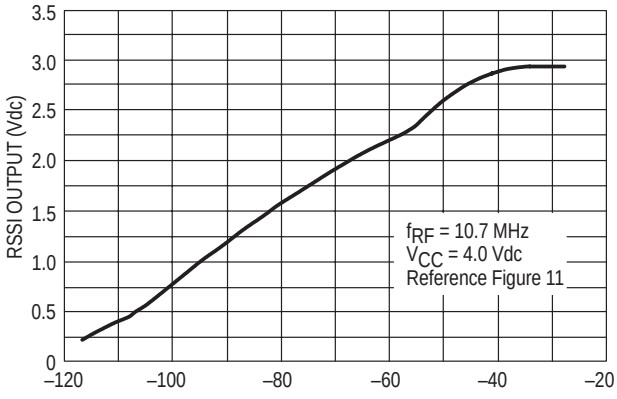


Figure 15. RSSI Output versus RF Input

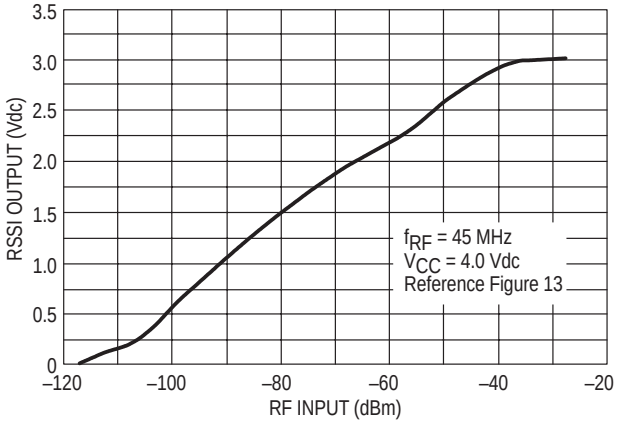
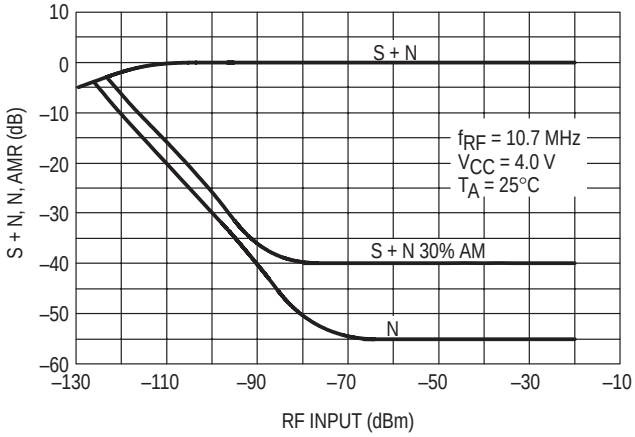


Figure 16. S + N, N, AMR versus Input



* Reference Figures 11, 12 and 13

Figure 17. Mixer Input Impedance versus Frequency

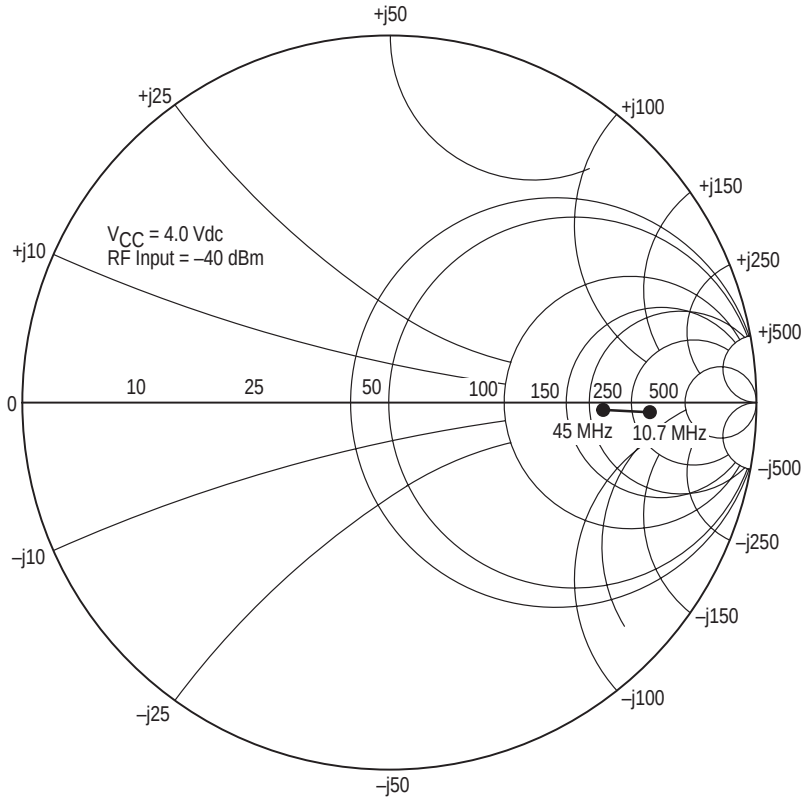


Figure 18. MC3371 PC Board Component View with Matched Input at 10.7 MHz

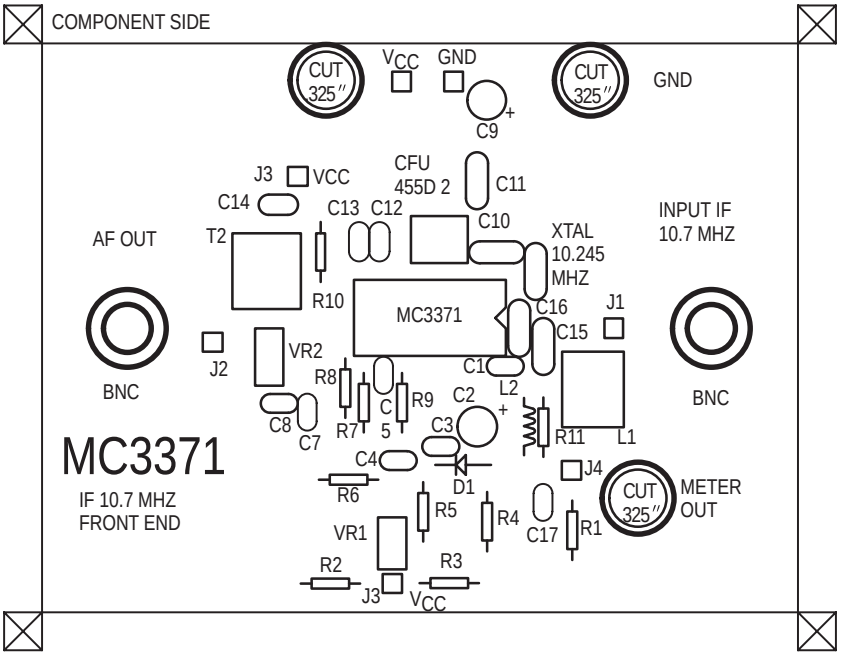
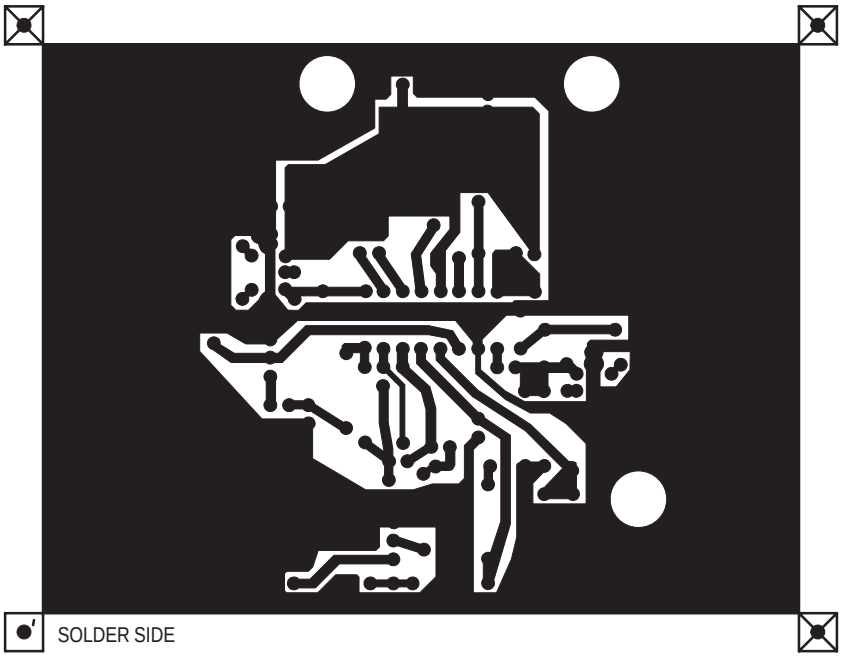


Figure 19. MC3371 PC Board Circuit or Solder Side as Viewed through Component Side



Above PC Board is laid out for the circuit in Figure 11.

Figure 20. MC3372P PC Board Component View with Matched Input at 10.7 MHz

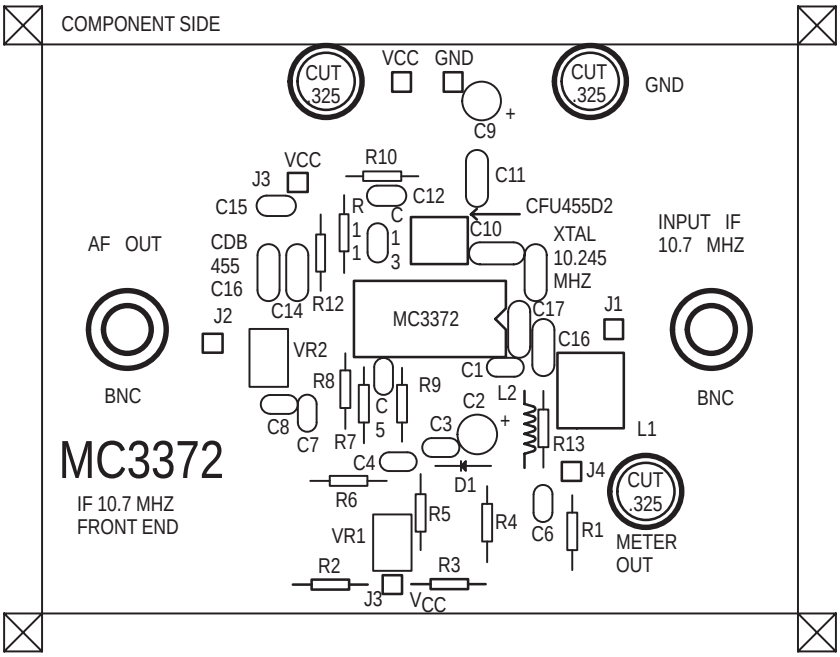
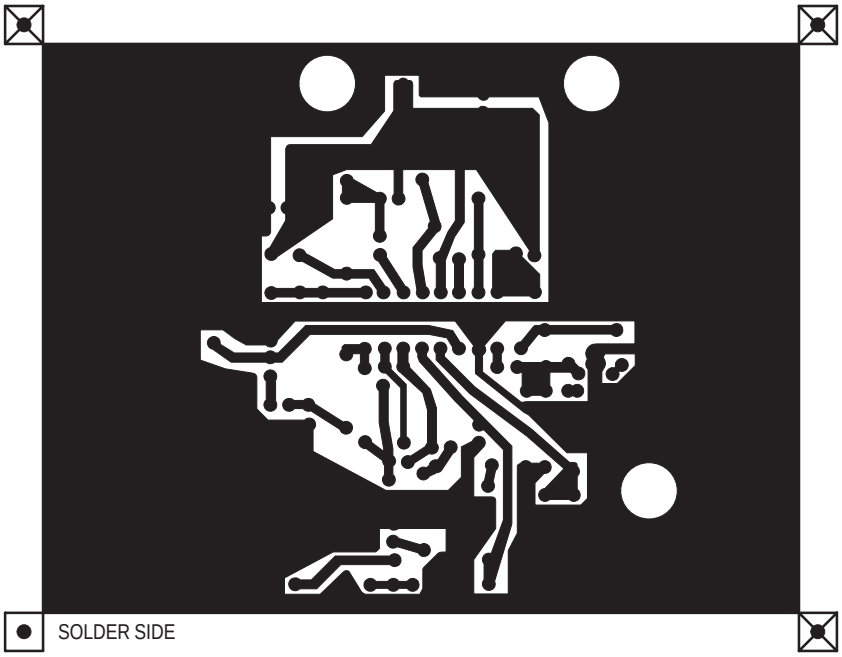


Figure 21. MC3372P PC Board Circuit or Solder Side as Viewed through Component Side



Above PC Board is laid out for the circuit in Figure 12.

MOTOROLA

Low Voltage FM Narrowband Receiver

. . . with single conversion circuitry including oscillator, mixer, IF amplifiers, limiting IF circuitry, and quadrature discriminator. The MC3374 is perfect for narrowband audio and data applications up to 75 MHz which require extremely low power consumption. Battery powered applications down to V_{CC} = 1.1 V are possible. The MC3374 also includes an on–board voltage regulator, low battery detection circuitry, a receiver enable allowing a power down Sleep–Mode™, two undedicated buffer amplifiers to allow simultaneous audio and data reception, and a comparator for enhancing FSK (Frequency Shift Keyed) data reception to 1200 baud.

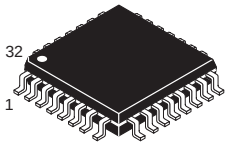
- Low Supply Voltage: V_{CC} = 1.1 to 3.0 Vdc
- Low Power Consumption: P_D = 1.5 to 5.0 mW
- Input Bandwidth 75 MHz
- Excellent Sensitivity: 0.5 μVrms for 12 dB SINAD
- Voltage Regulator Available (Source Capability 3.0 mA)
- Receiver Enable to Allow Active/Standby Operation
- Low Battery Detection Circuitry
- Self Biasing Audio Buffer
- Data Buffer
- FSK Data Shaping Comparator
- Standard 32–Lead QFP Surface Mount Package

Sleep–Mode is a trademark of Motorola, Inc.

MC3374

LOW VOLTAGE SINGLE CONVERSION FM RECEIVER

SEMICONDUCTOR TECHNICAL DATA

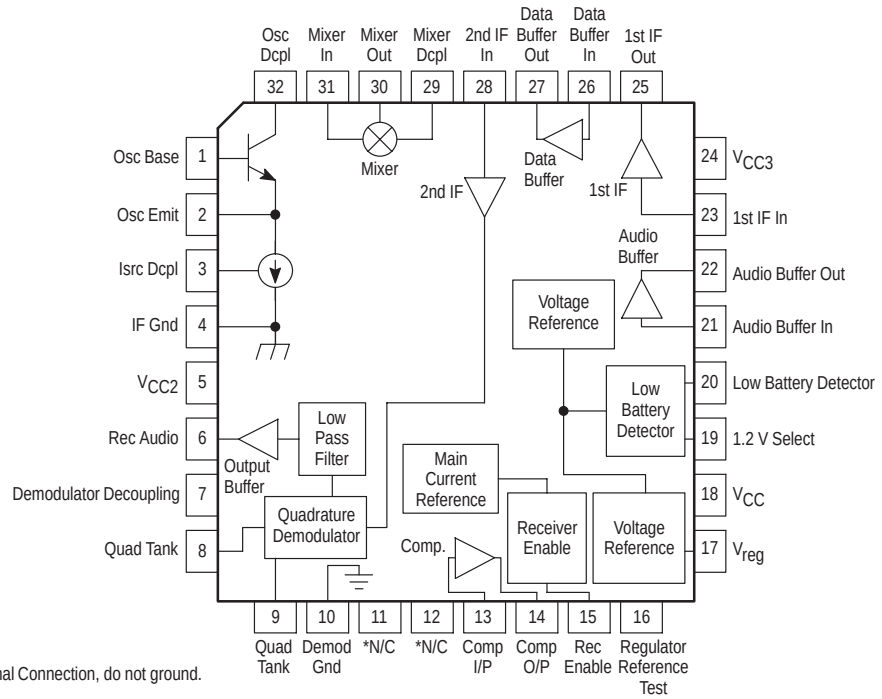


FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(Thin QFP)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC3374FTB	T_A = –10° to +70°C	TQFP–32

Simplified Block Diagram



*Internal Connection, do not ground.

This device contains 87 active transistors

MAXIMUM RATINGS (Voltage with respect to Pins 4 and 10; T_A = 25°C.)

Rating	Pin	Value	Unit
Supply Voltage	18	5.0	Vdc
RF Input Signal	31	1.0	Vrms
Audio Buffer Input	21	1.0	Vrms
Data Buffer Input	26	1.0	Vrms
Comparator Input	13	1.0	Vrms
Junction Temperature	–	150	°C
Storage Temperature	–	–65 to +150	°C

Device should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin	Value	Unit
Supply Voltage	18	1.1 to 3.0	Vdc
Receiver Enable Voltage	15	V_{CC}	Vdc
1.2 V Select Voltage	19	Open or V_{CC}	Vdc
RF Input Signal Level	31	0.001 to 100	mVrms
RF Input Frequency	31	0 to 75	MHz
Intermediate Frequency (IF)	–	455	kHz
Audio Buffer Input	21	0 to 75	mVrms
Data Buffer Input	26	0 to 75	mVrms
Comparator Input	13	10 to 300	mVrms
Ambient Temperature	–	–10 to 70	°C

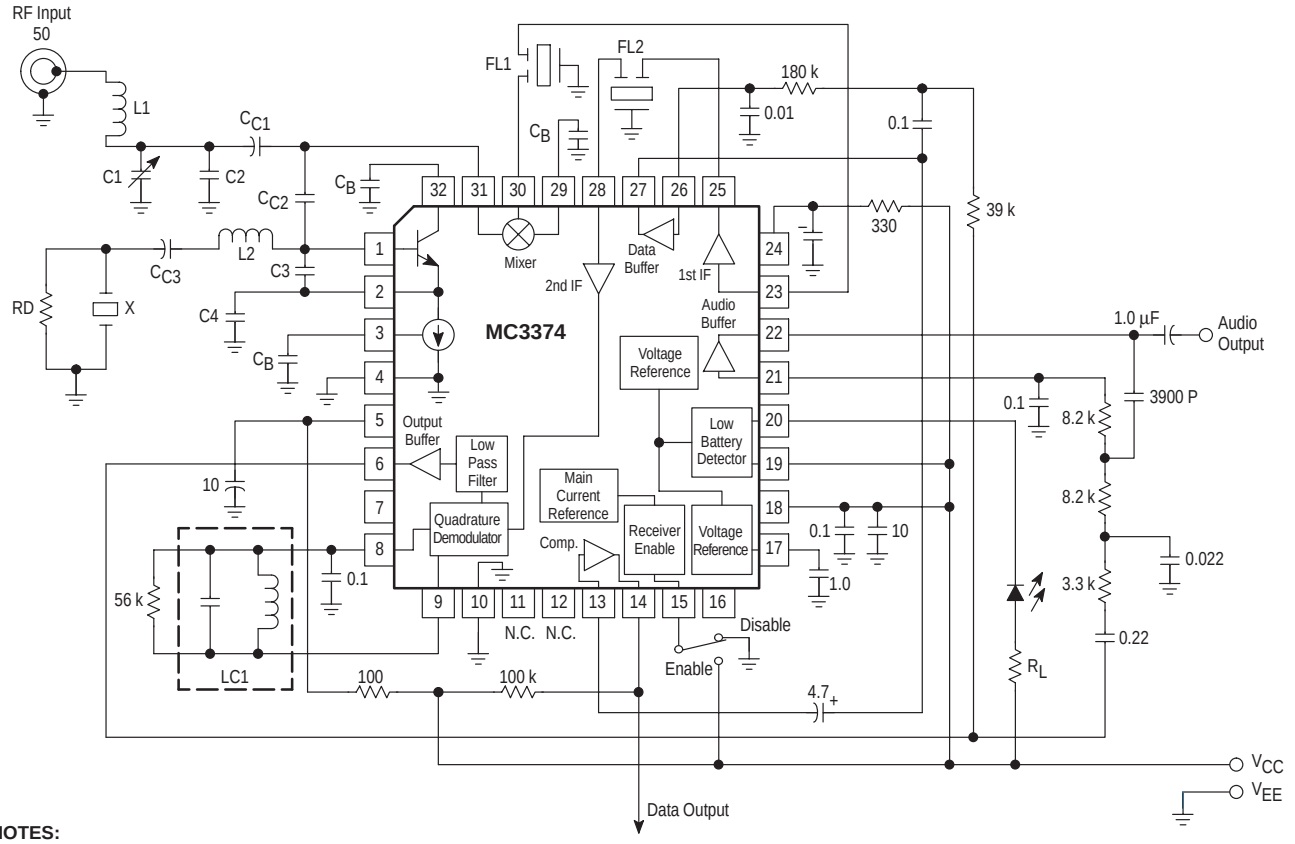
ELECTRICAL CHARACTERISTICS (V_{CC} = 1.3 V, f_o = 10.7 MHz, f_{mod} = 1.0 kHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 1, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
OVERALL MC3374 PERFORMANCE					
Drain Current – Pin 15 = V_{CC} (Enabled) – Pin 15 = 0 Vdc (Disabled)	5 + 18 + 24 5 + 18 + 24	– –	1.6 0.5	3.0 –	mA μA
Recovered Audio (RF Input = 10 μV)	6	13	18	30	mVrms
Noise Output (RF Input = 0 mV, 300 Hz–5.0 kHz)	6	–	1.0	–	mVrms
Input for –3.0 dB Limiting	31	–	0.6	–	μVrms
MIXER					
Mixer Input Resistance (Rp)	31	–	1.5	–	kΩ
Mixer Input Capacitance (Cp)	31	–	9.0	–	pF
FIRST IF AMPLIFIER					
First IF Amp Voltage Gain	–	–	27	–	dB
AUDIO BUFFER					
Voltage Gain	–	3.0	4.0	4.7	V/V
Input Resistance	21	–	110	–	kΩ
Maximum Input for Undistorted Output (<5% THD)	21	–	64	–	mVrms
Maximum Output Swing (<5% THD)	22	–	690	–	mV_{pp}
Output Resistance	22	–	780	–	Ω
DATA BUFFER					
Voltage Gain	–	1.4	2.7	4.3	V/V
Input Resistance	26	–	9.8	–	MΩ
Maximum Input for Undistorted Output (<5% THD)	26	–	100	–	mVrms
Maximum Output Swing (<5% THD)	27	–	800	–	mV_{pp}
Output Resistance	27	–	690	–	Ω

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 1.3 V, f_o = 10.7 MHz, f_{mod} = 1.0 kHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 1, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
COMPARATOR					
Minimum Input for Triggering (R_L = 100 kΩ)	13	–	7.0	–	mVrms
Maximum Input Frequency (R_L = 100 kΩ)	13	–	25	–	kHz
Rise Time (10–90%; R_L = 100 kΩ)	14	–	5.0	–	µs
Fall Time (90–10%; R_L = 100 kΩ)	14	–	0.4	–	µs
LOW BATTERY DETECTOR					
Low Battery Trip Point	19	–	1.2	–	Vdc
Low Battery Output – V_{CC} = 0.9 V – V_{CC} = 1.3 V	20 20	– –	0.2 V_{CC}	– –	Vdc
VOLTAGE REGULATOR					
Regulated Output (see Figure 4)	17	0.95	1.07	1.15	Vdc
Source Capability	17	–	–	3.0	mA

Figure 1. MC3374 Pager IF Application Circuit



NOTES:

1. FL1 and FL2 are 455 kHz ceramic bandpass filters, which should have input and output impedances of 1.5 kΩ to 2.0 kΩ. Suggested part numbers are MuRata CFU455X or CFW455x – the 'X' suffix denotes bandwidth.
2. LC1 is a 455 kHz LC resonator. Recommended part numbers are Toko America RMC2A6597HM or 5SVLC–0637BGT (smaller). The evaluation board layout shown provides for use of either resonator. Ceramic discriminator elements cannot be used with the MC3374 due to their low input impedance. The damping resistor value can be raised to increase the recovered audio or lowered to increase the quadrature detector's bandwidth and linearity – practical limits are approximately 27 kΩ to 75 kΩ. Typically the quadrature detector's bandwidth should match the low IF filter's bandwidth.
3. The data buffer is set up as a low–pass filter with a corner frequency of approximately 200 Hz. The audio buffer is a bandpass filter with corner frequencies of 300 Hz and 3.0 kHz. The audio amplifier provides bass suppression.
4. C_{C1} and C_{C3} are RF coupling capacitors and should have ≤ 20 Ω impedance at the desired input and oscillator frequencies.
5. C_{C2} provides "light coupling" of the oscillator signal into the mixer, and should have a 3.0 kΩ to 5.0 kΩ impedance at the desired local oscillator frequency.
6. Capacitors labelled C_B are bypass capacitors and should have 20 Ω impedance at the desired RF and local oscillator frequencies.
7. The network of L1, C1 and C2 provides impedance matching of the mixer input (nominally 3.0 kΩ shunted by 9.0 pF) to 50 Ω at the desired RF/IF input frequency. This will allow for bench testing of the receiver from typical RF signal generators or radio service monitors, but additional or different matching will be required to maximize receiver sensitivity when used in conjunction with an antenna, RF preamplifier or mixer.

In. Freq.	L1	L2	C1	C2	C3	C4	C_{C1}/C_{C3}	C_{C2}	C_B	RD
10.7 MHz	6.8 µH	Short	2–82 pF	10 pF	120 pF	50 pF	1.0 nF	5.0 pF	0.1 µF	Open
45 MHz	0.68 µH	1.2 µH	5–25 pF	Open	30 pF	5.0 pF	1.0 nF	1.0 pF	1.0 nF	1.0 k
72 MHz	0.22 µH	0.22 µH	5–25 pF	Open	18 pF	3.0 pF	470 pF	1.0 pF	470 pF	1.0 k

Figure 2. Recovered Audio versus Supply

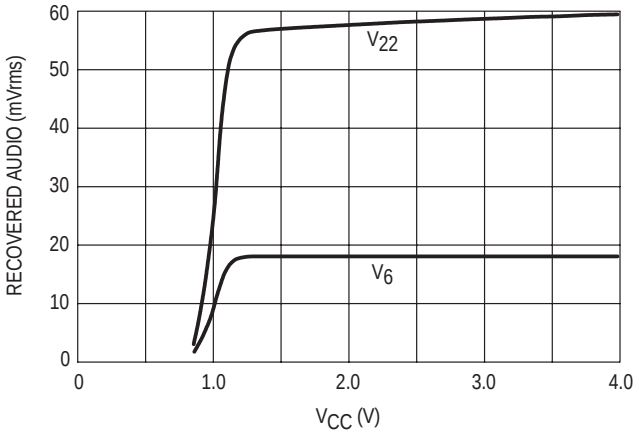


Figure 3. S+N, N versus Input

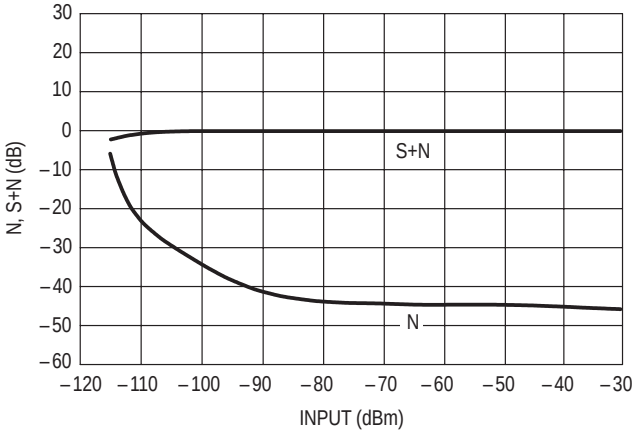


Figure 4. V_{REG} versus Supply

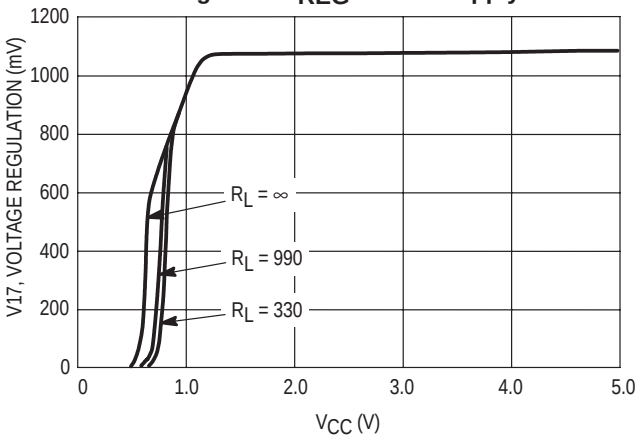


Figure 5. Regulated Output and Recovered Audio versus Temperature

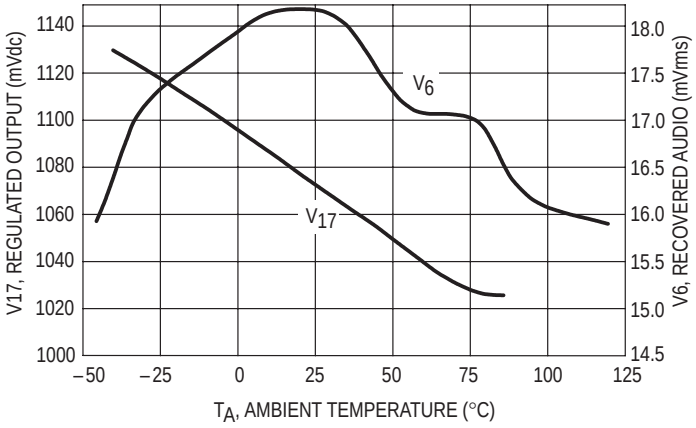


Figure 6. Buffer Amplifier Gains versus Temperature

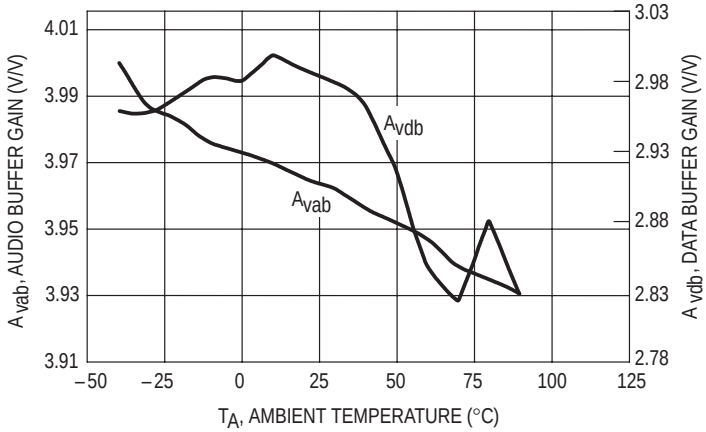
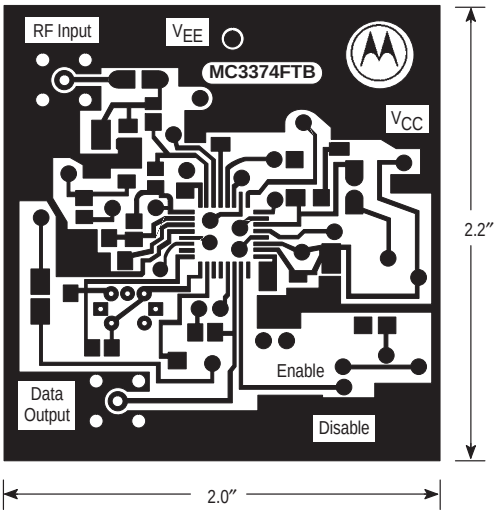
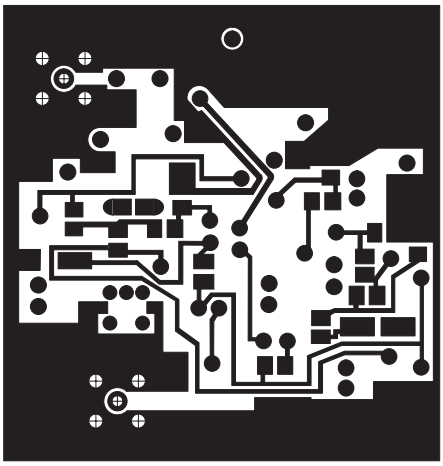


Figure 7. MC3374 Pager Receiver PCB Artwork

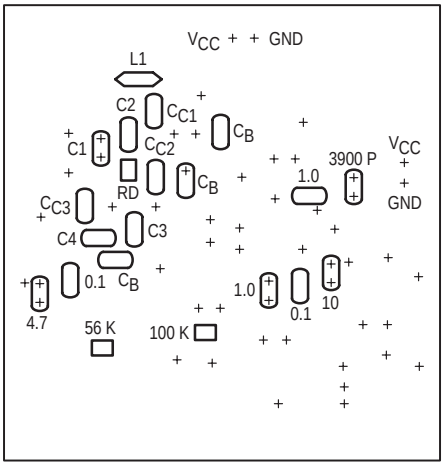
COPPER 1 LAYER
(Actual View of Surface Mount Side)



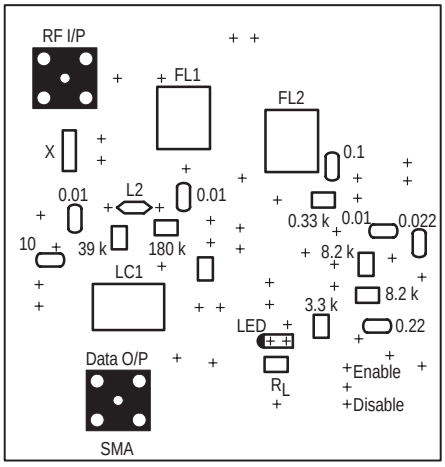
COPPER 2 LAYER
(Caution: Reversed View of Through–Hole Side)



COMPONENT 1 LAYER



COMPONENT 2 LAYER



NOTE: + = Through Hole

CIRCUIT DESCRIPTION

The MC3374 is an FM narrowband receiver capable of operation to 75 MHz. The low voltage design yields low power drain and excellent sensitivity in narrowband voice and data link applications. In the typical application the mixer amplifies the incoming RF or IF signal and converts this frequency to 455 kHz. The signal is then filtered by a 455 kHz ceramic filter and applied to the first intermediate frequency (IF) amplifier input, before passing through a second ceramic filter. The modulated IF signal is then applied to the limiting IF amplifier and detector circuitry. Modulation is recovered by a conventional quadrature detector. The typical modulation bandwidth available is 3.0 to 5.0 kHz.

Features available include buffers for audio/data amplification and active filtering, on board voltage regulator, low battery detection circuitry with programmable level, and receiver disable circuitry. The MC3374 is an FM utility receiver to be used for voice and/or narrowband data reception. It is especially suitable where extremely low power consumption and high design flexibility are required.

APPLICATION

The MC3374 can be used as a high performance FM IF for the use in low power dual conversion receivers. Because of the MC3374's extremely good sensitivity (0.6 μV for 20 dB (S+N/N, see Figure 3)), it can also be used as a stand alone single conversion narrowband receiver to 75 MHz for applications not sensitive to image frequency interference. An RF preamplifier will likely be needed to overcome preselector losses.

The oscillator is a Colpitts type which must be run under crystal control. For fundamental mode crystals choose resonators, parallel resonant, for a 32 pF load. For higher frequencies, use a 3rd overtone series mode type. The coil L2 and RD resistor are needed to ensure proper operation.

The best adjacent channel and sensitivity response occur when two 455 kHz ceramic filters are used, as shown in Figure 1. Either can be replaced by a 0.1 μF coupling capacitor to reduce cost, but some degradation in sensitivity and/or stability is suspected.

The detector is a quadrature type, with the connection from the limiter output to the detector input provided internally. A 455 kHz LC tank circuit must be provided externally. One of the tank pins (Pin 8) must be decoupled using a 0.1 μF capacitor. The 56 kΩ damping resistor (see Figure 1), determines the peak separation of the detector (and thus its bandwidth). Smaller values will increase the separation and bandwidth but decrease recovered audio and sensitivity.

The data buffer is a noninverting amplifier with a nominal voltage gain of 2.7 V/V. This buffer needs its dc bias (approximately 250 mV) provided externally or else debiasing will occur. A 2nd order Sallen–Key low pass filter, as shown in Figure 1, connecting the recovered audio output to the data buffer input provides the necessary dc bias and some post detection filtering. The buffer can also be used as an active filter.

The audio buffer is a noninverting amplifier with a nominal voltage gain of 4.0 V/V. This buffer is self–biasing so its input should be ac coupled. The two buffers, when applied as active filters, can be used together to allow simultaneous audio and very low speed data reception. Another possible configuration is to receive audio only and include a noise–triggered squelch.

The comparator is a noninverting type with an open collector output. Typically, the pull–up resistor used between Pin 14 and V_{CC} is 100 kΩ. With R_L = 100 kΩ the comparator is capable of operation up to 25 kHz. The circuit is self–biasing, so its input should be ac coupled.

The regulator is a 1.07 V reference capable of sourcing 3.0 mA. This pin (Pin 17) needs to be decoupled using a 1.0–10 μF capacitor to maintain stability of the MC3374.

All three V_{CC}s on the MC3374 (V_{CC}, V_{CC2}, V_{CC3}) run on the same supply voltage. V_{CC} is typically decoupled using capacitors only. V_{CC2} and V_{CC3} should be bypassed using the RC bypasses shown in Figure 1. Eliminating the resistors on the V_{CC2} and V_{CC3} bypasses may be possible in some applications, but a reduction in sensitivity and quieting will likely occur.

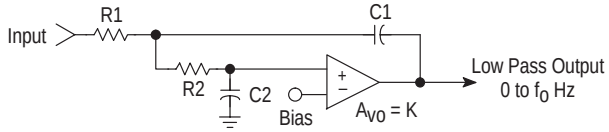
The low battery detection circuit gives an NPN open collector output at Pin 20 which drops low when the MC3374 supply voltage drops below 1.2 V. Typically it would be pulled up via a 100 kΩ resistor to supply.

The 1.2 V Select pin, when connected to the MC3374 supply, programs the low battery detector to trip at V_{CC} < 1.1 V. Leaving this pin open raises the trip voltage on the low battery detector.

Pin 15 is a receiver enable which is connected to V_{CC} for normal operation. Connecting this pin to ground shuts off receiver and reduces current drain to I_{CC} < 0.5 μA.

APPENDIX

Design of 2nd Order Sallen–Key Low Pass Filters



The audio and data buffers can easily be configured as active low pass filters using the circuit configuration shown above. The circuit has a center frequency (f_0) and quality factor (Q) given by the following:

$$f_0 = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

$$Q = \frac{1}{\sqrt{\frac{R2C2}{R1C1}} + \sqrt{\frac{R1C2}{R2C1}} + (1-K)\sqrt{\frac{R1C1}{R2C2}}}$$

If possible, let R1 = R2 or C1 = C2 to simplify the above equations. Be sure to avoid a negative Q value to prevent instability. Setting $Q = 1/\sqrt{2} = 0.707$ yields a maximally flat filter response.

Data Buffer Design

The data buffer is designed as follows:

f_O = 200 Hz
C1 = C2 = 0.01 μF
Q = 0.707 (target)

K = 2.7 (data buffer open loop voltage gain)

Setting C1 = C2 yields:

$$fo = \frac{1}{2\pi C1\sqrt{R1R2}}$$

$$Q = \frac{1}{\sqrt{\frac{R2}{R1}} + (2-K)\sqrt{\frac{R1}{R2}}}$$

Iteration yields R2 = 4.2 (R1) to make Q = 0.707.
Substitution into the equation for f_O yields:
R1 = 38 kΩ (use 39 kΩ)
R2 = 4.2(R1) = 180 kΩ
C1 = C2 = 0.01 μF

Audio Buffer Design

The audio buffer is designed as follows:

f_O = 3000 Hz
R1 = R2 = 8.2 kΩ
Q = 0.707 (target)

K = 3.9 (audio buffer open loop voltage gain)

Setting C1 = C2 yields:

$$fo = \frac{1}{2\pi R1\sqrt{C1C2}}$$

$$Q = \frac{1}{\sqrt{\frac{C2}{C1}} + (1-K)\sqrt{\frac{C1}{C2}}}$$

Iteration yields C2 = 2.65 (C1) to make Q = 0.707.
Substitution into the equation for f_O yields:
C1 = 3900 pF
C2 = 2.65(C1) = 0.01 μF
R1 = R2 = 8.2 kΩ

MOTOROLA

MC13055

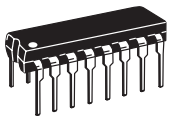
Wideband FSK Receiver

The MC13055 is intended fo RF data link systems using carrier frequencies up to 40 MHz and FSK (frequency shift keying) data rates up to 2.0 M Baud (1.0 MHz). This design is similar to the MC3356, except that it does not include the oscillator/mixer. The IF bandwidth has been increased and the detector output has been revised to a balanced configuration. The received signal strength metering circuit has been retained, as has the versatile data slicer/comparator.

- Input Sensitivity 20 μV @ 40 MHz
- Signal Strength Indicator Linear Over 3 Decades
- Available in Surface Mount Package
- Easy Application, Few Peripheral Components

WIDEBAND FSK RECEIVER

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

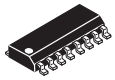
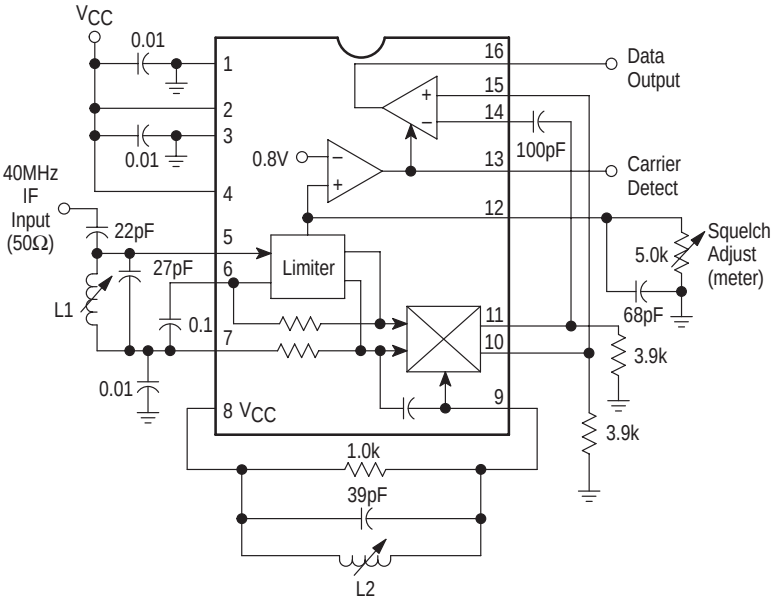
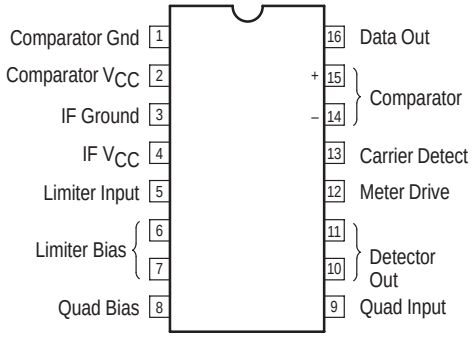


Figure 1. Block Diagram and Application Circuit



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13055D	T_A = – 40 to +85°C	SO–16
MC13055P		Plastic DIP

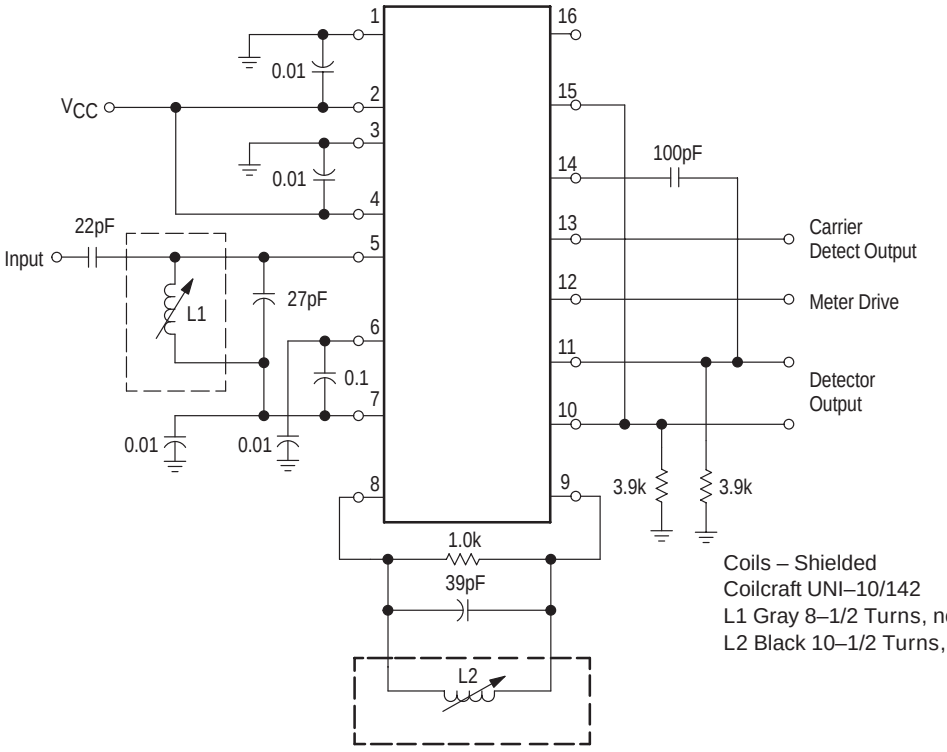
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Supply Voltage Range	V2, V4	3.0 to 12	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 40 MHz, f_{mod} = 1.0 MHz, Δf = ±1.0 MHz, T_A = 25°C, test circuit of Figure 2.)

Characteristic		Conditions	Min	Typ	Max	Unit
Total Drain Current		12 + 14	–	20	25	mA
Data Comparator Pull–Down Current		I16	–	10	–	mA
Meter Drive Slope versus Input		I12	4.5	7.0	9.0	µA/dB
Carrier Detect Pull–Down Current		I13	–	1.3	–	mA
Carrier Detect Pull–Up Current		I13	–	500	–	µA
Carrier Detect Threshold Voltage		V12	690	800	1010	mV
DC Output Current		I10, I11	–	430	–	µA
Recovered Signal		V10 – V11	–	350	–	mVrms
Sensitivity for 20 dB S + N/N, BW = 5.0 MHz		VIN	–	20	–	µVrms
S + N/N at V_{in} = 50 µV		V10 – V11	–	30	–	dB
Input Impedance @ 40 MHz	R_{in} C_{in}	Pin 5, Ground	– –	4.2 4.5	– –	kΩ pF
Quadrature Coil Loading	R_{in} C_{in}	Pin 9 to 8	– –	7.6 5.2	– –	kΩ pF

Figure 2. Test Circuit



Coils – Shielded
Coilcraft UNI–10/142
L1 Gray 8–1/2 Turns, nominal 300 nH
L2 Black 10–1/2 Turns, nominal 380 nH

Figure 3. Overall Gain, Noise, AM Rejection

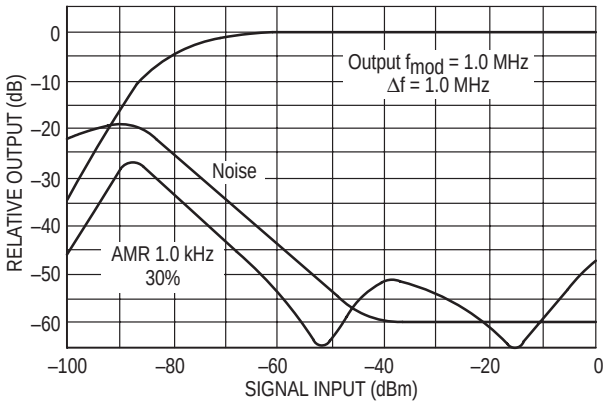


Figure 4. Meter Current versus Signal

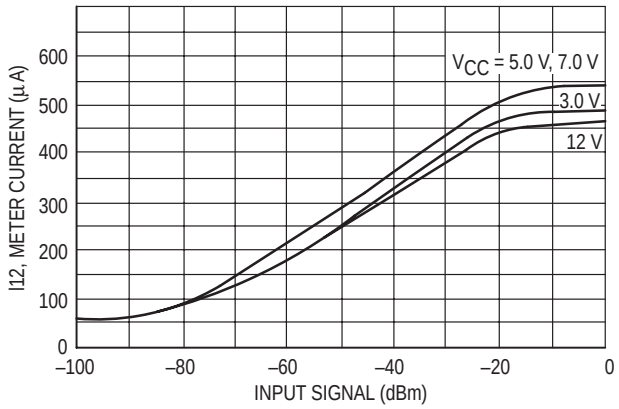


Figure 5. Untuned Input: Limiting Sensitivity versus Frequency

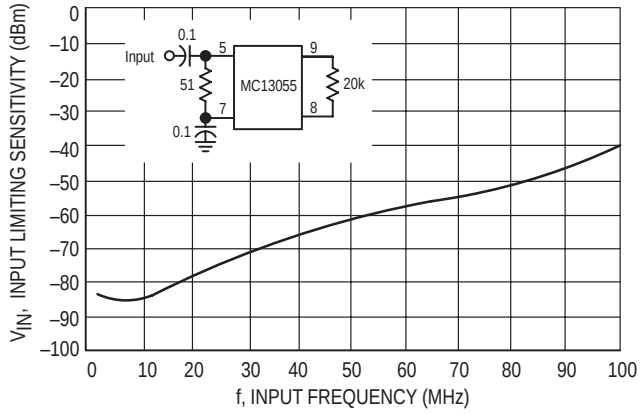


Figure 6. Untuned Input: Meter Current versus Frequency

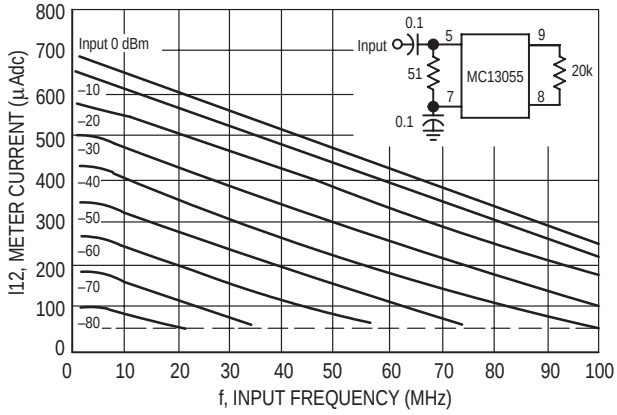


Figure 7. Limiting Sensitivity and Detuning versus Supply Voltage

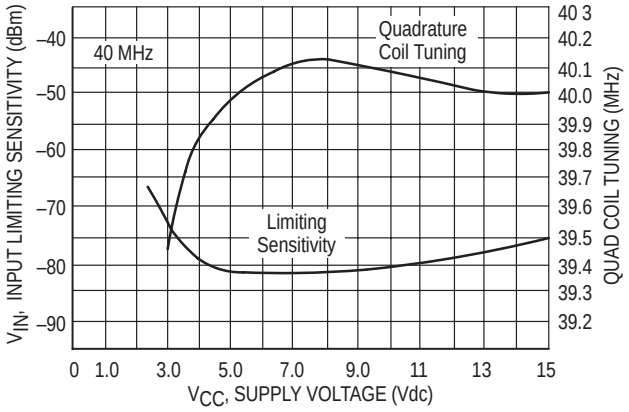


Figure 8. Detector Current and Power Supply Current versus Supply Voltage

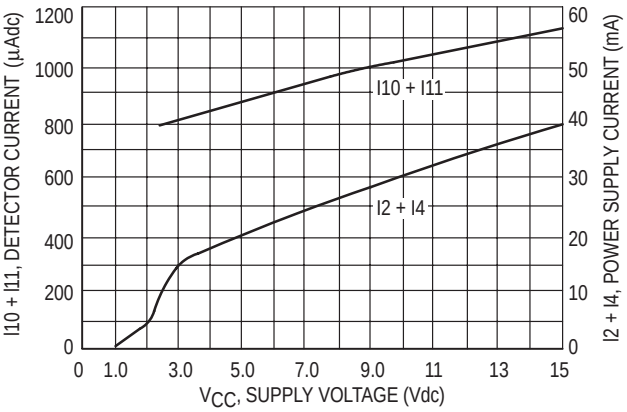


Figure 9. Recovered Audio versus Temperature

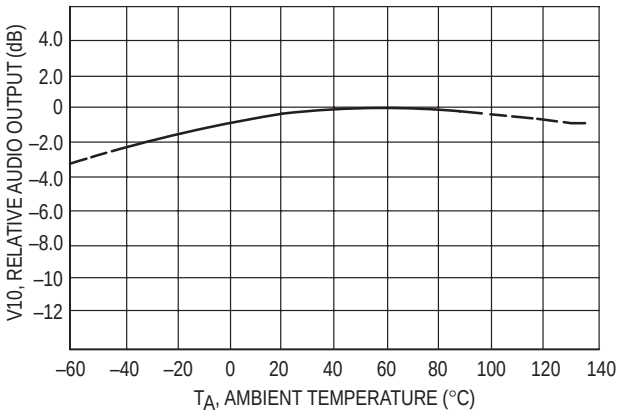


Figure 10. Carrier Detect Threshold versus Temperature

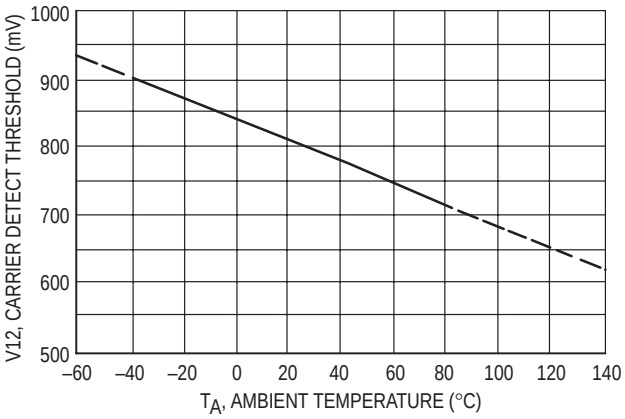


Figure 11. Meter Current versus Temperature

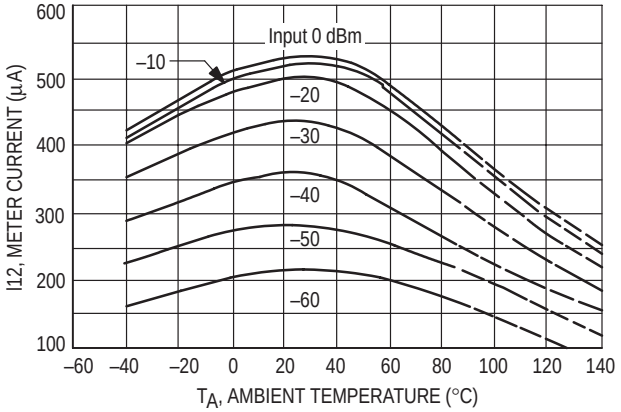


Figure 12. Input Limiting versus Temperature

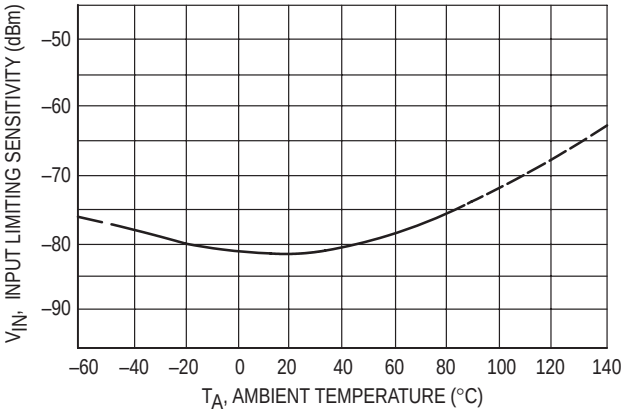


Figure 13. Input Impedance, Pin 5

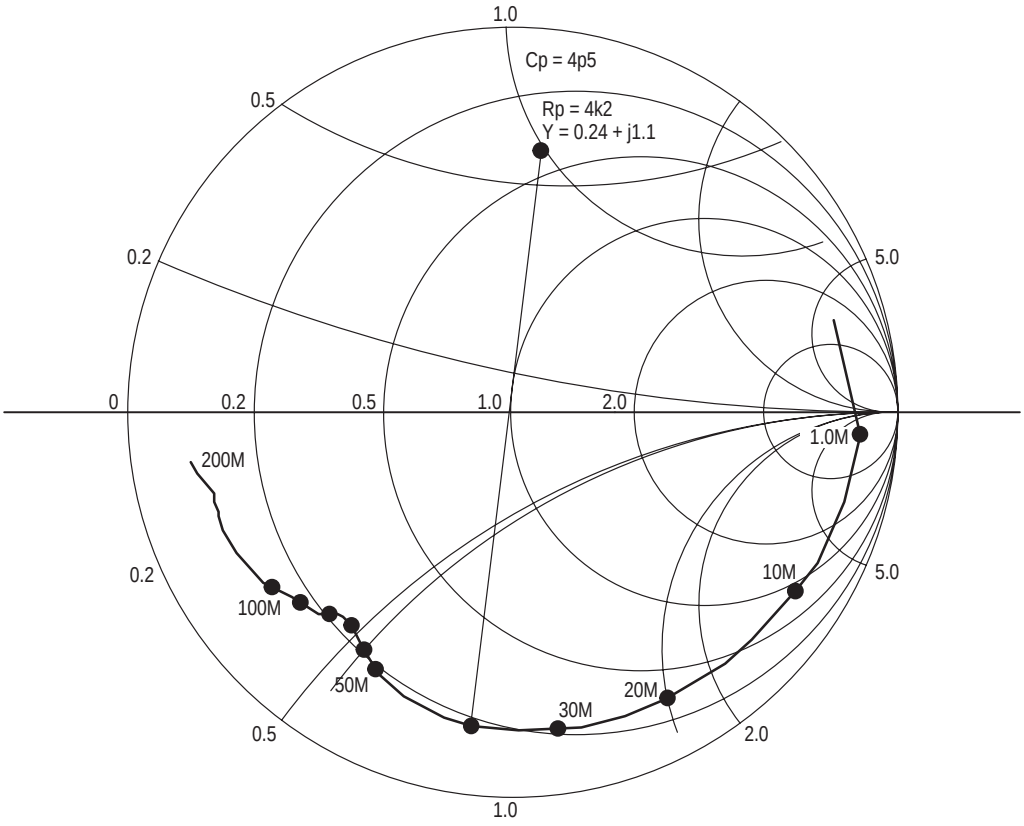
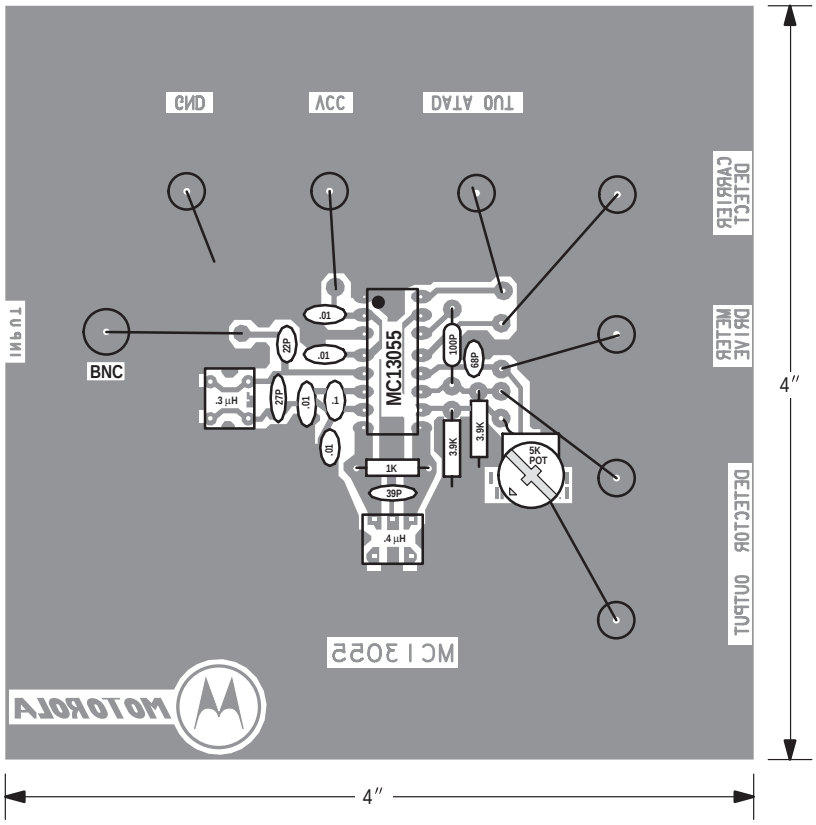
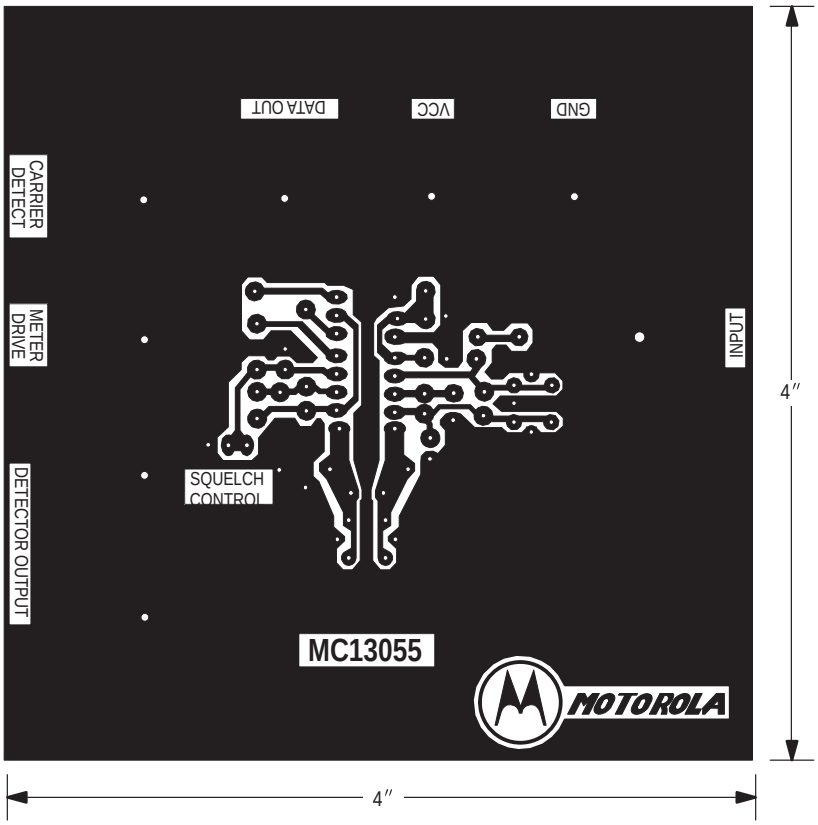


Figure 14. Test Fixture
(Component Layout)



(Circuit Side View)



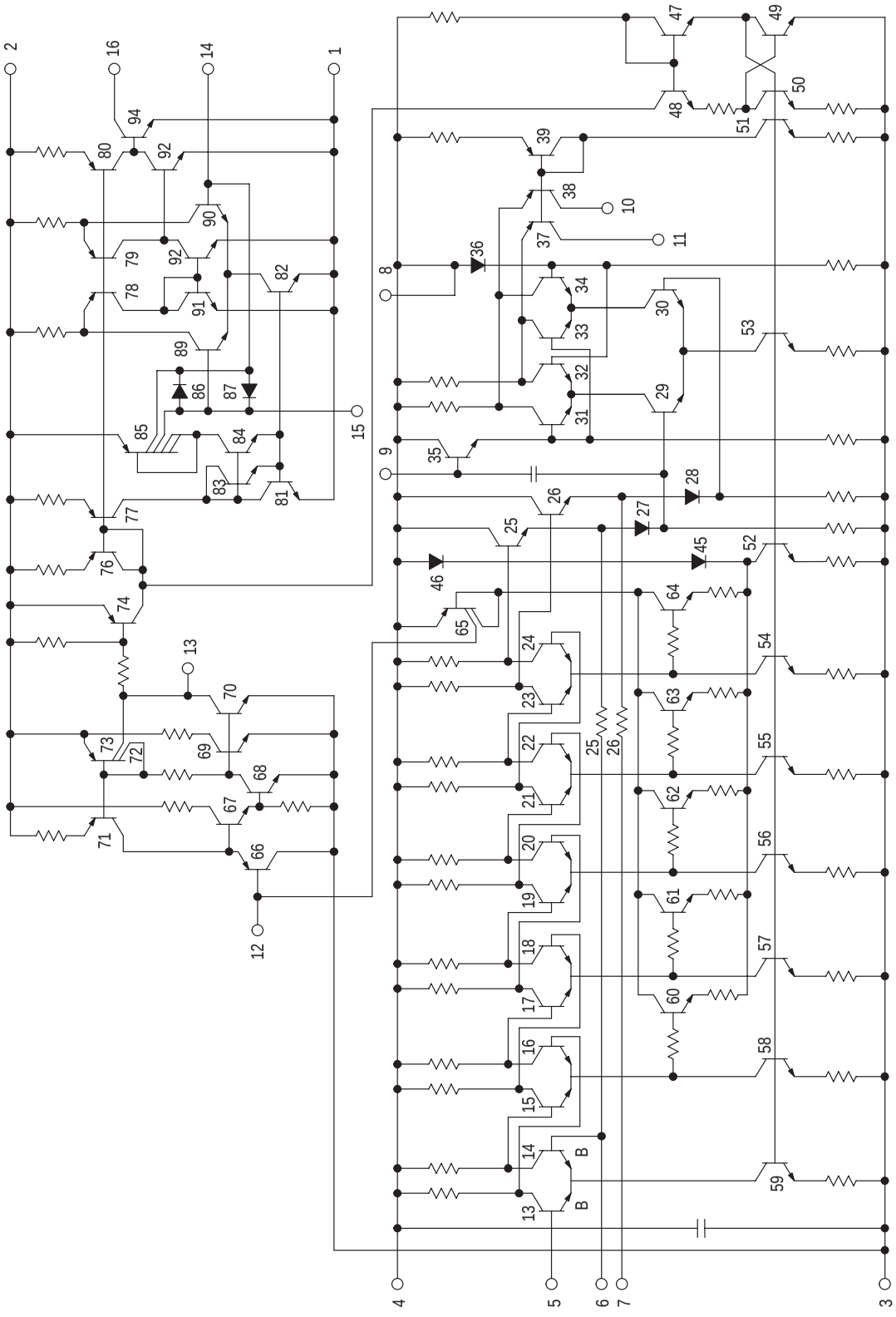


Figure 15. Internal Schematic

GENERAL DESCRIPTION

The MC13055 is an extended frequency range FM IF, quadrature detector, signal strength detector and data shaper. It is intended primarily for FSK data systems. The design is very similar to MC3356 except that the oscillator/mixer has been removed, and the frequency capability of the IF has been raised about 2:1. The detector output configuration has been changed to a balanced, open–collector type to permit symmetrical drive of the data shaper (comparator). Meter drive and squelch features have been retained.

The limiting IF is a high frequency type, capable of being operated up to 100 MHz. It is expected to be used at 40 MHz in most cases. The quadrature detector is internally coupled to the IF, and a 2.0 pF quadrature capacitor is internally provided. The 20 dB quieting sensitivity is approximately 20 μV, tuned input, and the IF can accept signals up to 220 mVrms without distortion or change of detector quiescent DC level.

The IF is unusual in that each of the last 5 stages of the 6 stage limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 20 μV to 20 mVrms (see Figure 4).

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator (+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 20 μVrms. A resistor (R) from Pin 13 to Pin 12 will provide V_{CC}/R of feedback current. This current can be correlated to an amount of signal strength hysteresis by using Figure 4.

The squelch is internally connected to the data shaper. Squelch causes the data shaper to produce a high (V_{CC}) output.

The data shaper is a complete “floating” comparator, with diodes across its inputs. The outputs of the quadrature detector can be fed directly to either or preferably both inputs of the comparator to produce a squared output swinging from V_{CC} to ground in inverted or noninverted form.

MOTOROLA

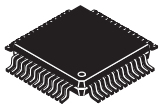
Universal Cordless Telephone Subsystem IC

MC13109A

UNIVERSAL CT–0 SUBSYSTEM INTEGRATED CIRCUIT

The MC13109A integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna Input to Audio Output 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expandor Includes Mute, Digital Volume Control and Speaker Driver
  - Compressor Includes Mute, ALC and Limiter
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign CT–0 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Output Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Externally Adjustable Trip Point
- 2.0 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices



FB SUFFIX
PLASTIC PACKAGE
CASE 848B
(QFP–52)

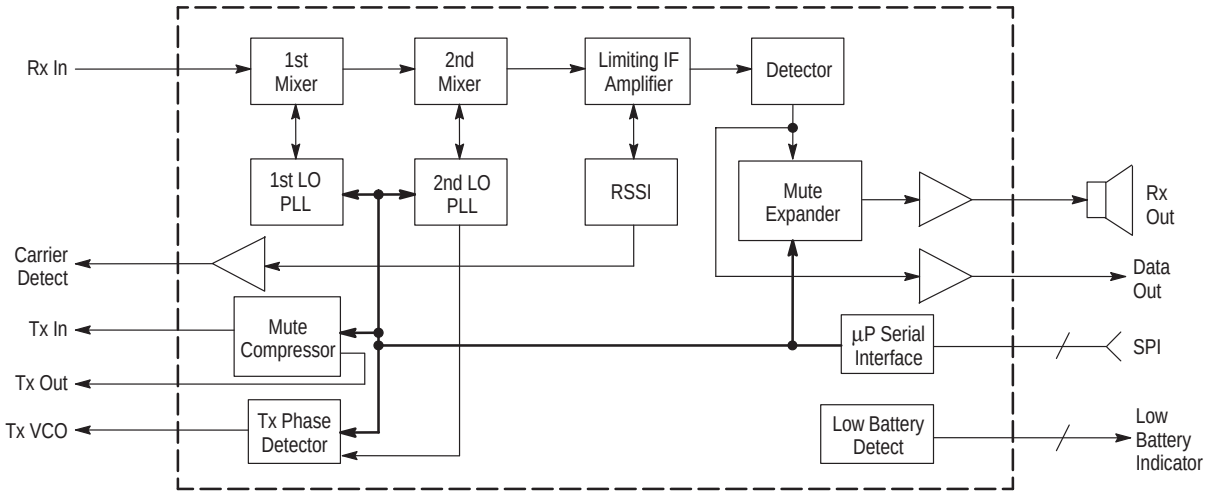


FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(LQFP–48)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC13109AFB	T_A = –20 to 85°C	QFP–52
MC13109AFTA		LQFP–48

Simplified Block Diagram



This device contains 6,609 active transistors.

Figure 1. MC13109AFB Test Circuit

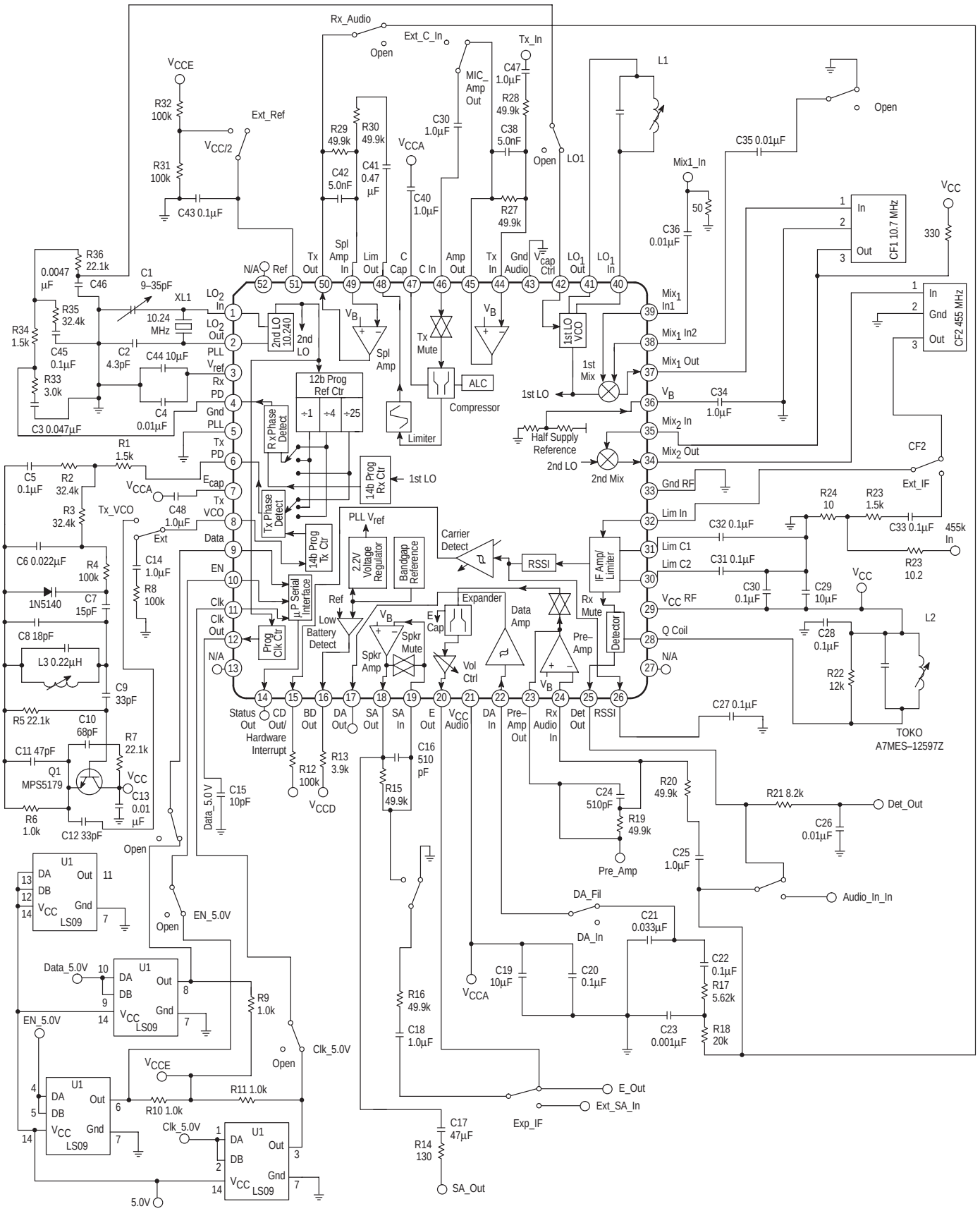
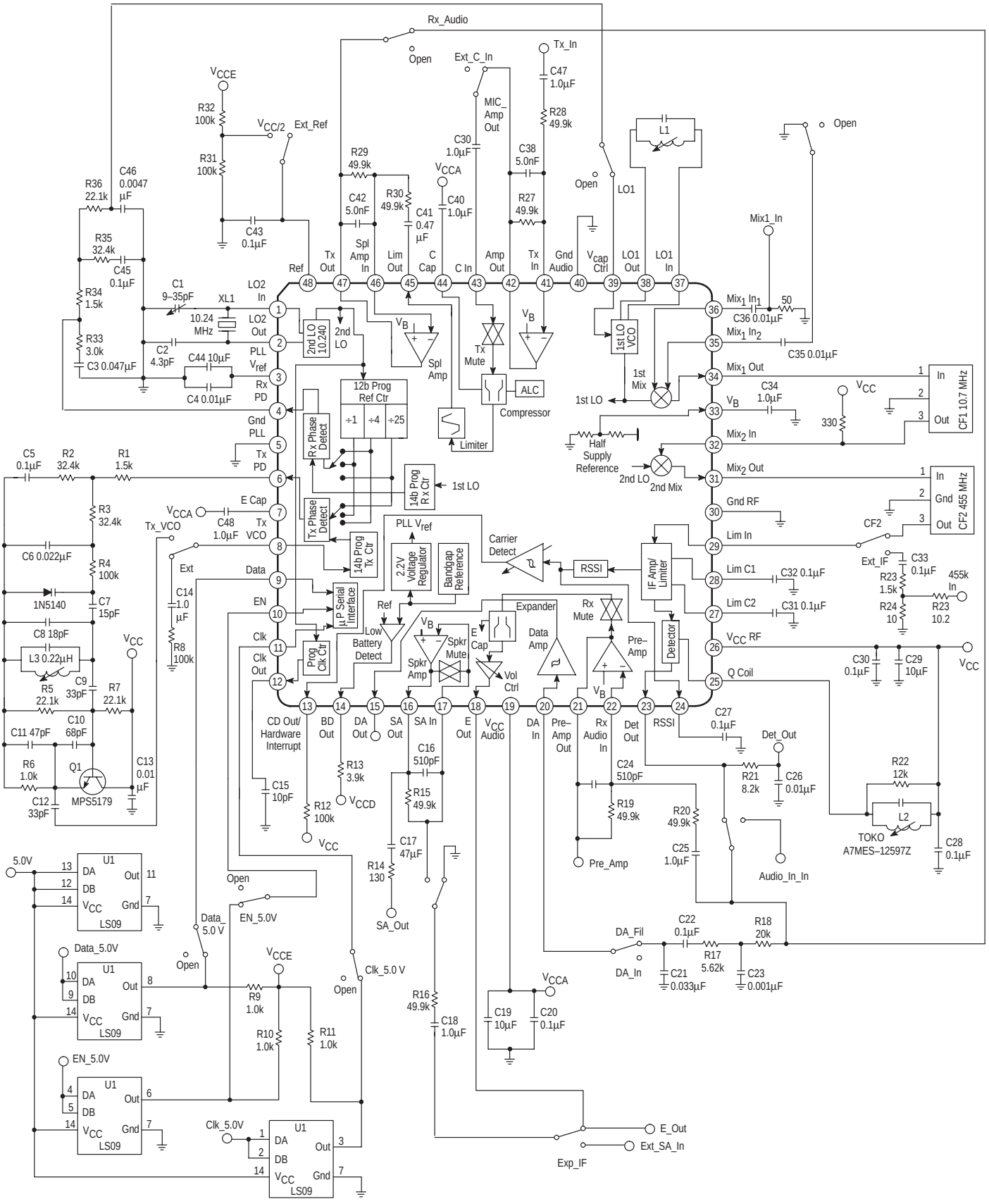


Figure 2. MC13109AFTA Test Circuit



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +5.5	Vdc
Junction Temperature	T_J	–65 to +150	°C

NOTES: 1. Devices should not be operated at or outside these limits. The "Recommended Operating Conditions" table provides for actual device operation.
2. ESD data available upon request.
3. Meets Human Body Model (HBM) ≤2000V and Machine Model (MM) ≤200V.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Min	Typ	Max	Unit
V_{CC}	2.0	–	5.5	Vdc
Operating Ambient Temperature	–20	–	85	°C

NOTE: All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.6 V, T_A = 25°C, RF In = 46.61 MHz, f_{DEV} = ±3.0 kHz, f_{mod} = 1.0 kHz; Test Circuit Figure 1.)

Characteristic	Min	Typ	Max	Unit
POWER SUPPLY				
Static Current				
Active Mode (V_{CC} = 2.6 V)	–	6.1	12	mA
Active Mode (V_{CC} = 3.6 V)	–	6.5	–	mA
Receive Mode (V_{CC} = 2.6 V)	–	3.9	7.0	mA
Receive Mode (V_{CC} = 3.6 V)	–	4.3	–	mA
Standby Mode (V_{CC} = 2.6 V)	–	320	600	µA
Standby Mode (V_{CC} = 3.6 V)	–	550	–	µA
Inactive Mode (V_{CC} = 2.6 V)	–	40	80	µA
Inactive Mode (V_{CC} = 3.6 V)	–	54	–	µA

ELECTRICAL CHARACTERISTICS (continued)

FM Receiver

The FM receivers can be used with either a quad coil or a ceramic resonator. The FM receiver and 1st LO have been designed to work for all country channels, including 25 channel U.S., without the need for any external switching circuitry (see Figure 25.)

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_O = 46.61 MHz, f_{DEV} = ±3.0 kHz, f_{mod} = 1.0 kHz.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Sensitivity (Input for 12 dB SINAD)	Matched Impedance Differential Input	Mix_1 $In_{1/2}$	Det Out	V_{SIN}	–	0.7	–	µVrms
1st Mixer Voltage Conversion Gain	V_{in} = 1.0 mVrms, with CF_1 as Load	Mix_1 $In_{1/2}$	Mix_1 Out	MX_{gain1}	–	10	–	dB
2nd Mixer Voltage Conversion Gain	V_{in} = 3.0 mVrms, with CF_2 as Load	Mix_2 In	Mix_2 Out	MX_{gain2}	–	20	–	dB
1st Mixer Input Impedance	–	–	Mix_1 In_1 Mix_1 In_2	R_{P1} C_{P1}	–	0.88 2.5	–	kΩ pF
2nd Mixer Input Impedance	–	–	Mix_2 In	R_{P2} C_{P2}	–	3.0 2.7	–	kΩ pF
1st Mixer Output Impedance	–	–	Mix_1 Out	R_{P1} Out C_{P1} Out	–	390 1.8	–	Ω pF
2nd Mixer Output Impedance	–	–	Mix_2 Out	R_{P2} Out C_{P2} Out	–	1.5 12	–	kΩ pF
1st and 2nd Mixer Voltage Gain Total	V_{in} = 1.0 mVrms, with CF_1 and CF_2 as Load	Mix_1 $In_{1/2}$	Mix_2 Out	$MX_{gain}T$	24	27	–	dB
IF –3.0 dB Limiting Sensitivity	f_{in} = 455 kHz	Lim In	Det Out	IF Sens	–	55	100	µVrms
Total Harmonic Distortion (CCITT Filter)	With R_C = 8.2 kΩ/ 0.01 µF Filter at Det Out	Mix_1 $In_{1/2}$	Det Out	THD	–	1.0	3.0	%
Recovered Audio	With R_C = 8.2 kΩ/ 0.01 µF Filter at Det Out	Mix_1 $In_{1/2}$	Det Out	AFO	80	100	154	mVrms
Demodulator Bandwidth	–	Lim In	Det Out	BW	–	20	–	kHz
Signal to Noise Ratio	V_{in} = 10 mVrms, R_C = 8.2 kΩ/0.01 µF	Mix_1 $In_{1/2}$	Det Out	SN	–	50	–	dB
AM Rejection Ratio	30% AM, V_{in} = 10 mVrms, R_C = 8.2 kΩ/0.001 µF	Mix_1 $In_{1/2}$	Det Out	AMR	30	40	–	dB
First Mixer 3rd Order Intercept (Input Referred)	Matched Impedance Input	Mix_1 $In_{1/2}$	Mix_1 Out	TOI_{mix1}	–	–10	–	dBm
Second Mixer 3rd Order Intercept (Input Referred)	Matched Impedance Input	Mix_2 In	Mix_2 Out	TOI_{mix2}	–	–27	–	dBm
Detector Output Impedance	–	–	Det Out	Z_O	–	870	–	Ω

ELECTRICAL CHARACTERISTICS (continued)

RSSI/Carrier Detect

Connect 0.01 μF to Gnd from "RSSI" output pin to form the carrier detect filter. "CD Out" is an open collector output which requires an external 100 kΩ pull–up resistor to V_{CC}. The carrier detect threshold is programmable through the MPU interface.

(R_L = 100 kΩ, V_{CC} = 2.6 V, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
RSSI Output Current Dynamic Range	–	Mix_1 In	RSSI	RSSI	–	65	–	dB
Carrier Sense Threshold	CD Threshold Adjust = (10100)	Mix_1 In	CD Out	V_T	–	11	–	mVrms
Hysteresis	–	Mix1 In	CD Out	Hys	–	1.5	–	dB
Output High Voltage	V_{in} = 0 μVrms, R_L = 100 kΩ, CD = (10100)	Mix_1 In	CD Out	V_{OH}	–	2.6	–	V
Output Low Voltage	V_{in} = 100 μVrms, R_L = 100 kΩ, CD = (10100)	Mix_1 In	CD Out	V_{OL}	–	0.01	0.4	V
Carrier Sense Threshold Adjustment Range	Programmable through MPU Interface	–	–	V_{Trange}	–20	–	11	dB
Carrier Sense Threshold – Number of Steps	Programmable through MPU Interface	–	–	V_{Tn}	–	32	–	–

Data Amp Comparator

Inverting hysteresis comparator. Open collector output with internal 100 kΩ pull–up resistor. A band pass filter is connected between the "Det Out" pin and the "DA In" pin with component values as shown in the attached block diagram. The "DA In" input signal is ac coupled.

(V_{CC} = 2.6 V, T_A = 25°C)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Hysteresis	–	DA In	DA Out	Hys	30	40	50	mV
Threshold Voltage	–	DA In	DA Out	V_T	V_{CC} – 0.9	V_{CC} – 0.7	V_{CC} – 0.5	V
Input Impedance	–	–	DA In	Z_I	–	12	–	kΩ
Output Impedance	–	–	DA Out	Z_O	–	104	–	kΩ
Output High Voltage	V_{in} = V_{CC} – 1.0 V, I_{OH} = 0 mA	DA In	DA Out	V_{OH}	V_{CC} – 0.1	2.6	–	V
Output Low Voltage	V_{in} = V_{CC} – 0.4 V, I_{OL} = 0 mA	DA In	DA Out	V_{OL}	–	0.04	0.4	V

ELECTRICAL CHARACTERISTICS (continued)

Pre–Amplifier/Expander/Rx Mute/Volume Control

The Pre–Amplifier is an inverting rail–to–rail output swing operational amplifier with the non–inverting input terminal connected to the internal V_B half supply reference. External resistors and capacitors can be connected to set the gain and frequency response. The expander analog ground is set to the half supply reference so the input and output swing capability will increase as the supply voltage increases. The volume control can be adjusted through the MPU interface. The “Rx Audio In” input signal is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, Set External Pre–Amplifier R’s for Gain of 1, Volume Control = (0111).)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Pre–Amp Open Loop Gain	–	Rx Audio In	Pre–Amp	A_{VOL}	–	60	–	dB
Pre–Amp Gain Bandwidth	–	Rx Audio In	Pre–Amp	GBW	–	100	–	kHz
Pre–Amp Maximum Output Swing	R_L = 10 kΩ	Rx Audio In	Pre–Amp	V_{Omax}	–	V_{CC} – 0.3	–	Vpp
Expander 0 dB Gain Level	V_{in} = –10 dBV	Rx Audio In	E Out	G	–3.0	–0.3	3.0	dB
Expander Gain Tracking	V_{in} = –20 dBV, Output Relative to G V_{in} = –30 dBV, Output Relative to G	Rx Audio In	E Out	G_t	–21 –42	–19.84 –40.12	–19 –37	dB
Total Harmonic Distortion	V_{in} = –10 dBV	Rx Audio In	E Out	THD	–	0.2	–	%
Maximum Output Voltage	Increase input voltage until output voltage THD = 5%, then measure output voltage. R_L = 10 kΩ	Rx Audio In	E Out	V_{Omax}	–	–5.0	–	dBV
Attack Time	E_{cap} = 1.0 μF, R_{filt} = 20 kΩ (See Appendix B)	Rx Audio In	E Out	t_a	–	3.0	–	ms
Release Time	E_{cap} = 1.0 μF, R_{filt} = 20 kΩ (See Appendix B)	Rx Audio In	E Out	t_r	–	13.5	–	ms
Compressor to Expander Crosstalk	V (Rx Audio In) = 0 Vrms, V_{in} = –10 dBV	C In	E Out	C_T	–	–76	–	dB
Rx Mute	V_{in} = –10 dBV No popping detectable during Rx Mute transitions	Rx Audio In	E Out	M_e	–	–65	–	dB
Volume Control Range	Programmable through MPU Interface	–	–	V_{Crange}	–14	–	16	dB
Volume Control Steps	Programmable through MPU Interface	–	–	V_{Cn}	–	16	–	–

ELECTRICAL CHARACTERISTICS (continued)

Speaker Amplifier/SP Mute

The Speaker Amplifier is an inverting rail–to–rail operational amplifier. The non–inverting input terminal is connected to the internal V_B half supply reference. External resistors and capacitors are used to set the gain and frequency response. The “SA In” input is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, External Resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Maximum Output Swing	V_{CC} = 2.3 V, R_L = 130 Ω V_{CC} = 2.3 V, R_L = 600 Ω V_{CC} = 3.4 V, R_L = 600 Ω	SA In	SA Out	V_{Omax}	– – –	0.8 2.0 3.0	– – –	V_{pp}
SP Mute	V_{in} = –20 dBV R_L = 130 Ω No popping detectable during SP Mute transitions	SA In	SA Out	M_{sp}	–	–67	–	dB

Mic Amplifier

The Mic Amplifier is an inverting rail–to–rail output operational amplifier with the non–inverting input terminal connected to the internal V_B half supply reference. External resistors and capacitors are connected to set the gain and frequency response. The “Tx In” input is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, External Resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Open Loop Gain	–	Tx In	Amp Out	A_{VOL}	–	60	–	dB
Gain Bandwidth	–	Tx In	Amp Out	G_{BW}	–	100	–	kHz
Maximum Output Swing	R_L = 10 kΩ	Tx In	Amp Out	V_{Omax}	–	V_{CC} – 0.3	–	Vpp

ELECTRICAL CHARACTERISTICS (continued)

Compressor/ALC/Tx Mute/Limiter

The compressor analog gound is set to the half supply reference so the input and output swing capability will increase as the supply voltage increases. The “C In” input is ac coupled. The ALC (Automatic Level Control) provides a soft limit to the output signal swing as the input voltage increases slowly (i.e., a sine wave is maintained). The Limiter circuit limits rapidly changing signal levels by clipping the signal peaks. The ALC and/or Limiter can be disabled through the MPU serial interface.

(Test Conditions: V_{CC} = 2.6 V, f_{in} = 1.0 kHz, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Compressor 0 dB Gain Level	V_{in} = –10 dBV, ALC disabled, Limiter disabled	C In	Lim Out	G	–3.0	–0.06	3.0	dB
Compressor Gain Tracking	V_{in} = –30 dBV, Output Relative to G V_{in} = –50 dBV, Output Relative to G	C In	Lim Out	G_t	–11 –23	–10.12 –20.16	–9.0 –17	dB
Maximum Compressor Gain	V_{in} –70 dBV	C In	Lim Out	A_{Vmax}	–	29	–	dB
Total Harmonic Distortion	V_{in} –10 dBV, ALC disabled, Limiter disabled	C In	Lim Out	THD	–	0.5	–	%
Input Impedance	–	C In	Lim Out	Z_{in}	–	16	–	kΩ
Attack Time	C_{cap} = 1.0 μF, R_{filt} = 20 kΩ (see Appendix B)	C In	Lim Out	t_a	–	3.0	–	ms
Release Time	C_{cap} = 1.0 μF, R_{filt} = 20 kΩ (see Appendix B)	C In	Lim Out	t_r	–	13.5	–	ms
Expander to Compressor Crosstalk	V (C In) = 0 Vrms, V_{in} = –10 dBV	Rx Audio In	Lim Out	C_T	–	–43.6	–	dB
Tx Data Mute	V_{in} = –10 dBV, ALC disabled No popping detectable during Rx Mute transitions	C In	Lim Out	M_e	–	–76	–	dB
ALC Dynamic Range	–	C In	Lim Out	DR	–	–18 to 2.5	–	dBV
ALC Output Level	V_{in} = –18 dBV V_{in} = –2.5 dBV	C In	Lim Out	ALC_{out}	– –	–16 –11.4	– –	dBV
Limiter Output Level	ALC disabled	C In	Tx Out	V_{lim}	–	0.8	–	V_{pp}

ELECTRICAL CHARACTERISTICS (continued)

Splatter Amplifier

The Splatter Amplifier is an inverting rail–to–rail output operational amplifier with the non–inverting input terminal connected to the internal V_B half supply reference. External resistors and capacitors can be connected to set the gain and frequency response. The “Spl Amp In” input is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, External resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Open Loop Gain	–	Spl Amp In	Tx Out	A_{VOL}	–	60	–	dB
Gain Bandwidth	–	Spl Amp In	Tx Out	GBW	–	100	–	kHz
Maximum Output Swing	R_L = 10 kΩ	Spl Amp In	Tx Out	V_{Omax}	–	V_{CC} – 0.3	–	V_{pp}

Tx Audio Path Recommendation

The recommended configuration for the Tx Audio path includes setting the Microphone Amplifier gain to 16 dB using the external gain setting resistors and setting the Splatter Amplifier gain to 9.0 dB using the external gain setting resistors.

PLL Voltage Regulator

The PLL supply voltage is regulated to a nominal of 2.2 V. The “V_{CC} Audio” pin is the supply voltage for the internal voltage regulator. The “PLL V_{ref} ” pin is the 2.2 V regulated output voltage. Two capacitors with 10 μF and 0.01 μF values must be connected to the “PLL V_{ref} ” pin to filter and stabilize this regulated voltage. The voltage regulator provides power for the 2nd LO, Rx and Tx PLL’s, and MPU Interface. The voltage regulator can also be used to provide a regulated supply voltage for external IC’s. Rx and Tx PLL loop performance are independent of the power supply voltage when the voltage regulator is used. The voltage regulator requires about 200 mV of “headroom”. When the power supply decreases to within about 200 mV of the output voltage, the regulator will go out of regulation but the output voltage will not turn off. Instead, the output voltage will maintain about a 200 mV delta to the power supply voltage as the power supply voltage continues to decrease. The “PLL V_{ref}” pin can be connected to “V_{CC} Audio” by the external wiring if voltage higher than 2.2 V is required. But it should not be connected to other supply except “V_{CC} Audio”. The voltage regulator is “on” in the Active and Rx modes. In the Standby and Inactive modes, the voltage regulator is turned off to reduce current drain and the “PLL V_{ref}” pin is internally connected to “V_{CC} Audio” (i.e., the supply voltage is maintained but is now unregulated).

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Output Voltge Level	V_{CC} = 2.6 V, O_L = 0 mA	–	V_{CC} PLL	V_{out}	–	2.2	–	V
Line Regulation	I_L = 0 mA, V_{CC} = 2.6 to 5.5 V	V_{CC}	V_{CC} PLL	Reg_{line}	–	3.66	40	mV
Load Regulation	V_{CC} = 2.6 V, I_L = 0 to 1.0 mA	V_{CC}	V_{CC} PLL	Reg_{load}	–40	–2.28	–	mV

ELECTRICAL CHARACTERISTICS (continued)

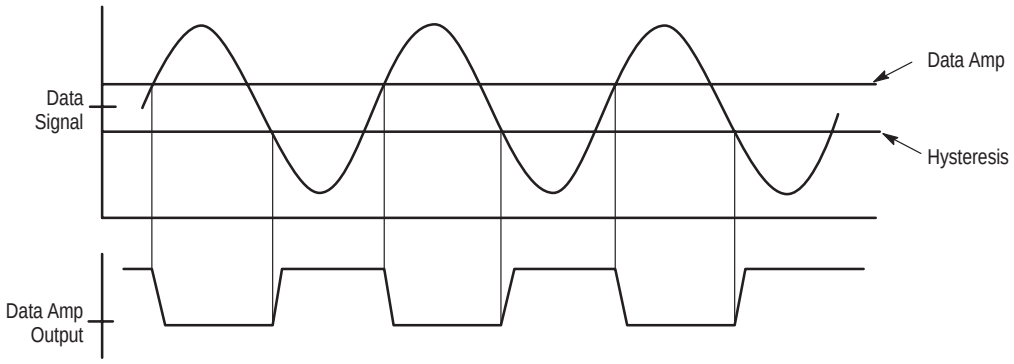
Low Battery Detect

An external resistor divider is connected to the “Ref” input pin to set the threshold for the low battery detect. The voltage at the “Ref” input pin is compared to an internal 1.23 V Bandgap reference voltage. The “BD Out” pin is open collector and requires and external pull–up resistor to V_{CC}.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Average Threshold Voltage	Take average of rising and falling threshold	Ref	Ref/ BD Out	Threshold	–	1.23	–	V
Hysteresis	–	Ref	Ref/ BD Out	Hys	–	2.0	–	mV
Input Current	V_{in} = 1.6 V	–	Ref	I_{in}	–	12.33	50	nA
Output High Voltage	V_{ref} = 1.6, R_L = 3.9 kΩ	Ref	BD Out	V_{OH}	V_{CC} – 0.1	2.59	–	V
Output Low Voltage	V_{ref} = 0.9, R_L = 3.9 kΩ	Ref	BD Out	V_{OL}	–	0.6	0.4	V

Figure 3. Data Amp Operation



PIN FUNCTION DESCRIPTION

48–TQFP Pin	52–QFP Pin	Symbol	Type	Description
1 2	1 2	LO_2 In LO2 Out	–	These pins form the PLL reference oscillator when connected to an external parallel–resonant crystal (10.24 MHz typical). The reference oscillator is also the second Local Oscillator (LO_2) for the RF receiver.
3	3	PLL V_{ref}	Supply	Voltage Regulator output pin. The internal voltage regulator provides a stable power supply voltage for the Rx and Tx PLL's and can also be used as a regulated supply voltage for the other IC's.
4	4	Rx PD	Output	Three state voltage output of the Rx Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external Rx PLL loop filter. It is important to minimize the line length and capacitance of this pin.
5	5	Gnd PLL	Gnd	Ground pin for PLL section of IC.
6	6	Tx PD	Output	Three state voltage output of the Tx Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external Tx PLL loop filter. It is important to minimize the line length and capacitance on this pin.
7	7	E Cap	–	Expander rectifier filter capacitor pin. Connect capacitor to V_{CC}.
8	8	Tx VCO	Input	Transmit divide counter input which is driven by an ac coupled external transmit loop VCO. The minimum signal level is 200 mV_{pp} @ 80.0 MHz. This pin also functions as the test mode input for the counter tests.
9 10 11	9 10 11	Data EN Clk	Input	Microprocessor serial interface input pins for programming various counters and control functions.
12	12	Clk Out	Output	Microprocessor Clock Output which is derived from the 2nd LO crystal oscillator and a programmable divider. It can be used to drive a microprocessor and thereby reduce the number of crystals required in the system design. The driver has an internal resistor in series with the output which can be combined with an external capacitor to form a low pass filter to reduce radiated noise on the PCB. This output also functions as the output for the counter test modes.
N/A	14	Status Out	Output	This pin indicates when the internal latches may have lost memory due to a power glitch.
13	15	CD Out/ Hardware Interrupt	Output/ Input	Dual function pin; 1) Carrier detect output (open collector with external 100 kΩ pull–up resistor. 2) Hardware interrupt input which can be used to "wake–up" from Inactive Mode.
14	16	BD Out	Output	Low battery detect output (open collector with external pull–up resistor).
15	17	DA Out	Output	Data amplifier output (open collector with internal 100 kΩ pull–up resistor).
16	18	SA Out	Output	Speaker amplifier output.
17	19	SA In	Input	Speaker amplifier input (ac coupled).
18	20	E Out	Output	Expander output.
19	21	V_{CC} Audio	Supply	V_{CC} supply for audio section.
20	22	DA In	Input	Data amplifier input (ac coupled).
21	23	Pre–Amp Out	Output	Pre–amplifier output for connection of pre–amplifier feedback resistor.
22	24	Rx Audio In	Input	Rx audio input to pre–amplifier (ac coupled).
23	25	Det Out	Output	Audio output from FM detector.
24	26	RSSI	–	Receive signal strength indicator filter capacitor.
N/A	27	N/A	–	Not used.
25	28	Q Coil	–	A quad coil or ceramic discriminator are connected to this pin.
26	29	V_{CC} RF	Supply	V_{CC} supply for RF receiver section.
27 28	30 31	Lim C2 Lim C1	–	IF amplifier/limiter capacitor pins.

PIN FUNCTION DESCRIPTION (continued)

48–TQFP Pin	52–QFP Pin	Symbol	Type	Description
29	32	Lim In	Input	Signal input for IF amplifier/limiter.
30	33	Gnd RF	Gnd	Ground pin for RF section of the IC.
31	34	Mix_2 Out	Output	Second mixer output.
32	35	Mix_2 In	Input	Second mixer input.
33	36	V_B	–	Internal half supply analog ground reference.
34	37	Mix_1 Out	Output	First mixer output.
35	38	Mix_1 In_2	Input	Negative polarity first mixer input.
36	39	Mix_1 In_1	Input	Positive polarity first mixer input.
37 38	40 41	LO_1 In LO_1 Out	–	Tank elements for 1st LO multivibrator oscillator are connected to these pins.
39	42	V_{cap} Ctrl	–	1st LO varactor control pin.
40	43	Gnd Audio	Gnd	Ground for audio section of the IC.
41	44	Tx In	Input	Tx path input to Microphone Amplifier (ac coupled).
42	45	Amp Out	Output	Microphone amplifier output.
43	46	C In	Input	Compressor input (ac coupled).
44	47	C Cap	–	Compressor rectifier filter capacitor pin. Connect capacitor to V_{CC}.
45	48	Lim Out	Output	Tx path limiter output.
46	49	Spl Amp In	Input	Splatter amplifier input (ac coupled).
47	50	Tx Out	Output	Tx path audio output.
48	51	Ref	Input	Reference voltage input for low battery detect.
N/A	52	N/A	–	Not used.

Power Supply Voltage

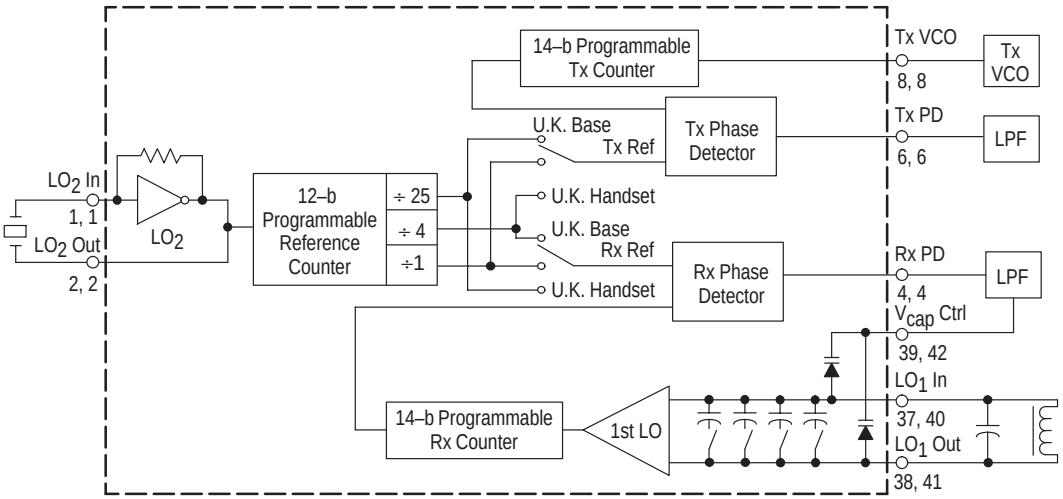
This circuit is used in a cordless telephone handset and base unit. The handset is battery powered and can operate on two or three NiCad cells or on 5.0 V power.

PLL Frequency Synthesizer General Description

Figure 4 shows a simplified block diagram of the programmable universal dual phase locked loop (PLL). This dual PLL is fully programmable through the MCU serial interface and supports most country channel frequencies including USA (25 ch), France, Spain, Australia, Korea, New Zealand, U.K., Netherlands and China (see channel frequency tables in Appendix A).

The 2nd local oscillator and reference divider provide the reference frequency for the Rx and Tx PLL loops. The programmed divider value for the reference divider is selected based on the crystal frequency and the desired Rx and Tx reference frequency values. Additional divide by 25 and divide by 4 blocks are provided to allow for generation of the 1.0 kHz and 6.25 kHz reference frequencies required for the U.K. The 14–Bit Tx counter is programmed for the desired transmit channel frequency. The 14–Bit Rx counter is programmed for the desired first local oscillator frequency. All counters power up in the proper default state for USA channel #6 and for a 10.24 MHz reference frequency crystal. Internal fixed capacitors can be connected to the tank circuit of the 1st LO through microprocessor control to extend the sensitivity of the 1st LO for U.S. 25 channel operation.

Figure 4. Dual PLL Simplified Block Diagram



ELECTRICAL CHARACTERISTICS (V_{CC} = 2.6 V, T_A = 25°C)

Characteristic	Condition	Measure Pin	Symbol	Min	Typ	Max	Unit
PLL PIN DC							
Input Voltage Low	–	Data Clk EN Hardware Int.	V_{IL}	–	–	0.3	V
Input Voltage High	–	Data Clk EN	V_{IH}	"PLL V_{ref}" – 0.3	–	"V_{CC} Audio"	V
Input Current Low	V_{in} = 0.3 V	Data Clk EN	I_{IL}	–5.0	–3.0	–	μA
Input Current High	V_{in} = (V_{CC} Audio) – 0.3	Data Clk EN	I_{IH}	–	0.6	5.0	μA
Hysteresis Voltage	–	Data Clk EN	V_{hys}	–	1.0	–	V
Output Current High	–	Rx PD Tx PD	I_{OH}	–	–	–0.7	mA
Output Current Low	–	Rx PD Tx PD	I_{OL}	0.7	–	–	mA
Output Voltage Low	I_{IL} = 0.7 mA	Rx PD Tx PD	V_{OL}	–	–	(PLL V_{ref})* 0.2	V
Output Voltage High	I_{IH} = –0. 7mA	Rx PD Tx PD	V_{OH}	(PLL V_{ref})* 0.8	–	–	V
Tri–State Leakage Current	V = 1.2 V	Rx PD Tx PD	I_{OZ}	–50	–	50	nA
Input Capacitance	–	Data Clk EN	C_{in}	–	–	8.0	pF
Output Capacitance	–	Rx PD Tx PD	C_{out}	–	–	8.0	pF

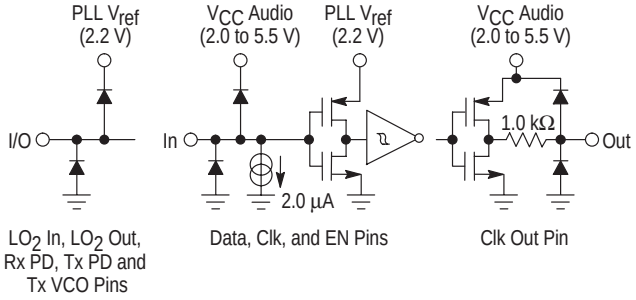
ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 2.6 V, T_A = 25°C)

Characteristic	Condition	Measure Pin	Symbol	Min	Typ	Max	Unit
PLL PIN INTERFACE							
EN to Clk Setup Time	–	EN, Clk	t_{suEC}	200	–	–	ns
Data to Clk Setup Time	–	Data, Clk	t_{suDC}	100	–	–	ns
Hold Time	–	Data, Clk	t_h	90	–	–	ns
Recovery Time	–	EN, Clk	t_{rec}	90	–	–	ns
Input Pulse Width	–	EN, Clk	t_w	100	–	–	ns
Input Rise and Fall Time	–	Data Clk EN	t_r, t_f	–	–	9.0	µs
MPU Interface Power–Up Delay	90% of PLL V_{ref} to Data, Clk, EN	–	t_{puMPU}	–	100	–	µs
PLL LOOP							
2nd LO Frequency	–	LO_2 In LO_2 Out	f_{LO}	–	–	12	MHz
"Tx VCO" Input Frequency	V_{in} = 200 mV_{pp}	Tx VCO	f_{txmax}	–	–	80	MHz

PLL I/O Pin Specifications

The 2nd LO, Rx and Tx PLL's and MPU serial interface are normally powered by the internal voltage regulator at the "PLL V_{ref}" pin. The "PLL V_{ref}" pin is the output of a voltage regulator which is powered from the "V_{CC} Audio" power supply pin. Therefore, the maximum input and output levels for most PLL I/O pins (LO_2 In, LO_2 Out, Rx PD, Tx PD, Tx VCO) is the regulated voltage at the "PLL V_{ref}" pin. The ESD protection diodes on these pins are also connected to "PLL V_{ref}". Internal level shift buffers are provided for the pins (Data, Clk, EN, Clk Out) which connect directly to the microprocessor. The maximum input and output levels for these pins is V_{CC}. Figure 5 shows a simplified schematic of the PLL I/O pins.

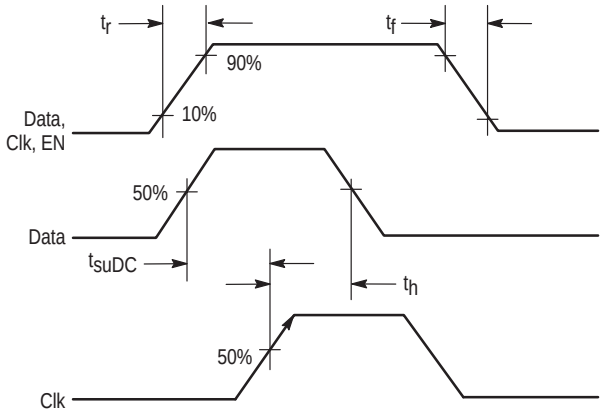
Figure 5. PLL I/O Pin Simplified Schematics



Microprocessor Serial Interface

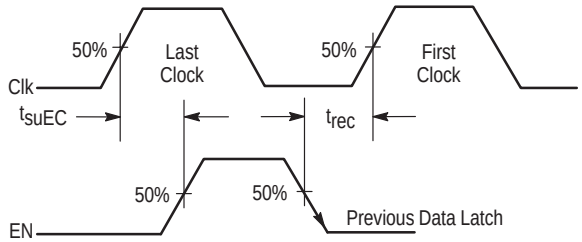
The "Data", "Clk", and "EN" pins provide an MPU serial interface for programming the reference counters, the transmit and receive channel divider counter and various control functions. The "Data" and "Clk" pins are used to load data into the shift register. Figure 6 shows "Data" and "Clk" pin timing. Data is clocked on positive clock transitions.

Figure 6. Data and Clock Timing Requirement



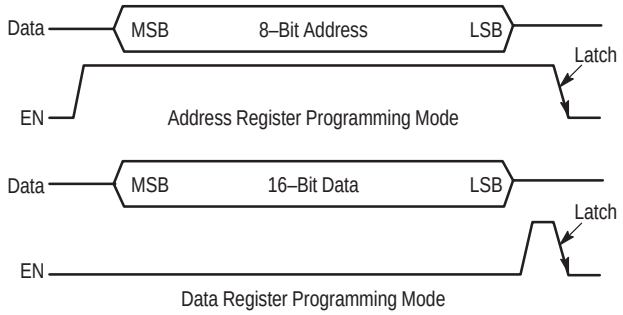
After data is loaded into the shift register, the data is latched into the appropriate latch register using the "EN" pin. This is done in two steps. First, an 8–Bit address is loaded into the shift register and latched into the 8–Bit address latch register. Then, up to 16–Bits of data is loaded into the shift register and latched into the data latch register specified by the address that was previously loaded. Figure 7 shows the timing required on the EN pin. Latching occurs on the negative EN transition.

Figure 7. Enable Timing Requirement



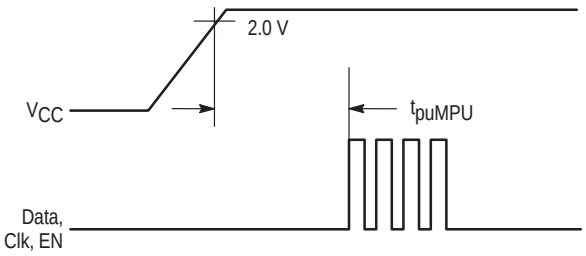
The state of the EN pin when clocking data into the shift register determines whether the data is latched into the address register or a data register. Figure 8 shows the address and data programming diagrams. In the data programming mode, there must not be any clock transitions when “EN” is high. The clock can be in a high state (default high) or a low state (default low) but must not have any transitions during the “EN” high state. The convention in these figures is that latch bits to the left are loaded into the shift register first.

Figure 8. Microprocessor Interface Programming Mode Diagrams



The MPU serial interface is fully operational within 100 μs after the power supply has reached its minimum level during power–up (See Figure 9). The MPU Interface shift registers and data latches are operational in all four power saving modes; Inactive, Standby, Rx, and Active Modes. Data can be loaded into the shift registers and latched into the latch registers in any of the operating modes.

Figure 9. Microprocessor Serial Interface Power–Up Delay



Status Out

This is a digital output which indicates whether the latch registers have been reset to their power–up default values. Latch power–up default values are given in Figure 28. If there is a power glitch or ESD event which causes the latch registers to be reset to their default values, the “Status Out” pin will indicate this to the MPU so it can reload the correct information into the latch registers.

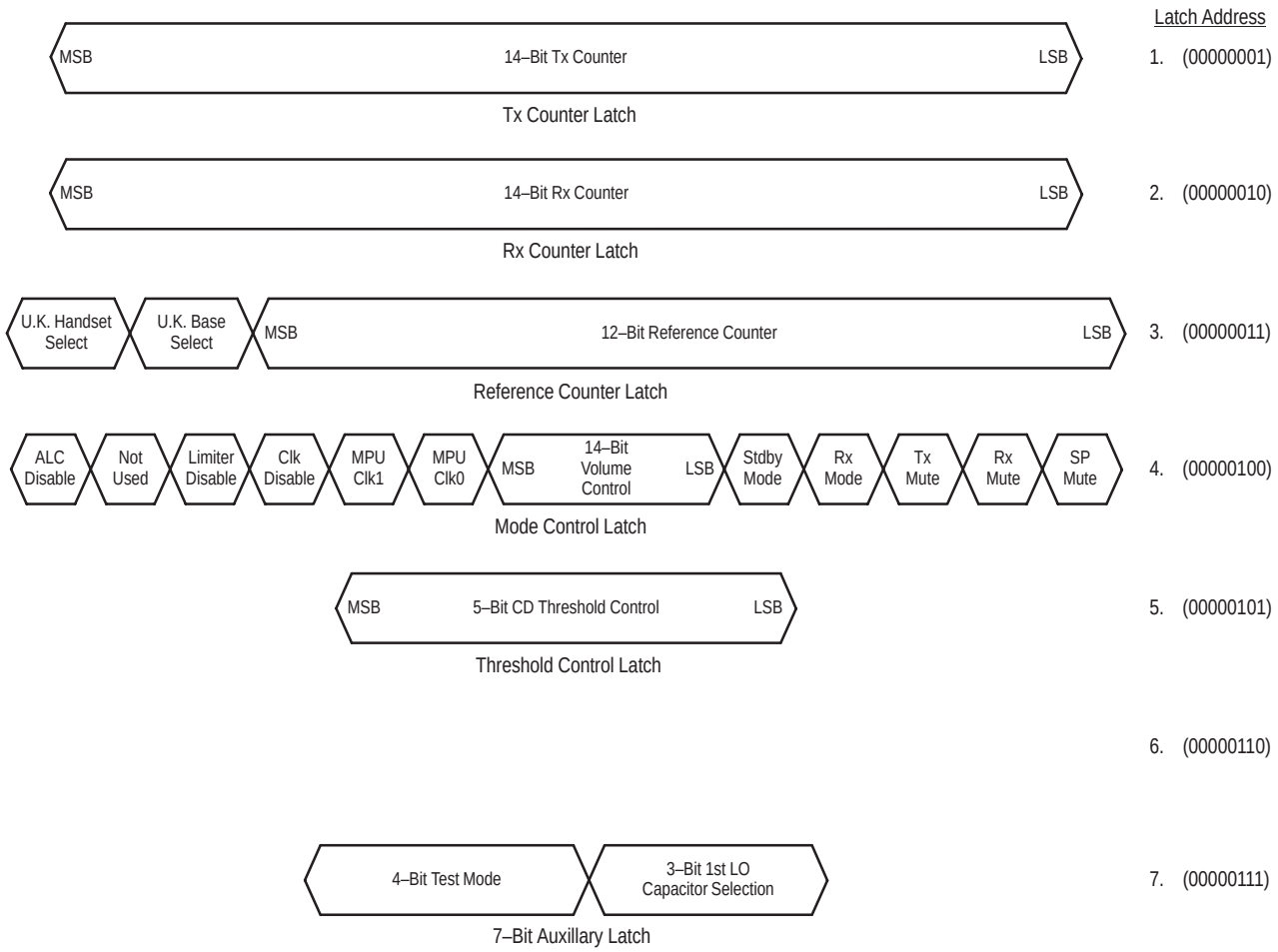
Figure 10. Status Out Operation

Status Latch Register Bits	Status Out Logic Level
Latch bits not at power–up default value	0
Latch bits at power–up default value	1

Data Registers

Figure 11 shows the data latch registers and addresses which are used to select each of these registers. Latch bits to the left (MSB) are loaded into the shift register first. The LSB bit must always be the last bit loaded into the shift register. “Don’t Care” bits can be loaded into the shift register first if 8–Bit bytes of data are loaded.

Figure 11. Microprocessor Interface Data Latch Registers



Reference Frequency Selection

The "LO_2 In" and "LO_2 Out" pins form a reference oscillator when connected to an external parallel–resonant crystal. The reference oscillator is also the second local oscillator for the RF Receiver. Figure 12 shows the relationship between different crystal frequencies and reference frequencies for cordless phone applications in various countries.

Figure 12. Reference Frequency and Reference Divider Values

Crystal Frequency	Reference Divider Value	U.K. Base/ Handset Divider	Reference Frequency
10.24 MHz	2048	1	5.0 kHz
10.24 MHz	1024	4	2.5 kHz
11.15 MHz	2230	1	5.0 kHz
12.00 MHz	2400	1	5.0 kHz
11.15 MHz	1784	1	6.25 kHz
11.15 MHz	446	4	6.25 kHz
11.15 MHz	446	25	1.0 kHz

Reference Counter

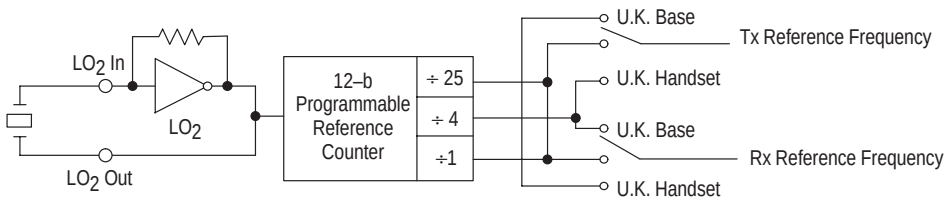
Figure 14 shows how the reference frequencies for the Rx and Tx loops are generated. All countries except U.K. require that the Tx and Rx reference frequencies be identical. In this case, set "U.K. Base Select" and "U.K. Handset Select" bits to "0". Then the fixed divider is set to "1" and the Tx and Rx reference frequencies will be equal to the crystal oscillator frequency divided by the programmable reference counter value. The U.K. is a special case which requires a different reference frequency value of Tx and Rx.

For U.K. base operation, set "U.K. Base Select" to "1". For U.K. handset operation, set "U.K. Handset Select" to "1". The Netherlands is also a special case since a 2.5 kHz reference frequency is used for both the Tx and Rx reference and the total divider value required is 4096 which is larger than the maximum divide value available from the 12–Bit reference divider (4095). In this case, set "U.K. Base Select" to "1" and set "U.K. Handset Select" to "1". This will give a fixed divide by 4 for both the Tx and Rx reference. Then set the reference divider to 1024 to get a total divider of 4096.

Mode Control Register

Power saving modes, mutes, disables, volume control, and microprocessor clock output frequency are all set by the Control Register. Operation of the Control Register is explained in Figures 15 through 21.

Figure 13. Reference Register Programming Mode



U.K. Handset Select	U.K. Base Select	Tx Divider Value	Rx Divider Value	Application
0	0	1	1	All but U.K. and Netherlands
0	1	25	4	U.K. Baseset
1	0	4	25	U.K. Handset
1	1	4	4	Netherlands Base and Handset

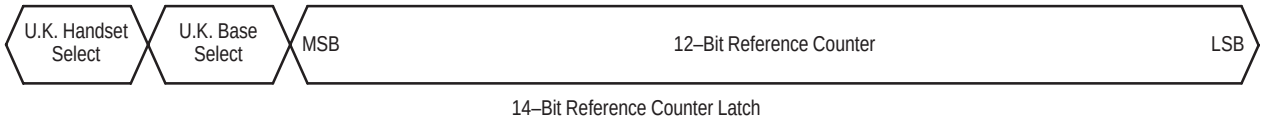


Figure 14. Control Register Bits

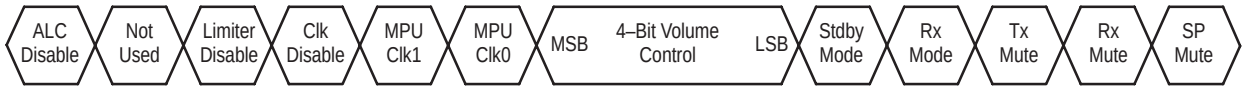


Figure 15. Mute and Disable Control Bit Descriptions

ALC Disable	1 0	Automatic Level Control Disabled Normal Operation
Limiter Disable	1 0	Limiter Disabled Normal Operation
Clock Disable	1 0	MPU Clock Output Disabled Normal Operation
Tx Mute	1 0	Transmit Channel Muted Normal Operation
Rx Mute	1 0	Receive Channel Muted Normal Operation
SP Mute	1 0	Speaker Amp Muted Normal Operation

Power Saving Operating Modes

When the MC13109A is used in a handset, it is important to conserve power in order to prolong battery life. There are five modes of operation; Active, Rx, Standby, Interrupt and Inactive. In Active Mode, all circuit blocks are powered. In Rx mode, all circuitry is powered down except for those circuit sections needed to receive a transmission from the base. In the Standby and Interrupt Modes, all circuitry is powered down except for the circuitry needed to provide the clock output for the microprocessor. In Inactive Mode, all circuitry is powered down except the MPU interface. Latch memory is maintained in all modes. Figure 17 shows the control register bit values for selection of each power saving mode and Figure 18 show the circuit blocks which are powered in each of these operating mode.

Figure 16. Power Saving Mode Selection

Stdby Mode Bit	Rx Mode Bit	"CD Out/Hardware Interrupt" Pin	Power Saving Mode
0	0	X	Active
0	1	X	Rx
1	0	X	Standby
1	1	1 or High Impedance	Inactive
1	1	0	Inactive

Figure 17. Circuit Blocks Powered During Power Saving Modes

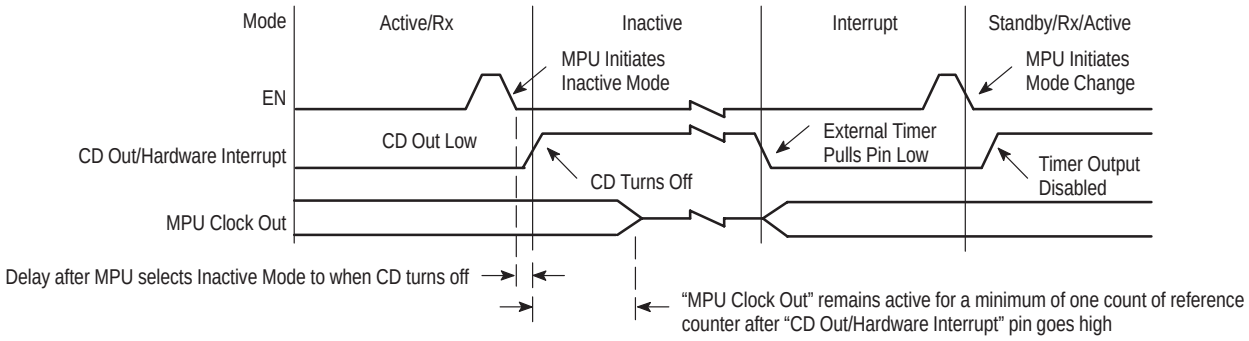
Circuit Blocks	Active	Rx	Standby	Inactive
"PLL V_{ref}" Regulated Voltage	X	X	X[1]	X[1]
MPU Interface	X	X	X	X
2nd LO Oscillator	X	X	X	
MPU Clock Output	X	X	X	
RF Receiver	X	X		
1st LO VCO	X	X		
Rx PLL	X	X		
Carrier Detect	X	X		
Data Amp	X	X		
Low Battery Detect	X	X		
Tx PLL	X			
Rx Audio Path	X			
Tx Audio Path	X			

NOTE: 1. In Standby and Inactive Modes, "PLL V_{ref}" remains powered but is not regulated. It will fluctuate with V_{CC}.

Inactive Mode Operation and Hardware Interrupt

In some handset applications it may be desirable to power down all circuitry including the microprocessor (MPU). First put the MC13109A into the Inactive mode, which turns off the MPU Clock Output (see Figure 21), and then disable the microprocessor. In order to give the MPU adequate time to power down, the MPU Clock output remains active for a minimum of one reference counter cycle (about 200 μs) after the command is given to switch into the "Inactive" mode. An external timing circuit should be used to initiate the turn–on sequence. The "CD Out" pin has a dual function. In the Active and Rx modes it performs the carrier detect function. In the Standby and Inactive modes the carrier detect circuit is disabled and the "CD Out" pin is in a "High" state due to the external pull–up resistor. In the Inactive mode the "CD Out" pin is the input for the hardware interrupt function. When the "CD Out" pin is pulled "low" by the external timing circuit, the MC13109A switches from the Inactive to the Interrupt mode thereby turning on the MPU Clock Output. The MPU can then resume control of the combo IC. The "CD Out" pin must remain low until the MPU changes the operating mode from Interrupt to Standby, Active or Rx modes.

Figure 18. Hardware Interrupt Operation



"Clk Out" Divider Programming

The "Clk Out" pin is derived from the 2nd local oscillator and can be used to drive a microprocessor, thereby reducing the number of crystals required. Figure 22 shows the relationship between the crystal frequency and the clock output for different divider values. Figure 20 shows the "Clk Out" register bit values.

Figure 19. Clock Output Values

Crystal Frequency	Clock Output Divider			
	2	3	5	10
10.24 MHz	5.120 MHz	3.413 MHz	2.048 MHz	1.024 MHz
11.15 MHz	5.575 MHz	3.717 MHz	2.230 MHz	1.115 MHz
12.00 MHz	6.000 MHz	4.000 MHz	2.400 MHz	1.200 MHz

Figure 20. Clock Output Divider

Clk Out Bit #1	Clk Out Bit #2	Clk Out Divider Value
0	0	2
0	1	3
1	0	5
1	1	10

MPU "Clk Out" Power–Up Default Divider Value

The power–up default divider value is "divide by 10". This provides an MPU clock of about 1.0 MHz after initial power–up. The reason for choosing this relatively low clock frequency after intial power–up is that some microprocessors that operate down to a 2.0 V power supply have a maximum clock frequency of 1.0 MHz. After initial power–up, the MPU can change the clock divider value to set the clock to the desired operating frequency. Special care has been taken in the design of the clock divider to ensure that the transition between one clock divider value and another is "smooth" (i.e., there will be no narrow clock pulses to disturb the MPU).

MPU "Clk Out" Radiated Noise on Circuit Board

The clock line running between the MC13109A and the microprocessor has the potential to radiate noise which can cause problems in the system especially if the clock is a square wave digital signal with large high frequency harmonics. In order to minimize radiated noise, a 1.0 kΩ resistor is included on–chip in–series with the "Clk Out" output driver. A small capacitor can be connected to the "Clk Out" line on the PCB to form a single pole low pass filter. This filter will significantly reduce noise radiated from the "Clk Out" line.

Volume Control

The volume control can be programmed in 2.0 dB gain steps from –14 dB to 16 dB. The power–up default value is 0 dB.

Figure 21. Volume Control

Volume Control Bit #3	Volume Control Bit #2	Volume Control Bit #1	Volume Control Bit #0	Volume Control #	Gain/Attenuation Amount
0	0	0	0	0	–14 dB
0	0	0	1	1	–12 dB
0	0	1	0	2	–10 dB
0	0	1	1	3	–8.0 dB
0	1	0	0	4	–6.0 dB
0	1	0	1	5	–4.0 dB
0	1	1	0	6	–2.0 dB
0	1	1	1	7	0 dB
1	0	0	0	8	2.0 dB
1	0	0	1	9	4.0 dB
1	0	1	0	10	6.0 dB
1	0	1	1	11	8.0 dB
1	1	0	0	12	10 dB
1	1	0	1	13	12 dB
1	1	1	0	14	14 dB
1	1	1	1	15	16 dB

Gain Control Register

The gain control register contains bits which control the Carrier Detect threshold. Operation of these latch bits are explained in Figures 22 and 23.

Figure 22. Gain Control Latch Bits



Carrier Detect Threshold Programming

The “CD Out” pin will give an indication to the microprocessor if a carrier signal is present on the selected channel. The nominal value and tolerance of the carrier detect threshold is given in the carrier detect specification section of this document. If a different carrier detect threshold value is desired, it can be set through the MPU interface as shown in Figure 23 below.

Figure 23. Carrier Detect Threshold Control

CD Bit #4	CD Bit #3	CD Bit #2	CD Bit #1	CD Bit #0	CD Control #	Carrier Detect Threshold
0	0	0	0	0	0	–20 dB
0	0	0	0	1	1	–19 dB
0	0	0	1	0	2	–18 dB
0	0	0	1	1	3	–17 dB
0	0	1	0	0	4	–16 dB
0	0	1	0	1	5	–15 dB
0	0	1	1	0	6	–14 dB
0	0	1	1	1	7	–13 dB
0	1	0	0	0	8	–12 dB
0	1	0	0	1	9	–11 dB
0	1	0	1	0	10	–10 dB
0	1	0	1	1	11	–9.0 dB
0	1	1	0	0	12	–8.0 dB
0	1	1	0	1	13	–7.0 dB
0	1	1	1	0	14	–6.0 dB
0	1	1	1	1	15	–5.0 dB
1	0	0	0	0	16	–4.0 dB
1	0	0	0	1	17	–3.0 dB
1	0	0	1	0	18	–2.0 dB
1	0	0	1	1	19	–1.0 dB
1	0	1	0	0	20	0 dB
1	0	1	0	1	21	1.0 dB
1	0	1	1	0	22	2.0 dB
1	0	1	1	1	23	3.0 dB
1	1	0	0	0	24	4.0 dB
1	1	0	0	1	25	5.0 dB
1	1	0	1	0	26	6.0 dB
1	1	0	1	1	27	7.0 dB
1	1	1	0	0	28	8.0 dB
1	1	1	0	1	29	9.0 dB
1	1	1	1	0	30	10 dB
1	1	1	1	1	31	11 dB

Auxiliary Register

The auxiliary register contains a 3–Bit 1st LO Capacitor Selection latch and a 4–Bit Test Mode latch. Operation of these latch bits are explained in Figures 24, 25 and 26.

Figure 24. Auxiliary Register Latch Bits



First Local Oscillator Capacitor Selection for 25 Channel U.S. Operation

There is a very large frequency difference between the minimum and maximum channel frequencies in the proposed 25 Channel U.S. standard. The sensitivity of the 1st LO is not large enough to accommodate this large frequency variation. Fixed capacitors can be connected across the 1st LO tank circuit to change the 1st LO sensitivity. Internal switches and capacitors are provided to enable microprocessor control over internal fixed capacitor values. Figure 25 shows the schematic of the 1st LO tank circuit. Figure 26 shows the latch control bit values.

Figure 25. First LO Schematic

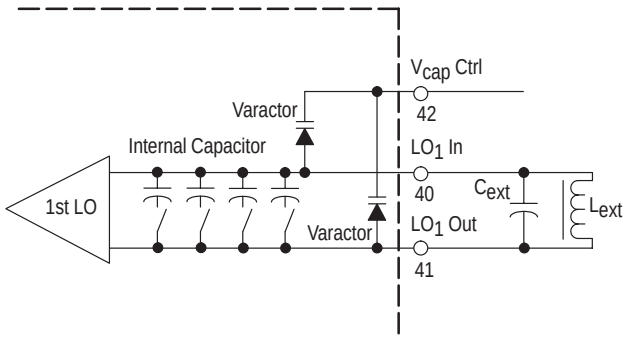


Figure 26. 1st LO Capacitor Select for U.S. 25 Channels

1st LO Cap. Bit 2	1st LO Cap. Bit 1	1st LO Cap. Bit 0	1st LO Cap. Select	U.S. Base Channels	U.S. Handset Channels	Varactor Value over 0.5 to 2.2 V Range	External Capacitor Value	External Inductor Value
0	0	0	0	16 – 25	–	10 – 6.4 pF	27 pF	0.47 μH
0	0	0	0	–	16 – 25	10 – 6.4 pF	33 pF	0.47 μH
0	0	1	1	1 – 6	–	10 – 6.4 pF	27 pF	0.47 μH
0	1	0	2	7 – 15	–	10 – 6.4 pF	27 pF	0.47 μH
0	1	1	3	–	1 – 6	10 – 6.4 pF	33 pF	0.47 μH
1	0	0	4	–	7 – 15	10 – 6.4 pF	33 pF	0.47 μH

Figure 27. Test Mode Description

TM #	TM 3	TM 2	TM 1	TM 0	Counter Under Test or Test Mode Option	"Tx V_{CO}" Input Signal	"Clk Out" Output Expected
0	0	0	0	0	Normal Operation	>200 mVpp	–
1	0	0	0	1	Rx Counter, upper 6	0 to 2.2 V	Input Frequency/64
2	0	0	1	0	Rx Counter, lower 8	0 to 2.2 V	See Note Below
3	0	0	1	1	Rx Prescaler	0 to 2.2 V	Input Frequency/4
4	0	1	0	0	Tx Counter, upper 6	0 to 2.2 V	Input Frequency/64
5	0	1	0	1	Tx Counter, lower 8	0 to 2.2 V	See Note Below
6	0	1	1	0	Tx Prescaler	>200 mVpp	Input Frequency/4
7	0	1	1	1	Reference Counter	0 to 2.2 V	Input Frequency/Reference Counter Value
8	1	0	0	0	Divide by 4, 25	0 to 2.2 V	Input Frequency/100
9	1	0	0	1	AGC Gain = 10 Option	N/A	–
10	1	0	1	0	AGC Gain = 25 Option	N/A	–

NOTE: To determine the correct output, look at the lower 8 bits in the Rx or Tx register (Divisor (7;0). If the value of the divisor is > 16, then the output divisor value is Divisor (7;2) (the upper 6 bits of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) > = 2, then output divisor value is Divisor (3;2) (bits 2 and 3 of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) < 2, then output divisor value is (Divisor (3;2) + 60).

Test Modes

Test Mode Control latch bits enable independent testing of internal counters and set AGC Gain Options. In test mode, the "Tx VCO" input pin is multiplexed to the input of the counter under test and the output of the counter under test is multiplexed to the "Clk Out" output pin so that each counter can be individually tested. Make sure test mode bits are set to "0" for normal operation. Test mode operation is described in Figure 27. During normal operation and when testing the Tx Prescaler, the "Tx VCO" input can be a minimum of 200 mVpp at 80 MHz and should be ac coupled. For other test modes, input signals should be standard logic levels of 0 to 2.2 V and a maximum frequency of 16 MHz.

Power–Up Defaults for Control and Counter Registers

When the IC is first powered up, all latch registers are initialized to a defined state. The MC13109A is initially placed in the Rx mode with all mutes active and nothing disabled. The reference counter is set to generate a 5.0 kHz reference frequency from a 10.24 MHz crystal. The MPU clock output divider is set to 10 to give the minimum clock output frequency. The Tx and Rx latch registers are set for USA Channel Frequency #21. Figure 28 shows the initial power–up states for all latch registers.

Figure 28. Latch Register Power–Up Defaults

		MSB								LSB							
Register	Count	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Tx	9965	–	–	1	0	0	1	1	0	1	1	1	0	1	1	1	0
Rx	7215	–	–	0	1	1	1	0	0	0	0	1	0	1	1	1	1
Ref	2048	–	–	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Mode	N/A	–	0	0	0	0	1	1	0	1	1	1	0	1	1	1	1
Gain	N/A	–	–	–	–	–	–	–	–	–	–	–	1	0	1	0	0
TM	N/A	–	–	–	–	–	–	–	–	–	0	0	0	0	0	0	0

Figure 29. I_{CC} versus V_{CC} at Active Mode

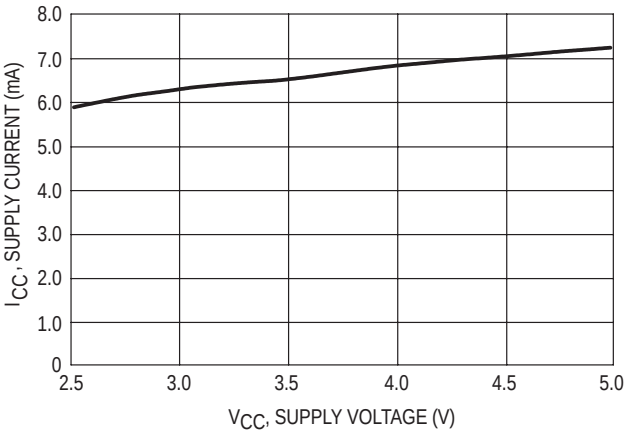


Figure 30. I_{CC} versus V_{CC} at Receive Mode

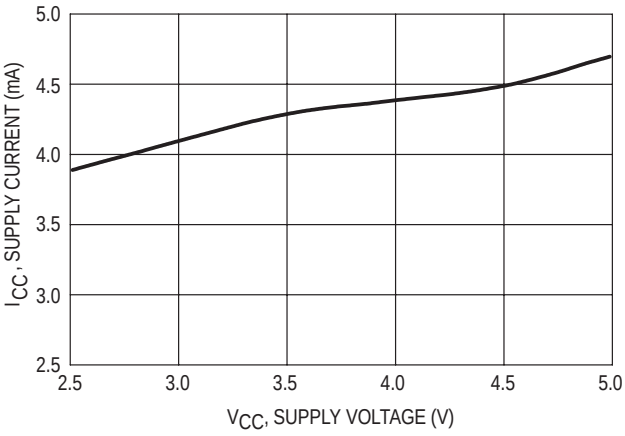


Figure 31. I_{CC} versus V_{CC} at Standby Mode

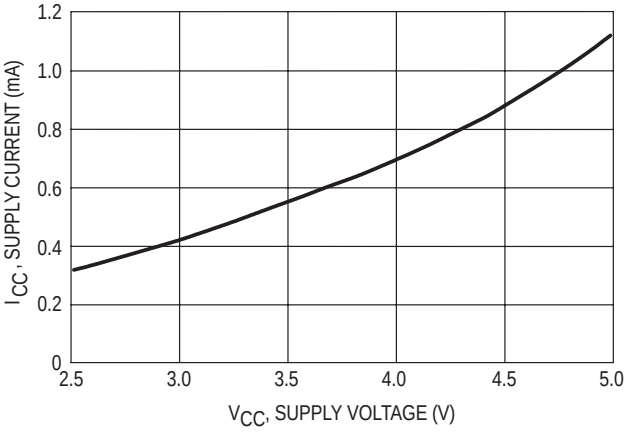


Figure 32. I_{CC} versus V_{CC} at Inactive Mode

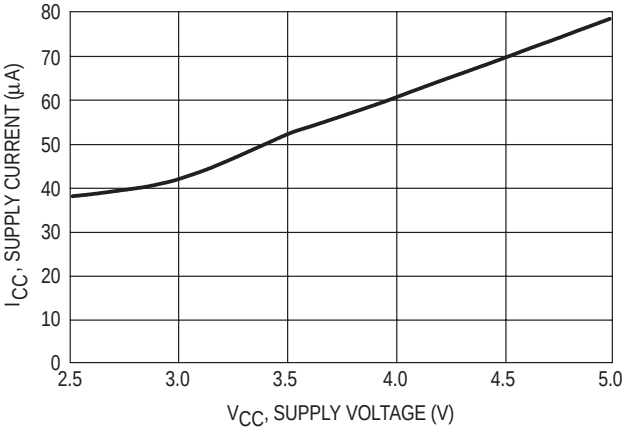


Figure 33. RSSI Output versus RF_{in}

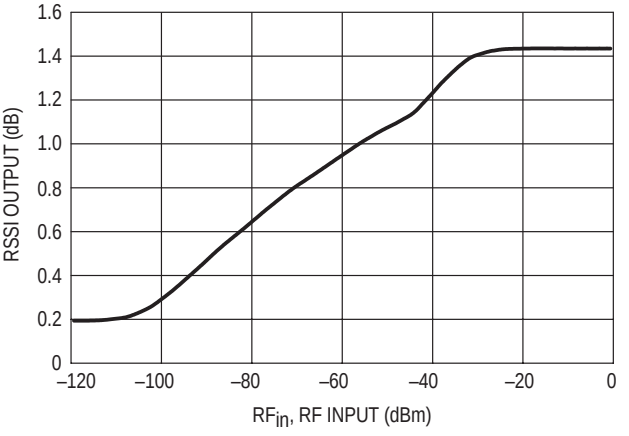


Figure 34. Recovered Audio/THD versus f_{DEV}

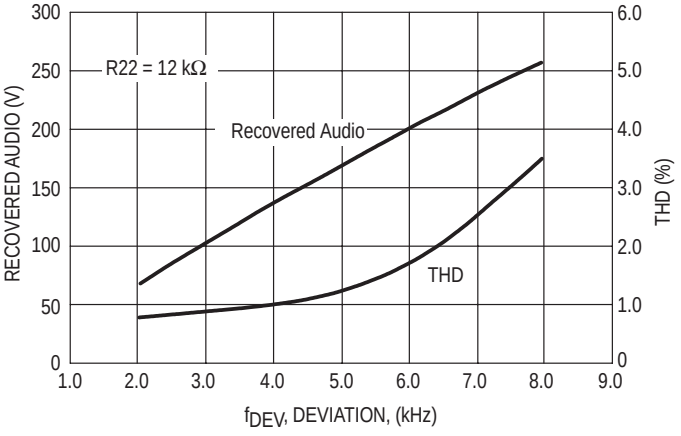


Figure 35. Typical Expander Response

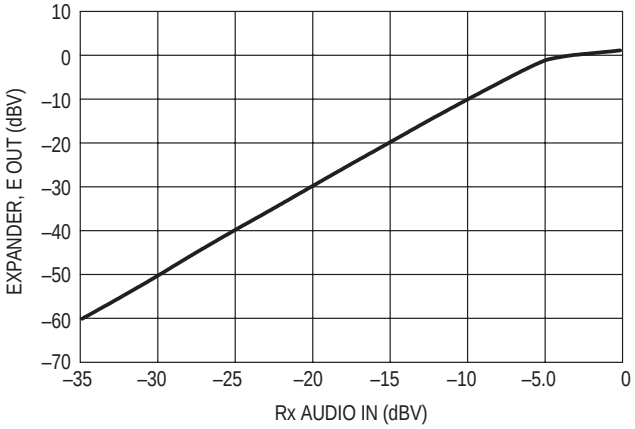


Figure 36. Typical Compressor Response

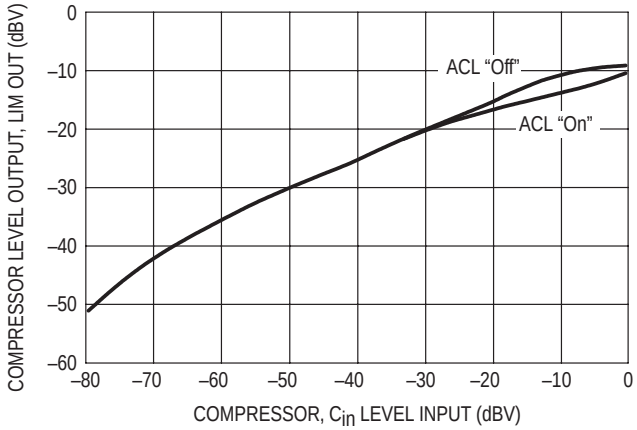


Figure 37. First Mixer Third Order Intercept Performance

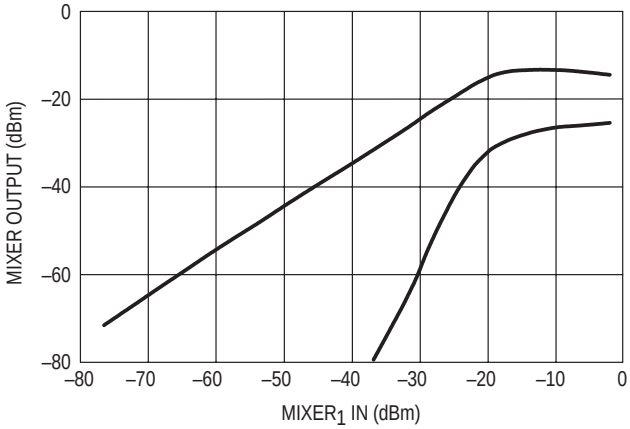
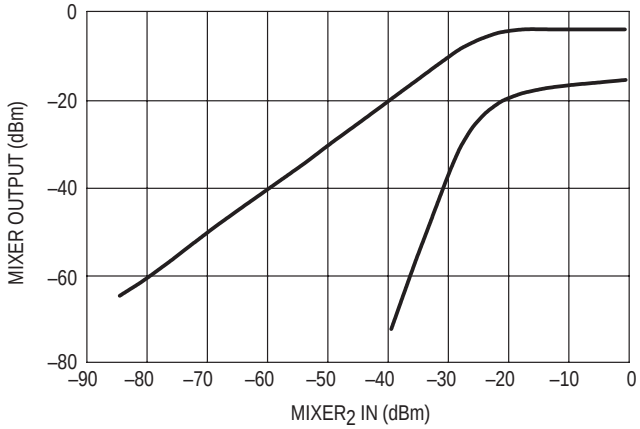


Figure 38. Second Mixer Third Order Intercept Performance



APPENDIX A – MEASUREMENT OF COMPANDOR ATTACK/DECAY TIME

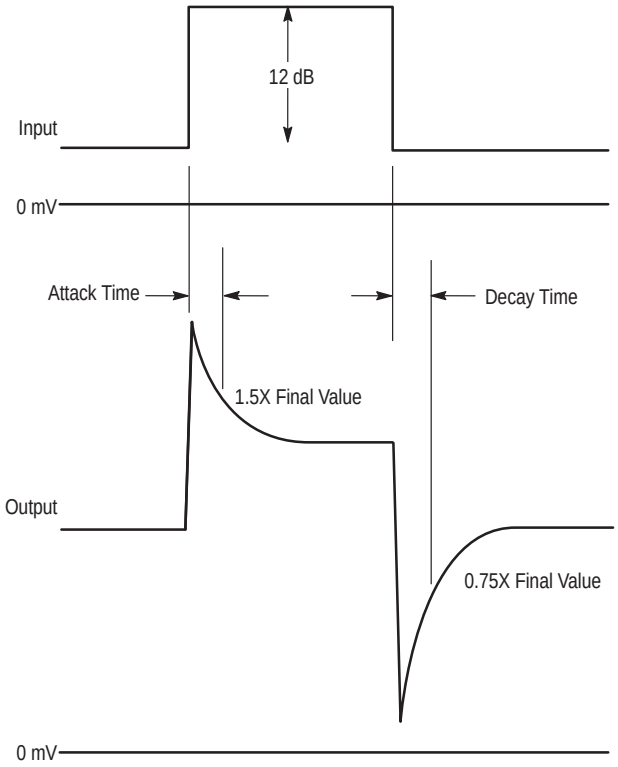
This measurement definition is based on EIA/CCITT recommendations.

Compressor Attack Time

For a 12 dB step up at the input, attack time is defined as the time for the output to settle to 1.5X of the final steady state value.

Compressor Decay Time

For a 12 dB step down at the input, decay time is defined as the time for the input to settle to 0.75X of the final steady state value.

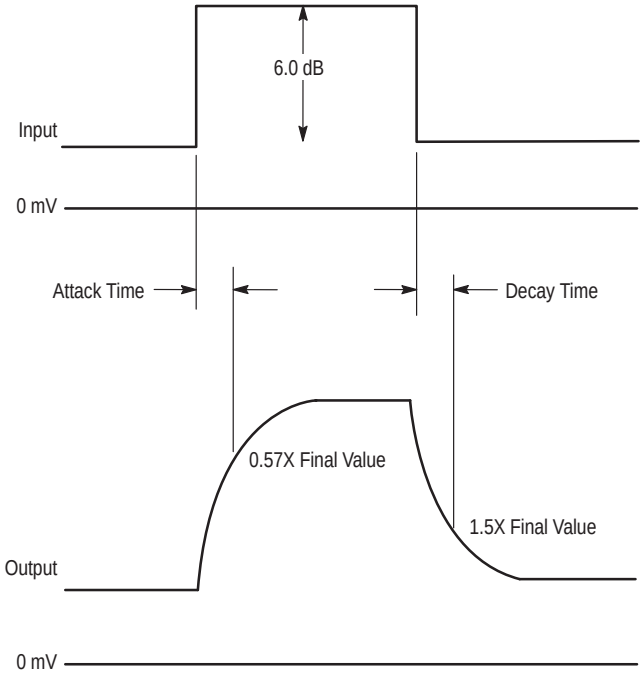


Expander Attack

For a 6.0 dB step up at the input, attack time is defined as the time for the output to settle to 0.57X of the final steady state value.

Expander Decay

For a 6.0 dB step down at the input, decay time is defined as the time for the output to settle to 1.5X of the final steady state value.



MOTOROLA

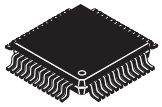
MC13110A
MC13111A

Universal Cordless Telephone Subsystem IC

The MC13110A and MC13111A integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, external adjustments, and lowers overall costs. It is designed for use in both the handset and the base.

- Fully Programmable in all Power Modes
- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna Input to Audio Out 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expander Includes Mute, Digital Volume Control, Speaker Driver, Programmable Low Pass Filter, and Gain Block
  - Compressor Includes Mute, Programmable Low Pass Filter, Limiter, and Gain Block
- MC13110A only: Frequency Inversion Scrambler
  - Function Controlled via MPU Interface
  - Programmable Carrier Modulation Frequency
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign Cordless Telephone Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Outputs Eliminates Need for MPU Crystal
- Low Battery Detect
  - Provides Two Levels of Monitoring with Separate Outputs
  - Separate, Adjustable Trip Points
- 2.7 to 5.5 V Operation (15 μA Current Consumption in Inactive Mode)
- AN1575: Refer to this Application Note for a List of the “Worldwide Cordless Telephone Frequencies

UNIVERSAL NARROWBAND FM RECEIVER INTEGRATED CIRCUIT



52 1

FB SUFFIX
PLASTIC PACKAGE
CASE 848B
(QFP–52)



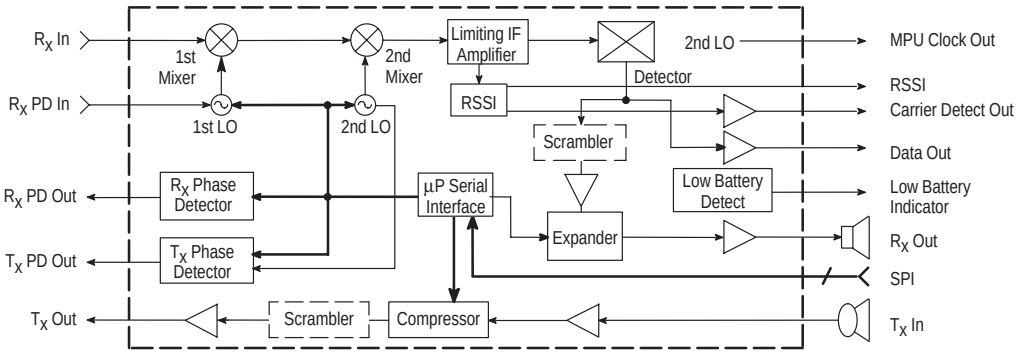
48 1

FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(LQFP–48)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC13110AFB	T_A = – 40° to 85°C	QFP–52
MC13110AFTA		LQFP–48
MC13111AFB		QFP–52
MC13111AFTA		LQFP–48

Simplified Block Diagram

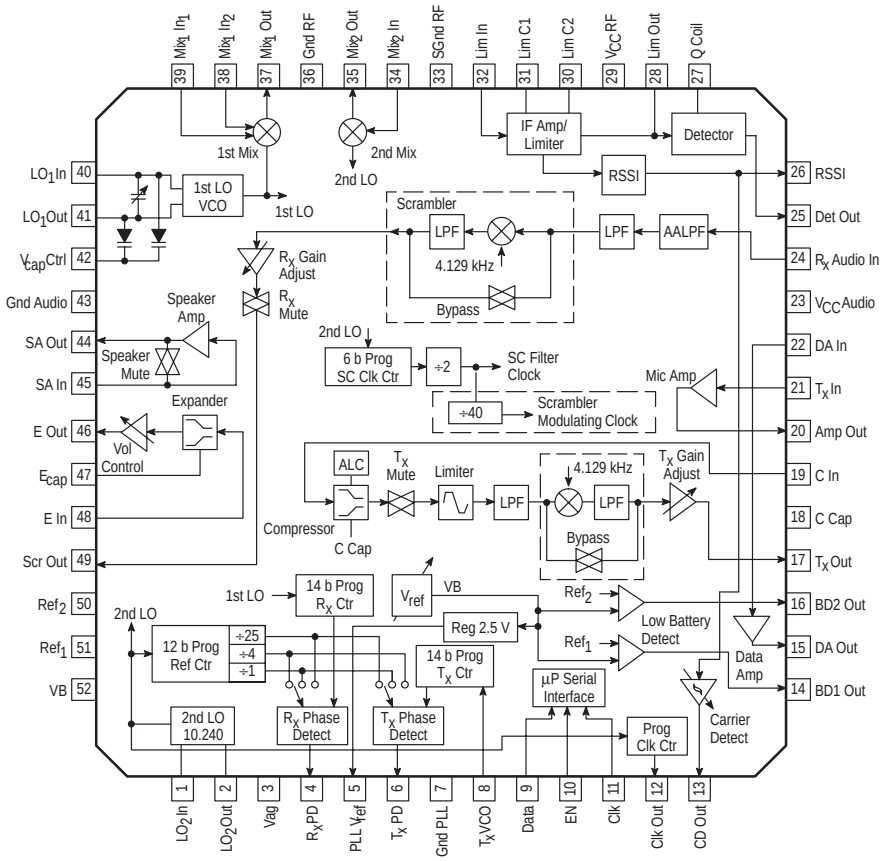


NOTE:
[ ] = MC13110A Only

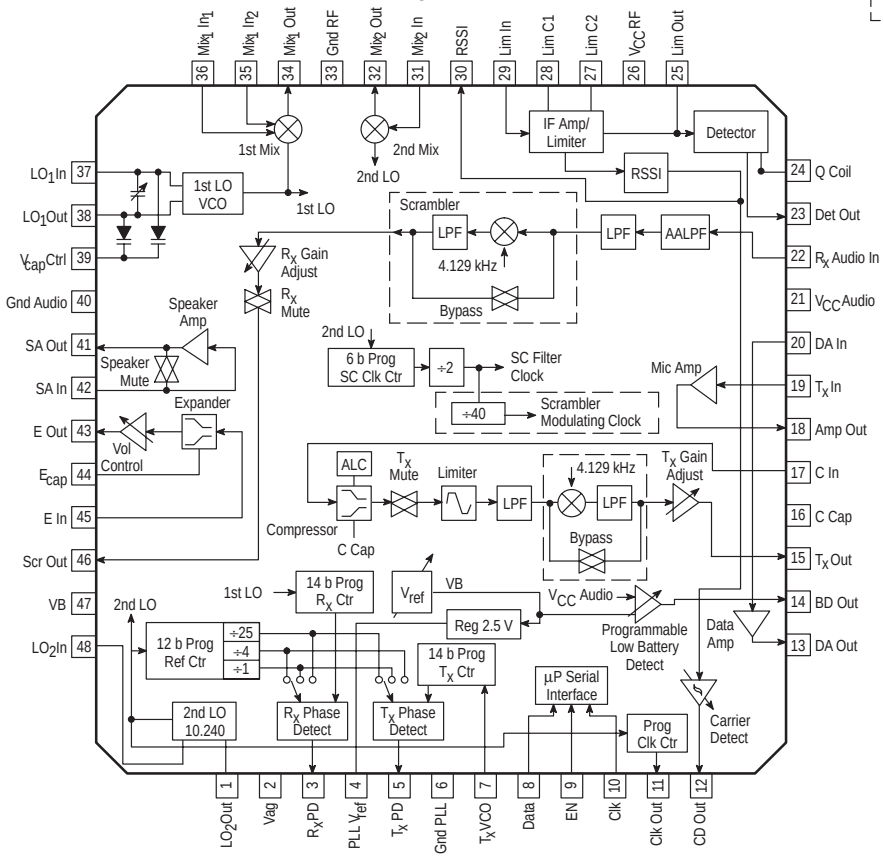
This device contains 8262 active transistors.

PIN CONNECTIONS

QFP–52



LQFP–48



NOTE:
[ ] = MC13110A Only

MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 6.0	Vdc
Junction Temperature	T_J	–65 to 150	°C
Maximum Power Dissipation, T_A = 25°C	P_D	70	mW

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Functional operation should be restricted to the limits in the Recommended Operating Conditions and Electrical Characteristics tables or Pin Descriptions section.
3. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.6	5.5	Vdc
Operating Ambient Temperature	T_A	–40	–	85	°C
Input Voltage Low (Data, Clk, EN)	V_{IL}	–	–	0.3	V
Input Voltage High (Data, Clk, EN)	V_{IH}	PLL V_{ref} – 0.3	–	–	V
Bandgap Reference Voltage	V_B	–	1.5	–	V

NOTE: 4. All limits are not necessarily functional concurrently.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, T_A = 25°C, unless otherwise specified, IP3 = 0; Test Circuit Figure 1.)

Characteristic	Symbol	Figure	Min	Typ	Max	Unit
Static Current		1				
Active Mode	ACT I_{CC}		5.5	8.5	10.5	mA
Receive Mode	R_X I_{CC}		3.1	4.1	5.3	mA
Standby Mode	STD I_{CC}		–	465	560	µA
Inactive Mode	INACT I_{CC}		–	15	30	µA
Current Increase When IP3 = 1 (Active and Receive Modes)	I_{IP3}	1	–	1.4	1.8	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_x Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
FM RECEIVER (f_{RF} = 46.77 MHz [USA Ch 21], f_{dev} = ±3.0 kHz, f_{mod} = 1.0 kHz, $V_{cap\ ctrl}$ = 1.2 V)								
Input Sensitivity (for 12 dB SINAD at Det Out Using C–Message Weighting Filter) 50 Ω Termination, Generator Referred	68, 69	Mix_1 In_1/In_2	Det Out	V_{SIN}	– –	2.2 –100	– –	µVrms dBm
Single–Ended, Matched Input, Generator Referred					– –	0.4 –115	– –	
Differential, Matched Input, Generator Referred					– –	0.4 –115	– –	
First and Second Mixer Voltage Gain Total (V_{in} = 1.0 mVrms, with CF_1 and CF_2 Load)	1	Mix_1 In_1 or In_2	Mix_2 Out	MX_{gainT}	24	29	–	dB
Isolation of First Mixer Output and Second Mixer Input (V_{in} = 1.0 mVrms, with CFI Removed)	–	Mix_1 In_1 or In_2	Mix_2 In	Mix–Iso	–	60	–	dB
Total Harmonic Distortion (V_{in} = 3.16 mVrms)	1	Mix_1 In_1 or In_2	Det Out	THD	–	1.4	2.0	%
Recovered Audio (V_{in} = 3.16 mVrms)	1	Mix_1 In_1 or In_2	Det Out	AFO	80	112	150	mVrms
AM Rejection Ratio (V_{in} = 3.16 mVrms, 30% AM, @ 1.0 kHz)	1	Mix_1 In_1 or In_2	Det Out	AMR	30	48	–	dB
Signal to Noise Ratio (V_{in} = 3.16 mVrms, No Modulation)	–	Mix_1 In_1 or In_2	Det Out	SNR	–	48	–	dB
FIRST MIXER (No Modulation, f_{in} = USA Ch21, 46.77 MHz, 50 Ω Termination at Inputs)								
Input Impedance Single–Ended	16	–	Mix_1 In_1 or In_2	R_{PS1} C_{PS1}	– –	1.6 3.7	– –	kΩ pF
Differential	16		Mix_1 In_1/In_2	R_{PD1} C_{PD1}	– –	1.6 1.8	– –	
Output Impedance	14	–	Mix_1 Out	R_{P1} Out C_{P1} Out	– –	300 3.7	– –	Ω pF
Voltage Conversion Gain (V_{in} = 1.0 mVrms, with CF_1 Filter as Load)	17, 18	Mix_1 In_1 or In_2	Mix_1 Out	MX_{gain1}	–	12	–	dB
1.0 dB Voltage Compression Level (Input Referred) IP3 Bit Set to 0	19, 21	Mix_1 In_1 or In_2	Mix_1 Out	V_O Mix_1 1 dB	– –	20 –21	– –	mVrms dBm
IP3 Bit Set to 1	20, 21				– –	56 –12	– –	
Third Order Intercept (Input Referred) [Note 5] IP3 Bit Set to 0	19, 21	Mix_1 In_1 or In_2	Mix_1 Out	TOI_{mix1}	– –	64 –11	– –	mVrms dBm
IP3 Bit Set to 1	20, 21				– –	178 –2.0	– –	
–3.0 dB IF Bandwidth	22	Mix_1 In_1 or In_2	Mix_1 Out	Mix_1 BW	–	13	–	MHz

NOTE: 5. Third order intercept calculated for input levels 10 dB below 1.0 dB compression point.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
SECOND MIXER (No Modulation, f_{in} = 10.7 MHz, 50 Ω Termination at Inputs)								
Input Impedance	24	Mix_2 In	Mix_2 In	R_{P2} In C_{P2} In	– –	2.8 3.6	– –	kΩ pF
Output Impedance	24	–	Mix_2 Out	R_{P2} Out C_{P2} Out	– –	1.5 6.1	– –	kΩ pF
Voltage Conversion Gain (V_{in} = 1.0 mVrms, with CF_2 Filter as Load)	26, 27	Mix_2 In	Mix_2 Out	MX_{gain2}	–	20	–	dB
1.0 dB Voltage Compression Level (Input Referred) IP3 Bit Set 0 IP3 Bit Set 1	28, 30 29, 30	Mix_2 In	Mix_2 Out	V_O Mix_2 1 dB	– – – –	32 –17 45 –14	– – – –	mVrms dBm
Third Order Intercept (Input Referred) [Note 6] IP3 Bit Set 0 IP3 Bit Set 1	28, 30 29, 30	Mix_2 In	Mix_2 Out	TOI_{mix2}	– – – –	136 –4.3 158 –3.0	– – – –	mVrms dBm
–3.0 dB IF Bandwidth	31	Mix_2 In	Mix_2 Out	Mix_2 BW	–	2.5	–	MHz
LIMITER/DEMODULATOR (f_{in} = 455 kHz, f_{dev} = ±3.0 kHz, f_{mod} = 1.0 kHz)								
Input Impedance	49	Lim In	Lim In	R_{PLim} C_{PLim}	– –	1.5 16	– –	kΩ pF
Detector Output Impedance	–	–	Det Out	R_O	–	1.1	–	kΩ
IF –3.0 dB Limiting Sensitivity	1	Lim In	Det Out	IF Sens	–	71	100	μVrms
Demodulator Bandwidth	–	Lim In	Det Out	BW	–	20	–	kHz
RSSI/CARRIER DETECT (No Modulation)								
RSSI Output Dynamic Range	56	Mix_1 In	RSSI	RSSI	–	80	–	dB
DC Voltage Range	56	Mix_1 In	RSSI	DC RSSI	–	0.2 to 1.5	–	Vdc
Carrier Detect Threshold CD Threshold Adjust = (10100) (Threshold Relative to Mix_1 In Level)	57	Mix_1 In	CD Out	V_T	–	15	–	μVrms
Hysteresis, CD = (10100) (Threshold Relative to Mix_1 In Level)	57	Mix1 In	CD Out	Hys	–	2.0	–	dB
Output High Voltage CD = (00000), RSSI = 0.2 V	1	RSSI	CD Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage CD = (11111), RSSI = 0.9 V	1	RSSI	CD Out	V_{OL}	–	0.02	0.4	V
Carrier Detect Threshold Adjustment Range (Programmable through MPU Interface)	125	–	–	V_T Range	–	–20 to 11	–	dB
Carrier Detect Threshold – Number of Programmable Levels	125	–	–	V_{Tn}	–	32	–	–

NOTE: 6. Third order intercept calculated for input levels 10 dB below 1.0 dB compression point.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
R_X AUDIO PATH (f_{in} = 1.0 kHz, Active Mode, scrambler bypassed)								
Absolute Gain (V_{in} = –20 dBV)	1, 72	R_X Audio In	SA Out	G	–4.0	0	4.0	dB
Gain Tracking (Referenced to E Out for V_{in} = –20 dBV) V_{in} = –30 dBV V_{in} = –40 dBV	1, 76	E In	E Out	G_t	 –21 –42	 –20 –40	 –19 –38	dB
Total Harmonic Distortion (V_{in} = –20 dBV)	1, 76	R_X Audio In	SA Out	THD	–	0.7	1.0	%
Maximum Input Voltage (V_{CC} = 2.7 V)	76	R_X Audio In	–	–	–	–11.5	–	dBV
Maximum Output Voltage (Increase input voltage until output voltage THD = 5.0%, then measure output voltage)	1	E In	E Out	V_{Omax}	–2.0	0	–	dBV
Input Impedance	–	R_X Audio In E In	–	Z_{in}	– –	600 7.5	– –	kΩ
Attack Time E_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	–	E In	E Out	t_a	–	3.0	–	ms
Release Time E_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	–	E In	E Out	t_r	–	13.5	–	ms
Compressor to Expander Crosstalk V_{in} = –10 dBV, $V_{(E\ In)}$ = AC Gnd	1	C In	E Out	C_T	–	–90	–70	dB
R_X Muting (Δ Gain) V_{in} = –20 dBV, R_X Gain Adj = (01111)	1	R_X Audio In	E Out	M_e	–	–84	–60	dB
R_X High Frequency Corner R_X Path, V R_X Audio In = –20 dBV	1	R_X Audio In	Scr Out	R_X f_{ch}	3.779	3.879	3.979	kHz
Low Pass Filter Passband Ripple (V_{in} = –20 dBV)	1, 73	R_X Audio In	Scr Out	Ripple	–	0.4	0.6	dB
R_X Gain Adjust Range (Programmable through MPU Interface)	124	R_X Audio In	Scr Out	R_X Range	–	–9.0 to 10	–	dB
R_X Gain Adjust Steps – Number of Programmable Levels	124	R_X Audio In	Scr Out	R_X n	–	20	–	dB
Audio Path Noise, C–Message Weighting (Input AC–Grounded)	70	R_X Audio In	Scr Out E Out SA Out	EN	– –	–85 <–95 <–95	– –	dBV
Volume Control Adjust Range	122	E In	E Out	V_{cr} Range	–	–14 to 16	–	dB
Volume Control – Number of Programmable Levels	122	E In	E Out	V_{cn}	–	16	–	–
SPEAKER AMP/SP MUTE (Active Mode)								
Maximum Output Swing R_L = No Load, V_{in} = 3.4 Vpp R_L = 130 Ω, V_{in} = 2.8 Vpp R_L = 620 Ω, V_{in} = 4.0 Vpp	1, 79	SA In	SA Out	V_{Omax}	 2.8 2.0 –	 3.2 2.6 3.4	 – – –	Vpp
Speaker Amp Muting V_{in} = –20 dBV, R_L = 130 Ω	1	SA In	SA Out	M_{sp}	–	–92	–60	dB

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
DATA AMP COMPARATOR								
Hysteresis	1	DA In	DA Out	Hys	30	42	50	mV
Threshold Voltage	–	DA In	DA Out	V_T	–	V_{CC} – 0.7	–	V
Input Impedance	1	–	DA In	Z_I	200	250	280	kΩ
Output Impedance	–	–	DA Out	Z_O	–	100	–	kΩ
Output High Voltage V_{in} = V_{CC} – 1.0 V, I_{OH} = 0 mA	1	DA In	DA Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage V_{in} = V_{CC} – 0.4 V, I_{OL} = 0 mA	1	DA In	DA Out	V_{OL}	–	0.1	0.4	V
Maximum Frequency	–	DA In	DA Out	F_{max}	–	10	–	kHz
MIC AMP (f_{in} = 1.0 kHz, External resistors set to gain of 1, Active Mode)								
Open Loop Gain	–	T_X In	Amp Out	AVOL	–	100,000	–	V/V
Gain Bandwidth	–	T_X In	Amp Out	GBW	–	100	–	kHz
Maximum Output Swing (R_L = 10 kΩ)	–	T_X In	Amp Out	V_{Omax}	–	3.2	–	Vpp
T_X AUDIO PATH (f_{in} = 1.0 kHz, T_X Gain Adj = (01111); ALC, Limiter, and Mutes Disabled; Active Mode, scrambler bypassed)								
Absolute Gain (V_{in} = –10 dBV)	1, 83	T_X In	T_X Out	G	–4.0	0	4.0	dB
Gain Tracking (Referenced to T_X Out for V_{in} = –10 dBV) V_{in} = –30 dBV V_{in} = –40 dBV	1, 87	T_X In	T_X Out	G_t	 –11 –17	 –10 –15	 –9.0 –13	dB
Total Harmonic Distortion (V_{in} = –10 dBV)	1, 87	T_X In	T_X Out	THD	–	0.8	1.8	%
Maximum Output Voltage (Increase input voltage until output voltage THD = 5.0%, then measure output voltage. T_X Gain Adjust = 8 dB)	1	T_X In	T_X Out	V_{Omax}	–2.0	0	–	dBV
Input Impedance	–	–	C In	Z_{in}	–	10	–	kΩ
Attack Time (C_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B))	–	C In	T_X Out	t_a	–	3.0	–	ms
Release Time (C_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B))	–	C In	T_X Out	t_r	–	13.5	–	ms
Expander to Compressor Crosstalk (V_{in} = –20 dBV, Speaker Amp No Load, $V_{(C\ In)}$ = AC Gnd)	1	E In	T_X Out	C_T	–	–60	–40	dB
T_X Muting (V_{in} – 10 dBV)	1	T_X In	T_X Out	M_C	–	–88	–60	dB
ALC Output Level (ALC enabled) V_{in} = –10 dBV V_{in} = –2.5 dBV	1, 87, 90	T_X In	T_X Out	ALC_{out}	 –15 –13	 –13 –11	 –8.0 –6.0	dBV
ALC Slope (ALC enabled) V_{in} = –10 dBv V_{in} = –2.5 dBv	1	T_X In	T_X Out	Slope	0.1	0.25	0.4	dB/dB
ALC Input Dynamic Range	–	C In	T_X Out	DR	–	–16 to –2.5	–	dBV
Limiter Output Level (V_{in} = –2.5 dBV, Limiter enabled)	1	T_X In	T_X Out	V_{lim}	–10	–8.0	–	dBV
T_X High Frequency Corner [Note 7] (VT_X In = –10 dBV, Mic Amp = Unity Gain)	1	T_X In	T_X Out	T_X f_c	3.6	3.7	3.8	kHz

NOTE: 7. The filter specification is based on a 10.24 MHz 2nd LO, and a switched–capacitor (SC) filter counter divider ratio of 31. If other 2nd LO frequencies and/or SC filter counter divider ratios are used, the filter corner frequency will be proportional to the resulting SC filter clock frequency.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
T_X AUDIO PATH (f_{in} = 1.0 kHz, T_X Gain Adj = (01111); ALC, Limiter, and Mutes Disabled; Active Mode, scrambler bypassed)								
Low Pass Filter Passband Ripple (V_{in} = –10 dBV)	1, 84	T_X In	T_X Out	Ripple	–	0.7	1.2	dB
Maximum Compressor Gain (V_{in} = –70 dBV)	–	C In	T_X Out	AV_{max}	–	23	–	dB
T_X Gain Adjust Range (Programmable through MPU Interface)	124	C In	T_X Out	T_X Range	–	–9.0 to 10	–	dB
T_X Gain Adjust Steps – Number of Programmable Levels	124	C In	T_X Out	T_X n	–	20	–	–
R_X AND T_X SCRAMBLER (2nd LO = 10.24 MHz, T_X Gain Adj = (01111), R_X Gain Adj = (01111), Volume Control = (0 dB Default Levels), SCF Clock Divider = 31. Total is divide by 62 for SCF clock frequency of 165.16 kHz)								
R_X High Frequency Corner (Note 8) R_X Path, f = 479 Hz, V R_X Audio In = –20 dBV	–	R_X Audio In	Scr Out	R_X f_{ch}	3.55	3.65	3.75	kHz
T_X High Frequency Corner (Note 8) T_X Path, f = 300 Hz, V T_X In = –10 dBV, Mic Amp = Unity Gain	–	T_X In	T_X Out	T_X f_{ch}	3.829	3.879	3.929	kHz
Absolute Gain R_X: V_{in} = –20 dBV T_X: V_{in} = –10 dBV, Limiter disabled	 – –	 R_X Audio In T_X In	 E Out T_X Out	AV	 –4.0 –4.0	 0.4 –1.0	 4.0 4.0	dB
Pass Band Ripple R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In, f_{in} = low corner frequency to high corner frequency	–	C In	E Out	Ripple	–	1.9	2.5	dB
Scrambler Modulation Frequency R_X: 100 mV (–20 dBV) T_X: 316 mV (–10 dBV)	 – –	 R_X Audio In C In	 E Out T_X Out	f_{mod}	4.119	4.129	4.139	kHz
Group Delay R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In, f_{in} = 1.0 kHz	–	C In	E Out	GD	–	1.0	–	ms
f_{in} = low corner frequency to high corner frequency	–	C In	E Out	GD	–	4.0	–	
Carrier Breakthrough R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In	–	C In	E Out	CBT	–	–60	–	dB
Baseband Breakthrough R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In, f_{in} = 1.0 kHz, f_{meas} = 3.192 kHz	–	C In	E Out	BBT	–	–50	–	dB
LOW BATTERY DETECT								
Average Threshold Voltage Before Electronic Adjustment (V_{ref}_Adj = (0111))	1, 130	Ref_1 Ref_2	BD_1 Out BD_2 Out	VT_i	1.38	1.48	1.58	V
Average Threshold Voltage After Electronic Adjustment (V_{ref}_Adj = (adjusted value))	1	Ref_1 Ref_2	BD_1 Out BD_2 Out	VT_f	1.475	1.5	1.525	V
Hysteresis	–	Ref_1 Ref_2	BD_1 Out BD_2 Out	Hys	–	4.0	–	mV
Input Current (V_{in} = 1.0 and 2.0 V)	1	–	Ref_1 Ref_2	I_{in}	–50	–	50	nA
Output High Voltage (V_{in} = 2.0 V)	1	Ref_1 Ref_2	BD_1 Out BD_2 Out	V_{OH}	V_{CC} – 0.1	3.6	–	V

NOTE: 8. The filter specification is based on a 10.24 MHz 2nd LO, and a switch–capacitor (SC) filter counter divider ratio of 31. If other 2nd LO frequencies and/or SC filter counter divider ratios are used, the filter corner frequency will be proportional to the resulting SC filter clock frequency.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
LOW BATTERY DETECT								
Output Low Voltage (V_{in} = 1.0 V)	1	Ref_1 Ref_2	BD_1 Out BD_2 Out	V_{OL}	–	0.2	0.4	V
BATTERY DETECT INTERNAL THRESHOLD								
After Electronic Adjustment of V_B Voltage	1, 127	V_{CC} Audio	BD_2 Out					V
BD Select = (111)				IBS_7	3.381	3.455	3.529	
BD Select = (110)				IBS_6	3.298	3.370	3.442	
BD Select = (101)				IBS_5	3.217	3.287	3.357	
BD Select = (100)				IBS_4	3.134	3.202	3.270	
BD Select = (011)				IBS_3	2.970	3.034	3.098	
BD Select = (010)				IBS_2	2.886	2.948	3.010	
BD Select = (001)				IBS_1	2.802	2.862	2.922	
PLL PHASE DETECTOR								
Output Source Current (V_{PD} = Gnd + 0.5 V to PLL V_{ref} – 0.5 V)	–	–	R_X PD T_X PD	I_{OH}	–	1.0	–	mA
Output Sink Current (V_{PD} = Gnd + 0.5 V to PLL V_{ref} – 0.5 V)	–	–	R_X PD T_X PD	I_{OL}	–	1.0	–	mA
PLL LOOP CHARACTERISTICS								
Maximum 2nd LO Frequency (No Crystal)	–	LO_2 In	–	f_{2ext}	–	12	–	MHz
Maximum 2nd LO Frequency (With Crystal)	–	–	LO_2 In LO_2 Out	f_{2ext}	–	12	–	MHz
Maximum T_X VCO (Input Frequency), V_{in} = 200 mVpp	–	–	T_X VCO	f_{txmax}	–	80	–	MHz
PLL VOLTAGE REGULATOR								
Regulated Output Level (I_L = 0 mA, after V_{ref} Adjustment)	1	–	PLL V_{ref}	V_O	2.4	2.5	2.6	V
Line Regulation (I_L = 0 mA, V_{CC} = 3.0 to 5.5 V)	1	V_{CC} Audio	PLL V_{ref}	V_{Reg}Line	–	11.8	40	mV
Load Regulation (I_L = 1.0 mA)	1	V_{CC} Audio	PLL V_{ref}	V_{Reg} Load	–20	–1.4	–	mV
MICROPROCESSOR SERIAL INTERFACE								
Input Current Low (V_{in} = 0.3 V, Standby Mode)	1	–	Data, Clk, EN	I_{IL}	–5.0	0.4	–	µA
Input Current High (V_{in} = 3.3 V, Standby Mode)	1	–	Data, Clk, EN	I_{IH}	–	1.6	5.0	µA
Hysteresis Voltage	–	–	Data, Clk, EN	V_{hys}	–	1.0	–	V
Maximum Clock Frequency	–	Data, EN, Clk	–	–	–	2.0	–	MHz
Input Capacitance	–	Data, Clk, EN	–	C_{in}	–	8.0	–	pF
EN to Clk Setup Time	106	–	EN, Clk	t_{suEC}	–	200	–	ns
Data to Clk Setup Time	105	–	Data, Clk	t_{suDC}	–	100	–	ns
Hold Time	105	–	Data, Clk	t_h	–	90	–	ns
Recovery Time	106	–	EN, Clk	t_{rec}	–	90	–	ns
Input Pulse Width	–	–	EN, Clk	t_w	–	100	–	ns
MPU Interface Power–Up Delay (90% of PLL V_{ref} to Data,Clk, EN)	108	–	–	t_{puMPU}	–	100	–	µs

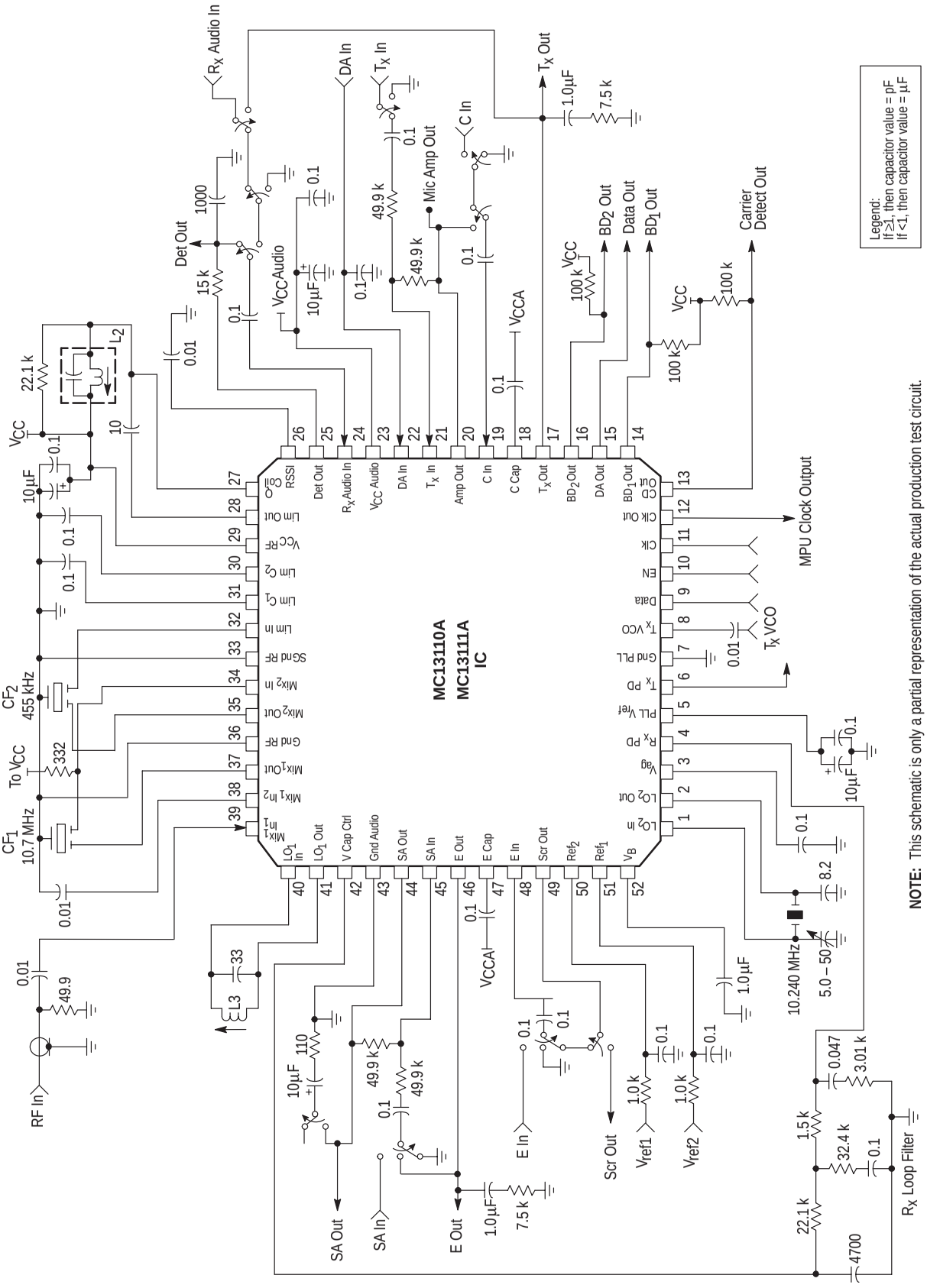
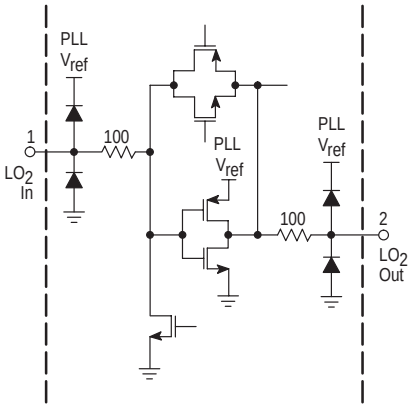
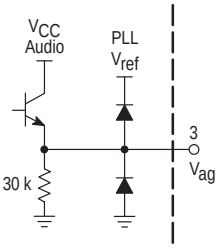
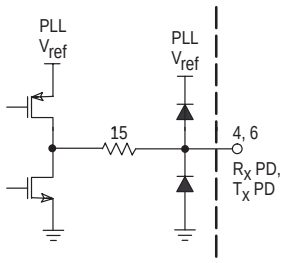
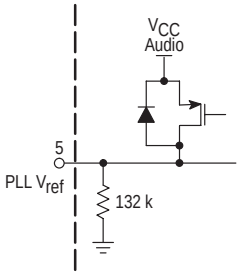
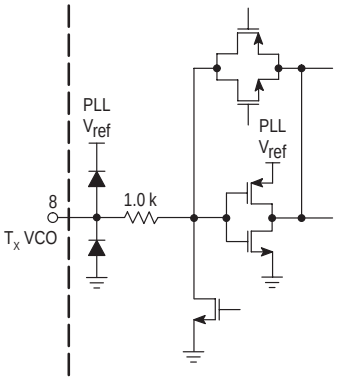


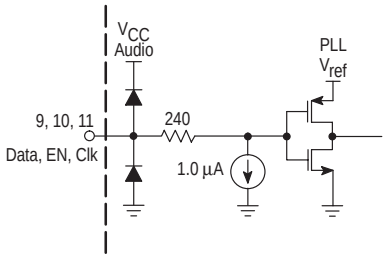
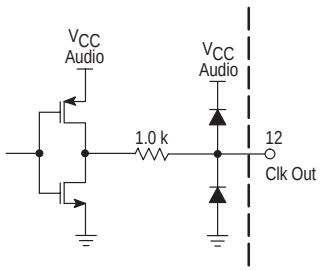
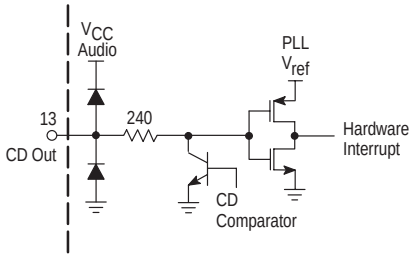
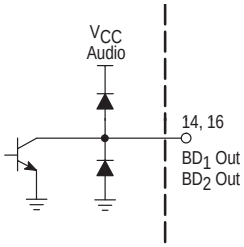
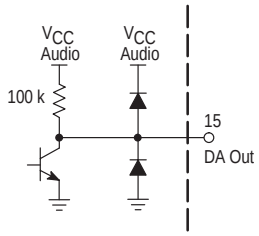
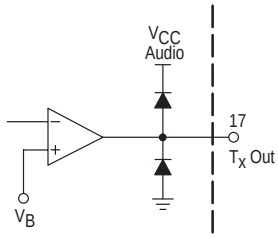
Figure 1. Production Test Circuit (52 Pin QFP)

NOTE: This schematic is only a partial representation of the actual production test circuit.

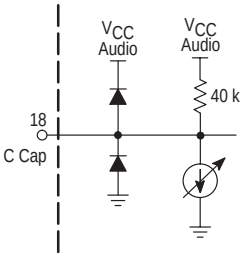
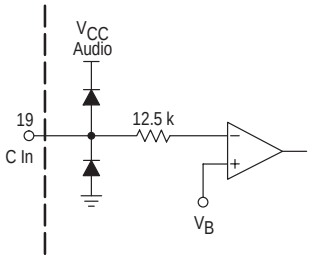
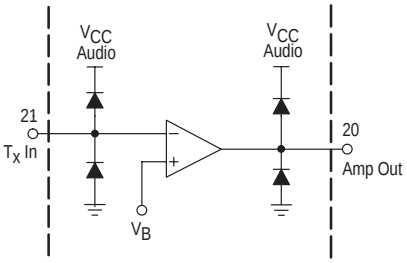
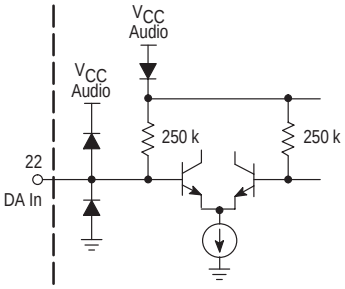
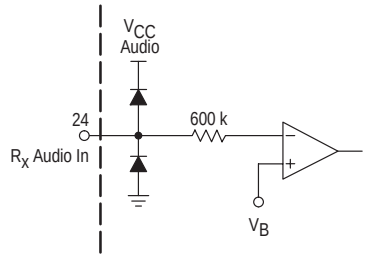
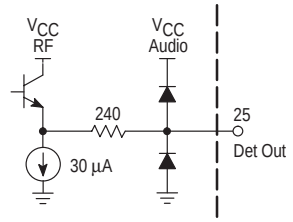
PIN FUNCTION DESCRIPTION

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
48 1	1 2	LO_2 In LO_2 Out		These pins form the PLL reference oscillator when connected to an external parallel–resonant crystal (10.24 MHz typical). The reference oscillator is also the second Local Oscillator (LO_2) for the RF receiver. "LO_2 In" may also serve as an input for an externally generated reference signal which is typically ac–coupled. When the IC is set to the inactive mode, LO_2 In is internally pulled low to disable the oscillator. The input capacitance to ground at each pin (LO_2 In/ LO_2 Out) is 3.0 pF.
2	3	V_{ag}		V_{ag} is the internal reference voltage for the switched capacitor filter section. This pin must be decoupled with a 0.1 μF capacitor.
3	4	R_X PD (Output)		This pin is a tri–state voltage output of the R_X and T_X Phase Detector. It is either "high", "low", or "high impedance," depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external R_X and T_X PLL loop filters. R_X and T_X PD outputs can sink or source 1.0 mA.
5	6	T_X PD (Output)		
4	5	PLL V_{ref}		PLL V_{ref} is a PLL voltage regulator output pin. An internal voltage regulator provides a stable power supply voltage for the R_X and T_X PLL's and can also be used as a regulated supply voltage for other IC's. It can source up to 1.0 mA externally. Proper supply filtering is a must on this pin. PLL V_{ref} is pulled up to V_{CC} audio for the standby and inactive modes (Note 1).
6	7	Gnd PLL		Ground pin for digital PLL section of IC.
7	8	T_X VCO (Input)		T_X VCO is the transmit divide counter input which is driven by an ac–coupled external transmit loop VCO. The minimum signal level is 200 mVpp @ 60.0 MHz. This pin also functions as the test mode input for the counter tests.

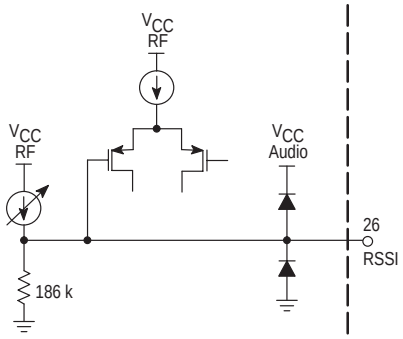
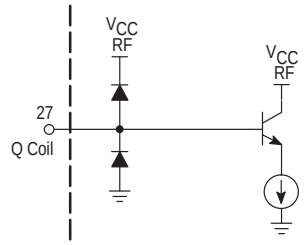
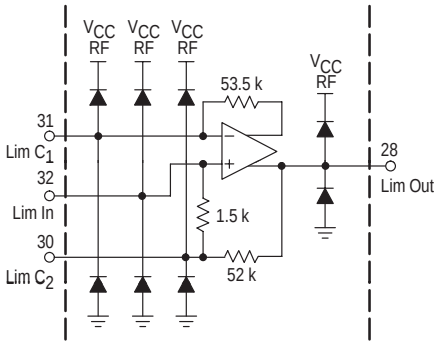
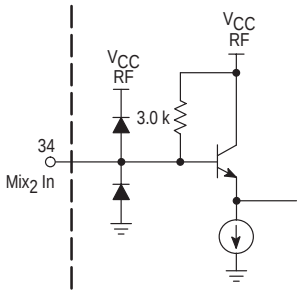
PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
8 9 10	9 10 11	Data EN Clk (Input)		Microprocessor serial interface input pins are for programming various counters and control functions. The switching thresholds are referenced to PLL V_{ref} and Gnd PLL. The inputs operate up to V_{CC}. These pins have 1.0 µA internal pull–down currents.
11	12	Clk Out (Output)		The microprocessor clock output is derived from the 2nd LO crystal oscillator and a programmable divider with divide ratios of 2 to 312.5. It can be used to drive a microprocessor and thereby reduce the number of crystals required in the system design. The driver has an internal resistor in series with the output which can be combined with an external capacitor to form a low pass filter to reduce radiated noise on the PCB. This output also functions as the output for the counter test modes. The Clk Out can be disabled via the MPU interface.
12	13	CD Out (I/O)		Dual function pin; 1) Carrier detect output (open collector with external 100 kΩ pull–up resistor. 2) Hardware interrupt input which can be used to “wake–up” from the Inactive Mode.
–	14	BD_1 Out		Low battery detect output #1 is an open collector with external pull–up resistor.
14	16	BD_2 Out (Output)		Low battery detect output #2 is an open collector with external pull–up resistor.
13	15	DA Out (Output)		Data amplifier output (open collector with internal 100 kΩ pull–up resistor).
15	17	T_X Out (Output)		T_X Out is the T_X path audio output. Internally this pin has a low–pass filter circuitry with –3 dB bandwidth of 4.0 kHz. T_X gain and mute are programmable through the MPU interface. This pin is sensitive to load capacitance.

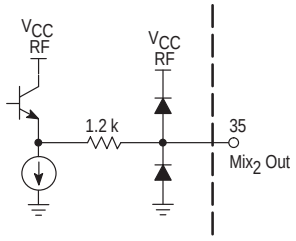
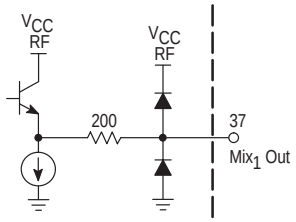
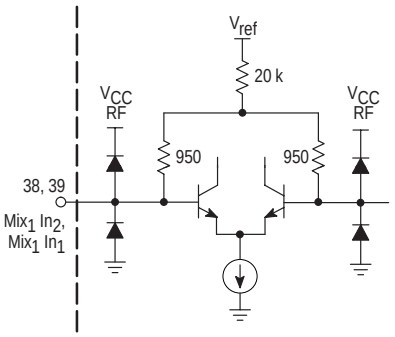
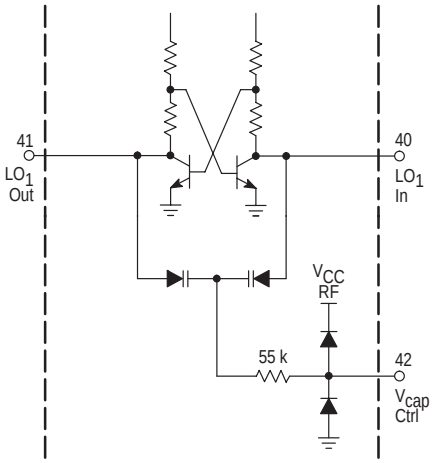
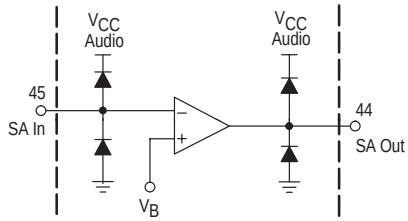
PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
16	18	C Cap		C Cap is the compressor rectifier filter capacitor pin. It is recommended that an external filter capacitor to V_{CC} audio be used. A practical capacitor range is 0.1 to 1.0 µF. 0.47 µF is the recommended value.
17	19	C In (Input)		C In is the compressor input. This pin is internally biased and has an input impedance of 12.5 k. C In must be ac–coupled.
18	20	Amp Out (Output)		Microphone amplifier output. The gain is set with external resistors. The feedback resistor should be less than 200 kΩ.
19	21	T_X In (Input)		T_X In is the T_X path input to the microphone amplifier (Mic Amp). An external resistor is connected to this pin to set the Mic Amp gain and input impedance. T_X In must be ac–coupled, too.
20	22	DA In (Input)		The data amplifier input (DA In) resistance is 250 kΩ and must be ac–coupled. Hysteresis is internally provided.
21	23	V_{CC} Audio		V_{CC} audio is the supply for the audio section. It is necessary to adequately filter this pin.
22	24	R_X Audio In (Input)		The R_X audio input resistance is 600 kΩ and must be ac–coupled.
23	25	Det Out (Output)		Det Out is the audio output from the FM detector. This pin is dc–coupled from the FM detector and has an output impedance of 1100 Ω.

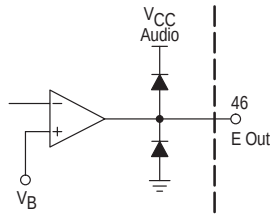
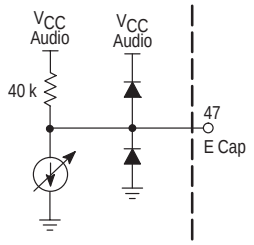
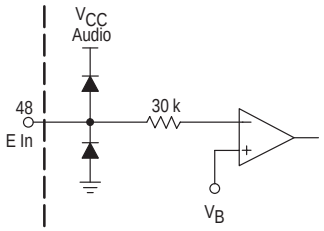
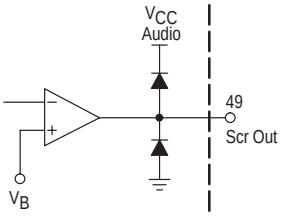
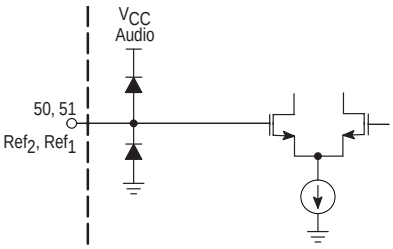
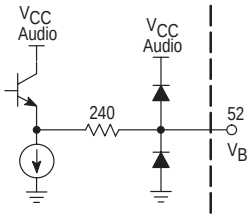
PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
30	26	RSSI		RSSI is the receive signal strength indicator. This pin must be filtered through a capacitor to ground. The capacitance value range should be 0.01 to 0.1 µF. This is also the input to the Carrier Detect comparator. An external R to ground shifts the RSSI voltage.
24	27	Q Coil		A quad coil or ceramic discriminator connects this pin as part of the FM demodulator circuit. DC–couple this pin to V_{CC} RF through the quad coil or the external resistor.
26	29	V_{CC} RF		V_{CC} supply for RF receiver section (1st LO, mixer, limiter, demodulator). Proper supply filtering is needed on this pin too.
25	28	Lim Out		A quad coil or ceramic discriminator are connected to these pins as part of the FM demodulator circuit. A coupling capacitor connects this pin to the quad coil or ceramic discriminator as part of the FM demodulator circuit. This pin can drive coupling capacitors up to 47 pF with no deterioration in performance.
27 28	30 31	Lim C_2 Lim C_1		IF amplifier/limiter capacitor pins. These decoupling capacitors should be 0.1 µF. They determine the IF limiter gain and low frequency bandwidth.
29	32	Lim In (Input)		Signal input for IF amplifier/limiter. Signals should be ac–coupled to this pin. The input impedance is 1.5 kΩ at 455 kHz.
–	33	SGnd RF		This pin is not connected internally but should be grounded to reduce potential coupling between pins.
31	34	Mix_2 In (Input)		Mix_2 In is the second mixer input. Signals are to be ac–coupled to this pin, which is biased internally to V_{CC} RF. The input impedance is 2.8 kΩ at 455 kHz. The input impedance can be reduced by connecting an external resistor to V_{CC} RF.

PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
32	35	Mix_2 Out (Output)		Mix_2 Out is the second mixer output. The second mixer has a 3 dB bandwidth of 2.5 MHz and an output impedance of 1.5 kΩ. The output current drive is 50 μA.
33	36	Gnd RF		Ground pin for RF section of the IC.
34	37	Mix_1 Out (Output)		The first mixer has a 3 dB IF bandwidth of 13 MHz and an output impedance of 300 Ω. The output current drive is 300 μA and can be programmed for 1.0 mA.
35	38	Mix_1 In_2 (Input)		Signals should be ac–coupled to this pin, which is biased internally to V_{CC} – 1.6 V. The single–ended and differential input impedance are about 1.6 and 1.8 kΩ at 46 MHz, respectively.
36	39	Mix_1 In_1 (Input)		
37 38	40 41	LO_1 In LO_1 Out		Tank Elements, an internal varactor and capacitor matrix for 1st LO multivibrator oscillator are connected to these pins. The oscillator is useable up to 80 MHz.
39	42	V_{cap} Ctrl		V_{cap} Ctrl is the 1st LO varactor control pin. The voltage at this pin is referenced to Gnd Audio and varies the capacitance between LO_1 In and LO_2 Out. An increase in voltage will decrease capacitance.
40	43	Gnd Audio		Ground for audio section of the IC.
41	44	SA Out (Output)		The speaker amplifier gain is set with an external feedback resistor. It should be less than 200 kΩ. The speaker amplifier can be muted through the MPU interface.
42	45	SA In (Input)		An external resistor is connected to the speaker amplifier input (SA In). This will set the gain and input impedance and must be ac–coupled.

PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
43	46	E Out (Output)		The output level of the expander output is determined by the volume control. Volume control is programmable through the MPU interface.
44	47	E Cap		E Cap is the expander rectifier filter capacitor pin. Connect an external filter capacitor between V_{CC} audio and E Cap. The recommended capacitance range is 0.1 to 1.0 μF. 0.47 μF is the suggested value.
45	48	E In (Input)		The expander input pin is internally biased and has input impedance of 30 kΩ.
46	49	Scr Out (Output)		Scr Out is the R_X audio output. An internal low pass filter has a –3 dB bandwidth of 4.0 kHz.
–	50	Ref_2		Reference voltage input for Low Battery Detect #2.
–	51	Ref_1		Reference voltage input for Low Battery Detect #1.
47	52	V_B		V_B is the internal half supply analog ground reference. This pin must be filtered with a capacitor to ground. A typical capacitor range of 0.5 to 10 μF is desired to reduce crosstalk and noise. It is important to keep this capacitor value equal to the PLL V_{ref} capacitor due to logic timing (Note 9).

NOTE: 9. A capacitor range of 0.5 to 10 μF is recommended. The capacitor value should be the same used on the V_B pin (Pin 52). An additional high quality parallel capacitor of 0.01 μF is essential to filter out spikes originating from the PLL logic circuitry.

The following text, graphics, tables and schematics are provided to the user as a source of valuable technical information about the Universal Cordless Telephone IC. This information originates from thorough evaluation of the device performance for the US and French applications. This data was obtained by using units from typical wafer lots. It is important to note that the forgoing data and information was from a limited number of units. By no means is the user to assume that the data following is a guaranteed parametric. Only the minimum and maximum limits identified in the electrical characteristics tables found earlier in this spec are guaranteed.

General Circuit Description

The MC13110A and MC13111A are a low power dual conversion narrowband FM receiver designed for applications up to 80 MHz carrier frequency. This device is primarily designated to be used for the 49 MHz cordless phone (CT–0), but has other applications such as low data rate narrowband data links and as a backend device for 900 MHz systems where baseband analog processing is required. This device contains a first and second mixer, limiter, demodulator, extended range receive signal strength (RSSI), receive and transmit baseband processing, dual programmable PLL, low battery detect, and serial interface for microprocessor control. The FM receiver can also be used with either a quadrature coil or ceramic resonator. Refer to the Pin Function Description table for the simplified internal circuit schematic and description of this device.

DC Current and Battery Detect

Figures 3 through 6 are the current consumption for Inactive, Standby, Receive, and Active modes versus supply voltages. Figures 7 and 8 show the typical behavior of current consumption in relation to temperature. The relationship of additional current draw due to IP3 bit set to <1> and supply voltage are shown in Figures 9 and 10.

For the Low Battery Detect, the user has the option to operate the IC in the programmable or non–programmable modes. Note that the 48 pin package can only be used in the programmable mode. Figure 127 describes this operation (refer to the Serial Interface section under Clock Divider Register).

In the programmable mode several different internal threshold levels are available (Figure 2). The bits are set through the SCF Clock Divider Register as shown in Figures 108 and 125. The reference for the internal divider network is V_{CC} Audio. The voltages on the internal divider network are compared to the Internal Reference Voltage, VB, generated by an internal source. Since the internal comparator used is non–inverting, a high at V_{CC} Audio will yield a high at the battery detect output, and vice versa for V_{CC} Audio set to a low level. For the 52 pin package option, the Ref 1 and Ref 2 pins need to be tied to V_{CC} when used in the programmable mode. It is essential to keep the external reference pins above Gnd to prevent any possible power–on reset to be activated.

When considering the non–programmable mode (bits set to <000>) for the 52 pin package, the Ref 1 and Ref 2 pins become the comparators reference. An internal switch is activated when the non–programmable mode is chosen connecting Ref 1 and Ref 2. Here, two external precision resistor dividers are used to set independent thresholds for two battery detect hysteresis comparators. The voltages on Ref 1 and Ref 2 are again compared to the internally generated 1.5 V reference voltage (VB).

The Low Battery Detect threshold tolerance can be improved by adjusting a trim–pot in the external resistor divider (user designed). The initial tolerance of the internal reference voltage (VB) is ±6.0%. Alternately, the tolerance of the internal reference voltage can be improved to ±1.5% through MPU serial interface programming (refer to the Serial Interface section, Figure 130). The internal reference can be measured directly at the “VB” pin. During final test of the telephone, the VB internal reference voltage is measured. Then, the internal reference voltage value is adjusted electronically through the MPU serial interface to achieve the desired accuracy level. The voltage reference register value should be stored in ROM during final test so that it can be reloaded each time the combo IC is powered up. The Low Battery Detect outputs are open collector. The battery detect levels will depend on the accuracy of the VB voltage. Figure 12 indicates that the VB voltage is fairly flat over temperature.

Figure 2. Internal Low Battery Detect Levels (with VB = 1.5 V)

Battery Detect Select	Ramping Up (V)	Ramping Down (V)	Average (V)	Hysteresis (mV)
0	–	–	–	–
1	2.867	2.861	2.864	4.0
2	2.953	2.947	2.950	6.0
3	3.039	3.031	3.035	8.0
4	3.207	3.199	3.204	8.0
5	3.291	3.285	3.288	6.0
6	3.375	3.367	3.371	8.0
7	3.461	3.453	3.457	8.0

NOTE: 10. Battery Detect Select 0 is the non–programmable operating mode.

DC CURRENT

Figure 3. Current versus Supply Voltage Inactive Mode

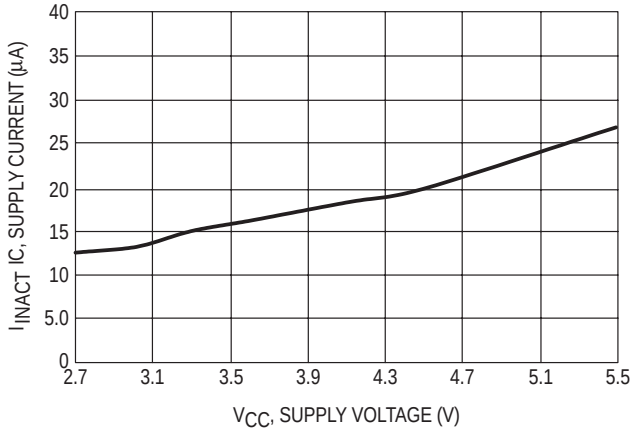


Figure 4. Current versus Supply Voltage Standby Mode, MCU Clock Output – On at 2.048 MHz

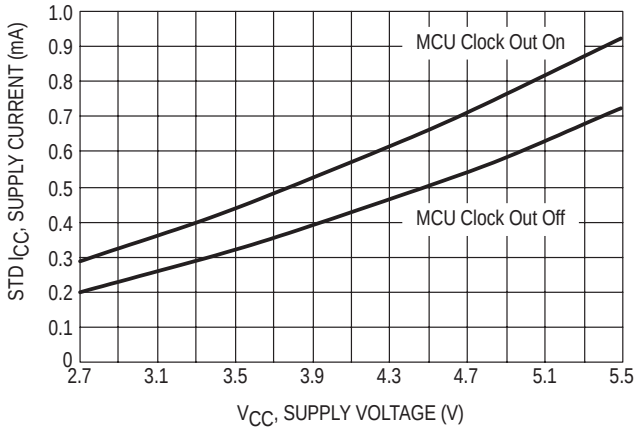


Figure 5. Current versus Supply Voltage Receive Mode

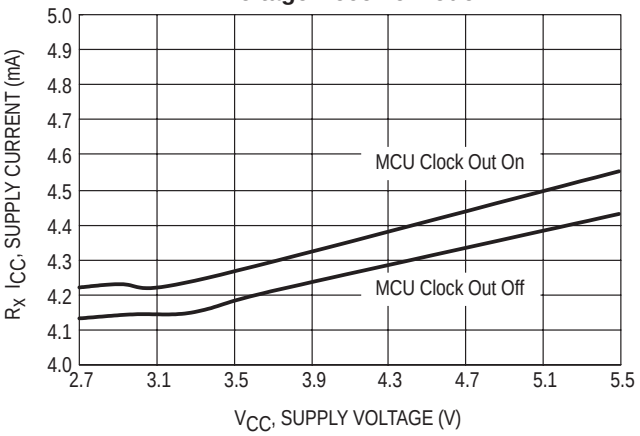


Figure 6. Current versus Supply Voltage Active Mode

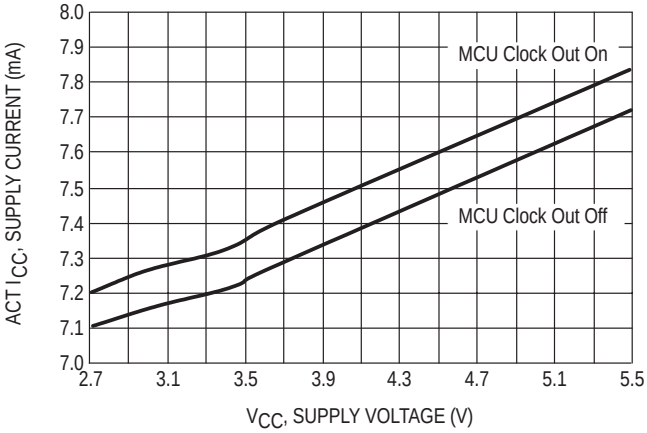


Figure 7. Current versus Temperature Normalized to 25°C

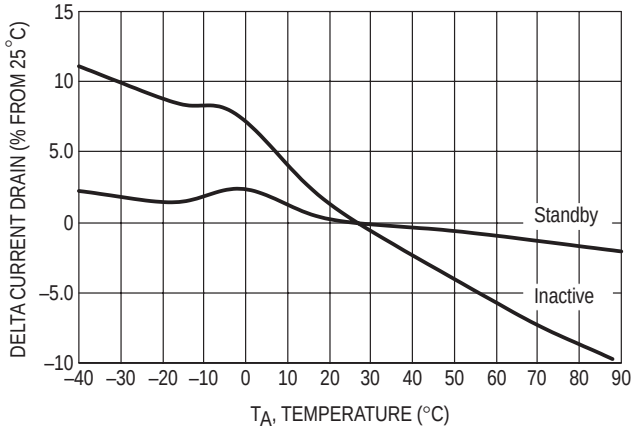
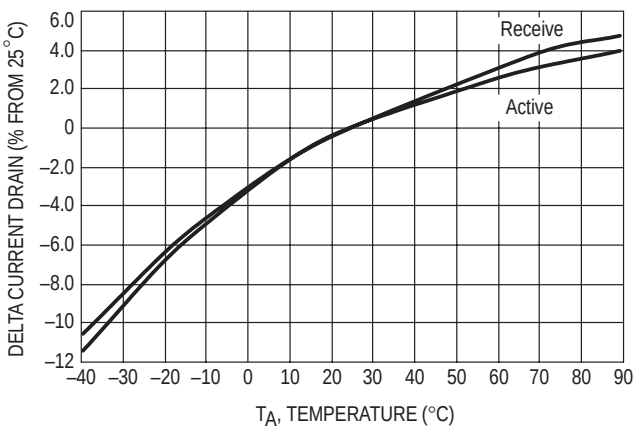


Figure 8. Current versus Temperature Normalized to 25°C



DC CURRENT

Figure 9. Additional Supply Current Consumption versus Supply Voltage, IP3 = <1>

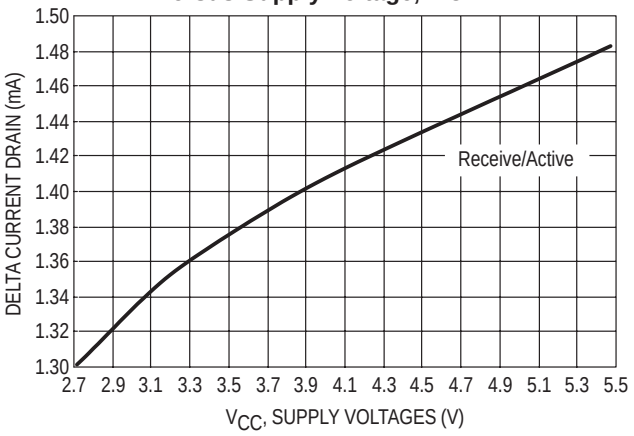


Figure 10. Additional IP3 Supply Current Consumption versus Temperature Normalized to 25°C

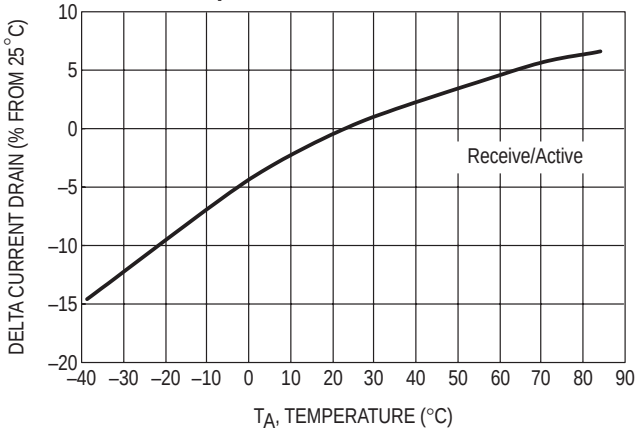


Figure 11. Current Standby Mode versus MCU Clock Output

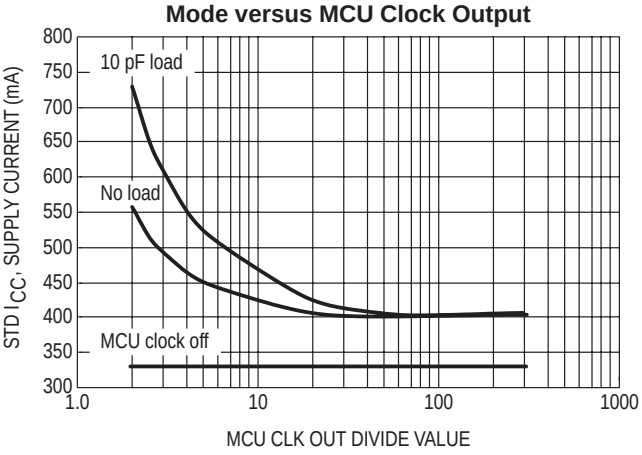
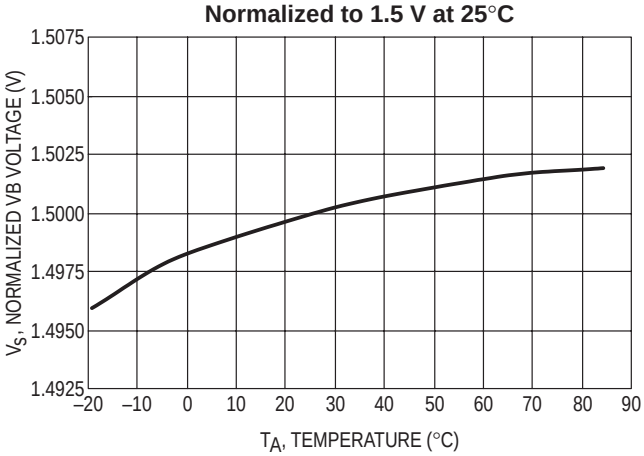


Figure 12. VB Voltage versus Temperature Normalized to 1.5 V at 25°C



FIRST AND SECOND MIXER

Mixer Description

The 1st and 2nd mixers are similar in design. Both are double balanced to suppress the LO and the input frequencies to give only the sum and difference frequencies at the mixer output. Typically the LO is suppressed better than –50 dB for the first mixer and better than –40 dB for the second mixer. The gain of the 1st mixer has a –3.0 dB corner at approximately 13 MHz and is used at a 10.7 MHz IF. It has an output impedance of 300 Ω and matches to a typical 10.7 MHz ceramic filter with a source and load impedance of 330 Ω. A series resistor may be used to raise the impedance for use with crystal filters. They typically have an input impedance much greater than 330 Ω.

First Mixer

Figures 17 through 20 show the first mixer transfer curves for the voltage conversion gain, output level, and intermodulation. Notice that there is approximately 10 dB linearity improvement when the “IP3 Increase” bit is set to <1>. The “IP3 Increase” bit is a programmable bit as shown in the Serial Programmable Interface section under the R_X Counter Latch Register. The IP3 = <1> option will increase the supply current demand by 1.3 mA.

Figure 13. First Mixer Input and Output Impedance Schematic

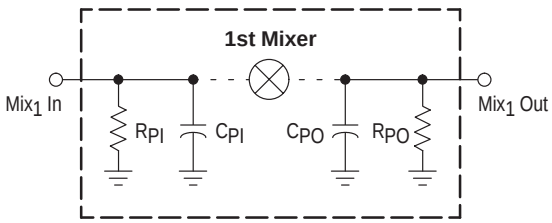


Figure 14. First Mixer Output Impedance

Unit	Output Impedance
B IP3 = <0> (Set Low)	304 Ω // 3.7 pF
B IP3 = <1> (Set High)	300 Ω // 4.0 pF

Figures 13, 14, and 16 represent the input and output impedance for the first mixer. Notice that the input single–ended and differential impedances are basically the same. The output impedance as described in Figure 14 will be used to match to a ceramic or crystal filter’s input impedance. A typical ceramic filter input impedance is 330 Ω while crystal filter input impedance is usually 1500 Ω. Exact impedance matching to ceramic filters are not critical, however, more attention needs to be given to the filter characteristics of a crystal filter. Crystal filters are much narrower. It is important to accurately match to these filters to guaranty a reasonable response.

To find the IF bandwidth response of the first mixer refer to Figure 22. The –3.0 dB bandwidth point is approximately 13 MHz. Figure 15 is a summary of the first mixer feedthrough parameters.

Figure 15. First Mixer Feedthrough Parameters

Parameter	(dBm)
1st LO Feedthrough @ Mix_1 In_1	–70.0
1st LO Feedthrough @ Mix_1 Out	–55.5
RF Feedthrough @ Mix_1 Out with –30 dBm	–61.0

Figure 16. First Mixer Input Impedance over Input Frequency

	US Center Channels		France Center Channels	
Unit	49 MHz	46 MHz	41 MHz	26 MHz
Single–Ended	1550 Ω // 3.7 pF	1560 Ω // 3.7 pF	1570 Ω // 3.8 pF	1650 Ω // 3.7 pF
Differential	1600 Ω // 1.8 pF	1610 Ω // 1.8 pF	1670 Ω // 1.8 pF	1710 Ω // 1.8 pF

NOTE: 11. Single–Ended data is from measured results. Differential data is from simulated results.

FIRST MIXER

Figure 17. First Mixer Voltage Conversion Gain, IP3_bit = 0

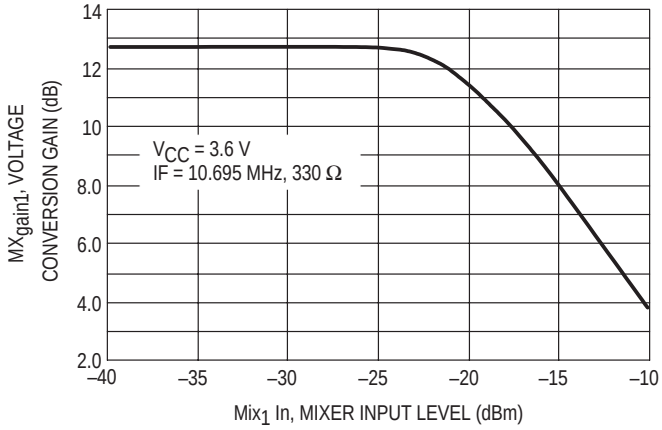


Figure 18. First Mixer Voltage Conversion Gain, IP3_bit = 1

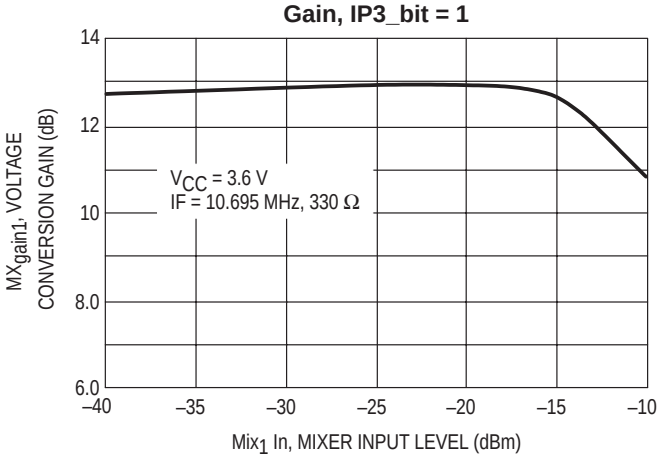


Figure 19. First Mixer Output Level and Intermodulation, IP3_bit = 0

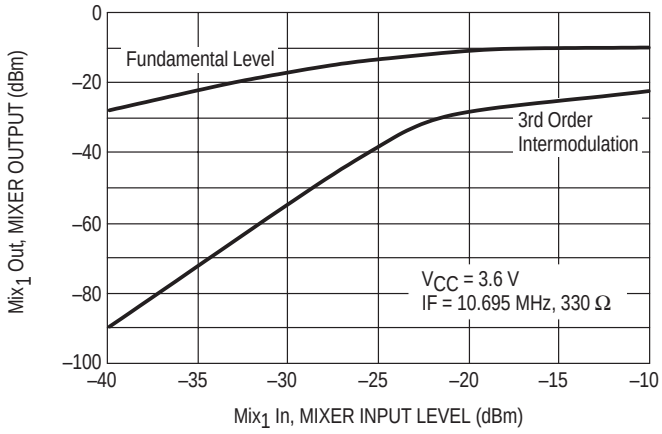


Figure 20. First Mixer Output Level and Intermodulation, IP3_bit = 1

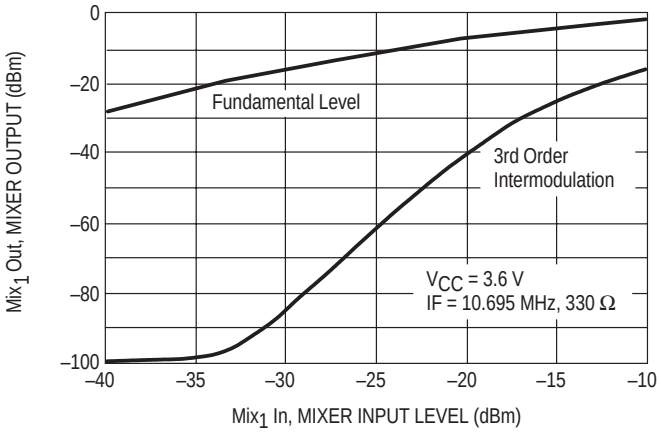


Figure 21. First Mixer Compression versus Supply Voltage

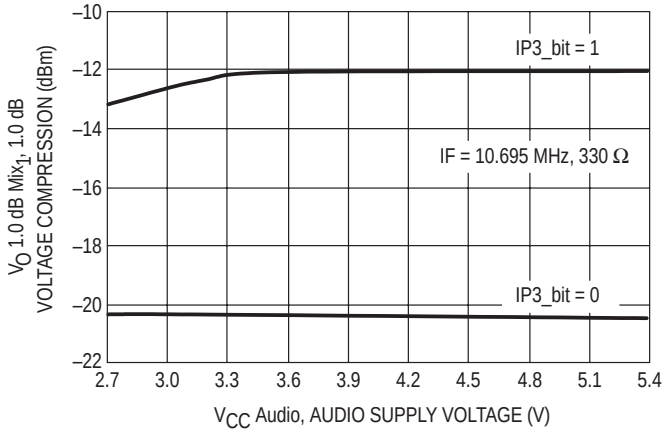
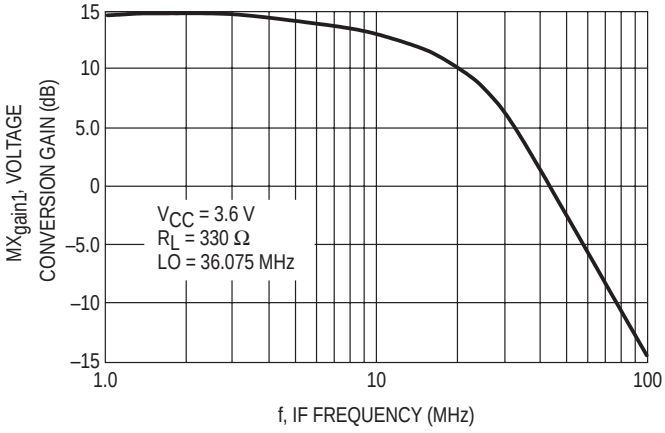


Figure 22. First IF Bandwidth



Second Mixer

Figures 26 through 29 represents the second mixer transfer characteristics for the voltage conversion gain, output level, and intermodulation. There is a slight improvement in gain when the “IP3 bit” is set to <1> for the second mixer. (Note: This is the same programmable bit discussed earlier in the section.)

Figure 23. Second Mixer Input and Output Impedance Schematic

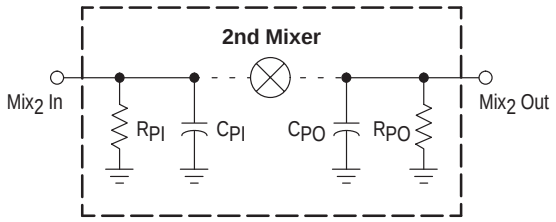


Figure 24. Second Mixer Input and Output Impedances

Unit	Input Impedance R_{PI} // C_{PI}	Output Impedance R_{PO} // C_{PO}
IP3 = <0> (Set Low)	2817 Ω // 3.6 pF	1493 Ω // 6.1 pF
IP3 = <1> (Set High)	2817 Ω // 3.6 pF	1435 Ω // 6.2 pF

The 2nd mixer input impedance is typically 2.8 kΩ. It requires an external 360 Ω parallel resistor for use with a standard 330 Ω, 10.7 MHz ceramic filter. The second mixer output impedance is 1.5 kΩ making it suitable to match standard 455 kHz ceramic filters.

The IF bandwidth response of the second mixer is shown in Figure 31. The –3.0 dB corner is 2.5 MHz. The feedthrough parameters are summarized in Figure 25.

Figure 25. Second Mixer Feedthrough Parameters

Parameter	(dBm)
2nd LO Feedthrough @ Mix_2 Out	–42.9
IF Feedthrough @ Mix_2 Out with –30 dBm	–61.7

SECOND MIXER

Figure 26. Second Mixer Conversion Gain, IP3_bit = 0

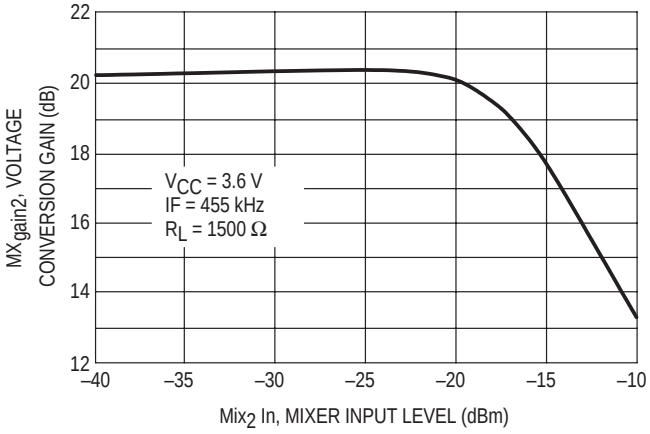


Figure 27. Second Mixer Conversion Gain, IP3_bit = 1

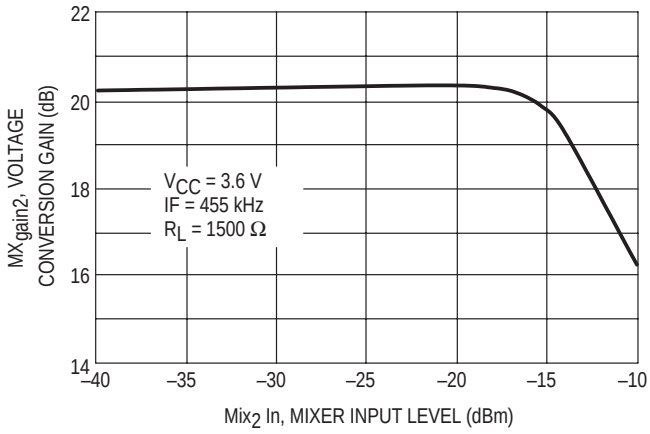


Figure 28. Second Mixer Output Level and Intermodulation, IP3_bit = 0

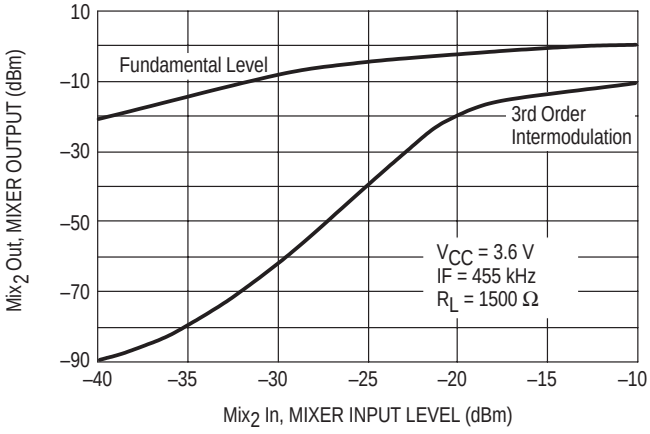


Figure 29. Second Mixer Output Level and Intermodulation, IP3_bit = 1

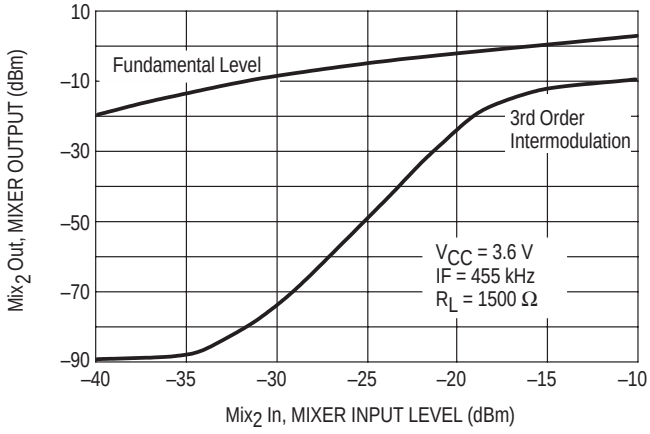


Figure 30. Second Mixer Compression versus Supply Voltage

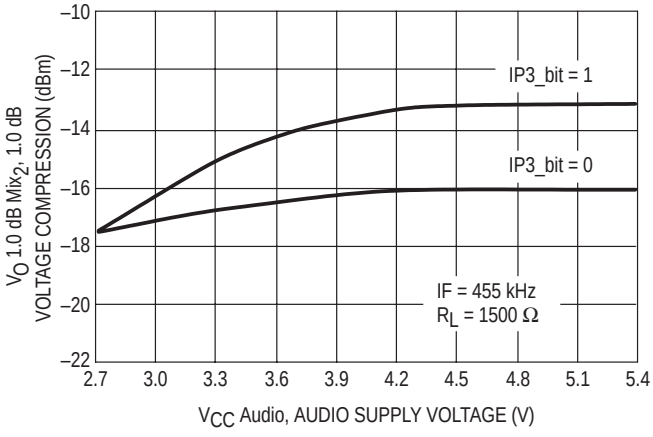
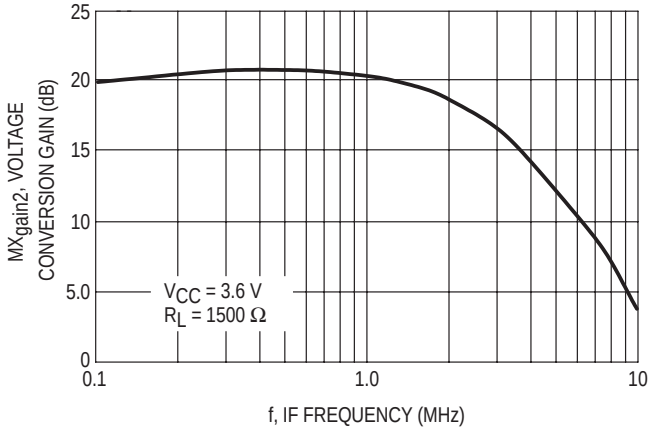


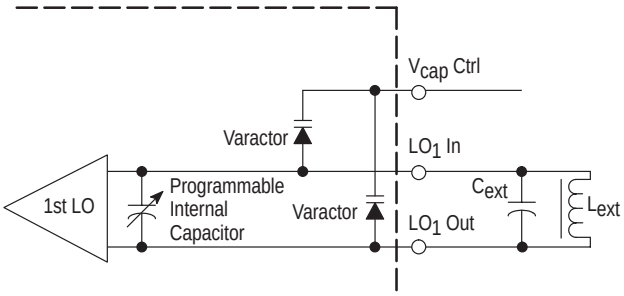
Figure 31. Second IF Bandwidth



First Local Oscillator

The 1st LO is a multi–vibrator oscillator. The tank circuit is composed of a parallel external capacitance and inductance, internal programmable capacitor matrix, and internal varactor. The local oscillator requires a voltage controlled input to the internal varactor and an external loop filter driven by on–board phase–lock control loop (PLL). The 1st LO internal component values have a tolerance of ±15%. A typical dc bias level on the LO Input and LO Output is 0.45 Vdc. The temperature coefficient of the varactor is +0.08%/°C. The curve in Figure 33 is the varactor control voltage range as it relates to varactor capacitance. It represents the expected internal capacitance for a given control voltage (V_{cap}Ctrl) of the MC13110A and MC13111A. Figure 32 shows a representative schematic of the first LO function.

Figure 32. First Local Oscillator Schematic



To select the proper L_{ext} and C_{ext} we can do the following analysis. From Figure 34 it is observed that an inductor will have a significant affect on first LO performance, especially over frequency. The overall minimum Q required for first LO to function as it relates to the LO frequency is also given in Figure 34.

Choose an inductor value, say 470 nH. From Figure 34, the minimum operating Q is approximately 25. From the following equation:

$$Q\ Coil = R_p/X\ Coil$$

where: R_p = parallel equivalent impedance (Figure 35).

C_{ext} can be determined as follows:

$$f_{LO} = \frac{1}{2\pi\sqrt{L_{ext}C_{ext}}}$$

where: L_{ext} = external inductance, C_{ext} = external capacitance.

Figure 34 clearly indicates that for lower coil values, higher quality factors (Q) are required for the first LO to function properly. Also, lower LO frequencies need higher Q's. In Figure 35 the internal programmable capacitor selection relative to the first LO frequency and the parallel impedance is shown. This information will help the user to decide what inductor (L_{ext}) to choose for best performance in terms of Q.

Refer to the Auxiliary Register in the Serial Interface Section for further discussion on LO programmability.

FIRST LOCAL OSCILLATOR

Figure 33. First LO Varicap Capacitance versus Control Voltage

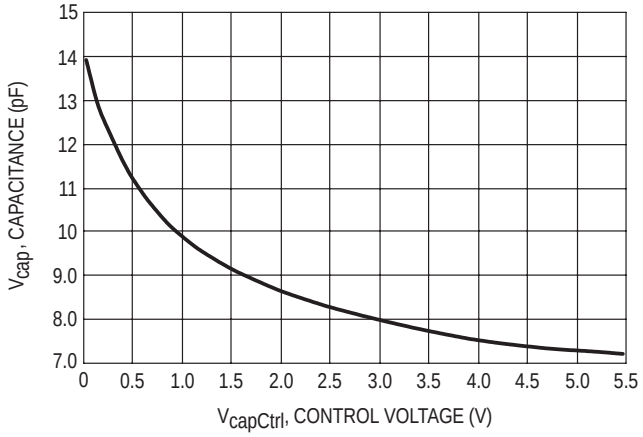


Figure 34. First LO Minimum Required Overall Q Value versus Inductor Value

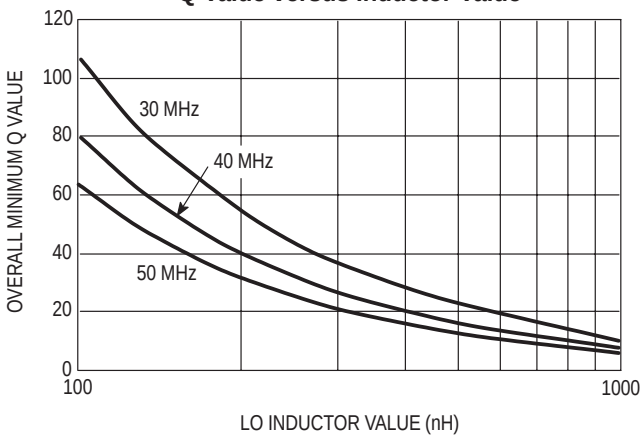


Figure 35. Representative Parallel Impedance versus Capacitor Select

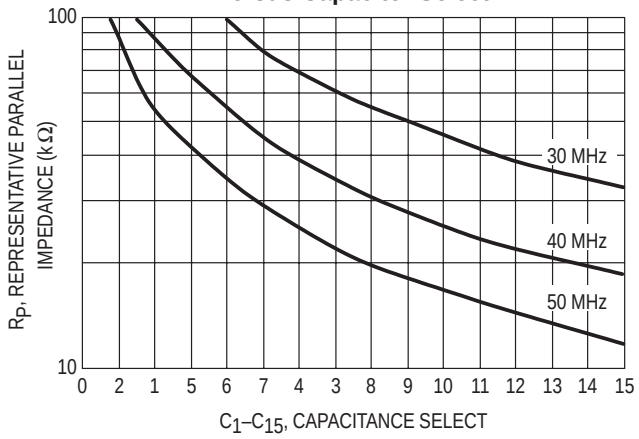


Figure 36. Varicap Value at V_{CV} = 1.0 V Over Temperature

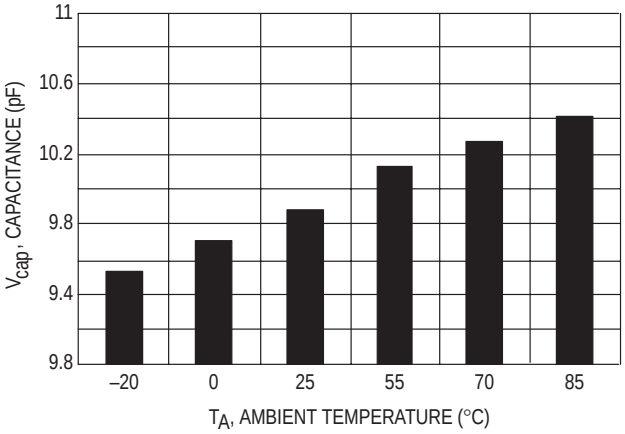


Figure 37. Control Voltage versus Channel Number, U.S. Handset Application

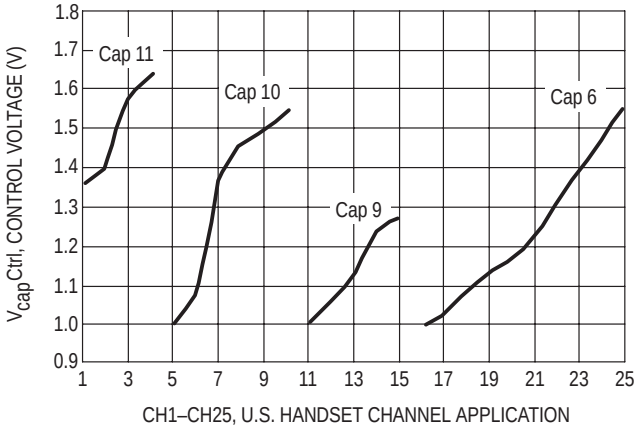
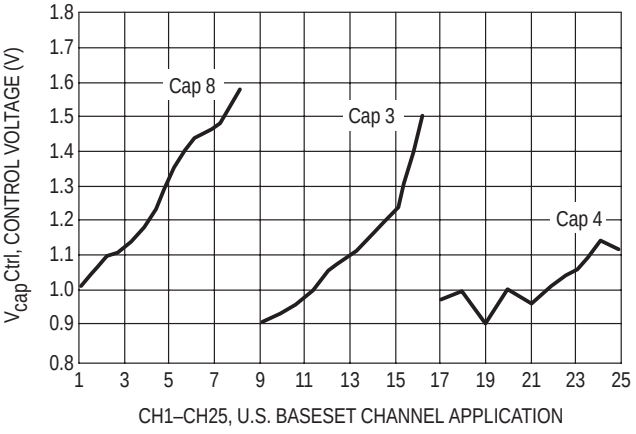


Figure 38. Control Voltage versus Channel Number, U.S. Baseset Application



Second Local Oscillator

The 2nd LO is a CMOS oscillator. It is used as the PLL reference oscillator and local oscillator for the second frequency conversion in the RF receiver. It is designed to utilize an external parallel resonant crystal. See schematic in Figure 39.

Figure 39. Second Local Oscillator Schematic

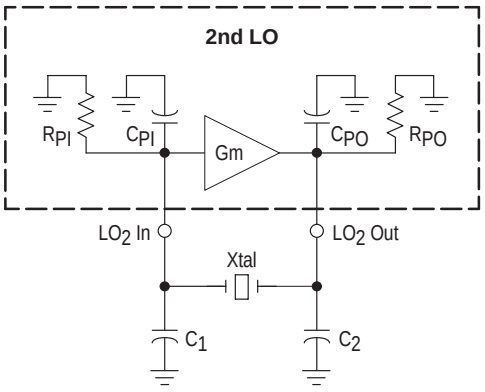


Figure 40. Second Local Oscillator Input and Output Impedance

Input Impedance (R_{PI} // C_{PI})	11.6 kΩ // 2.9 pF
Output Impedance (R_{PO} // C_{PO})	9.6 kΩ // 2.7 pF

Figure 41 shows a typical gain/phase response of the second local oscillator. Load capacitance (C_L), equivalent series resistance (ESR), and even supply voltage will have and affect on the 2nd LO response as shown in Figures 45 and 46. Except for the standby mode open loop gain is fairly constant as supply voltage increases from 2.5 V. This is due to the regulated voltage of 2.5 V on PLL V_{ref}. From the graphs it can seen that optimum performance is achieved when C1 equals C2 (C1/C2 = 1).

Figure 46 represents the ESR versus crystal load capacitance for the 2nd LO. This relationship was defined by using a 6.0 dB minimum loop gain margin at 3.6 V. This is considered the minimum gain margin to guarantee oscillator start–up.

Oscillator start–up is also significantly affected by the crystal load capacitance selection. In Figures 42 and 43 the relationship between crystal load capacitance, supply voltage, and external load capacitance ratio (C2/C1), can be seen. The lower the load capacitance the better the performance.

Given the desired crystal load capacitance, C1 and C2 can be determined from Figure 47. It is also interesting to point out that current consumption increases when C1 ≠ C2, as shown in Figure 44.

Be careful not to overdrive the crystal. This could cause a noise problem. An external series resistor on the crystal output can be added to reduce the drive level, if necessary.

SECOND LOCAL OSCILLATOR

Figure 41. Second LO Gain/Phase @ –10 dBm

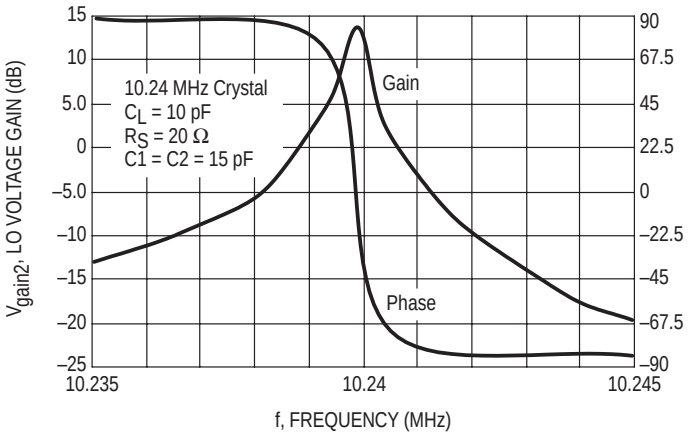
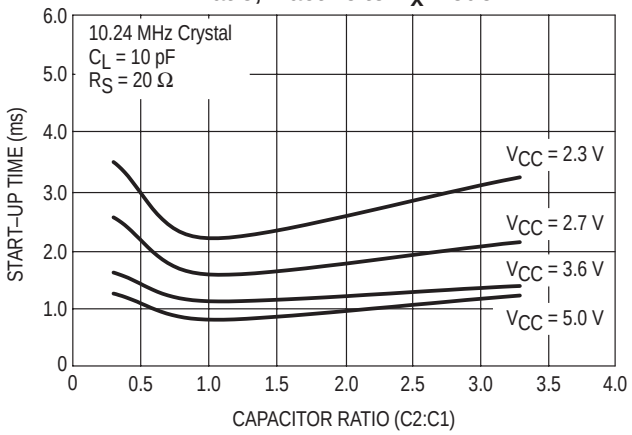


Figure 42. Start–Up Time versus Capacitor Ratio, Inactive to R_X Mode



SECOND LOCAL OSCILLATOR

Figure 43. Start–Up Time versus Capacitor Ratio, Inactive to R_X Mode

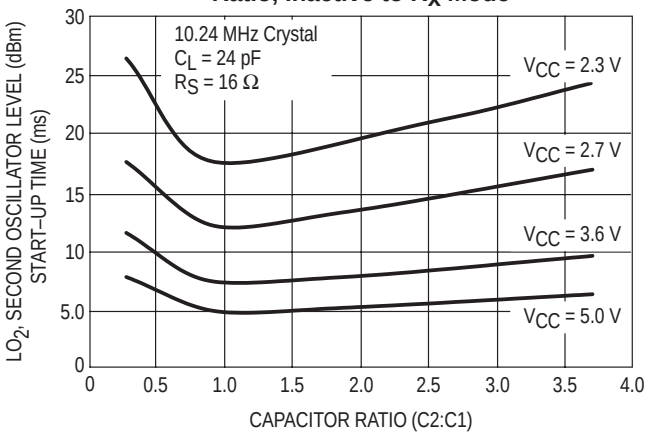


Figure 44. Second LO Current Consumption versus Capacitor Ratio

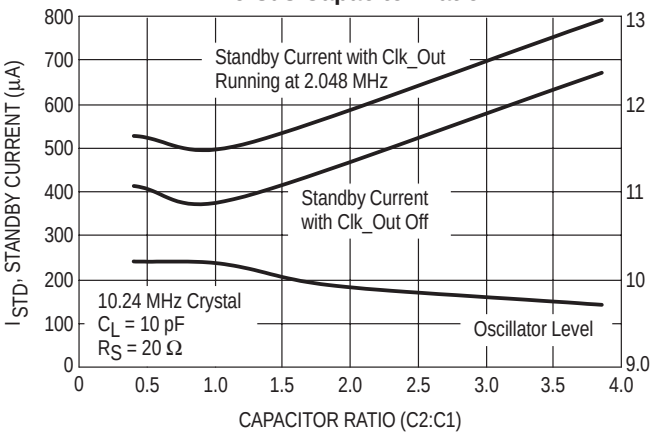


Figure 45. Maximum Open Loop Gain versus Capacitor Ratio

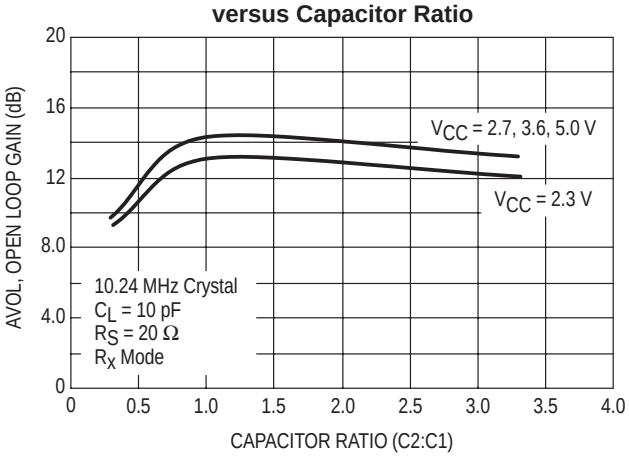


Figure 46. Maximum Allowable Equivalent Series Resistance (ESR) versus Crystal Load Capacitance

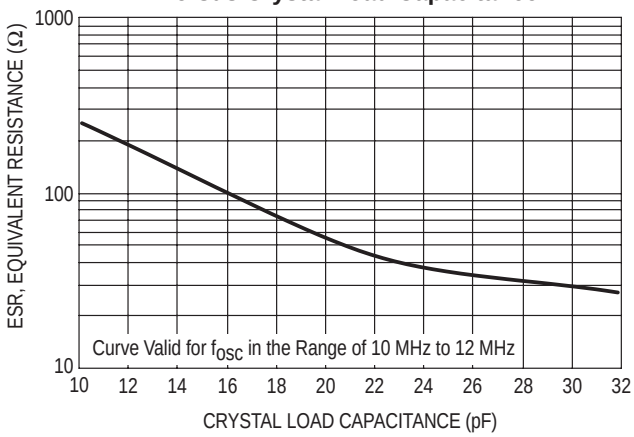
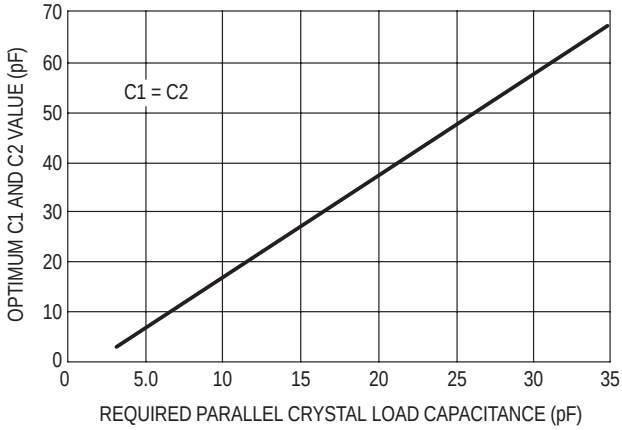


Figure 47. Optimum Value for C1 and C2 versus Equivalent Required Parallel Capacitance of the Crystal



IF Limiter and Demodulator

The limiting IF amplifier typically has about 110 dB of gain; the frequency response starts rolling off at 1.0 MHz. Decoupling capacitors should be placed close to Pins 31 and 32 to ensure low noise and stable operation. The IF input impedance is 1.5 kΩ. This is a suitable match to 455 kHz ceramic filters.

Figure 48. IF Limiter Schematic

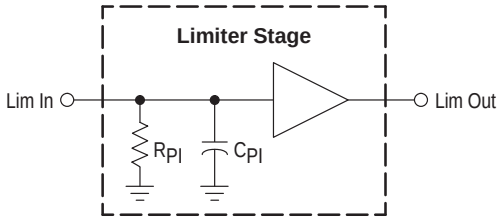
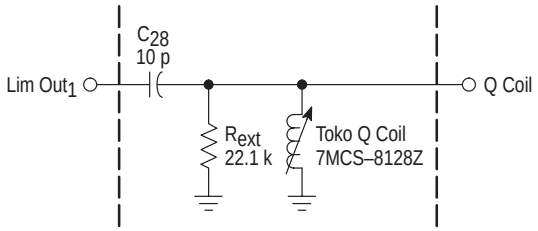


Figure 49. Limiter Input Impedance

Unit	Input Impedance (R_{PI})	Input Impedance (C_{PI})
Lim In	1538 Ω	15.7 pF

Figure 50. Quadrature Detector Demodulator Schematic



The quadrature detector is coupled to the IF with an external capacitor between Pins 27 and 28. Thus, the recovered signal level output is increased for a given bandwidth by increasing the capacitor. The external quadrature component may be either a LCR resonant circuit, which may be adjustable, or a ceramic resonator which is usually fixed tuned. (More on ceramic resonators later.)

The bandwidth performance of the detector is controlled by the loaded Q of the LC tank circuit (Figure 50). The following equation defines the components which set the detector circuit's bandwidth:

(1) $R_T = Q\ X_L$,

where R_T is the equivalent shunt resistance across the LC tank. X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi\ f\ L$).

The 455 kHz IF center frequency is calculated by:

(2) $f_C = [2\pi\ (L\ Cp)^{1/2}] - 1$

where L is the parallel tank inductor. Cp is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a detector at 455 kHz and a specific loaded Q:

The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass for margin. For an IF frequency of 455 kHz and an IF bandpass of 20 kHz, the IF bandpass Q is approximately 23; the loaded Q of the quadrature tank is chosen slightly lower at 15.

Example:

Let the total external C = 180 pF. (Note: the capacitance is the typical capacitance for the quad coil.) Since the external capacitance is much greater than the internal device and PCB parasitic capacitance, the parasitic capacitance may be neglected.

Rewrite equation (2) and solve for L:

$L = (0.159)^2/(C\ f_c^2)$
L = 678 μH ; Thus, a standard value is chosen:
L = 680 μH (surface mount inductor)

The value of the total damping resistor to obtain the required loaded Q of 15 can be calculated from equation (1):

$R_T = Q(2\pi\ f\ L)$
$R_T = 15(2\pi)(0.455)(680) = 29.5\ k\Omega$

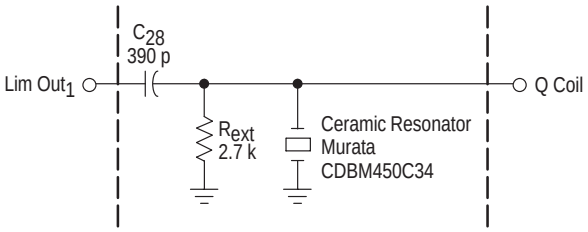
The internal resistance, R_{int} at the quadrature tank Pin 27 is approximately 100 kΩ and is considered in determining the external resistance, R_{ext} which is calculated from:

$R_{ext} = ((R_T)(R_{int}))/(R_{int} - R_T)$
R_{ext} = 41.8 kΩ;Thus, choose a standard value:
R_{ext} = 39 kΩ

In Figure 50, the R_{ext} is chosen to be 22.1 kΩ. An adjustable quadrature coil is selected. This tank circuit represents one popular network used to match to the 455 kHz carrier frequency. The output of the detector is represented as a "S–curve" as shown in Figure 52. The goal is to tune the inductor in the area that is most linear on the "S–curve" (minimum distortion) to optimize the performance in terms of dc output level. The slope of the curve can also be adjusted by choosing higher or lower values of R_{ext}. This will have an affect on the audio output level and bandwidth. As R_{ext} is increased the detector output slope will decrease. The maximum audio output swing and distortion will be reduced and the bandwidth increased. Of course, just the opposite is true for smaller R_{ext}.

A ceramic discriminator is recommended for the quadrature circuit in applications where fixed tuning is desired. The ceramic discriminator and a 5.6 kΩ resistor are placed from Pin 27 to V_{CC}. A 22 pF capacitor is placed from Pin 28 to 27 to properly drive the discriminator. MuRata Erie has designed a resonator for this part (CDBM455C48 for USA & A/P regions and CDBM450C48 for Europe). This resonator has been designed specifically for the MC13110/111 family. Figure 51 shows the schematic used to generate the "S–curve" and waveform shown in Figure 54 and 55.

Figure 51. Ceramic Resonator Demodulator Schematic with Murata CDBM450C48



(CDBM455C48 US; CDBM450C48 France)

The “S–curve” for the ceramic discriminator shown in Figure 54 is centered around 450 kHz. It is for the French application. The same resonator is also used for the US application and is centered around 455 kHz. Clearly, the “S–curves” for the resonator and quad coil have very similar limiter outputs. As discussed previously, the slope of the “S–curve” centered around the center frequency can be controlled by the parallel resistor, R_{ext}. Distortion, bandwidth, and audio output level will be affected.

IF LIMITER AND DEMODULATION

Figure 52. S–Curve of Limiter Discriminator with Quadrature Coil

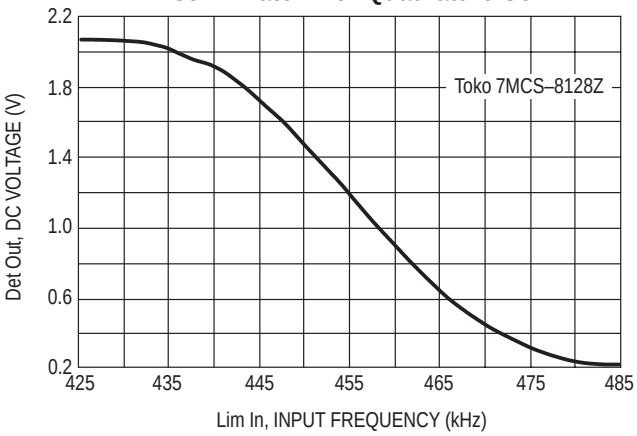


Figure 53. Typical Limiter Output Waveform with Quadrature Coil

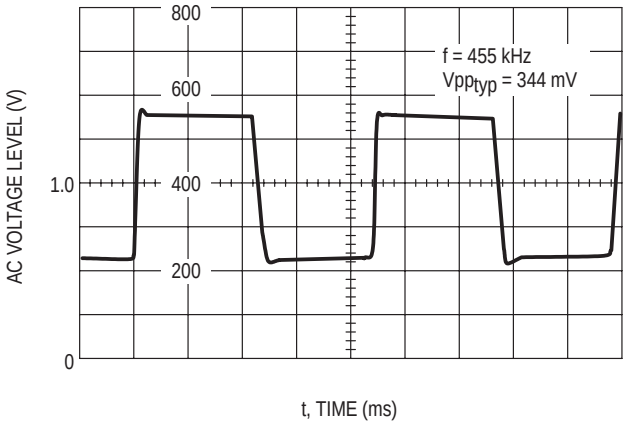


Figure 54. S–Curve of Limiter Discriminator with Ceramic Resonator

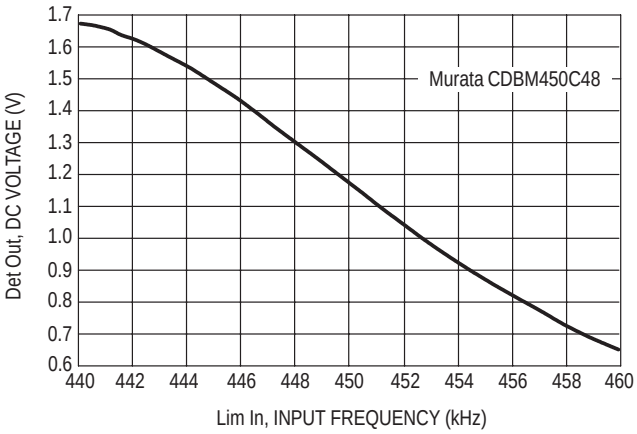
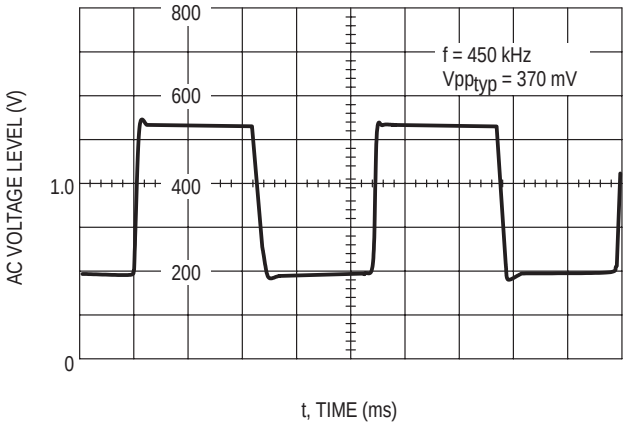


Figure 55. Typical Limiter Output Waveform with Ceramic Resonator



RSSI and Carrier Detect

The Received Signal Strength Indicator (RSSI) indicates the strength of the IF level. The output is proportional to the logarithm of the IF input signal magnitude. RSSI dynamic range is typically 80 dB. A 187 kΩ resistor to ground is provided internally to the IC. This internal resistor converts the RSSI current to a voltage level at the “RSSI” pin. To improve the RSSI accuracy over temperature an internal compensated reference is used. Figure 56 shows the RSSI versus RF input. The slope of the curve is 16.5 mV/dB.

The Carrier Detect Output (CD Out) is an open–collector transistor output. An external pull–up resistor of 100 kΩ will be required to bias this device. To form a carrier detect filter a capacitor needs to be connected from the RSSI pin to ground. The carrier detect threshold is programmable through the MPU interface (see “Carrier Detect Threshold Programming” in the serial interface section). The range can be scaled by connecting additional external resistance from the RSSI pin to ground in parallel with the capacitor. From Figure 57, the affect of an external resistor at RSSI on the carrier detect level can be noticed. Since there is hysteresis in the carrier detect comparator, one trip level can be found when the input signal is increased while the another one can be found when the signal is decreased.

Figure 58 represents the RSSI ripple in relation to the RF input for different filtering capacitors at RSSI. Clearly, the higher the capacitor, the less the ripple. However, at low carrier detect thresholds, the ripple might supersede the hysteresis of the carrier detect. The carrier detect output may appear to be unstable. Using a large capacitor will help to stabilize the RSSI level, but RSSI charge time will be affected. Figure 59 shows this relationship.

The user must decide on a compromise between the RSSI ripple and RSSI start–up time. Choose a 0.01 μf capacitor as a starting point. For low carrier detect threshold settings, a 0.047 μf capacitor is recommended.

RSSI AND CARRIER DETECT

Figure 56. Typical RSSI Voltage Level versus RF Input

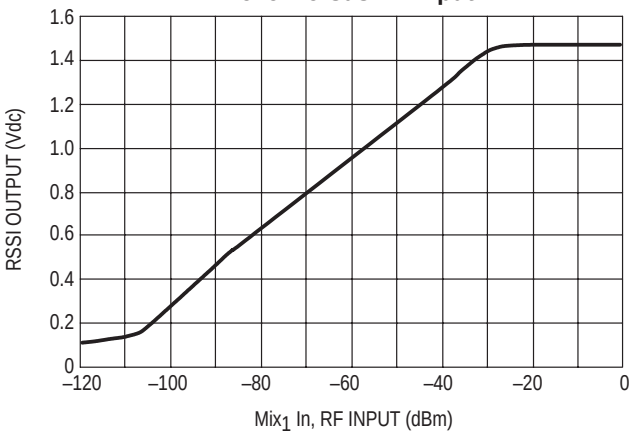


Figure 57. Carrier Detect Threshold versus External RSSI Resistor

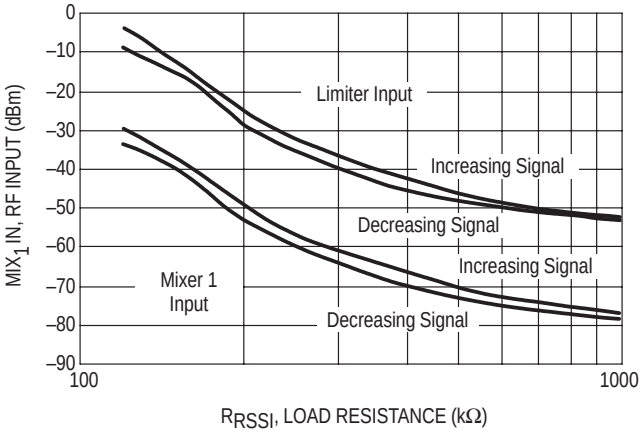


Figure 58. RSSI Ripple versus RF Input Level for Different RSSI Capacitors

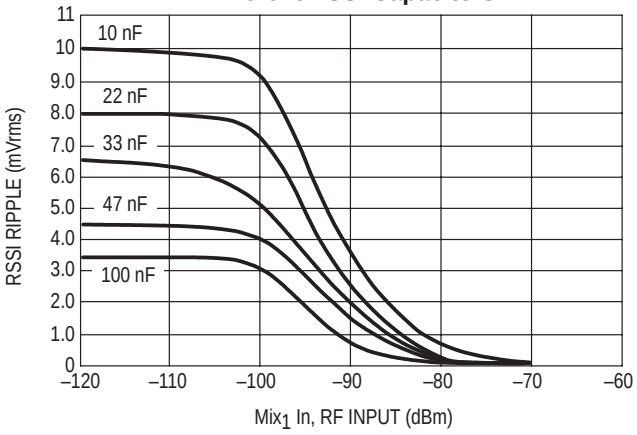
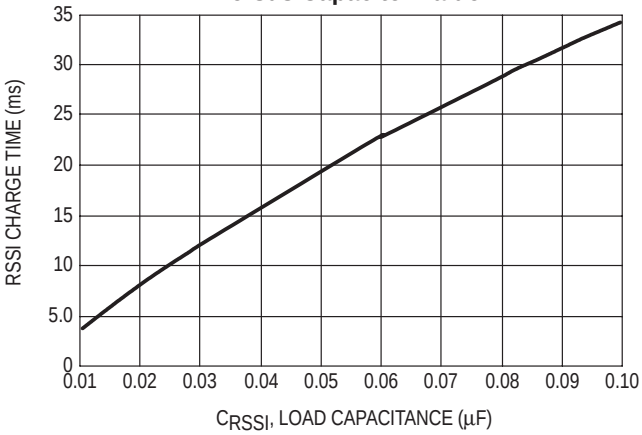


Figure 59. RSSI Charge Time versus Capacitor Value



RF System Performance

The sensitivity of the IC is typically 0.4 μVrms matched (single ended or differential) with no preamp. To achieve suitable system performance, a preamp and passive duplexer may be used. In production final test, each section of the IC is separately tested to guarantee its system performance in the specific application. The preamp and duplexer (differential, matched input) yields typically –115 dBm @ 12 dB SINAD sensitivity performance under full duplex operation. See Figure 45 and 48.

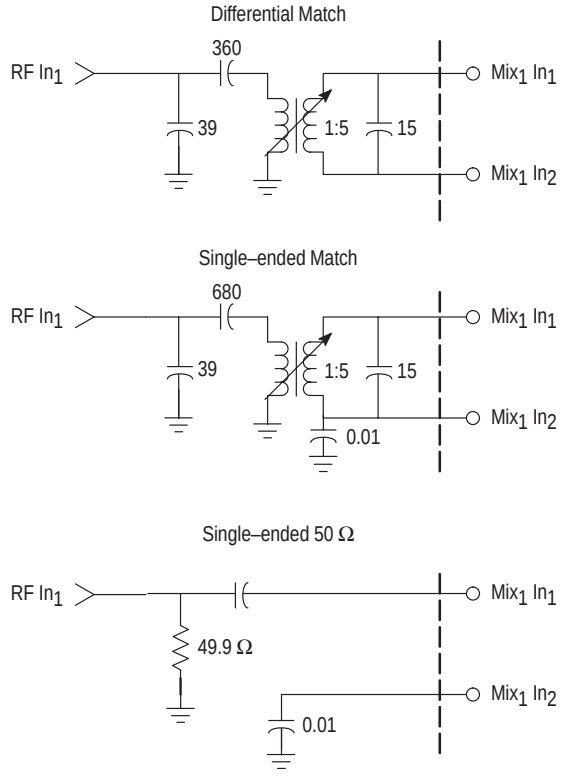
The duplexer is important to achieve full duplex operation without significant “de–sensing” of the receiver by the transmitter. The combination of the duplexer and preamp circuit should attenuate the transmitter power to the receiver by over 60 dB. This will improve the receiver system noise figure without giving up too much IMD performance.

The duplexer may be a two piece unit offered by Shimida, Sansui, or Toko products (designed for 25 channel CT–0 cordless phone). The duplexer frequency response at the receiver port has a notch at the transmitter frequency band of about 35 to 40 dB with a 2.0 to 3.0 dB insertion loss at the receiver frequency band.

The preamp circuit utilizes a tuned transformer at the output side of the amplifier. This transformer is designed to bandpass filter at the receiver input frequency while rejecting the transmitter frequency. The tuned preamp also improves the noise performance by reducing the bandwidth of the pass band and by reducing the second stage contribution of the 1st mixer. The preamp is biased such that it yields suitable noise figure and gain.

The following matching networks have been used to obtain 12 dB SINAD sensitivity numbers:

Figure 60. Matching Input Networks



The exact impedance looking into the RF In1 pin is displayed in the following table along with the sensitivity levels.

Figure 61. 12 dB SINAD Sensitivity Levels, US Handset Application Channel 21

	Sensitivity (dBm)	Input Impedance (dBm)
Differential matched	–115.3	50.2 ± 0.1j
Single–ended match	–114.8	50.2 ± 0.1j
Single–ended 50 Ω	–100.1	50.2 ± 0.1j

The graphs in Figures 64 to 69 are performance results based on Evaluation Board Schematic (Figure 137). This evaluation board did not use a duplexer or preamp stage. Figure 62 is a summary of the RF performance and Figure 63 contains the French RF Performance Summary.

Figure 62. RF Performance Summary for US Applications

MC13110A/MC13111A (fdev = 3.0 kHz, fmod = 1.0 kHz, 50 Ω)			
Parameter	**Handset**	**Baseset**	**Unit**
Sensitivity at 12 dB SINAD	–100.1	–100.1	dBm
Recovered Audio	132	132	mVrms
SINAD @ –30 dBm	41.8	41.4	dB
THD @ –30 dBm	0.8	0.8	%
S/N @ –30 dBm	78.2	78.5	dB
AMRR @ –30 dBm	73.4	72.2	dB
RSSI range	>80	>80	dB

Figure 63. RF Performance Summary for US French Applications

MC13110A/MC13111A (fdev = 1.5 kHz, fmod = 1.0 kHz, 50 Ω)			
Parameter	**Handset**	**Baseset**	**Unit**
Sensitivity at 12 dB SINAD	–91	–90.8	dBm
Recovered Audio	89.8	90	mVrms
SINAD @ –30 dBm	42.1	44.3	dB
THD @ –30 dBm	0.8	0.8	%
S/N @ –30 dBm	75.7	75.1	dB
AMRR @ –30 dBm	56	84.7	dB
RSSI range	>80	>80	dB

RF SYSTEM PERFORMANCE

Figure 64. Typical Receiver Performance Parameters U.S. Handset Application Channel 21

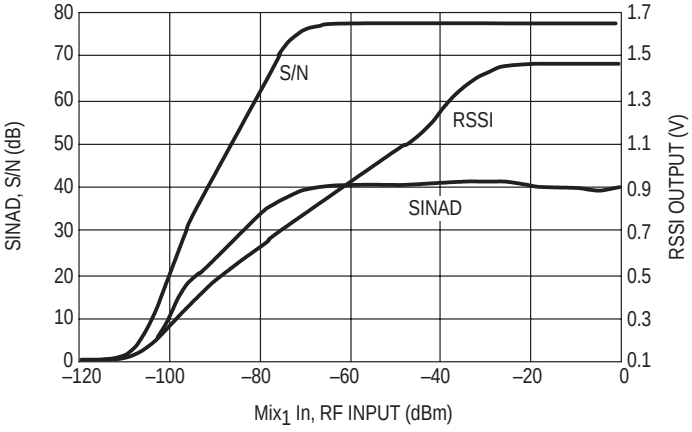


Figure 65. Typical Performance Parameters Over U.S. Handset Channel Frequencies

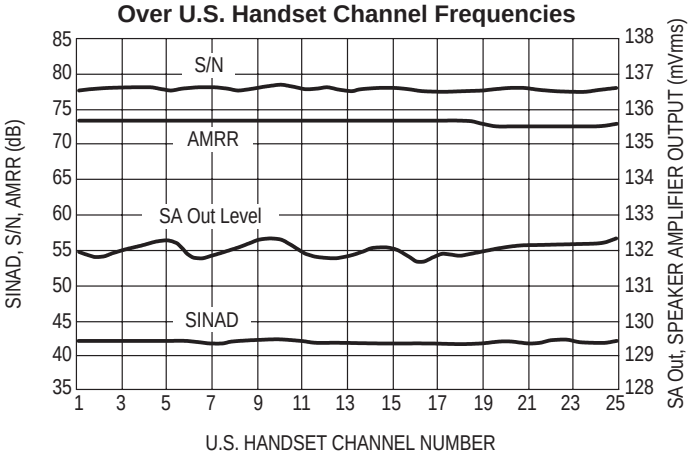


Figure 66. Typical Performance Parameters Over U.S. Baseset Channel Frequencies

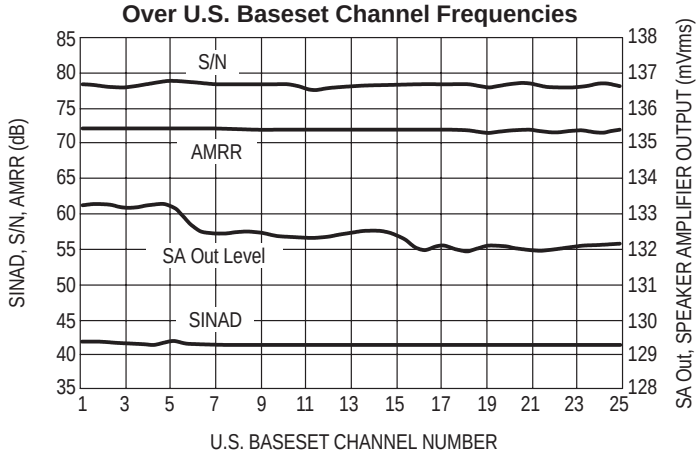


Figure 67. Typical Receiver Performance for US Handset Application Channel 21

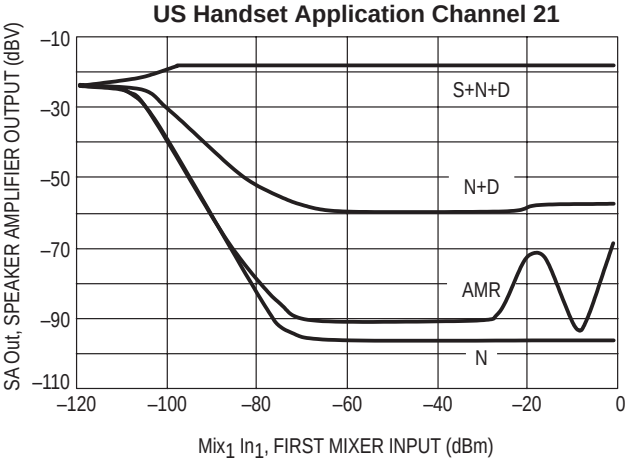


Figure 68. 12 dB SINAD Sensitivity Over US Handset Application Channels

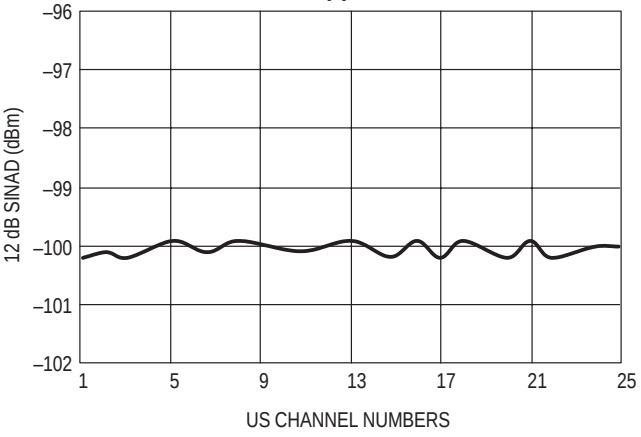
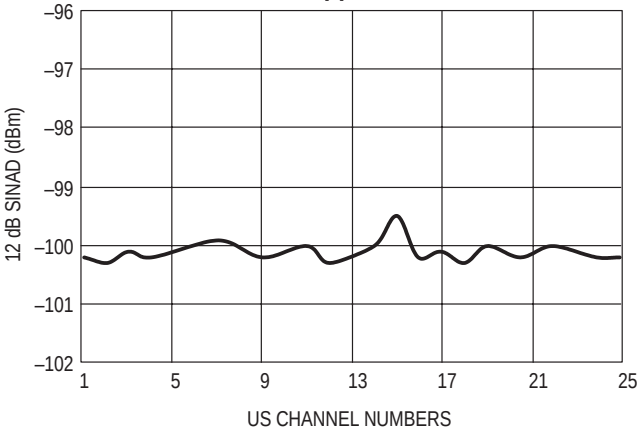


Figure 69. 12 dB SINAD Sensitivity Over US Baseset Application Channels



Receive Audio Path

The R_X Audio signal path begins at “Rx Audio In” and goes through the IC to “E Out”. The “R_X Audio In”, “Scr Out”, and “E In” pins are all ac–coupled. This signal path consists of filters; programmable R_X gain adjust, R_X mute, and volume control, and finally the expander. The typical maximum output voltage at “E Out” should be approximately 0 dBV @ THD = 5.0% .

Figures 71 to 73 represent the receive audio path filter response. The filter response attenuation is very sharp above 3900 Hz, which is the cutoff frequency. Inband (audio), out–of–band, and ripple characteristics are also shown in these graphs.

The group delay (Figure 75) has a peak around 6.5 kHz. This spike is formed by rapid change in the phase at the frequency. In practice this does not cause a problem since the signal is attenuated by at least 50 dB.

The output capability at “Scr Out” and “E Out” are shown in Figures 76, 77, and 78. The results were obtained by increasing the input level for 2.0% distortion at the outputs.

In Figure 70, noise data for the R_X audio path is shown. At Scr Out, the noise level clearly rises when the scrambler is enabled. However, assuming a nominal output level of –20 dBV (100 mVrms) at the 0 dB gain setting, the noise floor is more than 56 dB below the audio signal. However, the noise data at E Out and SA Out is much more improved.

Speaker Amp

The Speaker Amp is an inverting rail–to–rail operational amplifier. The noninverting input is connected to the internal VB reference. External resistors and capacitors are used to set the gain and frequency response. The “SA In” input pin must be ac–coupled. The typical output voltage at “SA Out” is 2.6 V_{pp} with a 130 Ω load. The speaker amp response is shown in Figures 79 and 80.

Data Amp Comparator

The data amp comparator is an inverting hysteresis comparator. Its open collector output has an internal 100 kΩ pull–up resistor. A band pass filter is connected between the “Det Out” pin and the “DA In” pin with component values as shown in the Application Circuit schematic. The “DA In” input signal needs to be ac–coupled, too.

Figure 70. R_X Path Noise Data

Receive Scrambler	Receive Gain (dB)	Volume (dB)	SCR_Out (dBV)	E_Out (dBV)	SA_Out (dBV)
off/on	muted	muted	< –95	< –95	< –95
off	–9.0	–14	–92	< –95	< –95
off	0	0	–85	< –95	< –95
off	1.0	16	–76	< –95	< –95
on (MC13110A)	–9.0	–14	–85	< –95	< –95
on (MC13110A)	0	0	–77	< –95	< –95
on (MC13110A)	10	16	–66	< –95	< –95

R_X AUDIO

Figure 71. R_X Audio Wideband Frequency Response

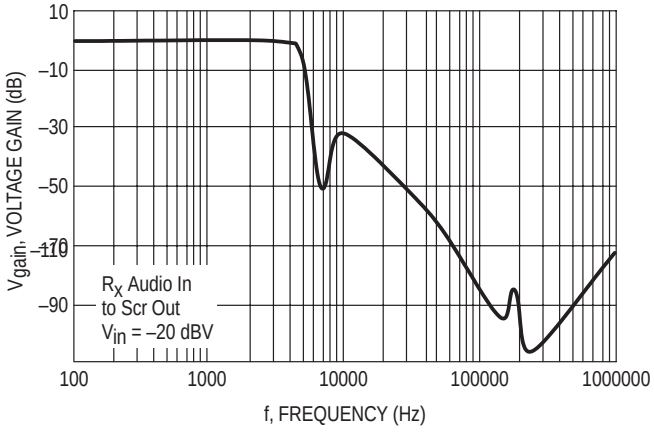


Figure 72. R_X Audio Inband Frequency Response

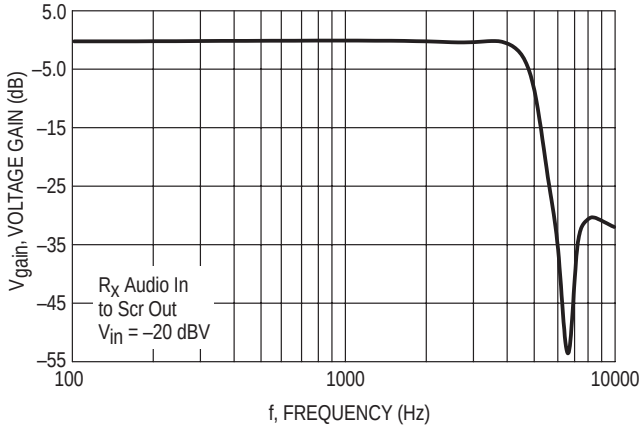


Figure 73. R_X Audio Ripple Response

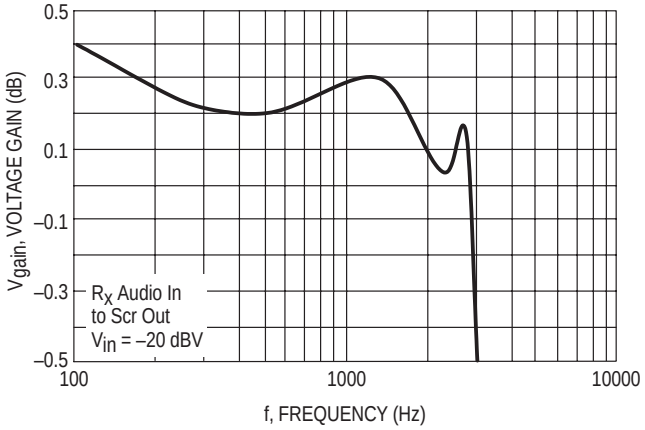


Figure 74. R_X Audio Inband Phase Response

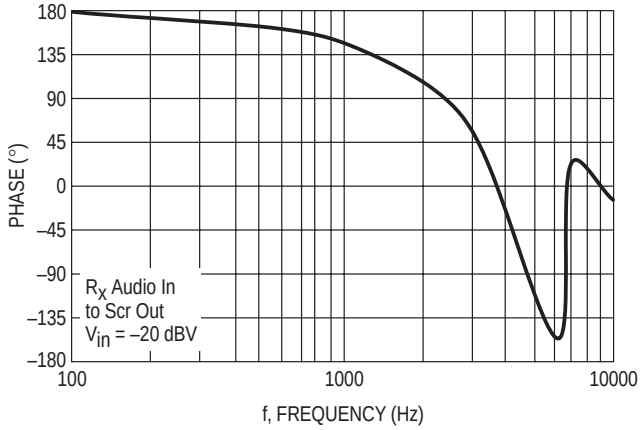


Figure 75. R_X Audio Inband Group Delay

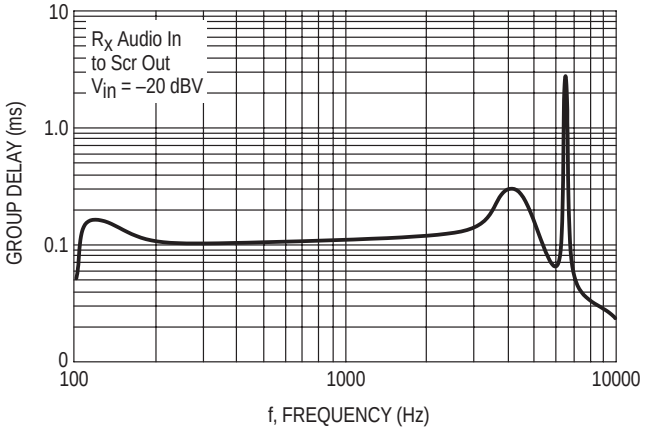
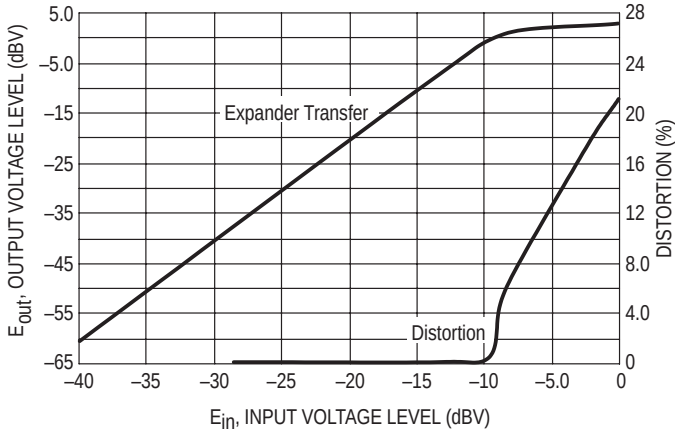


Figure 76. R_X Audio Expander Response



R_X AUDIO

Figure 77. R_X Audio Maximum Output Voltage versus Gain Control Setting

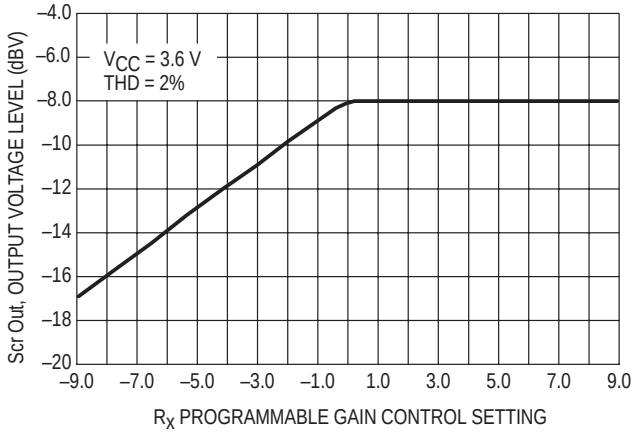


Figure 78. R_X Audio Maximum Output Voltage versus Volume Setting

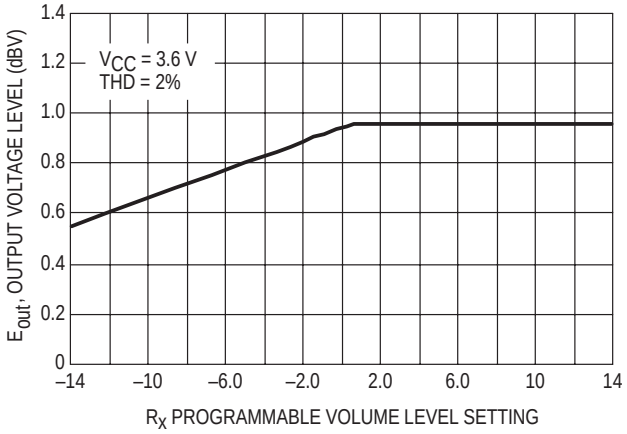


Figure 79. R_X Audio Speaker Amplifier Drive

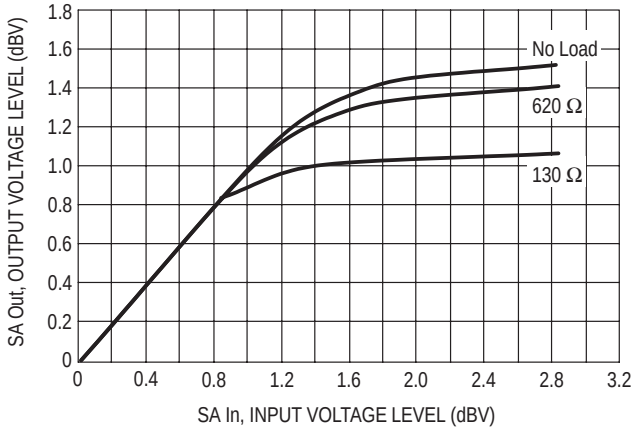
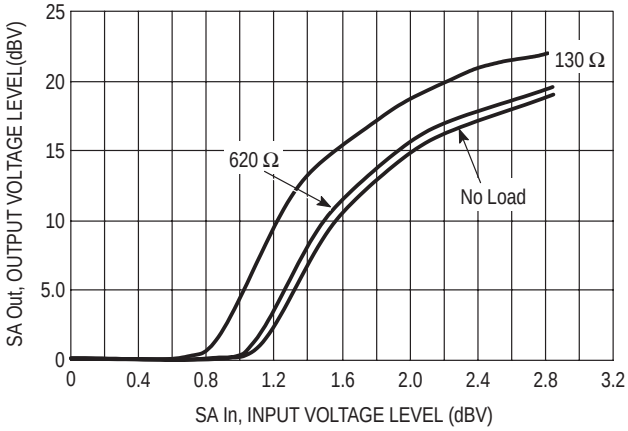


Figure 80. R_X Audio Speaker Amplifier Distortion



Transmit Audio Path

This portion of the audio path goes from "C In" to "T_X Out". The "C In" pin will be ac–coupled. The audio transmit signal path includes automatic level control (ALC) (also referred to as the Compressor), T_X mute, limiter, filters, and T_X gain adjust. The ALC provides "soft" limiting to the output signal swing as the input voltage slowly increases. With this technique the gain is slightly lowered to help reduce distortion of the audio signal. The limiter section provides hard limiting due to rapidly changing signal levels, or transients. This is accomplished by clipping the signal peaks. The ALC, T_X mute, and limiter functions can be enabled or disabled via the MPU serial interface. The T_X gain adjust can also be remotely controlled to set different desired signal levels. The typical maximum output voltage at "T_X Out" should be approximately 0 dBV @ THD = 5.0%.

Figures 82 to 86 represent the transmit audio path filter response. The filter response attenuation, again, is very definite above 3800 Hz. This is the filter cutoff frequency. Inband (audio), wideband, and ripple characteristics are also shown in these graphs.

The compressor transfer characteristics, shown in Figure 87, has three different slopes. A typical compressor slope can be found between –55 and –15 dBV. Here the slope is 2.0. At an input level above –15 dBV the automatic level control (ALC) function is activated and prevents hard clipping of the output. The slope below –55 dBV input level is one. This is where the compressor curve ends. Above 5.0 dBV the output actually begins to decrease and distort. This is due to supply voltage limitations.

In Figure 88 the ALC function is off. Here the compressor curve continues to increase above –15 dBV up to –4.0 dBV. The limiter begins to clip the output signal at this level and distortion is rapidly rising. Similarly, Figure 68 (ALC and Limiter Off) shows to compressor transfer curve extending all the way up to the maximum output. Finally, Figure 90 through 93 show the T_X Out signal versus several combinations of ALC and Limiter selected.

Figure 81 is the noise data measured for the MC13110A/13111A. This data is for 0 dB gain setting and –20 dBV (100 mVrms) audio levels.

Figure 81. T_X Path Noise Data

Transmit Scrambler	Transmit Gain (dB)	Amp_Out (dBV)	T_X_Out (dBV)
off/on	muted	muted	< –95
off	–9.0	< –95	–83
off	0	< –95	–74
off	10	< –95	–64
on (MC13110A)	–9.0	< –95	–82
on (MC13110A)	0	< –95	–73
on (MC13110A)	10	–< –95	–63

Mic Amp

Like the Speaker Amp the Mic Amp is also an inverting rail–to–rail operational amplifier. The noninverting input terminal is connected to the internal VB reference. External resistors and capacitors are used to set the gain and frequency response. The "T_X In" input is ac–coupled.

T_X AUDIO

Figure 82. T_X Audio Wideband Frequency Response

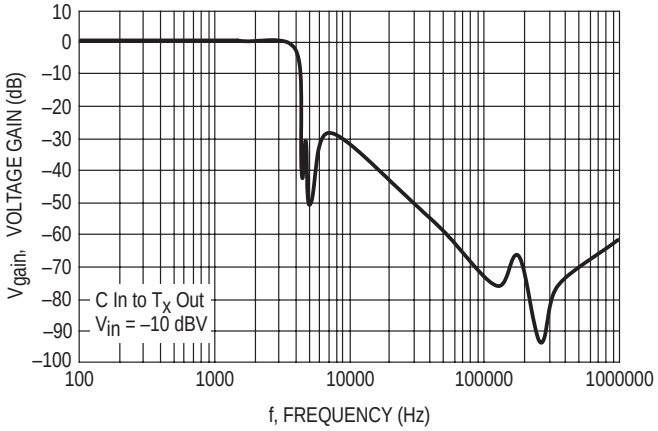


Figure 83. T_X Audio Inband Frequency Response

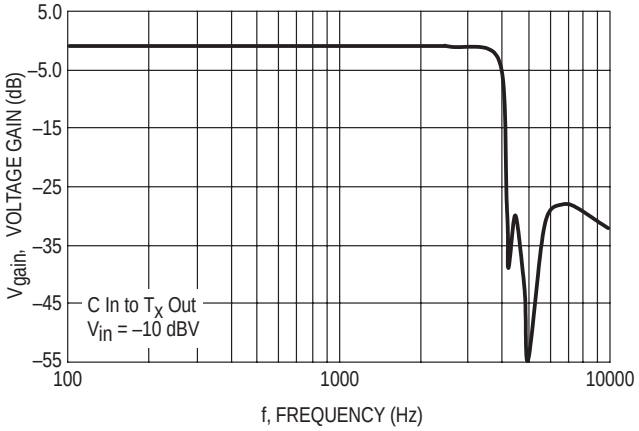


Figure 84. T_X Audio Ripple Response

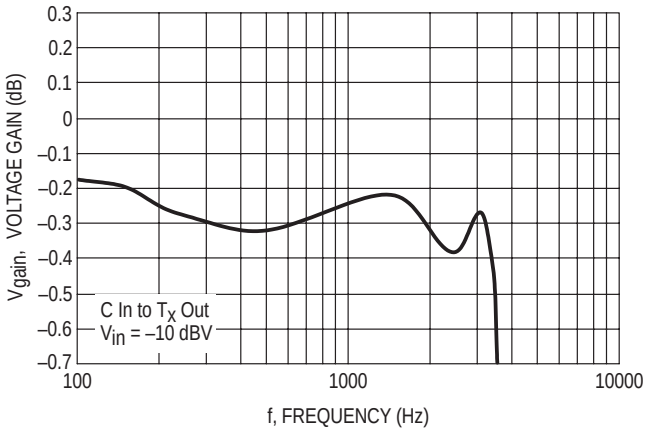


Figure 85. T_X Audio Inband Phase Response

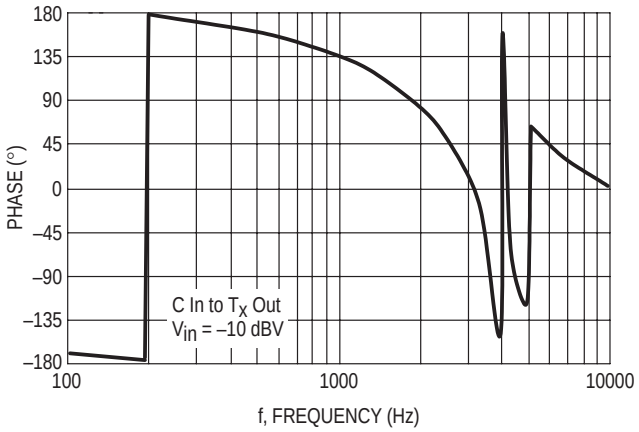


Figure 86. T_X Audio Inband Group Delay

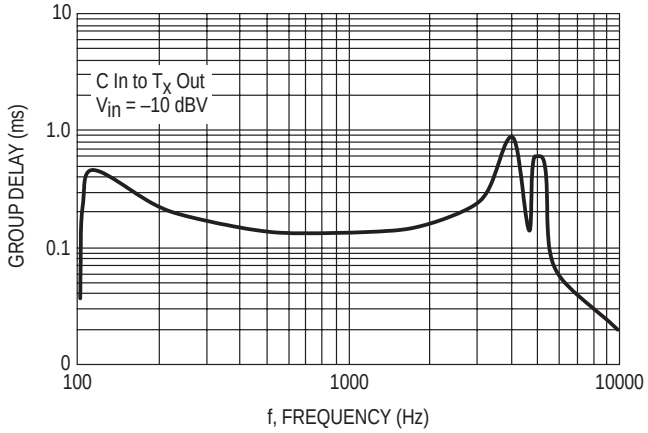
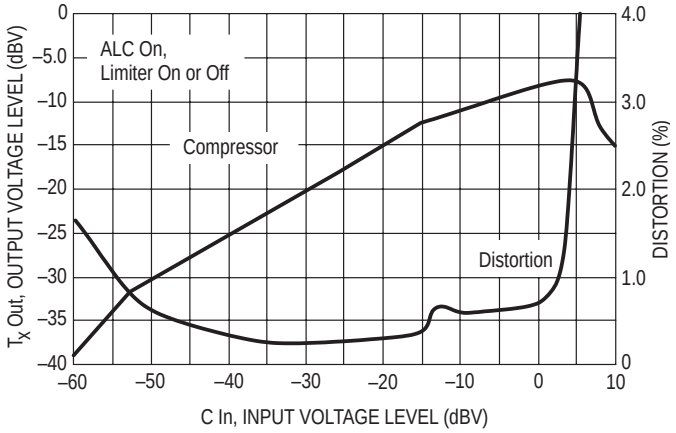


Figure 87. T_X Audio Compressor Response



T_X AUDIO

Figure 88. T_X Audio Compressor Response

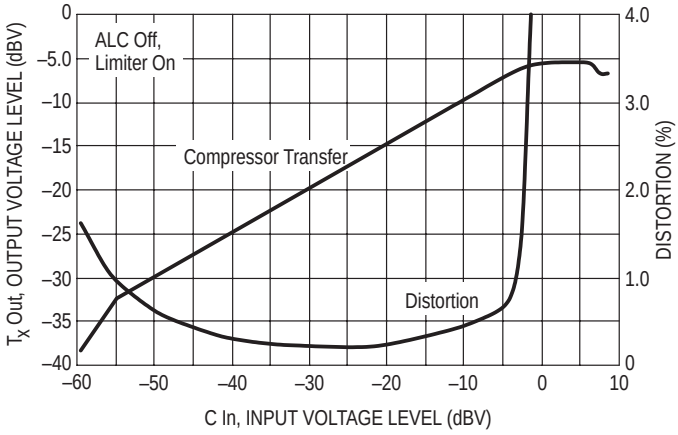


Figure 89. T_X Audio Compressor Response

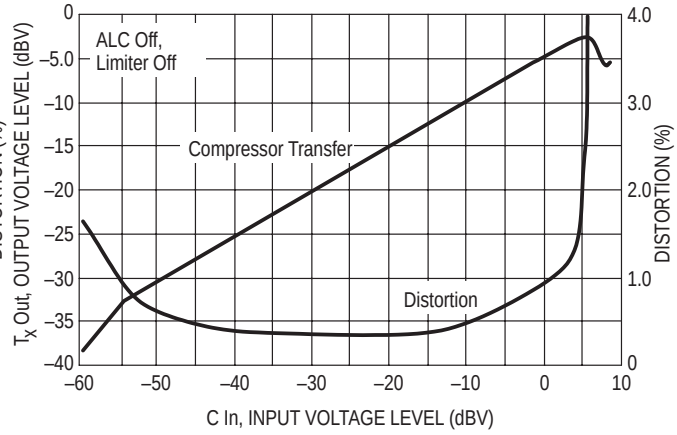


Figure 90. T_X Audio Maximum Output Voltage versus Gain Control Setting

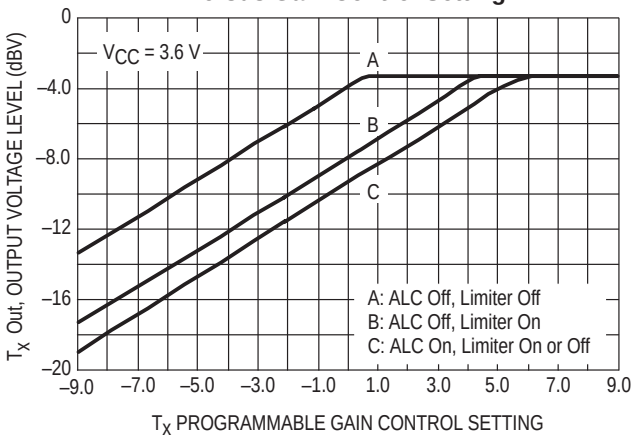


Figure 91. T_X Output Audio Response

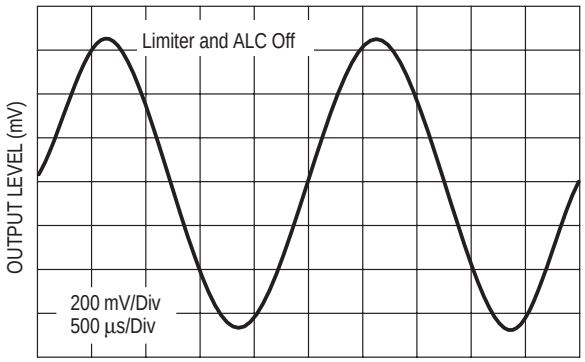


Figure 92. T_X Output Audio Response

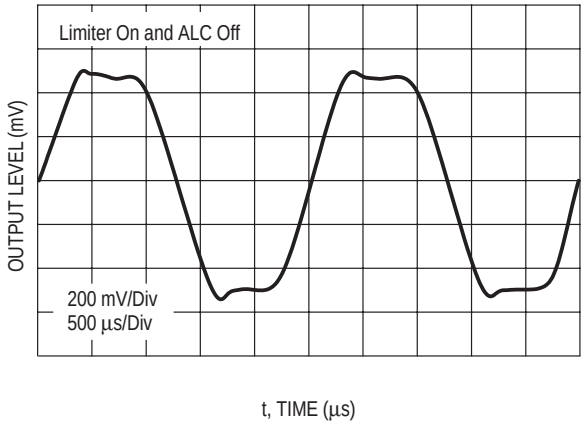
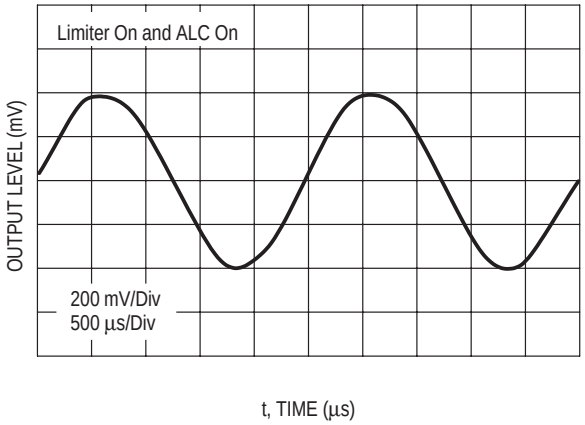


Figure 93. T_X Audio Output Response



PLL SYNTHESIZER SECTION

PLL Frequency Synthesizer General Description

Figure 95 shows a simplified block diagram of the programmable universal dual phase locked loop (PLL) designed into the MC13110A and MC13111A IC. This dual PLL is fully programmable through the MCU serial interface and supports most country channel frequencies including USA (25 ch), Spain, Australia, Korea, New Zealand, U.K., Netherlands, France, and China (see channel frequency tables in AN1575, "Worldwide Cordless Telephone Frequencies").

The 2nd local oscillator and reference divider provide the reference frequency signal for the R_X and T_X PLL loops. The programmed divider value for the reference divider is selected based on the crystal frequency and the desired R_X and T_X reference frequency values. For the U.K., additional divide by 25 and divide by 4 blocks are provided to allow for generation of the 1.0 kHz and 6.2 kHz reference frequencies.

The 14–bit R_X counter is programmed for the desired first local oscillator frequency. The 14–bit T_X counter is programmed for the desired transmit channel frequency. All counters power–up to a set default state for USA channel #21 using a 10.24 MHz reference frequency crystal (see power–up default latch register state in the Serial Programmable Interface section).

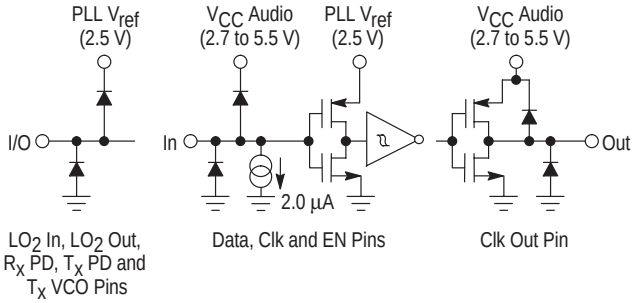
To extend the sensitivity of the 1st LO for U.S. 25 channel operation, internal fixed capacitors can be connected to the tank circuit through microprocessor programmable control. When designing the external PLL loop filters, it is recommended that the T_X and R_X phase detectors be considered as current drive type outputs. The loop filter control voltage must be 0.5 V away from either the positive or negative supply rail.

PLL I/O Pin Configurations

The 2nd LO, R_X and T_X PLL's, and MPU serial interface are powered by the internal voltage regulator at the "PLL V_{ref}" pin. The "PLL V_{ref}" pin is the output of a voltage regulator which is powered from the "V_{CC} Audio" power supply pin. It is regulated by an internal bandgap voltage reference. Therefore, the maximum input and output levels for most of the PLL I/O pins (LO2 In, LO2 Out, R_X PD, T_X PD, T_X VCO) is the regulated voltage at the "PLL V_{ref}" pin. The ESD protection diodes on these pins are also connected to "PLL V_{ref}".

Internal level shift buffers are provided for the pins (Data, Clk, EN, Clk Out) which connect directly to the microprocessor. The maximum input and output levels for these pins is V_{CC}. Figure 94 shows a simplified schematic of the I/O pins.

Figure 94. PLL I/O Pin Simplified Schematics

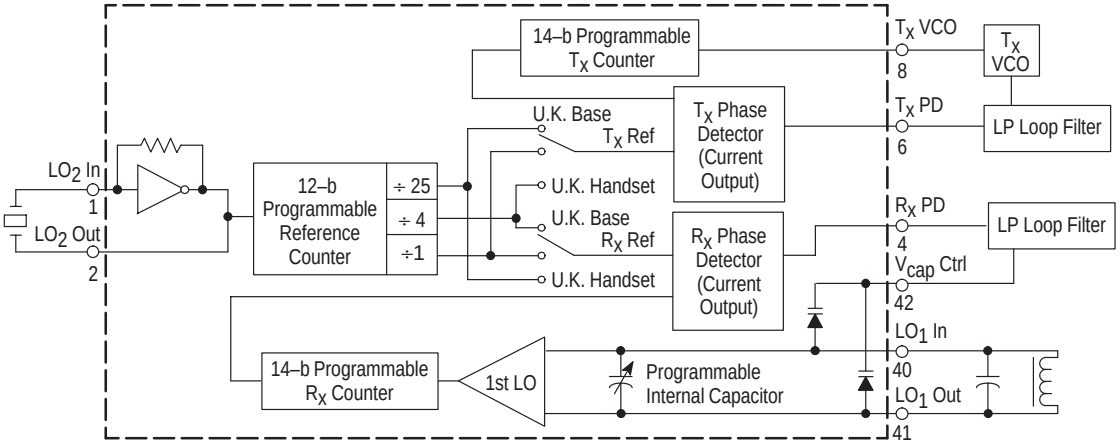


PLL Loop Control Voltage Range

The control voltage for the T_X and R_X loop filters is set by the phase detector outputs which drive the external loop filters. The phase detectors are best considered to have a current mode type output. The output can have three states; ground, high impedance, and positive supply, which in this case is the voltage at "PLL V_{ref}". When the loop is locked the phase detector outputs are at high impedance. An exception of this state is for narrow current pulses, referenced to either the positive or negative supply rails. If the loop voltages get within 0.5 V of either rail the linear current output starts to degrade. The phase detector current source was not designed to operate at the supply rails. VCO tuning range will also be limited by this voltage range

The maximum loop control voltage is the "PLL V_{ref}" voltage which is 2.5 V. If a higher loop control voltage range is desired, the "PLL V_{ref}" pin can be pulled to a higher voltage. It can be tied directly to the V_{CC} voltage (with suitable filter capacitors connected close to each pin). When this is done, the internal voltage regulator is automatically disabled. This is commonly used in the telephone base set where an external 5.0 V regulated voltage is available. It is important to remember, that if "PLL V_{ref}" is tied to V_{CC} and V_{CC} is not a regulated voltage, the PLL loop parameters and lock–up time will vary with supply voltage variation. The phase detector gain constant, K_{pd}, will not be affected if the "PLL V_{ref}" is tied to V_{CC}.

Figure 95. Dual PLL Simplified Block Diagram

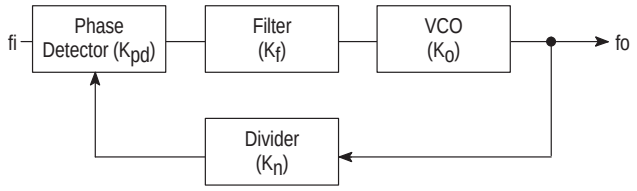


Loop Filter Characteristics

Lets consider the following discussion on loop filters. The fundamental loop characteristics, such as capture range, loop bandwidth, lock–up time, and transient response are controlled externally by loop filtering.

Figure 96 is the general model for a Phase Lock Loop (PLL).

Figure 96. PLL Model



Where:

K_{pd} = Phase Detector Gain Constant
K_f = Loop Filter Transfer Function
K_o = VCO Gain Constant
K_n = Divide Ratio (1/N)
fi = Input frequency
fo = Output frequency
fo/N = Feedback frequency divided by N

From control theory the loop transfer function can be represented as follows:

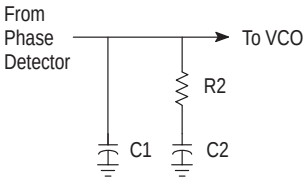
$A = K_{pd}\, K_f\, K_o\, K_n$ Open loop gain

K_{pd} can be either expressed as being 2.5 V/4.0 π or 1.0 mA/2.0 π for the CT–0 circuits. More details about performance of different type PLL loops, refer to Motorola application note AN535.

The loop filter can take the form of a simple low pass filter. A current output, type 2 filter will be used in this discussion since it has the advantage of improved step response, velocity, and acceleration.

The type 2 low pass filter discussed here is represented as follows:

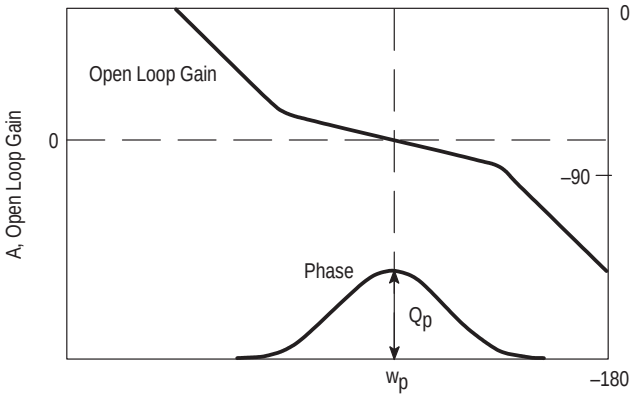
Figure 97. Loop Filter with Additional Integrating Element



From Figure 97, capacitor C1 forms an additional integrator, providing the type 2 response, and filters the discrete current steps from the phase detector output. The function of the additional components R2 and C2 is to create a pole and a zero (together with C1) around the 0 dB point of the open loop gain. This will create sufficient phase margin for stable loop operation.

In Figure 98, the open loop gain and the phase is displayed in the form of a Bode plot. Since there are two integrating functions in the loop, originating from the loopfilter and the VCO gain, the open loop gain response follows a second order slope (–40 dB/dec) creating a phase of –180 degrees at the lower and higher frequencies. The filter characteristic needs to be determined such that it is adding a pole and a zero around the 0 dB point to guarantee sufficient phase margin in this design (Qp in Figure 98).

Figure 98. Bode Plot of Gain and Phase in Open Loop Condition



The open loop gain including the filter response can be expressed as:

$$A_{openloop} = \frac{K_{pd}K_o(1 + jw(R2C2))}{jwK_n\left(jw\left(1 + jw\left(\frac{R2C1C2}{C1+C2}\right)\right)\right)} \quad \textbf{(1)}$$

The two time constants creating the pole and the zero in the Bode plot can now be defined as:

$$T1 = \frac{R2C1C2}{C1 + C2} \qquad T2 = R2C2 \quad \textbf{(2)}$$

By substituting equation (2) into (1), it follows:

$$A_{openloop} = \left(\frac{K_{pd}K_oT1}{w^2C1K_nT2}\right)\left(\frac{1 + jwT2}{1 + jwT1}\right) \quad \textbf{(3)}$$

The phase margin (phase + 180) is thus determined by:

$$Q_p = \arctan(wT2) - \arctan(wT1) \quad \textbf{(4)}$$

At $w=w_p$, the derivative of the phase margin may be set to zero in order to assure maximum phase margin occurs at w_p (see also Figure 98). This provides an expression for w_p:

$$\frac{dQ_p}{dw} = 0 = \frac{T2}{1 + (wT2)^2} - \frac{T1}{1 + (wT1)^2} \quad \textbf{(5)}$$

$$w = w_p = \frac{1}{\sqrt{T2T1}} \quad \textbf{(6)}$$

Or rewritten:

$$T1 = \frac{1}{w_p{}^2T2} \quad \textbf{(7)}$$

By substituting into equation (4), solve for T2:

$$T2 = \frac{\tan\left(\frac{Q_p}{2} + \frac{\pi}{4}\right)}{w_p} \quad \textbf{(8)}$$

By choosing a value for w_p and Q_p, T1 and T2 can be calculated. The choice of Q_p determines the stability of the loop. In general, choosing a phase margin of 45 degrees is a good choice to start calculations. Choosing lower phase margins will provide somewhat faster lock–times, but also generate higher overshoots on the control line to the VCO. This will present a less stable system. Larger values of phase margin provide a more stable system, but also increase lock–times. The practical range for phase margin is 30 degrees up to 70 degrees.

The selection of w_p is strongly related to the desired lock–time. Since it is quite complicated to accurately calculate lock time, a good first order approach is:

$$T_lock \approx \frac{3}{w_p} \quad \textbf{(9)}$$

Equation (9) only provides an order of magnitude for lock time. It does not clearly define what the exact frequency difference is from the desired frequency and it does not show the effect of phase margin. It assumes, however, that the phase detector steps up to the desired control voltage without hesitation. In practice, such step response approach is not really valid. The two input frequencies are not locked. Their phase maybe momentarily zero and force the phase detector into a high impedance mode. Hence, the lock times may be found to be somewhat higher.

In general, w_p should be chosen far below the reference frequency in order for the filter to provide sufficient attenuation at that frequency. In some applications, the reference frequency might represent the spacing between channels. Any feedthrough to the VCO that shows up as a spur might affect adjacent channel rejection. In theory, with the loop in lock, there is no signal coming from the phase detector. But in practice leakage currents will be supplied to both the VCO and the phase detector. The external capacitors may show some leakage, too. Hence, the lower w_p, the better the reference frequency is filtered, but the longer it takes for the loop to lock.

As shown in Figure 98, the open loop gain at w_p is 1 (or 0 dB), and thus the absolute value of the complex open loop gain as shown in equation (3) solves C1:

$$C1 = \left(\frac{K_{pd}K_oT1}{w^2K_nT2}\right)\sqrt{\frac{\left(1 + w_pT2\right)^2}{\left(1 + w_pT1\right)^2}} \quad \textbf{(10)}$$

With C1 known, and equation (2) solve C2 and R2:

$$C2 = C1\left(\frac{T2}{T1} - 1\right) \quad \textbf{(11)}$$

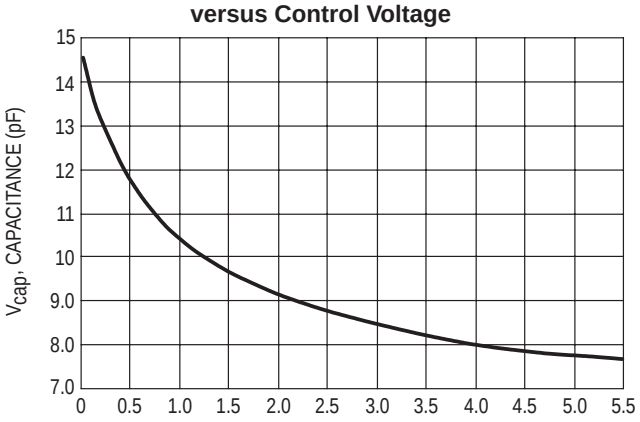
$$R2 = \frac{T2}{C2} \quad \textbf{(12)}$$

The VCO gain is dependent on the selection of the external inductor and the frequency required. The free running frequency of the VCO is determined by:

$$f = \frac{1}{2\pi\sqrt{LC_T}} \quad \textbf{(13)}$$

In which L represents the external inductor value and C_T represents the total capacitance (including internal capacitance) in parallel with the inductor. The VCO gain can be easily calculated via the internal varicap transfer curve shown below.

Figure 99. Varicap Capacitance versus Control Voltage



As can be derived from Figure 99, the varicap capacitance changes 1.3 pF over the voltage range from 1.0 V to 2.0 V:

$$\Delta Cvar = \frac{1.3\ pF}{V} \quad \textbf{(14)}$$

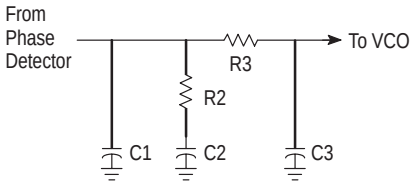
Combining (13) with (14) the VCO gain can be determined by:

$$K_O = \frac{1}{jw}\left\{\frac{1}{2\pi\sqrt{L\left(C_T + \frac{\Delta Cvar}{2}\right)}} - \frac{1}{2\pi\sqrt{L\left(C_T + \frac{\Delta Cvar}{2}\right)}}\right\} \quad \textbf{(15)}$$

Although the basic loopfilter previously described provides adequate performance for most applications, an extra pole may be added for additional reference frequency filtering. Given that the channel spacing in a CT–0 telephone set is based on the reference frequency, and any feedthrough to

the first LO may effect parameters like adjacent channel rejection and intermodulation. Figure 100 shows a loopfilter architecture incorporating an additional pole.

Figure 100. Loop Filter with Additional Integrating Element



For the additional pole formed by R3 and C3 to be efficient, the cut–off frequency must be much lower than the reference frequency. However, it must also be higher than w_p in order not to compromise phase margin too much. The following equations were derived in a similar manner as for the basic filter previously described.

Similarly, it can be shown:

$$A_{openloop} = -\frac{K_{pd}K_o}{K_n w^2\left((C1 + C2 + C3) - w^2 C1C2C3R2R3\right)} + \frac{1 + jwT2}{1 + jwT1} \quad \textbf{(16)}$$

In which:

$$T1 = \frac{(C1 + C2)T2 + (C1C2)T3}{C1 + C2 + C3 - w^2 C1T2T3} \quad \textbf{(17)}$$

$$T2 = R2C2 \quad \textbf{(18)} \qquad T3 = R3C3 \quad \textbf{(19)}$$

From T1 it can be derived that:

$$C2 = \frac{(T1 + T2)C3 - C1\left(T2 + T3 - T1 + w^2 T1T2T3\right)}{T3 - T1} \quad \textbf{(20)}$$

In analogy with (10), by forcing the loopgain to 1 (0 dB) at w_p, we obtain:

$$C1(T1 + T2) + C2T3 + C3T2 = \left(\frac{K_{pd}K_o}{K_n {w_p}^2}\right)\sqrt{\frac{1 + \left(w_pT2\right)^2}{1 + \left(w_pT1\right)^2}} \quad \textbf{(21)}$$

Solving for C1:

$$C1 = \frac{(T2 - T1)T3C3 - (T3 - T1)T2C3 + (T3 - T1)\left(\frac{K_{pd}K_oT1}{{w_p}^2K_n}\right)\sqrt{\frac{1+\left(w_pT2\right)^2}{1+\left(w_pT1\right)^2}}}{(T3 - T1)T2 + (T3 - T1)T3 - \left(T2 + T3 - T1 + {w_p}^2T1T2T3\right)T3} \quad \textbf{(22)}$$

By selecting w_p via (9), the additional time constant expressed as T3, can be set to:

$$T3 = \frac{1}{Kw_p} \quad \textbf{(23)}$$

The K–factor shown determines how far the additional pole frequency will be separated from w_p. Selecting too small of a K–factor, the equations may provide negative capacitance or resistor values. Too large of a K–factor may not provide the maximum attenuation.

By selecting R3 to be 100 kΩ, C3 becomes known and C1 and C2 can be solved from the equations. By using equations (8) and (7), time constants T2 and T1 can be derived by selecting a phase margin. Finally, R2 follows from T2 and C2.

The following pages, the loopfilter components are determined for both handset and baseset the US application based on the equations described. Choose K to be approximately five times w_p ($5w_p$).

In an application, w_p is chosen to be 20 times less than the reference frequency of 5.0 kHz and the phase margin has been set to 45 degrees. This provides a lock time according to (9) of about 2.0 ms (order of magnitude). With the adjacent channels spaced at least 15 kHz away, reference feedthrough at w_p will not be directly disastrous but still, the additional pole may be added in the loopfilter design for added safety.

In an application, w_p is chosen to be 20 times less than the reference frequency of 5.0 kHz and the phase margin has been set to 45 degrees. This provides a lock time according to (9) of about 2.0 ms (order of magnitude). With the adjacent channels spaced at least 15 kHz away, reference feedthrough at w_p will not be directly disastrous but still, the additional pole may be added in the loopfilter design for added safety.

Figure 101. Open Loop Response Handset US with Selected Values

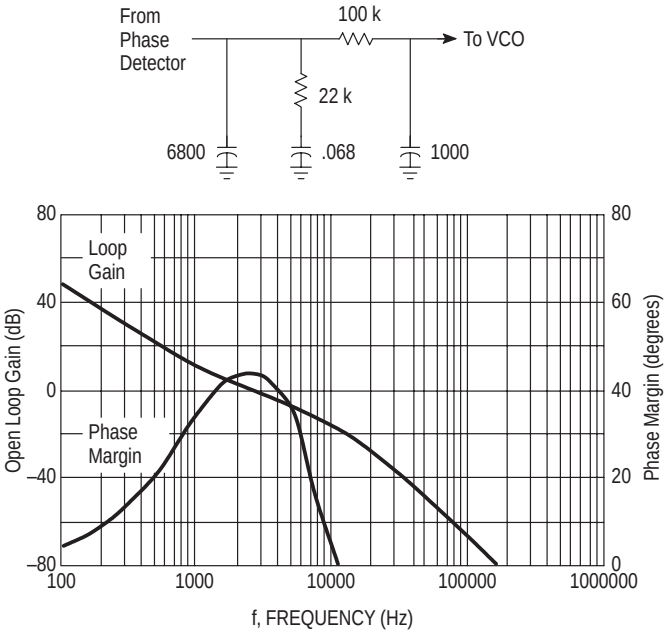


Figure 102. Open Loop Response Baseset US with Selected Values

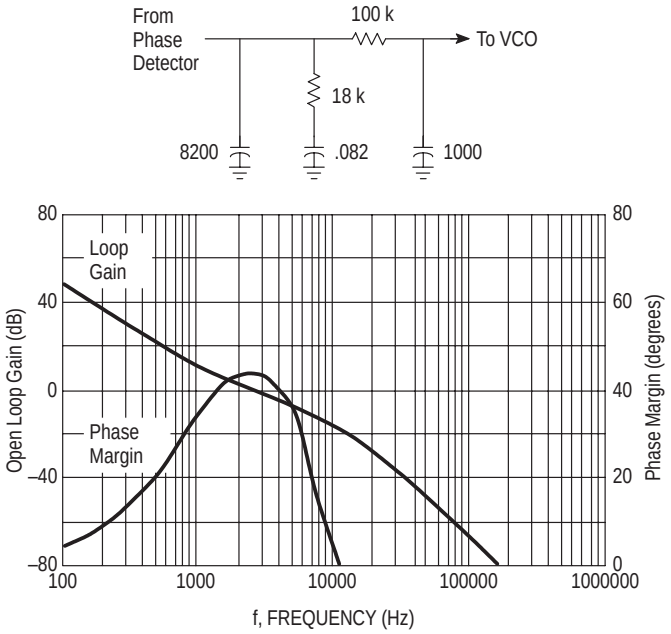


Figure 103. Handset US

Conditions		
L = 470 uH	F_{ref} = 5.0 kHz	
RF = 46.77 MHz	Q_p = 45 degrees	
VCO center = 36.075 MHz	$w_p = w_{ref}$ / 20 radians	
Results	**Equations**	**Select**
K_{pd} = 159.2 uA/rad		
K_{VCO} = 3.56 Mrad/V	(14), (15)	
T2 = 1540 µs	(8)	
T1 = 264 µs	(7)	
T3 = 91 µs	with K = 7	
C1 = 7.6 nF	(21)	C1 = 6.8 nF
C2 = 70.9 nF	(20)	C2 = 68 nF
R2 = 21.7 kΩ	(18)	R2 = 22 kΩ
R3 = 100 kΩ	choose:	R3 = 100 kΩ
C3 = 909.5 pF	(19)	C3 = 1 nf

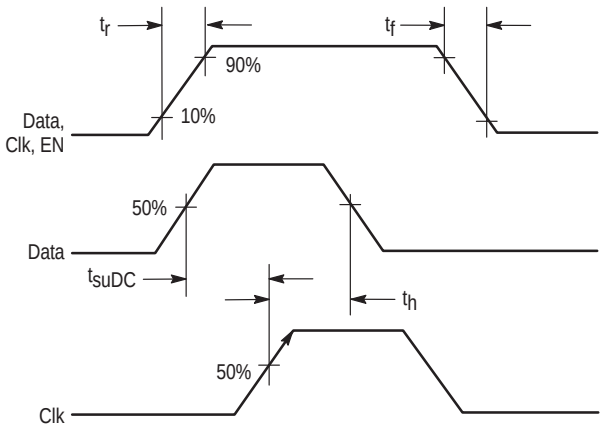
Figure 104. Baseset US

Conditions		
L = 470 uH	F_{ref} = 5.0 kHz	
RF = 49.83 MHz	Q_p = 45 degrees	
VCO center = 39.135 MHz	$w_p = w_{ref}$ / 20 radians	
Results	**Equations**	**Select**
K_{pd} = 159.2 uA/rad		
K_{VCO} = 4.54 Mrad/V	(14), (15)	
T2 = 1540 µs	(8)	
T1 = 264 µs	(7)	
T3 = 91 µs	with K = 7	
C1 = 9.1 nF	(21)	C1 = 8.2 nF
C2 = 83.5 nF	(20)	C2 = 82 nF
R2 = 18.4 kΩ	(18)	R2 = 18 kΩ
R3 = 100 kΩ	choose:	R3 = 100 kΩ
C3 = 909.5 pF	(19)	C3 = 1 nf

Microprocessor Serial Interface

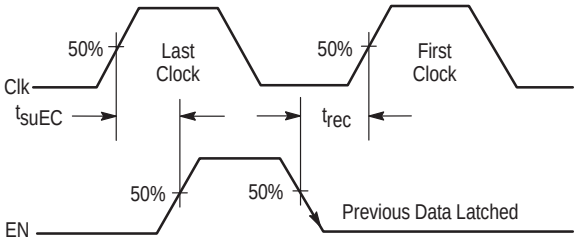
The Data, Clock, and Enable (“Data”, “Clk”, and “EN” respectively) pins provide a MPU serial interface for programming the reference counters, the transmit and receive channel divide counters, the switched capacitor filter clock counter, and various other control functions. The “Data” and “Clk” pins are used to load data into the MC13111A shift register (Figure 109). Figure 105 shows the timing required on the “Data” and “Clk” pins. Data is clocked into the shift register on positive clock transitions.

Figure 105. Data and Clock Timing Requirement



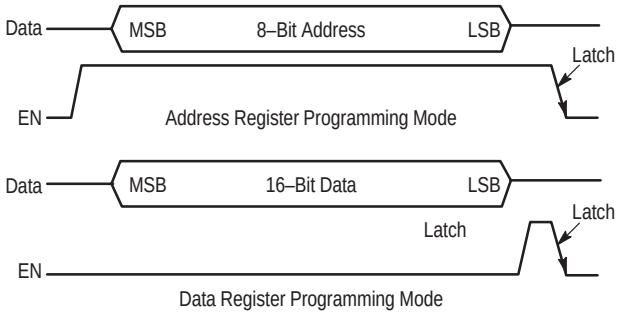
After data is loaded into the shift register, the data is latched into the appropriate latch register using the “EN” pin. This is done in two steps. First, an 8–bit address is loaded into the shift register and latched into the 8–bit address latch register. Then, up to 16–bits of data is loaded into the shift register and latched into the data latch register. It is specified by the address that was previously loaded. Figure 106 shows the timing required on the EN pin. Latching occurs on the negative EN transition.

Figure 106. Enable Timing Requirement



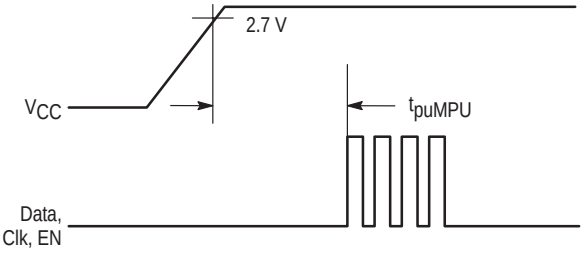
The state of the “EN” pin when clocking data into the shift register determines whether the data is latched into the address register or a data register. Figure 107 shows the address and data programming diagrams. In the data programming mode, there must not be any clock transitions when “EN” is high. The clock can be in a high state (default high) or a low state (default low) but must not have any transitions during the “EN” high state. The convention in these figures is that latch bits to the left are loaded into the shift register first. A minimum of four “Clk” rising edge transition must occur before a negative “EN” transition will latch data or an address into a register.

Figure 107. Microprocessor Interface Programming Mode Diagrams



The MPU serial interface is fully operational within 100 μs after the power supply has reached its minimum level during power–up (see Figure 108). The MPU Interface shift registers and data latches are operational in all four power saving modes; Inactive, Standby, R_X, and Active Modes. Data can be loaded into the shift registers and latched into the latch registers in any of the operating modes.

Figure 108. Microprocessor Serial Interface Power–Up Delay



Data Registers

Figure 109 shows the data latch registers and addresses which are used to select each of each registers. Latch bits to the left (MSB) are loaded into the shift register first. The LSB bit must always be the last bit loaded into the shift register. Bits proceeding the register must be “0’s” as shown.

Power–Up Defaults for Data Registers

When the IC is first powered up, all latch registers are initialized to a defined state. The device is initially placed in the R_X mode with all mutes active. The reference counter is set to generate a 5.0 kHz reference frequency from a 10.24 MHz crystal. The switched capacitor filter clock counter is set properly for operation with a 10.24 MHz crystal. The T_X and R_X counter registers are set for USA handset channel frequency, number 21 (Channel 6 for previous FCC 10 Channel Band). Figure 110 shows the initial power–up states for all latch registers.

Figure 109. Microprocessor Interface Data Latch Registers

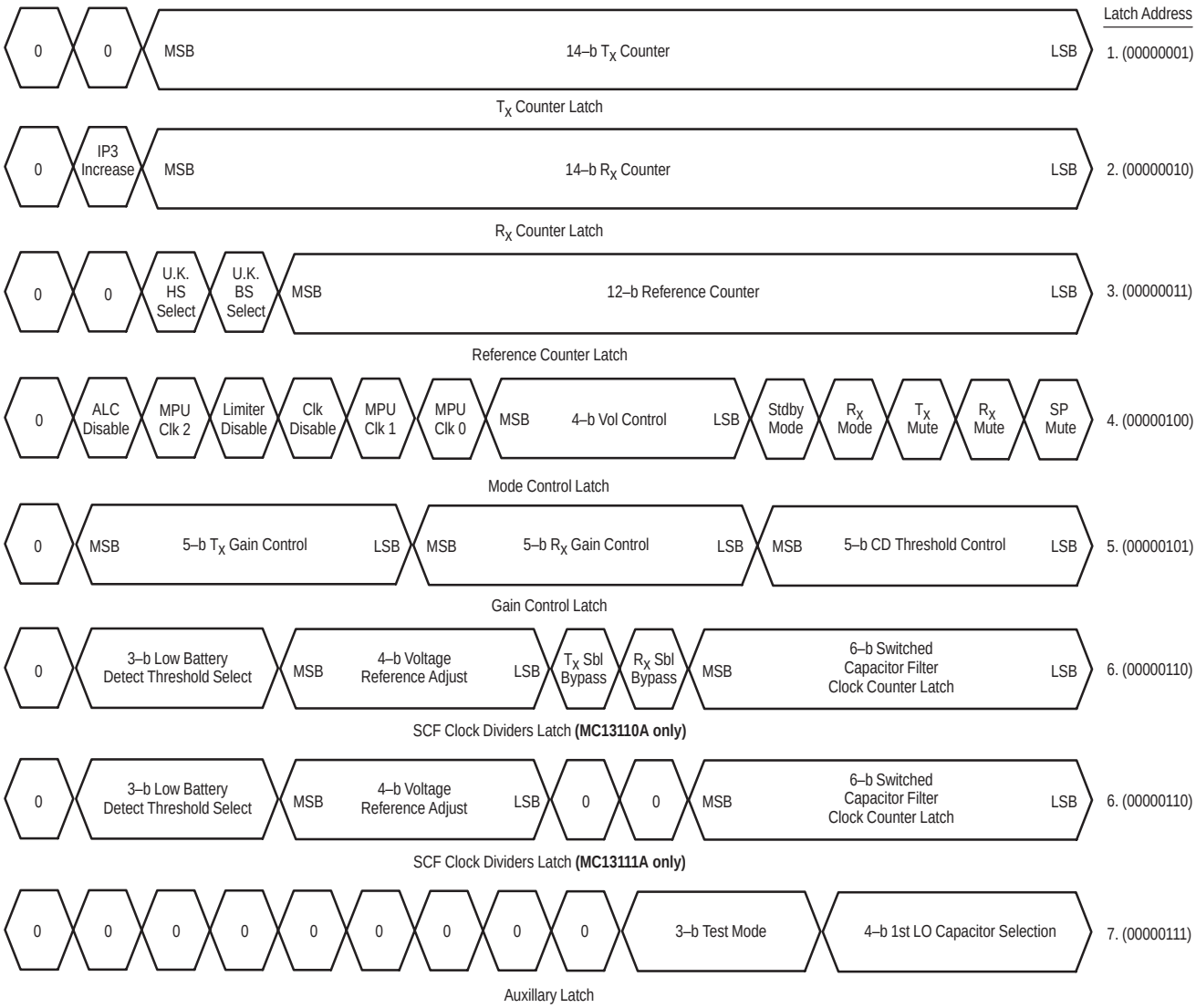


Figure 110. Latch Register Power–Up Defaults

Register	Count	MSB								LSB							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_X	9966	–	–	1	0	0	1	1	0	1	1	1	0	1	1	1	0
R_X	7215	–	–	0	1	1	1	0	0	0	0	1	0	1	1	1	1
Ref	2048	–	–	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Mode	N/A	–	0	0	0	0	1	1	0	1	1	1	0	1	1	1	1
Gain	N/A	–	0	1	1	1	1	0	1	1	1	1	1	0	1	0	0
SCF (MC13110A)	31	–	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1
SCF (MC13111A)	31	–	0	0	0	0	1	1	1	–	–	0	1	1	1	1	1
Aux	N/A	–	–	–	–	–	–	–	–	–	0	0	0	0	0	0	0

NOTE: 12. Bits 6 and 7 in the SCF latch register are ”Don’t Cares” for the MC13111A since this part does not have a scrambler.

T_X and R_X Counter Registers

The 14 bit T_X and R_X counter registers are used to select the transmit and receive channel frequencies. In the R_X counter there is an “IP3 Increase” bit that allows the ability to trade off increased receiver mixer performance versus reduced power consumption. With “IP3 increase” = <1>, there is about a 10 dB improvement in 1 dB compression and 3rd order intercept for both the 1st and 2nd mixers. However, there is also an increase in power supply current of 1.3 mA. The power–up default for the MC13111A is “IP3 Increase” = <0>. The register bits are shown in Figure 111.

Reference Counter Register

Reference Counter

Figure 113 shows how the reference frequencies for the R_X and T_X loops are generated. All countries except the U.K. require that the T_X and R_X reference frequencies be identical. In this case, set “U.K. Base Select” and “U.K. Handset Select” bits to “0”. Then the fixed divider is set to “1” and the T_X and R_X reference frequencies will be equal to the crystal oscillator frequency divided by the programmable reference counter value.

The U.K. is a special case which requires a different reference frequency value for T_X and R_X. For U.K. base operation, set “U.K. Base Select” to “1”. For U.K. handset operation, set “U.K. Handset Select” to “1”. The Netherlands is also a special case. A 2.5 kHz reference frequency is used for both the T_X and R_X reference and the total divider value required is 4096. This is larger than the maximum divide value available from the 12–bit reference divider (4095). In this case, set “U.K. Base Select” to “1” and set “U.K. Handset Select” to “1”. This will give a fixed divide by 4 for both the T_X and R_X reference. Then set the reference divider to 1024 to get a total divider of 4096.

Figure 111. R_X and T_X Counter Register Latch Bits

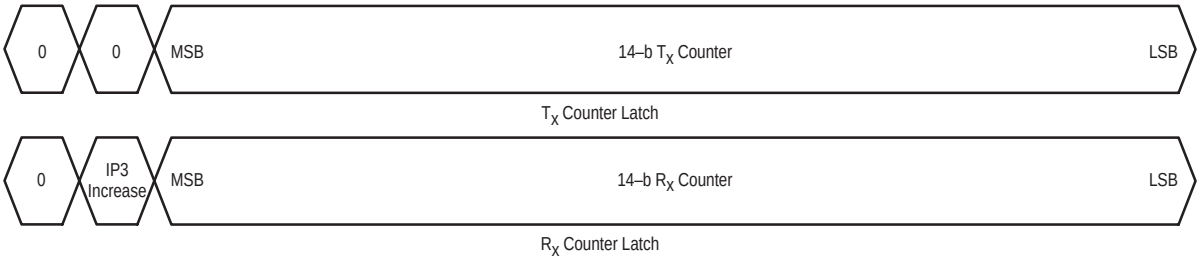
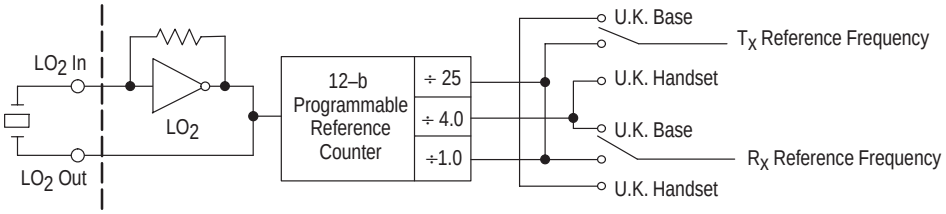


Figure 112. Reference Counter Register



Figure 113. Reference Counter Register Programming Mode

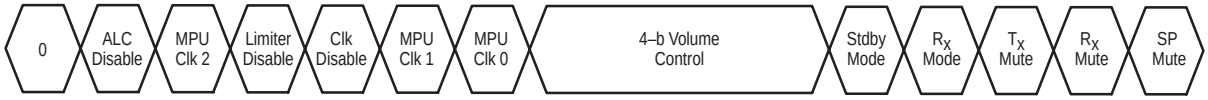


U.K. Handset Select	U.K. Base Select	T_X Divider Value	R_X Divider Value	Application
0	0	1	1	All but U.K. and Netherlands
0	1	25	4	U.K. Base Set
1	0	4	25	U.K. Hand Set
1	1	4	4	Netherlands Base and Hand Set

Figure 114. Reference Frequency and Divider Values

MC13110A / MC13111A							
Crystal Frequency	**Reference Divider Value**	**U.K. Base/ Handset Divider**	**Reference Frequency**	**SC Filter Clock Divider**	**SC Filter Clock Frequency**	**Scrambler Modulation Divider**	**Scrambler Modulation Frequency**
10.24 MHz	2048	1	5.0 kHz	31	165.16 kHz	40	4.129 kHz
10.24 MHz	1024	4	5.0 kHz	31	165.16 kHz	40	4.129 kHz
11.15 MHz	2230	1	5.0 kHz	34	163.97 kHz	40	4.099 kHz
12.00 MHz	2400	1	5.0 kHz	36	166.67 kHz	40	4.167 kHz
11.15 MHz	1784	1	6.25 kHz	34	163.97 kHz	40	4.099 kHz
11.15 MHz	446	4	6.25 kHz	34	163.97 kHz	40	4.099 kHz
11.15 MHz	446	25	1.0 kHz	34	163.97 kHz	40	4.099 kHz

Figure 115. Mode Control Register



Reference Frequency Selection

The "LO_2 In" and "LO_2 Out" pins form a reference oscillator when connected to an external parallel–resonant crystal. The reference oscillator is also the second local oscillator for the RF Receiver. Figure 114 shows the relationship between different crystal frequencies and reference frequencies for cordless phone applications in various countries. "LO_2 In" may also serve as an input for an externally generated reference signal which is ac–coupled. The switched capacitor filter 6–bit programmable counter must be programmed for the crystal frequency that is selected since this clock is derived from the crystal frequency and must be held constant regardless of the crystal that is selected. The actual switched capacitor clock divider ratio is twice the programmed divider ratio due to the a fixed divide by 2.0 after the programmable counter. The scrambler mixer modulation frequency is the switched capacitor clock divided by 40 for the MC13110A.

Mode Control Register

The power saving modes; mutes, disables, volume control, and microprocessor clock output frequency are all set by the Mode Control Register. Operation of the Control Register is explained in Figures 115 through 119.

Figure 116. Mute and Disable Control Bit Descriptions

ALC Disable	1 0	Automatic Level Control Disabled Normal Operation
T_X Limiter Disable	1 0	T_X Limiter Disabled Normal Operation
Clock Disable (MC13110A/111A)	1 0	MPU Clock Output Disabled Normal Operation
T_X Mute	1 0	Transmit Channel Muted Normal Operation
R_X Mute	1 0	Receive Channel Muted Normal Operation
SP Mute	1 0	Speaker Amp Muted Normal Operation

Power Saving Operating Modes

When the MC13110A or MC13111A are used in a handset, it is important to conserve power in order to prolong battery life. There are five modes of operation for the MC13110A/MC13111A; Active, R_X, Standby, Interrupt, and Inactive. They are Active, R_X, and Standby. In the Active mode, all circuit blocks are powered. In the R_X mode, all circuitry is powered down except for those circuit sections needed to receive a transmission from the base. In the Standby and Interrupt Modes, all circuitry is powered down except for the circuitry needed to provide the clock output for the microprocessor. In the Inactive Mode, all circuitry is powered down except the MPU serial interface. Latch memory is maintained in all modes. Figure 118 shows the control register bit values for selection of each power saving mode and Figure 118 shows the circuit blocks which are powered in each of these operating modes.

Figure 117. Power Saving Mode Selection

Stdby Mode Bit	R_X Mode Bit	"CD Out/ Hardware Interrupt" Pin	Power Saving Mode
MC13110A/MC13111A			
0	0	X	Active
0	1	X	R_X
1	0	X	Standby
1	1	1 or High Impedance	Inactive
1	1	0	Interrupt
MC13110B/MC13111B [Note 14]			
0	0	X	Active
0	1	X	R_X
1	X	X	Standby
1	1	0	Interrupt

NOTES: 13. "X" is a don't care
14. MPU Clock Out is "Always On"

Figure 118. Circuit Blocks Powered During Power Saving Modes

Circuit Blocks	MC13110A/MC13111A			
	Active	R_X	Standby	Inactive
"PLL V_{ref}" Regulated Voltage	X	X	X[1]	X[1, 2]
MPU Serial Interface	X	X	X	X[2]
2nd LO Oscillator	X	X	X	
MPU Clock Output	X	X	X	
RF Receiver and 1st LO VCO	X	X		
R_X PLL	X	X		
Carrier Detect	X	X		
Data Amp	X	X		
Low Battery Detect	X	X		
T_X PLL	X			
R_X and T_X Audio Paths	X			

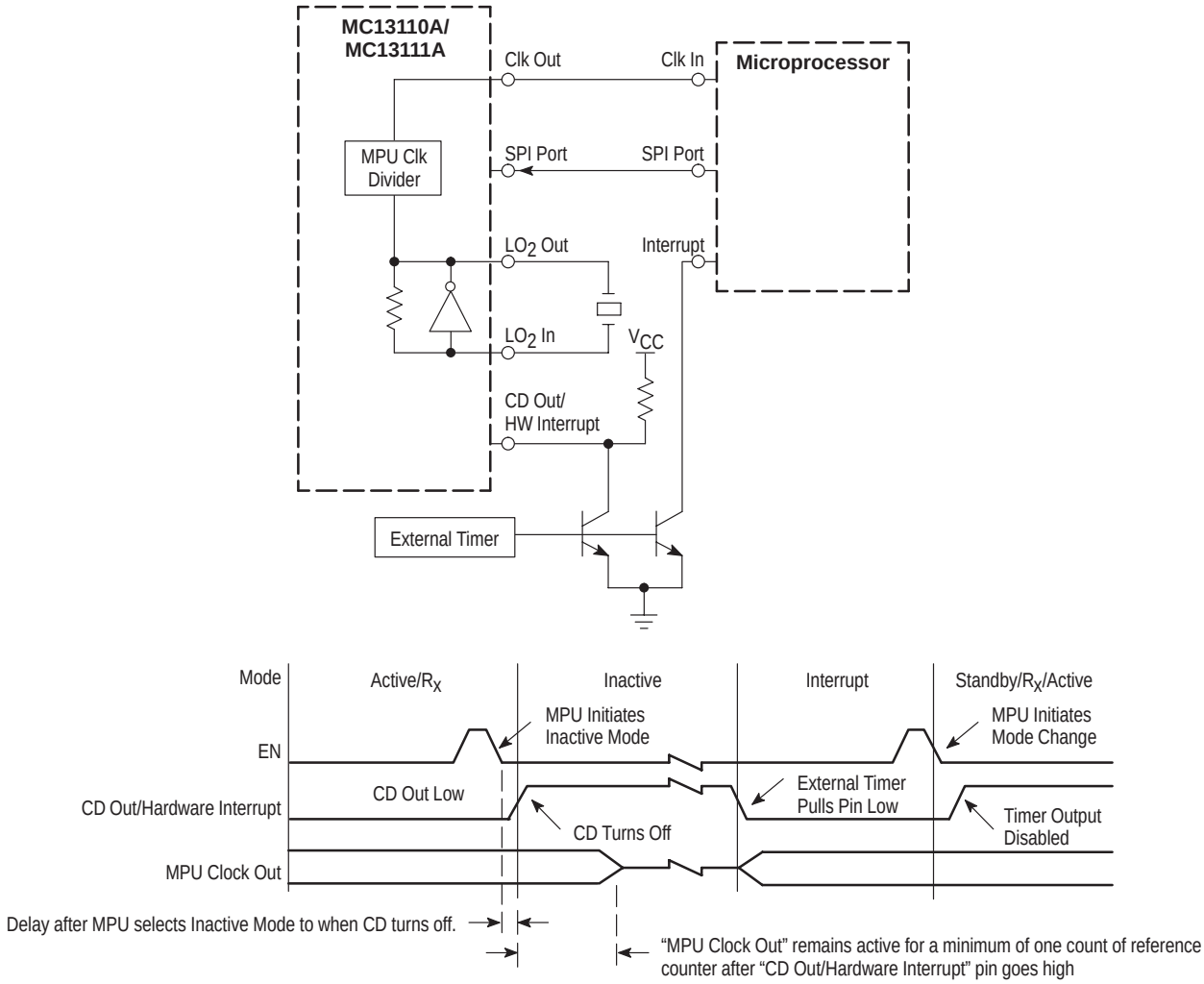
NOTE: 15. In Standby and Inactive Modes, "PLL V_{ref}" remains powered but is not regulated. It will fluctuate with V_{CC}.

Power Saving Application

In some handset applications it may be desirable to power down all circuitry including the microprocessor (MPU). First put the MC13110A/MC13111A into the Inactive mode. This turns off the MPU Clock Output (see Figure 119) and disables the microprocessor. Once a command is given to switch the IC into an "Inactive" mode, the MPU Clock output will remain active for a minimum of one reference counter cycle (about 200 μs) and up to a maximum of two reference counter cycles (about 400 μs). This is performed in order to give the MPU adequate time to power down.

An external timing circuit should be used to initiate the turn–on sequence. The "CD Out" pin has a dual function. In the Active and R_X modes it performs the carrier detect function. In the Standby and Inactive modes the carrier detect circuit is disabled and the "CD Out" pin is in a "High" state, because of an external pull–up resistor. In the Inactive mode, the "CD Out" pin is the input for the hardware interrupt function. When the "CD Out" pin is pulled "low", by the external timing circuit, the IC switches from the Inactive to the Interrupt mode. Thereby turning on the MPU Clock Output. The MPU can then resume control of the IC. The "CD Out" pin must remain low until the MPU changes the operating mode from Interrupt to Standby, Active, or R_X modes.

Figure 119. Power Saving Application



MPU "Clk Out" Divider Programming

The "Clk Out" signal is derived from the second local oscillator. It can be used to drive a microprocessor (MPU) clock input. This will eliminate the need for a separate crystal to drive the MPU, thus reducing system cost. Figure 120 shows the relationship between the second LO crystal frequency and the clock output for each divide value. Figure 121 shows the "Clk Out" register bit values. With a 10.24 MHz crystal, the divide by 312.5 gives the same clock frequency as a clock crystal and allows the MPU to display the time on a LCD display without additional external components.

Figure 120. Clock Output Values

Crystal Frequency	Clock Output Divider							
	2	2.5	3	4	5	20	80	312.5
10.24 MHz	5.120 MHz	4.096 MHz	3.413 MHz	2.560 MHz	2.048 MHz	512 kHz	128 kHz	32.768 kHz
11.15 MHz	5.575 MHz	4.460 MHz	3.717 MHz	2.788 MHz	2.230 MHz	557 kHz	139 kHz	35.680 kHz
12.00 MHz	6.000 MHz	4.800 MHz	4.000 MHz	3.000 MHz	2.400 MHz	600 kHz	150 kHz	38.400 kHz

Figure 121. Clock Output Divider

MPU Clk Bit #2	MPU Clk Bit #1	MPU Clk Bit #0	Clk Out Divider Value
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	2.5
1	0	1	20
1	1	0	80
1	1	1	312.5

MPU "Clk Out" Power–Up Default Divider Value

The power–up default divider value is "divide by 5". This provides a MPU clock of about 2.0 MHz after initial power–up. The reason for choosing a relatively low clock frequency at initial power–up is because some microprocessors operate using a 3.0 V power supply and have a maximum clock frequency of 2.0 MHz. After initial power–up, the MPU can change the clock divider value and set the clock to the desired operating frequency. Special care was taken in the design of the clock divider to insure that the transition between one clock divider value and another is "smooth" (i.e. there will be no narrow clock pulses to disturb the MPU).

MPU "Clk Out" Radiated Noise on Circuit Board

The clock line running between the MC13110A or MC13111A and the microprocessor has the potential to radiate noise. Problems in the system can occur, especially if the clock is a square wave digital signal with large high frequency harmonics. In order to minimize the radiated noise, a 1000 Ω resistor is included on–chip in series with the "Clk Out" output driver. A small capacitor or inductor with a capacitor can be connected to the "Clk Out" line on the PCB to form a one or two pole low pass filter. This filter should significantly reduce noise radiated by attenuating the high frequency harmonics on the signal line. The filter can also be used to attenuate the signal level so that it is only as large as required by the MPU clock input. To further reduce radiated noise, the PCB signal trace length should be kept to a minimum.

Volume Control Programming

The volume control adjustable gain block can be programmed in 2 dB gain steps from –14 dB to +16 dB. The power–up default value for the MC13110A and MC13111A is 0 dB. (see Figure 122)

Figure 122. Volume Control

Volume Control Bit #3	Volume Control Bit #2	Volume Control Bit #1	Volume Control Bit #0	Volume Control #	Gain/Attenuation Amount
0	0	0	0	0	–14 dB
0	0	0	1	1	–12 dB
0	0	1	0	2	–10 dB
0	0	1	1	3	–8 dB
0	1	0	0	4	–6 dB
0	1	0	1	5	–4 dB
0	1	1	0	6	–2 dB
0	1	1	1	7	0 dB
1	0	0	0	8	2 dB
1	0	0	1	9	4 dB
1	0	1	0	10	6 dB
1	0	1	1	11	8 dB
1	1	0	0	12	10 dB
1	1	0	1	13	12 dB
1	1	1	0	14	14 dB
1	1	1	1	15	16 dB

Gain Control Register

The gain control register contains bits which control the T_X Voltage Gain, R_X Voltage Gain, and Carrier Detect threshold. Operation of these latch bits are explained in Figures 123, 124 and 125.

T_X and R_X Gain Programming

The T_X and R_X audio signal paths each have a programmable gain block. If a T_X or R_X voltage gain, other than the nominal power–up default, is desired, it can be programmed through the MPU interface. Alternately, these programmable gain blocks can be used during final test of the telephone to electronically adjust for gain tolerances in the telephone system (see Figure 124). In this case, the T_X and R_X gain register values should be stored in ROM during final test so that they can be reloaded each time the IC is powered up.

Figure 123. Gain Control Latch Bits

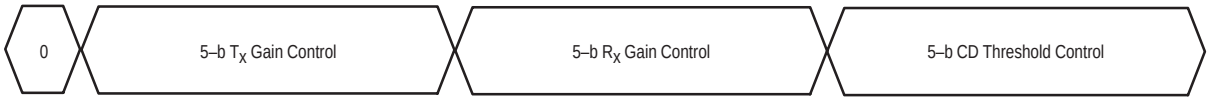


Figure 124. T_X and R_X Gain Control

Gain Control Bit #4	Gain Control Bit #3	Gain Control Bit #2	Gain Control Bit #1	Gain Control Bit #0	Gain Control #	Gain/Attenuation Amount
–	–	–	–	–	<6	–9 dB
0	0	1	1	0	6	–9 dB
0	0	1	1	1	7	–8 dB
0	1	0	0	0	8	–7 dB
0	1	0	0	1	9	–6 dB
0	1	0	1	0	10	–5 dB
0	1	0	1	1	11	–4 dB
0	1	1	0	0	12	–3 dB
0	1	1	0	1	13	–2 dB
0	1	1	1	0	14	–1 dB
0	1	1	1	1	15	0 dB
1	0	0	0	0	16	1 dB
1	0	0	0	1	17	2 dB
1	0	0	1	0	18	3 dB
1	0	0	1	1	19	4 dB
1	0	1	0	0	20	5 dB
1	0	1	0	1	21	6 dB
1	0	1	1	0	22	7 dB
1	0	1	1	1	23	8 dB
1	1	0	0	0	24	9 dB
1	1	0	0	1	25	10 dB
–	–	–	–	–	>25	10 dB

Carrier Detect Threshold Programming

The “CD Out” pin gives an indication to the microprocessor if a carrier signal is present on the selected channel. The nominal value and tolerance of the carrier detect threshold is given in the carrier detect specification section of this document. If a different carrier detect threshold value is desired, it can be programmed through the MPU interface as shown in Figure 125 below. Alternately, the carrier detect threshold can be electronically adjusted during final test of the telephone to reduce the tolerance of the carrier detect threshold. This is done by measuring the threshold and then by adjusting the threshold through the MPU interface. In this case, it is necessary to store the carrier detect register value in ROM so that the CD register can be reloaded each time the combo IC is powered up. If a preamp is used before the first mixer it may be desirable to scale the carrier detect range by connecting an external resistor from the “RSSI” pin to ground. The internal resistor is 187 kΩ.

Figure 125. Carrier Detect Threshold Control

CD Bit #4	CD Bit #3	CD Bit #2	CD Bit #1	CD Bit #0	CD Control #	Carrier Detect Threshold
0	0	0	0	0	0	–20 dB
0	0	0	0	1	1	–19 dB
0	0	0	1	0	2	–18 dB
0	0	0	1	1	3	–17 dB
0	0	1	0	0	4	–16 dB
0	0	1	0	1	5	–15 dB
0	0	1	1	0	6	–14 dB
0	0	1	1	1	7	–13 dB
0	1	0	0	0	8	–12 dB
0	1	0	0	1	9	–11 dB
0	1	0	1	0	10	–10 dB
0	1	0	1	1	11	–9 dB
0	1	1	0	0	12	–8 dB
0	1	1	0	1	13	–7 dB
0	1	1	1	0	14	–6 dB
0	1	1	1	1	15	–5 dB
1	0	0	0	0	16	–4 dB
1	0	0	0	1	17	–3 dB
1	0	0	1	0	18	–2 dB
1	0	0	1	1	19	–1 dB
1	0	1	0	0	20	0 dB
1	0	1	0	1	21	1 dB
1	0	1	1	0	22	2 dB
1	0	1	1	1	23	3 dB
1	1	0	0	0	24	4 dB
1	1	0	0	1	25	5 dB
1	1	0	1	0	26	6 dB
1	1	0	1	1	27	7 dB
1	1	1	0	0	28	8 dB
1	1	1	0	1	29	9 dB
1	1	1	1	0	30	10 dB
1	1	1	1	1	31	11 dB

Clock Divider/Voltage Adjust Register

This register controls the divider value for the programmable switched capacitor filter clock divider, the low battery detect threshold select, the voltage reference adjust, and the scrambler bypass mode (MC13110A only). Operation is explained in Figures 126 through 133. Figure 128 describes the operation of the Tx and Rx Audio bits. Note the power–up default bit is set to <0>, which is the scrambler bypass mode.

Low Battery Detect

The low battery detect circuit can be operated in programmable and non–programmable threshold modes. The non–programmable threshold mode is only available in the 52 QFP package. In this mode, there are two low battery detect comparators and the threshold values are set by external resistor dividers which are connected to the REF1 and REF2 pins. In the programmable threshold mode, several different threshold levels may be selected through the “Low Battery Detect Threshold Register” as shown in Figure 127. The power–on default value for this register is <0,0,0> and is the non–programmable mode. Figure 129 shows equivalent schematics for the programmable and non–programmable operating modes.

Figure 126. Clock Divider/Voltage Adjust Latch Bits

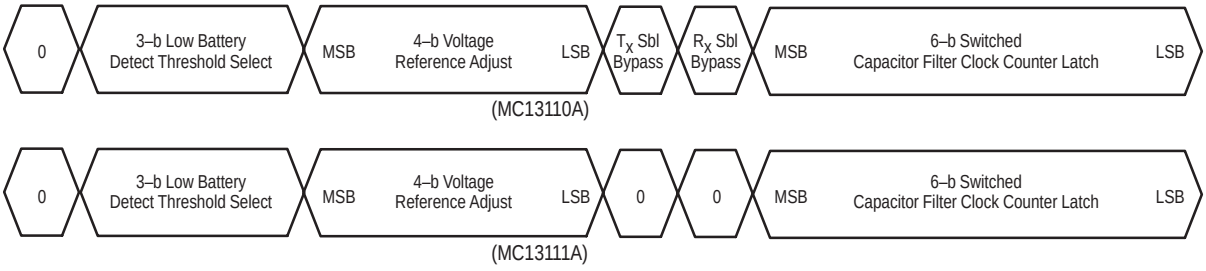


Figure 127. Low Battery Detect Threshold Selection

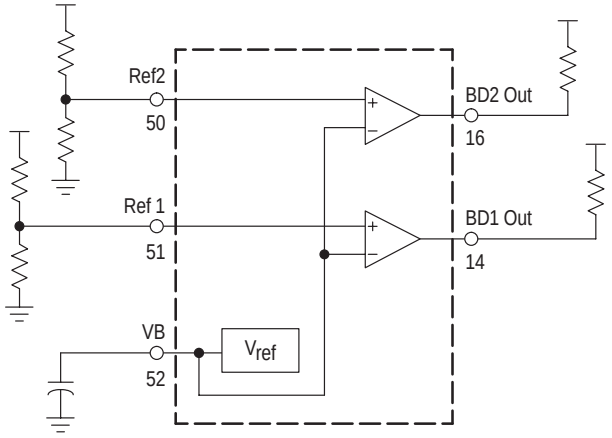
Low Battery Detect Threshold Select Bit #2	Low Battery Detect Threshold Select Bit #1	Low Battery Detect Threshold Select Bit #0	Select #	Operating Mode	Nominal Low Battery Detect Threshold Value (V)
0	0	0	0	Non–Programmable	N/A
0	0	1	1	Programmable	2.850
0	1	0	2	Programmable	2.938
0	1	1	3	Programmable	3.025
1	0	0	4	Programmable	3.200
1	0	1	5	Programmable	3.288
1	1	0	6	Programmable	3.375
1	1	1	7	Programmable	3.463

NOTE: 17. Nominal Threshold Value is before electronic adjustment.

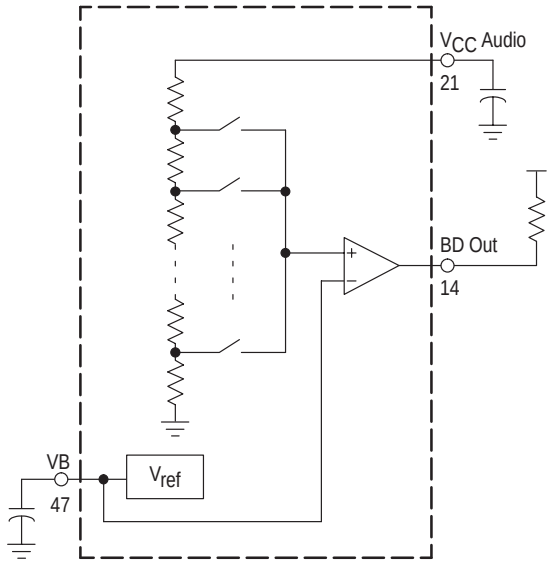
Figure 128. MC13110A Bypass Mode Bit Description (MC13110A Only)

T_X Scrambler Bypass	1	T_X Scrambler Post–Mixer LPF and Mixer Bypassed
	0	Normal Operation with T_X Scrambler
R_X Scrambler Bypass	1	R_X Scrambler Post–Mixer LPF and Mixer Bypassed
	0	Normal Operation R_X Scrambler

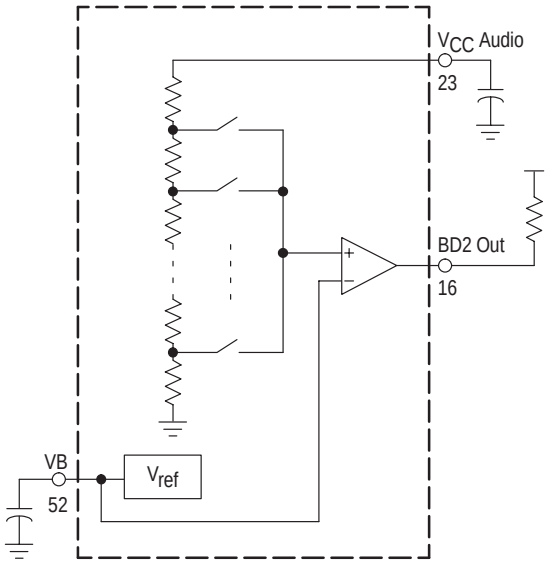
Figure 129. Low Battery Detect Equivalent Schematics



Non–Programmable Threshold Mode: 52–QFP Package



Programmable Threshold Mode: 48–LQFP Package



Programmable Threshold Mode: 52–QFP Package

Voltage Reference Adjustment

An internal 1.5 V bandgap voltage reference provides the voltage reference for the "BD_1 Out" and "BD_2 Out" low battery detect circuits, the "PLL V_{ref}" voltage regulator, the "V_B" reference, and all internal analog ground references. The initial tolerance of the bandgap voltage reference is ±6%. The tolerance of the internal reference voltage can be improved to ±1.5% through MPU serial interface programming. During final test of the telephone, the battery detect threshold is measured. Then, the internal reference voltage value is adjusted electronically through the MPU serial interface to achieve the desired accuracy level. The voltage reference register value should be stored in ROM during final test so that it can be reloaded each time the MC13110A or MC13111A is powered up (see Figure 130).

Figure 130. Bandgap Voltage Reference Adjustment

V_{ref}Adj. Bit #3	V_{ref}Adj. Bit #2	V_{ref}Adj. Bit #1	V_{ref}Adj. Bit #0	V_{ref}Adj. #	V_{ref} Adj. Amount
0	0	0	0	0	–9.0%
0	0	0	1	1	–7.8%
0	0	1	0	2	–6.6%
0	0	1	1	3	–5.4%
0	1	0	0	4	–4.2%
0	1	0	1	5	–3.0%
0	1	1	0	6	–1.8%
0	1	1	1	7	–0.6%
1	0	0	0	8	+0.6 %
1	0	0	1	9	+1.8 %
1	0	1	0	10	+3.0 %
1	0	1	1	11	+4.2 %
1	1	0	0	12	+5.4 %
1	1	0	1	13	+6.6 %
1	1	1	0	14	+7.8 %
1	1	1	1	15	+9.0 %

Switched Capacitor Filter Clock Programming

A block diagram of the switched capacitor filter clock divider is show in Figure 131. There is a fixed divide by 2 after the programmable divider. The switched capacitor filter clock value is given by the following equation;

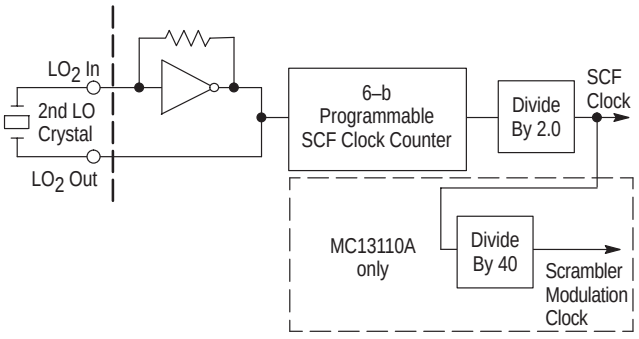
(SCF Clock) = F(2nd LO) / (SCF Divider Value * 2).

The scrambler modulation clock frequency (SMCF) is proportional to the SCF clock. The following equation defines its value:

SMCF = (SCF Clock)/40

The SCF divider should be set to a value which brings the SCF Clock as close to 165.16 kHz as possible. This is based on the 2nd LO frequency which is chosen in Figure 114.

Figure 131. SCF Clock Divider Circuit



Corner Frequency Programming for MC13110A and MC13111A

Four different corner frequencies may be selected by programming the SCF Clock divider as shown in Figures 132 and 133. It is important to note, that all filter corner frequencies will change proportionately with the SCF Clock Frequency and Scrambler Modulation Frequency. The power–up default SCF Clock divider value is 31.

Figure 132. Corner Frequency Programming for 10.240 MHz 2nd LO

MC13110A							
MC13111A							
SCF Clock Divider	Total Divide Value	SCF Clock Freq. (kHz)	R_X Upper Corner Frequency (kHz)	T_X Upper Corner Frequency (kHz)	Scrambler Modulation Frequency (Clk/40) (kHz)	Scrambler Lower Corner Frequency (Hz)	Scrambler Upper Corner Frequency (kHz)
29	58	176.55	4.147	3.955	4.414	267.2	3.902
30	60	170.67	4.008	3.823	4.267	258.3	3.772
31	62	165.16	3.879	3.700	4.129	250.0	3.650
32	64	160.00	3.758	3.584	4.000	242.2	3.536

NOTE: 18. All filter corner frequencies have a tolerance of ±3%.
19. R_X and T_X Upper Corner Frequencies are the same corner frequencies for the MC13110A in scrambler bypass

Figure 133. Corner Frequency Programming for 11.15 MHz 2nd LO

MC13110A / MC13111A							
SCF Clock Divider	Total Divide Value	SCF Clock Freq. (kHz)	R_X Upper Corner Frequency (kHz)	T_X Upper Corner Frequency (kHz)	Scrambler Modulation Frequency (Clk/40) (kHz)	Scrambler Lower Corner Frequency (Hz)	Scrambler Upper Corner Frequency (kHz)
32	64	174.22	4.092	3.903	4.355	263.7	3.850
33	66	168.94	3.968	3.785	4.223	255.7	3.733
34	68	163.97	3.851	3.673	4.099	248.2	3.624
35	70	159.29	3.741	3.568	3.982	241.1	3.520

NOTES: 20. All filter corner frequencies have a tolerance of ±3%.
21. R_X and T_X Upper Corner Frequencies are the same corner frequencies for the MC13110A in scrambler bypass

Figure 134. Auxiliary Register Latch Bits

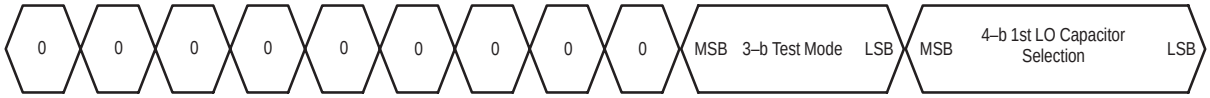


Figure 135. Digital Test Mode Description

TM #	TM 2	TM 1	TM 0	Counter Under Test or Test Mode Option	"T_X V_{CO}" Input Signal	"Clk Out" Output Expected
0	0	0	0	Normal Operation	>200 mVpp	–
1	0	0	1	R_X Counter	0 to 2.5 V	Input Frequency/R_X Counter Value
2	0	1	0	T_X Counter	0 to 2.5 V	Input Frequency/T_X Counter Value
3	0	1	1	Reference Counter + Divide by 4/25	0 to 2.5 V	Input Frequency/Reference Counter Value * 100
4	1	0	0	SC Counter	0 to 2.5 V	Input Frequency/SC Counter Value * 2
5	1	0	1	ALC Gain = 10 Option	N/A	N/A
6	1	1	0	ALC Gain = 25 Option	N/A	N/A

Auxiliary Register

The auxiliary register contains a 4–bit First LO Capacitor Selection latch and a 3–bit Test Mode latch. Operation of these latch bits are explained in Figures 134, 135 and 136.

Test Modes

Test modes are be selected through the 3–bit Test Mode Register. In test mode, the "T_X VCO" input pin is multiplexed to the input of the counter under test. The output of the counter under test is multiplexed to the "Clk Out" output pin so that each counter can be individually tested. **Make sure test mode bits are set to "0's" for normal operation.** Test mode operation is described in Figure 135. During normal operation, the "T_X VCO" input can be a minimum of 200 mVpp at 80 MHz and should be AC coupled. Input signals should be standard logic levels of 0 to 2.5 V and a maximum frequency of 16 MHz.

First Local Oscillator Programmable Capacitor Selection

There is a very large frequency difference between the minimum and maximum channel frequencies in the 25 Channel U.S. standard. The internal varactor adjustment range is not large enough to accommodate this large frequency span. An internal capacitor with 15 programmable capacitor values can be used to cover the 25 channel frequency span without the need to add external capacitors and switches. The programmable internal capacitor can also be used to eliminate the need to use an external variable capacitor to adjust the 1st LO center frequency during telephone assembly. Figure 32 shows the schematic of the 1st LO tank circuit. Figure 136 shows the register control bit values.

The internal programmable capacitor is composed of a matrix bank of capacitors that are switched in as desired. Programmable capacitor values between about 0 and 16 pF can be selected in steps of approximately 1.1 pF. The internal parallel resistance values in the table can be used to calculate the quality factor (Q) of the oscillator if the Q of the external inductor is known. The temperature coefficient of the varactor is 0.08%/°C. The temperature coefficient of the internal programmable capacitor is negligible. Tolerance on the varactor and programmable capacitor values is ±15%.

Figure 136. First Local Oscillator Internal Capacitor Selection

1st LO Cap. Bit 3	1st LO Cap. Bit 2	1st LO Cap. Bit 1	1st LO Cap. Bit 0	1st LO Cap. Select	Internal Programmable Capacitor Value (pF)	Varactor Value over 0.3 to 2.5 V (pF)	Equivalent Internal Parallel Resistance at 40 MHz (kΩ)	Equivalent Internal Parallel Resistance at 51 MHz (kΩ)
0	0	0	0	0	0.0	9.7 to 5.8	1200	736
0	0	1	0	2	0.6	9.7 to 5.8	79.3	48.8
0	0	0	1	1	1.7	9.7 to 5.8	131	80.8
0	1	0	1	5	2.8	9.7 to 5.8	31.4	19.3
0	1	1	0	6	3.9	9.7 to 5.8	33.8	20.8
0	1	1	1	7	4.9	9.7 to 5.8	66.6	41
0	1	0	0	4	6.0	9.7 to 5.8	49.9	30.7
0	0	1	1	3	7.1	9.7 to 5.8	40.7	25.1
1	0	0	0	8	8.2	9.7 to 5.8	27.1	16.7
1	0	0	1	9	9.4	9.7 to 5.8	21.6	13.3
1	0	1	0	10	10.5	9.7 to 5.8	20.5	12.6
1	0	1	1	11	11.6	9.7 to 5.8	18.6	11.5
1	1	0	0	12	12.7	9.7 to 5.8	17.2	10.6
1	1	0	1	13	13.8	9.7 to 5.8	15.8	9.7
1	1	1	0	14	14.9	9.7 to 5.8	15.3	9.4
1	1	1	1	15	16.0	9.7 to 5.8	14.2	8.7

OTHER APPLICATIONS INFORMATION

PCB Board Lay–Out Considerations

The ideal printed circuit board (PCB) lay out would be double–sided with a full ground plane on one side. The ground plane would be divided into separate sections to prevent any audio signal from feeding into the first local oscillator via the ground plane. Leaded components, can likewise, be inserted on the ground plane side to improve shielding and isolation from the circuit side of the PCB. The opposite side of the PCB is typically the circuit side. It has the interconnect traces and surface mount components. In cases where cost allows, it may be beneficial to use multi–layer boards to further improve isolation of components and sensitive sections (i.e. RF and audio). For the CT–0 band, it is also permissible to use single–sided PC layouts, but with continuous full ground fill in and around the components.

The proper placement of certain components specified in the application circuit may be very critical. In a lay–out design, these components should be placed before the other less critical components are inserted. It is also imperative that all RF paths be kept as short as possible. Finally, the MC13110A and MC13111A ground pins should be tied to ground at the pins and V_{CC} pins should have adequate decoupling to ground as close to the IC as possible. In mixed mode systems where digital and RF/Analog circuitry are present, the V_{CC} and V_{EE} buses need to be ac–decoupled and isolated from each other. The design must also take great caution to avoid interference with low level analog circuits. The receiver can be particularly susceptible to interference as they respond to signals of only a few microvolts. Again, be sure to keep the dc supply lines for the digital and analog portions separate. Avoid ground paths carrying common digital and analog currents, as well.

Component Selection

The evaluation circuit schematics specify particular components that were used to achieve the results shown in the typical curves and tables, but alternate components should give similar results. The MC13110A and MC13111A IC are capable of matching the sensitivity, IMD, adjacent channel rejection, and other performance criteria of a multi–chip analog cordless telephone system. For the most part, the same external components are used as in the multi–chip solution.

VB and PLL V_{ref}

VB is an internally generated bandgap voltage. It functions as an ac reference point for the operational amplifiers in the audio section as well as for the battery detect circuitry. This pin needs to be sufficiently filtered to reduce noise and prevent crosstalk between R_X audio to T_X audio signal paths. A practical capacitor range to choose that will minimize crosstalk and noise relative to start up time is 0.5 μf to 10 μf. The start time for a 0.5 μf capacitor is approximately 5.0 ms, while a 10μf capacitor is about 10 ms.

The “PLL V_{ref}” pin is the internal supply voltage for the R_X and T_X PLL’s. It is regulated to a nominal 2.5 V. The “V_{CC} Audio” pin is the supply voltage for the internal voltage regulator. Two capacitors with 10 μF and 0.01 μF values must be connected to the “PLL V_{ref}” pin to filter and stabilize this regulated voltage. The “PLL V_{ref}” pin may be used to power other IC’s as long as the total external load current does not exceed 1.0 mA. The tolerance of the regulated voltage is initially ±8.0%, but is improved to ±4.0% after the internal Bandgap voltage reference is adjusted electronically through the MPU serial interface. The voltage regulator is turned off in the Standby and Inactive modes to reduce current drain. In these modes, the “PLL V_{ref}” pin is internally connected to the “V_{CC} Audio” pin (i.e., the power supply voltage is maintained but is now unregulated).

It is important to note that the momentary drop in voltage below 2.5 V during this transition may affect initial PLL lock times and also may trigger the reset. To prevent this, the PLL V_{ref} capacitor described above should be kept the same or larger than the VB capacitor, say 10 μf as shown in the evaluation and application diagrams.

DC Coupling

Choosing the right coupling capacitors for the compander is also critical. The coupling capacitors will have an affect on the audio distortion, especially at lower audio frequencies. A useful capacitor range for the compander timing capacitors is 0.1 μf to 1.0 μf. It is advised to keep the compander capacitors the same value in both the handset and baseset applications.

All other dc coupling capacitors in the audio section will form high pass filters. The designer should choose the overall cut off frequency (–3.0 dB) to be around 200 Hz. Designing for lower cut off frequencies may add unnecessary cost and capacitor size to the design, while selecting too high of a cut off frequency may affect audio quality. It is not necessary or advised to design each audio coupling capacitors for the same cut off frequency. Design for the overall system cut off frequency. (Note: Do not expect the application, evaluation, nor production test schematics to necessarily be the correct capacitor selections.) The goals of these boards may be different than the systems approach a designer must consider.

For the supply pins (V_{CC} Audio and V_{CC} RF) choose a 10 μf in parallel with a high quality 0.01 μf capacitor. Separation of the these two supply planes is essential, too. This is to prevent interference between the RF and audio sections. It is always a good design practice to add additional coupling on each supply plane to ground as well.

The IF limiter capacitors are recommended to be 0.1 μf. Smaller values lower the gain of the limiter stage. The –3.0 dB limiting sensitivity and SINAD may be adversely affected.

Figure 138. Evaluation Board Schematic

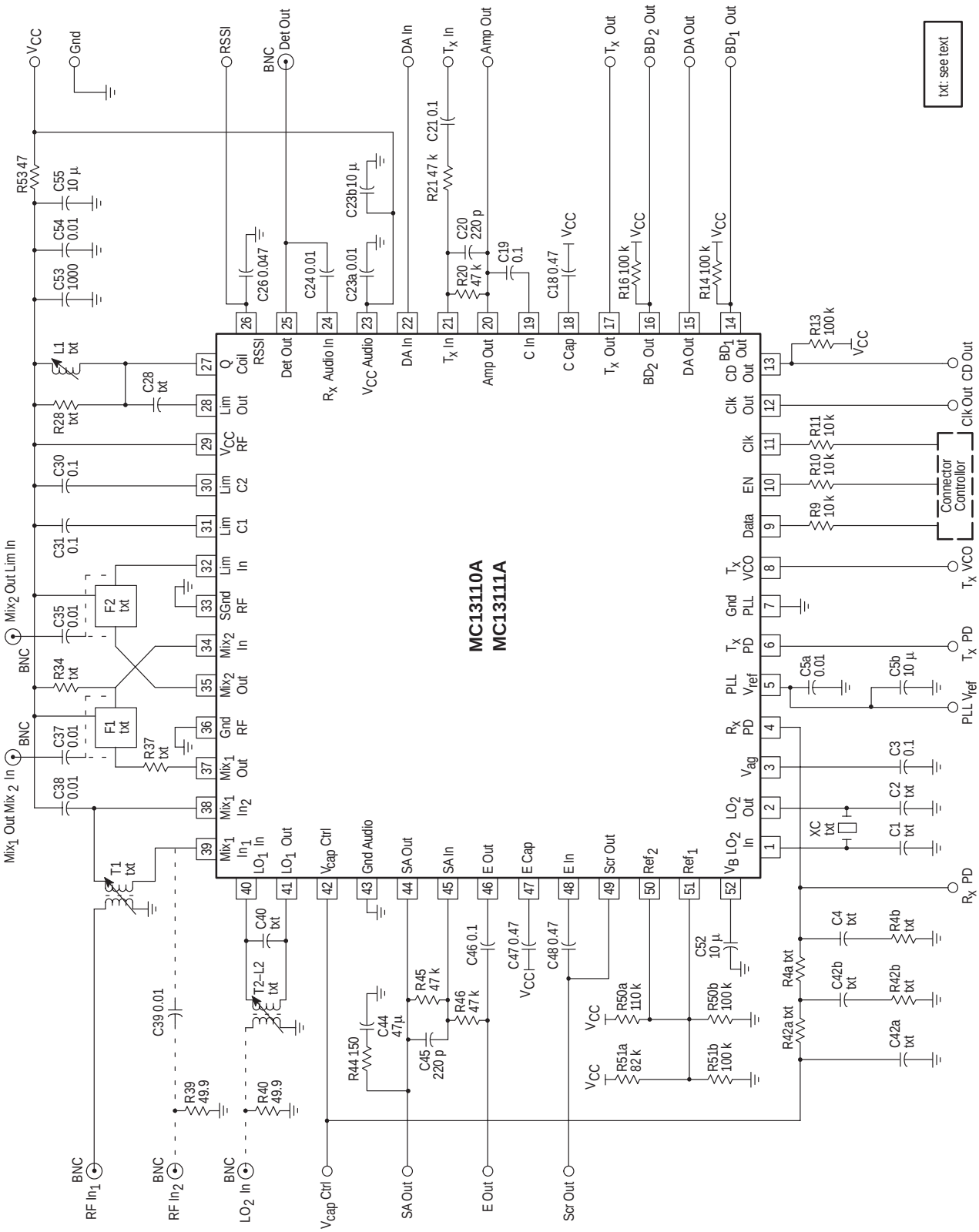


Figure 138. Evaluation Board Bill of Materials for U.S. and French Application

Comp. Number	USA Application Handset		French Application Base		
	RF (50 Ω)	RF Matched	RF Crystal (50 Ω)	RF Ceramic (50 Ω)	RF Matched
INPUT MATCHING					
T1	n.m.	Toko 1:5 292GNS–765A0	n.m.	n.m.	Toko 1:5 292GNS–765A0
C38	0.01	n.m.	0.01	0.01	n.m.
C39	0.01	n.m.	0.01	0.01	n.m.
10.7 MHz FILTER					
F1	Ceramic	Ceramic	Crystal	Ceramic	Ceramic
R37	0	0	1.2 k	0	0
R34	360	360	3.01 k	360	360
450 kHz FILTER					
F2	4 Element Murata E	4 Element Murata E	4 Element Murata G	4 Element Murata G	4 Element Murata G
DEMODULATOR					
L1	Q Coil Toko 7MCS–8128Z	Q Coil Toko 7MCS–8128Z	Ceramic Murata CDBM 450C34	Ceramic Murata CDBM 450C34	Ceramic Murata CDBM 450C34
R28	22.1 k	22.1 k	2.7 k	2.7 k	2.7 k
C28	10 p	10 p	390 p	390 p	390 p
OSCILLATOR					
Xtal	10.24 C1 = 10 p	10.24 C1 = 10 p	11.15 C1 = 18 p	11.15 C1 = 18 p	11.15 C1 = 18 p
C2	18 p	18 p	33 p	33 p	33 p
C1	5–25 p	5–25 p	15 p + 5–25 p	15 p + 5–25 p	15 p + 5–25 p
FIRST LO					
L2	0.47 Toko T1370	0.47 Toko T1370	0.22 Toko T1368	0.22 Toko T1368	0.22 Toko T1368
C40 HS/BS	HS: 27 pF BS: 22 pF	HS: 27 pF BS: 22 pF	BS: 100 p HS: 68 pF	BS: 100 p HS: 68 pF	BS: 100 p HS: 68 pF
LOOP FILTER HANDSET/BASESET					
R4a	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0
R4b	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0
C4	HS: 6800 BS: 8200	HS: 6800 BS: 8200	HS: 8600 BS: 6800	HS: 8600 BS: 6800	HS: 8600 BS: 6800
R42a	HS: 100 k BS: 100 k	HS: 100 k BS: 100 k	HS: 100 k BS: 100 k	HS: 100 k BS: 100 k	HS: 100 k BS: 100 k
R42b	HS: 22 k BS: 18 k	HS: 22 k BS: 18 k	HS: 18 k BS: 22 k	HS: 18 k BS: 22 k	HS: 18 k BS: 22 k
C42a	HS: 1000 BS: 1000	HS: 1000 BS: 1000	HS: 1000 BS: 1000	HS: 1000 BS: 1000	HS: 1000 BS: 1000
C42b	HS: 0.068 BS: 0.082	HS: 0.068 BS: 0.082	HS: 0.082 BS: 0.068	HS: 0.082 BS: 0.068	HS: 0.082 BS: 0.068

APPENDIX B
APPLICATIONS CIRCUIT

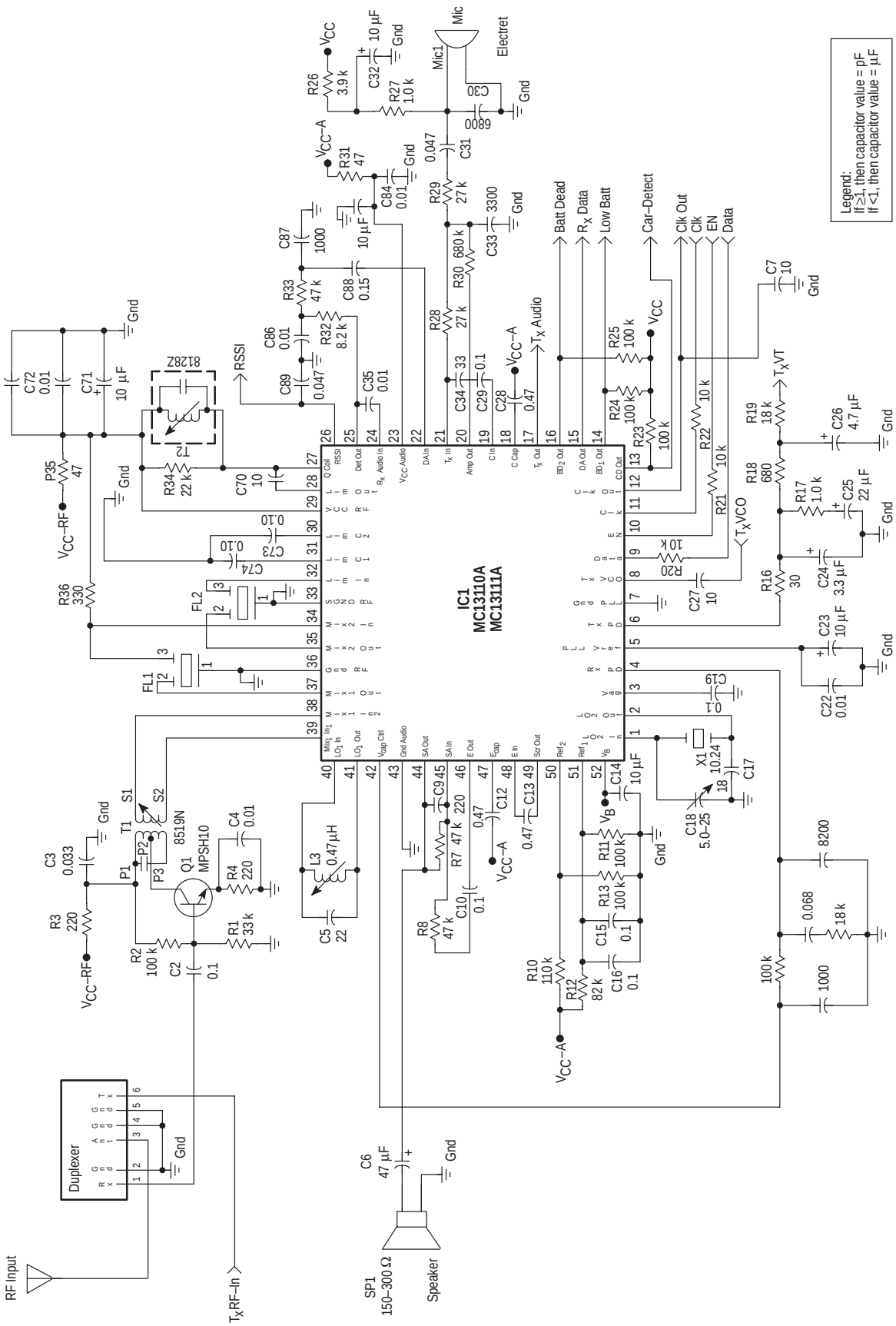
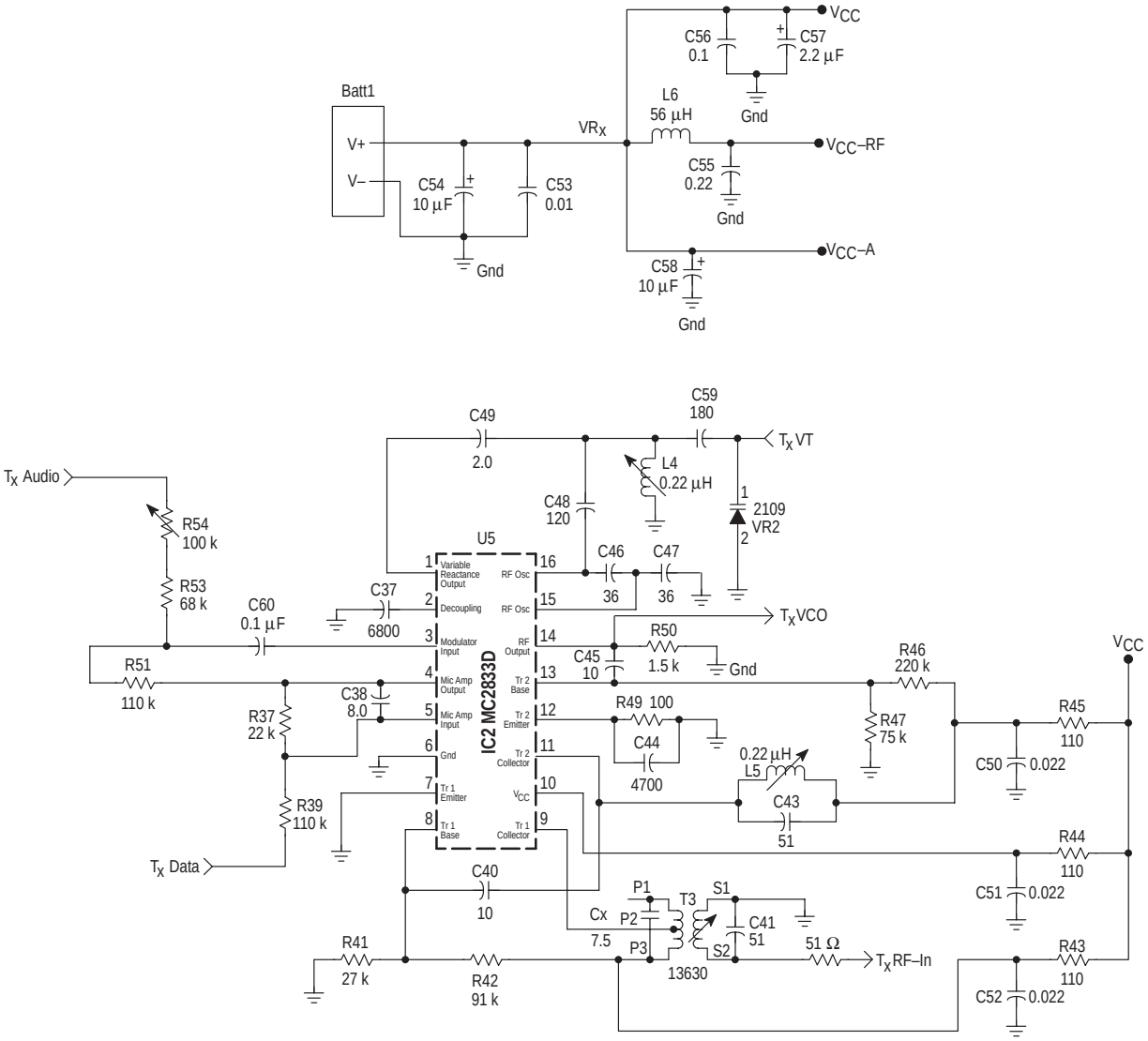


Figure 140. Basic Cordless Telephone Transceiver Application Circuit

Figure 140. Basic Cordless Telephone Transceiver Application Circuit (continued)



APPENDIX C – MEASUREMENT OF COMPANDER ATTACK/DECAY TIME

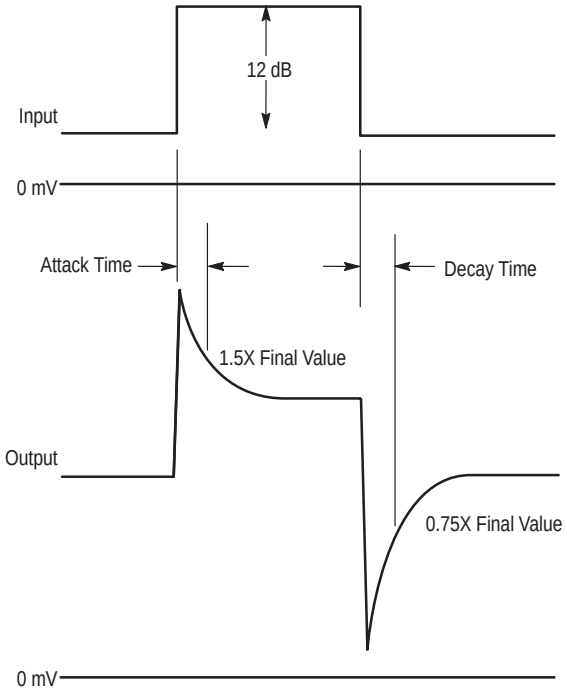
This measurement definition is based on EIA/CCITT recommendations.

Compressor Attack Time

For a 12 dB step up at the input, attack time is defined as the time for the output to settle to 1.5X of the final steady state value.

Compressor Decay Time

For a 12 dB step down at the input, decay time is defined as the time for the input to settle to 0.75X of the final steady state value.

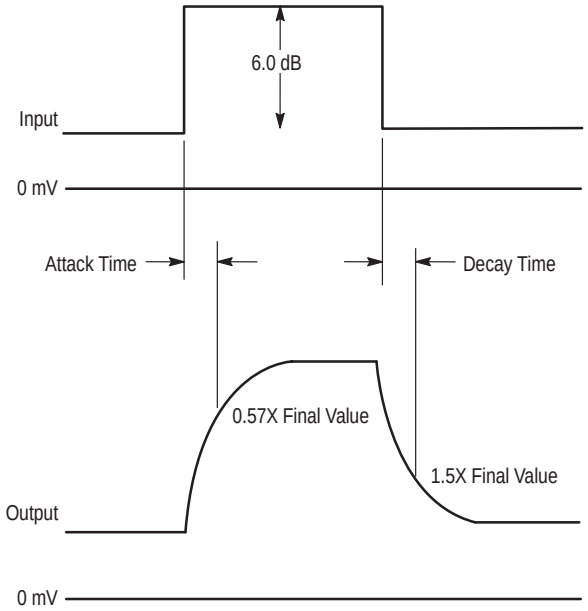


Expander Attack

For a 6.0 dB step up at the input, attack time is defined as the time for the output to settle to 0.57X of the final steady state value.

Expander Decay

For a 6.0 dB step down at the input, decay time is defined as the time for the output to settle to 1.5X of the final steady state value.



MOTOROLA

FM Communications Receivers

MC13135
MC13136

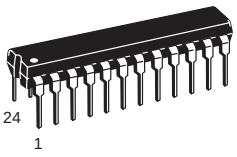
DUAL CONVERSION NARROWBAND FM RECEIVERS

The MC13135/MC13136 are the second generation of single chip, dual conversion FM communications receivers developed by Motorola. Major improvements in signal handling, RSSI and first oscillator operation have been made. In addition, recovered audio distortion and audio drive have improved. Using Motorola's MOSAIC™ 1.5 process, these receivers offer low noise, high gain and stability over a wide operating voltage range.

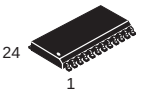
Both the MC13135 and MC13136 include a Colpitts oscillator, VCO tuning diode, low noise first and second mixer and LO, high gain limiting IF, and RSSI. The MC13135 is designed for use with an LC quadrature detector and has an uncommitted op amp that can be used either for an RSSI buffer or as a data comparator. The MC13136 can be used with either a ceramic discriminator or an LC quad coil and the op amp is internally connected for a voltage buffered RSSI output.

These devices can be used as stand–alone VHF receivers or as the lower IF of a triple conversion system. Applications include cordless telephones, short range data links, walkie–talkies, low cost land mobile, amateur radio receivers, baby monitors and scanners.

- Complete Dual Conversion FM Receiver – Antenna to Audio Output
- Input Frequency Range – 200 MHz
- Voltage Buffered RSSI with 70 dB of Usable Range
- Low Voltage Operation – 2.0 to 6.0 Vdc (2 Cell NiCad Supply)
- Low Current Drain – 3.5 mA Typ
- Low Impedance Audio Output < 25 Ω
- VHF Colpitts First LO for Crystal or VCO Operation
- Isolated Tuning Diode
- Buffered First LO Output to Drive CMOS PLL Synthesizer



P SUFFIX
PLASTIC PACKAGE
CASE 724



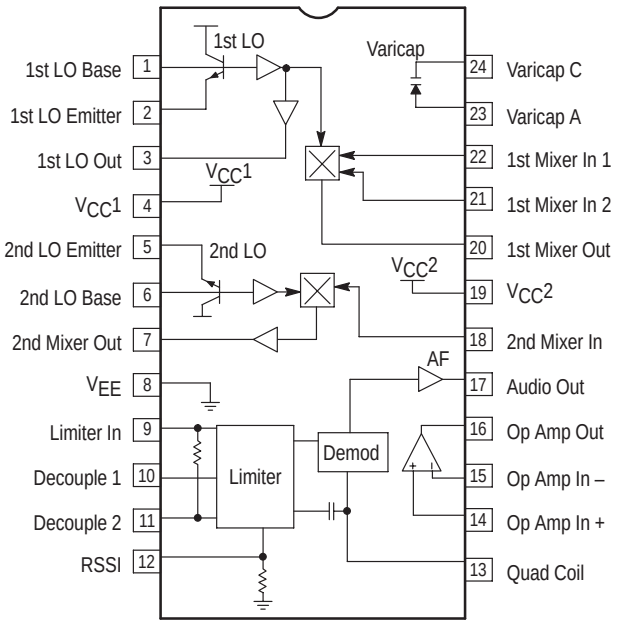
DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)

ORDERING INFORMATION

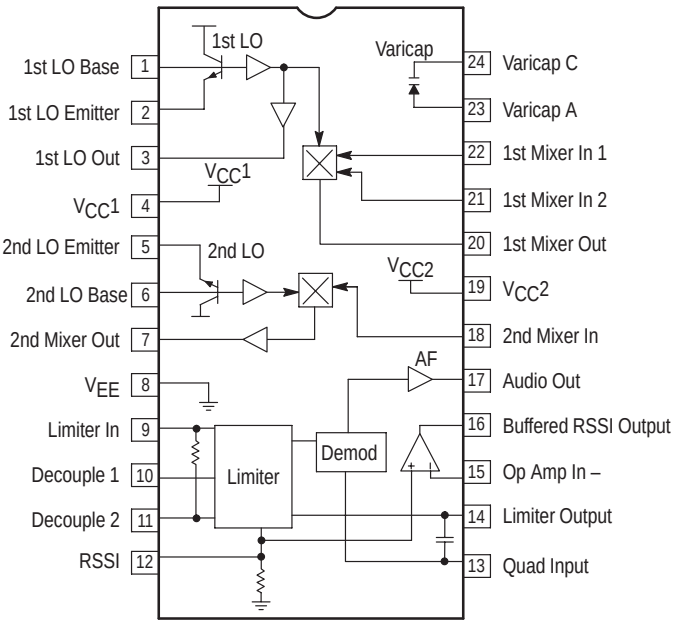
Device	Operating Temperature Range	Package
MC13135P	T_A = – 40° to +85°C	Plastic DIP
MC13135DW		SO–24L
MC13136DW		SO–24L

PIN CONNECTIONS

MC13135



MC13136



Each device contains 142 active transistors.

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 19	V_{CC} (max)	6.5	Vdc
RF Input Voltage	22	RF_{in}	1.0	Vrms
Junction Temperature	–	T_J	+150	°C
Storage Temperature Range	–	T_{stg}	– 65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 19	V_{CC}	2.0 to 6.0	Vdc
Maximum 1st IF	–	f_{IF1}	21	MHz
Maximum 2nd IF	–	f_{IF2}	3.0	MHz
Ambient Temperature Range	–	T_A	– 40 to + 85	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 4.0 Vdc, f_0 = 49.7 MHz, f_{MOD} = 1.0 kHz, Deviation = ±3.0 kHz, $f_{1st LO}$ = 39 MHz, $f_{2nd LO}$ = 10.245 MHz, IF1 = 10.7 MHz, IF2 = 455 kHz, unless otherwise noted. All measurements performed in the test circuit of Figure 1.)

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Total Drain Current	No Input Signal	I_{CC}	–	4.0	6.0	mAdc
Sensitivity (Input for 12 dB SINAD)	Matched Input	V_{SIN}	–	1.0	–	µVrms
Recovered Audio MC13135 MC13136	V_{RF} = 1.0 mV	AF_O	 170 215	 220 265	 300 365	mVrms
Limiter Output Level (Pin 14, MC13136)		V_{LIM}	 –	 130	 –	mVrms
1st Mixer Conversion Gain	V_{RF} = – 40 dBm	MX_{gain1}	–	12	–	dB
2nd Mixer Conversion Gain	V_{RF} = – 40 dBm	MX_{gain2}	–	13	–	dB
First LO Buffered Output	–	V_{LO}	–	100	–	mVrms
Total Harmonic Distortion	V_{RF} = – 30 dBm	THD	–	1.2	3.0	%
Demodulator Bandwidth	–	BW	–	50	–	kHz
RSSI Dynamic Range	–	RSSI	–	70	–	dB
First Mixer 3rd Order Intercept (Input)	 Matched Unmatched	TOI_{Mix1}	 – –	 –17 –11	 – –	dBm
Second Mixer 3rd Order Intercept (RF Input)	Matched Input	TOI_{Mix2}	 –	 – 27	 –	dBm
First LO Buffer Output Resistance	–	R_{LO}	–	–	–	Ω
First Mixer Parallel Input Resistance	–	R	–	722	–	Ω
First Mixer Parallel Input Capacitance	–	C	–	3.3	–	pF
First Mixer Output Impedance	–	ZO	–	330	–	Ω
Second Mixer Input Impedance	–	Z_I	–	4.0	–	kΩ
Second Mixer Output Impedance	–	ZO	–	1.8	–	kΩ
Detector Output Impedance	–	ZO	–	25	–	Ω

TEST CIRCUIT INFORMATION

Although the MC13136 can be operated with a ceramic discriminator, the recovered audio measurements for both the MC13135 and MC13136 are made with an LC quadrature detector. The typical recovered audio will depend on the external circuit; either the Q of the quad coil, or the RC matching network for the ceramic discriminator. On the MC13136, an external capacitor between Pins 13 and 14 can be used with a quad coil for slightly higher recovered audio. See Figures 10 through 13 for additional information.

Since adding a matching circuit to the RF input increases the signal level to the mixer, the third order intercept (TOI) point is better with an unmatched input (50 Ω from Pin 21 to Pin 22). Typical values for both have been included in the Electrical Characterization Table. TOI measurements were taken at the pins with a high impedance probe/spectrum analyzer system. The first mixer input impedance was measured at the pin with a network analyzer.

Figure 1a. MC13135 Test Circuit

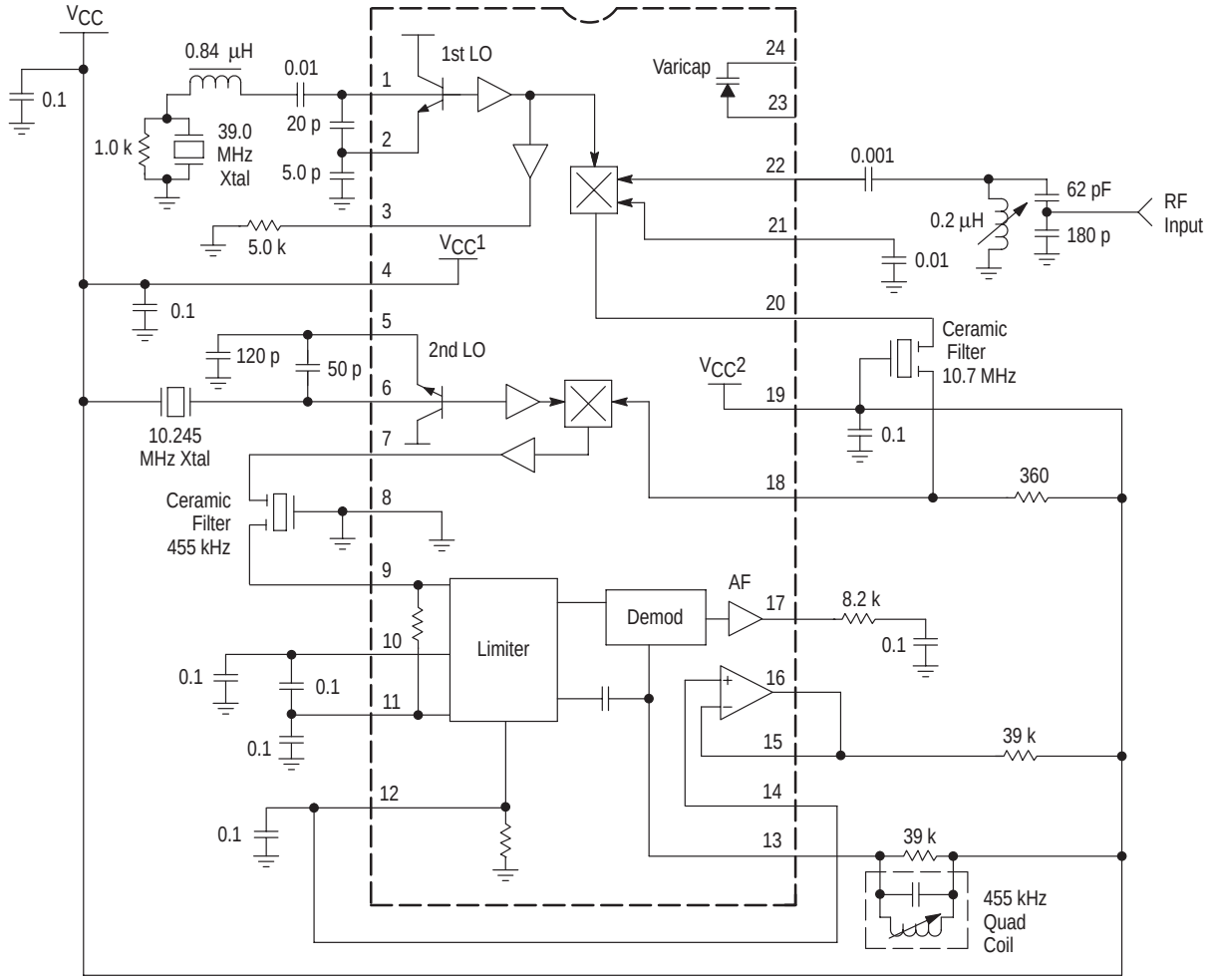


Figure 1b. MC13136 Quad Detector Test Circuit

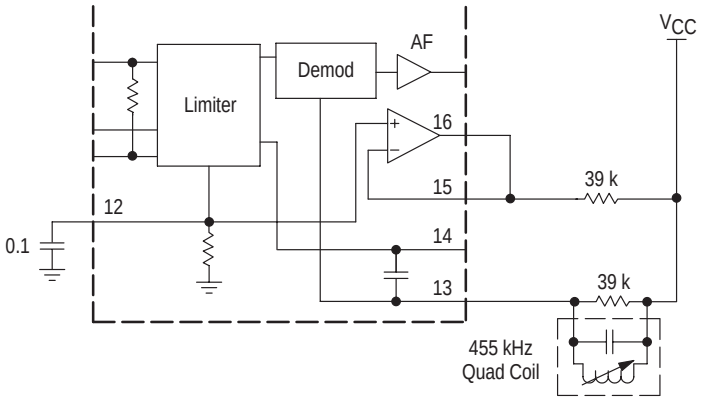


Figure 2. Supply Current versus Supply Voltage

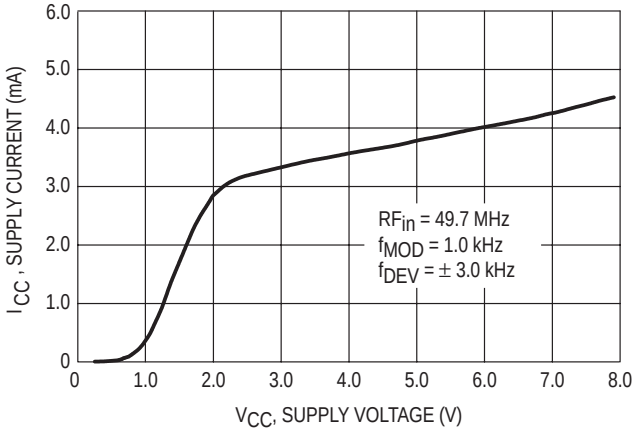


Figure 3. RSSI Output versus RF Input

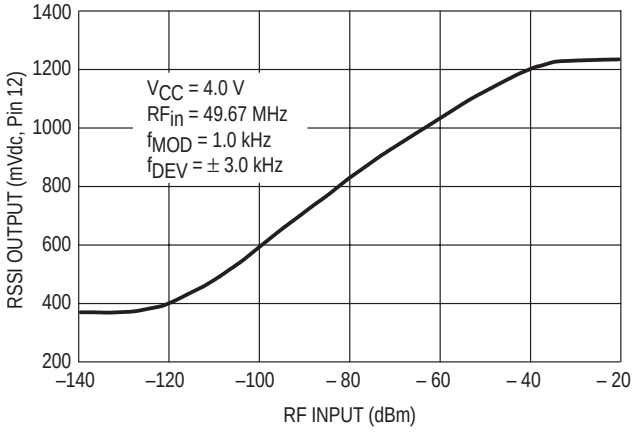


Figure 4. Varactor Capacitance, Resistance versus Bias Voltage

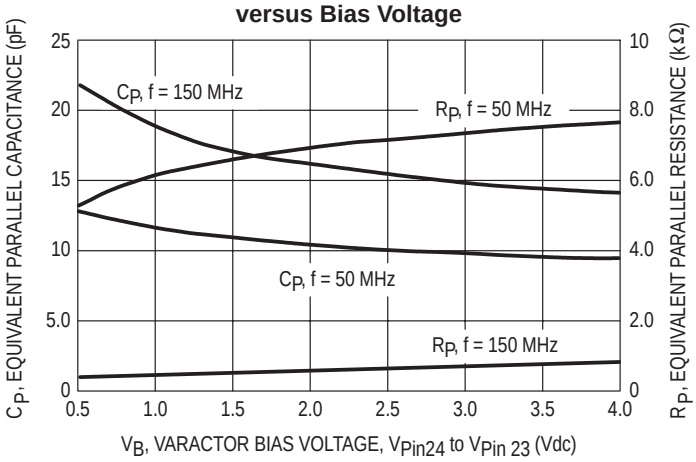


Figure 5. Oscillator Frequency versus Varactor Bias

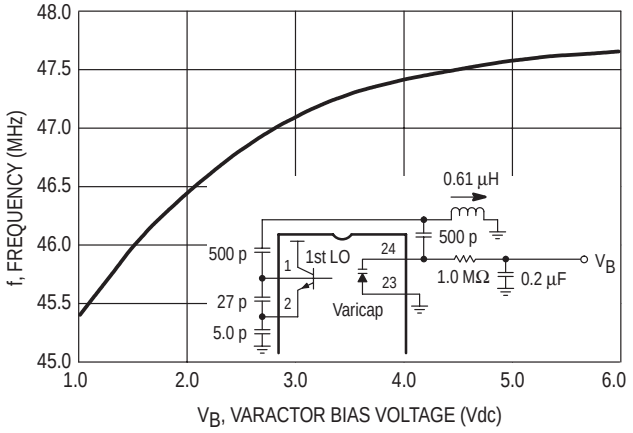


Figure 6. Signal Levels versus RF Input

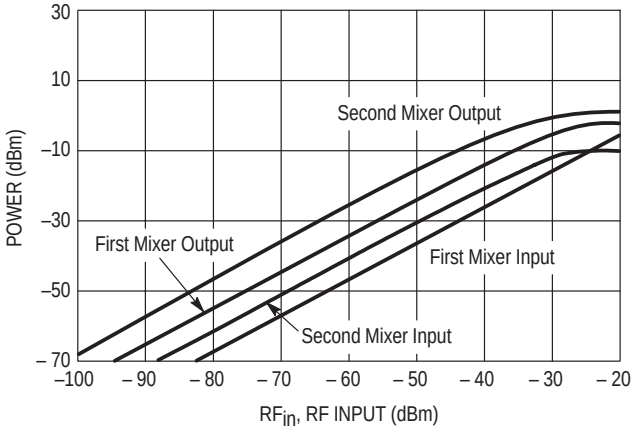


Figure 7. Signal + Noise, Noise, and AM Rejection versus Input Power

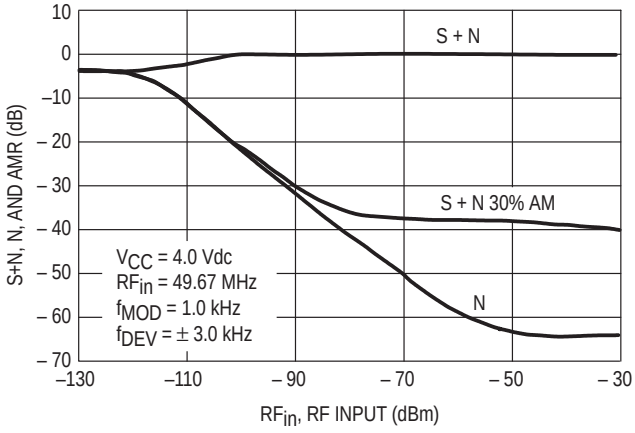


Figure 8. Op Amp Gain and Phase versus Frequency

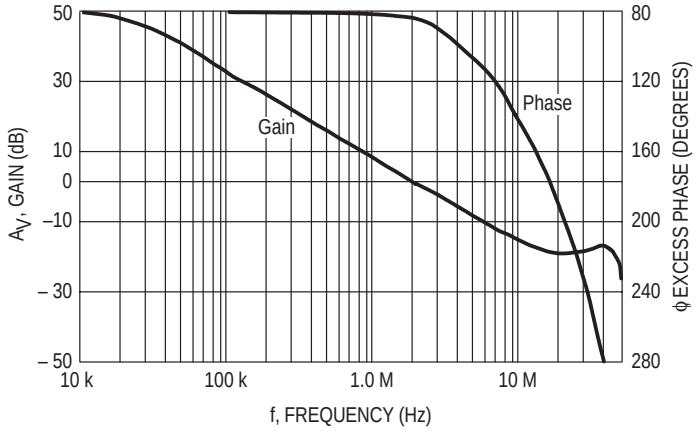


Figure 9. First Mixer Third Order Intermodulation (Unmatched Input)

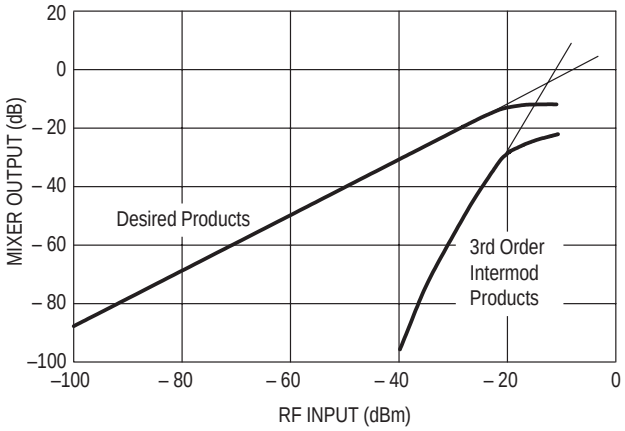


Figure 10. Recovered Audio versus Deviation for MC13135

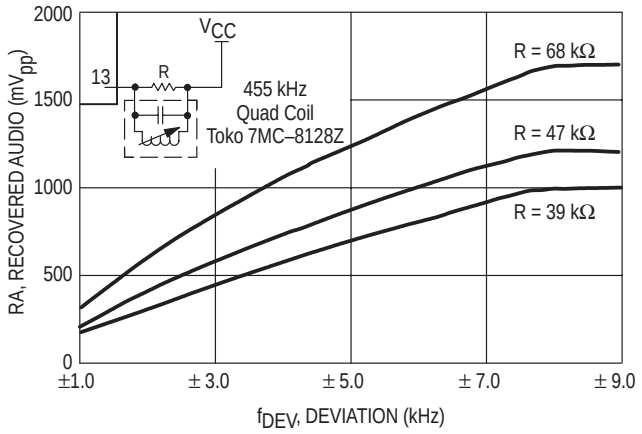


Figure 11. Distortion versus Deviation for MC13135

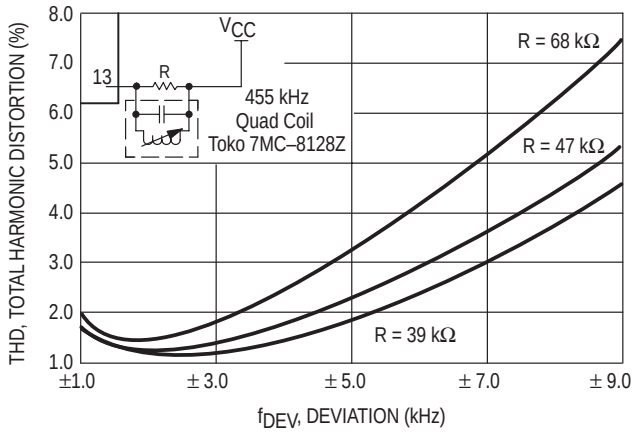


Figure 12. Recovered Audio versus Deviation for MC13136

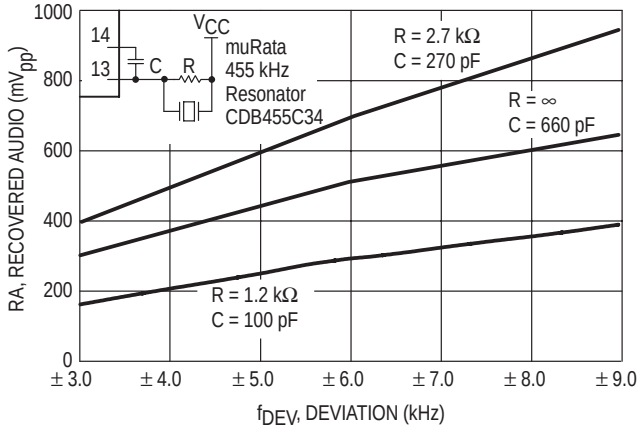
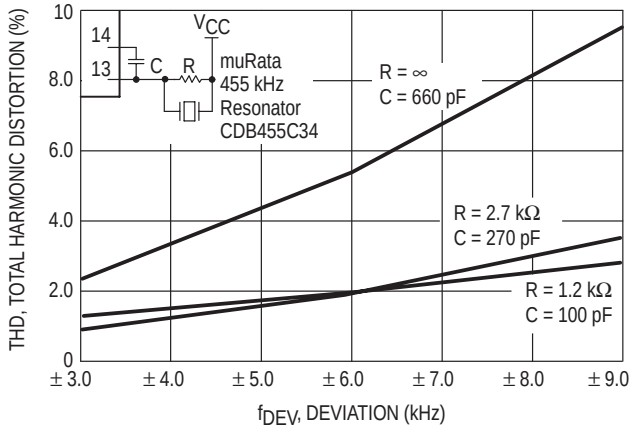


Figure 13. Distortion versus Deviation for MC13136



CIRCUIT DESCRIPTION

The MC13135/13136 are complete dual conversion receivers. They include two local oscillators, two mixers, a limiting IF amplifier and detector, and an op amp. Both provide a voltage buffered RSSI with 70 dB of usable range, isolated tuning diode and buffered LO output for PLL operation, and a separate V_{CC} pin for the first mixer and LO. Improvements have been made in the temperature performance of both the recovered audio and the RSSI.

V_{CC}

Two separate V_{CC} lines enable the first LO and mixer to continue running while the rest of the circuit is powered down. They also isolate the RF from the rest of the internal circuit.

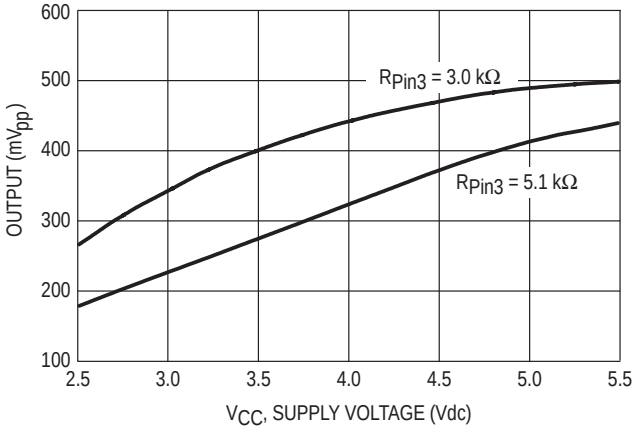
Local Oscillators

The local oscillators are grounded collector Colpitts, which can be easily crystal–controlled or VCO controlled with the on–board varactor and external PLL. The first LO transistor is internally biased, but the emitter is pinned–out and I_Q can be increased for high frequency or VCO operation. The collector is not pinned out, so for crystal operation, the LO is generally limited to 3rd overtone crystal frequencies; typically around 60 MHz. For higher frequency operation, the LO can be provided externally as shown in Figure 16.

Buffer

An amplifier on the 1st LO output converts the single–ended LO output to a differential signal to drive the mixer. Capacitive coupling between the LO and the amplifier minimizes the effects of the change in oscillator current on the mixer. Buffered LO output is pinned–out at Pin 3 for use with a PLL, with a typical output voltage of 320 mV_{pp} at V_{CC} = 4.0 V and with a 5.1 k resistor from Pin 3 to ground. As seen in Figure 14, the buffered LO output varies with the supply voltage and a smaller external resistor may be needed for low voltage operation. The LO buffer operates up to 60 MHz, typically. Above 60 MHz, the output at Pin 3 rolls off at approximately 6.0 dB per octave. Since most PLLs require about 200 mV_{pp} drive, an external amplifier may be required.

Figure 14. Buffered LO Output Voltage versus Supply Voltage



Mixers

The first and second mixer are of similar design. Both are double balanced to suppress the LO and input frequencies to give only the sum and difference frequencies out. This configuration typically provides 40 to 60 dB of LO suppression. New design techniques provide improved mixer linearity and third order intercept without increased noise. The gain on the output of the 1st mixer starts to roll off at about 20 MHz, so this receiver could be used with a 21 MHz first IF. It is designed for use with a ceramic filter, with an output impedance of 330 Ω. A series resistor can be used to raise the impedance for use with a crystal filter, which typically has an input impedance of 4.0 kΩ. The second mixer input impedance is approximately 4.0 kΩ; it requires an external 360 Ω parallel resistor for use with a standard ceramic filter.

Limiting IF Amplifier and Detector

The limiter has approximately 110 dB of gain, which starts rolling off at 2.0 MHz. Although not designed for wideband operation, the bandwidth of the audio frequency amplifier has been widened to 50 kHz, which gives less phase shift and enables the receiver to run at higher data rates. However, care should be taken not to exceed the bandwidth allowed by local regulations.

The MC13135 is designed for use with an LC quadrature detector, and does not have sufficient drive to be used with a ceramic discriminator. The MC13136 was designed to use a ceramic discriminator, but can also be run with an LC quad coil, as mentioned in the Test Circuit Information section. The data shown in Figures 12 and 13 was taken using a muRata CDB455C34 ceramic discriminator which has been specially matched to the MC13136. Both the choice of discriminators and the external matching circuit will affect the distortion and recovered audio.

RSSI/Op Amp

The Received Signal Strength Indicator (RSSI) on the MC13135/13136 has about 70 dB of range. The resistor needed to translate the RSSI current to a voltage output has been included on the internal circuit, which gives it a tighter tolerance. A temperature compensated reference current also improves the RSSI accuracy over temperature. On the MC13136, the op amp on board is connected to the output to provide a voltage buffered RSSI. On the MC13135, the op amp is not connected internally and can be used for the RSSI or as a data slicer (see Figure 17c).

Figure 15. PLL Controlled Narrowband FM Receiver at 46/49 MHz

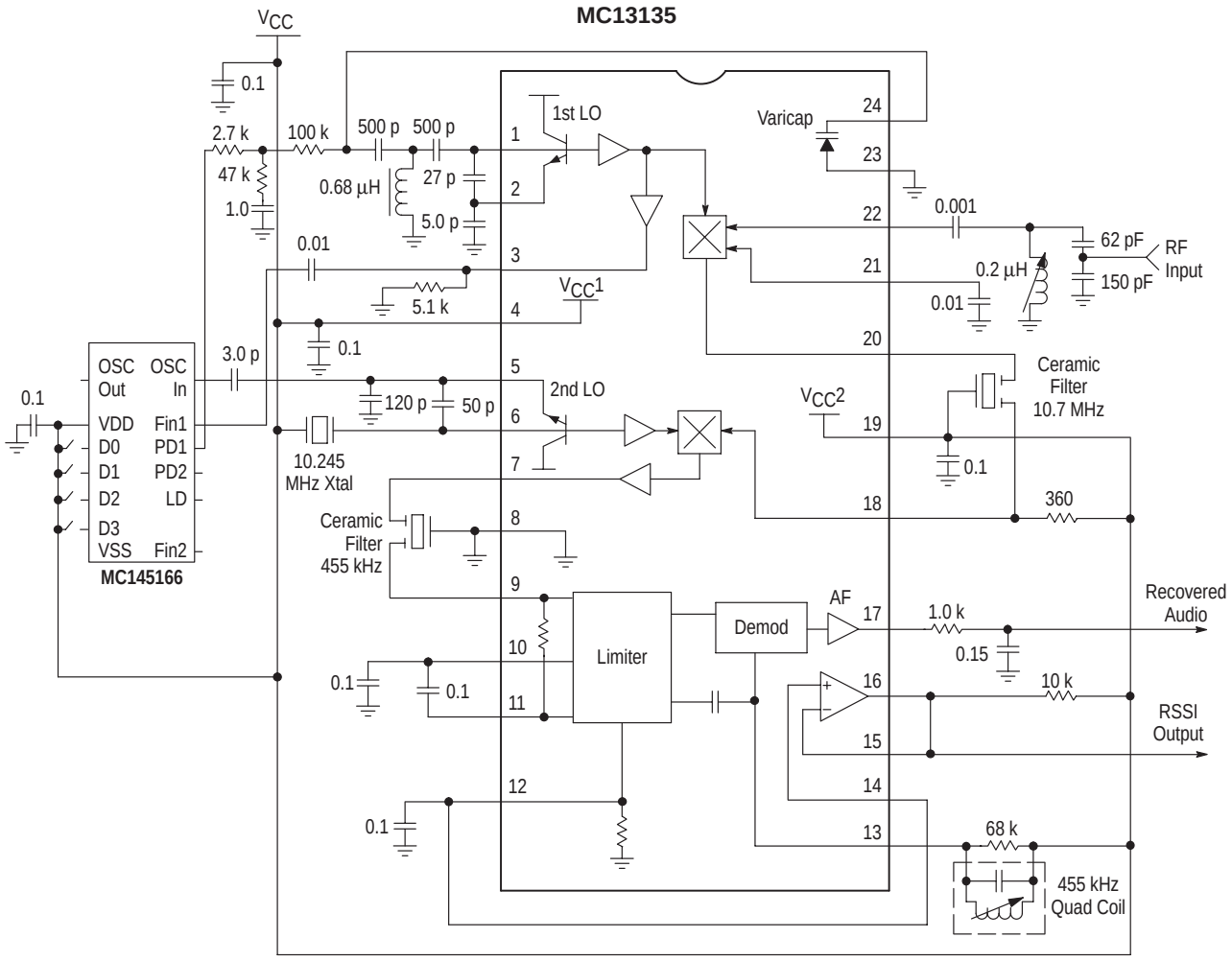
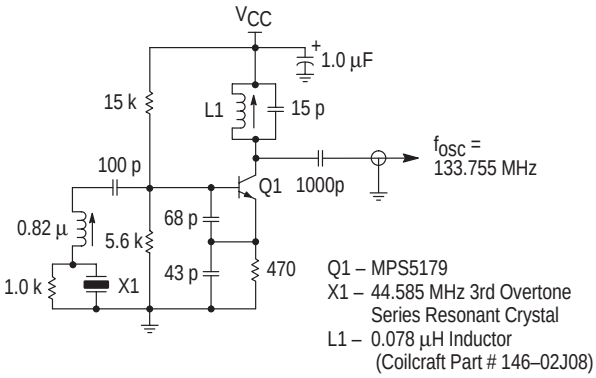


Figure 16. 144 MHz Single Channel Application Circuit

1st LO External Oscillator Circuit



Preamp for MC13135 at 144.455 MHz

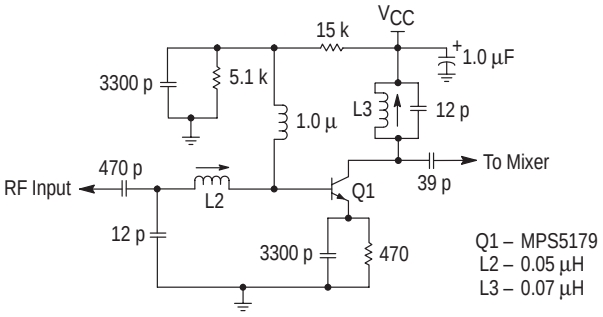


Figure 17a. Single Channel Narrowband FM Receiver at 49.7 MHz

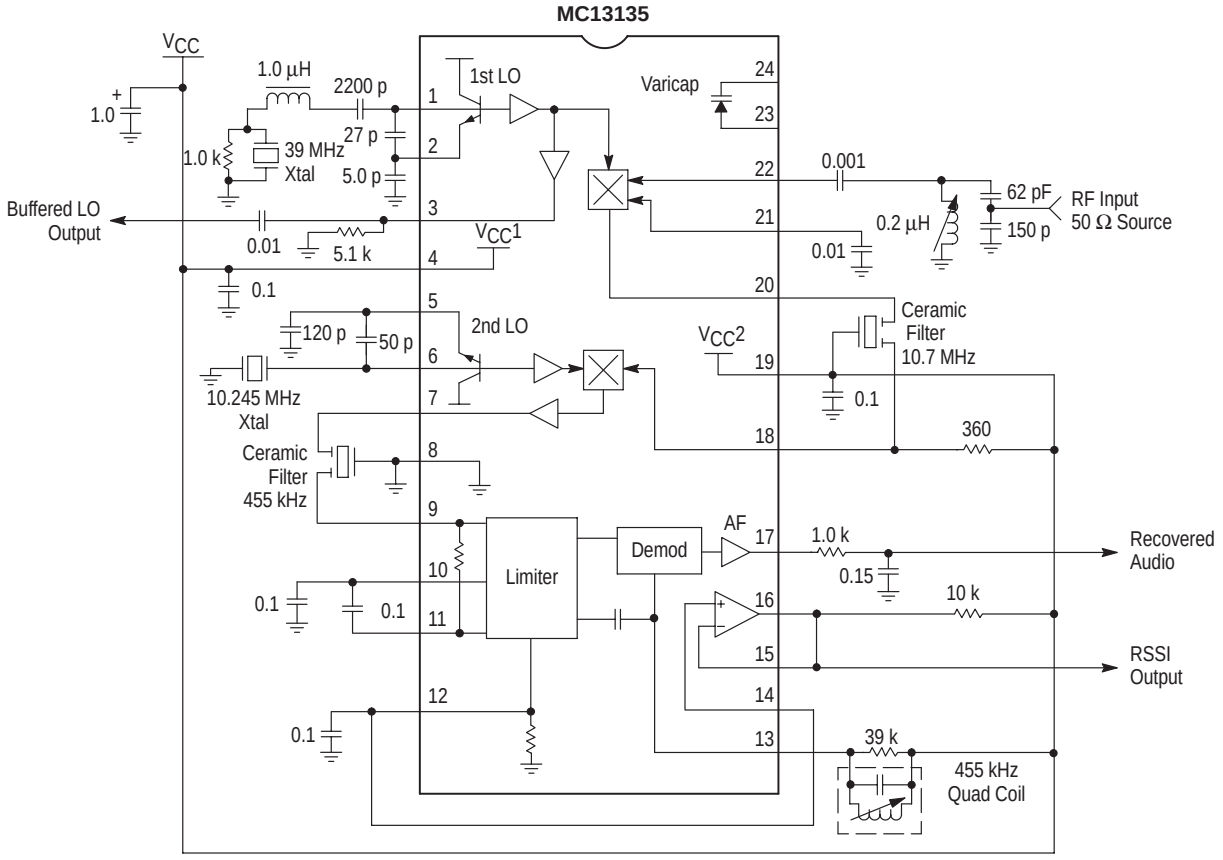
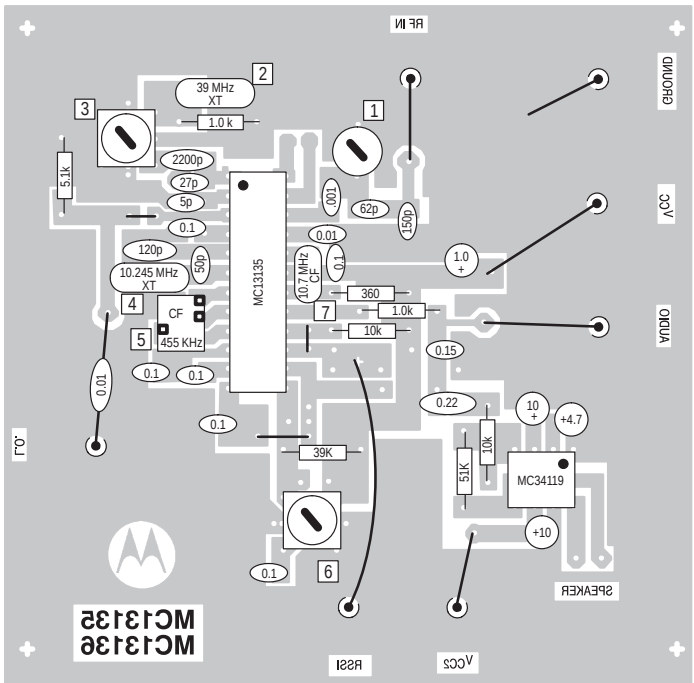


Figure 17b. PC Board Component View



NOTES:
1. 0.2 µH tunable (unshielded) inductor
2. 39 MHz Series mode resonant 3rd Overtone Crystal
3. 1.5 µH tunable (shielded) inductor
4. 10.245 MHz Fundamental mode crystal, 32 pF load
5. 455 kHz ceramic filter, muRata CFU 455B or equivalent
6. Quadrature coil, Toko 7MC–8128Z (7mm) or Toko RMC–2A6597HM (10mm)
7. 10.7 MHz ceramic filter, muRata SFE10.7MJ–A or equivalent

Figure 17c. Optional Data Slicer Circuit
(Using Internal Op Amp)

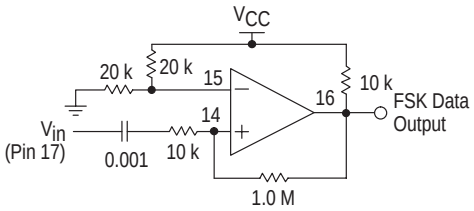
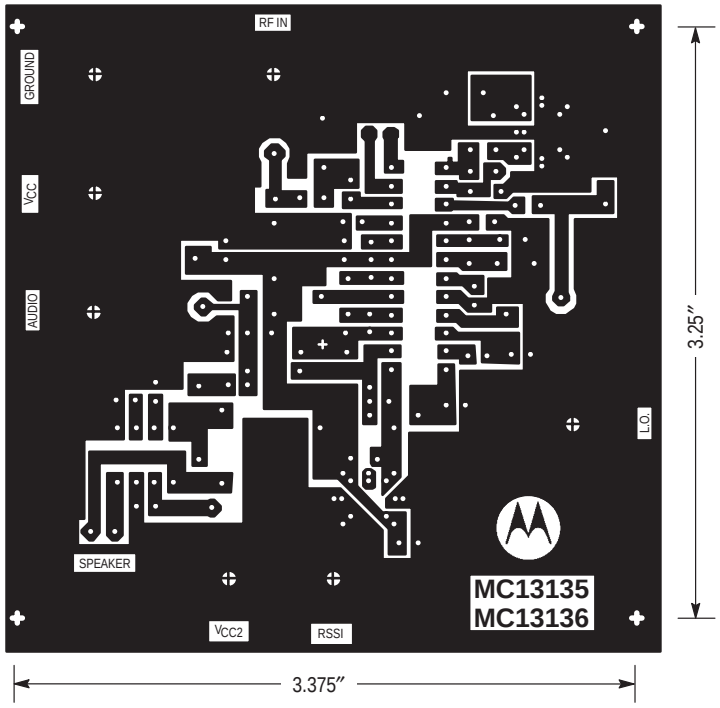
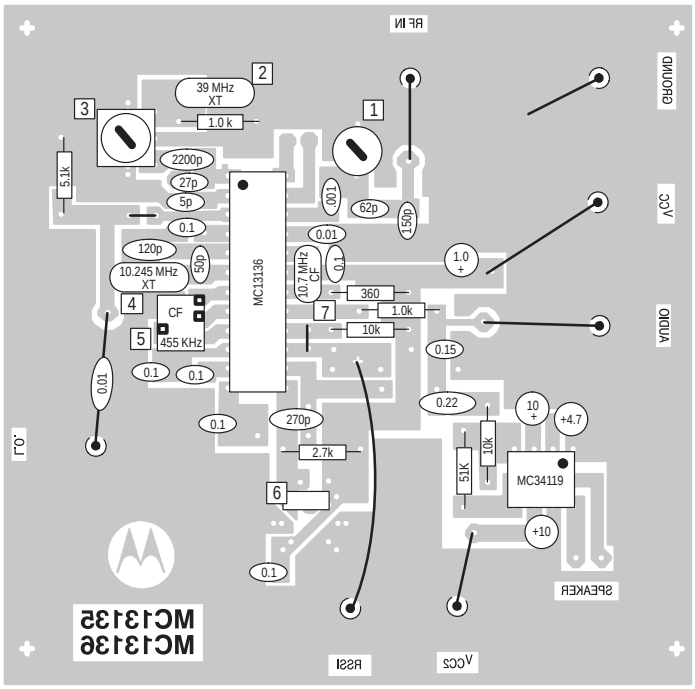


Figure 18. PC Board Solder Side View



(Circuit Side View)

Figure 19. PC Board Component View



NOTES:
1. 0.2 µH tunable (unshielded) inductor
2. 39 MHz Series mode resonant 3rd Overtone Crystal
3. 1.5 µH tunable (shielded) inductor
4. 10.245 MHz Fundamental mode crystal, 32 pF load
5. 455 kHz ceramic filter, muRata CFU 455B or equivalent
6. Ceramic discriminator, muRata CDB455C34 or equivalent
7. 10.7 MHz ceramic filter, muRata SFE10.7MJ–A or equivalent

Figure 20a. Single Channel Narrowband FM Receiver at 49.7 MHz

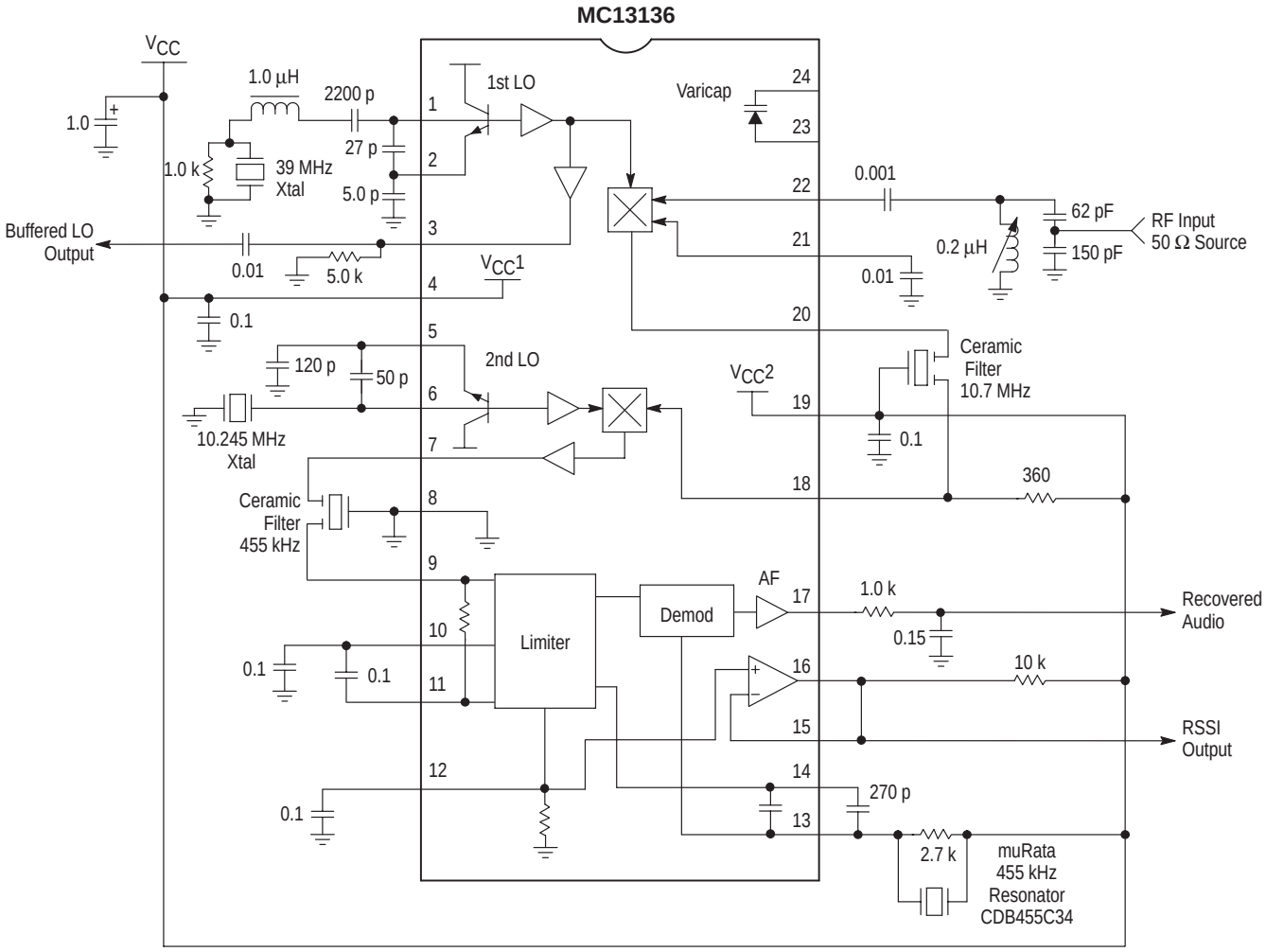


Figure 20b. Optional Audio Amplifier Circuit

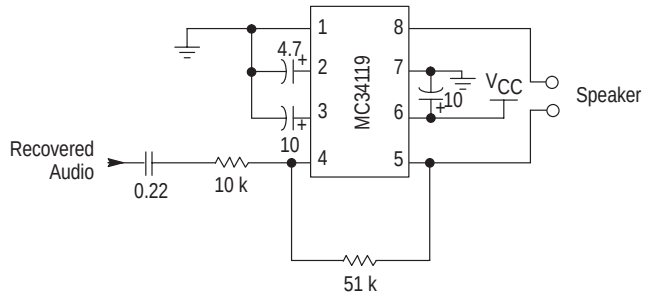
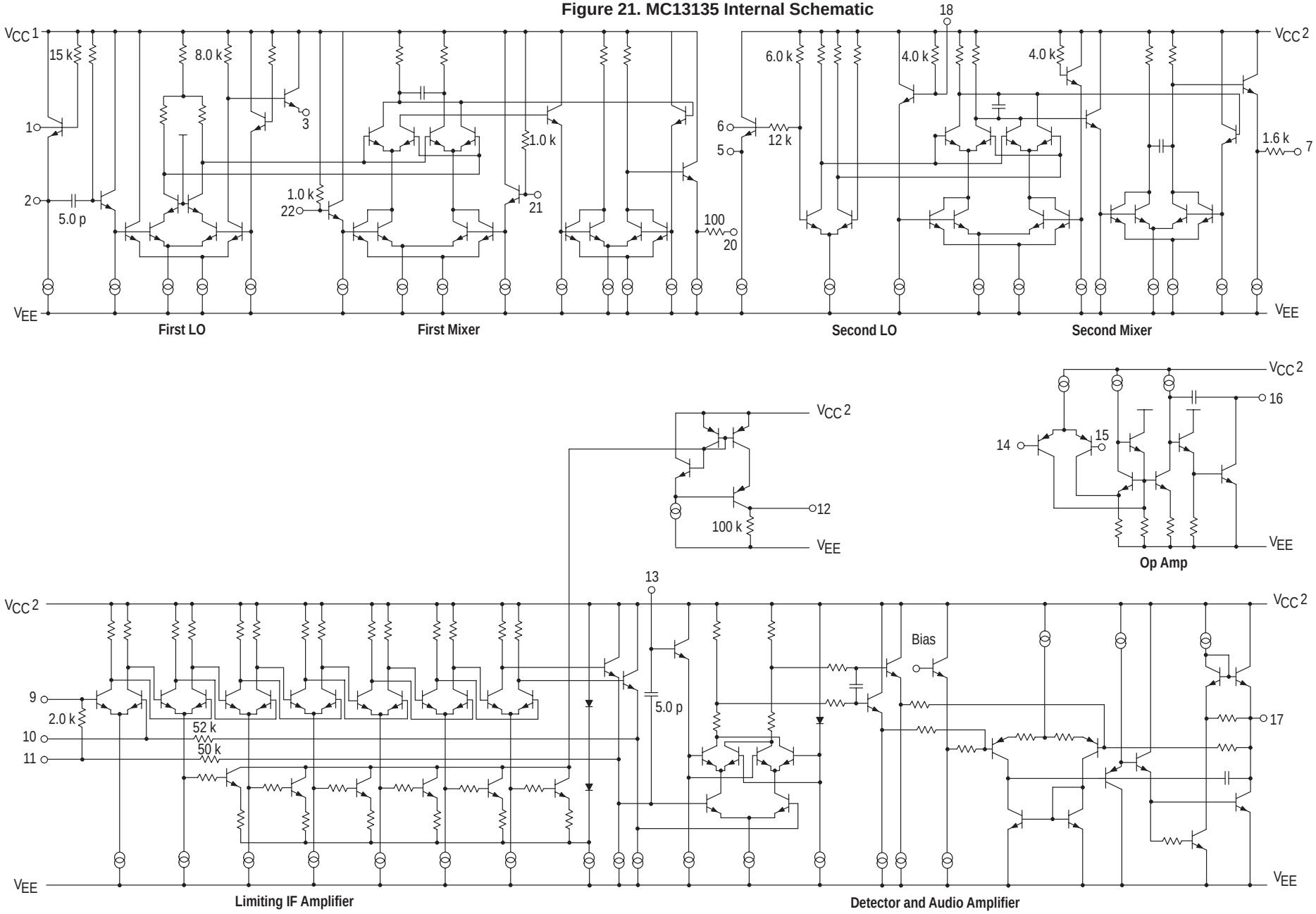
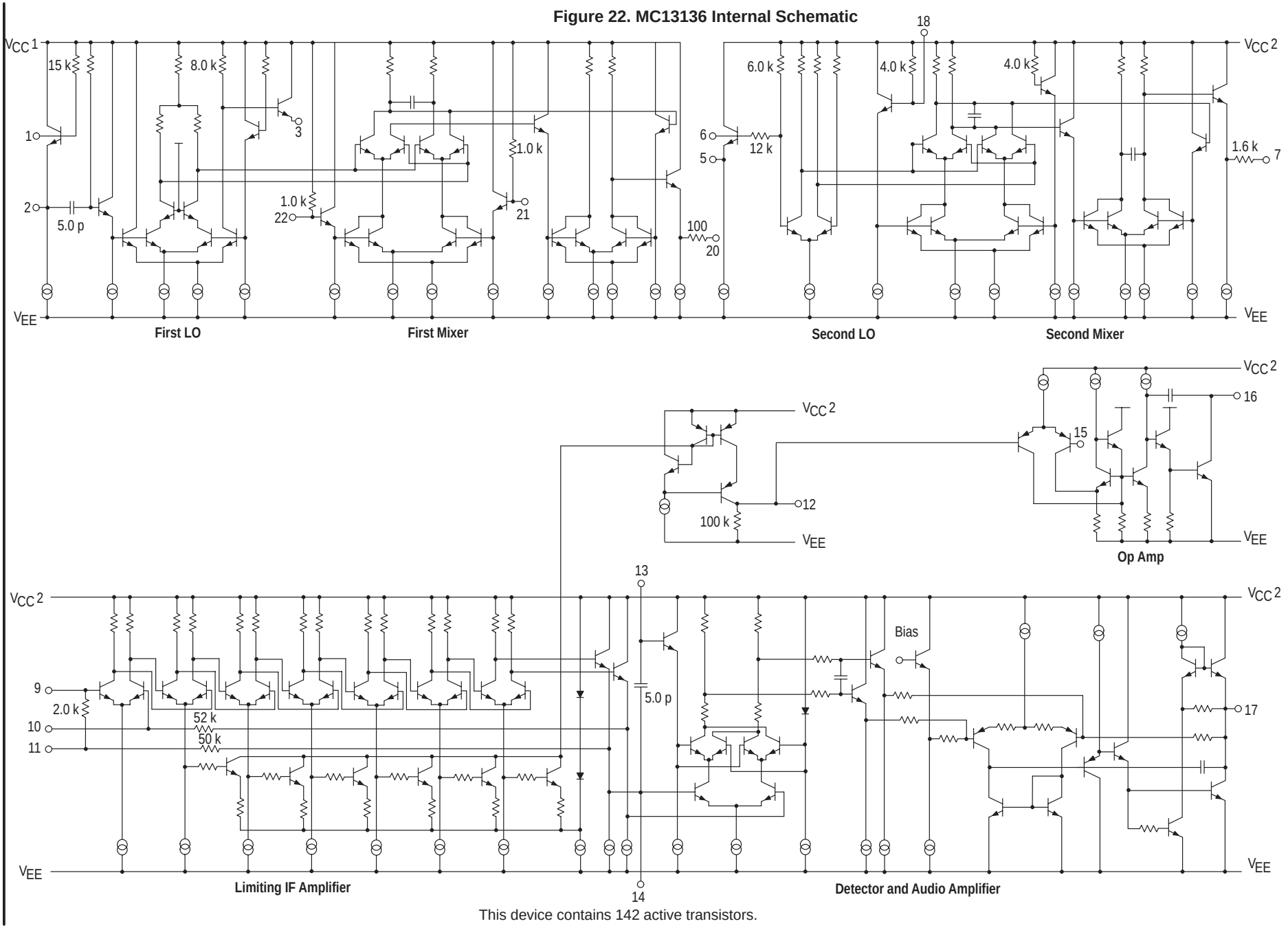


Figure 21. MC13135 Internal Schematic



This device contains 142 active transistors.

Figure 22. MC13136 Internal Schematic



This device contains 142 active transistors.

MOTOROLA

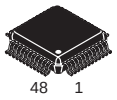
MC13145

Low Power Integrated Receiver for ISM Band Applications

UHF WIDEBAND RECEIVER SUBSYSTEM (LNA, Mixer, VCO, Prescalar, IF Subsystem, Coilless Detector)

The MC13145 is a dual conversion integrated RF receiver intended for ISM band applications. It features a Low Noise Amplifier (LNA), two 50 Ω linear Mixers with linearity control, Voltage Controlled Oscillator (VCO), second LO amplifier, divide by 64/65 dual modulus Prescalar, split IF Amplifier and Limiter, RSSI output, Coilless FM/FSK Demodulator and power down control. Together with the transmit chip (MC13146) and the baseband chip (MC33410 or MC33411A/B), a complete 900 MHz cordless phone system can be implemented. This device may be used in applications up to 1.8 GHz.

- Low (<1.8 dB @ 900 MHz) Noise Figure LNA with 14 dB Gain
- Externally Programmable Mixer linearity: IIP3 = 10(nom.) to 17 dBm (Mixer1); IIP3 = 10 (nom.) to 17 dBm (Mixer2)
- 50 Ω Mixer Input Impedance and Open Collector Output (Mixer 1 and Mixer 2); 50 Ω Second LO (LO2) Input Impedance
- Low Power 64/65 Dual Modulus Prescalar (MC12053 type)
- Split IF for Improved Filtering and Extended RSSI Range
- Internal 330 Ω Terminations for 10.7 MHz Filters
- Linear Coilless FM/FSK Demodulator with Externally Programmable Bandwidth, Center Frequency and Audio level
- 2.7 to 6.5 V Operation, Low Current Drain (<27 mA, Typ @ 3.6 V) with Power Down Mode (<10 μA, Typ)
- 2.4 GHz RF, 1.0 GHz IF1 and 50 MHz IF2 Bandwidth

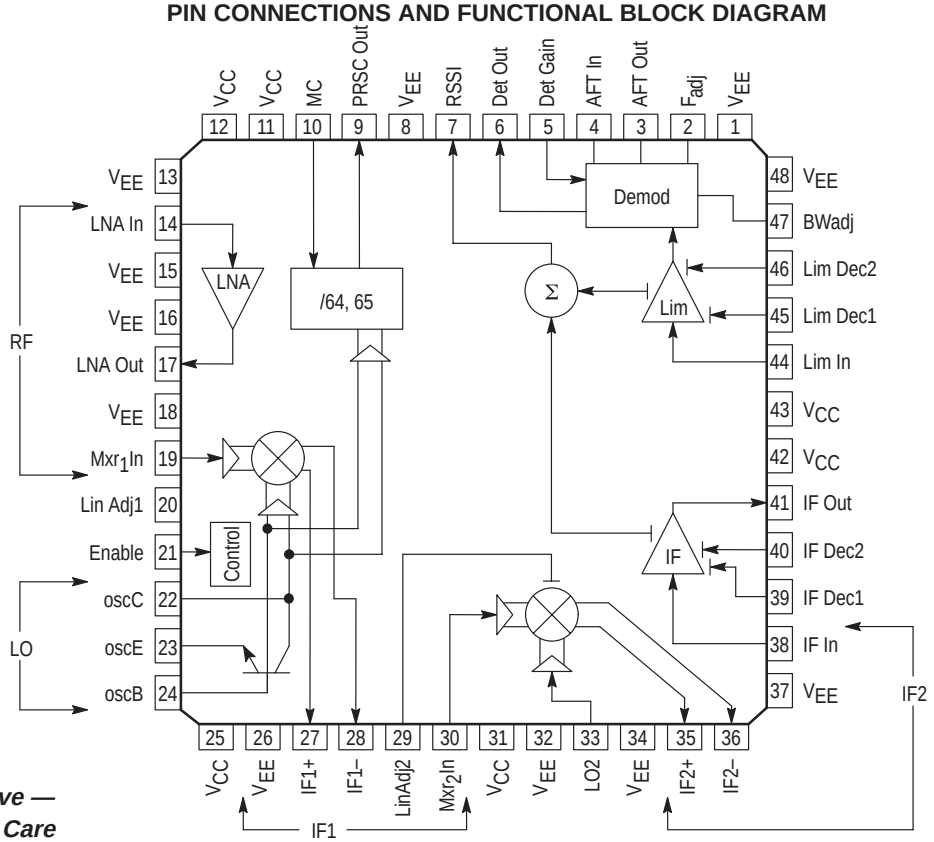


FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(LQFP–48)

ORDERING INFORMATION

Device	Temperature Range	Package
MC13145FTA	T_A = –20 to 70°C	LQFP–48

PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



ESD Sensitive — Handle with Care

This device contains 626 active transistors.

OVERALL RECEIVER SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}(max)	7.0	Vdc
Junction Temperature	T_J(max)	150	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Maximum Input Signal	P_{in}	5.0	dBm

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions, Electrical Characteristics tables or Pin Descriptions section.
2. Meets Human Body Model (HBM) ≤250 V and Machine Model (MM) ≤25 V. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (T_A = 25°C)	V_{CC} V_{EE}	2.7 0	– 0	6.5 0	Vdc
Input Frequency (LNA In, Mxr$_1$ In)	f_{in}	100	–	1800	MHz
Ambient Temperature Range	T_A	–20	–	70	°C
Input Signal Level (with minor performance degradation)	P_{in}	–	–10	–	dBm

RECEIVER DC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.6 Vdc; No Input Signal, unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Total Supply Current (Enable = V_{CC})	I_{total}	24	27	34	mA
Power Down Current (Enable = V_{EE})	I_{total}	–	10	50	μA

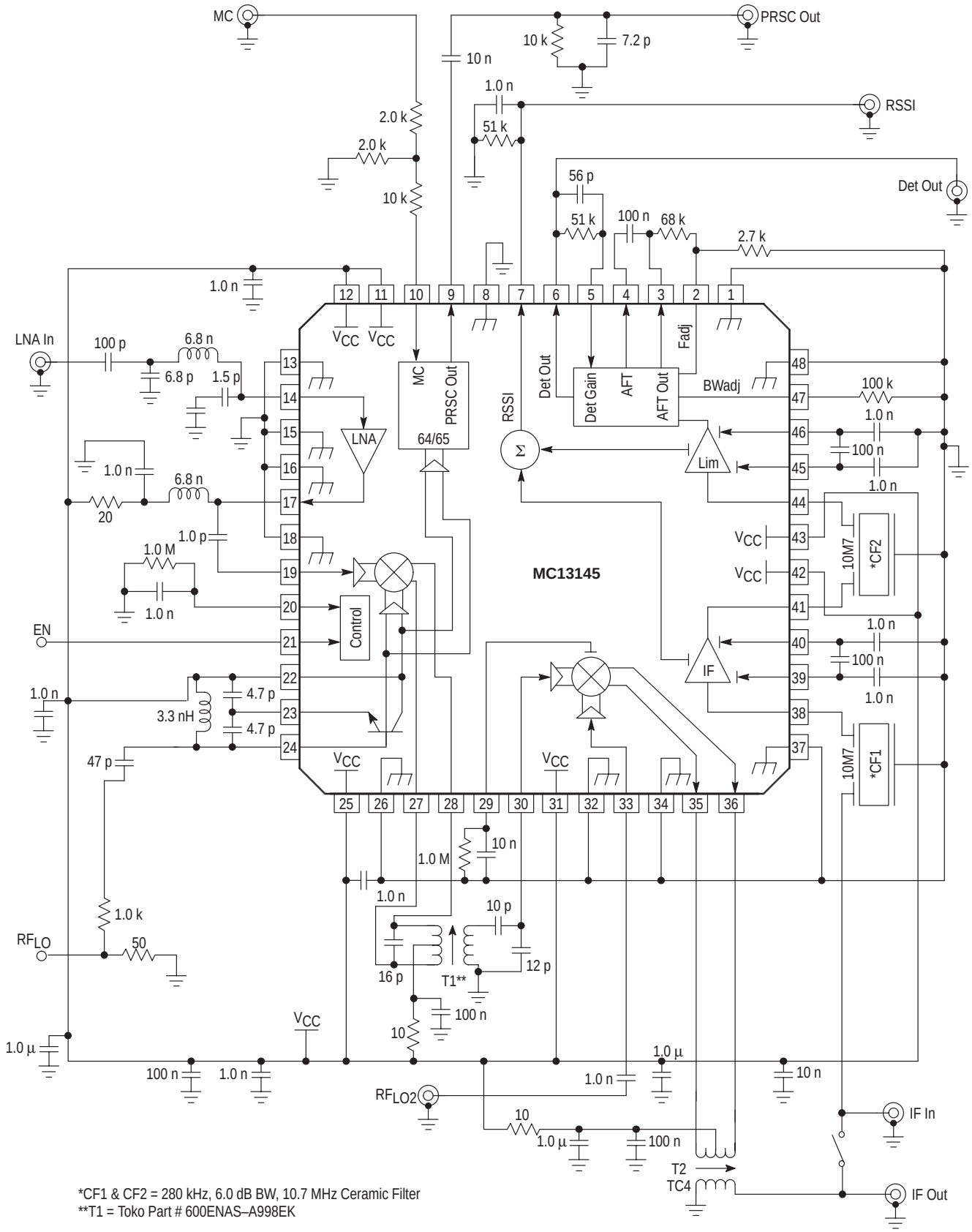
RECEIVER AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.6 Vdc; RF In = 1.0 GHz; 1st LO Freq = 1070.7 MHz; 2nd LO Freq = 60 MHz; f_{mod} = 1.0 kHz; f_{dev} = ±40 kHz; IF filter bandwidth = 280 kHz, unless otherwise noted. See Figure 1 Test Circuit)

Characteristics	Input Pin	Measure Pin	Symbol	MIn	Typ	Max	Unit
SINAD @ –110 dBm LNA Input	LNA In	Det Out	SINAD	12	20	–	dB
12 dB SINAD Sensitivity (Apps Circuit with C–message filter at DetOut)	LNA In	Det Out	$SINAD_{12dB}$	–	–115	–	dBm
30 dB SINAD Sensitivity (No IF filter distortion within ±40 kHz)	LNA In	Det Out	$SINAD_{30dB}$	–	–100	–	dBm
SINAD Variation with IF Offset of ±40 kHz (No IF filter distortion within ±40 kHz)	LNA In	Det Out	–	–	5.0	–	dB
Noise Figure: LNA, 1st Mixer & 2nd Mixer	LNA In	IF Out	NF	–	3.5	5.0	dB
Power Gain: LNA, 1st Mixer & 2nd Mixer	LNA In	IF Out	G	15	19	25	dB
RSSI Dynamic Range	IF In	RSSI	–	–	80	–	dB
RSSI Current	IF In	RSSI	–				μA
–10 dBm @ IF Input				35	40	55	
–20 dBm @ IF Input				–	35	–	
–30 dBm @ IF Input				–	30	–	
–40 dBm @ IF Input				–	25	–	
–50 dBm @ IF Input				15	20	37	
–60 dBm @ IF Input				–	15	–	
–70 dBm @ IF Input				–	10	–	
–80 dBm @ IF Input				–	5.0	–	
–90 dBm @ IF Input				–	1.0	7.0	
Input 1.0 dB Compression Point(Measured at IF output)			P_{in1dB}	–	–18	–	dBm

RECEIVER AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.6 Vdc; RF In = 1.0 GHz; 1st LO Freq = 1070.7 MHz; 2nd LO Freq = 60 MHz; f_{mod} = 1.0 kHz; f_{dev} = ±40 kHz; IF filter bandwidth = 280 kHz, unless otherwise noted. See Figure 1 Test Circuit)

Characteristics	Input Pin	Measure Pin	Symbol	MIn	Typ	Max	Unit
Input 3rd Order Intercept Point (Measured at IF output)			IIP3	–	–8.0	–	dBm
Demodulator Output Swing (50 k || 56 pF Load)	IF In	Det Out	V_{out}	0.8	1.0	1.2	V_{pp}
Demodulator Bandwidth (±1.0 dB bandwidth)		Det Out	BW	–	100	–	kHz
Prescalar Output Level (10 kΩ//8.0 pF load) Prescaler 64 Frequency = 16.72968 MHz Prescaler 65 Frequency = 16.4723 MHz		$PRSC_{out}$	V_{out}	 0.4 0.4	 0.51 0.51	 0.6 0.6	V_{pp}
MC Current Input (High)		MC	I_{ih}	70	100	130	µA
MC Current Input (Low)		MC	I_{il}	–130	–100	–70	µA
Input high voltage		Enable	V_{ih}	V_{CC} – 0.4	–	V_{CC}	V
Input low voltage		Enable	V_{il}	0	–	0.4	V
Input Current		Enable	I_{in}	–50	–	50	µA
PLL Setup Time [Note 1]	MC	$PRSC_{out}$	T_{PLL}	–	10	–	nS
SNR @ –30 dBm Signal Input (<40 kHz deviation;with C–Message Filter)				–	50	–	dB
Total Harmonic Distortion (<40 kHz deviation;with C–Message Filter)				–	1.0	–	%
Spurious Response SINAD (RF In: –50 dBm)				–	12	–	dB

Figure 1. Test Circuit



*CF1 & CF2 = 280 kHz, 6.0 dB BW, 10.7 MHz Ceramic Filter
**T1 = Toko Part # 600ENAS–A998EK

CIRCUIT DESCRIPTION

General

The MC13145 is a low power dual conversion wideband FM receiver incorporating a split IF. This device is designated for use as the receiver in analog and digital FM systems such as 900 Mhz ISM Band Cordless phones and wideband data links with data rates up to 150kbps. It contains a 1st and 2nd mixer , 1st and 2nd local oscillator, Received Signal Strength Indicator (RSSI), IF amplifier, limiting IF, a unique coilless quadrature detector, and a device enable function.

Current Regulation/Enable

The MC13145 is designed for battery powered portable applications. Supply current is typically 27 mA at 3.6 Vdc.

Temperature compensating, voltage independent current regulators are controlled by the Enable Pin where ”high” powers up and ”low” powers down the entire circuit.

Low Noise Amplifier (LNA)

The LNA is a cascoded common emitter amplifier configuration. Under very large RF input signals, the DC base current of the common emitter and cascode transistors can become very significant. To maintain linear operation of the LNA, adequate dc current source is needed to establish the 2Vbe reference at the base of the RF cascoded transistor and to provide the base voltage on the common emitter transistor. A sensing circuit, together with a current mirror guarantees that there is always sufficient dc base current available for the cascode transistor under all power levels.

1st and 2nd Mixer

Each mixer is a double–balanced class AB four quadrant multiplier which may be externally biased for high mixer dynamic range. Mixer input third order intercept point of up to 17 dBm is achieved with only 7.0 mA of additional supply current. The 1st mixer has a single–ended input at 50 Ω and operates at 1.0 GHz with –3.0 dB of power gain at approximately 100 mVrms LO drive level. The mixers have open collector differential outputs to provide excellent mixer dynamic range and linearity.

1st Local Oscillator

The 1st LO has an on–chip transistor which operates with coaxial transmssion line and LC resonant elements up to 1.8 GHz. A VCO output is available for multi–frequency operation under PLL synthesizer control.

RSSI

The received signal strength indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output (Pin 7) is derived by summing the currents from the IF and limiting amplifier stages. An increase in RSSI dynamic range, particularly at higher input signal levels is achieved. The RSSI circuit is designed to provide typically 80 dB of dynamic range with temperature compensation.

Linearity of the RSSI is optimized by using external ceramic bandpass filters which have an insertion loss of 4.0 dB and 330 Ω source and load impedance.

IF Amplifier

The first IF amplifier section is composed of three differential stages with the second and third stages contributing to the RSSI. This section has internal DC feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 40 dB up to 40MHz.

The fixed internal input impedance is 330 Ω. When using ceramic filters requiring source and load impedances of 330 Ω, no external matching is necessary. Overall RSSI linearity is dependent on having total midband attenuation of 10 dB (4.0 dB insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the IF amplifier is buffered and the impedance is 330 Ω.

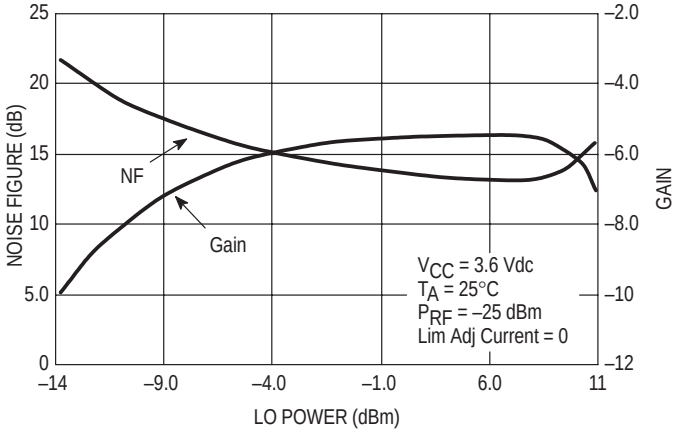
Limiter

The limiter section is similar to the IF amplifier section except that five stages are used with the middle three contributing to the RSSI. The fixed internal input impedance is 330 Ω. The total gain of the limiting amplifier section is approximately 84 dB. This IF limiting amplifier section internally drives the coilless quadrature detector section.

Coilless Quadrature Detector

The coilless detector is a unique design which eliminates the conventional tunable quadrature coil in FM receiver systems. The frequency detector implements a phase locked loop with a fully integrated on chip relaxation oscillator which is current controlled and externally adjusted, a bandwidth adjust, and an automatic frequency tuning circuit. The loop filter is external to the chip allowing the user to set the loop dynamics. Two outputs are used: one to deliver the audio signal (detector output) and the other to filter and tune the detector (AFT).

Figure 2. 2nd Mixer NF & Gain versus LO Power



Evaluation PCB

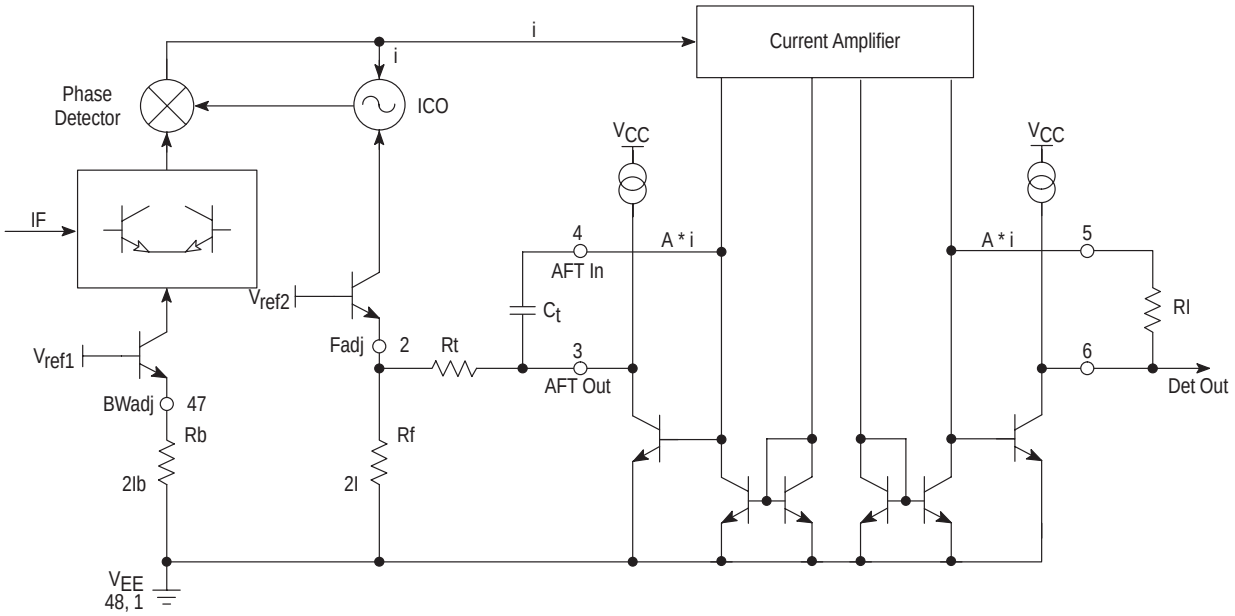
The evaluation PCB is a versatile board which allows the MC13145 to be configured as a dual–conversion receiver, or to characterize individual operating parameters.

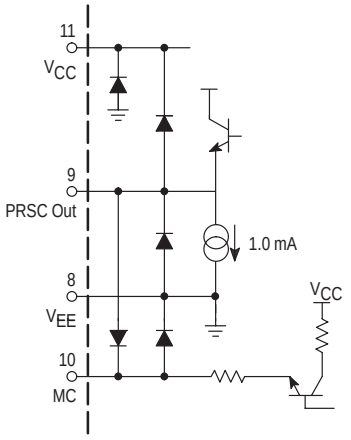
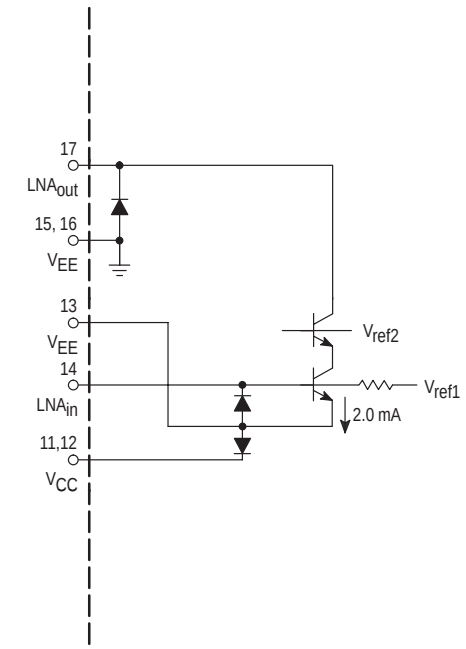
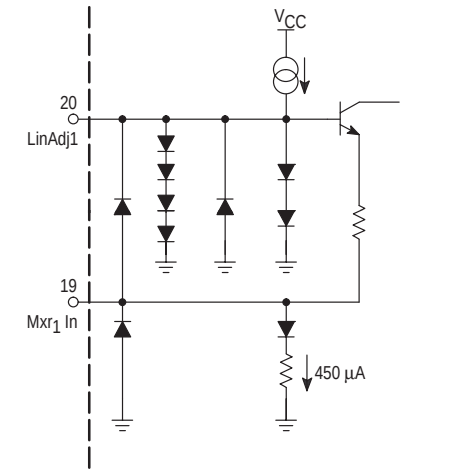
The general purpose schematic and associated parts list for a typical application are given in Figure 15. Please refer to AN1687/D and AN1691/D for additional details and applications for the device.

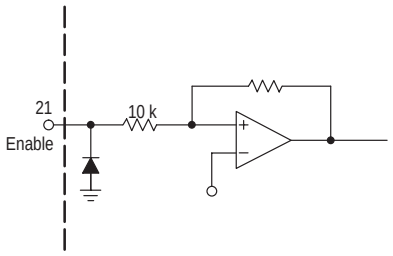
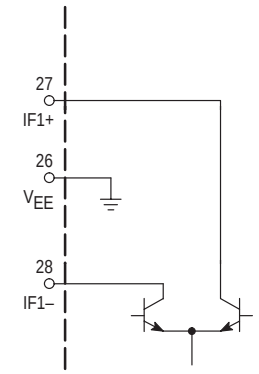
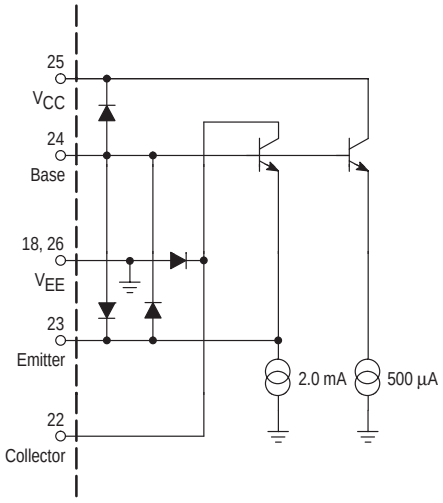
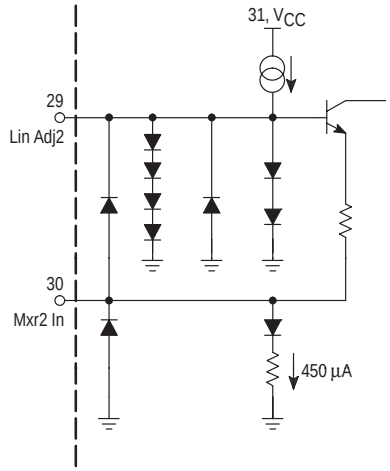
PIN FUNCTION DESCRIPTION

Pin	Symbol/Type	Description	Description
47	BWadj	See Figure 3.	**COILLESS DETECTOR** **Bandwidth Adjust** The deviation bandwidth of the detector response is determined by the combination of an on–chip capacitor and an external resistor to ground.
2	F_{adj}		**Frequency Adjust** The free running frequency of the detector oscillator is defined by the combination of an on–chip capacitor and an external resistor, Radj from frequency adjust pin to ground.
1, 48	V_{EE}		**V_{EE}, Negative Supply** These pins are V_{EE} supply for the coilless detector circuit.
3	AFT Out		**AFT Out** The AFT is low pass filtered with a corner frequency below the audio bandwidth allowing the error to be added to the center frequency adjust signal at Fadj, Pin 2. The low frequency high pass corner is set by the external capacitor, Ct from AFT out (Pin 3) to AFT in (Pin 4) and external resistor, Rt from AFT out to Fadj (Pin 2).
4	AFT In		**AFT In** The AFT in is used to set the buffer transfer function.
5	Det Gain		**Detector Gain** The AFT buffer is used to set the buffer transfer function.
6	Det Out		**Detector Output** Set gain and output level of detector with resistor to Det Out Pin.

Figure 3. Coilless Detector Internal Circuit



Pin	Symbol/Type	Description	Description
8	V_{EE}		**V_{EE}, Negative Supply Voltage**
9	PRSCout		**Prescaler Output** The prescaler output provides typically 500 mVpp drive to the fin pin of a PLL synthesizer. Conjugately matching the interface will increase the drive delivered to the PLL input.
10	MC		**Dual Modulus Control Current Input** This requires a current input of typically 200 μApp.
11, 12	V_{CC}		**V_{CC}, Positive Supply** V_{CC} pin is taken to the incoming positive battery or regulated dc voltage through a low impedance trace on the PCB. It decoupled to V_{EE} ground at the pin of the IC.
14	LNA In		**LNA In** The input is the base of the common emitter transistor. Minimum external matching is required to optimize the input return loss and gain.
13, 15, & 16	V_{EE}		**V_{EE}, Negative Supply** V_{EE} pin is taken to an ample dc ground plane through a low impedance path. The path should be kept as short as possible. A minimum two sided PCB is recommended so that ground returns can be easily made through via holes.
17	LNAout		**LNA Out** The output is from the collector of the cascode transistor amplifier. The output may be conjugately matched with a shunt L (needed to dc bias the open collector), and series L and C network.
19	Mxr_1In		**1st Mixer Input** The mixer input impedance is broadband 50 Ω for applications up to 2.4 GHz. It easily interfaces with a RF ceramic filter.
20	Lin Adj1		**1st Mixer Linearity Control** The mixer linearity control circuit accepts approximately 0 to 300 μA control current to set the dynamic range of the mixer. An Input Third Order Intercept Point, IIP3 of 17 dBm may be achieved at 300 μA of control current.

Pin	Symbol/Type	Description	Description
21	Enable		**Enable** Enable the receiver by pulling the pin up to V_{CC}.
26	V_{EE}		**V_{EE}, Negative Supply** V_{EE} supply for the mixer IF output.
27	IF1+		**1st Mixer Outputs** The Mixer is a differential open collector output configuration which is designed to use over a wide frequency range. The differential output of the mixer has back to back diodes across them to limit the output voltage swing and to prevent pulling of the VCO. Differential to single–ended circuit configuration and matching options are shown in the Test Circuit. Additional mixer gain can be achieved by matching the outputs for the desired passband Q.
28	IF1–		
22	Collector		**On–board VCO Transistor** The transistor has the emitter, base, collector, VCC, and VEE pins available. Internal biasing which is compensated for stability over temperature is provided. It is recommended that the base pin is pulled up to VCC through an RFC chosen for the particular oscillator center frequency .
23	Emitter		
24	Base		
25	V_{CC}		**V_{CC}, Positive Supply Voltage** A VCC pin is provided for the VCO. The operating supply voltage range is from 2.7 Vdc to 6.5 Vdc.
18, 26	V_{EE}		**V_{EE}, Negative Supply Voltage**
29	Lin Adj2		**2nd Mixer Linearity Control** The mixer linearity control circuit accepts approximately 0 to 400 µA control current to set the dynamic range of the mixer. An Input Third Order Intercept Point, IIP3 of 17 dBm may be achieved at 400 µA of control current. IIP3 default with no external bias is 10 dBm.
30	Mxr2 In		**2nd Mixer Input** The mixer input impedance is broadband 50 Ω.
31	V_{CC}		**V_{CC}, Positive Supply**

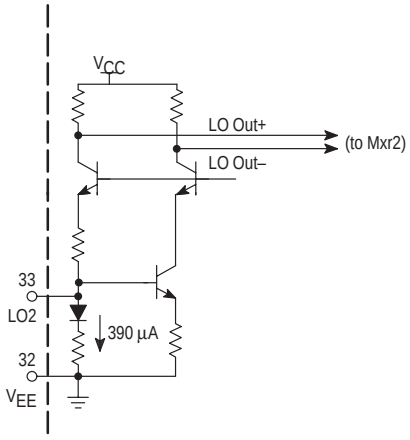
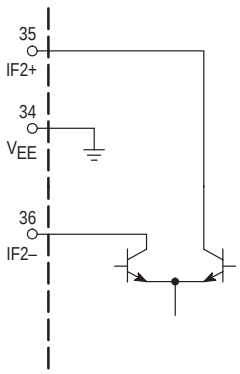
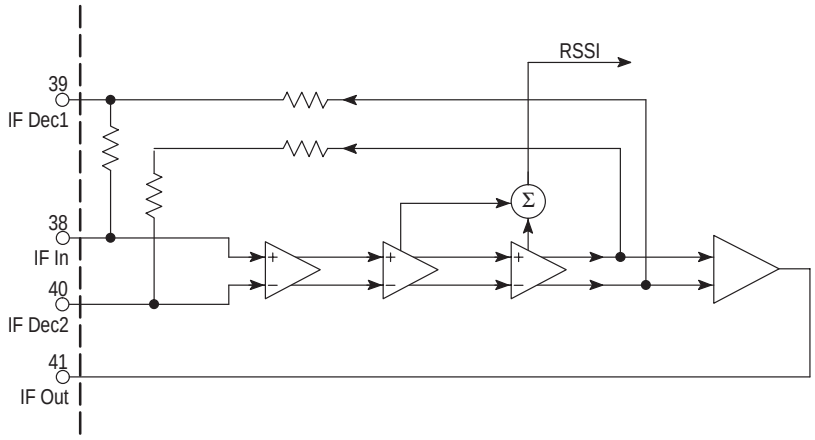
Pin	Symbol/Type	Description	Description
32, 34	V_{EE}		**V_{EE}, Negative Supply Voltage**
33	LO2		**2nd Local Oscillator** The 2nd LO input impedance is broadband 50 Ω; it is driven from an external 50 Ω source. Typical level is –15 to –10 dBm.
35	IF2+		**2nd Mixer Outputs** The Mixer is a differential open collector configuration.
36	IF2–		
37	V_{EE}	See Figure 4.	**V_{EE}, Negative Supply Voltage**
38	IF In		**IF Amplifier Input** IF amplifier input source impedance is 330 Ω.. The three stage amplifier has 40 dB of gain with 3.0 dB bandwidth of 40 MHz.
39, 40	IF Dec1, IF Dec2		**IF Decoupling** These pins are decoupled to V_{CC} to provide stable operation of the limiting IF amplifier.
41	IF Out		**IF Amplifier Output** IF amplifier output load impedance is 330 Ω.
42	V_{CC}		**V_{CC}, Positive Supply Voltage**
7	RSSI		**RSSI** The RSSI circuitry in the 2nd & 3rd amplifier stages outputs a current when the output of the previous stage enters limiting. The net result is a RSSI current which represents the logarithm of the IF input voltage. An external resistor to ground is used to provide a voltage output.

Figure 4. IF Amplifier Functional Diagram



Pin	Symbol/Type	Description	Description
43	V_{CC}	See Figure 5.	**V_{CC}, Positive Supply Voltage**
44	Lim In		**Limiting Amplifier Input** Limiting amplifier input source impedance is 330 Ω. This amplifier has 84 dB of gain with 3.0 dB bandwidth of 40 MHz; this enables the IF and limiting ampliers chain to hard limit on noise.
45, 46	Lim Dec1, Lim Dec2		**If Decoupling** These pins are decoupled to V_{CC} to provide stable operation of the 2nd IF limiting amplifier.
7	RSSI		**RSSI** The RSSI circuitry in the 2nd, 3rd, & 4th amplifier stages outputs a current when the output of the previous stage enters limiting. The net result is a RSSI current which represents the logarithm of the IF input voltage. An external resistor to ground is used to provide a voltage output.

Figure 5. Limiter Amplifier Functional Diagram

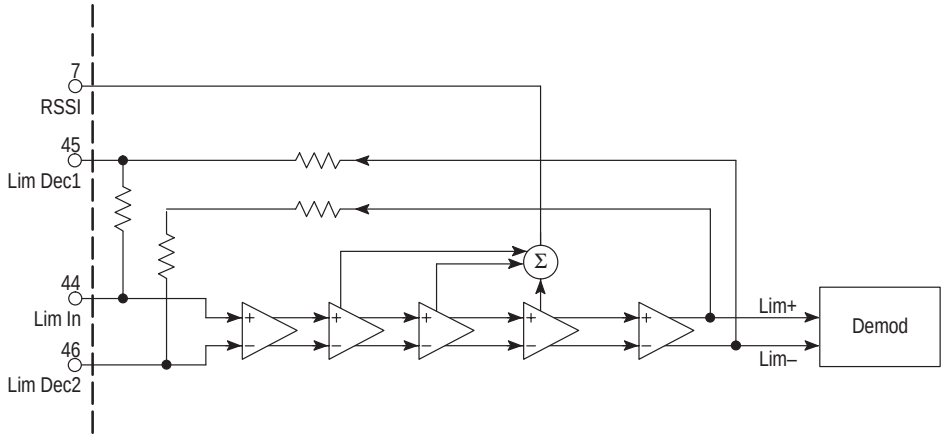


Figure 6. 2nd Mixer Gain versus LO Drive

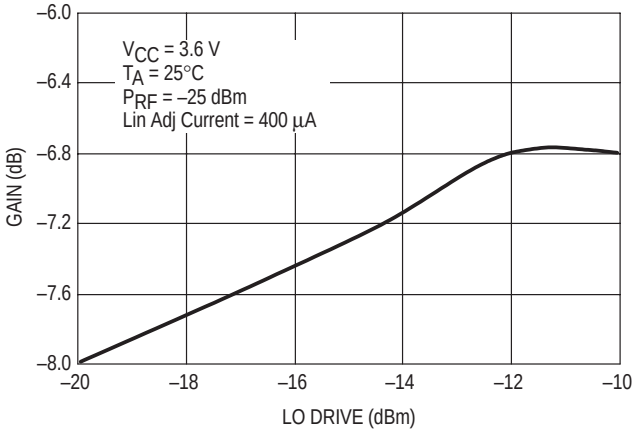


Figure 7. 2nd Mixer P_{1dB} versus LO Drive

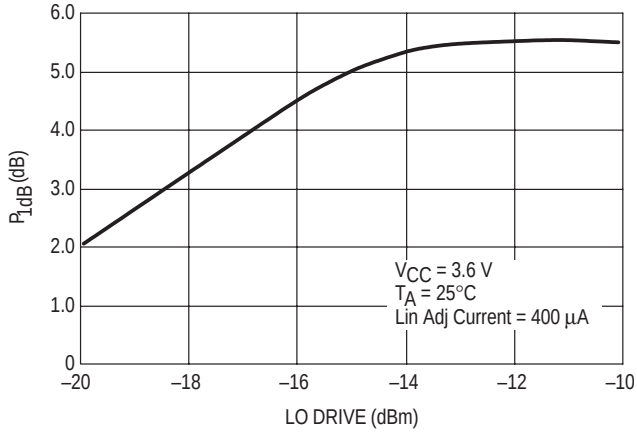


Figure 8. 2nd Mixer IP3/P_{1dB} versus Lin Adj Current

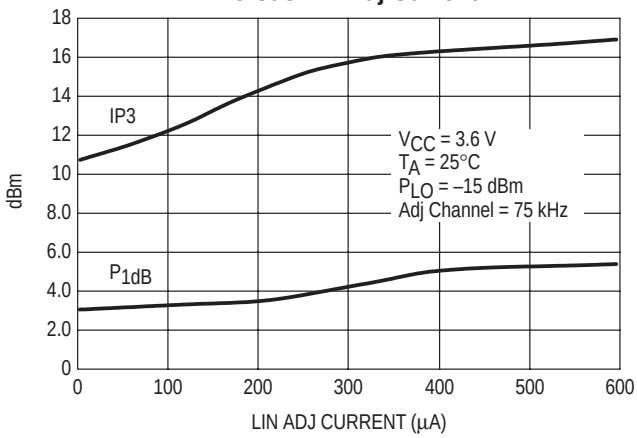


Figure 9. 2nd Mixer Gain versus Lin Adj Current

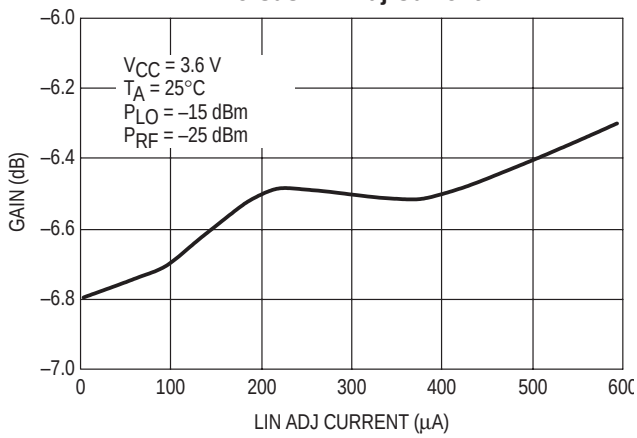
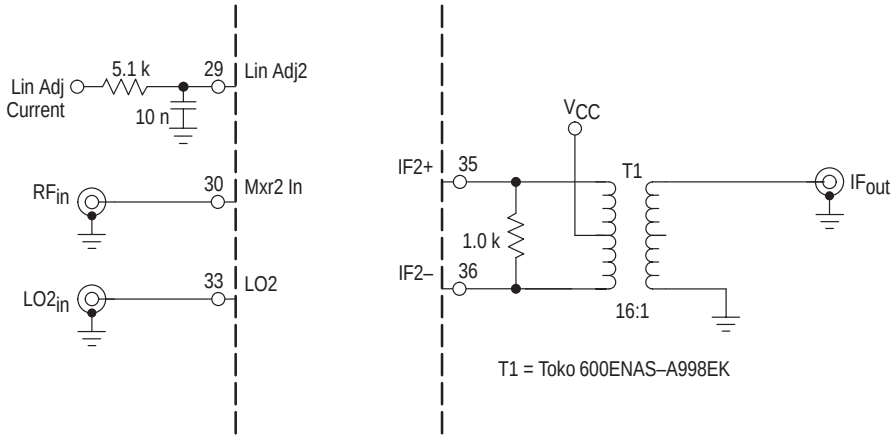


Figure 10. Test Circuit for Figures 6 thru 9.



APPLICATION INFORMATION

Input Matching / Components

It is desirable to use a RF ceramic or SAW filter before the mixer to provide image frequency rejection. The filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 1.5 to 2.5 dB insertion loss. The evaluation PC board layout accommodates ceramic RF filters which are offered by various suppliers.

Interface matching between the LNA, RF filter and the mixer will be required. The interface matching networks shown in the evaluation circuit are designed for 50 Ω interfaces.

1st Mixer Output & 2nd Mixer Input Interface Matching

In a wideband system the primary sensitivity of the receiver backend may be achieved before the last mixer. The evaluation circuit shows the matching and impedance transformation network bewtween the 1st mixer open collector differential outputs and 2nd mixer single ended 50 ohm input. This adjustable shielded transformer and tapped capacitor transform network does two things: 1) bandpass limits the 1st IF signal with a loaded Q of approximately 40 and 2) provides adequate second image rejection and a low cost alternative to a SAW filter.

However, a SAW filter may be selected as a more costly alternative while providing improved 2nd image rejection and a fixed tuned 1st IF filter.

2nd Mixer & Limiting IF Matching / Filtering

A simple LCR network is needed to interface the 2nd mixer differential outputs to 330 ohm ceramic filters or directly to the 330 ohm IF input. TDK, Toko and Murata offer single 10.7 MHz ceramic filters with various 3.0 dB bandwidths from 110 to 380 kHz. Murata offers a series–parallel resonator pair (part number KMFC545) with a 3.0 dB bandwidth of ±325 kHz and a maximum insertion loss of 5.0 dB. However, even the series–parallel ceramic filter pair yields only a maximum bandpass of 650 kHz. In some data applications a wider band IF bandpass is necessary.

Local Oscillators – VHF/UHF Applications

The on–chip transistor may be used for HF and VHF local oscillator with higher order overtone crystals. It is recommended that a Butler overtone oscillator configuration is used. The crystal is driven from the emitter and is coupled to the high impedance base through a capacitive tap network. Operation at the desired overtone frequency is ensured by the parallel resonant circuit formed by an inductor and the tap capacitors and parasitic capacitances of the on–chip transistor and PC board. A high tolerance, high Q ceramic or air wound surface mount component may be used if the other components have tight enough tolerances; however, a variable inductor provides an adjustment for gain and frequency of the resonant tank ensuring lock up and start–up of the crystal oscillator. The overtone crystal is chosen with ESR of typically 80 ohms and 120 ohms maximum; if the resistive loss in the crystal is too high the performance of oscillator may be impacted by lower gain margins.

A series LC network to ac ground (which is V_{CC}) is comprised of the inductance of the base lead of the on–chip transistor and PC board traces and tap capacitors. Parasitic oscillations often occur in the 200 to 900 MHz range. A small resistor is placed in series with the base (pin 9) to cancel the negative resistance associated with this undesired mode of oscillation. Since the base input impedance is so large a small resistor in the range of 27 to 68 ohms has very little effect on the desired Butler mode of oscillation.

The crystal parallel capacitance, C_O, provides a feedback path that is low enough in reactance at frequencies of 5th overtones or higher to cause trouble. C_O has little effect near resonance because of the low impedance of the crystal motional arm (R_m–L_m–C_m). As the tunable inductor which forms the resonant tank with the tap capacitors is tuned off the crystal resonant frequency it may be difficult to tell if the oscillation is under crystal control. Frequency jumps may occur as the inductor is tuned. In order to eliminate this behavior an inductor, L_O, is placed in parallel with the crystal. L_O is chosen to be resonant with the crystal parallel capacitance, C_O, at the desired operation frequency. The inductor provides a feedback path at frequencies well below resonance; however, the parallel tank network of the tap capacitors and tunable inductor prevent oscillation at these frequencies.

Coilless Detector

The coilless detector (see Figure 3) is unique and offers cost and performance advantages over the conventional quadrature detector. It consists of a current controlled oscillator (ICO) and a phase detector. The error current, I is also amplified to provide an output, and the output is duplicated and filtered and fed back to the oscillator to provide automatic fine tuning (AFT).

The oscillator free running frequency, fo is set by Rf and is calculated by the following equation where C is approximately 4.0 pF:

$$fo = 1/(8*Rf*C)$$

The demodulator bandwidth is set by Rb and is shown in Figure 14.

The AFT is filtered by Ct and Rt. The low pass pole creates a high pass pole in the overall demodulator frequency response at:

$$A/(2*\pi*Ct*Rt)$$

where A, the current gain = 10.

Typical coilless detector output level is:

$$V_{out}(peak) = (f_{peak\ dev}/f_{IF})*A*i*RI$$

For example, if peak deviation is 25 kHz, i = 250 μA at f_{IF} = 10.7 MHz, and RI is 50 kΩ; then V_{out} is 292 mVp or 584 mVpp.

The AFT Out pin is capable of voltage swings from about 300 mV to V_{CC} – 300 mV. At these extreme values, the AFT circuit can become saturated and very long detector lock–up times may be observed. It is best, therefore, to limit the AFT Out swing from about 500 mV to V_{CC} – 500 mV and attempt to center the AFT Out voltage at V_{CC}/2 for a detector lock condition.

As an example, for V_{CC} = 2.7 V, the ideal AFT Out voltage at lock would be 1.35 V, with an available swing of 0.5 V to 2.2 V (1.7 V total). If the AFT tuning range is to be ±500 kHz, this corresponds to an adjustment current of 1.0 MHz/f_{IF}*i. From Figure 11, to set f_{IF} at 10.7 MHz, i is approximately 240 μA, and the total adjustment current range is therefor about 22.4 μA over a 1.7 V total swing, or Rt = 75.9 k. At lock,

current equaling (AFT Out – Fadj)/Rt will be flowing into the Fadj node. This current then is approximately (1.35 V – 0.7 V)/75.9 kΩ or 8.6 μA. The Fadj resistor, Rf, is therefore equal to 0.7 V/(240 μA + 8.6 μA) or about 2.82 kΩ.

Figure 11. Fadj Current versus IF Frequency

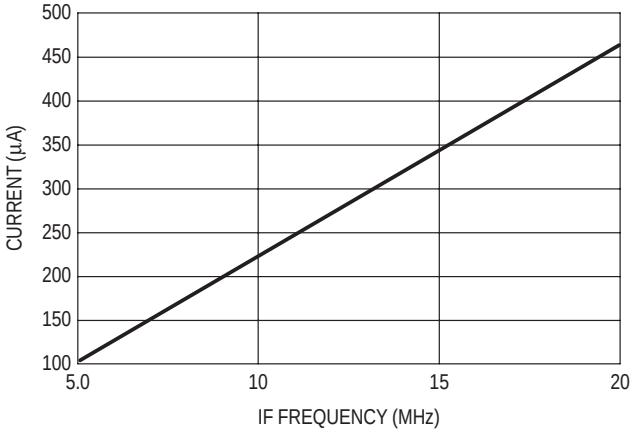


Figure 12. Fadj Resistor versus IF Frequency

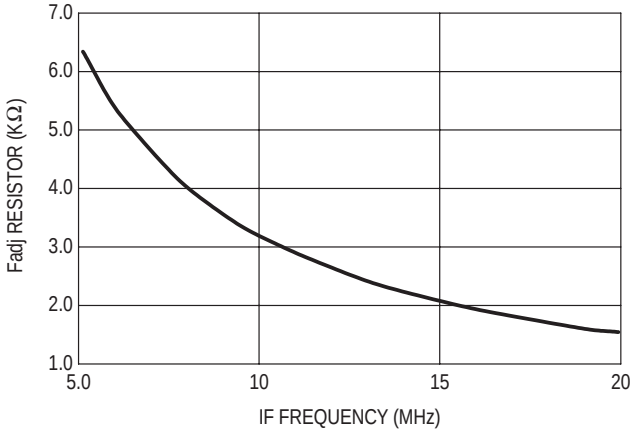


Figure 13. BWadj Resistor versus BWadj Current

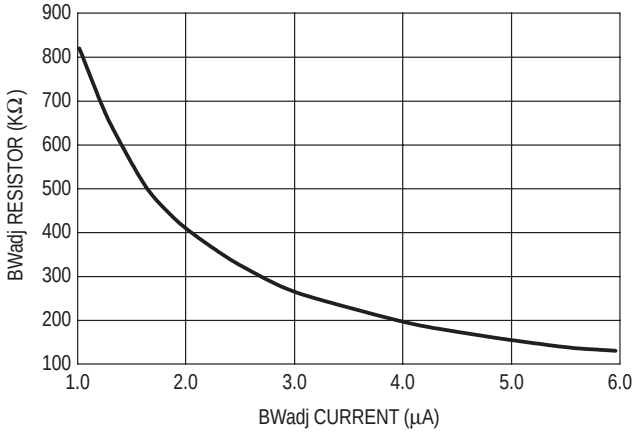


Figure 14. IF Frequency versus BWadj Current

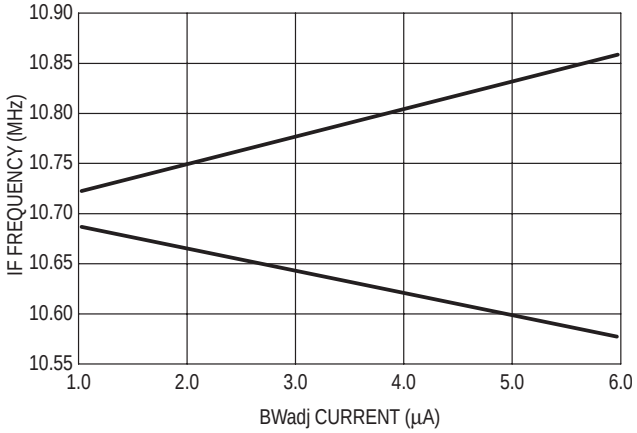


Table 1. LNA S–Parameters: 3.6 Vdc

Freq (MHz)	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 mag	S22 Ang
25	0.84	–3.0	10.8	176	0.00005	–27	1.0	–1.2
50	0.84	–71	10.7	171	0.0004	76	1.0	–3.7
100	0.83	–15	10.3	162	0.0006	61	0.99	–4.9
150	0.81	–22	10.	154	0.0011	91	0.99	–7.3
200	0.78	–28	9.6	147	0.001	60	0.99	–9.7
300	0.73	–41	9.0	132	0.002	42	0.99	–15
400	0.66	–50	7.8	116	0.00070	22	0.95	–19
450	0.64	–54	7.4	111	0.0014	39	0.96	–21
500	0.62	–59	7.0	106	0.0009	69	0.96	–23
750	0.51	–77	5.5	80	0.0013	–51	0.94	–33
800	0.49	–80	5.2	75	0.002	–80	0.93	–36
850	0.47	–81	4.9	71	0.004	–120	0.92	–37
900	0.46	–82	4.6	67	0.0057	–130	0.92	–38
950	0.44	—82	4.3	62	0.008	–142	0.91	–40
1000	0.45	–81	3.9	58	0.014	–162	0.95	–41
1250	0.55	–94	3.5	47	0.029	140	0.099	–50
1500	0.48	–120	3.1	24	0.02	63	0.94	–65
1750	0.43	–126	2.5	6.9	0.0066	79	0.93	–74
2000	0.43	–135	2.1	–9.9	0.0099	129	0.92	–85
2250	0.45	–145	1.8	–27	0.017	133	0.91	–96
2500	0.47	–155	1.5	–43	0.021	132	0.89	–106
2750	0.51	–167	1.2	–60	0.03	130	0.88	–118
3000	0.55	–180	1.0	–78	0.039	120	0.85	–129

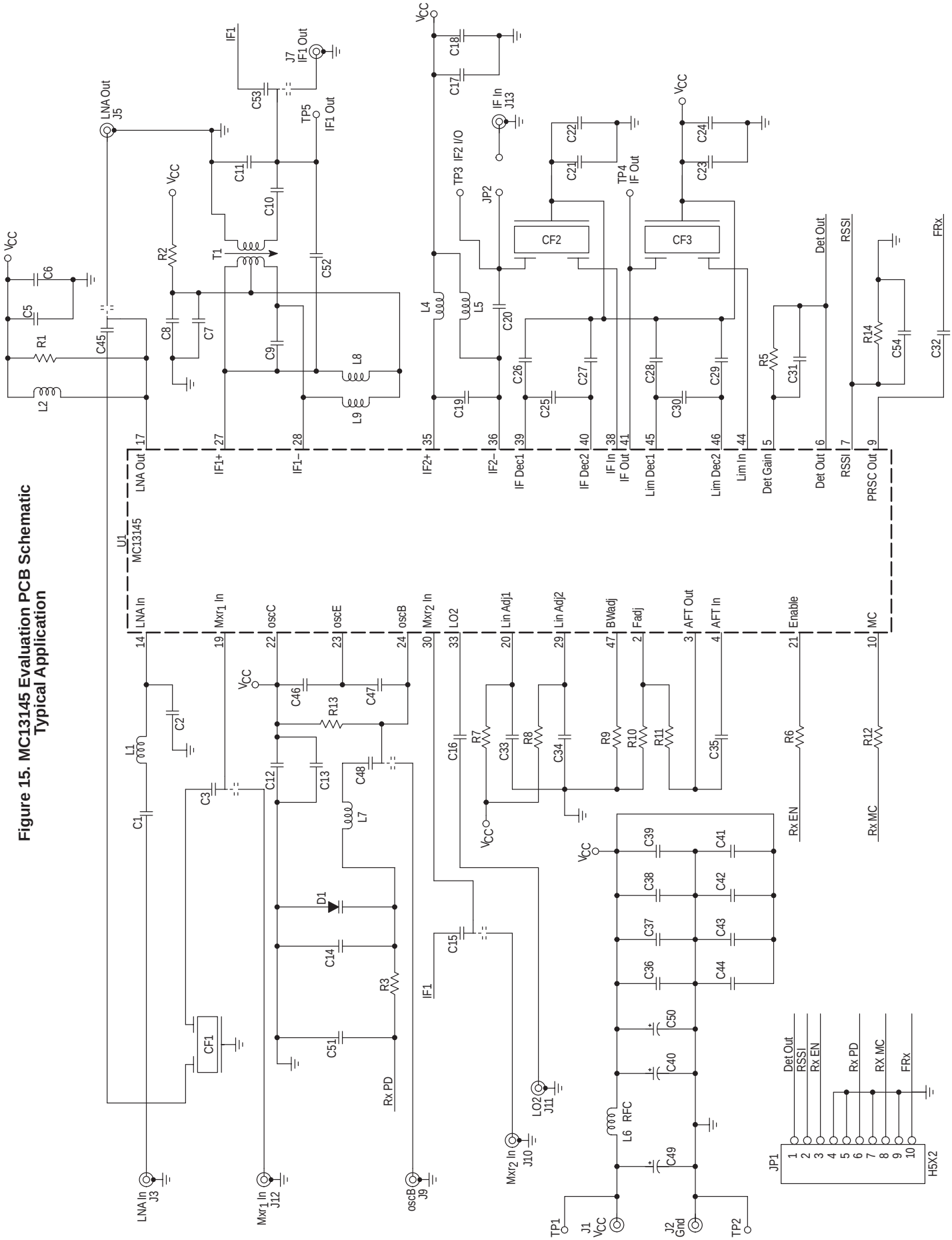


Figure 15. MC13145 Evaluation PCB Schematic
Typical Application

Figure 16. Evaluation PCB Component Side

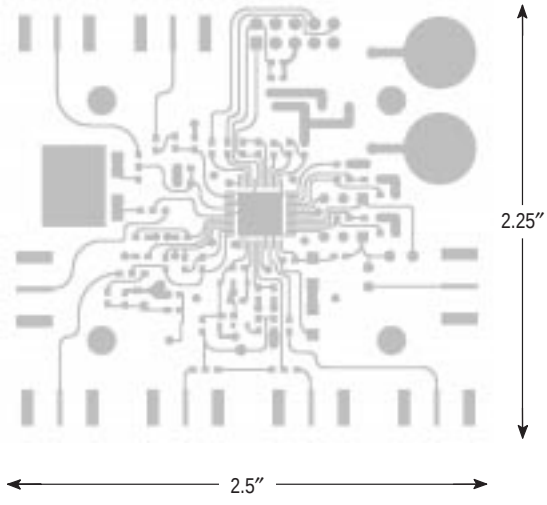
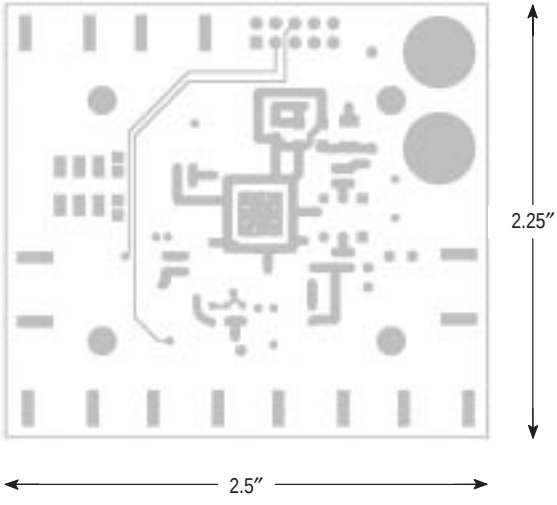
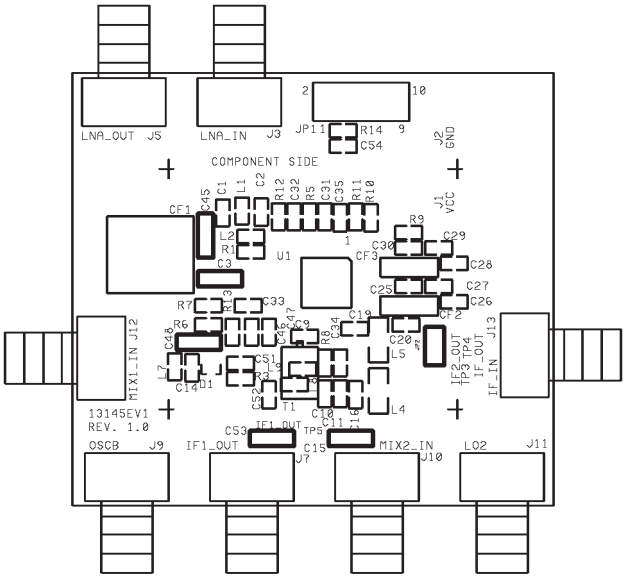
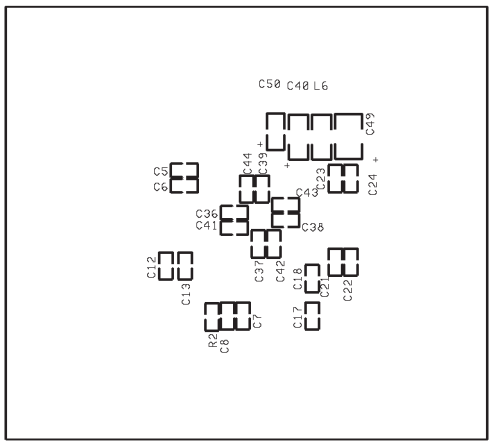


Figure 17. Evaluation PCB Solder Side







CF1	TDK CF6118702
	or TDK CF6118902
CF2,CF3	Toko Type CFSK Series SK107MX–AE–XXX
C1,C3,C5,C7,C13,C17,C31, C41,C42,C43,C44,C48,C51	100 p
C2	1.5 p
C6,C12,C21,C23,C26,C27, C28,C29,C33,C34,C36,C37, C38,C39,C54	1.0 n
C8,C15,C16,C18,C32,C53	0.01
C9	16 p
C10	10 p
C11	12 p
C14	2.0–4.0 p
C19	36 p
C20	39 p
C22,C24,C25,C30,C35	0.1
C40	10 μ
C45	3.3 p
C46,C47	2.0 p
C49	22
C50	1.0
R1,R7,R8,L8,L9,C52, J5,J7,J9,J10,J12,J13	No Component
D1	MMBV809LT1
L1	6.8 n
L2	5.6 n
L4, L5	2.7 μ
L6	RFC
L7	2.7 n
R2	10
R3	33 k
R5	27 k
R6,R11,R12,R14	51 k
R9	68 k
R10	2.85 k
R13	51 or RFC
T1	Toko A638AN–A099YWN
U1	MC13145FTA
J3,J11	SMA EF Johnson 142–0701–851
J1,J2	Bananna Johnson Components 108–0902–001
JP1	Header, 5x2

Default Units: Ohms, Microfarads, and Microhenries

Figure 18. Evaluation PCB Ground Plane

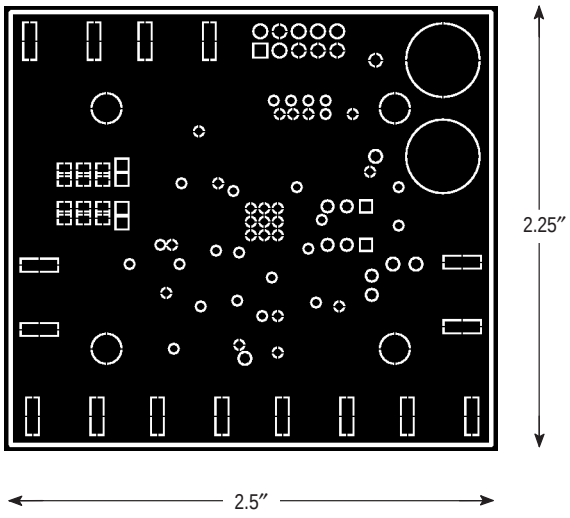
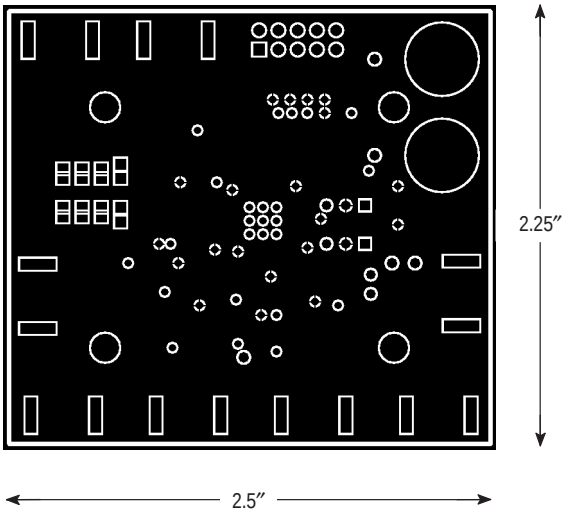


Figure 19. Evaluation PCB Power Plane



MOTOROLA

MC13146

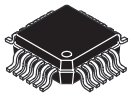
Low Power Integrated Transmitter for ISM Band Applications

The MC13146 is an integrated RF transmitter targeted at ISM band applications. It features a 50 Ω linear Mixer with linearity control, voltage controlled oscillator, divide by 64/65 dual modulus Prescaler and Low Power Amplifier (LPA). Together with the receiver chip (MC13145) and either baseband chip (MC33410 or MC33411A/B), a complete 900 MHz cordless phone system can be implemented. This device may be used in applications up to 1.8 GHz.

- Low Distortion LPA: $P_{out_1\ dB}$ Compression Point ≈ 10 dBm
- High Mixer Linearity: IIP3 = 10 dBm
- 50 Ω Mixer Input Impedance
- Differential Open Collector Mixer Output
- Low Power 64/65 Dual Modulus Prescaler (MC12054 type)
- 2.7 to 6.5 V Operation, Low Current Drain (25 mA @ 2.0 GHz)
- Powerdown Mode: <60 μA
- Usable up to 1.8 GHz

LOW POWER DC – 1.8 GHz TRANSMITTER

SEMICONDUCTOR TECHNICAL DATA

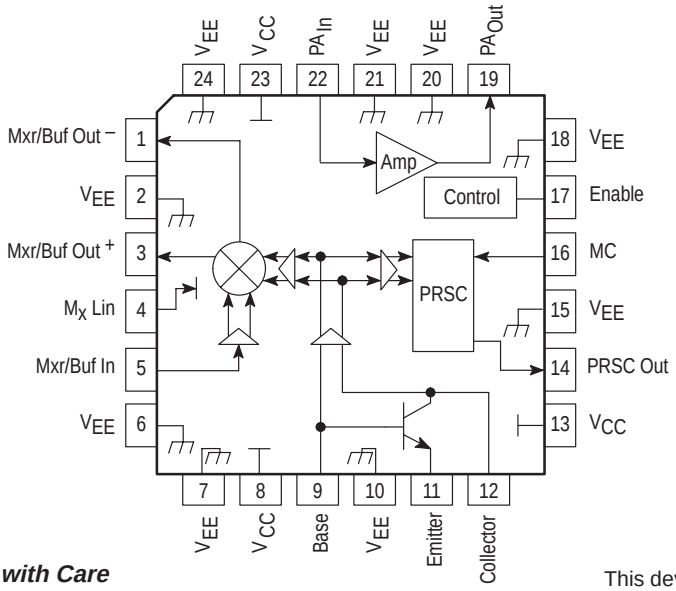


FTA SUFFIX
PLASTIC PACKAGE
CASE 977
(LQFP–24)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13146FTA	T_A = –20 to 70°C	LQFP–24

PIN CONNECTIONS



ESD Sensitive — Handle with Care

This device contains 268 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}(max)	7.0	Vdc
Junction Temperature	T_J(max)	150	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions, Electrical Characteristics tables or Pin Descriptions section.
2. Meets Human Body Model (HBM) ≤100 V and Machine Model (MM) ≤25 V. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (TA = 25°C)					
	VCC	2.7	–	6.5	Vdc
	VEE	–	0	–	Vdc
RF Frequency Range	f_{RF}	1.0	–	2500	MHz
Ambient Temperature Range	T_A	–20	–	70	°C
Maximum Input Signal Level	P_{IF}				
– with no damage		–	–10	–	dBm
– with minor performace degradation		–	15	–	dBm

TRANSMITTER DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.6 Vdc, no input signal, unless otherwise noted)

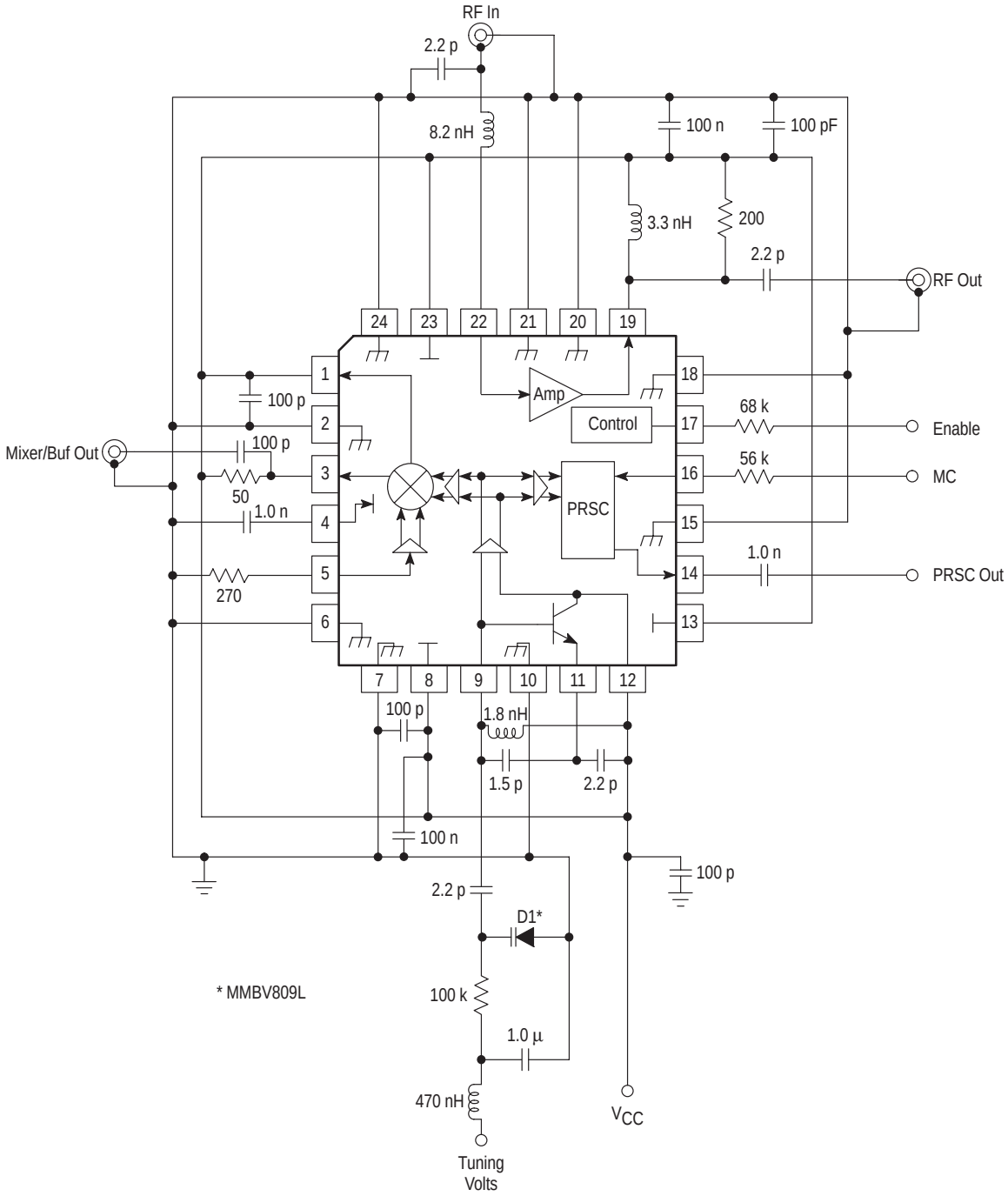
Characteristic	Symbol	Min	Typ	Max	Unit
Total Supply Current (Enable = V_{CC})	I_{total}	15	18	21	mA
Power Down Current (Enable = V_{EE})	I_{total}	-	30	100	µA
MC Current Input (High)	I_{ih}	70	100	130	µA
MC Current Input (Low)	I_{il}	–130	–100	–70	µA
Input high voltage	V_{ih}	V_{CC} – 0.4	–	–	V
Input low voltge	V_{il}	–	–	0.4	V
Input Current	I_{in}	–50	–	50	µA

TRANSMITTER AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.6 Vdc, Enable = 3.6 Vdc, per Test Circuit shown in Figure 1, unless otherwise noted)

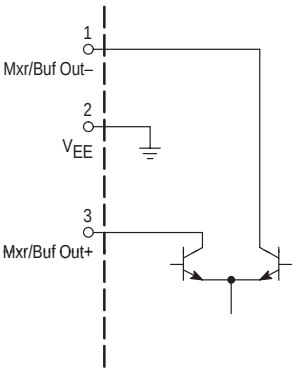
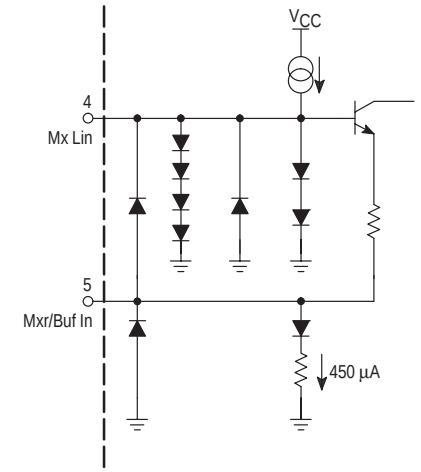
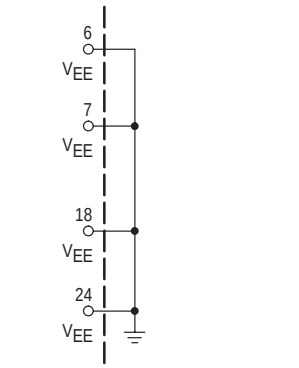
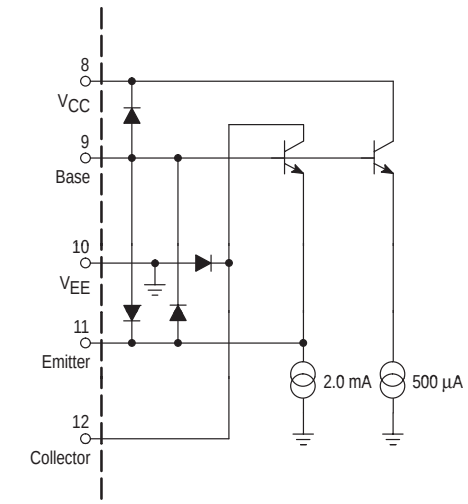
Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Amplifier Output Power (with external matching) @ 950 MHz; P_{in} = –19 dBm	PA_{in}	PA_{out}	P_{A_PO}	–4.5	–3.3	–2.1	dBm
Amplifier 1.0 dB Compression Point (@ 950 MHz = f_{IF_out})	PA_{in}	PA_{out}	$P_{1dBC.Pt.}$	–	8.0	–	dBm
Amplifier Output Harmonics (with external matching) @ 950 MHz; P_{in} = –19 dBm	PA_{in}	PA_{out}					dBc
2nd			P_{A-2f}	–25	–37	–	
3rd			P_{A-3f}	–35	–52	–	
Mixer/Buffer Output (@ 950 MHz = f_{osc}; Mixer input (Pin 5) pulled through 270 Ω resistor)		Buf_out+	P_{Mx/Buf_out}	–19	–18	–17	dBm
PLL Setup Time [Note 1]	MC	$PRSC_{out}$	T_{PLL}	-	10	–	nS
Mixer Input Third Order Intercept Point			IIP3	–	10	–	dBm
VCO Phase Noise (@ 10 kHz offset)		Buf_out+		–	–80	–	dBc/Hz
Prescalar Output Level (10 k || 8.0 pF Load)		$PRSC_{out}$		400	–	600	mVpp

NOTES: 1. MC input (50%) to $PRSC_{out}$ rising output (50%) for proper modulus selection.
2. Typical performance parameters indicate the potential of the device under ideal operation conditions.

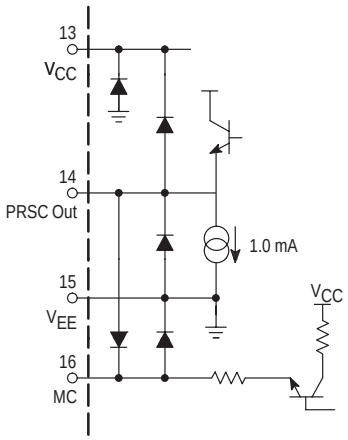
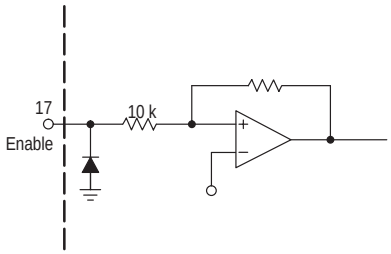
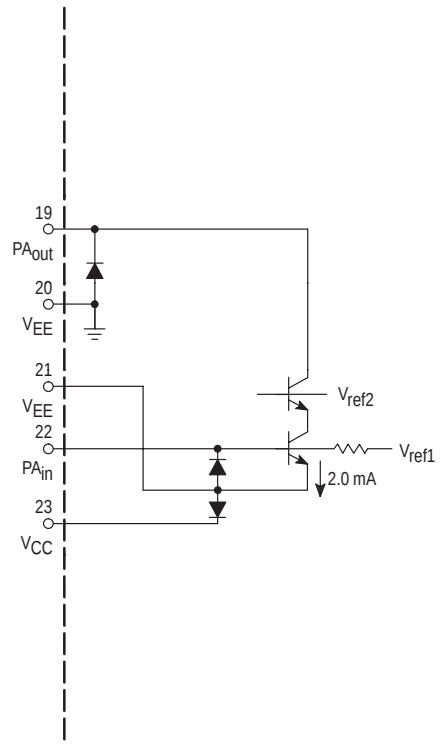
Figure 1. Test Circuit



PIN FUNCTION DESCRIPTION

Pin	Symbol/Type	Description	Description
1, 3	Mxr/Buf Out–, Mxr/Buf Out+		**Mixer/Buffer Outputs** The Mixer/Buffer is a differential open collector configuration which designed to use over a wide frequency range for up conversion as well as direct conversion. Differential to single–ended circuit configuration and matching options are discussed in the Circuit Description section. 6.0 dB of additional Mixer gain can be achieved by conjugately matching the outputs at the desired RF frequency.
2	V_{EE}		**V_{EE}, Negative Supply** This pin is V_{EE} supply for the mixer IF output. In the application PC board this pin is tied to a common V_{EE} trace with other V_{EE} pins.
4	Mx Lin		**Mixer Linearity Control** The mixer linearity control circuit accepts approximately 0 to 200 µA control current to set the dynamic range of the mixer. An Input Third Order Intercept Point, IIP3 of 17 dBm may be achieved at 200 µA of control current.
5	Mxr/Buf In		**Mixer/Buffer Input** The mixer input impedance is broadband 50 Ω for applications up to 2.4 GHz.
6, 7, 18, 24	V_{EE}		**V_{EE}, Negative Supply** These pins are substrate connections on the IC. In the application PC board these pins are tied to a common V_{EE} trace with other V_{EE} pins.
8	V_{CC}		**V_{CC}, Supply Voltage** Two V_{CC} pins are provided for the Local Oscillator and LO Buffer Amplifier. The operating supply voltage range is from 2.7 Vdc to 6.5 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as feasible to minimize inductive reactances along the trace. V_{CC} should be decoupled to V_{EE} at the IC pin.
9	Base		**On–board VCO Transistor** The transistor has the emitter, base, collector, V_{CC} and V_{EE} pins available. Internal biasing which is compensated for stability over temperature is provided. It is recommended that the base pin is pulled up to V_{CC} through an RFC chosen for the particular oscillator center frequency. The application circuit shows a Colpitts oscillator configuration.
10	V_{EE}		
11	Emitter		
12	Collector		

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
13	V_{CC}		**V_{CC}, Supply Voltage**
14	PRSC Out		**Prescaler Output** The prescaler output provides 500 mVpp drive to the F_{in} Pin of a PLL synthesizer. Conjugately matching the interface will increase the drive delivered to the PLL input.
15	V_{EE}		**V_{EE}, Negative Supply**
16	MC		**Dual Modulus Control Current Input** This requires a current input of typically 200 μApp.
17	Enable		**Transmitter Enable** Enable the transmitter by pulling the pin up to V_{CC}.
19	PA_{out}		**PA Out** The output is an open collector of the cascode transistor low power amplifier (LPA); it is externally biased. The output may be conjugately matched with a shunt L, and series L and C network.
20, 21	V_{EE}		**V_{EE}, Negative Supply** V_{EE} pin is taken to an ample dc ground plane through a low impedance path. The path should be kept as short as possible. A two sided PCB is implemented so that ground returns can be easily made through via holes.
22	PA_{in}		**PA In** The input is the base of the common emitter transistor. Minimum external matching is required to optimize the input return loss and gain.
23	V_{CC}		**V_{CC}, Positive Supply** V_{CC} pin is taken to the incoming positive battery or regulated dc voltage through a low impedance trace on the PCB. It is decoupled to V_{EE} ground at the pin of the IC.

CIRCUIT DESCRIPTION

General

The MC13146 consists of a low power amplifier, a 50 Ω linear mixer with linearity control, divide by 64/65 dual modulus prescaler and LPA. This device is designated for use as the low power transmitter in analog and digital FM systems such as UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services, PCS and 902 to 928 MHz cordless telephones. It features a mixer linearity control to preset or auto program the mixer dynamic range, an enable function and a wideband mixer output so the IC may be used either as an upconverter or for a direct conversion source. Additional details are covered in the Pin by Pin Description which shows the equivalent internal circuit and external circuit requirements.

Current Regulation/Enable

The device features temperature compensating, voltage independent current regulators which are controlled by the enable function in which ”high” powers up the IC.

Mixer: General

The mixer is a double–balanced four quadrant multiplier biased class AB allowing for programmable linearity control via an external current source. An input third order intercept point of 20 dBm has been achieved. The mixer has a 50 Ω single–ended RF input and open collector differential outputs. An onboard Local Oscillator transistor has the emitter, base and collector pinned out to implement a low phase noise VCO in various configurations. Additionally, a buffered prescaler output is provided for operation with a low frequency synthesizer. For direct conversion applications the input of the mixer may be terminated to ground through a 120 to 330 Ω resistor.

Local Oscillator/Voltage Control Oscillator

The on–chip transistor operates with coaxial transmission line or LC resonant elements to over 1.8 GHz. Biasing is done with a temperature/voltage compensated current source in the emitter. A RFC from V_{CC} to the base is recommended.

The transistor can be operated in the classic Colpitts, Clapp, or Hartley configuration. The application circuit (Figure 8) depicts a parallel resonant VCO which can cover the entire 902 to 928 MHz frequency band with phase noise of approximately –80 dBc/Hz at a 10 kHz offset (see Figure 2). For this configuration, the LO will be driven with approximately 100 mVrms, and the frequency of oscillation can be approximated by:

$$F_{osc} = \frac{1}{\left(2\pi\sqrt{\left(\frac{C1\ C2}{C1+C2}\right)\left(\frac{C3\ Cv}{C3+Cv} + 3.6\ pF\right)(L1 + 1.8\ nH)}\right)}$$

where Cv is the equivalent capacitance of the varactor at the control voltage.

For higher frequency operation, a series tuned oscillator configuration is recommended. Table 1 contains the S–parameters for the VCO transistor in a common collector configuration. This information is useful for designing a VCO at other operating frequencies or for various other oscillator topologies.

The output power (at Mix/Buf Out) can be varied by adjusting the value of R5 as illustrated in Figures 3 and 4. Figure 5 shows the typical operating window for the prescaler.

Figure 2. Typical Tuning Performance

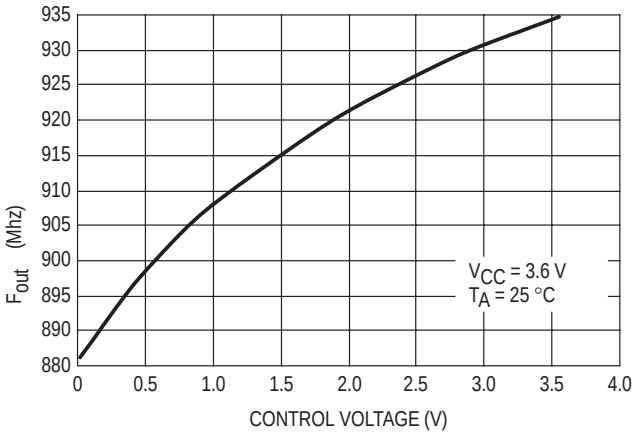


Figure 3. Mixer/Buffer Output versus 1st LO Input

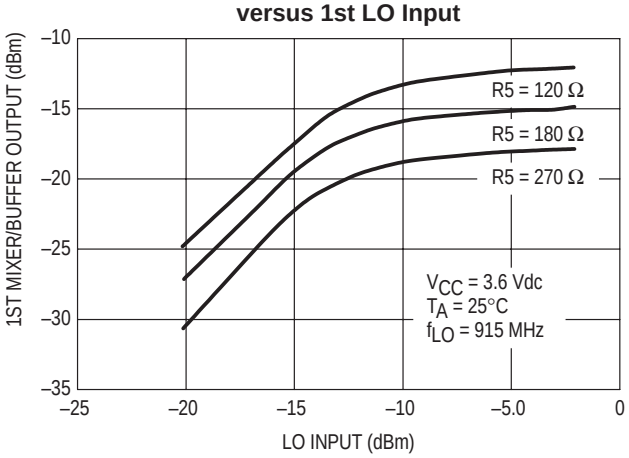


Figure 4. Test Circuit for Figure 3.

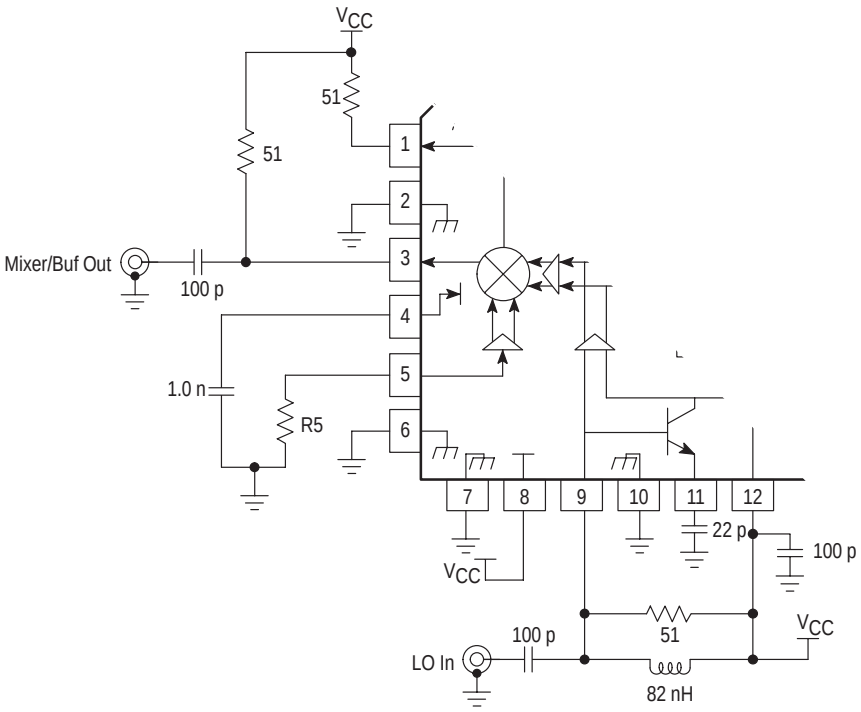
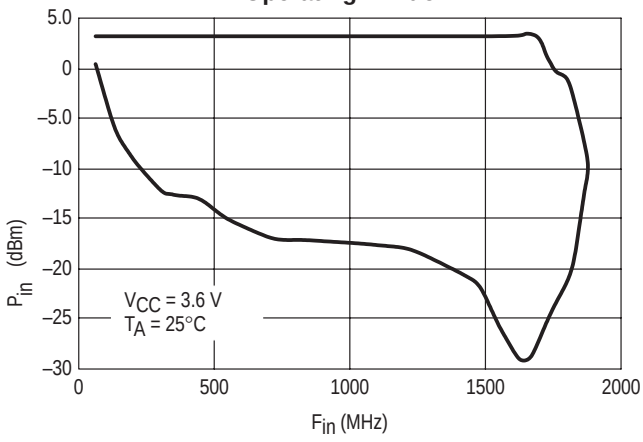


Figure 5. Typical Prescaler Operating Window



Mixer/Buffer Input

The Mixer/Buf In pin is a broadband, 50 Ω input used to drive the IF port of the mixer (see Table 2, S11 parameters).The Mixer/Buf In pin can be used in one of three modes:

2. A IF signal can be applied to this pin and up–converted to the desired RF frequency.
3. A resistor can be connected to ground, controlling the RF output power.
4. A resistor can be connected to V_{CC}, disabling the entire mixer.

The linear gain of the Mixer/Buf when used as a buffer is approximately –5.0 to –8.0 dB.

Mixer/Buffer Outputs

The mixer outputs (Mixer/Buf Out + and Mixer/Buf Out –) are balanced, open collector. A shunt resistor of 200 Ω minimum to V_{CC} is recommended for stability.

The outputs can be used as a single–ended driver or connected in a balanced–to–unbalanced configuration. If the single–ended driver configuration is used, the unused output must be tied directly to V_{CC}. For the balanced–to–unbalanced configuration, an additional 3.0 to 6.0 dB of power gain can be achieved. Conjugate matching is easily accomplished to the desired load by the addition of a shunt and series element (see Table 2, S22 parameters).

Low Power Amplifier (LPA)

The LPA is internally biased at low supply current (approximately 2.0 mA emitter current) for optimal low power operation, yielding a 10 dBm 1.0 dB output power compression point. Input and output matching may be achieved at various frequencies using few external components (see Table 3 S–parameters). Typical power gain is 16 dB with the input/output conjugately matched to the source/load impedance. A minimum 200 Ω shunt resistor from the output to V_{CC} is recommended for stability.

Figure 6. I_{CC} versus Temperature

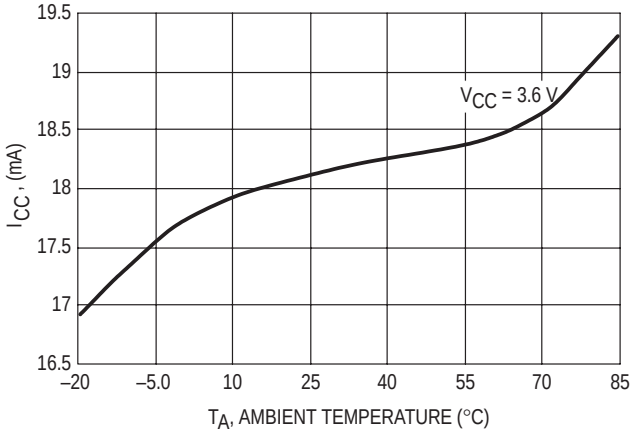


Figure 7. Output Power versus Temperature

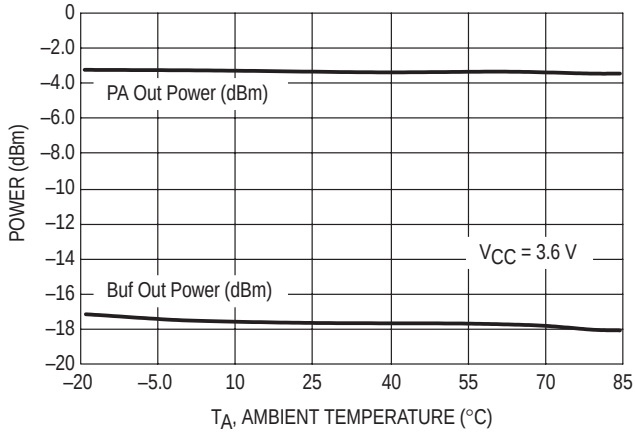
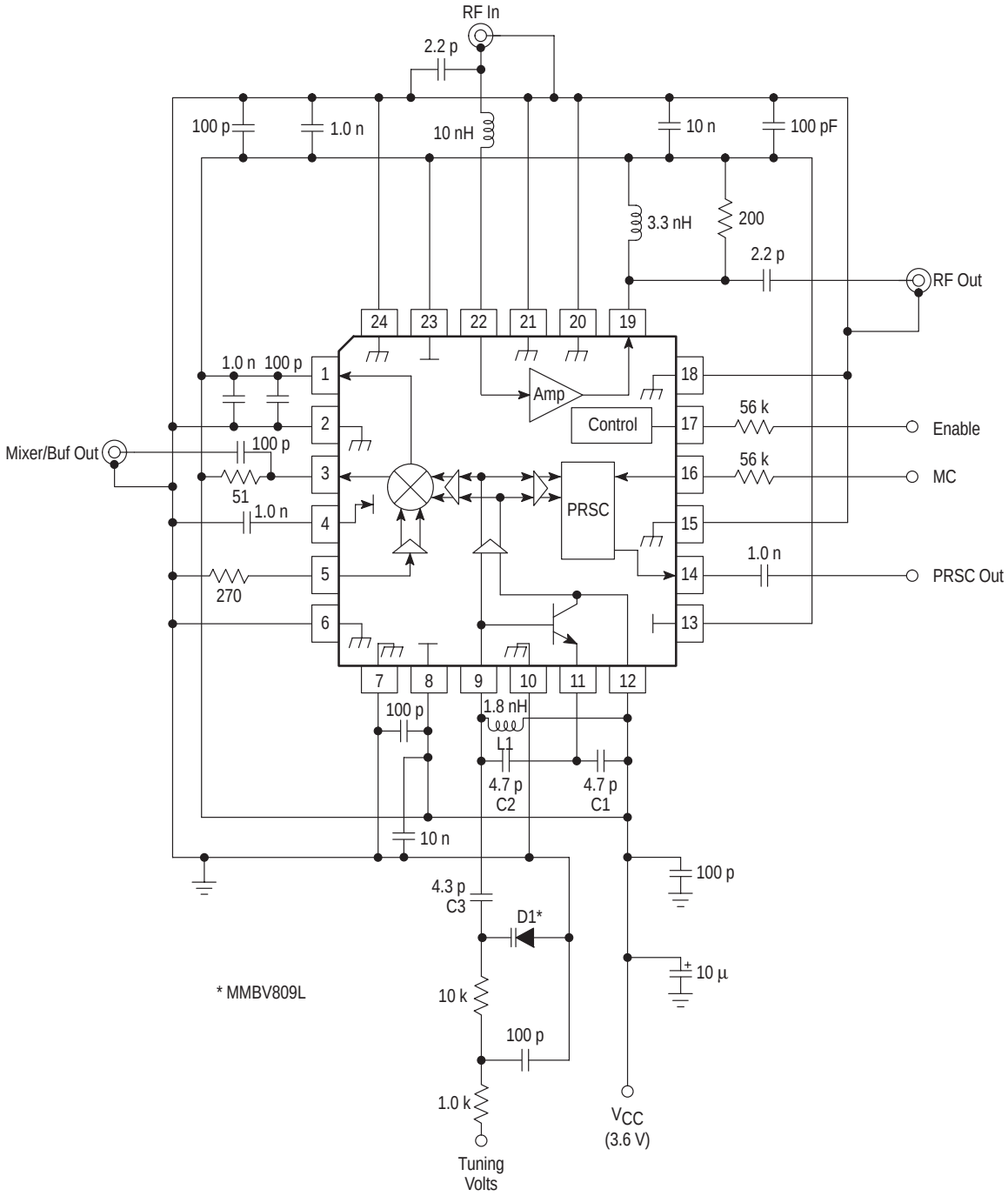


Figure 8. Applications Circuit



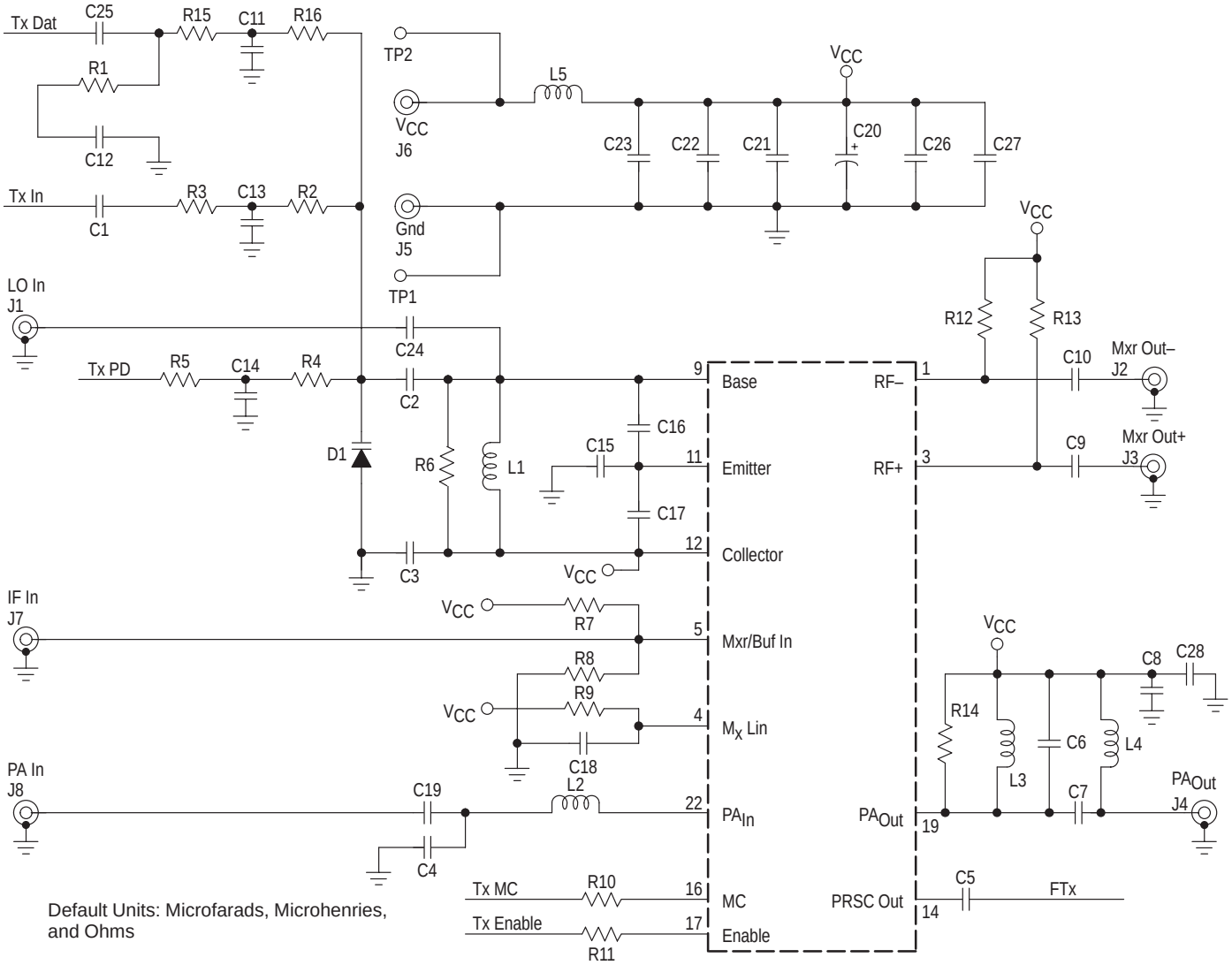
Evaluation PCB

The evaluation PCB is a versatile board which allows the MC13146 to be configured as a basic transmitter, or to characterize individual operating parameters.

The general purpose schematic and associated parts list for the PCB is given in Figure 9. This parts list build–up is identical to the Test Circuit illustrated in Figure 1, although parameters can very significantly due to differences in PCB parasitics. Figures 10, 11, and 12 show the actual PCB component, ground and solder sides, respectively.

Please refer to AN1687/D and AN1691/D for additional details and applications for the device.

Figure 9. Evaluation PCB Schematic



Default Units: Microfarads, Microhenries, and Ohms

R1,R2,R3,R15,R16, C1,C11,C12,C13,C25, R6,R7,R9,L4,J1,J2,J7, C6,C10,C15,C24	No component
R4	100 k
R5,R12,C19	Short
R8	270
R10	56 k
R11	68 k
R13	51
R14	200
C2	2.2 p
C3,C8,C9,C26,C27	100 p
C4, C7	2.2 p
C5,C18,C21,C22,C23	1.0 n
C14	1.0 µ
C16	1.5 p
C17	2.2 p
C20	10 µ
C28	10 n
L1	1.8 n
L2	8.2 n
L3	3.3 n
L5	RFC
D1	MMBV809LT1
J3,J4,J8	SMA EF Johnson 142–0701–851
J5,J6	Bananna Johnson Components 108–0902–001
JP1	Header, 5x2
U1	MC13146FTA

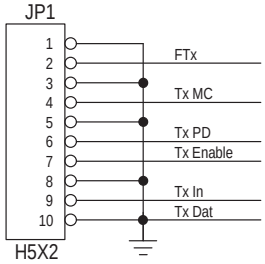


Figure 10. MC13146 Evaluation PCB Component Side

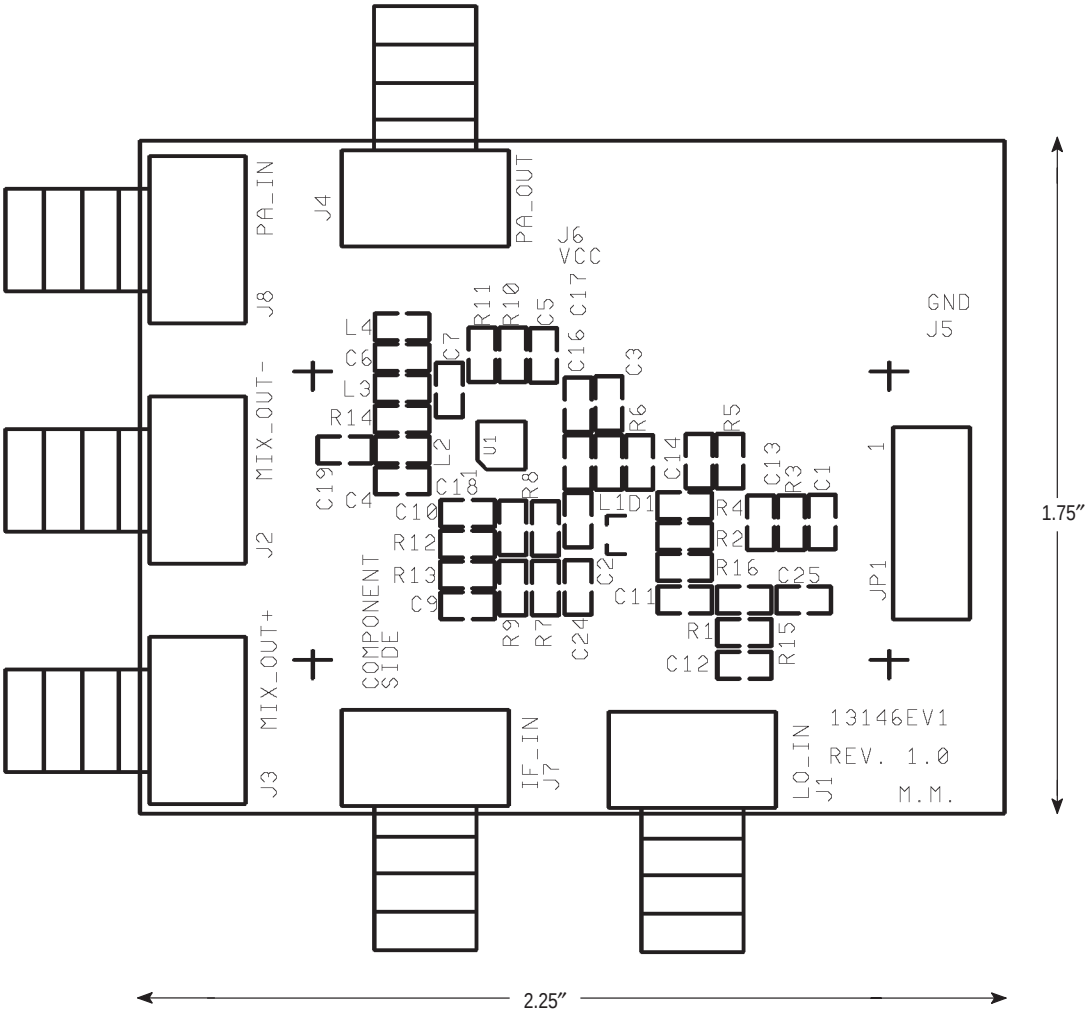


Figure 11. MC13146 Evaluation PCB Ground Plane

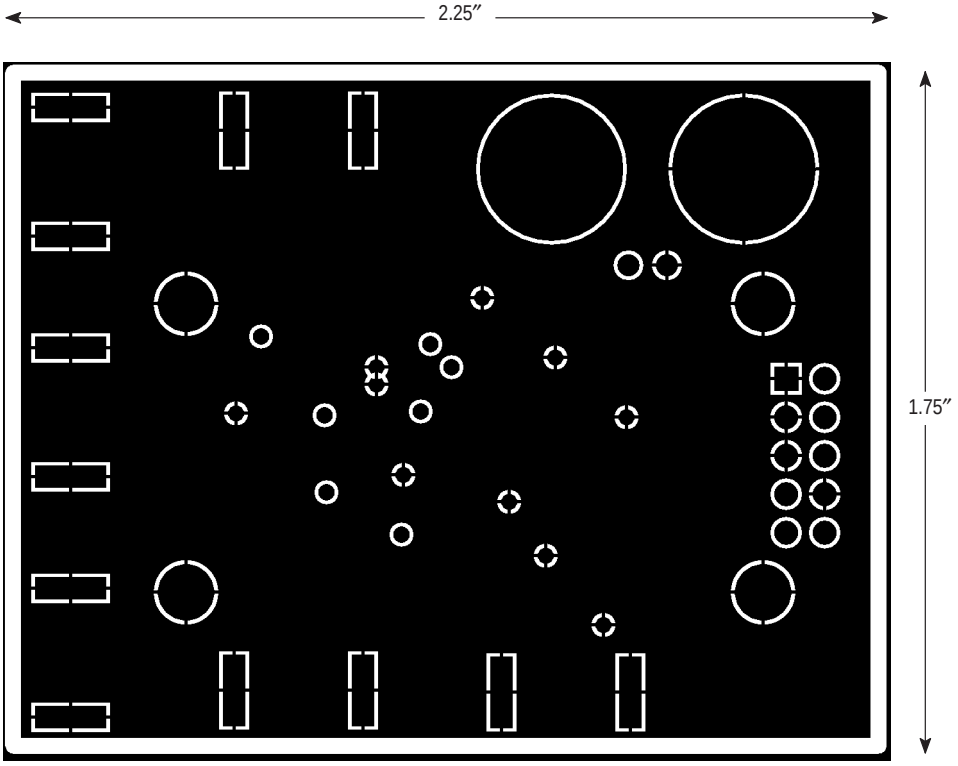


Figure 12. MC13146 Evaluation PCB Solder Side

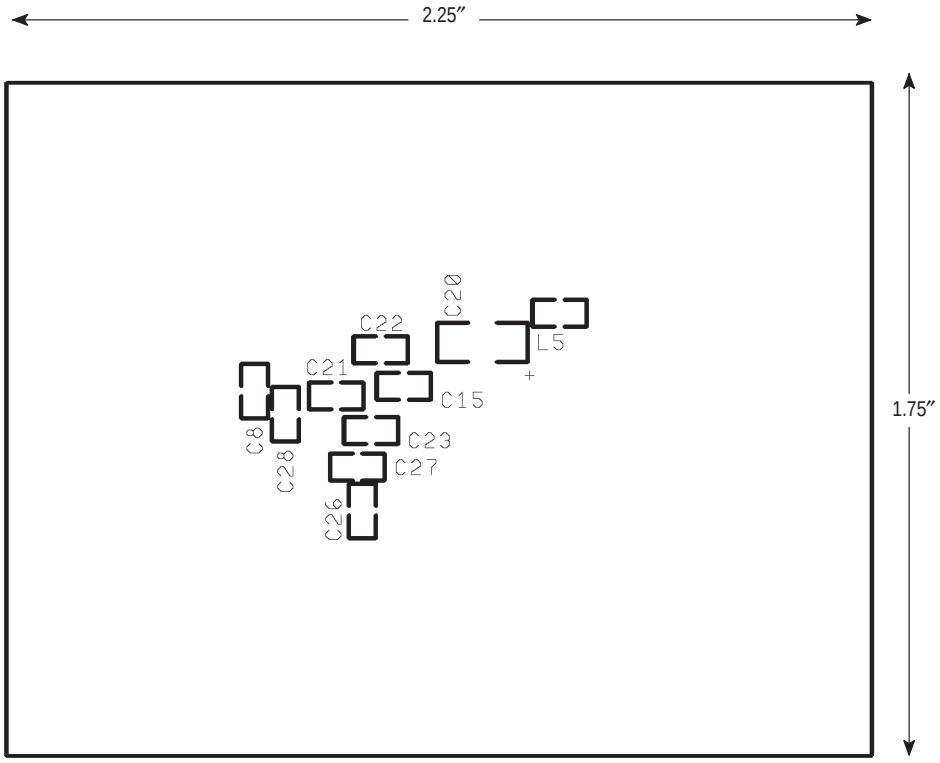


Table 1. VCO Transistor S–Parameters 3.6 Vdc; 50 Ω Load and Source Impedance; Common Collector

Freq (MHz)	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
25	0.99	–1	0.88	0	0.01	44	0.10	–7
50	0.99	–2	0.92	–1	0.02	61	0.09	–9
100	0.98	–5	0.95	–2	0.04	70	0.07	–37
150	0.98	–7	0.97	–3	0.06	73	0.07	–47
200	0.97	–10	1.04	–4	0.07	73	0.06	–86
300	0.95	–14	1.11	–8	0.10	71	0.09	–124
400	0.93	–19	1.23	–12	0.13	67	0.14	–149
450	0.92	–21	1.26	–14	0.15	66	0.15	–155
500	0.91	–23	1.30	–16	0.16	65	0.17	–159
600	0.86	–28	1.35	–20	0.19	61	0.20	–167
750	0.79	–37	1.46	–25	0.24	57	0.26	–172
800	0.79	–39	1.48	–26	0.25	56	0.28	–174
850	0.77	–42	1.48	–28	0.26	54	0.29	–177
900	0.74	–44	1.47	–31	0.28	52	0.28	–179
950	0.67	–49	1.53	–35	0.30	49	0.31	174
1000	0.61	–55	1.59	–38	0.33	47	0.34	171
1250	0.45	–81	1.61	–50	0.41	38	0.38	157
1500	0.35	–159	1.68	–67	0.53	16	0.38	134
1750	0.85	107	1.60	–100	0.57	–15	0.33	97
2000	1.02	76	1.17	–117	0.47	–32	0.18	86
2250	1.25	76	1.13	–125	0.55	–38	0.19	89
2500	1.58	53	0.84	–150	0.56	–64	0.09	57

Table 2. Mixer Input/Output S–Parameters: 200 Ω Pull–Up Resistor

Freq (MHz)	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
50	0.11	176.8	0.43	–4.2	0.001	38.7	0.60	–1.9
100	0.11	177.9	0.43	–7.5	0.002	19.8	0.60	–3.5
200	0.11	179.4	0.42	–13.7	0.001	28.3	0.60	–6.7
300	0.10	179.5	0.42	–20.7	0.001	69.8	0.61	–9.9
400	0.10	177.2	0.42	–27.3	0.001	106.3	0.61	–13.2
450	0.11	174.9	0.41	–31.1	0.001	135.2	0.62	–14.8
500	0.10	177.7	0.42	–34.1	0.002	138.2	0.62	–16.6
600	0.09	174.3	0.42	–41.8	0.003	150.5	0.63	–20.0
700	0.09	167.2	0.41	–49.3	0.005	158.7	0.64	–23.5
750	0.08	162.8	0.41	–53.9	0.006	166.0	0.65	–25.2
800	0.08	156.6	0.40	–58.4	0.008	166.5	0.65	–26.9
850	0.06	152.3	0.40	–62.7	0.009	171.2	0.66	–28.7
900	0.05	145.2	0.39	–66.4	0.012	177.6	0.66	–30.3
950	0.04	131.1	0.38	–71.6	0.015	–179.7	0.67	–31.9
1000	0.02	101.1	0.38	–76.7	0.019	178.0	0.68	–33.7
1250	0.08	–41.5	0.27	–96.8	0.042	137.1	0.73	–43.2
1500	0.40	–87.6	0.24	–90.2	0.036	129.9	0.78	–53.3
1750	0.50	–144.1	0.30	–114.0	0.058	142.8	0.86	–63.8
2000	0.51	–173.5	0.22	–133.0	0.174	151.6	0.96	–81.3

Table 3. LPA S–Parameters: 200 Ω Pull–Up Resistor

Freq (MHz)	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
200	0.76	–26.0	9.3	148.1	0.0006	73.3	0.60	–12.4
300	0.71	–37.5	8.5	135.2	0.0011	74.4	0.60	–18.5
400	0.67	–47.2	7.6	124.5	0.0011	79.6	0.61	–24.6
450	0.64	–51.7	7.2	118.6	0.0010	66.0	0.62	–28.3
500	0.62	–55.4	6.9	114.2	0.0011	45.4	0.62	–31.6
600	0.58	–63.7	6.3	105.3	0.0012	16.7	0.64	–38.8
700	0.54	–72.1	5.6	95.2	0.0016	–20.9	0.66	–45.6
750	0.52	–74.6	5.4	91.8	0.0013	–36.9	0.66	–48.5
800	0.51	–77.9	5.2	87.7	0.0023	–50.8	0.67	–52.6
850	0.49	–80.3	5.0	83.8	0.0033	–63.6	0.68	–56.1
900	0.49	–83.5	4.7	79.6	0.0044	–78.7	0.68	–60.3
950	0.48	–85.4	4.5	77.2	0.0060	–90.3	0.68	–63.2
1000	0.48	–88.8	4.3	74.7	0.0082	–97.6	0.68	–65.8
1250	0.51	–102.7	3.7	58.8	0.0249	–136.6	0.73	–74.6
1500	0.48	–119.7	3.3	37.6	0.0273	172.0	0.90	–87.7
1750	0.47	–130.0	2.7	20.5	0.0290	166.5	0.97	–103.7
2000	0.51	–136.7	2.2	–1.1	0.0386	164.1	1.01	–119.1

MOTOROLA

MC13150

Narrowband FM Coilless Detector IF Subsystem

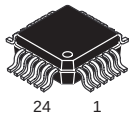
NARROWBAND FM COILLESS DETECTOR IF SUBSYSTEM FOR CELLULAR AND ANALOG APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA

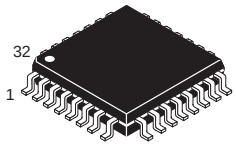
The MC13150 is a narrowband FM IF subsystem targeted at cellular and other analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13150 has an onboard Colpitts VCO for Crystal controlled second LO in dual conversion receivers. The mixer is a double balanced configuration with excellent third order intercept. It is useful to beyond 200 MHz. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. The quadrature detector is a unique design eliminating the conventional tunable quadrature coil.

Applications for the MC13150 include cellular, CT–1 900 MHz cordless telephone, data links and other radio systems utilizing narrowband FM modulation.

- Linear Coilless Detector
- Adjustable Demodulator Bandwidth
- 2.5 to 6.0 Vdc Operation
- Low Drain Current: < 2.0 mA
- Typical Sensitivity of 2.0 μV for 12 dB SINAD
- IIP3, Input Third Order Intercept Point of 0 dBm
- RSSI Range of Greater Than 100 dB
- Internal 1.4 kΩ Terminations for 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range



FTA SUFFIX
PLASTIC PACKAGE
CASE 977
(LQFP–24)



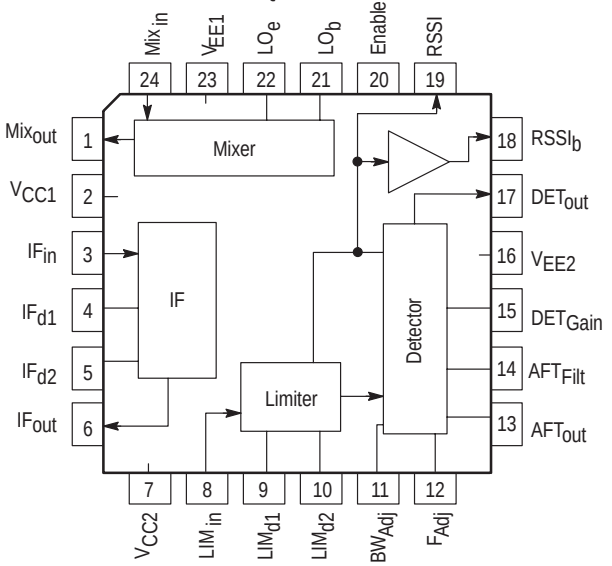
FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(LQFP–32)

ORDERING INFORMATION

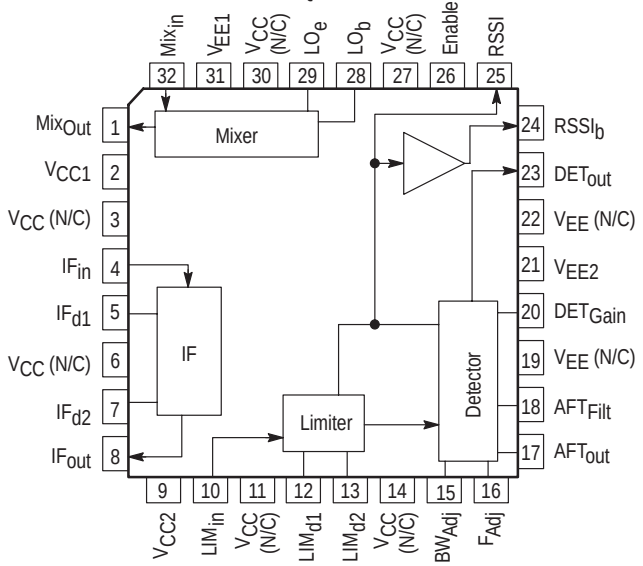
Device	Operating Temperature Range	Package
MC13150FTA	T_A = –40 ° to +85°C	LQFP–24
MC13150FTB		LQFP–32

PIN CONNECTIONS

LQFP–24



LQFP–32



MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	2, 9	V_{CC}(max)	6.5	Vdc
Junction Temperature	–	T_{Jmax}	+150	°C
Storage Temperature Range	–	T_{stg}	–65 to +150	°C

NOTE: 1. Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage T_A = 25°C –40°C ≤ T_A ≤ 85°C (See Figure 22)	2, 9 21, 31	V_{CC} V_{EE}	2.5 to 6.0 0	Vdc
Input Frequency	32	f_{in}	10 to 500	MHz
Ambient Temperature Range	–	T_A	–40 to +85	°C
Input Signal Level	32	V_{in}	0	dBm

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC1} = V_{CC2} = 3.0 Vdc, No Input Signal.)

Characteristics	Condition	Pin	Symbol	Min	Typ	Max	Unit
Total Drain Current (See Figure 2)	V_S = 3.0 Vdc	2 + 9	I_{TOTAL}	–	1.7	3.0	mA
Supply Current, Power Down (See Figure 3)	–	2 + 9	–	–	40	–	nA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = 3.0 Vdc, f_{RF} = 50 MHz, f_{LO} = 50.455 MHz, LO Level = –10 dBm, see Figure 1 Test Circuit*, unless otherwise specified.)

Characteristics	Condition	Pin	Symbol	Min	Typ	Max	Unit
12 dB SINAD Sensitivity (See Figure 15)	f_{mod} = 1.0 kHz; f_{dev} = ±5.0 kHz	32	–	–	–100	–	dBm
RSSI Dynamic Range (See Figure 7)	–	25	–	–	100	–	dB
Input 1.0 dB Compression Point Input 3rd Order Intercept Point (See Figure 18)	– –	– –	1.0 dB C. Pt. IIP3	– –	–11 –1.0	– –	dBm
Coilless Detector Bandwidth Adjust (See Figure 11)	Measured with No IF Filters	–	ΔBW adj	–	26	–	kHz/μA
MIXER							
Conversion Voltage Gain (See Figure 5)	P_{in} = –30 dBm; PLO = –10 dBm	32	–	–	10	–	dB
Mixer Input Impedance	Single–Ended	32	–	–	200	–	Ω
Mixer Output Impedance	–	1	–	–	1.5	–	kΩ
LOCAL OSCILLATOR							
LO Emitter Current (See Figure 26)	–	29	–	30	63	100	μA
IF & LIMITING AMPLIFIERS SECTION							
IF and Limiter RSSI Slope	Figure 7	25	–	–	0.4	–	μA/dB
IF Gain	Figure 8	4, 8	–	–	42	–	dB
IF Input & Output Impedance	–	4, 8	–	–	1.5	–	kΩ
Limiter Input Impedance	–	10	–	–	1.5	–	kΩ
Limiter Gain	–	–	–	–	96	–	dB

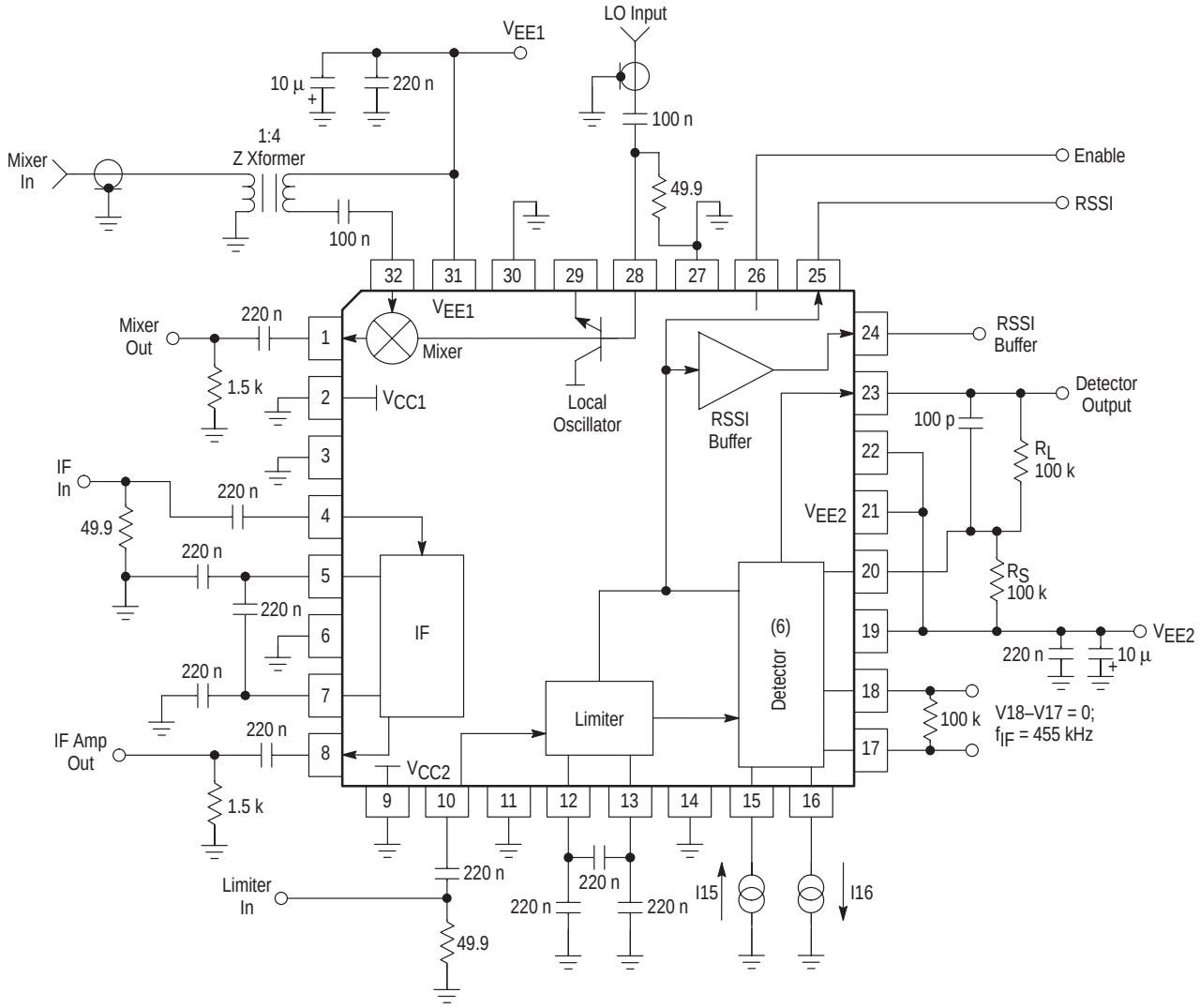
* Figure 1 Test Circuit uses positive (V_{CC}) Ground.

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_S = 3.0 Vdc, f_{RF} = 50 MHz, f_{LO} = 50.455 MHz, LO Level = –10 dBm, see Figure 1 Test Circuit*, unless otherwise specified.)

Characteristics	Condition	Pin	Symbol	Min	Typ	Max	Unit
DETECTOR							
Frequency Adjust Current	Figure 9, f_{IF} = 455 kHz	16	–	41	49	56	μA
Frequency Adjust Voltage	Figure 10, f_{IF} = 455 kHz	16	–	600	650	700	mVdc
Bandwidth Adjust Voltage	Figure 12, I_{15} = 1.0 μA	15	–	–	570	–	mVdc
Detector DC Output Voltage (See Figure 25)	–	23	–	–	1.36	–	Vdc
Recovered Audio Voltage	f_{dev} = ±3.0 kHz	23	–	85	122	175	mVrms

* Figure 1 Test Circuit uses positive (V_{CC}) Ground.

Figure 1. Test Circuit



This device contains 292 active transistors.

MC13150 CIRCUIT DESCRIPTION

General

The MC13150 is a very low power single conversion narrowband FM receiver incorporating a split IF. This device is designated for use as the backend in analog narrowband FM systems such as cellular, 900 MHz cordless phones and narrowband data links with data rates up to 9.6 k baud. It contains a mixer, oscillator, extended range received signal strength indicator (RSSI), RSSI buffer, IF amplifier, limiting IF, a unique coilless quadrature detector and a device enable function (see Package Pin Outs/Block Diagram).

Low Current Operation

The MC13150 is designed for battery and portable applications. Supply current is typically 1.7 mAdc at 3.0 Vdc. Figure 2 shows the supply current versus supply voltage.

Enable

The enable function is provided for battery powered operation. The enabled pin is pulled down to enable the regulators. Figure 3 shows the supply current versus enable voltage, V_{enable} (relative to V_{CC}) needed to enable the device. Note that the device is fully enabled at V_{CC} – 1.3 Vdc. Figure 4 shows the relationship of enable current, I_{enable} to enable voltage, V_{enable}.

Mixer

The mixer is a double–balanced four quadrant multiplier and is designed to work up to 500 MHz. It has a single ended input. Figure 5 shows the mixer gain and saturated output response as a function of input signal drive and for –10 dBm LO drive level. This is measured in the application circuit shown in Figure 15 in which a single LC matching network is used. Since the single–ended input impedance of the mixer is 200 Ω, an alternate solution uses a 1:4 impedance transformer to match the mixer to 50 Ω input impedance. The linear voltage gain of the mixer alone is approximately 4.0 dB (plus an additional 6.0 dB for the transformer). Figure 6 shows the mixer gain versus the LO input level for various mixer input levels at 50 MHz RF input.

The buffered output of the mixer is internally loaded, resulting in an output impedance of 1.5 kΩ.

Local Oscillator

The on–chip transistor operates with crystal and LC resonant elements up to 220 MHz. Series resonant, overtone crystals are used to achieve excellent local oscillator stability. 3rd overtone crystals are used through about 65 to 70 MHz. Operation from 70 MHz up to 200 MHz is feasible using the on–chip transistor with a 5th or 7th overtone crystal. To enhance operation using an overtone crystal, the internal transistor's bias is increased by adding an external resistor from Pin 29 (in 32 pin QFP package) to V_{EE} to keep the oscillator on continuously or it may be taken to the enable pin to shut it off when the receiver is disabled. –10 dBm of local oscillator drive is needed to adequately drive the mixer (Figure 6). The oscillator configurations specified above are described in the application section.

RSSI

The received signal strength indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the IF and limiting amplifier stages. An external resistor at Pin 25 (in 32 pin QFP package) sets the voltage range or swing of the RSSI output voltage. Linearity of the RSSI is optimized by using external ceramic bandpass filters which have an insertion loss of 4.0 dB. The RSSI circuit is designed to provide 100+ dB of dynamic range with temperature compensation (see Figures 7 and 23 which show the RSSI response of the applications circuit).

RSSI Buffer

The RSSI buffer has limitations in what loads it can drive. It can pull loads well towards the positive and negative supplies, but has problems pulling the load away from the supplies. The load should be biased at half supply to overcome this limitation.

Figure 2. Supply Current versus Supply Voltage

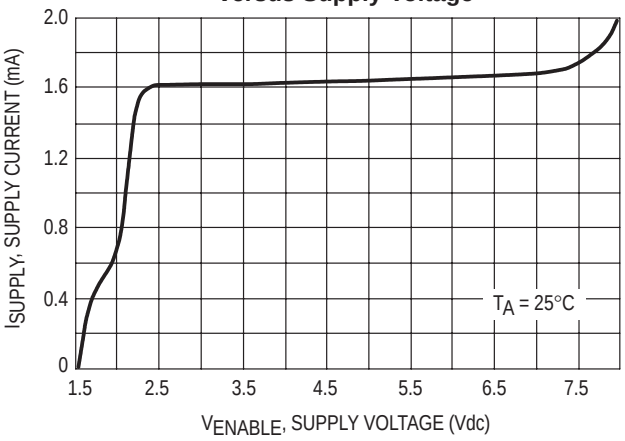


Figure 3. Supply Current versus Enable Voltage

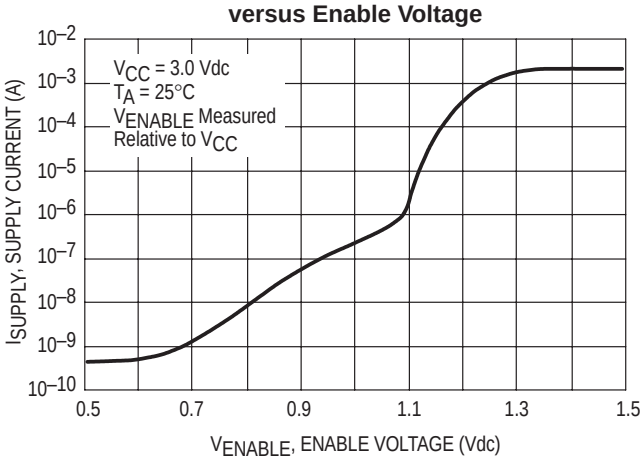


Figure 4. Enable Current versus Enable Voltage

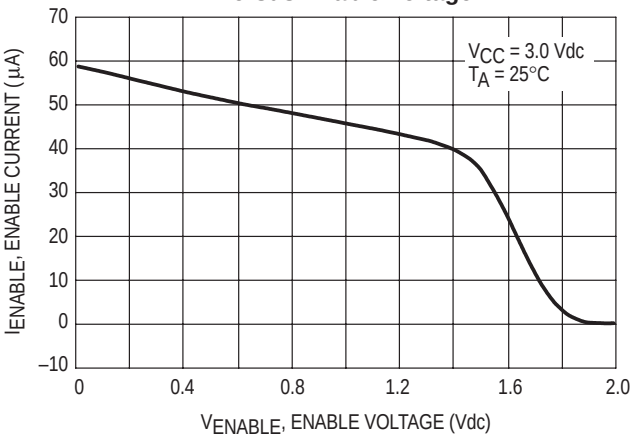


Figure 5. Mixer IF Output Level versus RF Input Level

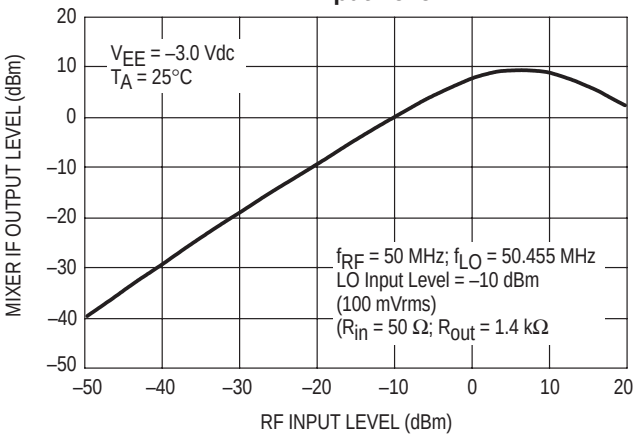


Figure 6. Mixer IF Output Level versus Local Oscillator Input Level

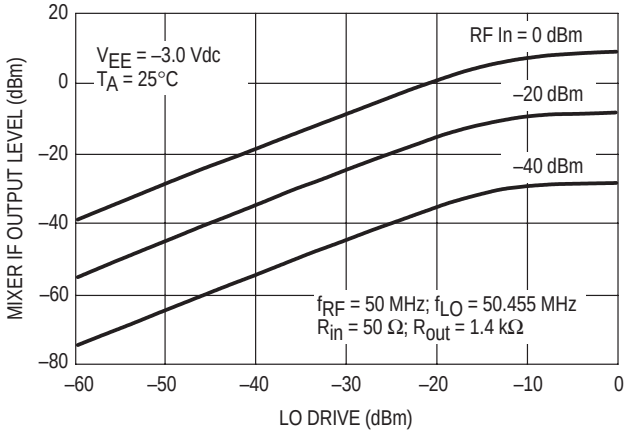
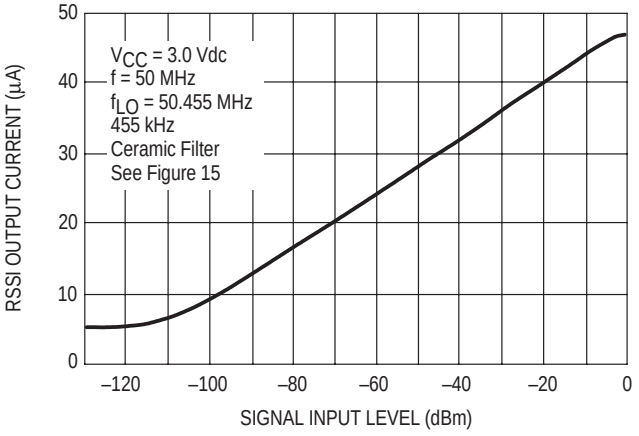


Figure 7. RSSI Output Current versus Input Signal Level



IF Amplifier

The first IF amplifier section is composed of three differential stages. This section has internal dc feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 42 dB at 455 kHz. Figure 8 shows the gain of the IF amplifier as a function of the IF frequency.

The fixed internal input impedance is 1.5 kΩ; it is designed for applications where a 455 kHz ceramic filter is used and no external output matching is necessary since the filter requires a 1.5 kΩ source and load impedance.

Overall RSSI linearity is dependent on having total midband attenuation of 10 dB (4.0 dB insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the IF amplifier is buffered and the impedance is 1.5 kΩ.

Limiter

The limiter section is similar to the IF amplifier section except that six stages are used. The fixed internal input impedance is 1.5 kΩ. The total gain of the limiting amplifier section is approximately 96 dB. This IF limiting amplifier section internally drives the quadrature detector section.

Figure 8. IF Amplifier Gain versus IF Frequency

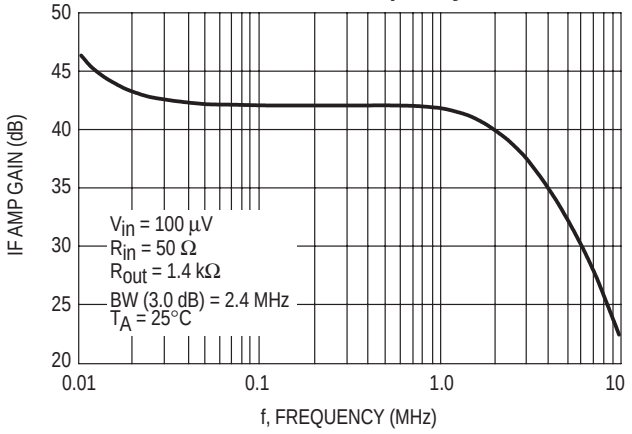


Figure 9. F_{adj} Current versus IF Frequency

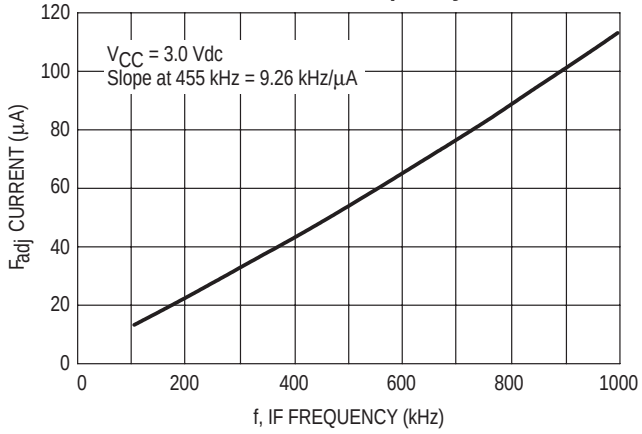


Figure 10. F_{adj} Voltage versus F_{adj} Current

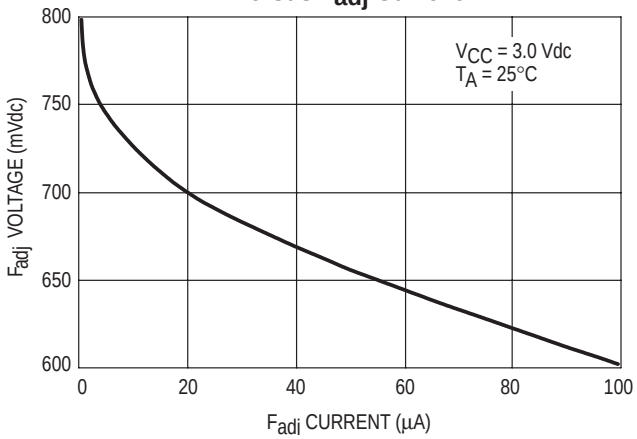
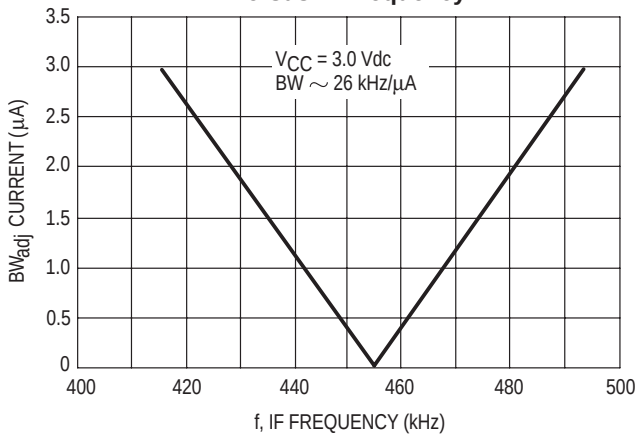


Figure 11. BW_{adj} Current versus IF Frequency



Coilless Detector

The quadrature detector is similar to a PLL. There is an internal oscillator running at the IF frequency and two detector outputs. One is used to deliver the audio signal and the other one is filtered and used to tune the oscillator.

The oscillator frequency is set by an external resistor at the F_{adj} pin. Figure 9 shows the control current required for a particular frequency; Figure 10 shows the pin voltage at that current. From this the value of R_F is chosen. For example, 455 kHz would require a current of around 50 μA. The pin voltage (Pin 16 in the 32 pin QFP package) is around 655mV giving a resistor of 13.1 kΩ. Choosing 12 kΩ as the nearest standard value gives a current of approximately 55 μA. The 5.0 μA difference can be taken up by the tuning resistor, R_T.

The best nominal frequency for the AFT_{out} pin (Pin 17) would be half supply. A supply voltage of 3.0 Vdc suggests a resistor value of (1.5 – 0.655)V/5.0 μA = 169 kΩ. Choosing 150 kΩ would give a tuning current of 3/150 k = 20 μA. From Figure 9 this would give a tuning range of roughly 10 kHz/μA or ± 100 kHz which should be adequate.

The bandwidth can be adjusted with the help of Figure 11. For example, 1.0 μA would give a bandwidth of ± 13 kHz. The voltage across the bandwidth resistor, R_B from Figure 12 is V_{CC} – 2.44 Vdc = 0.56 Vdc for V_{CC} = 3.0 Vdc, so R_B = 0.56V/1.0 μA = 560 kΩ. Actually the locking range will be ±13 kHz while the audio bandwidth will be approximately ±8.4 kHz due to an internal filter capacitor. This is verified in Figure 13. For some applications it may be desirable that the audio bandwidth is increased; this is done by reducing R_B. Reducing R_B widens the detector bandwidth and improves the distortion at high input levels at the expense of 12 dB SINAD sensitivity. The low frequency 3.0dB point is set by the tuning circuit such that the product

$$R_T C_T = 0.68/f3dB.$$

So, for example, 150 k and 1.0 μF give a 3.0 dB point of 4.5 Hz. The recovered audio is set by R_L to give roughly 50mV per kHz deviation per 100 k of resistance. The dc level can be shifted by R_S from the nominal 0.68 V by the following equation:

$$\text{Detector DC Output} = ((R_L + R_S)/R_S)\ 0.68\ \text{Vdc}$$

Thus, $R_S = R_L$ sets the output at 2 x 0.68 = 1.36 V; $R_L = 2R_S$ sets the output at 3 x 0.68 = 2.0 V.

Figure 12. BW_{adj} Current versus BW_{adj} Voltage

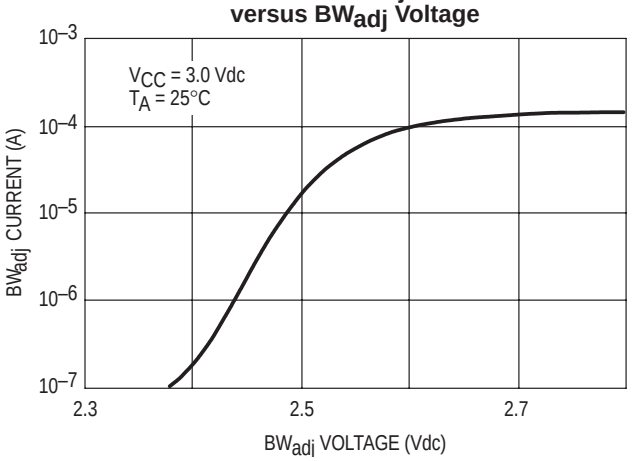
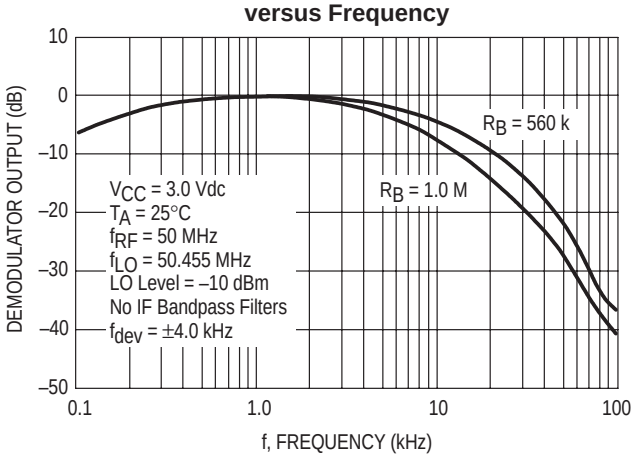


Figure 13. Demodulator Output versus Frequency



APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side (see Figures 29 and 30). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. There is an area dedicated for a LNA preamp. This evaluation board will be discussed and referenced in this section.

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. The applications circuit schematic (Figure 15) specifies particular components that were used to achieve the results shown in the typical curves but equivalent components should give similar results. Component placement views are shown in Figures 27 and 28 for the application circuit in Figure 15 and for the 83.616 MHz crystal oscillator circuit in Figure 16.

Input Matching Components

The input matching circuit shown in the application circuit schematic (Figure 15) is a series L, shunt C single L section which is used to match the mixer input to 50 Ω. An alternative input network may use 1:4 surface mount transformers or BALUNs. The 12 dB SINAD sensitivity using the 1:4 impedance transformer is typically –100 dBm for f_{mod} = 1.0 kHz and f_{dev} = ±5.0 kHz at f_{in} = 50 MHz and f_{LO} = 50.455 MHz (see Figure 14).

It is desirable to use a SAW filter before the mixer to provide additional selectivity and adjacent channel rejection and improved sensitivity. SAW filters sourced from Toko (Part # SWS083GBWA) and Murata (Part # SAF83.16MA51X) are excellent choices to easily interface with the MC13150 mixer. They are packaged in a 12 pin low profile surface mount ceramic package. The center frequency is 83.161 MHz and the 3.0 dB bandwidth is 30 kHz.

Figure 14. S+N+D, N+D, N, 30% AMR versus Input Signal Level

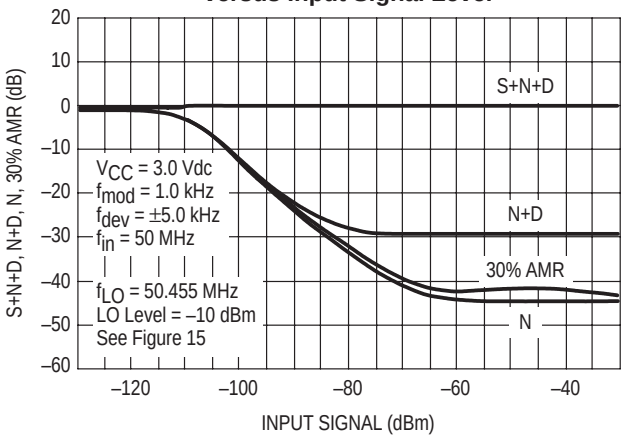
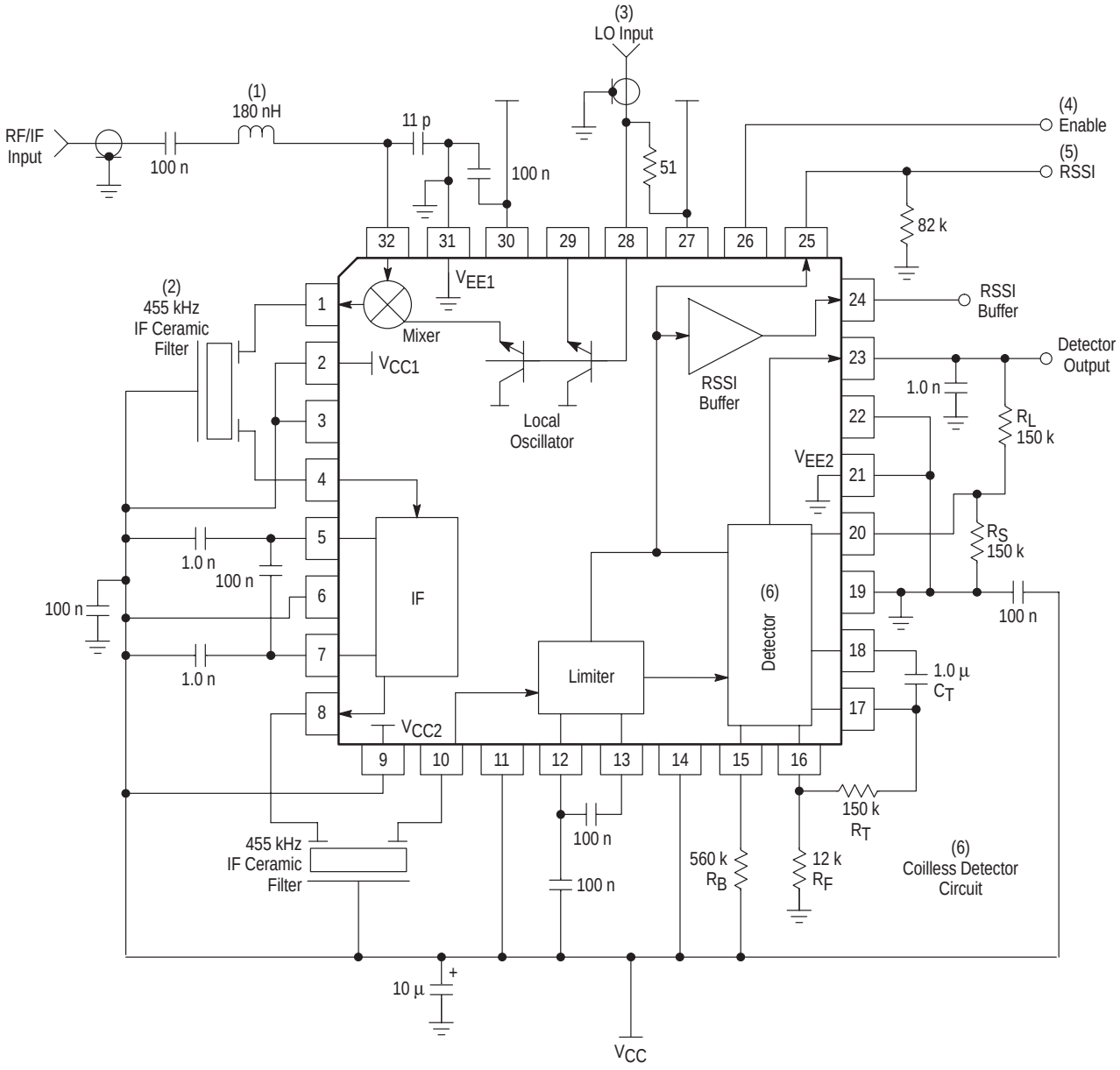


Figure 15. Application Circuit



NOTES: 1. Alternate solution is 1:4 impedance transformer (sources include Mini Circuits, Coilcraft and Toko).
2. 455 kHz ceramic filters (source Murata CFU455 series which are selected for various bandwidths).
3. For external LO source, a 51 Ω pull–up resistor is used to bias the base of the on–board transistor as shown in Figure 15. Designer may provide local oscillator with 3rd, 5th, or 7th overtone crystal oscillator circuit. The PC board is laid out to accommodate external components needed for a Butler emitter coupled crystal oscillator (see Figure 16).
4. Enable IC by switching the pin to V_{EE}.
5. The resistor is chosen to set the range of RSSI voltage output swing.
6. Details regarding the external components to setup the coilless detector are provided in the application section.

Local Oscillators

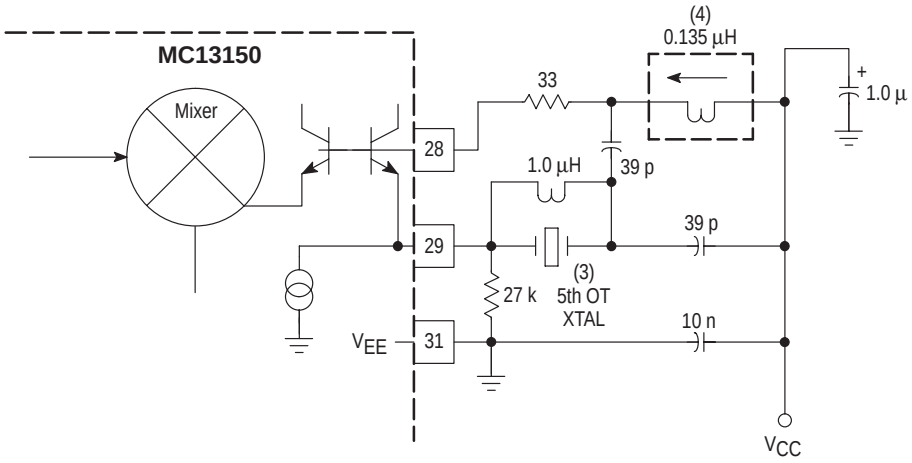
HF & VHF Applications

In the application schematic, an external sourced local oscillator is utilized in which the base is biased via a 51 Ω resistor to V_{CC}. However, the on–chip grounded collector transistor may be used for HF and VHF local oscillators with higher order overtone crystals. Figure 16 shows a 5th overtone oscillator at 83.616 MHz. The circuit uses a Butler overtone oscillator configuration. The amplifier is an emitter follower. The crystal is driven from the emitter and is coupled to the high impedance base through a capacitive tap network. Operation at the desired overtone frequency is ensured by the parallel resonant circuit formed by the variable inductor and the tap capacitors and parasitic capacitances of the on–chip transistor and PC board. The variable inductor specified in the schematic could be replaced with a high tolerance, high Q ceramic or air wound surface mount component if the other components have tight enough tolerances. A variable inductor provides an adjustment for gain and frequency of the resonant tank ensuring lock up and start–up of the crystal oscillator. The overtone crystal is chosen with ESR of typically 80 Ω and 120 Ω maximum; if the resistive loss in the crystal is too high the performance of oscillator may be impacted by lower gain margins.

A series LC network to ac ground (which is V_{CC}) is comprised of the inductance of the base lead of the on–chip transistor and PC board traces and tap capacitors. Parasitic oscillations often occur in the 200 to 800 MHz range. A small resistor is placed in series with the base (Pin 28) to cancel the negative resistance associated with this undesired mode of oscillation. Since the base input impedance is so large, a small resistor in the range of 27 to 68 Ω has very little effect on the desired Butler mode of oscillation.

The crystal parallel capacitance, C_O, provides a feedback path that is low enough in reactance at frequencies of 5th overtones or higher to cause trouble. C_O has little effect near resonance because of the low impedance of the crystal motional arm (R_m–L_m–C_m). As the tunable inductor, which forms the resonant tank with the tap capacitors, is tuned off the crystal resonant frequency, it may be difficult to tell if the oscillation is under crystal control. Frequency jumps may occur as the inductor is tuned. In order to eliminate this behavior an inductor, L_O, is placed in parallel with the crystal. L_O is chosen to resonant with the crystal parallel capacitance, C_O, at the desired operation frequency. The inductor provides a feedback path at frequencies well below resonance; however, the parallel tank network of the tap capacitors and tunable inductor prevent oscillation at these frequencies.

Figure 16. MC13150FTB Overtone Oscillator
f_{RF} = 83.16 MHz; f_{LO} = 83.616 MHz
5th Overtone Crystal Oscillator



Receiver Design Considerations

The curves of signal levels at various portions of the application receiver with respect to RF input level are shown in Figure 17. This information helps determine the network topology and gain blocks required ahead of the MC13150 to achieve the desired sensitivity and dynamic range of the receiver system. The PCB is laid out to accommodate a low noise preamp followed by the 83.16 MHz SAW filter. In the application circuit (Figure 15), the input 1.0 dB compression point is –10 dBm and the input third order intercept (IP3) performance of the system is approximately 0 dBm (see Figure 18).

Typical Performance Over Temperature

Figures 19–26 show the device performance over temperature.

Figure 17. Signal Levels versus RF Input Signal Level

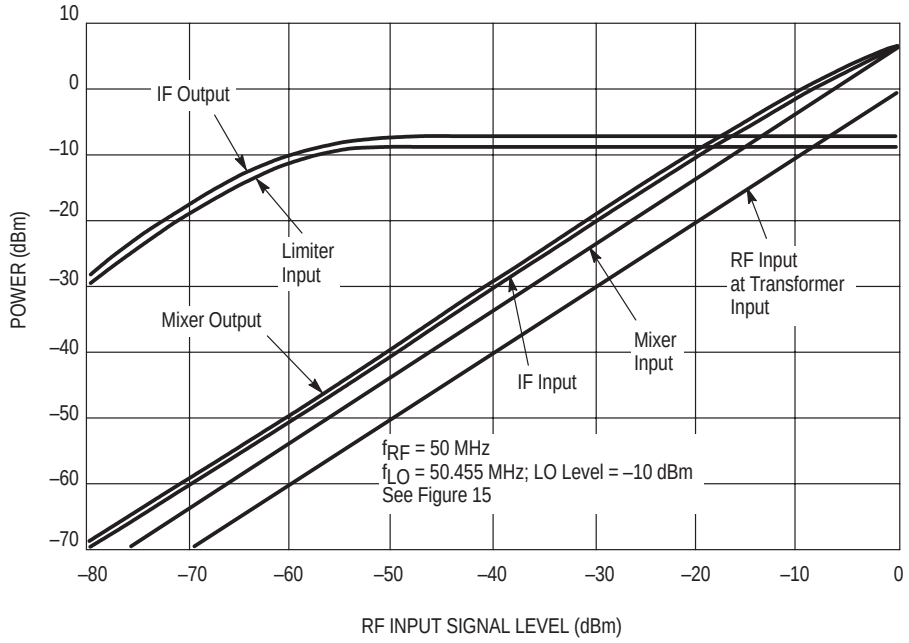
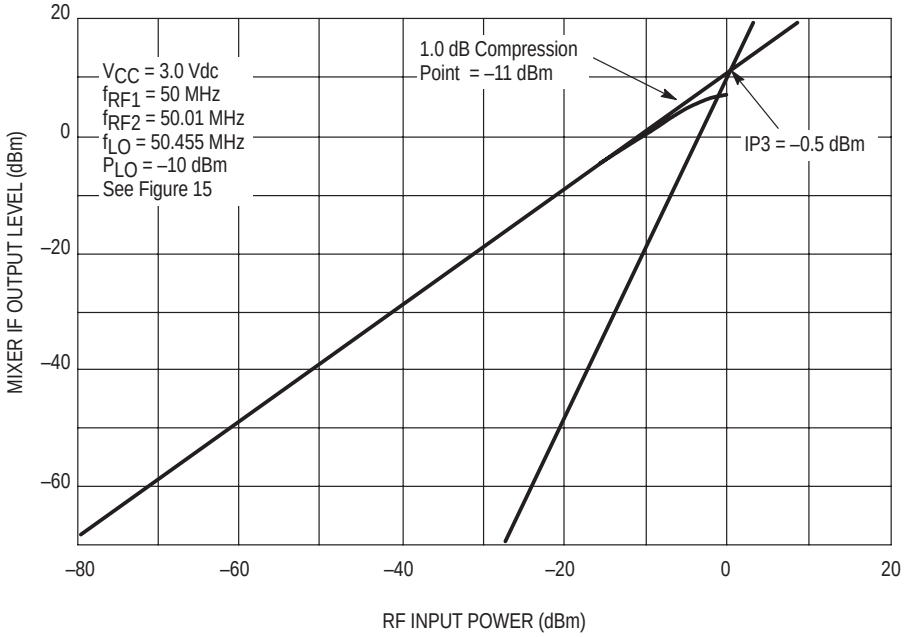


Figure 18. 1.0 dB Compression Point and Input Third Order Intercept Point versus Input Power



TYPICAL PERFORMANCE OVER TEMPERATURE

Figure 19. Supply Current, I_{VEE1} versus Signal Input Level

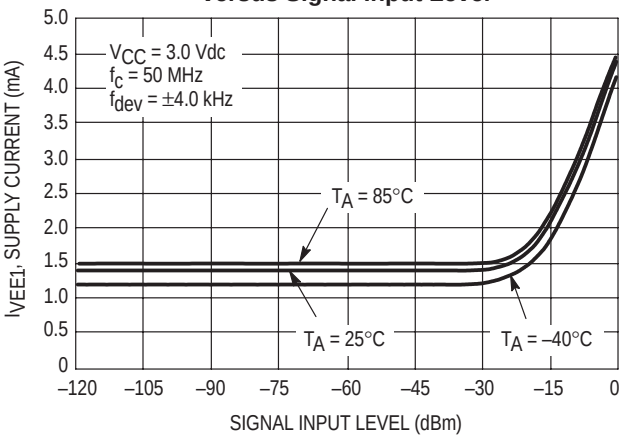
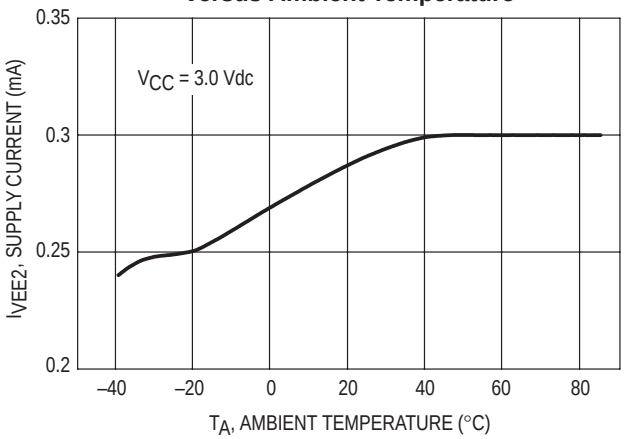


Figure 20. Supply Current, I_{VEE2} versus Ambient Temperature



TYPICAL PERFORMANCE OVER TEMPERATURE

Figure 21. Total Supply Current versus Ambient Temperature

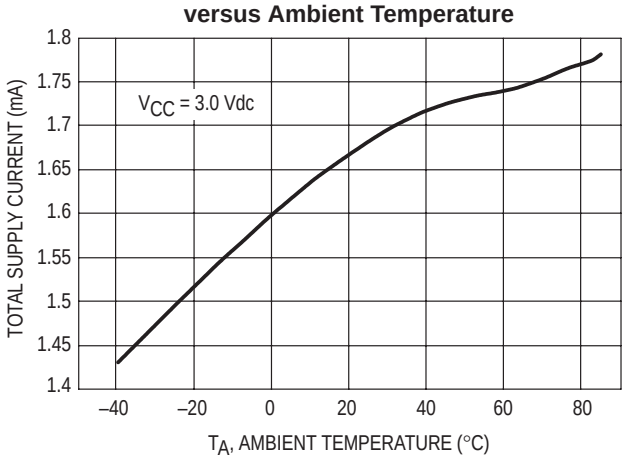


Figure 22. Minimum Supply Voltage versus Ambient Temperature

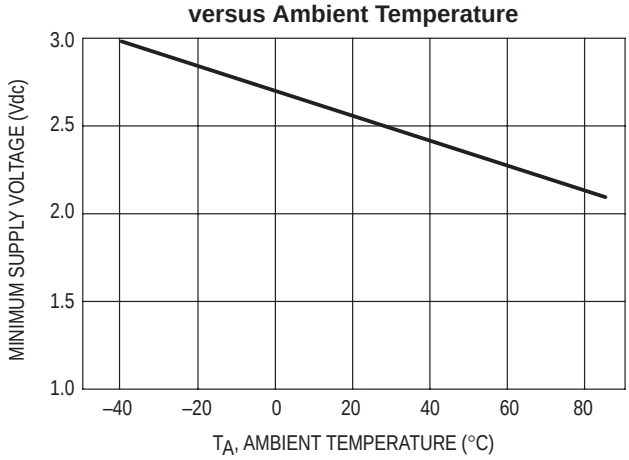


Figure 23. RSSI Current versus Ambient Temperature and Signal Level

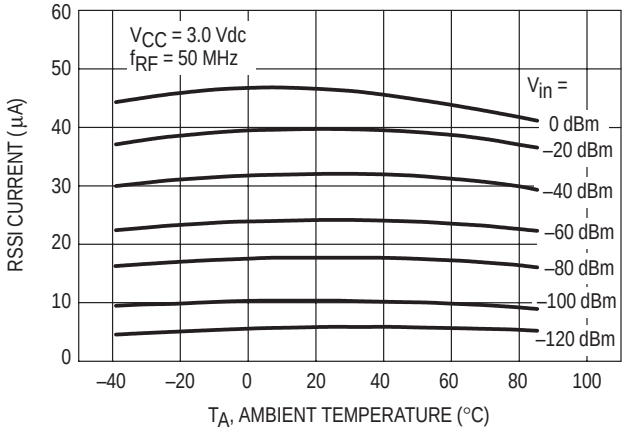


Figure 24. Recovered Audio versus Ambient Temperature

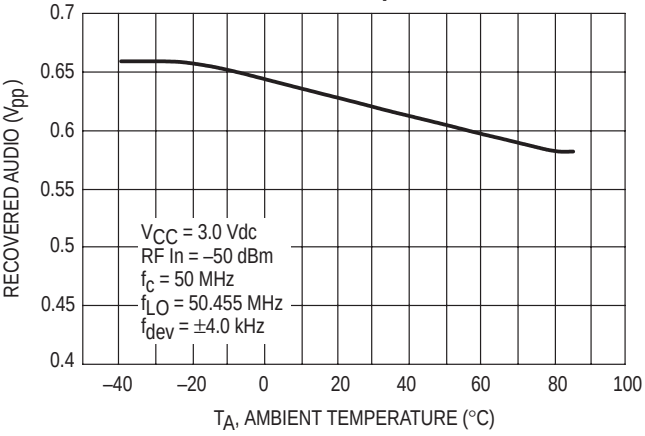


Figure 25. Demod DC Output Voltage versus Ambient Temperature

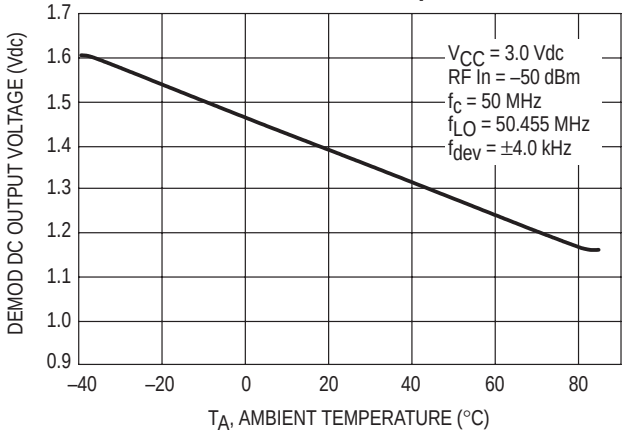


Figure 26. LO Current versus Ambient Temperature

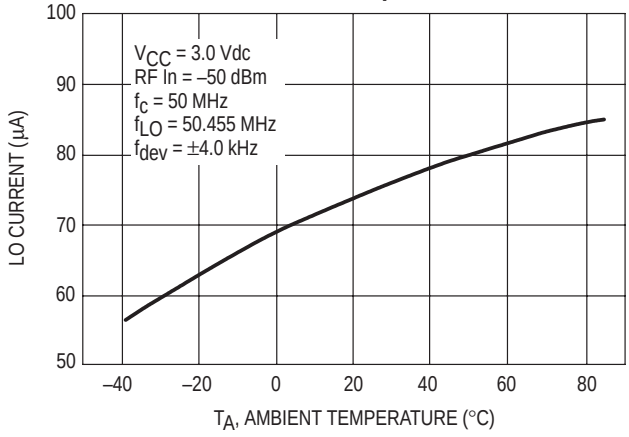


Figure 27. Component Placement View – Circuit Side

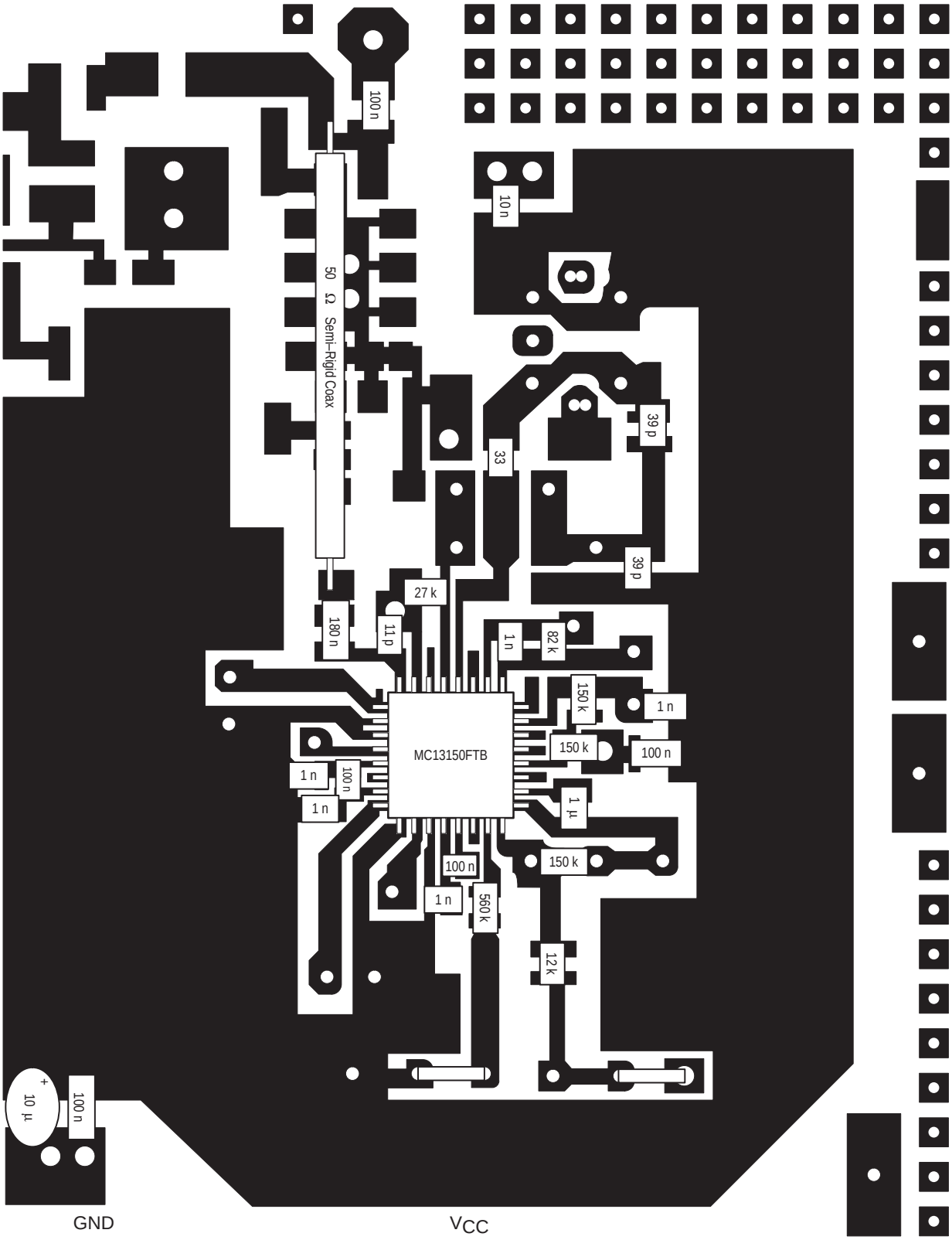


Figure 28. Component Placement View – Ground Side

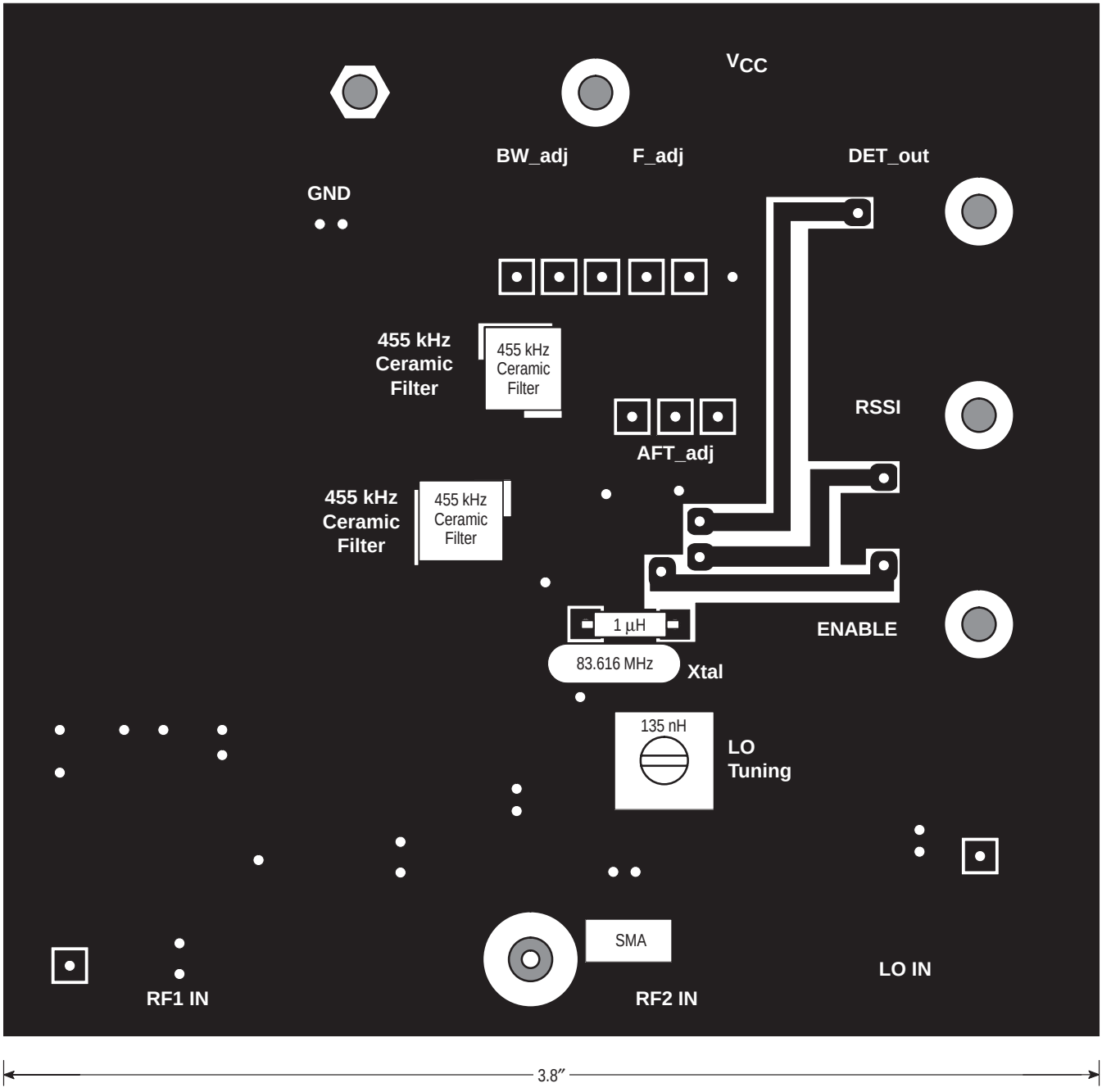


Figure 29. PCB Circuit Side View

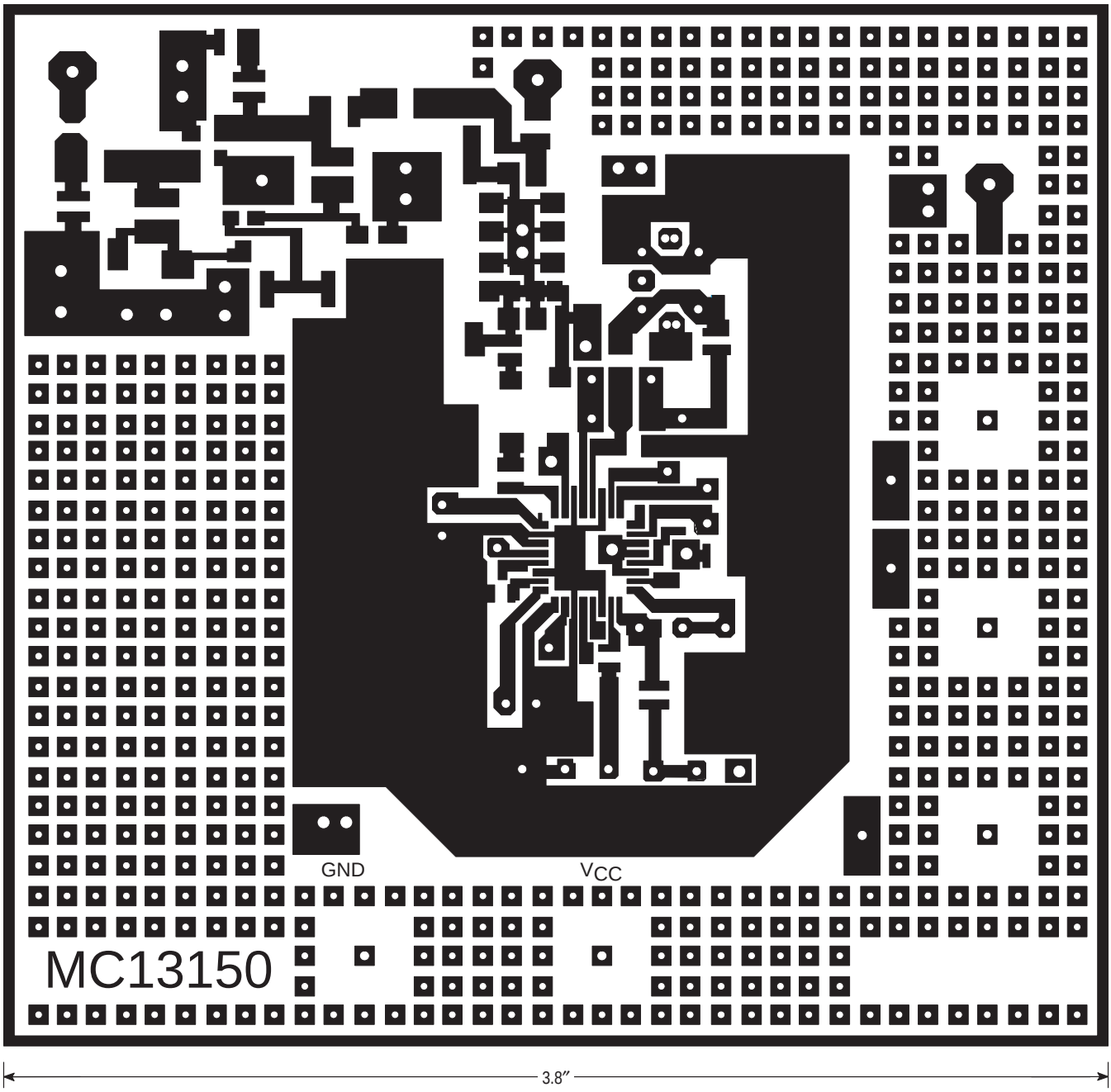
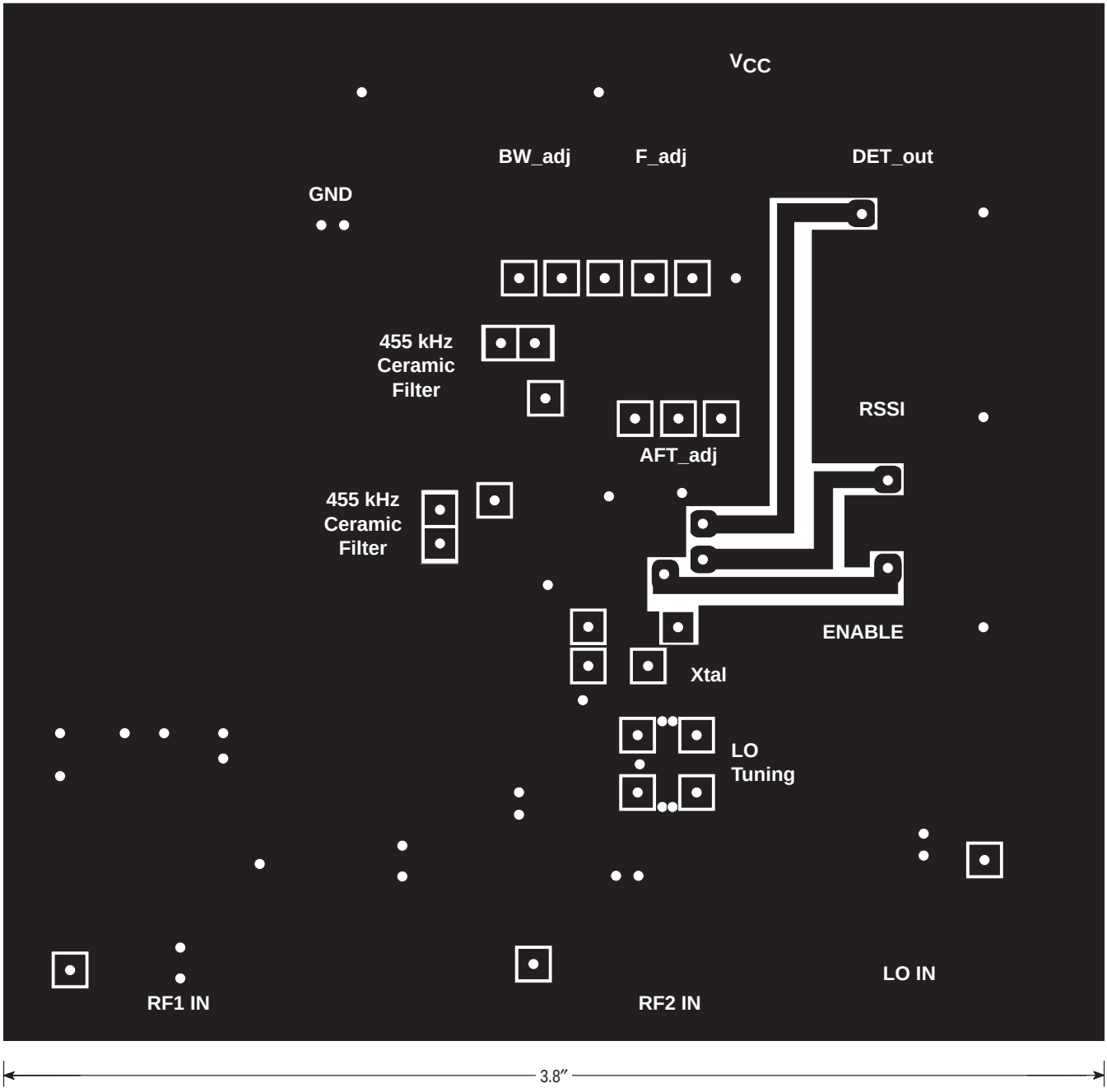


Figure 30. PCB Ground Side View



MOTOROLA

Wideband FM IF

The MC13155 is a complete wideband FM detector designed for satellite TV and other wideband data and analog FM applications. This device may be cascaded for higher IF gain and extended Receive Signal Strength Indicator (RSSI) range.

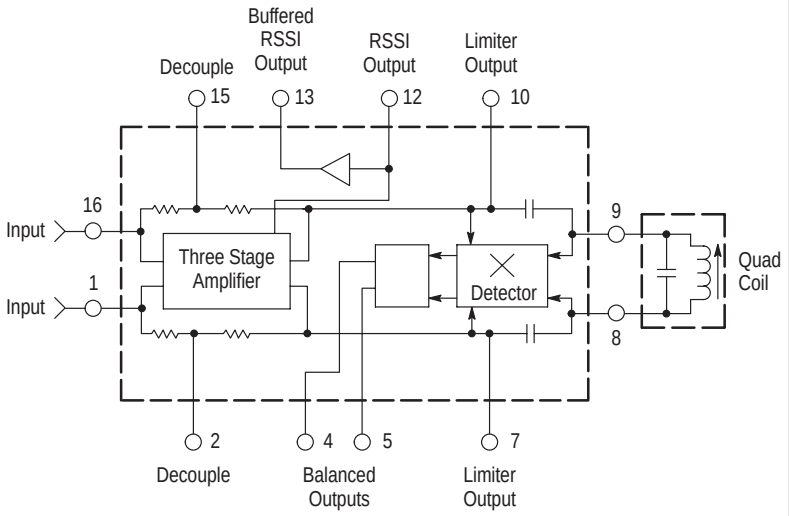
- 12 MHz Video/Baseband Demodulator
- Ideal for Wideband Data and Analog FM Systems
- Limiter Output for Cascade Operation
- Low Drain Current: 7.0 mA
- Low Supply Voltage: 3.0 to 6.0 V
- Operates to 300 MHz

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	11, 14	V_{EE} (max)	6.5	Vdc
Input Voltage	1, 16	V_{in}	1.0	Vrms
Junction Temperature	–	T_J	+150	°C
Storage Temperature Range	–	T_{stg}	– 65 to +150	°C

NOTE: Devices should not be operated at or outside these values. The "Recommended Operating Conditions" provide for actual device operation.

Figure 1. Representative Block Diagram

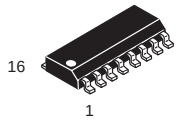


NOTE: This device requires careful layout and decoupling to ensure stable operation.

MC13155

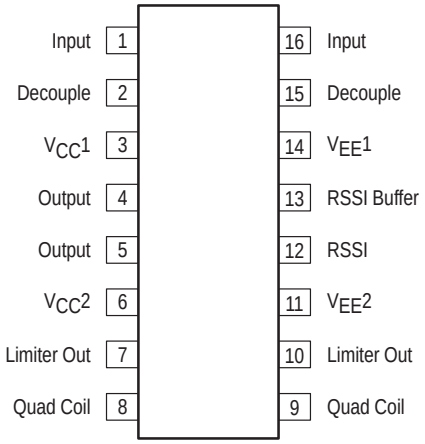
WIDEBAND FM IF

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13155D	T_A = – 40 to +85°C	SO–16

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage (T_A= 25°C) – 40°C ≤ T_A ≤ 85°C	11, 14 3, 6	V_{EE} V_{CC}	– 3.0 to – 6.0 Grounded	Vdc
Maximum Input Frequency	1, 16	f_{in}	300	MHz
Ambient Temperature Range	–	T_J	– 40 to + 85	°C

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, no input signal.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Drain Current (V_{EE} = – 5.0 Vdc) (V_{EE} = – 5.0 Vdc)	11 14 14	I_{11} I_{14} I_{14}	2.0 3.0 3.0	2.8 4.3 4.3	4.0 6.0 6.0	mA
Drain Current Total (see Figure 3) (V_{EE} = – 5.0 Vdc) (V_{EE} = – 6.0 Vdc) (V_{EE} = – 3.0 Vdc)	11, 14	I_{Total}	5.0 5.0 5.0 4.7	7.1 7.5 7.5 6.6	10 10.5 10.5 9.5	mA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, f_{IF} = 70 MHz, V_{EE} = – 5.0 Vdc Figure 2, unless otherwise noted.)

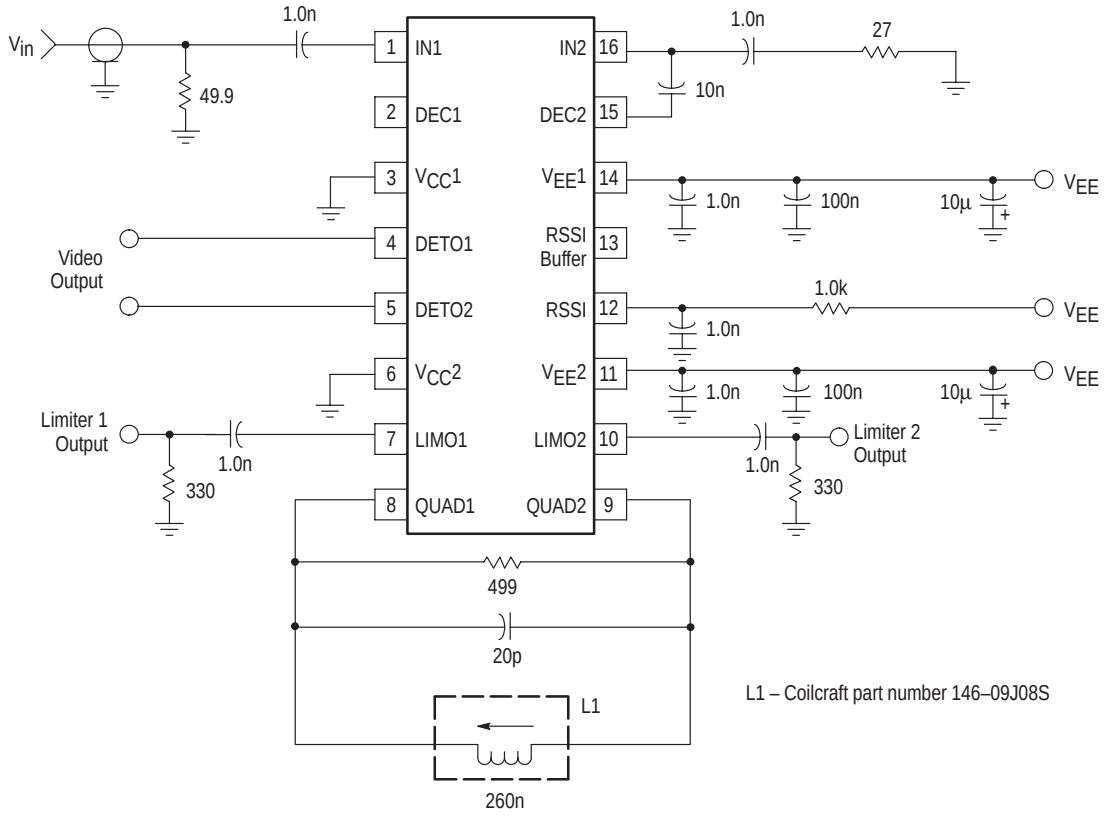
Characteristic	Pin	Min	Typ	Max	Unit
Input for – 3 dB Limiting Sensitivity	1, 16	–	1.0	2.0	mVrms
Differential Detector Output Voltage (V_{in} = 10 mVrms) (f_{dev} = ± 3.0 MHz) (V_{EE} = – 6.0 Vdc) (V_{EE} = – 5.0 Vdc) (V_{EE} = – 3.0 Vdc)	4, 5	 470 450 380	 590 570 500	 700 680 620	$mV_{p–p}$
Detector DC Offset Voltage	4, 5	– 250	–	250	mVdc
RSSI Slope	13	1.4	2.1	2.8	µA/dB
RSSI Dynamic Range	13	31	35	39	dB
RSSI Output (V_{in} = 100 µVrms) (V_{in} = 1.0 mVrms) (V_{in} = 10 mVrms) (V_{in} = 100 mVrms) (V_{in} = 500 mVrms)	12	 – – 16 – –	 2.1 2.4 24 65 75	 – – 36 – –	µA
RSSI Buffer Maximum Output Current (V_{in} = 10 mVrms)	13	–	2.3	–	mAdc
Differential Limiter Output (V_{in} = 1.0 mVrms) (V_{in} = 10 mVrms)	7, 10	100 –	140 180	– –	mVrms
Demodulator Video 3.0 dB Bandwidth	4, 5	–	12	–	MHz
Input Impedance (Figure 14) @ 70 MHz Rp (V_{EE} = – 5.0 Vdc) Cp (C_2=C_{15} = 100 p)	1, 16	 – –	 450 4.8	 – –	 Ω pF
Differential IF Power Gain	1, 7, 10, 16	–	46	–	dB

NOTE: Positive currents are out of the pins of the device.

CIRCUIT DESCRIPTION

The MC13155 consists of a wideband three–stage limiting amplifier, a wideband quadrature detector which may be operated up to 200 MHz, and a received signal strength indicator (RSSI) circuit which provides a current output linearly proportional to the IF input signal level for approximately 35 dB range of input level.

Figure 2. Test Circuit



APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB shown in Figures 19 and 20 is very versatile and is designed to cascade two ICs. The center section of the board provides an area for attaching all surface mount components to the circuit side and radial leaded components to the component ground side of the PCB (see Figures 17 and 18). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Limiting Amplifier

Differential input and output ports interfacing the three stage limiting amplifier provide a differential power gain of typically 46 dB and useable frequency range of 300 MHz. The IF gain flatness may be controlled by decoupling of the internal feedback network at Pins 2 and 15.

Scattering parameter (S–parameter) characterization of the IF as a two port linear amplifier is useful to implement maximum stable power gain, input matching, and stability over a desired bandpass response and to ensure stable operation outside the bandpass as well. The MC13155 is unconditionally stable over most of its useful operating frequency range; however, it can be made unconditionally stable over its entire operating range with the proper decoupling of Pins 2 and 15. Relatively small decoupling capacitors of about 100 pF have a significant effect on the wideband response and stability. This is shown in the scattering parameter tables where S–parameters are shown for various values of C2 and C15 and at V_{EE} of – 3.0 and – 5.0 Vdc.

TYPICAL PERFORMANCE AT TEMPERATURE
(See Figure 2. Test Circuit)

Figure 3. Drain Current versus Supply Voltage

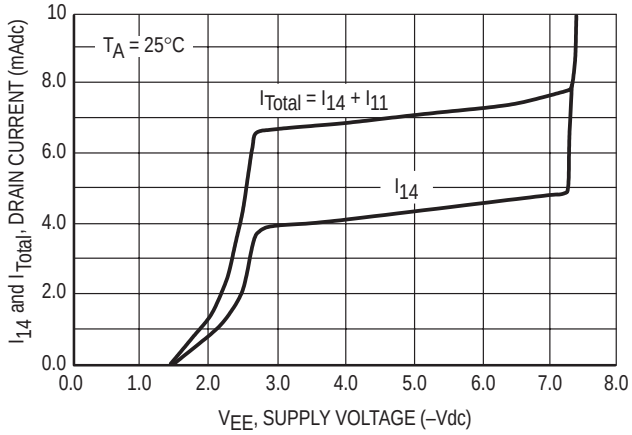


Figure 4. RSSI Output versus Frequency and Input Signal Level

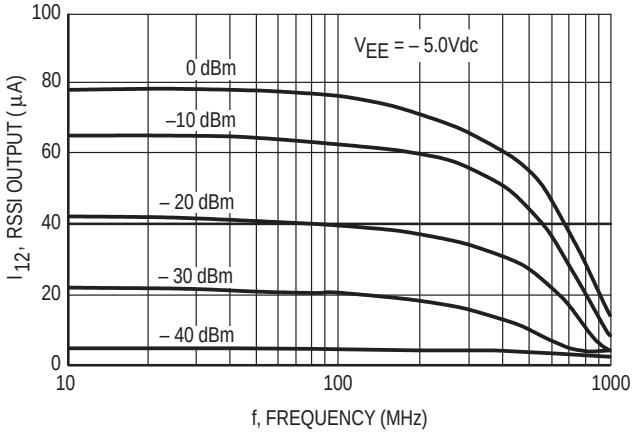


Figure 5. Total Drain Current versus Ambient Temperature and Supply Voltage

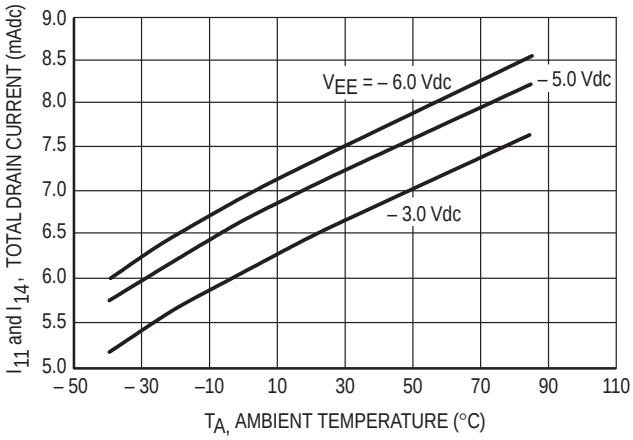


Figure 6. Detector Drain Current and Limiter Drain Current versus Ambient Temperature

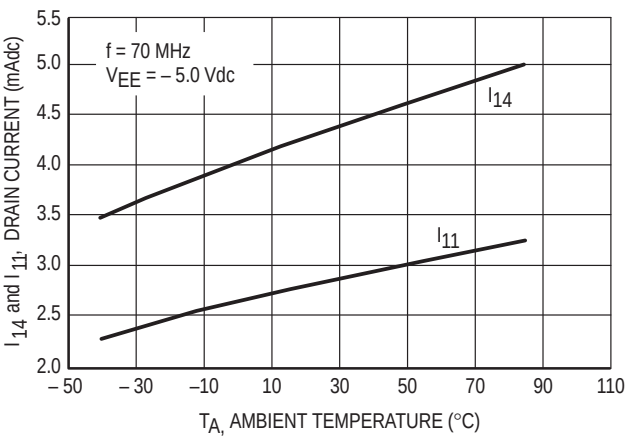


Figure 7. RSSI Output versus Ambient Temperature and Supply Voltage

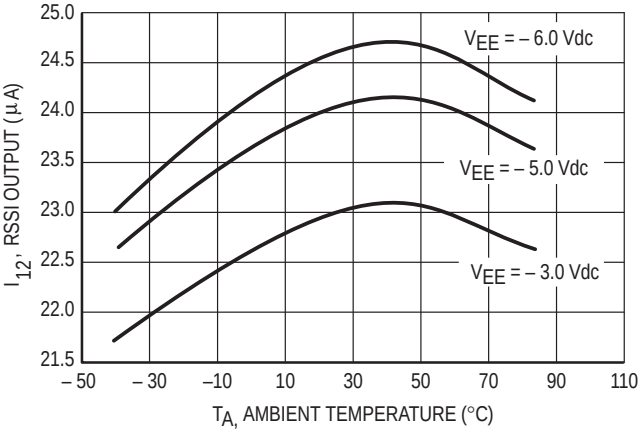


Figure 8. RSSI Output versus Input Signal Voltage (V_{in} at Temperature)

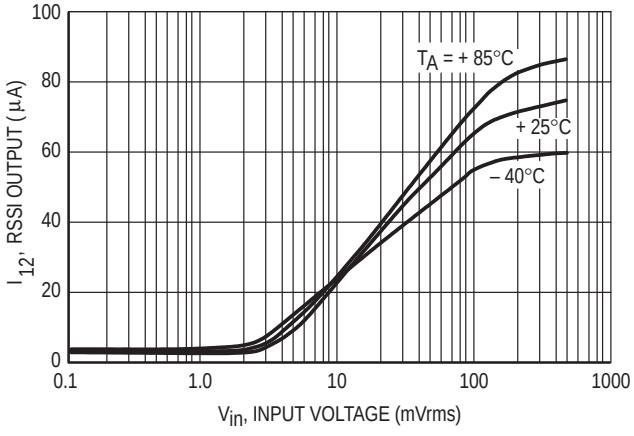


Figure 9. Differential Detector Output Voltage versus Ambient Temperature and Supply Voltage

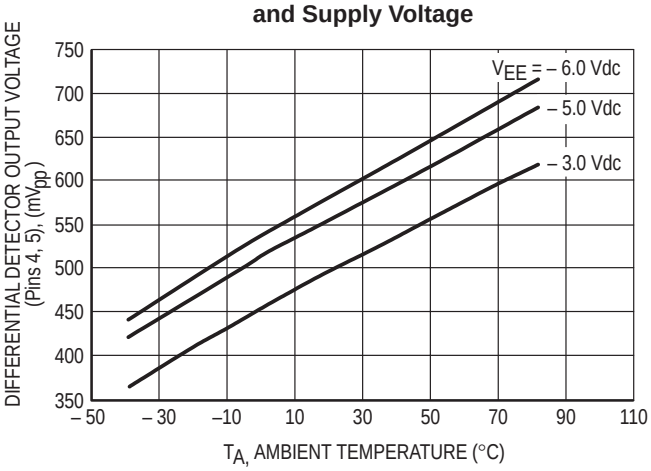


Figure 10. Differential Limiter Output Voltage versus Ambient Temperature
(V_{in} = 1 and 10 mVrms)

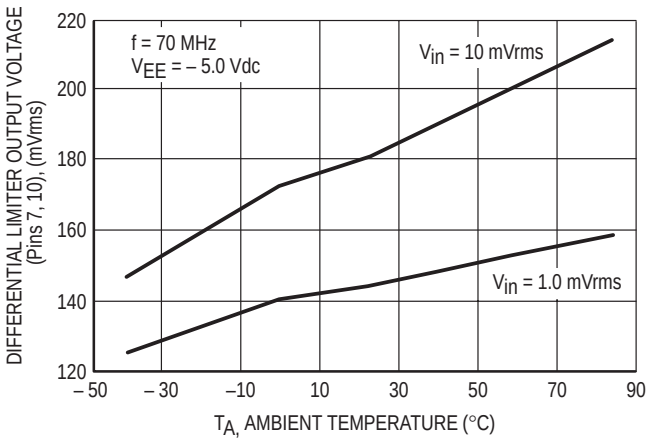


Figure 11A. Differential Detector Output Voltage versus Q of Quadrature LC Tank

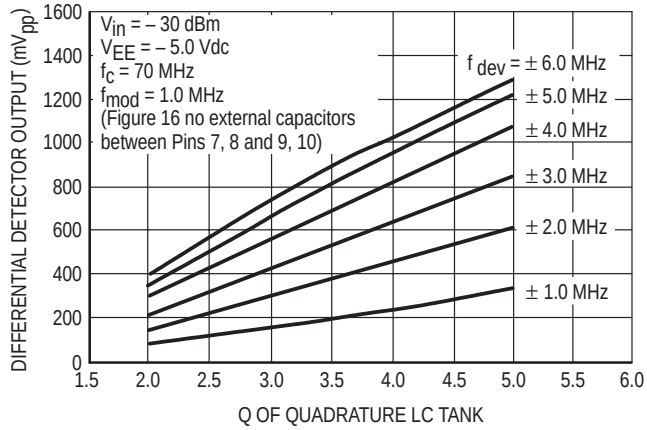


Figure 11B. Differential Detector Output Voltage versus Q of Quadrature LC Tank

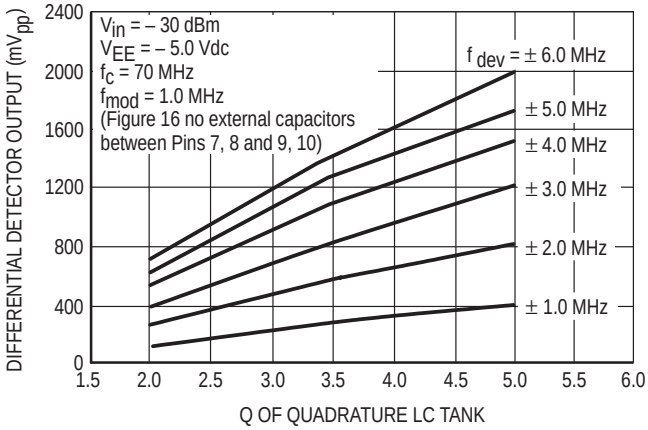


Figure 12. RSSI Output Voltage versus IF Input

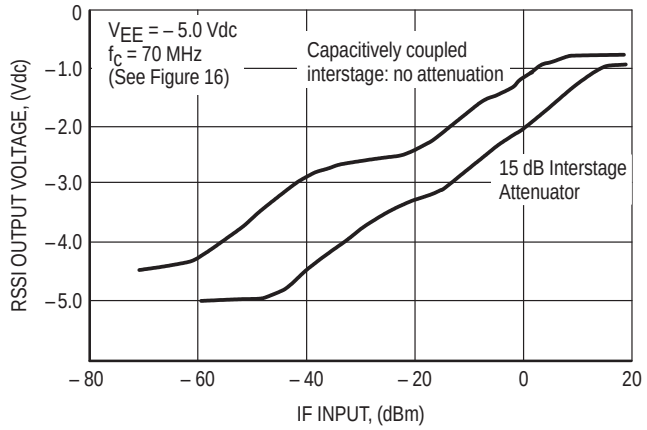
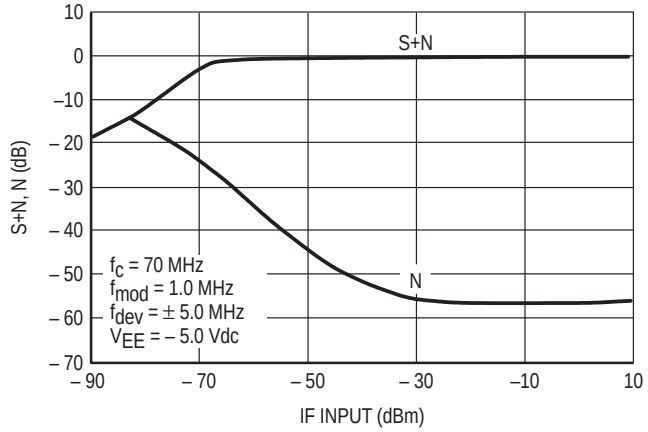


Figure 13. – S+N, N versus IF Input



In the S–parameters measurements, the IF is treated as a two–port linear class A amplifier. The IF amplifier is measured with a single–ended input and output configuration in which the Pins 16 and 7 are terminated in the series combination of a 47 Ω resistor and a 10 nF capacitor to V_{CC} ground (see Figure 14. S–Parameter Test Circuit).

The S–parameters are in polar form as the magnitude (MAG) and angle (ANG). Also listed in the tables are the calculated values for the stability factor (K) and the Maximum Available Gain (MAG). These terms are related in the following equations:

$$K = (1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2) / (2 |S_{12} S_{21}|)$$

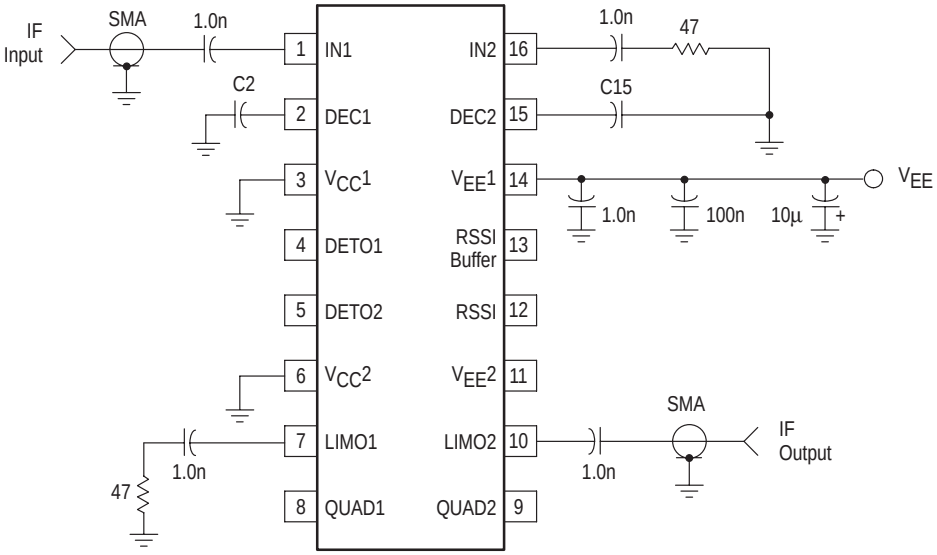
where: $|\Delta| = |S_{11} S_{22} - S_{12} S_{21}|$.

$$MAG = 10 \log |S_{21}| / |S_{12}| + 10 \log |K - (K^2 - 1)^{1/2}|$$

where: K > 1. The necessary and sufficient conditions for unconditional stability are given as K > 1:

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0$$

Figure 14. S–Parameter Test Circuit



S–Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 0 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.94	–13	8.2	143	0.001	7.0	0.87	– 22	2.2	32
2.0	0.78	– 23	23.5	109	0.001	– 40	0.64	– 31	4.2	33.5
5.0	0.48	1.0	39.2	51	0.001	– 97	0.34	–17	8.7	33.7
7.0	0.59	15	40.3	34	0.001	– 41	0.33	–13	10.6	34.6
10	0.75	17	40.9	19	0.001	– 82	0.41	–1.0	5.7	36.7
20	0.95	7.0	42.9	– 6.0	0.001	– 42	0.45	0	1.05	46.4
50	0.98	–10	42.2	– 48	0.001	– 9.0	0.52	– 3.0	0.29	–
70	0.95	–16	39.8	– 68	0.001	112	0.54	–16	1.05	46.4
100	0.93	– 23	44.2	– 93	0.001	80	0.53	– 22	0.76	–
150	0.91	– 34	39.5	–139	0.001	106	0.50	– 34	0.94	–
200	0.87	– 47	34.9	–179	0.002	77	0.42	– 44	0.97	–
500	0.89	–103	11.1	– 58	0.022	57	0.40	–117	0.75	–
700	0.61	–156	3.5	–164	0.03	0	0.52	179	2.6	13.7
900	0.56	162	1.2	92	0.048	– 44	0.47	112	4.7	4.5
1000	0.54	131	0.8	42	0.072	– 48	0.44	76	5.1	0.4

S–Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 100 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.98	–15	11.7	174	0.001	–14	0.84	– 27	1.2	37.4
2.0	0.50	– 2.0	39.2	85.5	0.001	–108	0.62	– 35	6.0	35.5
5.0	0.87	8.0	39.9	19	0.001	100	0.47	– 9.0	4.2	39.2
7.0	0.90	5.0	40.4	9.0	0.001	– 40	0.45	– 8.0	3.1	40.3
10	0.92	3.0	41	1.0	0.001	– 40	0.44	– 5.0	2.4	41.8
20	0.92	– 2.0	42.4	–14	0.001	– 87	0.49	– 6.0	2.4	41.9
50	0.91	– 8.0	41.2	– 45	0.001	85	0.50	– 5.0	2.3	42
70	0.91	–11	39.1	– 63	0.001	76	0.52	– 4.0	2.2	41.6
100	0.91	–15	43.4	– 84	0.001	85	0.50	–11	1.3	43.6
150	0.90	– 22	38.2	–126	0.001	96	0.43	– 22	1.4	41.8
200	0.86	– 33	35.5	–160	0.002	78	0.43	– 21	1.3	39.4
500	0.80	– 66	8.3	– 9.0	0.012	75	0.57	– 63	1.7	23.5
700	0.62	– 96	2.9	– 95	0.013	50	0.49	–111	6.3	12.5
900	0.56	–120	1.0	–171	0.020	53	0.44	–150	13.3	2.8
1000	0.54	–136	0.69	154	0.034	65	0.44	–179	12.5	– 0.8

S–Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 680 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.74	4.0	53.6	110	0.001	101	0.97	– 35	0.58	–
2.0	0.90	3.0	70.8	55	0.001	60	0.68	– 34	1.4	45.6
5.0	0.91	0	87.1	21	0.001	–121	0.33	– 60	1.1	49
7.0	0.91	0	90.3	11	0.001	–18	0.25	– 67	1.2	48.4
10	0.91	– 2.0	92.4	2.0	0.001	33	0.14	– 67	1.5	47.5
20	0.91	– 4.0	95.5	–16	0.001	63	0.12	–15	1.3	48.2
50	0.90	– 8.0	89.7	– 50	0.001	– 43	0.24	26	1.8	46.5
70	0.90	–10	82.6	–70	0.001	92	0.33	21	1.4	47.4
100	0.91	–14	77.12	–93	0.001	23	0.42	–1.0	1.05	49
150	0.94	– 20	62.0	–122	0.001	96	0.42	– 22	0.54	–
200	0.95	– 33	56.9	–148	0.003	146	0.33	– 62	0.75	–
500	0.82	– 63	12.3	–12	0.007	79	0.44	– 67	1.8	26.9
700	0.66	– 98	3.8	–107	0.014	84	0.40	–115	4.8	14.6
900	0.56	–122	1.3	177	0.028	78	0.39	–166	8.0	4.7
1000	0.54	–139	0.87	141	0.048	76	0.41	165	7.4	0.96

S–Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 0 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.89	–14	9.3	136	0.001	2.0	0.84	– 27	3.2	30.7
2.0	0.76	– 22	24.2	105	0.001	– 90	0.67	– 37	3.5	34.3
5.0	0.52	5.0	35.7	46	0.001	– 32	0.40	–13	10.6	33.3
7.0	0.59	12	38.1	34	0.001	– 41	0.40	–10	9.1	34.6
10	0.78	15	37.2	16	0.001	– 92	0.40	–1.0	5.7	36.3
20	0.95	5.0	38.2	– 9.0	0.001	47	0.51	– 4.0	0.94	–
50	0.96	–11	39.1	– 50	0.001	–103	0.48	– 6.0	1.4	43.7
70	0.93	–17	36.8	– 71	0.001	– 76	0.52	–13	2.2	41.4
100	0.91	– 25	34.7	– 99	0.001	–152	0.51	–19	3.0	39.0
150	0.86	– 37	33.8	–143	0.001	53	0.49	– 34	1.7	39.1
200	0.81	– 49	27.8	86	0.003	76	0.55	– 56	2.4	35.1
500	0.70	– 93	6.2	– 41	0.015	93	0.40	–110	2.4	19.5
700	0.62	–144	1.9	–133	0.049	56	0.40	–150	3.0	8.25
900	0.39	–176	0.72	125	0.11	–18	0.25	163	5.1	–1.9
1000	0.44	166	0.49	80	0.10	– 52	0.33	127	7.5	– 4.8

S–Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 100 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.97	–15	11.7	171	0.001	– 4.0	0.84	– 27	1.4	36.8
2.0	0.53	2.0	37.1	80	0.001	– 91	0.57	– 31	6.0	34.8
5.0	0.88	7.0	37.7	18	0.001	– 9.0	0.48	– 7.0	3.4	39.7
7.0	0.90	5.0	37.7	8.0	0.001	–11	0.49	– 7.0	2.3	41
10	0.92	2.0	38.3	1.0	0.001	– 59	0.51	– 9.0	2.0	41.8
20	0.92	– 2.0	39.6	–15	0.001	29	0.48	– 3.0	1.9	42.5
50	0.91	– 8.0	38.5	– 46	0.001	– 21	0.51	– 7.0	2.3	41.4
70	0.91	–11	36.1	– 64	0.001	49	0.50	– 8.0	2.3	40.8
100	0.91	–15	39.6	– 85	0.001	114	0.52	–13	1.7	37.8
150	0.89	– 22	34.4	–128	0.001	120	0.48	– 23	1.6	40.1
200	0.86	– 33	32	–163	0.002	86	0.40	– 26	1.7	37.8
500	0.78	– 64	7.6	–12	0.013	94	0.46	– 71	1.9	22.1
700	0.64	– 98	2.3	–102	0.027	58	0.42	–109	4.1	10.1
900	0.54	–122	0.78	179	0.040	38.6	0.35	–147	10.0	– 0.14
1000	0.53	–136	0.47	144	0.043	23	0.38	–171	15.4	– 4.52

S–Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 680 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.81	3.0	37	101	0.001	–19	0.90	– 32	1.1	43.5
2.0	0.90	2.0	47.8	52.7	0.001	– 82	0.66	– 39	0.72	–
5.0	0.91	0	58.9	20	0.001	104	0.37	– 56	2.3	44
7.0	0.90	–1	60.3	11	0.001	– 76	0.26	– 55	2.04	44
10	0.91	– 2.0	61.8	3.0	0.001	105	0.18	– 52	2.2	43.9
20	0.91	– 4.0	63.8	– 15	0.001	59	0.11	–13	2.0	44.1
50	0.90	– 8.0	60.0	– 48	0.001	96	0.22	33	2.3	43.7
70	0.90	–11	56.5	– 67	0.001	113	0.29	15	2.3	43.2
100	0.91	–14	52.7	– 91	0.001	177	0.36	5.0	2.0	43
150	0.93	– 21	44.5	–126	0.001	155	0.35	–17	1.8	42.7
200	0.90	– 43	41.2	–162	0.003	144	0.17	– 31	1.6	34.1
500	0.79	– 65	7.3	–13	0.008	80	0.44	– 75	3.0	22
700	0.65	– 97	2.3	–107	0.016	86	0.38	–124	7.1	10.2
900	0.56	–122	0.80	174	0.031	73	0.38	–174	12	0.37
1000	0.55	–139	0.52	137	0.50	71	0.41	157	11.3	– 3.4

DC Biasing Considerations

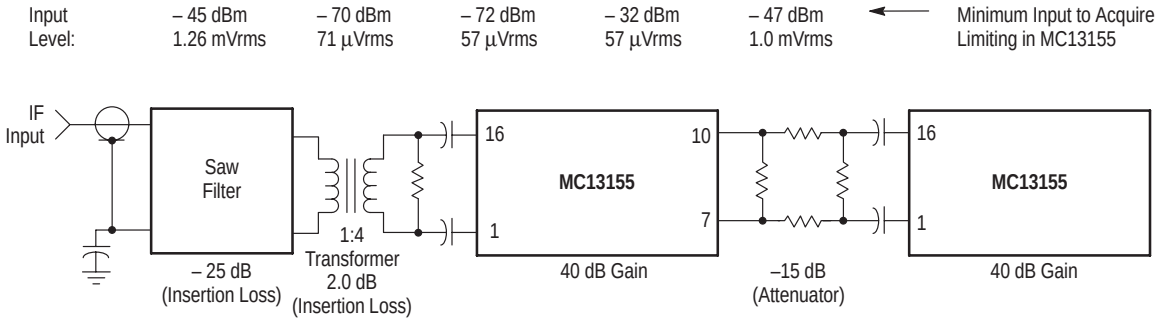
The DC biasing scheme utilizes two V_{CC} connections (Pins 3 and 6) and two V_{EE} connections (Pins 14 and 11). $V_{EE}1$ (Pin 14) is connected internally to the IF and RSSI circuits' negative supply bus while $V_{EE}2$ (Pin 11) is connected internally to the quadrature detector's negative bus. Under positive ground operation, this unique configuration offers the ability to bias the RSSI and IF separately from the quadrature detector. When two ICs are cascaded as shown in the 70 MHz application circuit and provided by the PCB (see Figures 17 and 18), the first MC13155 is used without biasing its quadrature detector, thereby saving approximately 3.0 mA. A total current of 7.0 mA is used to fully bias each IC, thus the total current in the application circuit is approximately 11 mA. Both V_{CC} pins are biased by the same supply. $V_{CC}1$ (Pin 3) is connected internally to the positive bus of the first half of the IF limiting amplifier, while $V_{CC}2$ is internally connected to the positive bus of the RSSI, the quadrature detector circuit, and the second half of the IF limiting amplifier (see Figure 15). This distribution of the V_{CC} enhances the stability of the IC.

RSSI Circuitry

The RSSI circuitry provides typically 35 dB of linear dynamic range and its output voltage swing is adjusted by selection of the resistor from Pin 12 to V_{EE}. The RSSI slope is typically 2.1 μA/dB ; thus, for a dynamic range of 35 dB, the current output is approximately 74 μA. A 47 k resistor will yield an RSSI output voltage swing of 3.5 Vdc. The RSSI buffer output at Pin 13 is an emitter–follower and needs an external emitter resistor of 10 k to V_{EE}.

In a cascaded configuration (see circuit application in Figure 16), only one of the RSSI Buffer outputs (Pin 13) is used; the RSSI outputs (Pin 12 of each IC) are tied together and the one closest to the V_{EE} supply trace is decoupled to V_{CC} ground. The two pins are connected to V_{EE} through a 47 k resistor. This resistor sources a RSSI current which is proportional to the signal level at the IF input; typically, 1.0 mVrms (– 47 dBm) is required to place the MC13155 into limiting. The measured RSSI output voltage response of the application circuit is shown in Figure 12. Since the RSSI current output is dependent upon the input signal level at the IF input, a careful accounting of filter losses, matching and other losses and gains must be made in the entire receiver system. In the block diagram of the application circuit shown below, an accounting of the signal levels at points throughout the system shows how the RSSI response in Figure 12 is justified.

Block Diagram of 70 MHz Video Receiver Application Circuit

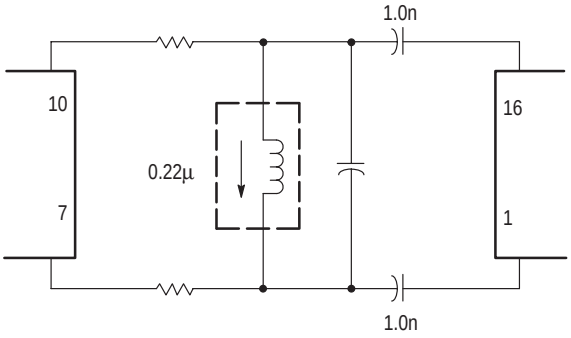


Cascading Stages

The limiting IF output is pinned–out differentially, cascading is easily achieved by AC coupling stage to stage. In the evaluation PCB, AC coupling is shown, however, interstage filtering may be desirable in some applications. In which case, the S–parameters provide a means to implement a low loss interstage match and better receiver sensitivity.

Where a linear response of the RSSI output is desired when cascading the ICs, it is necessary to provide at least 10 dB of interstage loss. Figure 12 shows the RSSI response with and without interstage loss. A 15 dB resistive attenuator is an inexpensive way to linearize the RSSI response. This has its drawbacks since it is a wideband noise source that is dependent upon the source and load impedance and the amount of attenuation that it provides. A better, although more costly, solution would be a bandpass filter designed to the desired center frequency and bandpass response while carefully selecting the insertion loss. A network topology shown below may be used to provide a bandpass response with the desired insertion loss.

Network Topology



Quadrature Detector

The quadrature detector is coupled to the IF with internal 2.0 pF capacitors between Pins 7 and 8 and Pins 9 and 10. For wideband data applications, such as FM video and satellite receivers, the drive to the detector can be increased with additional external capacitors between these pins, thus, the recovered video signal level output is increased for a given bandwidth (see Figure 11A and Figure 11B).

The wideband performance of the detector is controlled by the loaded Q of the LC tank circuit. The following equation defines the components which set the detector circuit's bandwidth:

$$Q = R_T/X_L \quad (1)$$

where: R_T is the equivalent shunt resistance across the LC Tank and X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi fL$).

The inductor and capacitor are chosen to form a resonant LC Tank with the PCB and parasitic device capacitance at the desired IF center frequency as predicted by:

$$fc = (2\pi \sqrt{(LC_p)})^{-1} \quad (2)$$

where: L is the parallel tank inductor and C_p is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a wideband detector at 70 MHz and a loaded Q of 5. The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass. For an IF frequency of 70 MHz and an IF bandpass of 10.9 MHz, the IF bandpass Q is approximately 6.4.

Example:

Let the external Cext = 20 pF. (The minimum value here should be greater than 15 pF making it greater than the internal device and PCB parasitic capacitance, Cint ≈ 3.0 pF).

$$C_p = Cint + Cext = 23\ pF$$

Rewrite Equation 2 and solve for L:

$L = (0.159)^2 /(C_p\ fc^2)$

L = 198 nH, thus, a standard value is chosen.

L = 0.22 μH (tunable shielded inductor).

The value of the total damping resistor to obtain the required loaded Q of 5 can be calculated by rearranging Equation 1:

$$R_T = Q(2\pi fL)$$

$R_T = 5\ (2\pi)(70)(0.22) = 483.8\ \Omega.$

The internal resistance, Rint between the quadrature tank Pins 8 and 9 is approximately 3200 Ω and is considered in determining the external resistance, Rext which is calculated from:

$Rext = ((R_T)(Rint))/ (Rint – R_T)$

Rext = 570, thus, choose the standard value.

Rext = 560 Ω.

SAW Filter

In wideband video data applications, the IF occupied bandwidth may be several MHz wide. A good rule of thumb is to choose the IF frequency about 10 or more times greater than the IF occupied bandwidth. The IF bandpass filter is a SAW filter in video data applications where a very selective response is needed (i.e., very sharp bandpass response). The evaluation PCB is laid out to accommodate two SAW filter package types: 1) A five–leaded plastic SIP package. Recommended part numbers are Siemens X6950M which operates at 70 MHz; 10.4 MHz 3 dB passband, X6951M (X252.8) which operates at 70 MHz; 9.2 MHz 3 dB passband; and X6958M which operates at 70 MHz, 6.3 MHz 3 dB passband, and 2) A four–leaded TO–39 metal can package. Typical insertion loss in a wide bandpass SAW filter is 25 dB.

The above SAW filters require source and load impedances of 50 Ω to assure stable operation. On the PC board layout, space is provided to add a matching network, such as a 1:4 surface mount transformer between the SAW filter output and the input to the MC13155. A 1:4 transformer, made by Coilcraft and Mini Circuits, provides a suitable interface (see Figures 16, 17 and 18). In the circuit and layout, the SAW filter and the MC13155 are differentially configured with interconnect traces which are equal in length and symmetrical. This balanced feed enhances RF stability, phase linearity, and noise performance.

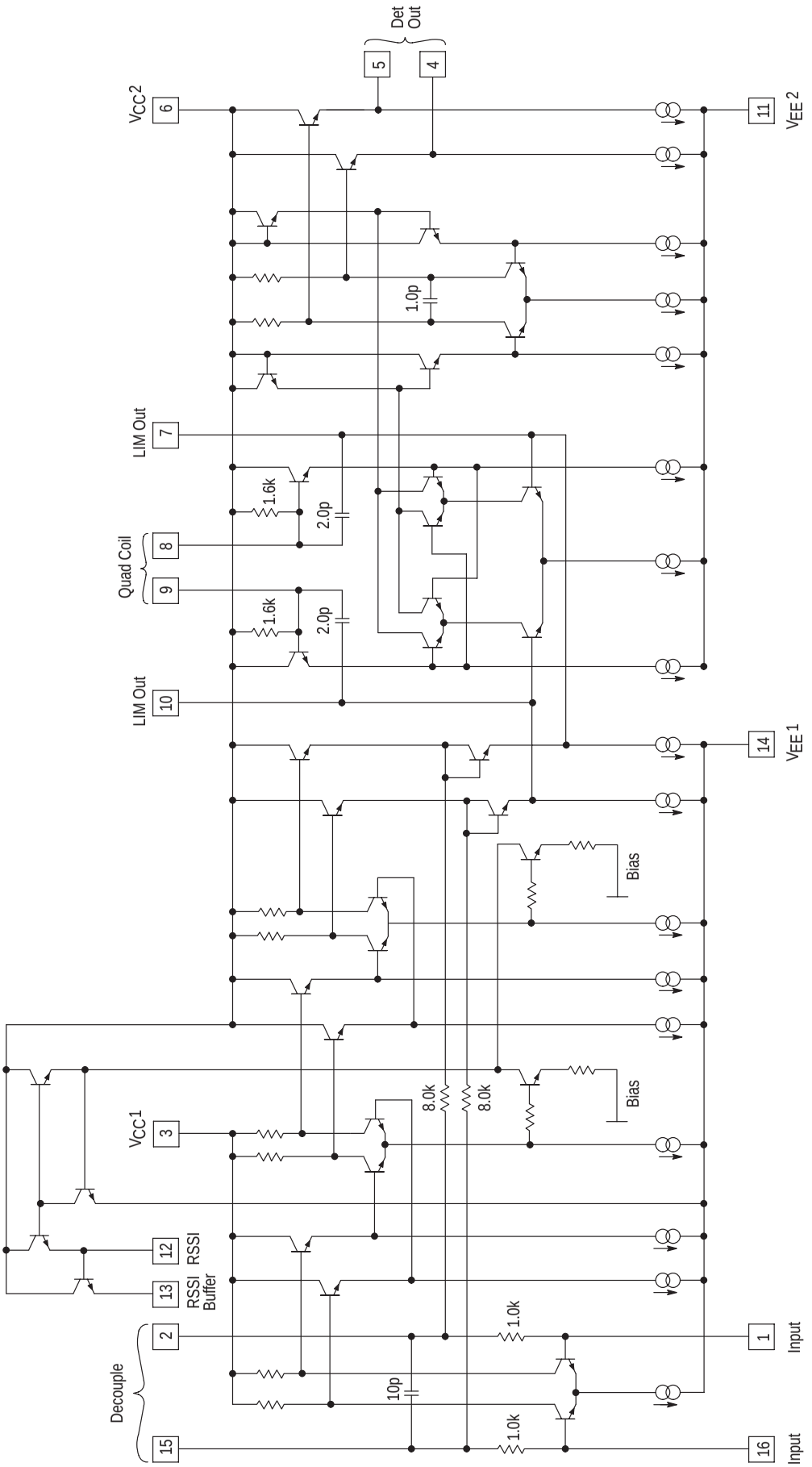


Figure 15. Simplified Internal Circuit Schematic

Figure 16. 70 MHz Video Receiver Application Circuit

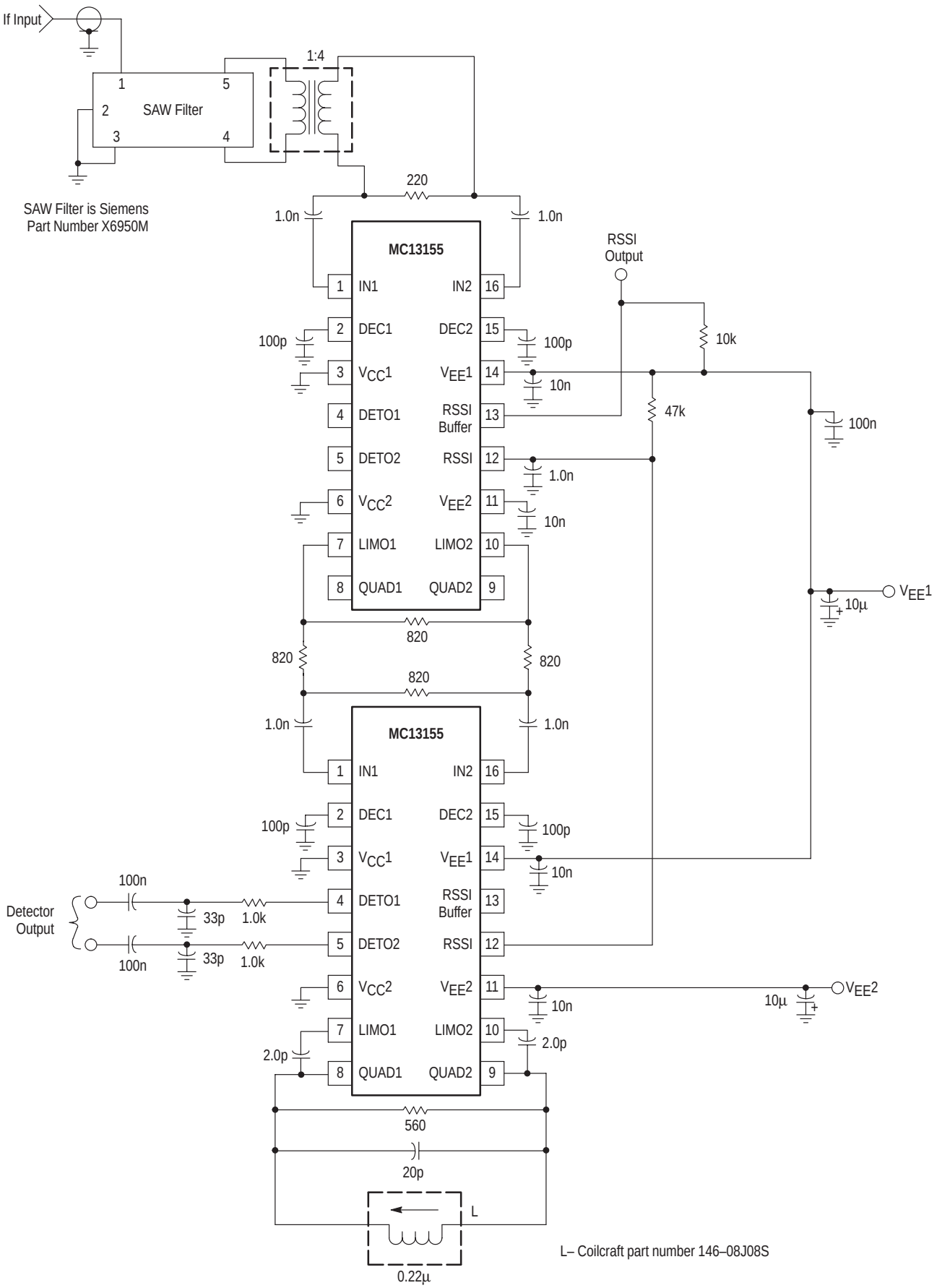


Figure 17. Component Placement (Circuit Side)

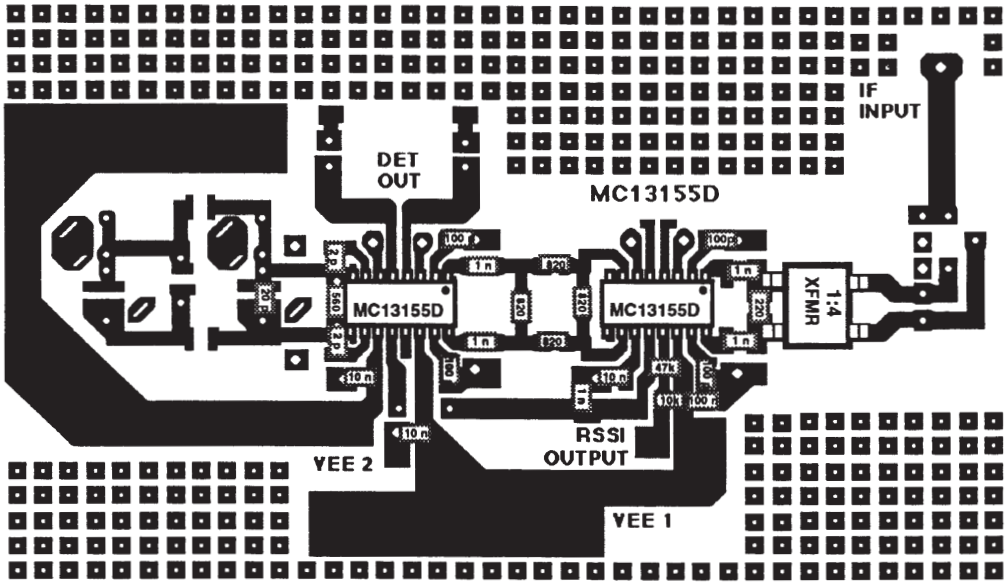


Figure 18. Component Placement (Ground Side)

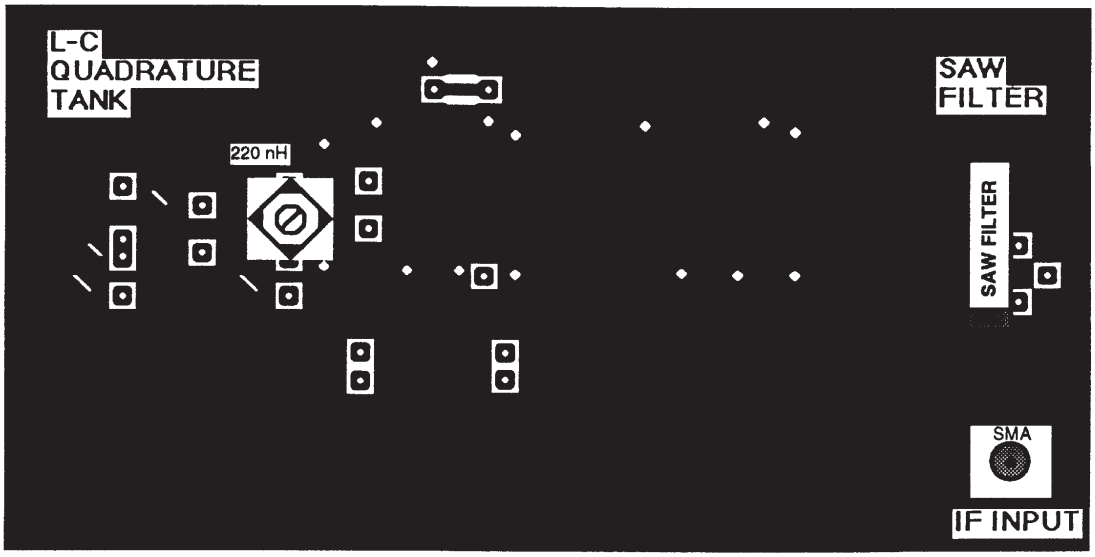


Figure 19. Circuit Side View

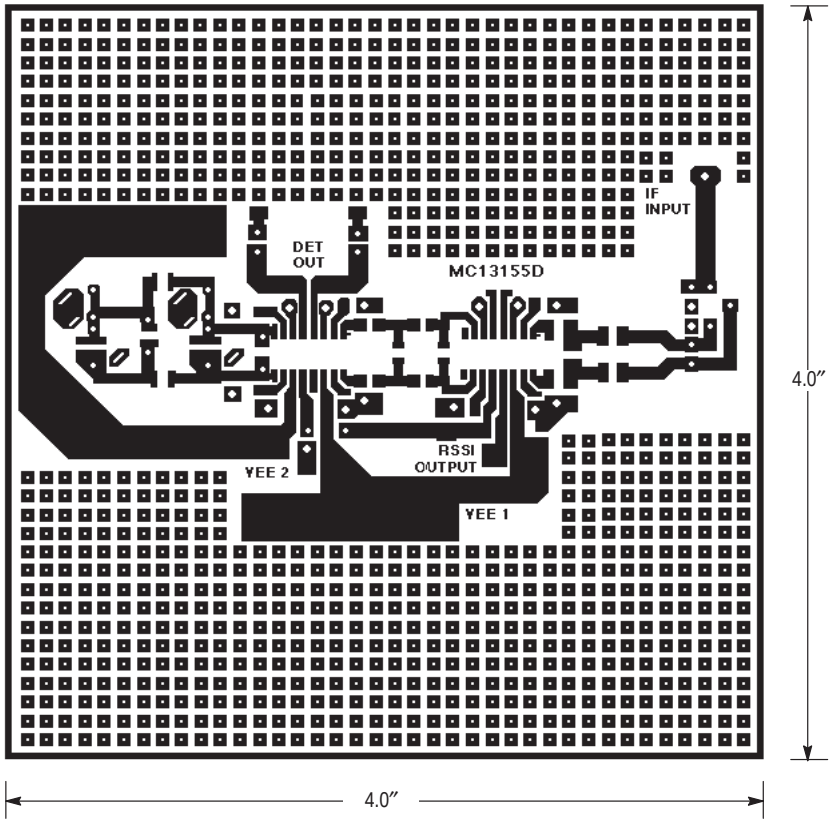
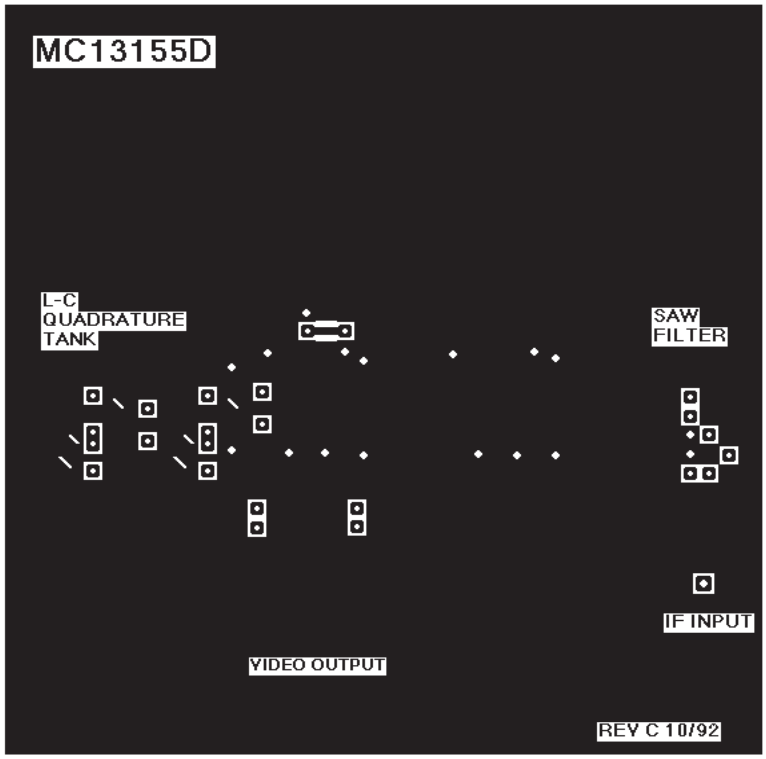


Figure 20. Ground Side View



MOTOROLA

MC13156

Wideband FM IF System

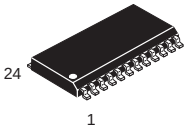
The MC13156 is a wideband FM IF subsystem targeted at high performance data and analog applications. Excellent high frequency performance is achieved at low cost using Motorola's MOSAIC 1.5™ bipolar process. The MC13156 has an onboard grounded collector VCO transistor that may be used with a fundamental or overtone crystal in single channel operation or with a PLL in multichannel operation. The mixer is useful to 500 MHz and may be used in a balanced–differential, or single–ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has a hold function to preset the shaper for fast recovery of new data.

Applications for the MC13156 include CT–2, wideband data links and other radio systems utilizing GMSK, FSK or FM modulation.

- 2.0 to 6.0 Vdc Operation
- Typical Sensitivity at 200 MHz of 2.0 μV for 12 dB SINAD
- RSSI Dynamic Range Typically 80 dB
- High Performance Data Shaper for Enhanced CT–2 Operation
- Internal 330 Ω and 1.4 kΩ Terminations for 10.7 MHz and 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range
- 3rd Order Intercept (Input) of –25 dBm (Input Matched)

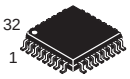
WIDEBAND FM IF SYSTEM FOR DIGITAL AND ANALOG APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA

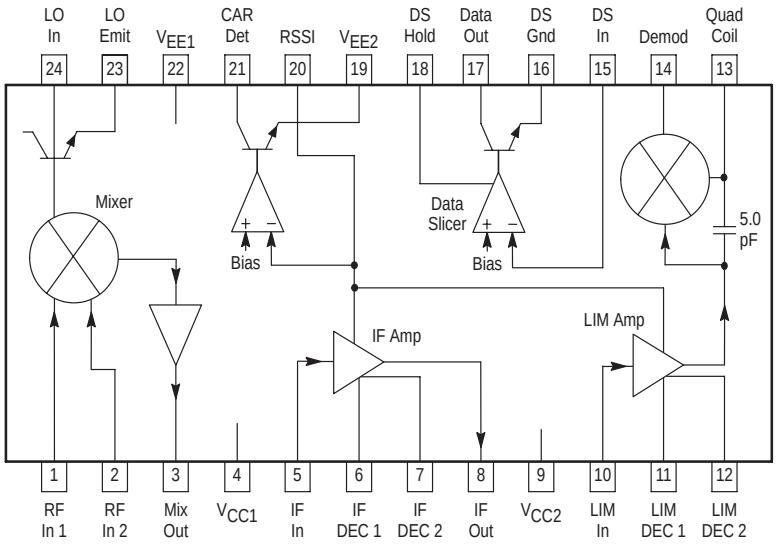


DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)

FB SUFFIX
PLASTIC QFP PACKAGE
CASE 873



Simplified Block Diagram



NOTE: Pin Numbers shown for SOIC package only. Refer to Pin Assignments Table.

This device contains 197 active transistors.

PIN CONNECTIONS

Function	SO–24L	QFP
RF Input 1	1	31
RF Input 2	2	32
Mixer Output	3	1
V_{CC1}	4	2
IF Amp Input	5	3
IF Amp Decoupling 1	6	4
IF Amp Decoupling 2	7	5
V_{CC} Connect (N/C Internal)	–	6
IF Amp Output	8	7
V_{CC2}	9	8
Limiter IF Input	10	9
Limiter Decoupling 1	11	10
Limiter Decoupling 2	12	11
V_{CC} Connect (N/C Internal)	–	12, 13, 14
Quad Coil	13	15
Demodulator Output	14	16
Data Slicer Input	15	17
V_{CC} Connect (N/C Internal)	–	18
Data Slicer Ground	16	19
Data Slicer Output	17	20
Data Slicer Hold	18	21
V_{EE2}	19	22
RSSI Output/Carrier Detect In	20	23
Carrier Detect Output	21	24
V_{EE1} and Substrate	22	25
LO Emitter	23	26
LO Base	24	27
V_{CC} Connect (N/C Internal)	–	28, 29, 30

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13156DW	T_A = –40 to +85°C	SO–24L
MC13156FB		QFP

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	16, 19, 22	$V_{EE(max)}$	–6.5	Vdc
Junction Temperature	–	$T_{J(max)}$	150	°C
Storage Temperature Range	–	T_{stg}	–65 to +150	°C

NOTES: 1. Devices should not be operated at or outside these values. The "Recommended Operating Conditions" table provides for actual device operation.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage @ T_A = 25°C –40°C ≤ T_A ≤ +85°C	4, 9 16, 19, 22	V_{CC} V_{EE}	0 (Ground) –2.0 to –6.0	Vdc
Input Frequency	1, 2	f_{in}	500	MHz
Ambient Temperature Range	–	T_A	–40 to +85	°C
Input Signal Level	1, 2	V_{in}	200	mVrms

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC1} = V_{CC2} = 0, no input signal.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Total Drain Current (See Figure 2)	19, 22	I_{Total}				mA
V_{EE} = –2.0 Vdc			–	4.8	–	
V_{EE} = –3.0 Vdc			3.0	5.0	8.0	
V_{EE} = –5.0 Vdc			–	5.2	–	
V_{EE} = –6.0 Vdc			–	5.4	–	
Drain Current, I_{22} (See Figure 3)	22	I_{22}				mA
V_{EE} = –2.0 Vdc			–	3.0	–	
V_{EE} = –3.0 Vdc			–	3.1	–	
V_{EE} = –5.0 Vdc			–	3.3	–	
V_{EE} = –6.0 Vdc			–	3.4	–	
Drain Current, I_{19} (See Figure 3)	19	I_{19}				mA
V_{EE} = –2.0 Vdc			–	1.8	–	
V_{EE} = –3.0 Vdc			–	1.9	–	
V_{EE} = –5.0 Vdc			–	1.9	–	
V_{EE} = –6.0 Vdc			–	2.0	–	

DATA SLICER (Input Voltage Referenced to V_{EE} = –3.0 Vdc, no input signal; See Figure 15.)

Input Threshold Voltage (High V_{in})	15	V_{15}	1.0	1.1	1.2	Vdc
Output Current (Low V_{in}) Data Slicer Enabled (No Hold) V_{15} > 1.1 Vdc V_{18} = 0 Vdc	17	I_{17}	–	1.7	–	mA

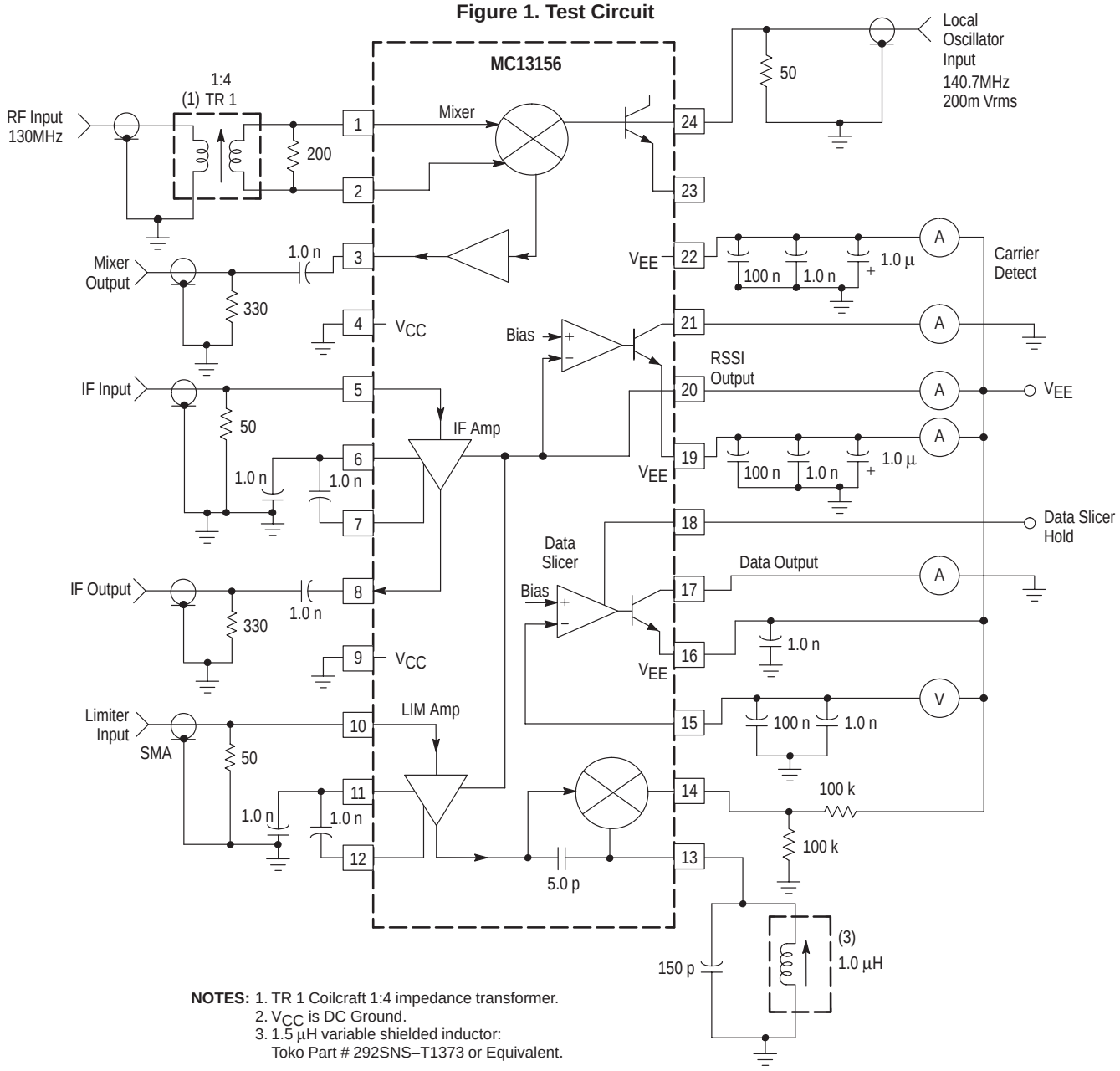
AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{EE} = –3.0 Vdc, f_{RF} = 130 MHz, f_{LO} = 140.7 MHz, Figure 1 test circuit, unless otherwise specified.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
12 dB SINAD Sensitivity (See Figures 17, 25) f_{in} = 144.45 MHz; f_{mod} = 1.0 kHz; f_{dev} = ±75 kHz	1, 14	–	–	–100	–	dBm
MIXER						
Conversion Gain P_{in} = –37 dBm (Figure 4)	1, 3	–	–	22	–	dB
Mixer Input Impedance	1, 2	R_p	–	1.0	–	kΩ
Single–Ended (Table 1)		C_p	–	4.0	–	pF
Mixer Output Impedance	3	–	–	330	–	Ω
IF AMPLIFIER SECTION						
IF RSSI Slope (Figure 6)	20	–	0.2	0.4	0.6	µA/dB
IF Gain (Figure 5)	5, 8	–	–	39	–	dB
Input Impedance	5	–	–	1.4	–	kΩ
Output Impedance	8	–	–	290	–	Ω

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{EE} = –3.0 Vdc, f_{RF} = 130 MHz, f_{LO} = 140.7 MHz, Figure 1 test circuit, unless otherwise specified.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
LIMITING AMPLIFIER SECTION						
Limiter RSSI Slope (Figure 7)	20	–	0.2	0.4	0.6	µA/dB
Limiter Gain	–	–	–	55	–	dB
Input Impedance	10	–	–	1.4	–	kΩ
CARRIER DETECT						
Output Current – Carrier Detect (High V_{in})	21	–	–	0	–	µA
Output Current – Carrier Detect (Low V_{in})	21	–	–	3.0	–	mA
Input Threshold Voltage – Carrier Detect Input Voltage Referenced to V_{EE} = –3.0 Vdc	20	–	0.9	1.2	1.4	Vdc

Figure 1. Test Circuit



NOTES: 1. TR 1 Coilcraft 1:4 impedance transformer.
2. V_{CC} is DC Ground.
3. 1.5 µH variable shielded inductor:
Toko Part # 292SNS–T1373 or Equivalent.

Figure 2. Total Drain Current versus Supply Voltage and Temperature

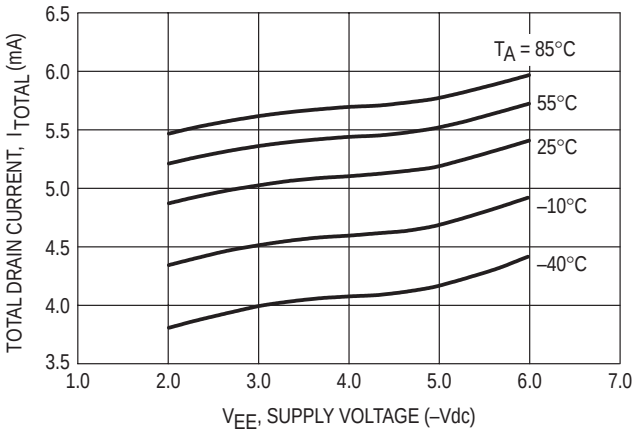


Figure 3. Drain Currents versus Supply Voltage

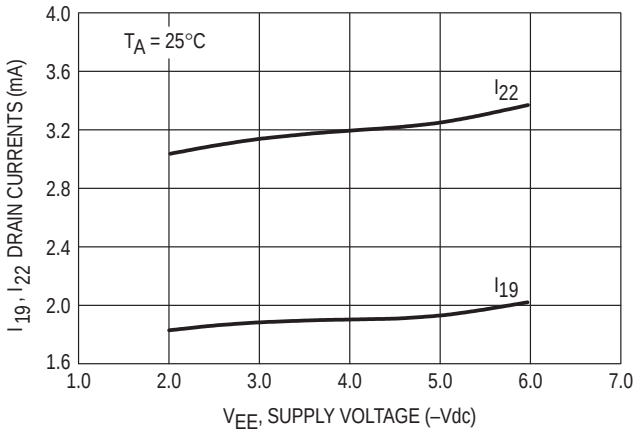


Figure 4. Mixer Gain versus Input Signal Level

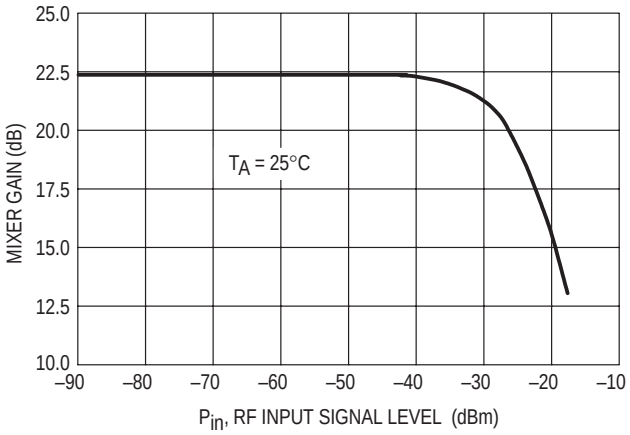


Figure 5. IF Amplifier Gain versus Input Signal Level and Ambient Temperature

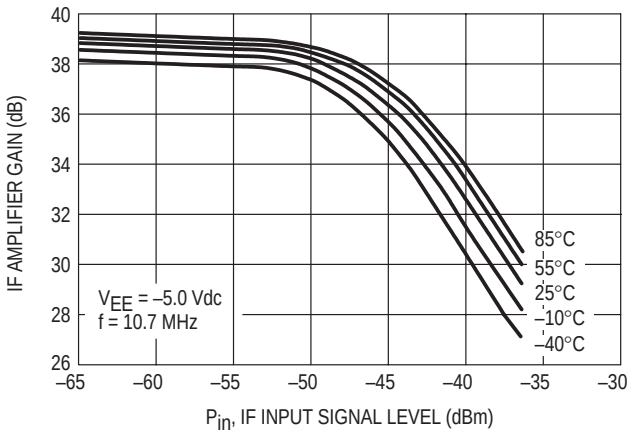


Figure 6. IF Amplifier RSSI Output Current versus Input Signal Level and Ambient Temperature

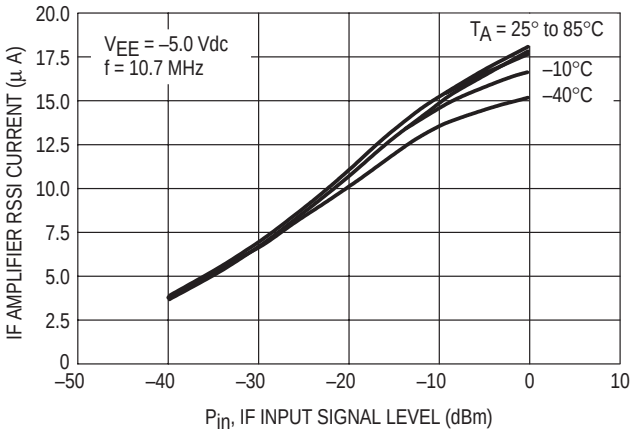


Figure 7. Limiter Amplifier RSSI Output Current versus Input Signal Level and Temperature

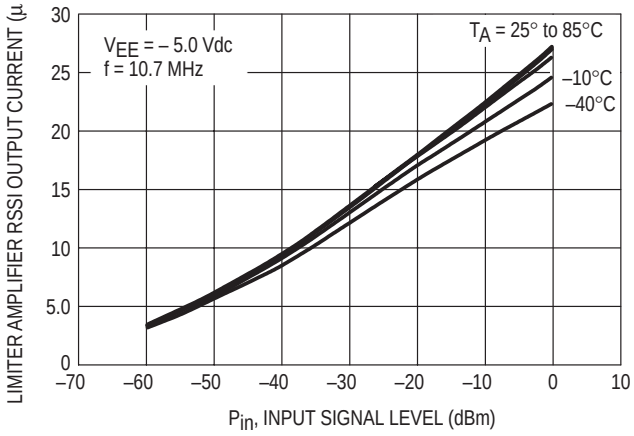
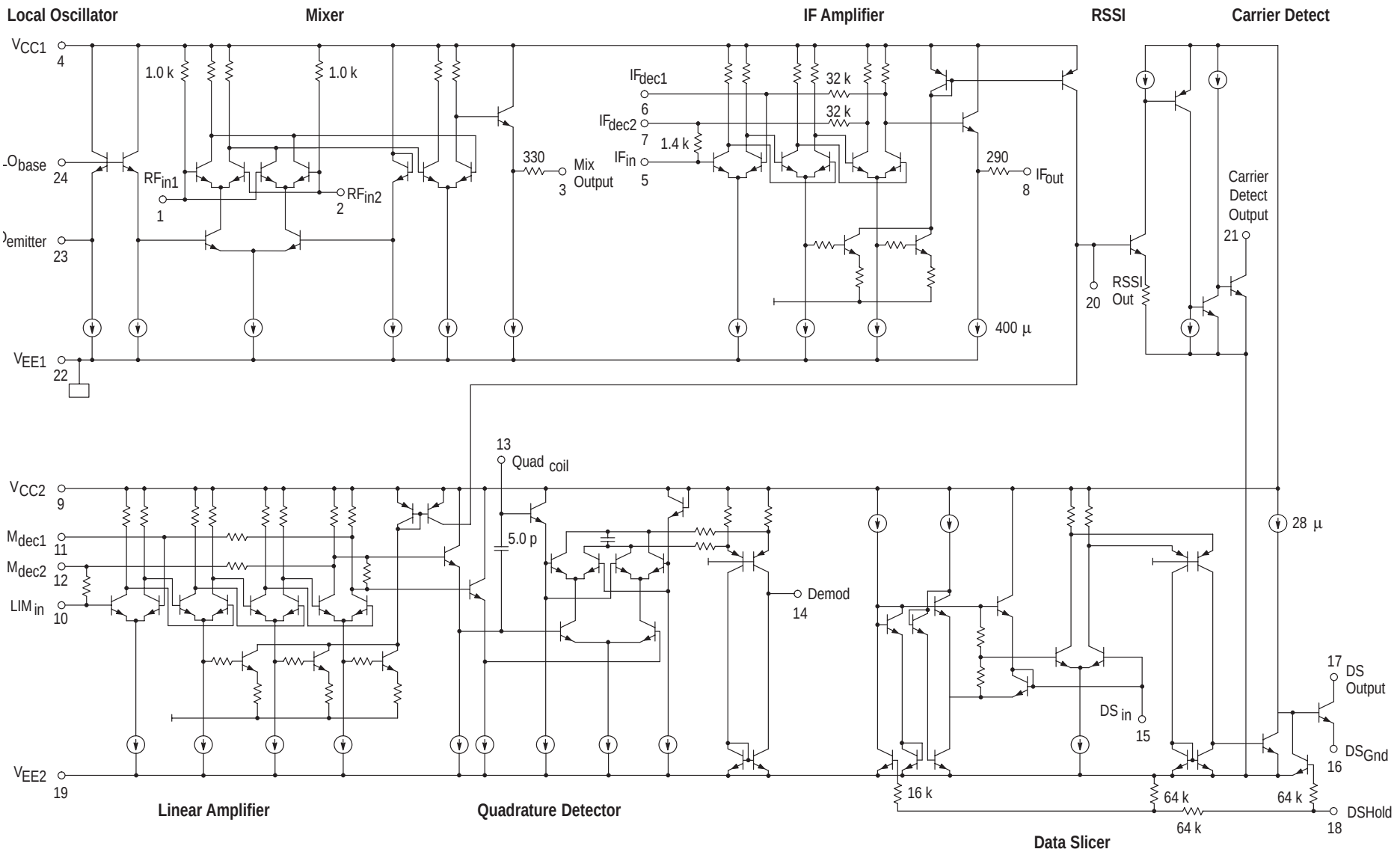


Figure 8. MC13156DW Internal Circuit Schematic



CIRCUIT DESCRIPTION

General

The MC13156 is a low power single conversion wideband FM receiver incorporating a split IF. This device is designated for use as the backend in digital FM systems such as CT–2 and wideband data links with data rates up to 500 kbaud. It contains a mixer, oscillator, signal strength meter drive, IF amplifier, limiting IF, quadrature detector and a data slicer with a hold function (refer to Figure 8, Simplified Internal Circuit Schematic).

Current Regulation

Temperature compensating voltage independent current regulators are used throughout.

Mixer

The mixer is a double–balanced four quadrant multiplier and is designed to work up to 500 MHz. It can be used in differential or in single–ended mode by connecting the other input to the positive supply rail.

Figure 4 shows the mixer gain and saturated output response as a function of input signal drive. The circuit used to measure this is shown in Figure 1. The linear gain of the mixer is approximately 22 dB. Figure 9 shows the mixer gain versus the IF output frequency with the local oscillator of 150 MHz at 100 mVrms LO drive level. The RF frequency is swept. The sensitivity of the IF output of the mixer is shown in Figure 10 for an RF input drive of 10 mVrms at 140 MHz and IF at 10 MHz.

The single–ended parallel equivalent input impedance of the mixer is Rp ~ 1.0 kΩ and Cp ~ 4.0 pF (see Table 1 for details). The buffered output of the mixer is internally loaded resulting in an output impedance of 330 Ω.

Local Oscillator

The on–chip transistor operates with crystal and LC resonant elements up to 220 MHz. Series resonant, overtone crystals are used to achieve excellent local oscillator stability. 3rd overtone crystals are used through about 65 to 70 MHz. Operation from 70 MHz up to 180 MHz is feasible using the on–chip transistor with a 5th or 7th overtone crystal. To enhance operation using an overtone crystal, the internal transistor's bias is increased by adding an external resistor from Pin 23 to V_{EE}. –10 dBm of local oscillator drive is needed to adequately drive the mixer (Figure 10).

The oscillator configurations specified above, and two others using an external transistor, are described in the application section:

1) A 133 MHz oscillator multiplier using a 3rd overtone crystal, and
2) A 307.8 to 309.3 MHz manually tuned, varactor controlled local oscillator.

RSSI

The Received Signal Strength Indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the IF and limiting amplifier stages. An external resistor at Pin 20 sets the voltage range or swing of the RSSI output voltage. Linearity of the RSSI is optimized by using external ceramic or crystal bandpass filters which have an insertion loss of 8.0 dB. The RSSI circuit is designed to provide 70+ dB of dynamic range with temperature compensation (see Figures 6 and 7 which show RSSI responses of the IF and Limiter amplifiers). Variation in the RSSI output current with supply voltage is small (see Figure 11).

Carrier Detect

When the meter current flowing through the meter load resistance reaches 1.2 Vdc above ground, the comparator flips, causing the carrier detect output to go high. Hysteresis can be accomplished by adding a very large resistor for positive feedback between the output and the input of the comparator.

IF Amplifier

The first IF amplifier section is composed of three differential stages with the second and third stages contributing to the RSSI. This section has internal dc feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 39 dB at 10.7 MHz. Figure 5 shows the gain and saturated output response of the IF amplifier over temperature, while Figure 12 shows the IF amplifier gain as a function of the IF frequency.

The fixed internal input impedance is 1.4 kΩ. It is designed for applications where a 455 kHz ceramic filter is used and no external output matching is necessary since the filter requires a 1.4 kΩ source and load impedance.

For 10.7 MHz ceramic filter applications, an external 430 Ω resistor must be added in parallel to provide the equivalent load impedance of 330 Ω that is required by the filter; however, no external matching is necessary at the input since the mixer output matches the 330 Ω source impedance of the filter. For 455 kHz applications, an external 1.1 kΩ resistor must be added in series with the mixer output to obtain the required matching impedance of 1.4 kΩ of the filter input resistance. Overall RSSI linearity is dependent on having total midband attenuation of 12 dB (6.0 dB insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the IF amplifier is buffered and the impedance is 290 Ω.

Limiter

The limiter section is similar to the IF amplifier section except that four stages are used with the last three contributing to the RSSI. The fixed internal input impedance is 1.4 kΩ. The total gain of the limiting amplifier section is approximately 55 dB. This IF limiting amplifier section internally drives the quadrature detector section.

Figure 9. Mixer Gain versus IF Frequency

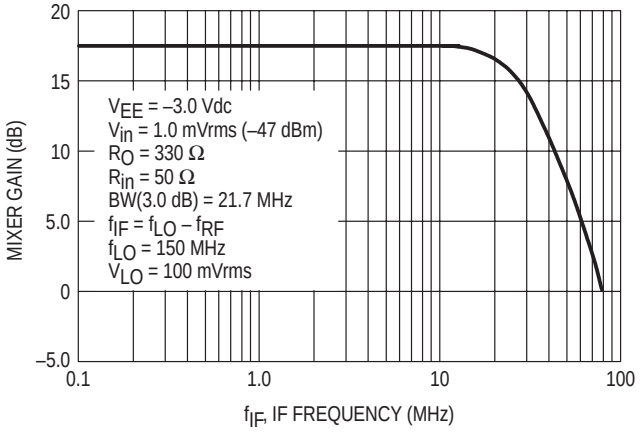


Figure 10. Mixer IF Output Level versus Local Oscillator Input Level

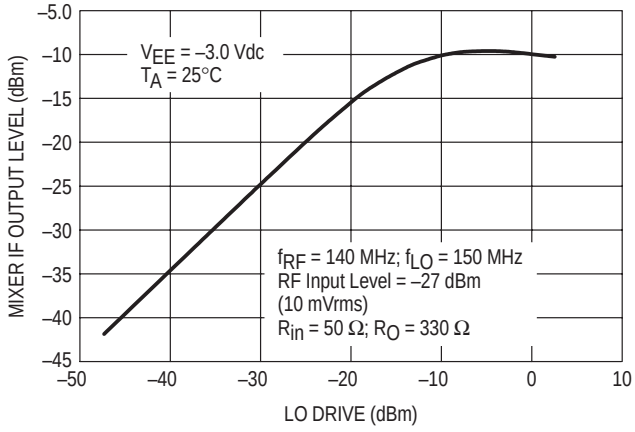


Figure 11. RSSI Output Current versus Supply Voltage and RF Input Signal Level

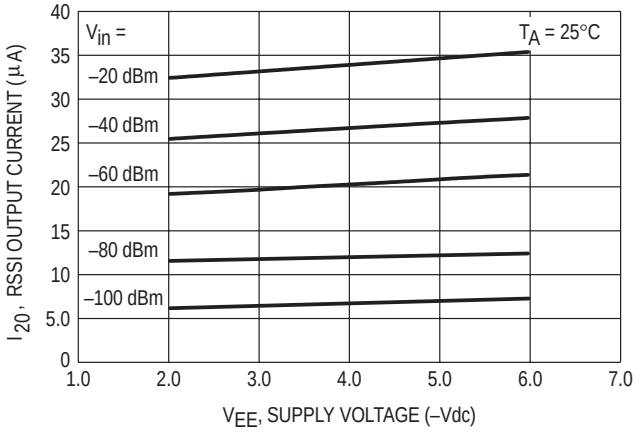


Figure 12. IF Amplifier Gain versus IF Frequency

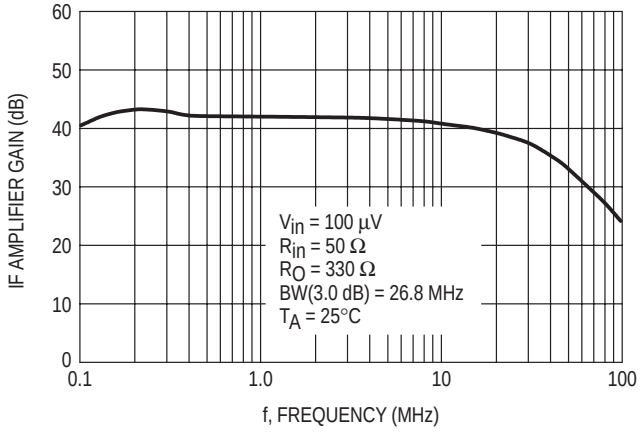
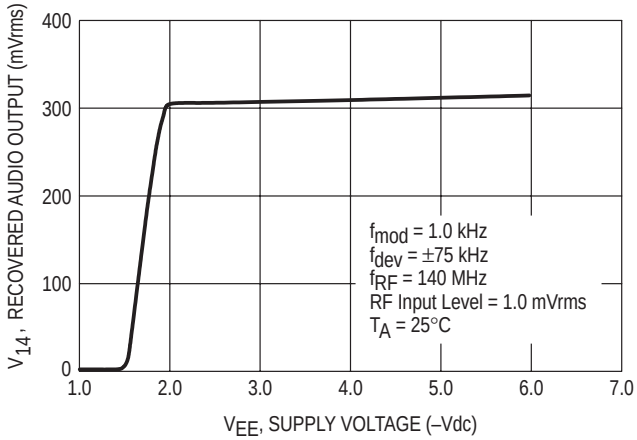


Figure 13. Recovered Audio Output Voltage versus Supply Voltage



Quadrature Detector

The quadrature detector is a doubly balanced four quadrant multiplier with an internal 5.0 pF quadrature capacitor to couple the IF signal to the external parallel RLC resonant circuit that provides the 90 degree phase shift and drives the quadrature detector. A single pin (Pin 13) provides for the external LC parallel resonant network and the internal connection to the quadrature detector.

The bandwidth of the detector allows for recovery of relatively high data rate modulation. The recovered signal is converted from differential to single ended through a push–pull NPN/PNP output stage. Variation in recovered audio output voltage with supply voltage is very small (see Figure 13). The output drive capability is approximately ±9.0 μA for a frequency deviation of ±75 kHz and 1.0 kHz modulating frequency (see Application Circuit).

Data Slicer

The data slicer input (Pin 15) is self centering around 1.1 V with clamping occurring at $1.1 \pm 0.5\ V_{be}$ Vdc. It is designed to square up the data signal. Figure 14 shows a detailed schematic of the data slicer.

The Voltage Regulator sets up 1.1 Vdc on the base of Q12, the Differential Input Amplifier. There is a potential of 1.0 V_{be} on the base–collector of transistor diode Q11 and 2.0 V_{be} on the base–collector of Q10. This sets up a 1.5 V_{be} (~ 1.1 Vdc) on the node between the 36 kΩ resistors which is connected to the base of Q12. The differential output of the data slicer Q12 and Q13 is converted to a single–ended output by the Driver Circuit. Additional circuitry, not shown in Figure 14, tends to keep the data slicer input centered at 1.1 Vdc as input signal levels vary.

The Input Diode Clamp Circuit provides the clamping at 1.0 V_{be} (0.75 Vdc) and 2.0 V_{be} (1.45 Vdc). Transistor diodes Q7 and Q8 are on, thus, providing a 2.0 V_{be} potential at the base of Q1. Also, the voltage regulator circuit provides a potential of 2.0 Vbe on the base of Q3 and 1.0 V_{be} on the emitter of Q3 and Q2. When the data slicer input (Pin 15) is pulled up, Q1 turns off; Q2 turns on, thereby clamping the input at 2.0 V_{be}. On the other hand, when Pin 15 is pulled down, Q1 turns on; Q2 turns off, thereby clamping the input at 1.0 V_{be}.

The recovered data signal from the quadrature detector is ac coupled to the data slicer via an input coupling capacitor. The size of this capacitor and the nature of the data signal determine how faithfully the data slicer shapes up the recovered signal. The time constant is short for large peak to peak voltage swings or when there is a change in dc level at the detector output. For small signal or for continuous bits of the same polarity which drift close to the threshold voltage, the time constant is longer. When centered there is no input current allowed, which is to say, that the input looks high in impedance.

Another unique feature of the data slicer is that it responds to various logic levels applied to the Data Slicer Hold Control pin (Pin 18). Figure 15 illustrates how the input and output currents under “no hold” condition relate to the input voltage. Figure 16 shows how the input current and input voltage relate for both the “no hold” and “hold” condition.

The hold control (Pin18) does three separate tasks:

1) With Pin 18 at 1.0 V_{be} or greater, the output is shut off (sets high). Q19 turns on which shunts the base drive from Q20, thereby turning the output off.
2) With Pin 18 at 2.0 V_{be} or greater, internal clamping diodes are open circuited and the comparator input is shut off and effectively open circuited. This is accomplished by turning off the current source to emitters of the input differential amplifier, thus, the input differential amplifier is shut off.
3) When the input is shut off, it allows the input capacitor to hold its charge during transmit to improve recovery at the beginning of the next receive period. When it is turned on, it allows for very fast charging of the input capacitor for quick recovery of new tuning or data average. The above features are very desirable in a TDD digital FM system.

Figure 14. Data Slicer Circuit

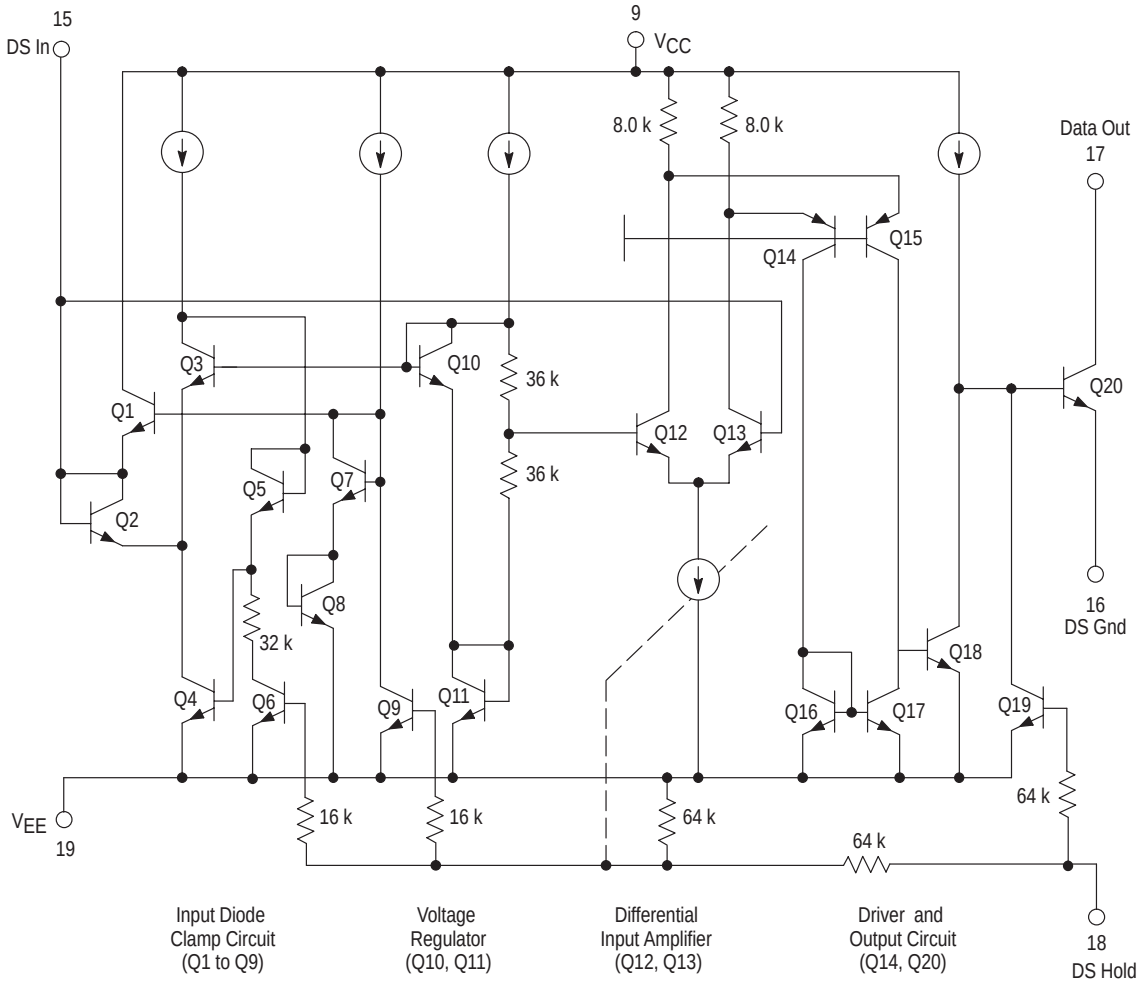


Figure 15. Data Slicer Input/Output Currents versus Input Voltage

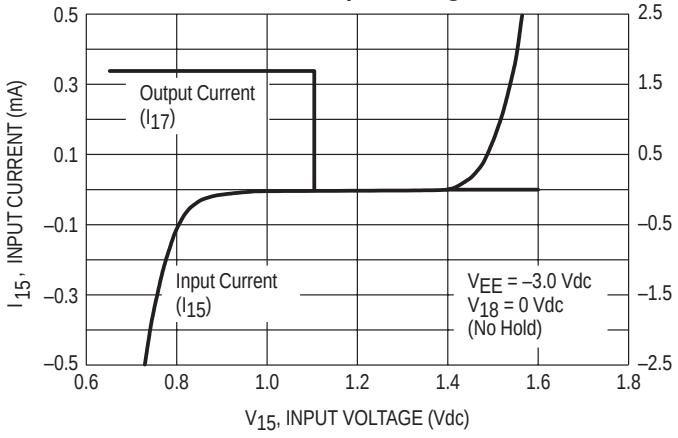


Figure 16. Data Slicer Input Current versus Input Voltage

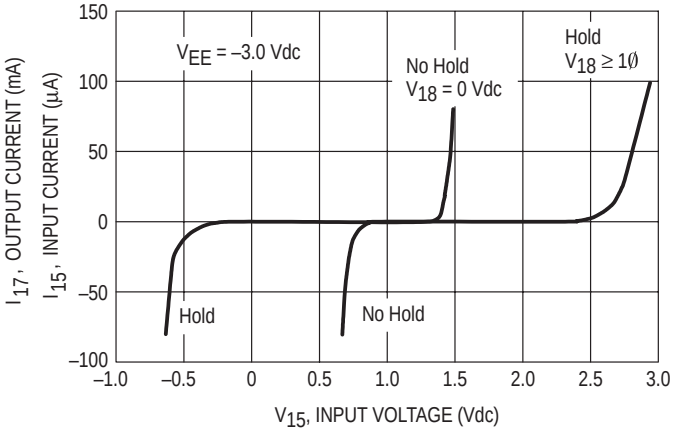
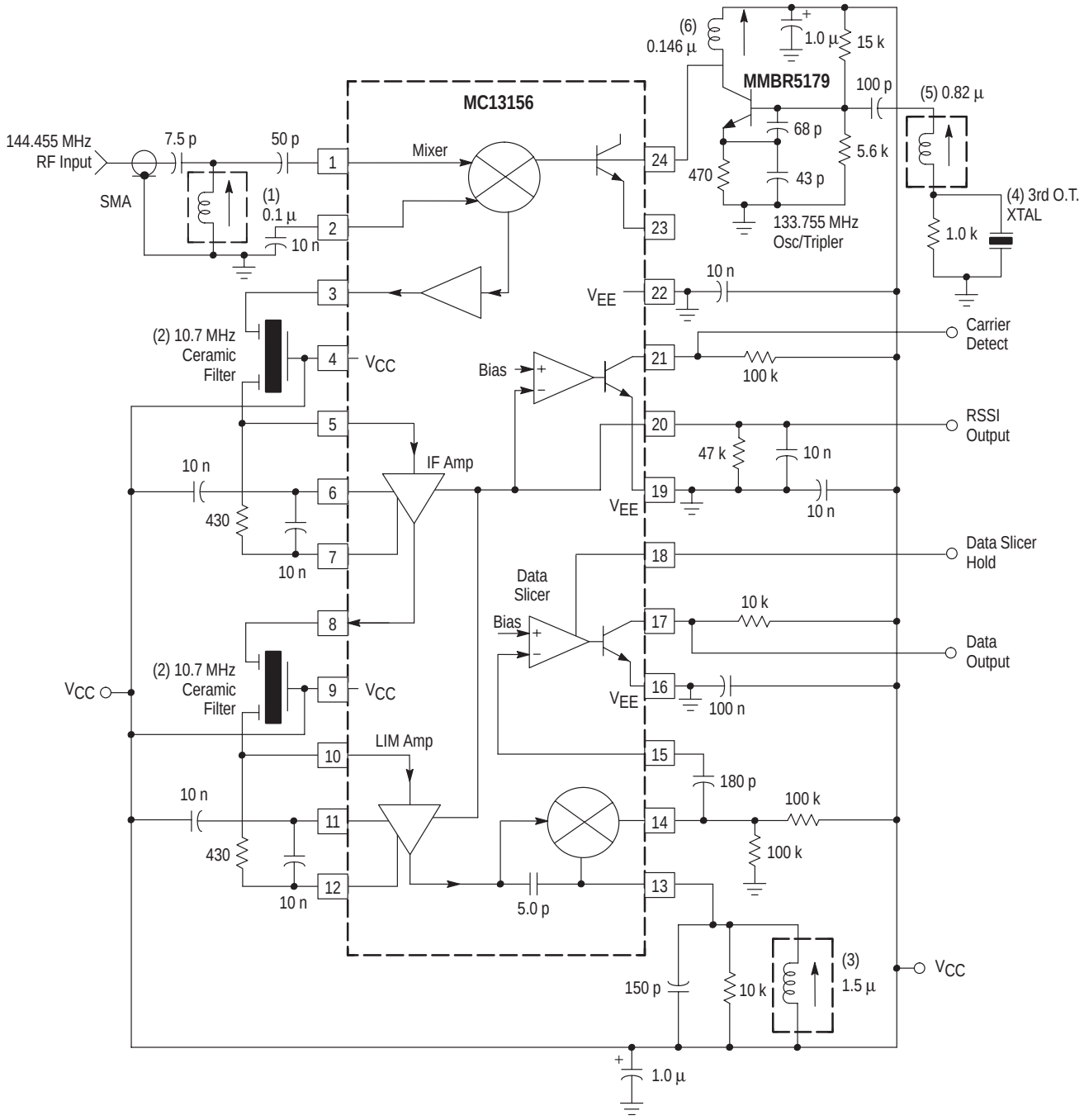


Figure 17. MC13156DW Application Circuit



NOTES: 1. 0.1 µH Variable Shielded Inductor: Coilcraft part # M1283–A or equivalent.
2. 10.7 MHz Ceramic Filter: Toko part # SK107M5–A0–10X or Murata Erie part # SFE10.7MHY–A.
3. 1.5 µH Variable Shielded Inductor: Toko part # 292SNS–T1373.
4. 3rd Overtone, Series Resonant, 25 PPM Crystal at 44.585 MHz.
5. 0.814 µH Variable Shielded Inductor: Coilcraft part # 143–18J12S.
6. 0.146 µH Variable Inductor: Coilcraft part # 146–04J08.

Figure 18. MC13156DW Circuit Side Component Placement

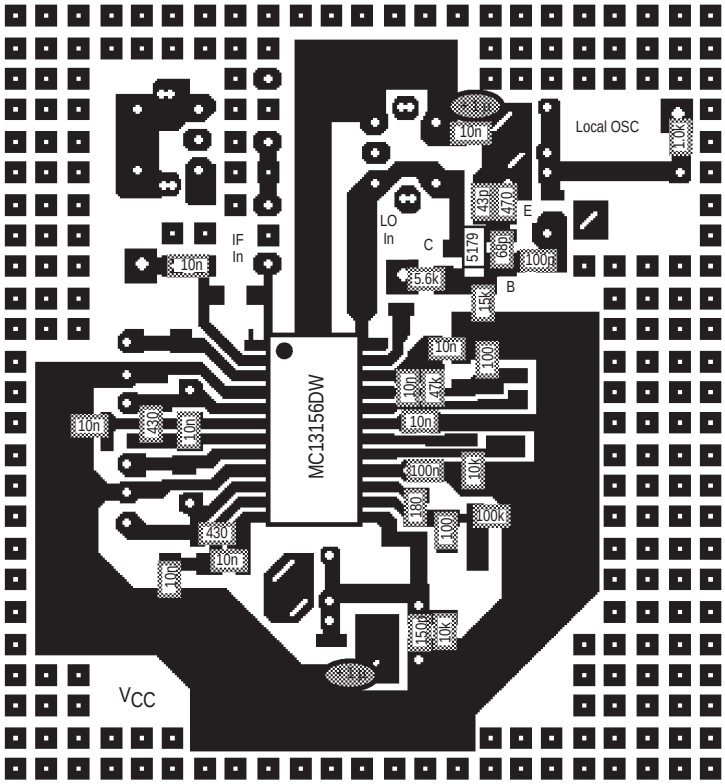
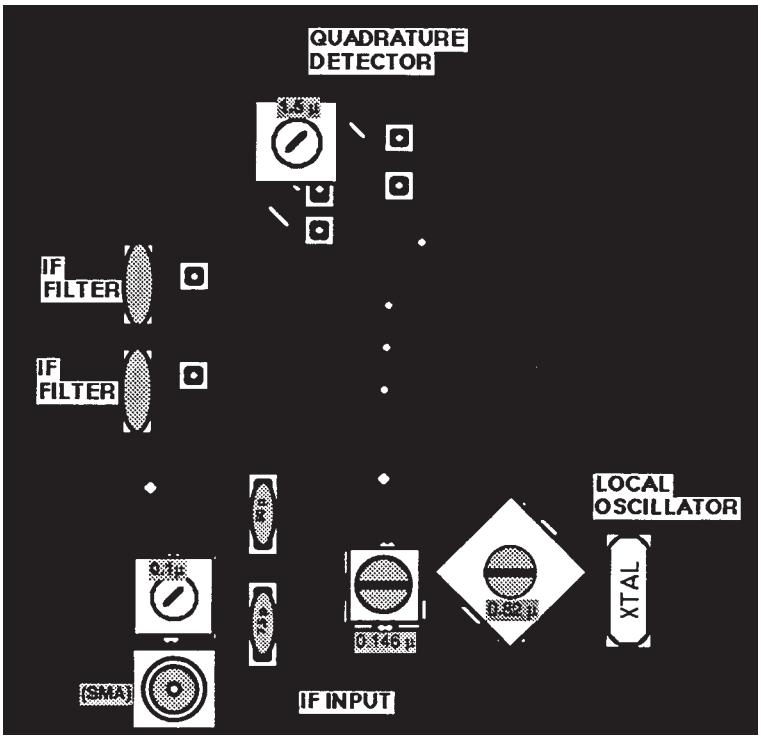


Figure 19. MC13156DW Ground Side Component Placement



APPLICATIONS INFORMATION

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. Figures 18 and 19 show the placement for the components specified in the application circuit (Figure 17). The applications circuit schematic specifies particular components that were used to achieve the results shown in the typical curves and tables but equivalent components should give similar results.

Input Matching Networks/Components

The input matching circuit shown in the application circuit schematic is passive high pass network which offers effective image rejection when the local oscillator is below the RF input frequency. Silver mica capacitors are used for their high Q and tight tolerance. The PC board is not dedicated to any particular input matching network topology; space is provided for the designer to breadboard as desired.

Alternate matching networks using 4:1 surface mount transformers or BALUNs provide satisfactory performance. The 12 dB SINAD sensitivity using the above matching networks is typically –100 dBm for f_{mod} = 1.0 kHz and f_{dev} = ±75 kHz at f_{IN} = 144.45 MHz and f_{OSC} = 133.75 MHz (see Figure 25).

It is desirable to use a SAW filter before the mixer to provide additional selectivity and adjacent channel rejection and improved sensitivity. The SAW filter should be designed to interface with the mixer input impedance of approximately 1.0 kΩ. Table 1 displays the series equivalent single–ended mixer input impedance.

Local Oscillators

VHF Applications – The local oscillator circuit shown in the application schematic utilizes a third overtone crystal and an RF transistor. Selecting a transistor having good phase noise performance is important; a mandatory criteria is for the device to have good linearity of beta over several decades of collector current. In other words, if the low current beta is suppressed, it will not offer good 1/f noise performance. A third overtone series resonant crystal having at least 25 ppm tolerance over the operating temperature is recommended. The local oscillator is an impedance inversion third overtone Colpitts network and harmonic generator. In this circuit a 560 to 1.0 kΩ resistor shunts the crystal to ensure that it operates in its overtone mode; thus, a blocking capacitor is needed to eliminate the dc path to ground. The resulting parallel LC network should “free–run” near the crystal frequency if a short to ground is placed across the crystal. To provide sufficient output loading at the collector, a high Q variable inductor is used that is tuned to self resonate at the 3rd harmonic of the overtone crystal frequency.

The on–chip grounded collector transistor may be used for HF and VHF local oscillator with higher order overtone crystals. Figure 20 shows a 5th overtone oscillator at 93.3 MHz and Figure 21 shows a 7th overtone oscillator at 148.3 MHz. Both circuits use a Butler overtone oscillator configuration. The amplifier is an emitter follower. The crystal is driven from the emitter and is coupled to the high impedance base through a capacitive tap network. Operation at the desired overtone frequency is ensured by the parallel resonant circuit formed by the variable inductor and the tap capacitors and parasitic capacitances of the on–chip transistor and PC board. The variable inductor specified in the schematic could be replaced with a high tolerance, high Q ceramic or air wound surface mount component if the other components have good tolerances. A variable inductor provides an adjustment for gain and frequency of the resonant tank ensuring lock up and startup of the crystal oscillator. The overtone crystal is chosen with ESR of typically 80 Ω and 120 Ω maximum; if the resistive loss in the crystal is too high, the performance of the oscillator may be impacted by lower gain margins.

Table 1. Mixer Input Impedance Data
(Single–ended configuration, V_{CC} = 3.0 Vdc, local oscillator drive = 100 mVrms)

Frequency (MHz)	Series Equivalent Complex Impedance (R + jX) (Ω)	Parallel Resistance Rp (Ω)	Parallel Capacitance Cp (pF)
90	190 – j380	950	4.7
100	160 – j360	970	4.4
110	130 – j340	1020	4.2
120	110 – j320	1040	4.2
130	97 – j300	1030	4.0
140	82 – j280	1040	4.0
150	71 – j270	1100	4.0
160	59 – j260	1200	3.9
170	52 – j240	1160	3.9
180	44 – j230	1250	3.8
190	38 – j220	1300	3.8

A series LC network to ground (which is V_{CC}) is comprised of the inductance of the base lead of the on–chip transistor and PC board traces and tap capacitors. Parasitic oscillations often occur in the 200 to 800 MHz range. A small resistor is placed in series with the base (Pin 24) to cancel the negative resistance associated with this undesired mode of oscillation. Since the base input impedance is so large a small resistor in the range of 27 to 68 Ω has very little effect on the desired Butler mode of oscillation.

The crystal parallel capacitance, C_O, provides a feedback path that is low enough in reactance at frequencies of 5th overtone or higher to cause trouble. C_O has little effect near resonance because of the low impedance of the crystal motional arm (R_m–L_m–C_m). As the tunable inductor which forms the resonant tank with the tap capacitors is tuned off the crystal resonant frequency, it may be difficult to tell if the oscillation is under crystal control. Frequency jumps may occur as the inductor is tuned. In order to eliminate this behavior an inductor (L_O) is placed in parallel with the crystal. L_O is chosen to resonant with the crystal parallel capacitance (C_O) at the desired operation frequency. The inductor provides a feedback path at frequencies well below resonance; however, the parallel tank network of the tap capacitors and tunable inductor prevent oscillation at these frequencies.

UHF Application

Figure 22 shows a 318.5 to 320 MHz receiver which drives the mixer with an external varactor controlled (307.8 to 309.3 MHz) LC oscillator using an MPS901 (RF low power transistor in a TO–92 plastic package; also MMBR901 is available in a SOT–23 surface mount package). With the 50 kΩ 10 turn potentiometer this oscillator is tunable over a range of approximately 1.5 MHz. The MMBV909L is a low voltage varactor suitable for UHF applications; it is a dual back–to–back varactor in a SOT–23 package. The input matching network uses a 1:4 impedance matching transformer (Recommended sources are Mini–Circuits and Coilcraft).

Using the same IF ceramic filters and quadrature detector circuit as specified in the applications circuit in Figure 17, the 12 dB SINAD performance is –95 dBm for a f_{mod} = 1.0 kHz sinusoidal waveform and f_{dev} ±40 kHz.

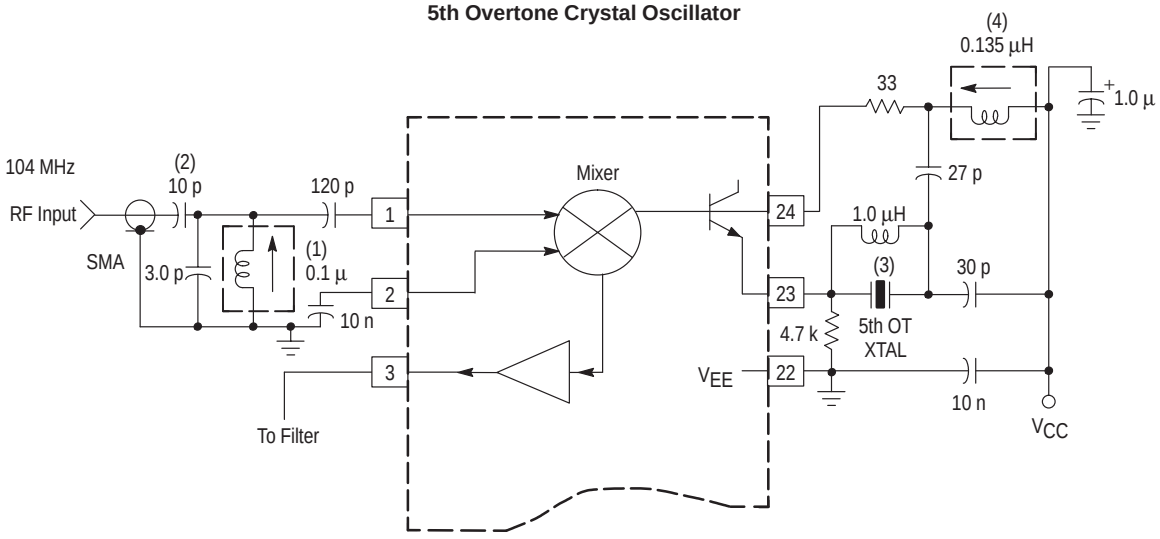
This circuit is breadboarded using the evaluation PC board shown in Figures 32 and 33. The RF ground is V_{CC} and path lengths are minimized. High quality surface mount components were used except where specified. The absolute values of the components used will vary with layout placement and component parasitics.

RSSI Response

Figure 26 shows the full RSSI response in the application circuit. The 10.7 MHz, 110 kHz wide bandpass ceramic filters (recommended sources are TOKO part # SK107M5–AO–10X or Murata Erie SFE10.7MHY–A) provide the correct bandpass insertion loss to linearize the curve between the limiter and IF portions of RSSI. Figure 25 shows that limiting occurs at an input of –100 dBm. As shown in Figure 26, the RSSI output linear from –100 dBm to –30 dBm.

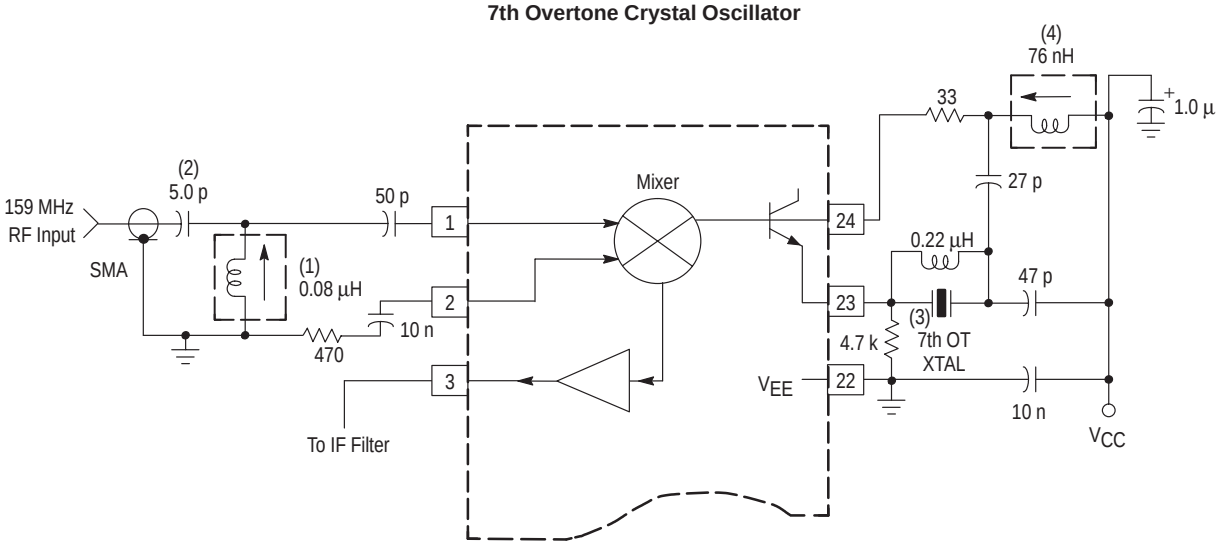
The RSSI rise and fall times for various RF input signal levels and R20 values are measured at Pin 20 without 10 nF filter capacitor. A 10 kHz square wave pulses the RF input signal on and off. Figure 27 shows that the rise and fall times are short enough to recover greater than 10 kHz ASK data; with a wider IF bandpass filters data rates up to 50 kHz may be achieved. The circuit used is the application circuit in Figure 17 with no RSSI output filter capacitor.

Figure 20. MC13156DW Application Circuit
f_{RF} = 104 MHz; f_{LO} = 93.30 MHz
5th Overtone Crystal Oscillator



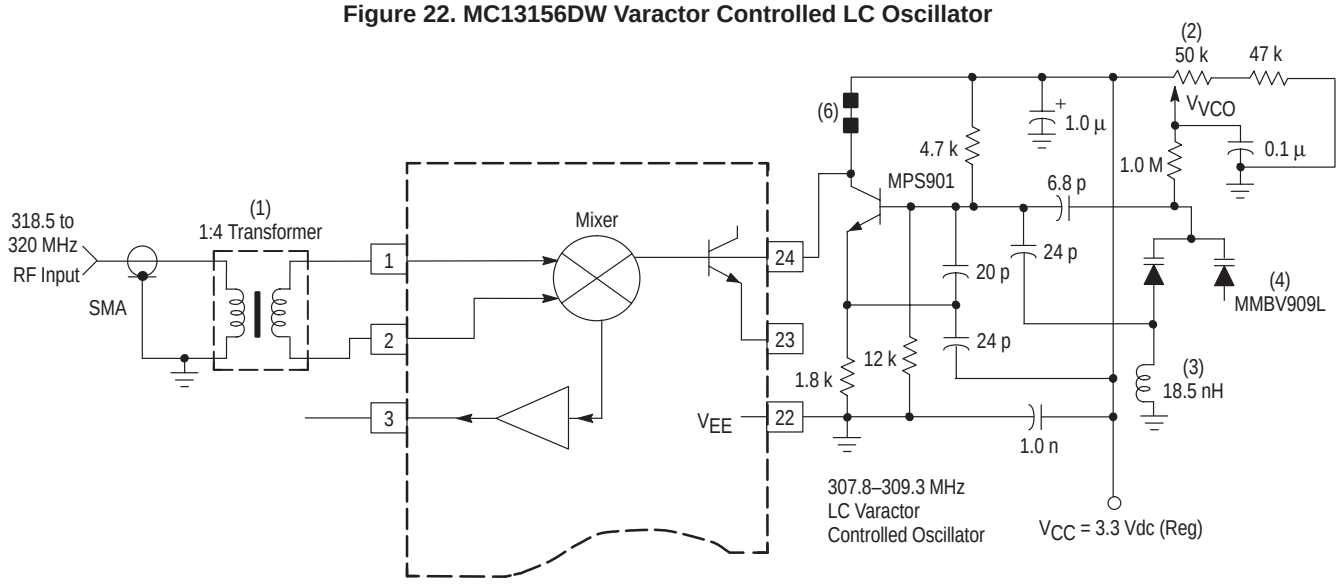
NOTES: 1. 0.1 µH Variable Shielded Inductor: Coilcraft part # M1283–A or equivalent.
2. Capacitors are Silver Mica.
3. 5th Overtone, Series Resonant, 25 PPM Crystal at 93.300 MHz.
4. 0.135 µH Variable Shielded Inductor: Coilcraft part # 146–05J08S or equivalent.

Figure 21. MC13156DW Application Circuit
f_{RF} = 159 MHz; f_{LO} = 148.30 MHz
7th Overtone Crystal Oscillator



NOTES: 1. 0.08 µH Variable Shielded Inductor: Toko part # 292SNS–T1365Z or equivalent.
2. Capacitors are Silver Mica.
3. 7th Overtone, Series Resonant, 25 PPM Crystal at 148.300 MHz.
4. 76 nH Variable Shielded Inductor: Coilcraft part # 150–03J08S or equivalent.

Figure 22. MC13156DW Varactor Controlled LC Oscillator



NOTES: 1. 1:4 Impedance Transformer: Mini–Circuits.
2. 50 k Potentiometer, 10 turns.
3. Spring Coil; Coilcraft A05T.
4. Dual Varactor in SOT–23 Package.
5. All other components are surface mount components.
6. Ferrite beads through loop of 24 AWG wire.

45 MHz Narrowband Receiver

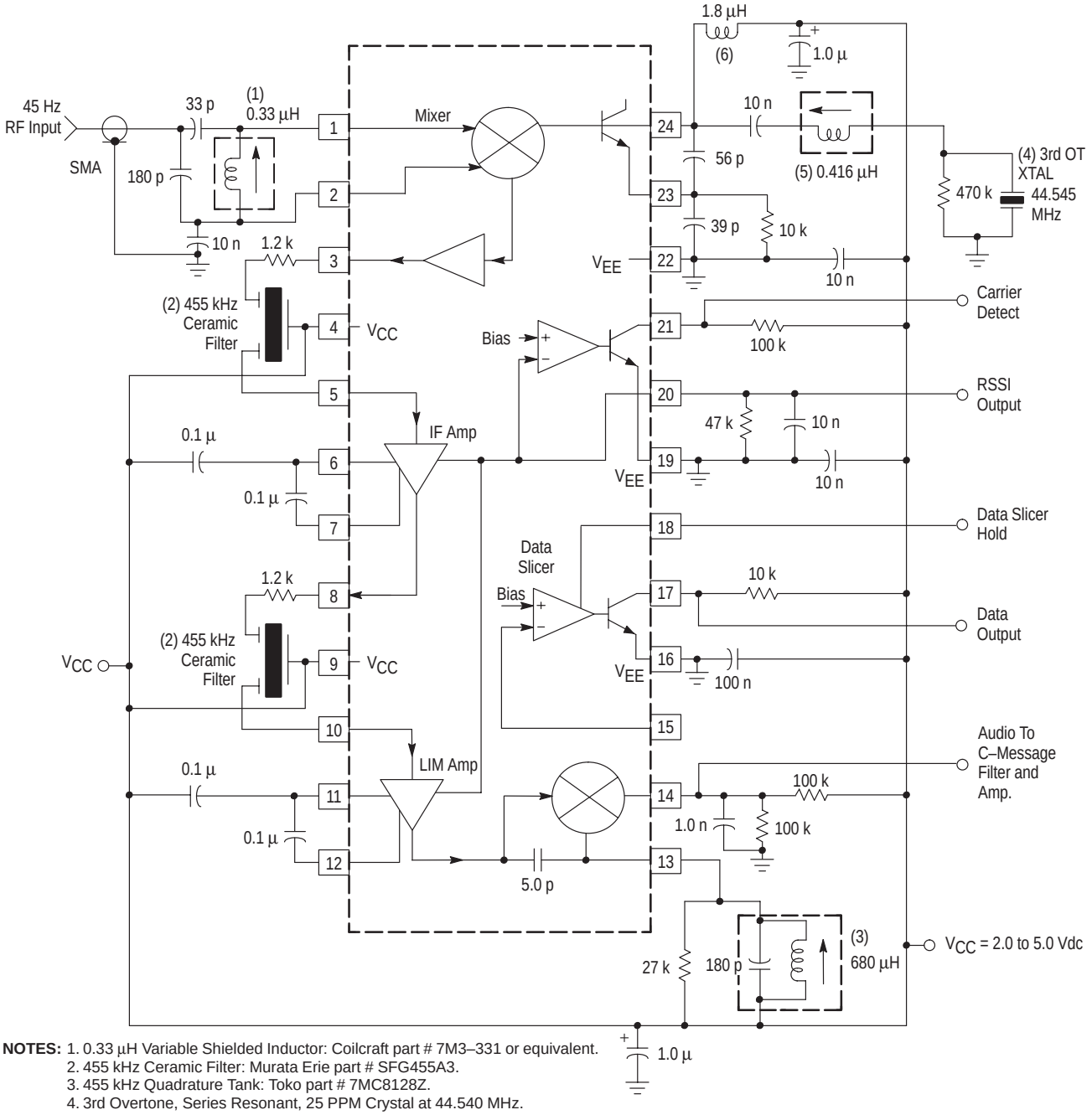
The above application examples utilize a 10.7 MHz IF. In this section a narrowband receiver with a 455 kHz IF will be described. Figure 23 shows a full schematic of a 45 MHz receiver that uses a 3rd overtone crystal with the on–chip oscillator transistor. The oscillator configuration is similar to the one used in Figure 17; it is called an impedance inversion Colpitts. A 44.545 MHz 3rd overtone, series resonant crystal is used to achieve an IF frequency at 455 kHz. The ceramic IF filters selected are Murata Erie part # SFG455A3. 1.2 kΩ chip resistors are used in series with the filters to achieve the terminating resistance of 1.4 kΩ to the filter. The IF decoupling is very important; 0.1 μF chip capacitors are used at Pins 6, 7, 11 and 12. The quadrature detector tank circuit uses a 455 kHz quadrature tank from Toko.

The 12 dB SINAD performance is –109 dBm for a f_{mod} = 1.0 kHz and a f_{dev} = ±4.0 kHz. The RSSI dynamic range is approximately 80 dB of linear range (see Figure 24).

Receiver Design Considerations

The curves of signal levels at various portions of the application receiver with respect to RF input level are shown in Figure 28. This information helps determine the network topology and gain blocks required ahead of the MC13156 to achieve the desired sensitivity and dynamic range of the receiver system. In the application circuit the input third order intercept (IP3) performance of the system is approximately –25 dBm (see Figure 29).

Figure 23. MC13156DW Application Circuit at 45 MHz



NOTES: 1. 0.33 μH Variable Shielded Inductor: Coilcraft part # 7M3–331 or equivalent.
2. 455 kHz Ceramic Filter: Murata Erie part # SFG455A3.
3. 455 kHz Quadrature Tank: Toko part # 7MC8128Z.
4. 3rd Overtone, Series Resonant, 25 PPM Crystal at 44.540 MHz.
5. 0.416 μH Variable Shielded Inductor: Coilcraft part # 143–10J12S.
6. 1.8 μH Molded Inductor.

Figure 24. RSSI Output Voltage versus Input Signal Level

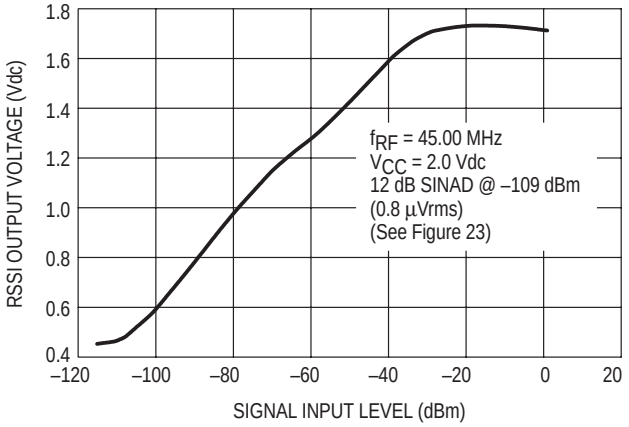


Figure 25. S + N/N versus RF Input Signal Level

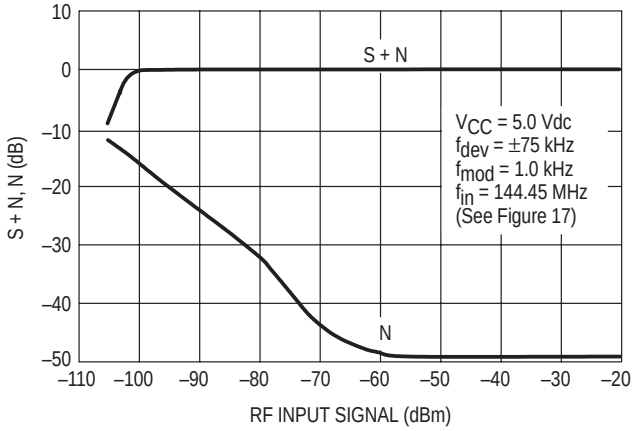


Figure 26. RSSI Output Voltage versus Input Signal Level

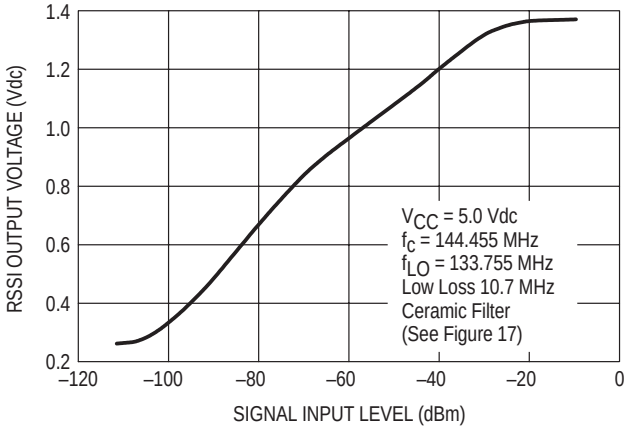


Figure 27. RSSI Output Rise and Fall Times versus RF Input Signal Level

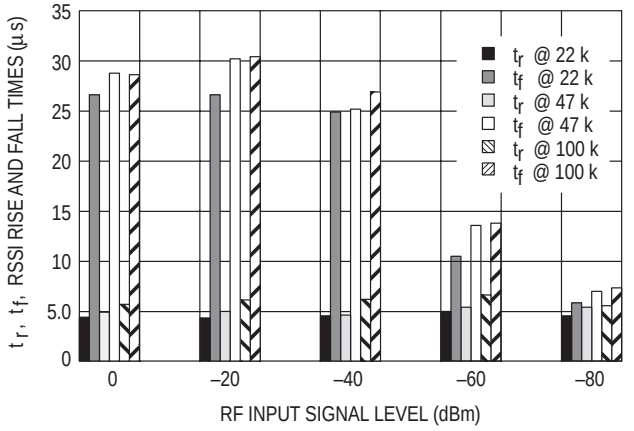


Figure 28. Signal Levels versus RF Input Signal Level

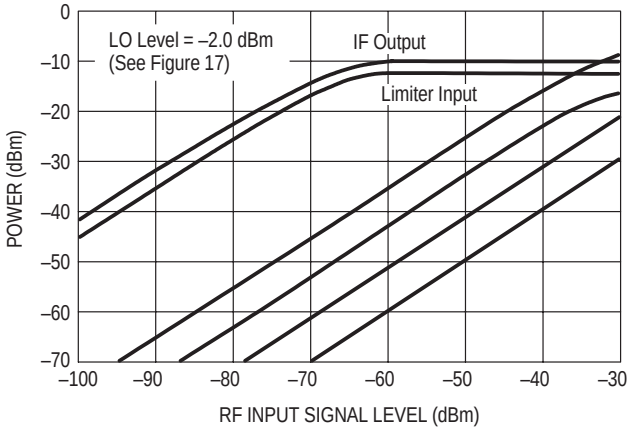
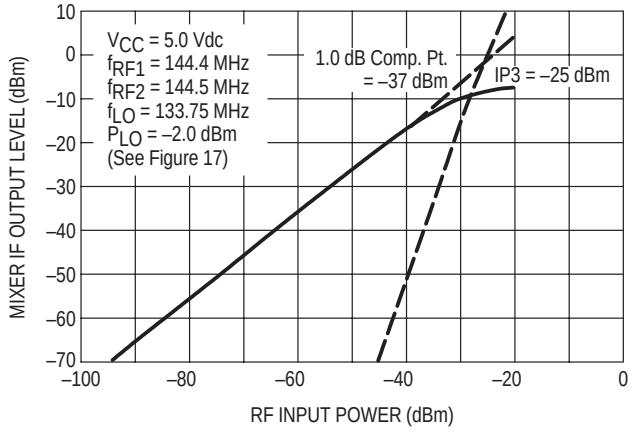


Figure 29. 1.0 dB Compression Pt. and Input Third Order Intercept Pt. versus Input Power



BER TESTING AND PERFORMANCE

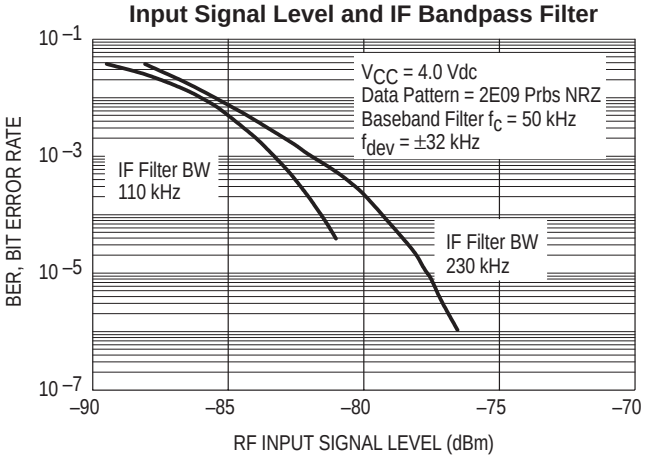
Description

The test setup shown in Figure 31 is configured so that the function generator supplies a 100 kHz clock source to the bit error rate tester. This device generates and receives a repeating data pattern and drives a 5 pole baseband data filter. The filter effectively reduces harmonic content of the baseband data which is used to modulate the RF generator which is running at 144.45 MHz. Following processing of the signal by the receiver (MC13156), the recovered baseband sinewave (data) is AC coupled to the data slicer. The data slicer is essentially an auto–threshold comparator which tracks the zero crossing of the incoming sinewave and provides logic level data at its ouput. Data errors associated with the recovered data are collected by the bit error rate receiver and displayed.

Bit error rate versus RF signal input level and IF filter bandwidth are shown in Figure 30. The bit error rate data was taken under the following test conditions:

- Data rate = 100 kbps
- Filter cutoff frequency set to 39% of the data rate or 39 kHz.
- Filter type is a 5 pole equal–ripple with 0.5° phase error.
- V_{CC} = 4.0 Vdc
- Frequency deviation = ±32 kHz.

Figure 30. Bit Error Rate versus RF Input Signal Level and IF Bandpass Filter



Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side (see Figures 32 and 33). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates.

Figure 31. Bit Error Rate Test Setup

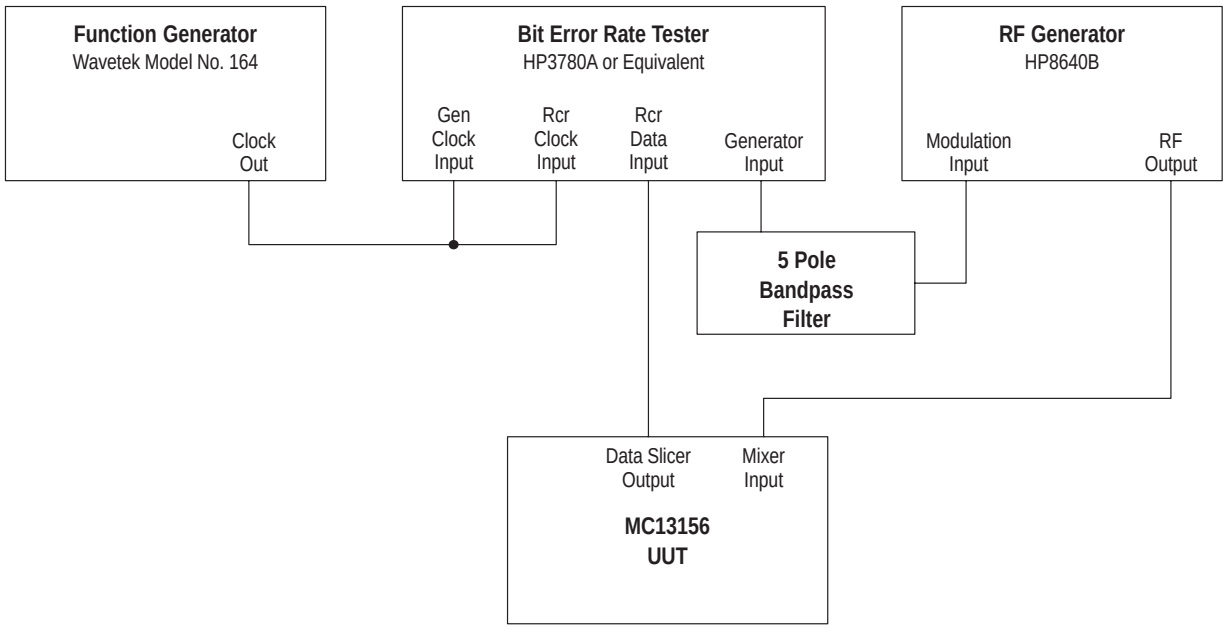


Figure 32. Circuit Side View

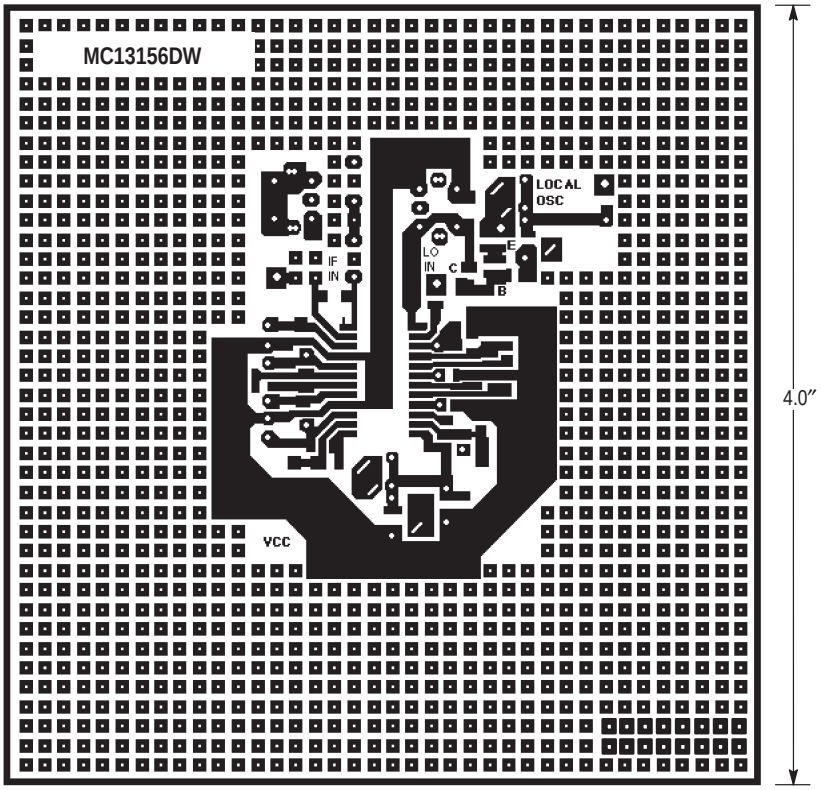
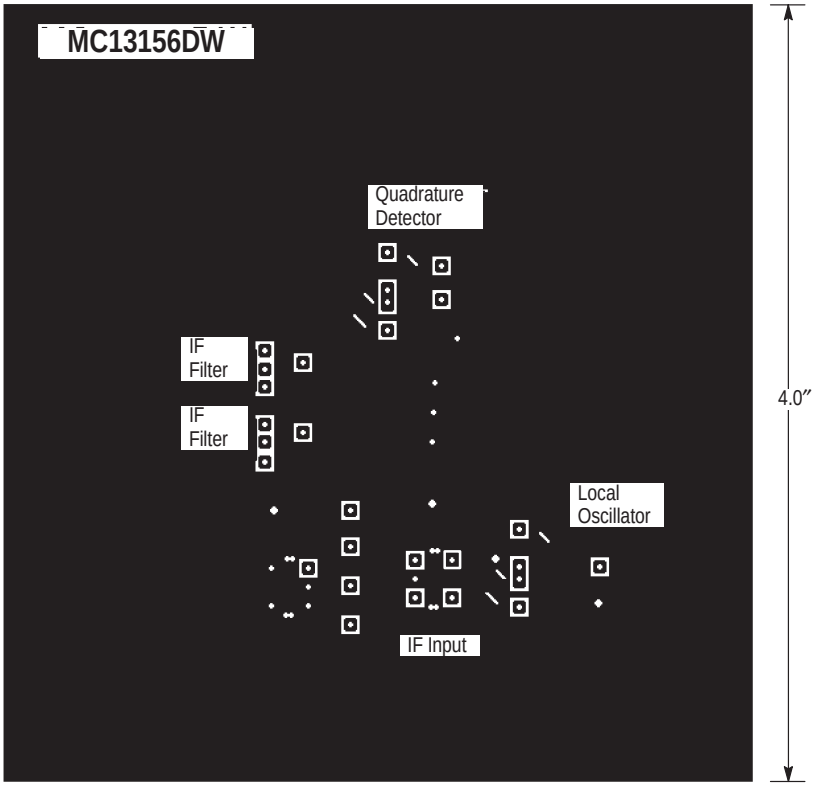


Figure 33. Ground Side View



MOTOROLA

MC13158

Wideband FM IF Subsystem

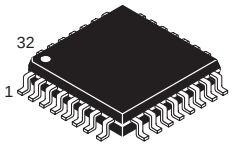
WIDEBAND FM IF SUBSYSTEM FOR DECT AND DIGITAL APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA

The MC13158 is a wideband IF subsystem that is designed for high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through the use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13158 has an on–board grounded collector VCO transistor that may be used with a fundamental or overtone crystal in single channel operation or with a PLL in multi–channel operation. The mixer is useful to 500 MHz and may be used in a balanced differential or single ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has an Off function to shut the output off to save current. An enable control is provided to power down the IC for power management in battery operated applications.

Applications include DECT, wideband wireless data links for personal and portable laptop computers and other battery operated radio systems which utilize GFSK, FSK or FM modulation.

- Designed for DECT Applications
- 1.8 to 6.0 Vdc Operating Voltage
- Low Power Consumption in Active and Standby Mode
- Greater than 600 kHz Detector Bandwidth
- Data Slicer with Special Off Function
- Enable Function for Power Down of Battery Operated Systems
- RSSI Dynamic Range of 80 dB Minimum
- Low External Component Count

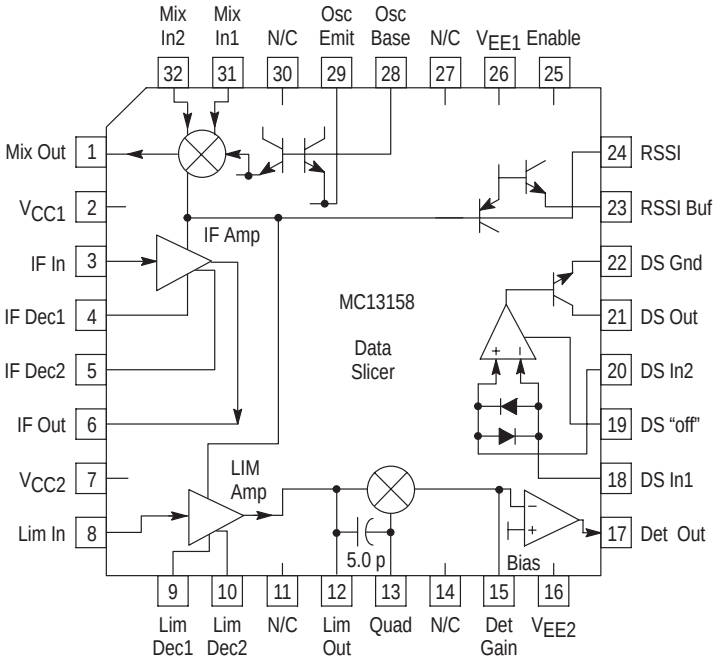


FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(Thin QFP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13158FTB	T_A = – 40 to +85°C	TQFP–32

Representative Block Diagram



This device contains 234 active transistors.

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	16, 26	$V_{S(max)}$	6.5	Vdc
Junction Temperature		T_{JMAX}	+150	°C
Storage Temperature Range		T_{stg}	–65 to +150	°C

NOTE: 1. Devices should not be operated at or outside these values. The "Recommended Operating Conditions" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS ($V_{CC} = V_2 = V_7$; $V_{EE} = V_{16} = V_{22} = V_{26}$; $V_S = V_{CC} - V_{EE}$)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage T_A = 25°C –40°C ≤ T_A ≤ 85°C	2, 7 16, 26	V_S	2.0 to 6.0	Vdc
Input Frequency	31, 32	F_{in}	10 to 500	MHz
Ambient Temperature Range		T_A	–40 to +85	°C
Input Signal Level	31, 32	V_{in}	200	mVrms

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_S = 3.0 Vdc; No Input Signal; See Figure 1.)

Characteristic	Condition	Pin	Symbol	Min	Typ	Max	Unit
Total Drain Current	V_S = 2.0 Vdc V_S = 3.0 Vdc V_S = 6.0 Vdc See Figure 2	16, 26	I_{TOTAL}	2.5 3.5 3.5	5.5 5.7 6.0	8.5 8.5 9.5	mA
DATA SLICER (Input Voltage Referenced to V_{EE}; V_S = 3.0 Vdc; No Input Signal)							
Output Current; V_{18} LO; Data Slicer Enabled (DS "on")	$V_{19} = V_{EE}$ $V_{18} < V_{20}$ $V_{20} = V_S/2$ See Figure 3	21	I_{21}	2.0	5.9	–	mA
Output Current; V_{18} HI; Data Slicer Enabled (DS "on")	$V_{19} = V_{EE}$ $V_{18} > V_{20}$ $V_{20} = V_S/2$ See Figure 4	21	I_{21}	–	0.1	1.0	μA
Output Current; Data Slicer Disabled (DS "off")	$V_{19} = V_{CC}$ $V_{20} = V_S/2$	21	I_{21}	–	0.1	1.0	μA

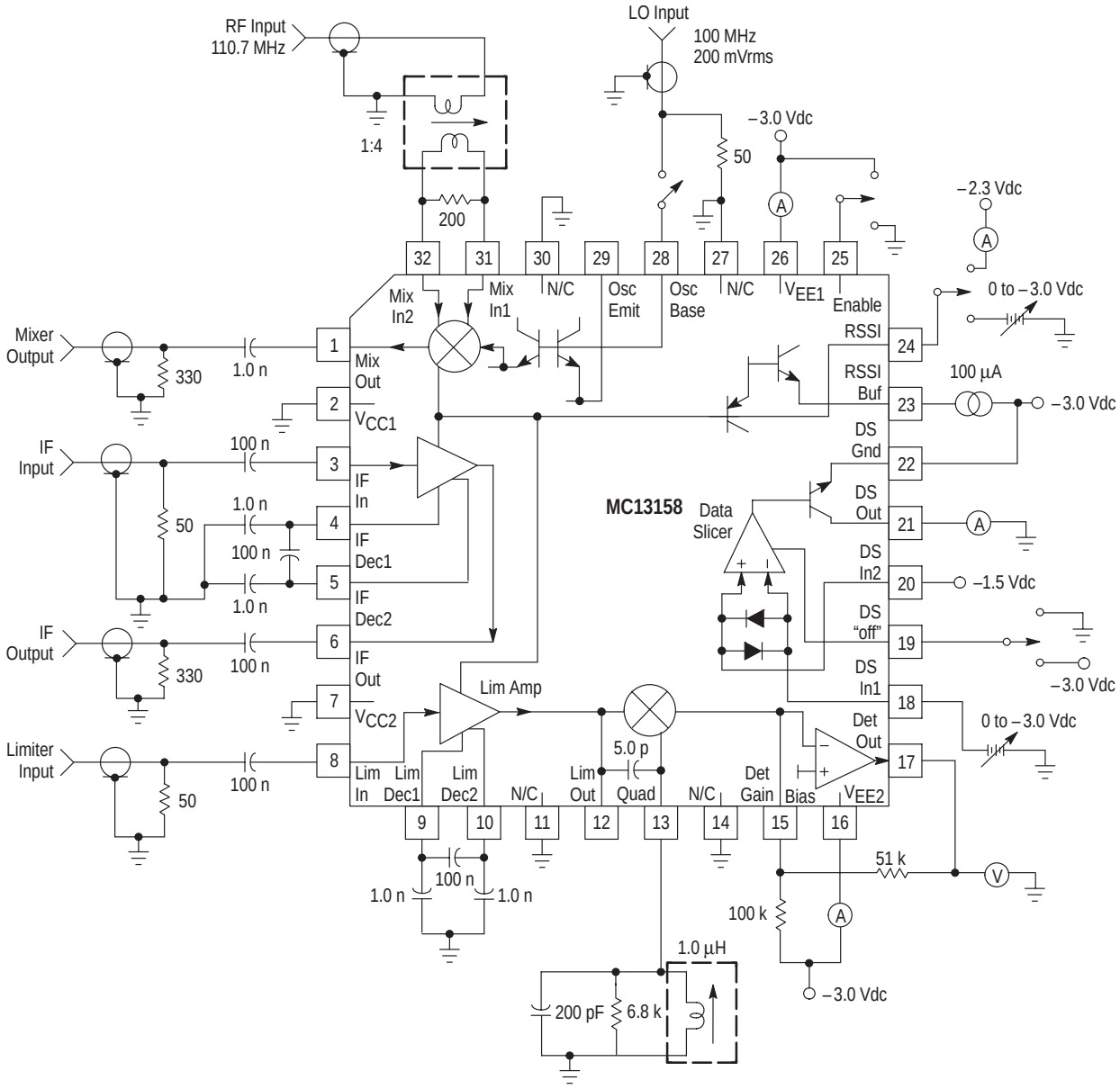
AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_S = 3.0 Vdc; f_{RF} = 110.7 MHz; f_{LO} = 100 MHz; See Figure 1.)

Characteristic	Condition	Pin	Symbol	Min	Typ	Max	Unit
MIXER							
Mixer Conversion Gain	V_{in} = 1.0 mVrms See Figure 5	31, 32, 1	–	–	22	–	dB
Noise Figure	Input Matched	31, 32, 1	NF	–	14	–	dB
Mixer Input Impedance	Single–Ended See Figure 15	31, 32	Rp Cp	– –	865 1.6	– –	Ω pF
Mixer Output Impedance		1	–	–	330	–	Ω

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C; V_S = 3.0 Vdc; f_{RF} = 110.7 MHz; f_{LO} = 100 MHz; See Figure 1.)

Characteristic	Condition	Pin	Symbol	Min	Typ	Max	Unit
IF AMPLIFIER SECTION							
IF RSSI Slope	See Figure 8	23	–	0.15	0.3	0.4	μA/dB
IF Gain	f = 10.7 MHz See Figure 7	3, 6	–	–	36	–	dB
Input Impedance		3	–	–	330	–	Ω
Output Impedance		6	–	–	330	–	Ω
LIMITING AMPLIFIER SECTION							
Limiter RSSI Slope	See Figure 9	23	–	0.15	0.3	0.4	μA/dB
Limiter Gain	f = 10.7 MHz	8, 12	–	–	70	–	dB
Input Impedance		8	–	–	330	–	Ω

Figure 1. Test Circuit



Typical Performance Over Temperature

(per Figure 1)

Figure 2. Total Supply Current versus Ambient Temperature, Supply Voltage

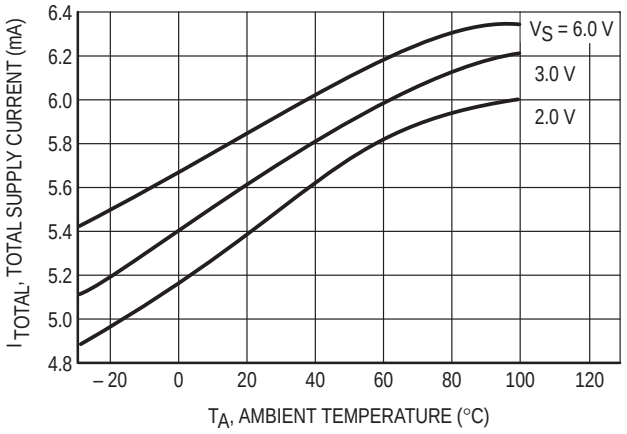


Figure 3. Data Slicer On Output Current versus Ambient Temperature

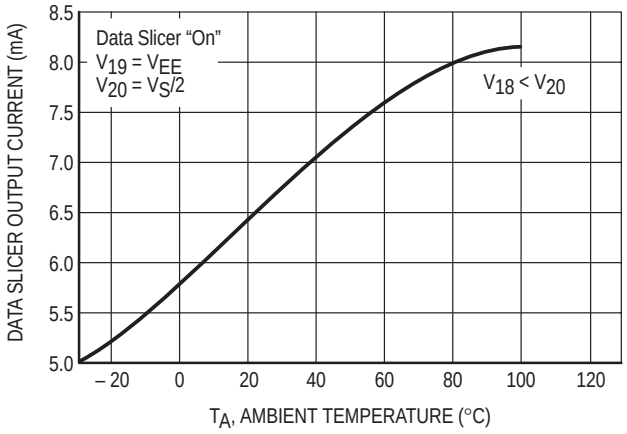


Figure 4. Data Slicer On Output Current versus Ambient Temperature

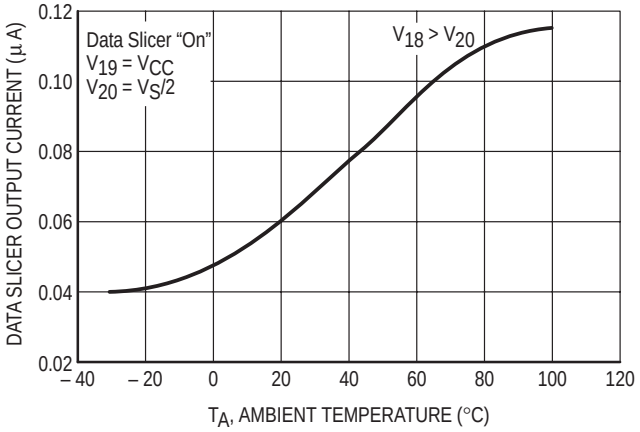


Figure 5. Normalized Mixer Gain versus Ambient Temperature

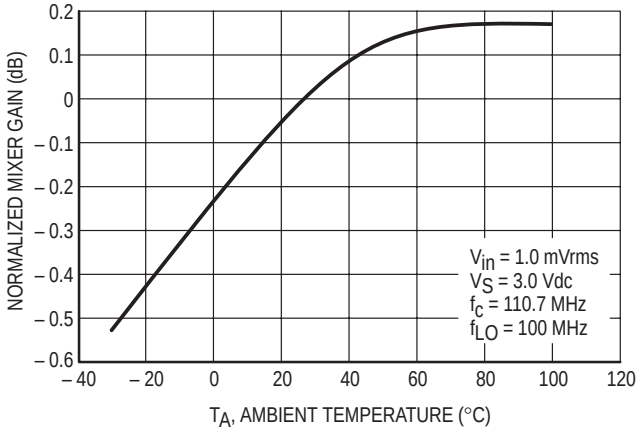


Figure 6. Mixer RSSI Output Current versus Ambient Temperature, Mixer Input Level

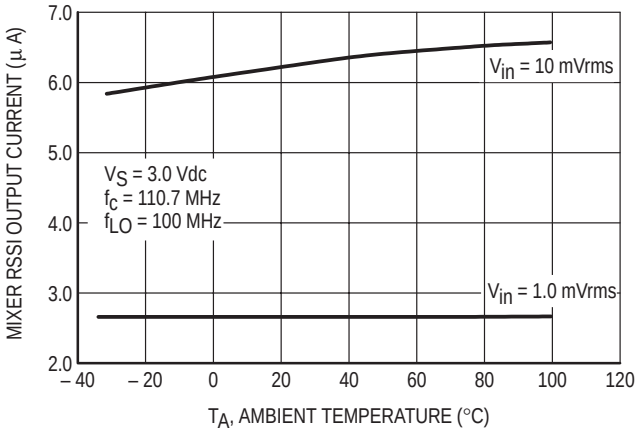
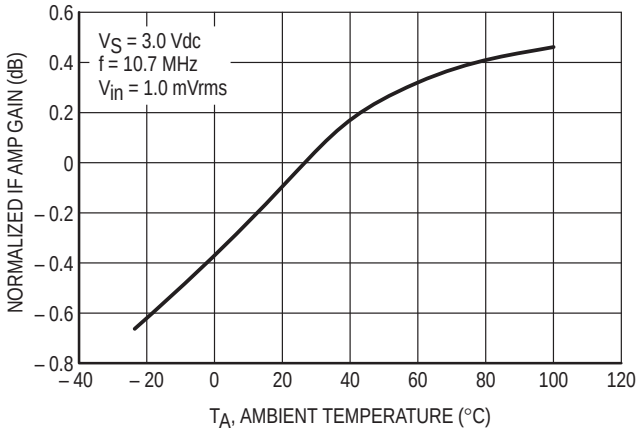


Figure 7. Normalized IF Amp Gain versus Ambient Temperature



tTypical Performance Over Temperature

(per Figure 1)

Figure 8. IF Amp RSSI Output Current versus Ambient Temperature, IF Input Level

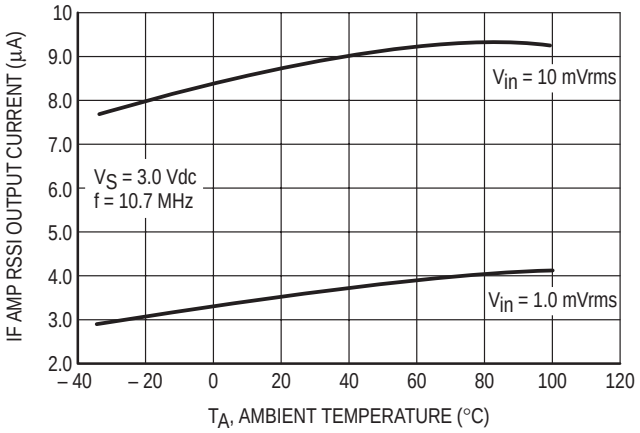


Figure 9. Limiter Amp RSSI Output Current versus Ambient Temperature, Input Signal Level

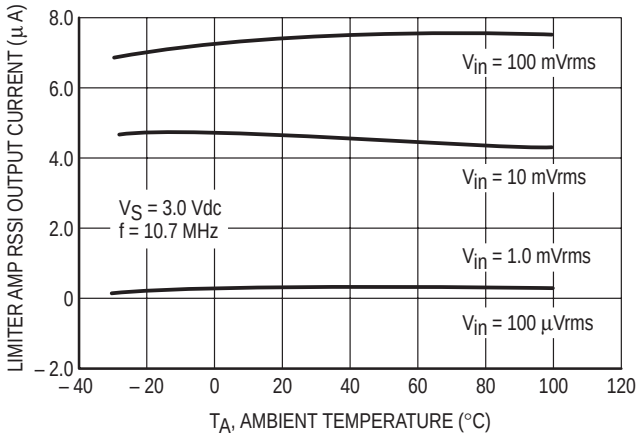


Figure 10. Total RSSI Output Current versus Ambient Temperature (No Signal)

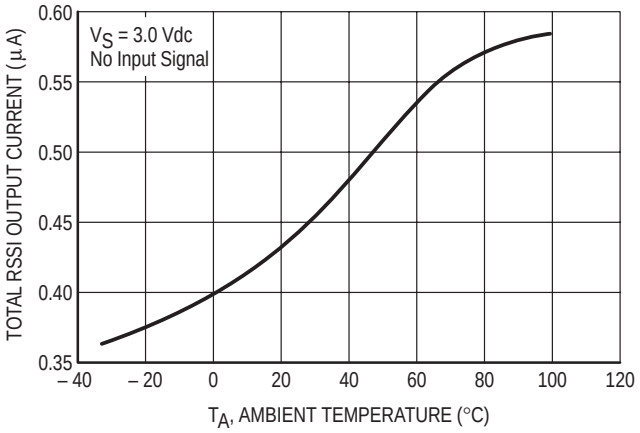
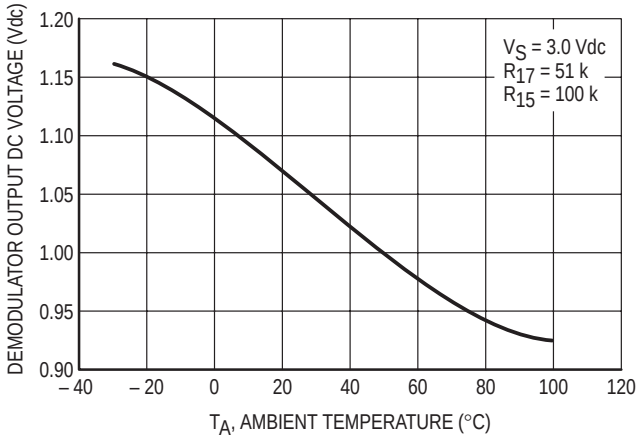


Figure 11. Demodulator DC Voltage versus Ambient Temperature



SYSTEM LEVEL AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_S = 3.0 Vdc; f_{RF} = 112 MHz; f_{LO} = 122.7 MHz)

Characteristic	Condition	Notes	Symbol	Typ	Unit
12 dB SINAD Sensitivity: Narrowband Application	f_{RF} = 112 MHz f_{mod} = 1.0 kHz f_{dev} = ±125 kHz SINAD Curve	1	–		dBm
Without Preamp	Figure 25			–101	
With Preamp	Figure 26			–113	
Third Order Intercept Point	f_{RF1} = 112 MHz f_{RF2} = 112.1 MHz	2	IIP3	–32	dBm
1.0 dB Comp. Point	V_S = 3.5 Vdc Figure 28		1.0 dB C.Pt.	–39	

NOTES: 1. Test Circuit & Test Set per Figure 24.
2. Test Circuit & Test Set per Figure 27.

CIRCUIT DESCRIPTION

General

The MC13158 is a low power single conversion wideband FM receiver incorporating a split IF. This device is designated for use as the backend in digital FM systems such as Digital European Cordless Telephone (DECT) and wideband data links with data rates up to 2.0 Mbps. It contains a mixer, oscillator, Received Signal Strength Indicator (RSSI), IF amplifier, limiting IF, quadrature detector, power down or enable function, and a data slicer with output off function. Further details are covered in the Pin Function Description which shows the equivalent internal circuit and external circuit requirements.

Current Regulation/Enable

Temperature compensating voltage independent current regulators which are controlled by the enable pin (Pin 25) where “low” powers up and “high” powers down the entire circuit.

Mixer

The mixer is a double–balanced four quadrant multiplier and is designed to work up to 500 MHz. It can be used in differential or in single ended mode by connecting the other input to the positive supply rail. The linear gain of the mixer is approximately 22 dB at 100 mVrms LO drive level. The mixer gain and noise figure have been emphasized at the expense of intermodulation performance. RSSI measurements are added in the mixer to extend the range to higher signal levels. The single–ended parallel equivalent input impedance of the mixer is Rp ~ 1.0 kΩ and Cp ~ 2.0 pF. The buffered output of the mixer is internally loaded resulting in an output impedance of 330 Ω.

Local Oscillator

The on–chip transistor operates with crystal and LC resonant elements up to 220 MHz. Series resonant, overtone crystals are used to achieve excellent local oscillator stability. Third overtone crystals are used through about 65 to 70 MHz. Operation from 70 MHz up to 180 MHz is feasible using the on–chip transistor with a 5th or 7th overtone crystal. To enhance operation using an overtone crystal, the internal transistor bias is increased by adding an external resistor from Pin 29 to V_{EE}; however, with an external resistor the oscillator stays on during power down. Typically, –10 dBm of local oscillator drive is needed to adequately drive the mixer. With an external oscillator source, the IC can be operated up to 500 MHz.

RSSI

The received signal strength indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the mixer, IF and limiting amplifier stages. An increase in RSSI dynamic range, particularly at higher input signal levels is achieved. The RSSI circuit is designed to provide typically 85 dB of dynamic range with temperature compensation.

Linearity of the RSSI is optimized by using external ceramic bandpass filters which have an insertion loss of 4.0 dB and 330 Ω source and load impedance. For higher data rates used in DECT and related applications, LC bandpass filtering is necessary to acquire the desired bandpass response; however, the RSSI linearity will require the same insertion loss.

RSSI Buffer

The RSSI output current creates a voltage across an external resistor. A unity voltage–gain amplifier is used to buffer this voltage. The output of this buffer has an active pull–up but no pull–down, so it can also be used as a peak detector. The negative slew rate is determined by external capacitance and resistance to the negative supply.

IF Amplifier

The first IF amplifier section is composed of three differential stages with the second and third stages contributing to the RSSI. This section has internal DC feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 40 dB at 10.7 MHz.

The fixed internal input impedance is 330 Ω. When using ceramic filters requiring source and loss impedances of 330 Ω, no external matching is necessary. Overall RSSI linearity is dependent on having total midband attenuation of 10 dB (4.0 dB insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the IF amplifier is buffered and the impedance is 330 Ω.

Limiter

The limiter section is similar to the IF amplifier section except that five differential stages are used. The fixed internal input impedance is 330 Ω. The total gain of the limiting amplifier section is approximately 70 dB. This IF limiting amplifier section internally drives the quadrature detector section and it is also brought out on Pin 12.

Quadrature Detector

The quadrature detector is a doubly balanced four quadrant multiplier with an internal 5.0 pF quadrature capacitor between Pins 12 and 13. An external capacitor may be added between these pins to increase the IF signal to the external parallel RLC resonant circuit that provides the 90 degree phase shift and drives the quadrature detector. A single pin (Pin 13) provides for the external LC parallel resonant network and the internal connection to the quadrature detector.

Internal low pass filter capacitors have been selected to control the bandwidth of the detector. The recovered signal is brought out by the inverting amplifier buffer. An external feedback resistor from the output (Pin 17) to the input of the inverting amplifier (Pin 15) controls the output amplitude; it is combined with another external resistor from the input to the negative supply (Pin 16) to set the output dc level. For a resistor ratio of 1, the DC level at the detector output is 2.0 V_{BE} (see Figure 12). A small capacitor C_{17} across the first resistor (from Pin 17 to 15) can be used to reduce the bandwidth.

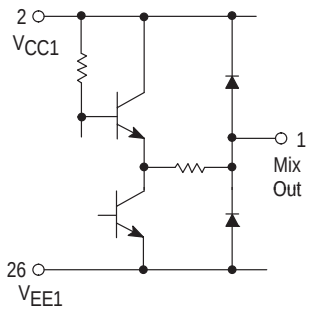
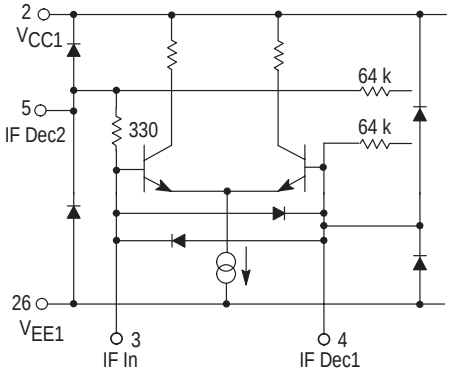
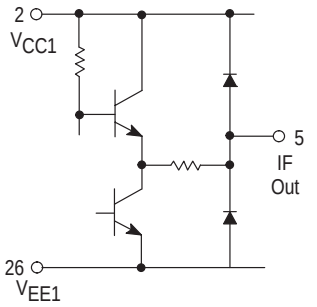
Data Slicer

The data slicer is a comparator that is designed to square up the data signal. Across the data slicer inputs (Pins 18 and 20) are back to back diodes.

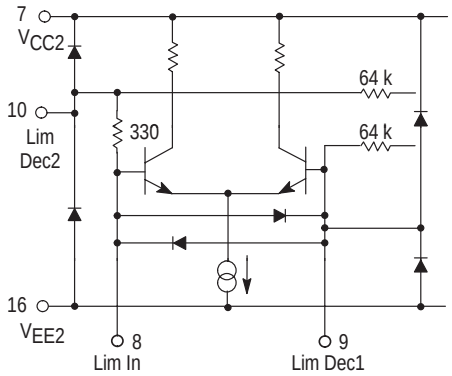
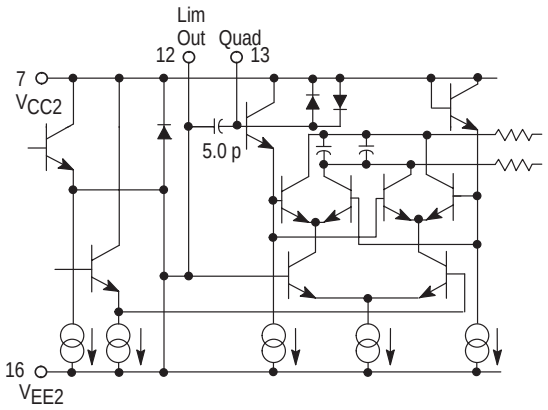
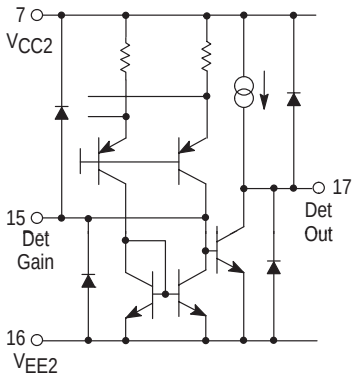
The recovered data signal from the quadrature detector can be DC coupled to the data slicer DS IN1 (Pin 18). In the application circuit shown in Figure 1 it will be centered at 2.0 V_{BE} and allowed to swing ± V_{BE}. A capacitor is placed from DS IN2 (Pin 20) to V_{EE}. The size of this capacitor and the nature of the data signal determine how faithfully the data slicer shapes up the recovered signal. The time constant is short for large peak to peak voltage swings or when there is a change in DC level at the detector output. For small signal or for continuous bits of the same polarity which drift close to the threshold voltage, the time constant is longer.

A unique feature of the data slicer is that the inverting switching stages in the comparator are supplied through the emitter pin of the output transistor (Pin 22 – DS Gnd) to V_{EE} rather than internally to V_{EE}. This is provided in order to reduce switching feedback to the front end. A control pin is provided to shut the data slicer output off (DS "off" – Pin 19). With DS "off" pin at V_{CC} the data slicer output is shut off by shutting down the base drive to the output transistor. When a channel is being monitored to make an RSSI measurement, but not to collect data, the data output may be shut off to save current.

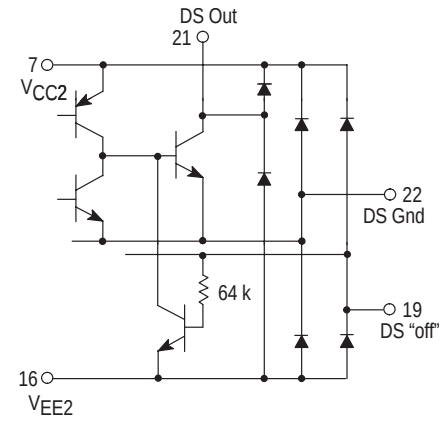
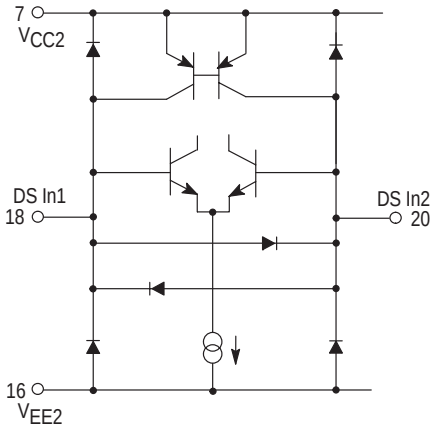
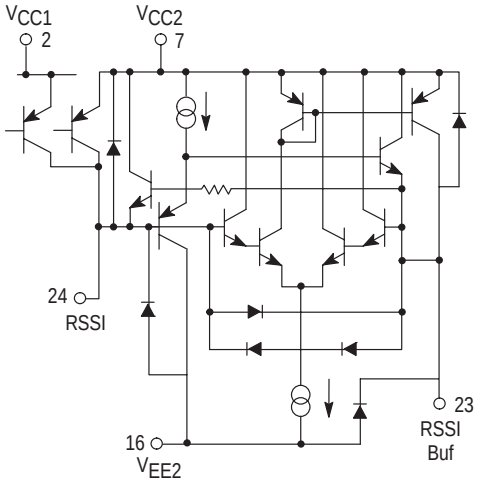
PIN FUNCTION DESCRIPTION

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
1	Mix Out		**Mixer Output** The mixer output impedance is 330 Ω; it matches to 10.7 MHz ceramic filters with 330 Ω input impedance.
2	V_{CC1}		**Supply Voltage (V_{CC1})** This pin is the V_{CC} pin for the Mixer, Local Oscillator, and IF Amplifer. The operating supply voltage range is from 1.8 Vdc to 5.0 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as possible to minimize inductive reactances along the trace; it is best to have it completely fill around the surface mount components and traces on the circuit side of the PCB.
3	IF In		**IF Input** The input impedance at Pin 3 is 330 Ω. It matches the 330 Ω load impedance of a 10.7 MHz ceramic filter. Thus, no external matching is required.
4	IF Dec1		**IF DEC1 & DEC2** IF decoupling pins. Decoupling capacitors should be placed directly at the pins to enhance stability. Two capacitors are decoupled to the RF ground V_{CC1}; one is placed between DEC1 & DEC2.
5	IF Dec2		
6	IF Out		**IF Output** The output impedance is 330 Ω; it matches the 330 input resistance of a 10.7 MHz ceramic filter.

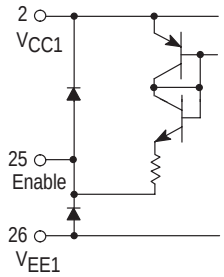
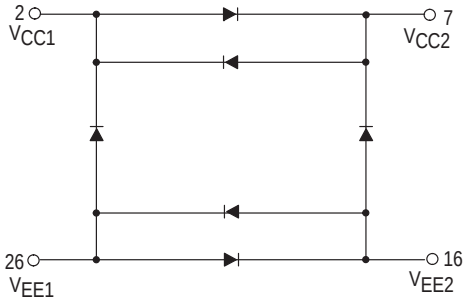
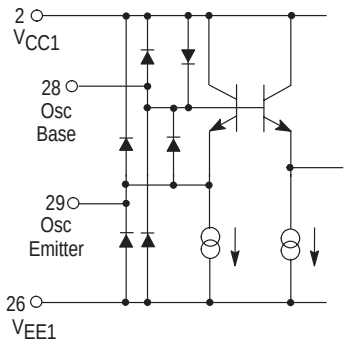
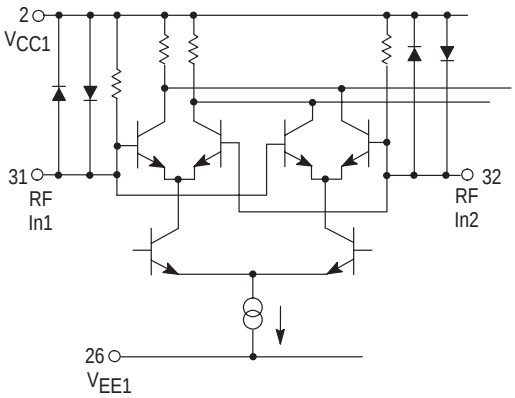
PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
7	V_{CC2}		**Supply Voltage (V_{CC2})** This pin is V_{CC} supply for the Limiter, Quadrature Detector, data slicer and RSSI buffer circuits. In the application PC board this pin is tied to a common V_{CC} trace with V_{CC1}.
8	Lim In		**Limiter Input** The limiter input impedance is 330 Ω.
9	Lim Dec1		**Limiter Decoupling** Decoupling capacitors are placed directly at these pins and to V_{CC} (RF ground). Use the same procedure as in the IF decoupling.
10	Lim Dec2		
11,14, 27 & 28	N/C		**No Connects** There is no internal connection to these pins; however it is recommended that these pins be connected externally to V_{CC} (RF ground).
12	Lim Out		**Limiter Output** The output impedance is low. The limiter drives a quadrature detector circuit with in–phase and quadrature phase signals.
13	Quad		**Quadrature Detector Circuit** The quadrature detector is a doubly balanced four–quadrant multiplier with an internal 5.0 pF capacitor between Pins 12 and 13. An external capacitor may be added to increase the IF signal to Pin 13. The quadrature detector pin is provided to connect the external RLC parallel resonant network which provides the 90 degree phase shift and drives the quadrature detector.
15	Det Gain		**Detector Buffer Amplifier** This is an inverting amplifier. An external feedback resistor from Pin 17 to 15, (the inverting input) controls the output amplitude; another resistor from Pin 15 to the negative supply (Pin 16) sets the DC output level. A 1:1 resistor ratio sets the output DC level at two V_{BE} with respect to V_{EE}. A small capacitor from Pin 17 to 15 can be used to set the bandwidth.
17	Det Out		
16	V_{EE2}		**Supply Ground (V_{EE2})** In the PCB layout, the ground pins (also applies to Pin 26) should be connected directly to chassis ground. Decoupling capacitors to V_{CC} should be placed directly at the ground pins.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
19 21 22	DS “off” DS Out DS Gnd		**Data Slicer Off** The data output may be shut off to save current by placing DS “off” (Pin 19) at V_{CC}. **Data Slicer Output** In the application example a 10 kΩ pull–up resistor is connected to the collector of the output transistor at Pin 21. **Data Slicer Ground** All the inverting switching stages in the comparator are supplied through the emitter pin of the output transistor (Pin 22) to ground rather than internally to V_{EE} in order to reduce switching feedback to the front end.
18 20	DS In1 DS In2		**Data Slicer Inputs** The data slicer has differential inputs with back to back diodes across them. The recovered signal is DC coupled to DS IN1 (Pin 18) at nominally V_{18} with respect to V_{EE}; thus, it will maintain $V_{18} \pm V_{BE}$ at Pin 18. DS IN2 (Pin 20) is AC coupled to V_{EE}. The choice of coupling capacitor is dependent on the nature of the data signal. For small signal or continuous bits of the same polarity, the response time is relatively large. On the other hand, for large peak to peak voltage swings or when the DC level at the detector output changes, the response time is short. See the discussion in the application section for external circuit design details.
23 24	RSSI Buf RSSI		**RSSI Buffer** A unity gain amplifier is used to buffer the voltage at Pin 24 to 23.The output of the unity gain buffer (Pin 23) has an active pull up but no pull down. An external resistor is placed from Pin 23 to V_{EE} to provide the pull down. **RSSI** The RSSI output current creates a voltage drop across an external resistor from Pin 24 to V_{EE}. The maximum RSSI current is 26 μA; thus, the maximum RSSI voltage using a 100 kΩ resistor is approximately 2.6 Vdc. Figure 22 shows the RSSI Output Voltage versus Input Signal Level in the application circuit. The negative slew rate is determined by an external capacitor and resistor to V_{EE} (negative supply). The RSSI rise and fall times for various RF input signal levels and R_{24} values without the capacitor, C_{24} are displayed in Figure 24. This is the maximum response time of the RSSI.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
25 26	Enable V_{EE1}		**Enable** The IC regulators are enabled by placing this pin at V_{EE}.
			**V_{CC} and V_{EE} ESD Protection** ESD protection diodes exist between the V_{CC} and V_{EE} pins. It is important to note that significant differences in potential (> 0.5 V_{BE}) between the two V_{CC} pins or between the V_{EE} pins can cause these structures to start to conduct, thus compromising isolation between the supply busses. V_{CC1} & V_{CC2} should be maintained at the same DC potential, as should V_{EE1} & V_{EE2}.
28 29	Osc Base Osc Emitter		**Oscillator Base** This pin is connected to the base lead of the common collector transistor. Since there is no internal bias resistor to the base, V_{CC} is applied through an external choke or coil. **Oscillator Emitter** This pin is connected to the emitter lead; the emitter is connected internally to a current source of about 200 μA. Additional emitter current may be obtained by connecting an external resistor to V_{EE}; $I_E = V_{29}/R_{29}$. Details of circuits using overtone crystal and LC varactor controlled oscillators are discussed in the application section.
31 32	Mix In1 Mix In2		**Mixer Inputs** The parallel equivalent differential input impedance of the mixer is approximately 2.0 kΩ in parallel with 1.0 pF. This equates to a single ended input impedance of 1.0 kΩ in parallel with 2.0 pF. The application circuit utilizes a SAW filter having a differential output that requires a 2.0 kΩ II 2.0 pF load. Therefore, little matching is required between the SAW filter and the mixer inputs. This and alternative circuits are discussed in more detail in the application section.

APPLICATIONS INFORMATION

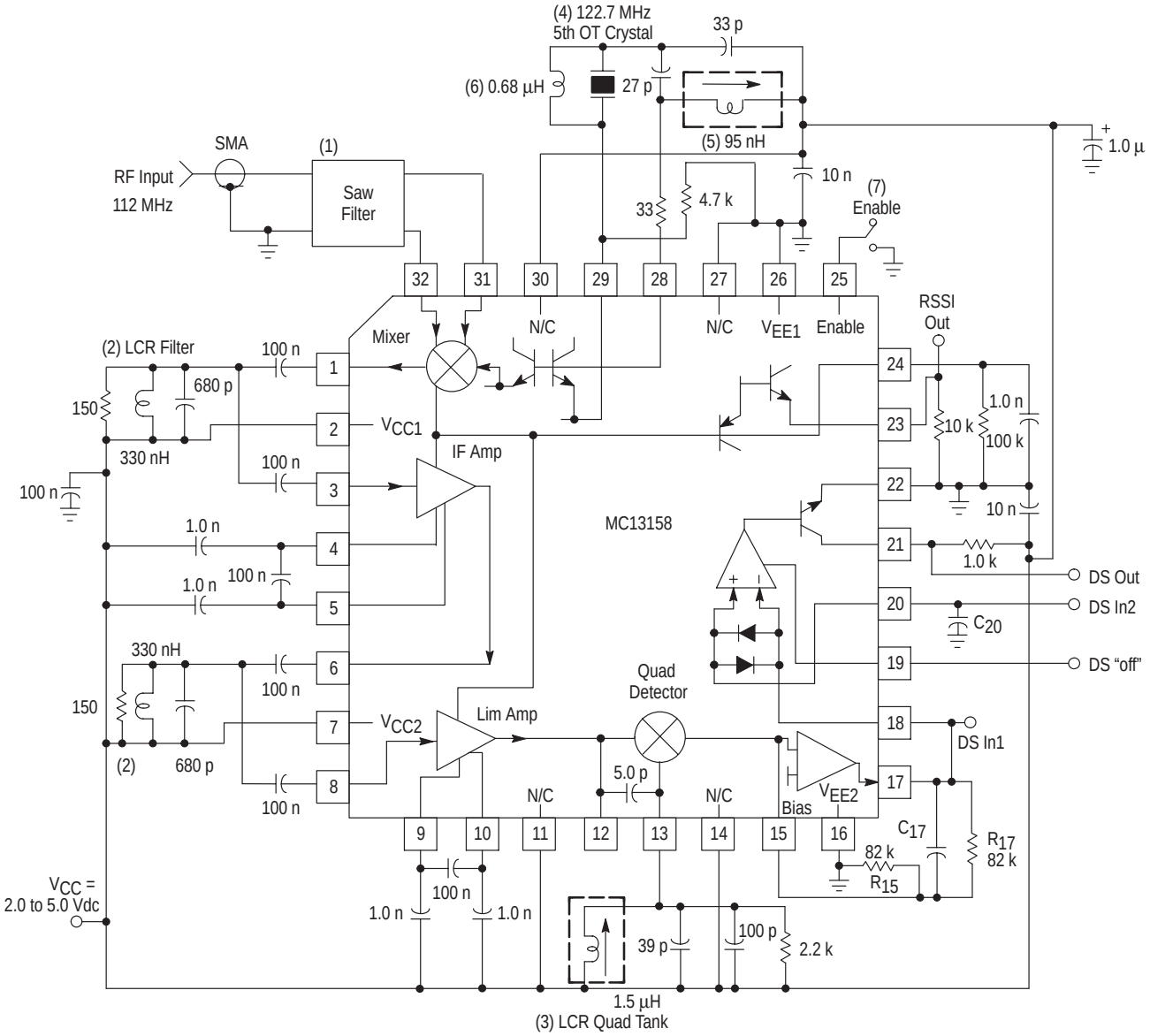
Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side (see Figures 29 and 30). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. Figures 13 and 14 show the placement for the components specified in the application circuit (Figure 12). The application circuit schematic specifies particular components that were used to achieve the results shown in the typical curves and tables but alternate components should give similar results.

Figure 12. Application Circuit



NOTES: 1. Saw Filter – Siemens part number Y6970M(5 pin SIP plastic package).
2. An LCR filter reduces the broadband noise in the IF; ceramic filters may be used for data rates under 500 kHz. 4.0 dB insertion loss filters optimize the linearity of RSSI.
3. The quadrature tank components are chosen to optimize linearity of the recovered signal while maintaining adequate recovered signal level. 1.5 µH 7.0 mm variable shielded inductor: Toko part # 292SNS–T1373Z. The shunt resistor is approximately equal to Q(2πfL), where Q ~ 18 (3.0 dB BW = 600 kHz).
4. The local oscillator circuit utilizes a 122.7 MHz, 5th overtone, series resonant crystal specified with a frequency tolerance of 25 PPM, ESR of 120 Ω max. The oscillator configuration is an emitter coupled butler.
5. The 95 NH (Nominal) inductor is a 7.0 mm variable shielded inductor: Coilcraft part # 150–04J08S or equivalent.
6. 0.68 µH axial lead chokes (molded inductor): Coilcraft part # 90–11.
7. To enable the IC, Pin 25 is taken to V_{EE}. The external pull down resistor at Pin 29 could be linked to the enable function; otherwise if it is taken to V_{EE} as shown, it will keep the oscillator biased at about 500 µA depending on the V_{CC} level.
8. The other resistors and capacitors are surface mount components.

Figure 13. Circuit Side Component Placement

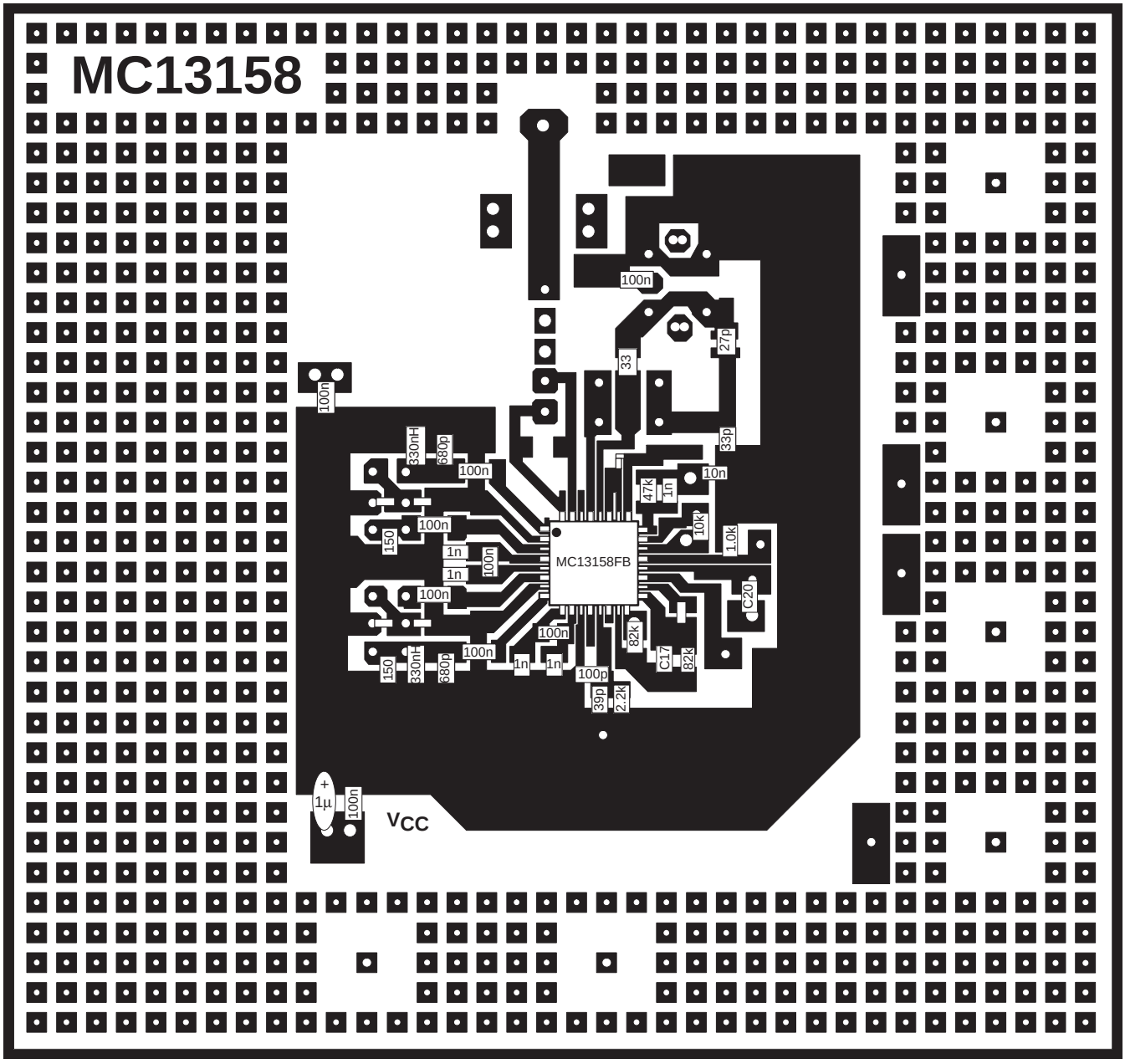
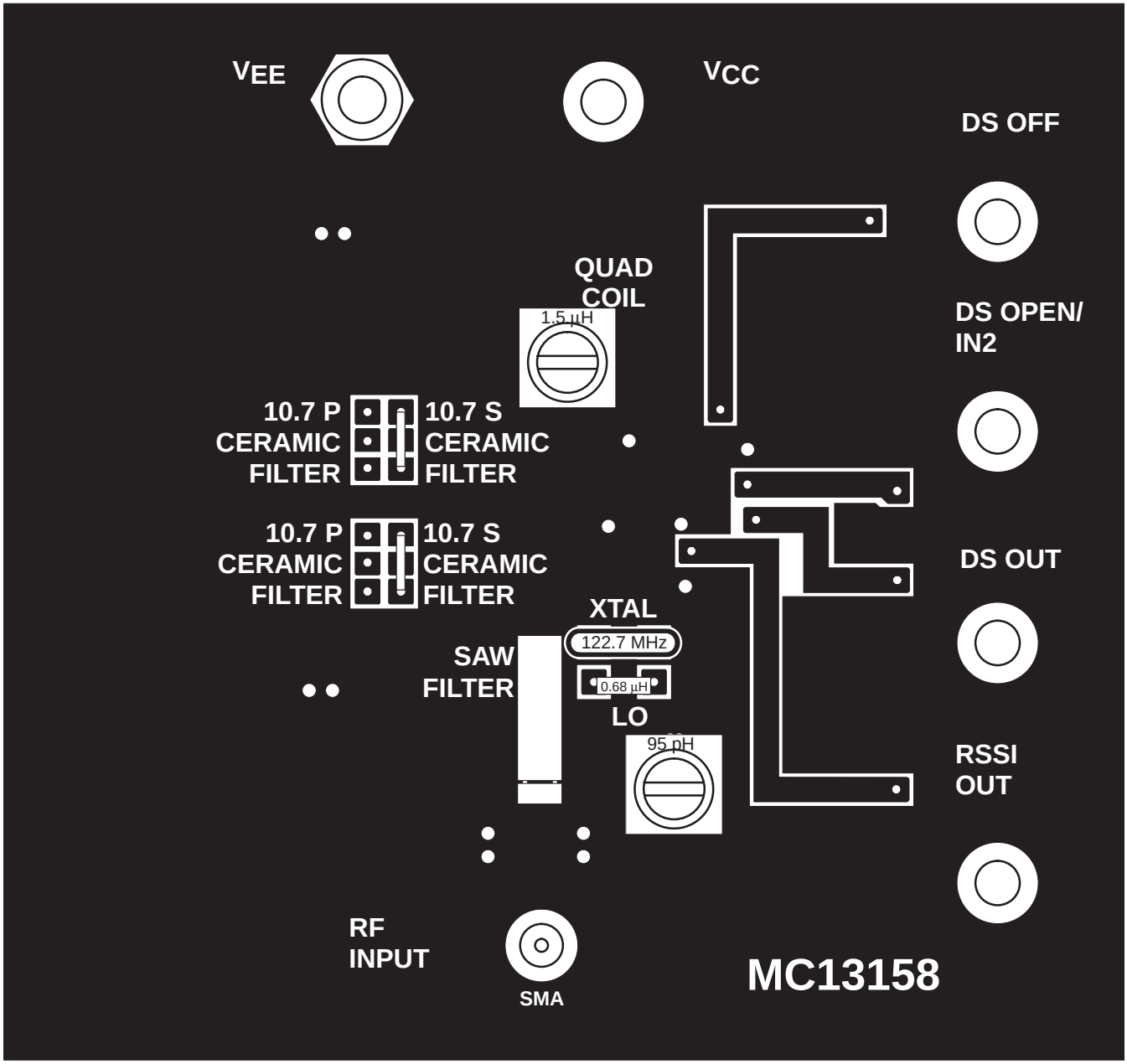


Figure 14. Ground Side Component Placement



Input Matching/Components

It is desirable to use a SAW filter before the mixer to provide additional selectivity and adjacent channel rejection. In a wideband system the primary sensitivity of the receiver backend may be achieved before the last mixer. Bandpass filtering in the limiting IF is costly and difficult to achieve for bandwidths greater than 280 kHz.

The SAW filter should be selected to easily interface with the mixer differential input impedance of approximately 2.0 kΩ in parallel with 1.0 pF. The PC board is dedicated to the Siemens SAW filter (part number Y6970M); the part is designed for DECT at 112 MHz 1st IF frequency. It is designed for a load impedance of 2.0 kΩ in parallel with 2.0 pF; thus, no or little input matching is required between the SAW filter and the mixer.

The Siemens SAW filter has an insertion loss of typically 10 dB and a 3.0 dB bandwidth of 1.0 MHz. The relatively high insertion loss significantly contributes to the system noise and a filter having lower insertion loss would be desirable. In existing low loss SAW filters, the required load impedance is 50 Ω; thus, interface matching between the filter and the mixer will be required. Figure 15 is a table of the single–ended mixer input impedance. A careful noise analysis is necessary to determine the secondary contribution to system noise.

Figure 15. Mixer Input Impedance

(Single–ended)

f (MHz)	Rs (Ω)	Xs (Ω)	Rp (Ω)	Xp (Ω)	Cp (pF)
50	930	–350	1060	–2820	1.1
100	480	–430	865	–966	1.6
150	270	–400	860	–580	1.8
200	170	–320	770	–410	1.9
250	130	–270	690	–330	1.85
300	110	–250	680	–300	1.8
400	71	–190	580	–220	1.8
500	63	–140	370	–170	1.9
600	49	–110	300	–130	2.0

System Noise Considerations

The system block diagram in Figure 16 shows the cascaded noise stages contributing to the system noise; it represents the application circuit in Figure 12 and a low noise preamp using a MRF941 transistor (see Figure 17). The preamp is designed for a conjugately matched input and output at 2.0 Vdc V_{CE} and 3.0 mAdc I_C. S–parameters at 2.0 V, 3.0 mA and 100 MHz are:

S11 = 0.86, –20
S21 = 9.0, 164
S12 = 0.02, 79
S22 = 0.96, –12

The bias network sets V_{CE} at 2.0 V and I_C at 3.0 mA for V_{CC} = 3.0 to 3.5 Vdc. The preamp operates with 18 dB gain and 2.7 dB noise figure.

In the cascaded noise analysis the system noise equation is:

$$Fsystem = F1 + [(F2–1)/G1] + [(F3–1)]/[(G1)(G2)]$$

where:

F1 = the Noise Factor of the Preamp
G1 = the Gain of the Preamp
F2 = the Noise factor of the SAW Filter
G2 = the Gain of the SAW Filter
F3 = the Noise factor of the Mixer

Note: the proceeding terms are defined as linear relationships and are related to the log form for gain and noise figure by the following:

$$F = \log^{-1}[(NF \text{ in dB})/10] \quad \text{and similarly}$$

$$G = \log^{-1}[(Gain \text{ in dB})/10]$$

The noise figure and gain measured in dB are shown in the system block diagram. The mixer noise figure is typically 14 dB and the SAW filter adds typically 10 dB insertion loss. Addition of a low noise preamp having a 18 dB gain and 2.7 dB noise figure not only improves the system noise figure but it increases the reverse isolation from the local oscillator to the antenna input at the receiver. Calculating in terms of gain and noise factor yields the following:

F1 = 1.86; G1 = 63.1
F2 = 10; G2 = 0.1
F3 = 25.12

Thus, substituting in the equation for system noise factor:

Fsystem = 5.82; NFsystem = 7.7 dB

Figure 16. System Block Diagram for Noise Analysis

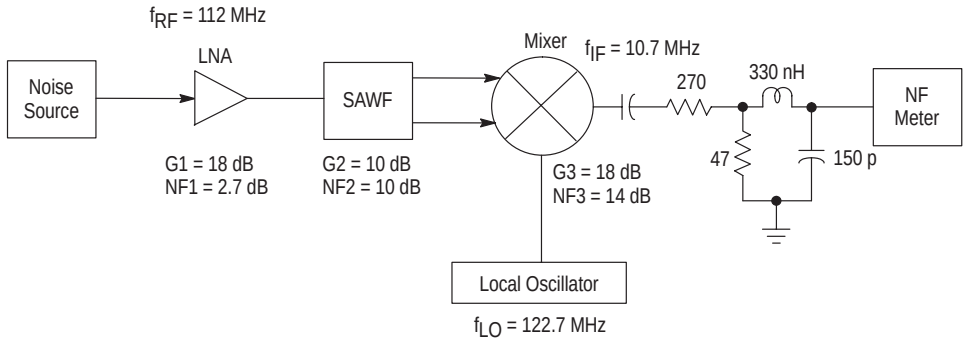
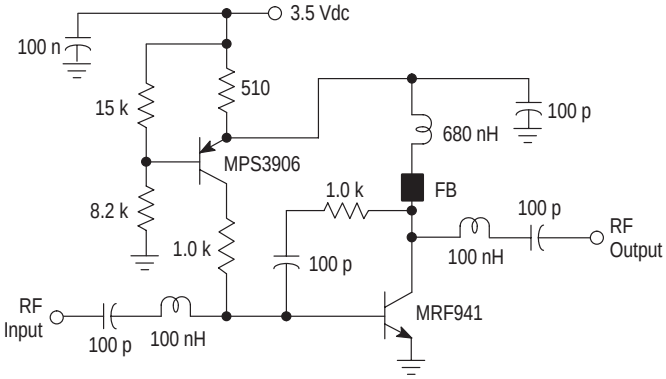


Figure 17. 112 MHz LNA



LOCAL OSCILLATORS

VHF Applications

The on–chip grounded collector transistor may be used for HF and VHF local oscillator with higher order overtone crystals. The local oscillator in the application circuit (Figure 12) shows a 5th overtone oscillator at 122.7 MHz. This circuit uses a Butler overtone oscillator configuration. The amplifier is an emitter follower. The crystal is driven from the emitter and is coupled to the high impedance base through a capacitive tap network. Operation at the desired overtone frequency is ensured by the parallel resonant circuit formed by the variable inductor and the tap capacitors and parasitic capacitances of the on–chip transistor and PC board. The variable inductor specified in the schematic could be replaced with a high tolerance, high Q ceramic or air wound surface mount component if the other components have tight enough tolerances. A variable inductor provides an adjustment for gain and frequency of the resonant tank ensuring lock up and start–up of the crystal oscillator. The overtone crystal is chosen with ESR of typically 80 Ω and 120 Ω maximum; if the resistive loss in the crystal is too high the performance of oscillator may be impacted by lower gain margins.

A series LC network to ground (which is V_{CC}) is comprised of the inductance of the base lead of the on–chip transistor and PC board traces and tap capacitors. Parasitic oscillations often occur in the 200 to 800 MHz range. A small resistor is placed in series with the base (Pin 28) to cancel the negative resistance associated with this undesired mode of oscillation. Since the base input impedance is so large a small resistor in the range of 27 to 68 Ω has very little effect on the desired Butler mode of oscillation.

The crystal parallel capacitance, C_O, provides a feedback path that is low enough in reactance at frequencies of 5th overtones or higher to cause trouble. C_O has little effect near resonance because of the low impedance of the crystal motional arm (R_m–L_m–C_m). As the tunable inductor which forms the resonant tank with the tap capacitors is tuned “off” the crystal resonant frequency it may be difficult to tell if the oscillation is under crystal control. Frequency jumps may occur as the inductor is tuned. In order to eliminate this behavior an inductor, L_O, is placed in parallel with the crystal. L_O is chosen to be resonant with the crystal parallel capacitance, C_O, at the desired operation frequency. The inductor provides a feedback path at frequencies well below resonance; however, the parallel tank network of the tap capacitors and tunable inductor prevent oscillation at these frequencies.

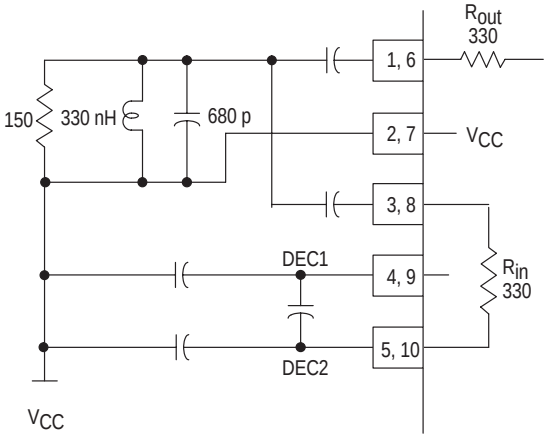
IF Filtering/Matching

In wideband data systems the IF bandpass needed is greater than can be found in low cost ceramic filters operating at 10.7 MHz. It is necessary to bandpass limit with LC networks or series–parallel ceramic filter networks. Murata offers a series–parallel resonator pair (part number

KMFC545) with a 3.0 dB bandwidth of ±325 kHz and a maximum insertion loss of 5.0 dB. The application PC board is laid out to accommodate this filter pair (a filter pair is used at both locations of the split IF). However, even using a series parallel ceramic filter network yields only a maximum bandpass of 650 kHz. In some applications a wider band IF bandpass is necessary.

A simple LC network yields a bandpass wider than the SAW filter but it does reduce an appreciable amount of wideband IF noise. In the application circuit an LC network is specified using surface mount components. The parallel LC components are placed from the outputs of the mixer and IF amplifier to the V_{CC} trace; internal 330 loads are connected from the mixer and IF amplifier outputs to DEC2 (Pin 5 and 10 respectively).This loads the outputs with the optimal load impedance but creates a low insertion loss filter. An external shunt resistor may be used to widen the bandpass and to acquire the 10 dB composite loss necessary to linearize the RSSI output. The equivalent circuit is shown in Figure 18.

Figure 18. IF LCR Filter



The following equations satisfy the 12 dB loss (1:4 resistive ratio):

$$(Rext)(330)/(Rext + 330) = Requivalent$$
$$Requivalent/(Requivalent + 330) = 1/4$$

Solve for Requivalent:

$$4(Requivalent) = Requivalent + 330$$
$$3(Requivalent) = 330$$
$$Requivalent = 110$$

Substitute for Requivalent and solve for Rext:

$$330(Rext) = 110(Rext) + (330)(110)$$
$$Rext = (330)(110)/220$$
$$Rext = 165\ \Omega$$

The IF is 10.7 MHz although any IF between 10 to 20 MHz could be used. The value of the coil is lowered from that used in the quadrature circuit because the unloaded Q must be maintained in a surface mount component. A standard value component having an unloaded Q = 100 at 10.7 MHz is 330 nH; therefore the capacitor is 669 pF. Standard values have been chosen for these components;

$$Rext = 150\ \Omega$$
$$C = 680\ pF$$
$$L = 330\ nH$$

Computation of the loaded Q of this LCR network is

$$Q = Requivalent/X_L$$

where: $X_L = 2\pi fL$ and Requivalent is 103 Ω

Thus, $Q = 4.65$

The total system loss is

$$20\ \log\ (103/433) = -12.5\ dB$$

Quadrature Detector

The quadrature detector is coupled to the IF with an internal 5.0 pF capacitor between Pins 12 and 13. For wideband data applications, the drive to the detector can be increased with an additional external capacitor between these pins; thus, the recovered signal level output is increased for a given bandwidth

The wideband performance of the detector is controlled by the loaded Q of the LC tank circuit. The following equation defines the components which set the detector circuit's bandwidth:

$$Q = R_T/X_L \quad \textbf{[1]}$$

where R_T is the equivalent shunt resistance across the LC Tank

X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi fL$).

The inductor and capacitor are chosen to form a resonant LC tank with the PCB and parasitic device capacitance at the desired IF center frequency as predicted by

$$f_c = [2\pi\ (LC_p)^{1/2}]^{-1} \quad \textbf{[2]}$$

where L is the parallel tank inductor C_p is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a wideband detector at 10.7 MHz and a loaded Q of 18. The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass. For an IF frequency of 10.7 MHz and an IF bandpass of 600 kHz, the IF bandpass Q is approximately 6.4.

Example:

Let the external Cext = 139 pF. (The minimum value here should be much greater than the internal device and PCB parasitic capacitance, Cint ≈ 3.0 pF). Thus, C_p = Cint + Cext = 142 pF.

Rewrite equation (2) and solve for L:

$$L = (0.159)^2/(C_p fc^2)$$

L = 1.56 μH; Thus, a standard value is choosen:

L = 1.56 μH (tunable shielded inductor)

The value of the total damping resistor to obtain the required loaded Q of 18 can be calculated by rearranging equation (1):

$$R_T = Q(2\pi fL)$$
$$R_T = 18(2\pi)(10.7)(1.5) = 1815\ \Omega$$

The internal resistance, Rint at the quadrature tank Pin 13 is approximately 13 kΩ and is considered in determining the external resistance, Rext which is calculated from

$$Rext = ((R_T)(Rint))/(Rint - R_T)$$

$$Rext = 2110; \text{ Thus, choose the standard value:}$$

$$Rext = 2.2\ k\Omega$$

It is important to set the DC level of the detector output at Pin 17 to center the peak to peak swing of the recovered signal. In the equivalent internal circuit shown in the Pin Function Description, the reference voltage at the positive terminal of the inverting op amp buffer amplifier is set at 1.0 V_{BE}. The detector DC level, V_{17} is determined by the following equation:

$$V_{17} = [((R_{15}/R_{17}) + 1)/(R_{15}/R_{17})]\ V_{BE}$$

Thus, for a 1:1 ratio of R_{15}/R_{17}, V_{17} = 2.0 V_{BE} = 1.4 Vdc. Similarly for a 2:1, V_{17} = 1.5 V_{BE} = 1.05 Vdc; and for 3:1, V_{17} = 1.33 V_{BE} = 0.93 Vdc.

Figure 19 shows the detector "S–Curves", in which the resistor ratio is varied while maintaining a constant gain (R_{17} is held at 62 k). R_{15} is 62 k for a 1:1 ratio; while R_{15} = 120 k and 180 k to produce the 2:1 and 3:1 ratios. The IF signal into the detector is swept ± 500 kHz about the 10.7 MHz IF center frequency. The resulting curve show how the resistor ratio and the supply voltage effects the symmetry of the "S–curve" (Figure 21 Test Setup). For the 3:1 and 2:1 ratio, symmetry is maintained with V_S from 2.0 to 5.0 Vdc; however, for the 1:1 ratio, symmetry is lost at 2.0 Vdc.

Figure 19. Detector Output Voltage versus Frequency Deviation

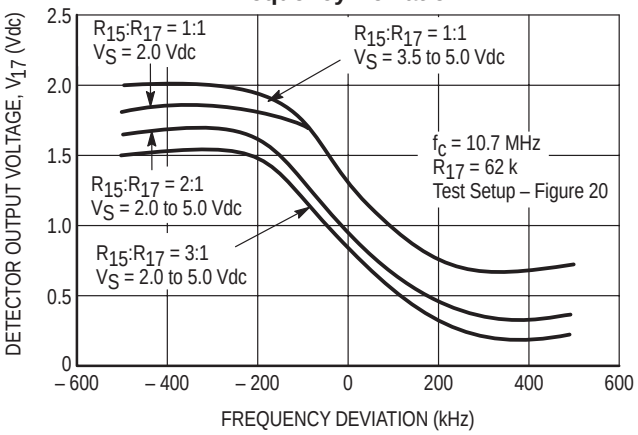
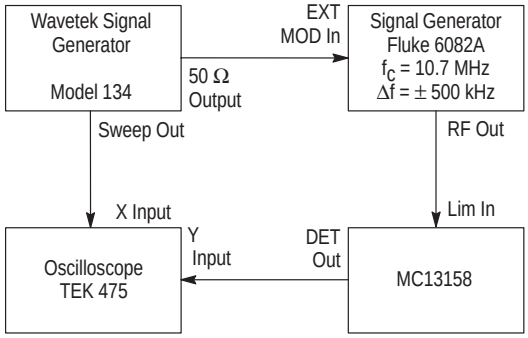


Figure 20. Demodulator "S–Curve" Test Setup



Data Slicer Circuit

C_{20} at the input of the data slicer is chosen to maintain a time constant long enough to hold the charge on the capacitor for the longest strings of bits at the same polarity. For a data rate at 576 kHz a bit stream of 15 bits at the same polarity would equate to an apparent data rate of approximately 77 kbps or 38 kHz. The time constant would be approximately 26 μs. The following expression equates the time constant, t, to the external components:

$$t = 2\pi\ (R_{18})(C_{20})$$

Solve for C_{20}:

$$C_{20} = t/2\pi\ (R_{18})$$

where the effective resistance R_{18} is a complex function of the demodulator feedback resistance and the data slicer input circuit. In the data input network the back to back diodes form a charge and discharge path for the capacitor at Pin 20; however, the diodes create a non–linear response. This resistance is loaded by the ß, beta of the detector output transistor; beta =100 is a typical value (see Figure 21). Thus, the apparent value of the resistance at Pin 18 (DS IN1) is approximately equal to:

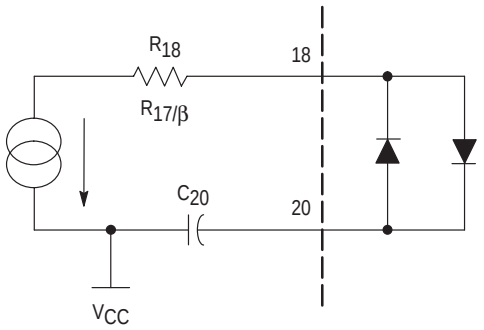
$$R_{18} \backsim R_{17}/100$$

where R_{17} is 82 kΩ, the feedback resistor from Pin 17 to 15. Therefore, substituting for R_{18} and solving for C_{20}:

$$C_{20} = 15.9\ (t)/R_{17} = 5.04\ nF$$

The closest standard value is 4.7 nF.

Figure 21. Data Slicer Equivalent Input Circuit



SYSTEM PERFORMANCE DATA

RSSI

In Figure 22, the RSSI versus RF Input Level shows the linear response of RSSI over a 65 dB range but it has extended capability over 80 dB from –80 dBm to +10 dBm. The RSSI is measured in the application circuit (Figure 12) in which a SAW filter is used before the mixer; thus, the overall sensitivity is compromised for the sake of selectivity. The curves are shown for three filters having different bandwidths:

1) LCR Filter with 2.3 MHz 3.0 dB BW (Circuit and Component Placement is shown in Figure 12)
2) Series–Parallel Ceramic Filter with 650 kHz 3.0 dB BW (Murata Part # KMFC–545)
3) Ceramic Filter with 280 kHz 3.0 dB BW.

Figure 22. RSSI Output Voltage versus Signal Input Level

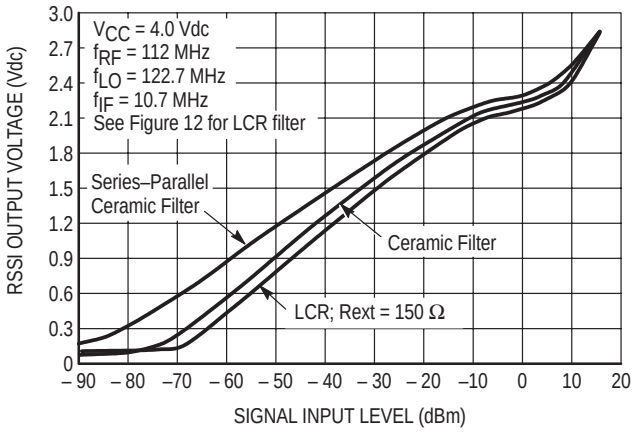
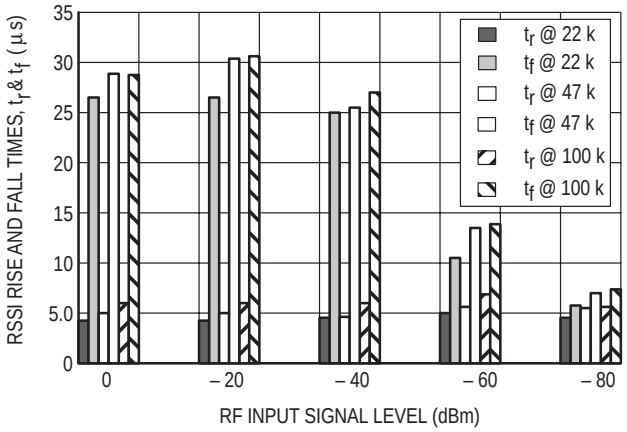


Figure 23. RSSI Output Rise and Fall Times versus RF Input Signal Level



SINAD Performance

Figure 24 shows a test setup for a narrowband demodulator output response in which a C–message filter and an active de–emphasis filter is used following the demodulator. The input is matched using a 1:4 impedance transformer. The SINAD performance is shown in Figure 25 with no preamp and in Figure 26 with a preamp (Preamp – Figure 16). The 12 dB SINAD sensitivity is –101 dBm with no preamp and –113 dBm with the preamp.

Figure 24. Test Setup for Narrowband SINAD

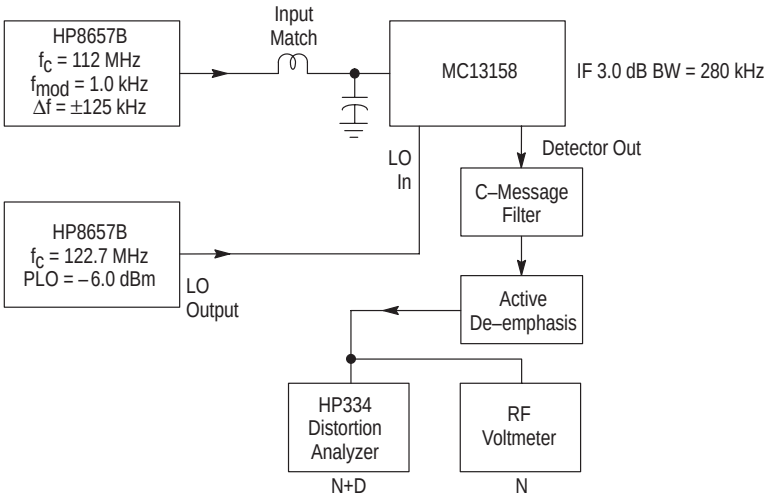


Figure 25. S+N+D, N+D, N versus Input Signal Level (without preamp)

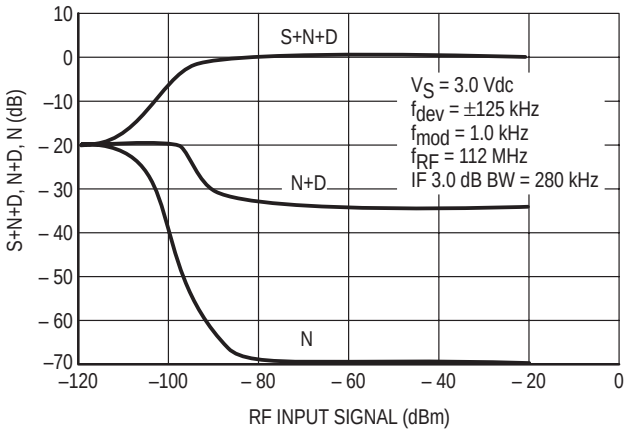


Figure 26. S+N+D, N+D, N versus Input Signal Level (with preamp)

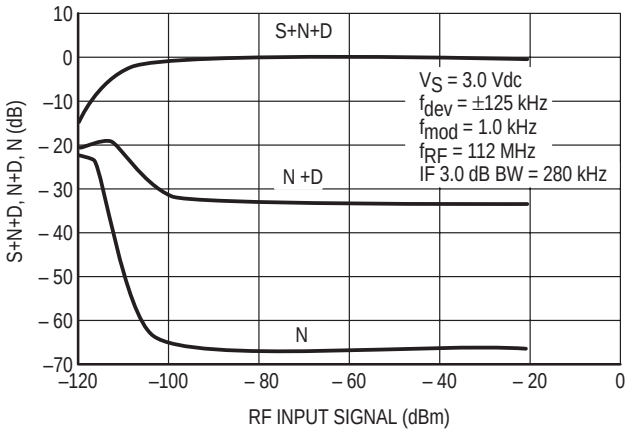


Figure 27. Input IP3, 1.0 dB Compression Pt. Test Setup

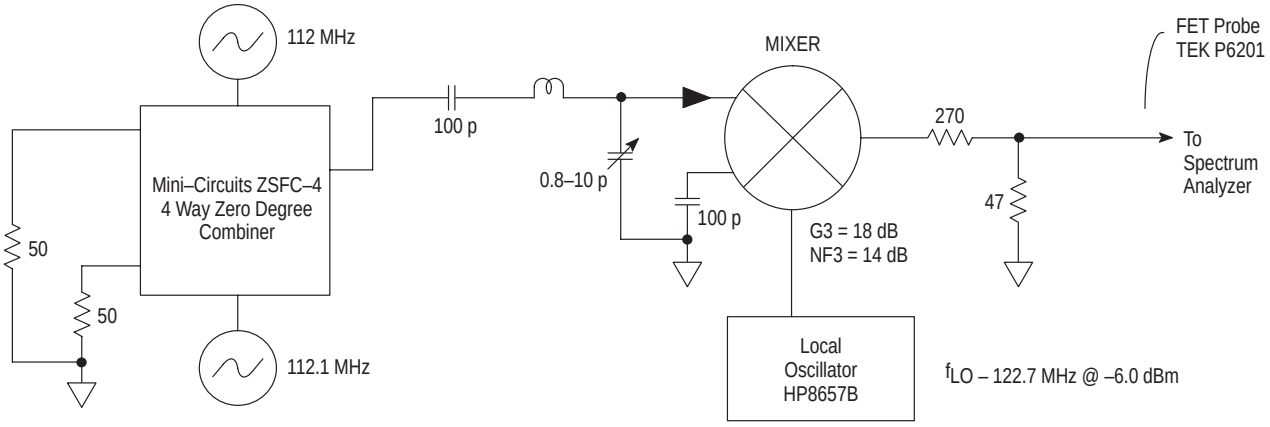


Figure 28. –1.0 dB Compression Pt. and Input Third Order Intercept

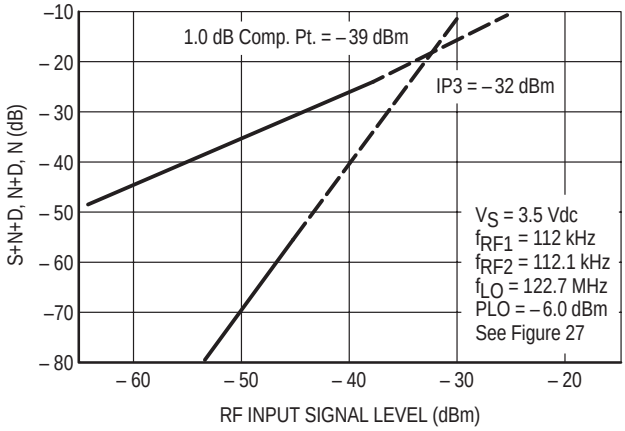


Figure 29. Circuit Side View

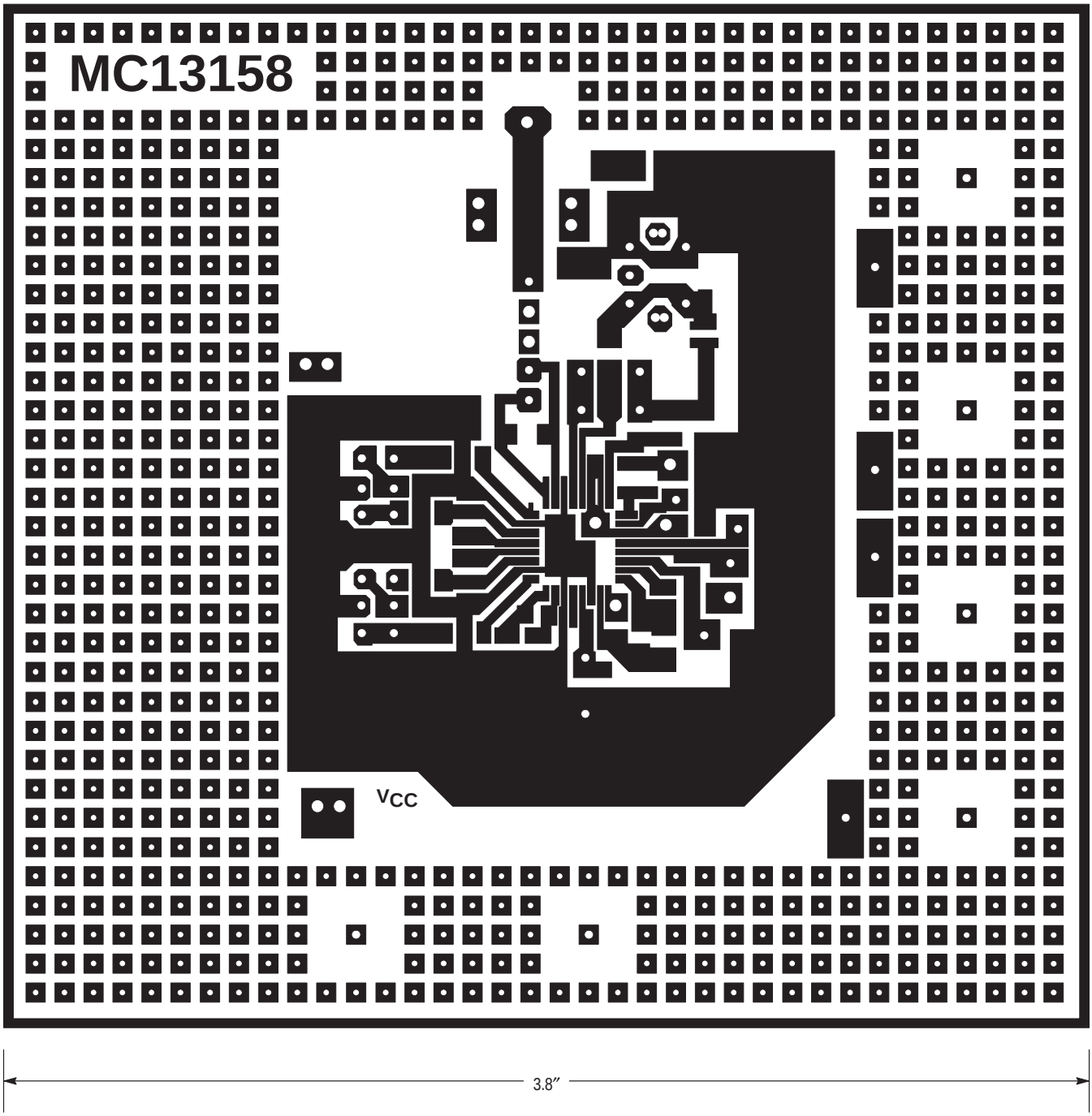
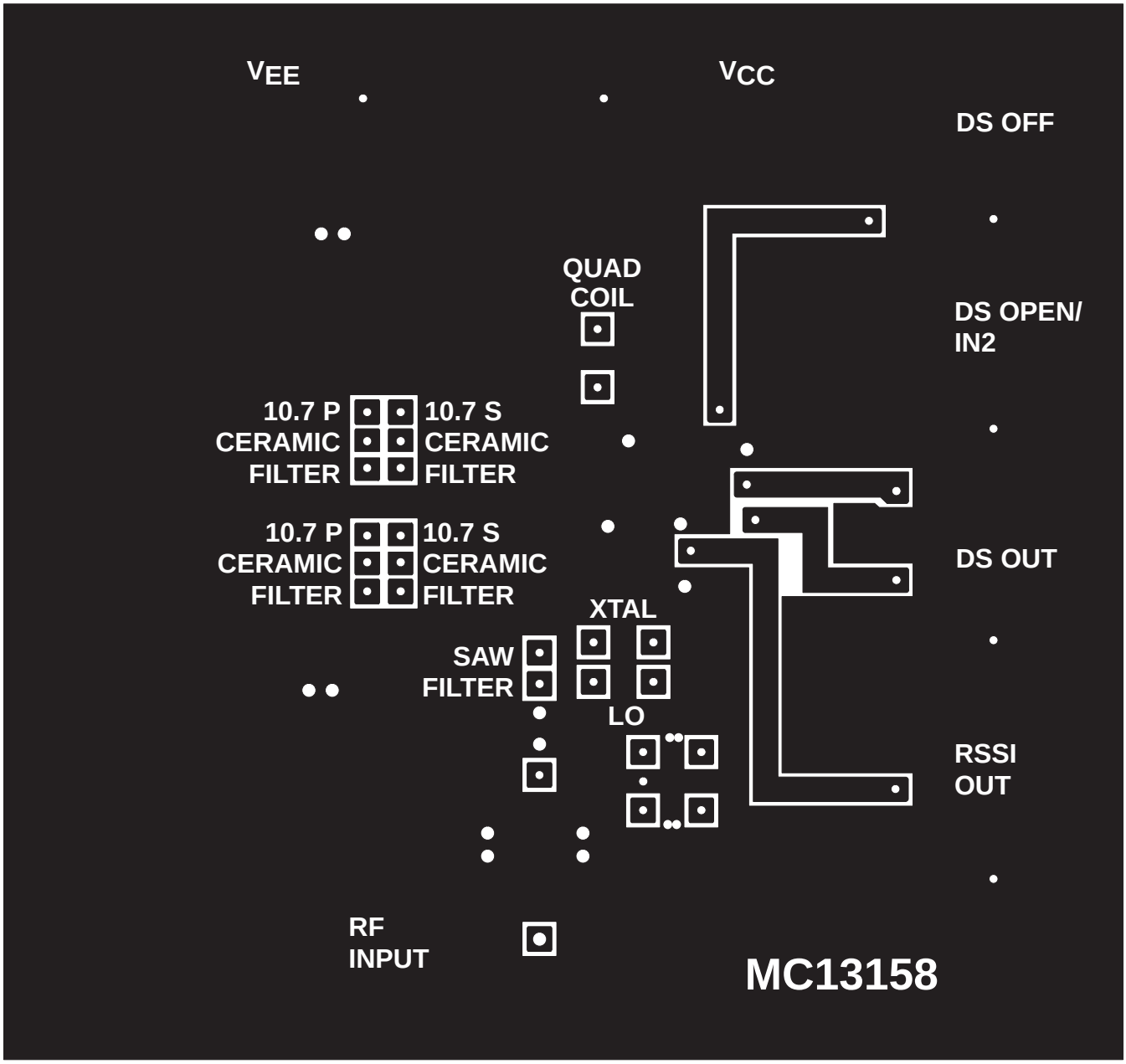


Figure 30. Ground Side View



MOTOROLA

MC13176

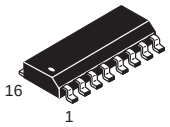
UHF FM/AM Transmitter

The MC13176 is a one chip FM/AM transmitter subsystem designed for AM/FM communication systems. It include a Colpitts crystal reference oscillator, UHF oscillator, ÷32 prescaler and phase detector forming a versatile PLL system. Targeted applications are in the 260 to 470 MHz band and the 902 to 928 MHz band covered by FCC Title 47; Part 15. Other applications include local oscillator sources in UHF and 900 MHz receivers, UHF and 900 MHz video transmitters, RF Local Area Networks (LANs), and high frequency clock drivers. The MC13176 offers the following features:

- UHF Current Controlled Oscillator
- Uses Easily Available 3rd Overtone or Fundamental Crystals for Reference
- Fewer External Parts Required
- Low Operating Supply Voltage (1.8 to 5.0 Vdc)
- Low Supply Drain Currents
- Power Output Adjustable (Up to 10 dBm)
- Differential Output for Loop Antenna or Balun Transformer Networks
- Power Down Feature
- ASK Modulated by Switching Output On and Off
- $f_o = 32 \times f_{ref}$

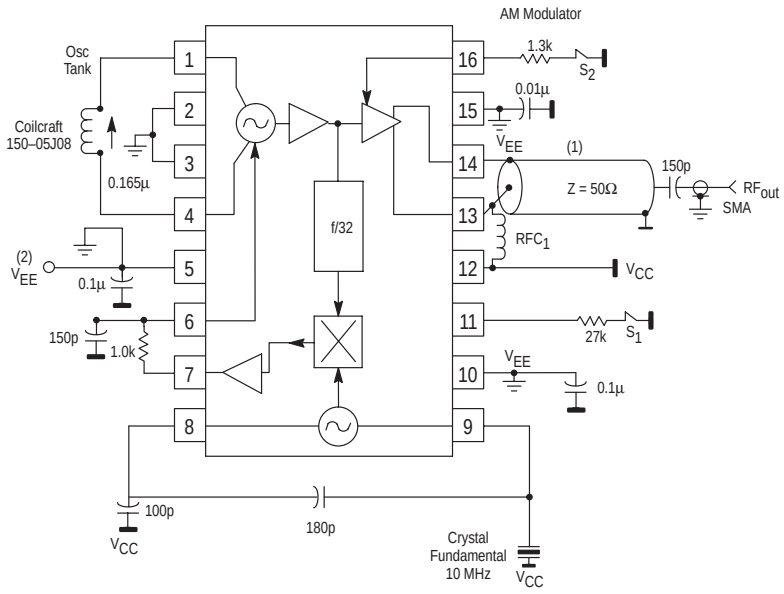
UHF FM/AM TRANSMITTER

SEMICONDUCTOR TECHNICAL DATA



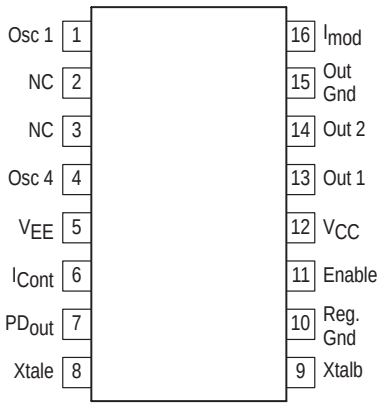
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Figure 1. Typical Application as 320 MHz AM Transmitter



NOTES: 1. 50 Ω coaxial balun, 1/10 wavelength at 320 MHz equals 1.5 inches.
2. Pins 5, 10 & 15 are ground and connected to V_{EE} which is the component/DC ground plane side of PCB. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13176D	T_A = – 40 to 85°C	SO–16

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

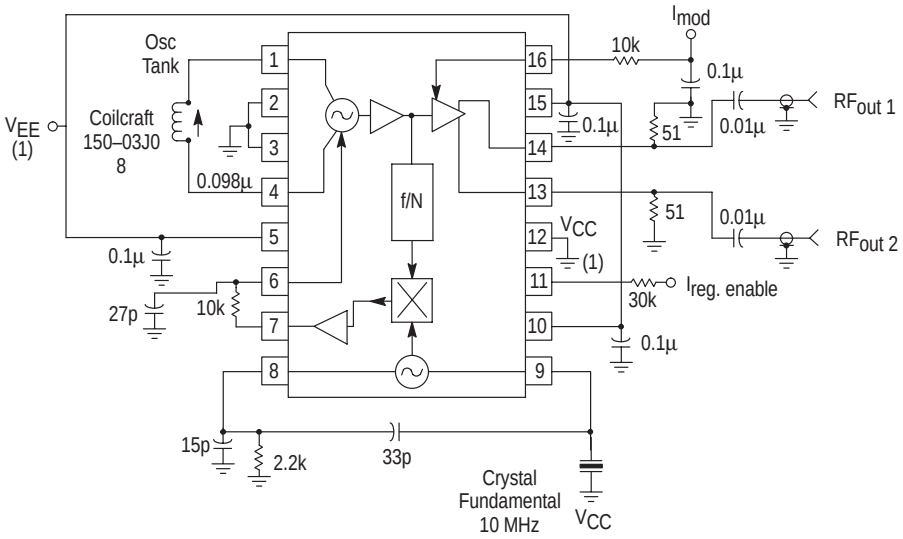
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0 (max)	Vdc
Operating Supply Voltage Range	V_{CC}	1.8 to 5.0	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	–40 to 85	°C
Storage Temperature	T_{stg}	–65 to 150	°C

ELECTRICAL CHARACTERISTICS (Figure 2; V_{EE} = – 3.0 Vdc, T_A = 25°C, unless otherwise noted.)*

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Supply Current (Power down: I_{11} & I_{16} = 0)	–	I_{EE1}	–0.5	–	–	µA
Supply Current (Enable [Pin 11] to V_{CC} thru 30 k, I_{16} = 0)	–	I_{EE2}	–18	–14	–	mA
Total Supply Current (Transmit Mode) (I_{mod} = 2.0 mA; f_o = 320 MHz)	–	I_{EE3}	– 39	–34	–	mA
Differential Output Power (f_o = 320 MHz; V_{ref} [Pin 9] = 500 $mV_{p–p}$; f_o = N x f_{ref}) I_{mod} = 2.0 mA (see Figure 7) I_{mod} = 0 mA	13 & 14	P_{out}	 2.0 –	 4.7 –45	 – –	dBm
Hold–in Range (± Δf_{ref} x N) (see Figure 7)	13 & 14	± Δf_H	4.0	8.0	–	MHz
Phase Detector Output Error Current	7	I_{error}	22	27	–	µA
Oscillator Enable Time (see Figure 26)	11 & 8	t_{enable}	–	4.0	–	ms
Amplitude Modulation Bandwidth (see Figure 28)	16	BW_{AM}	–	25	–	MHz
Spurious Outputs (I_{mod} = 2.0 mA) Spurious Outputs (I_{mod} = 0 mA)	13 & 14 13 & 14	P_{son} P_{soff}	– –	–50 –50	– –	dBc
Maximum Divider Input Frequency Maximum Output Frequency	– 13 & 14	f_{div} f_o	– –	950 950	– –	MHz

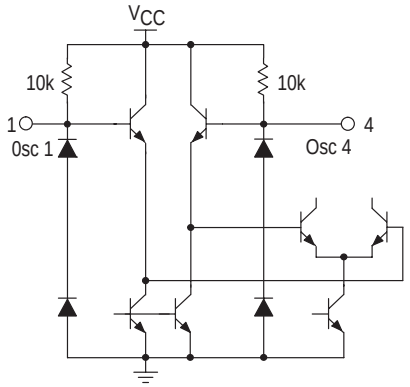
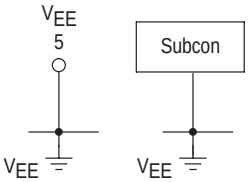
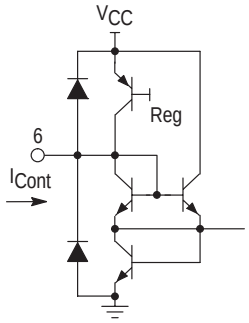
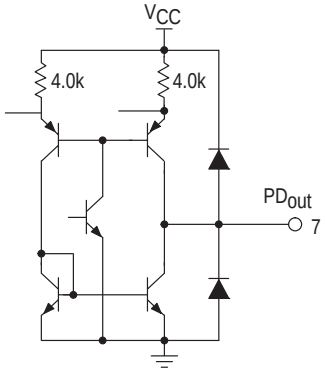
* For testing purposes, V_{CC} is ground (see Figure 2).

Figure 2. 320 MHz Test Circuit



NOTES: 1. V_{CC} is ground; while V_{EE} is negative with respect to ground.
2. Pins 5, 10 and 15 are brought to the circuit side of the PCB via plated through holes.
They are connected together with a trace on the PCB and each Pin is decoupled to V_{CC} (ground).

PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
1 & 4	Osc 1, Osc 4		**CCO Inputs** The oscillator is a current controlled type. An external oscillator coil is connected to Pins 1 and 4 which forms a parallel resonance LC tank circuit with the internal capacitance of the IC and with parasitic capacitance of the PC board. Three base–emitter capacitances in series configuration form the capacitance for the parallel tank. These are the base–emitters at Pins 1 and 4 and the base–emitter of the differential amplifier. The equivalent series capacitance in the differential amplifier is varied by the modulating current from the frequency control circuit (see Pin 6, internal circuit). A more thorough discussion is found in the Applications Information section.
5	V_{EE}		**Supply Ground (V_{EE})** In the PCB layout, the ground pins (also applies to Pins 10 and 15) should be connected directly to chassis ground. Decoupling capacitors to V_{CC} should be placed directly at the ground returns.
6	I_{Cont}		**Frequency Control** For V_{CC} = 3.0 Vdc, the voltage at Pin 6 is approximately 1.55 Vdc. The oscillator is current controlled by the error current from the phase detector. This current is amplified to drive the current source in the oscillator section which controls the frequency of the oscillator. Figures 8 and 9 show the Δf_{osc} versus I_{Cont}, Figure 5 shows the Δf_{osc} versus I_{Cont} at – 40°C, + 25°C and + 85°C for 320 MHz. The CCO may be FM modulated as shown in Figures 17 and 18, MC13176 320 MHz FM Transmitter. A detailed discussion is found in the Applications Information section.
7	PD_{out}		**Phase Detector Output** The phase detector provides ± 30 μA to keep the CCO locked at the desired carrier frequency. The output impedance of the phase detector is approximately 53 kΩ. Under closed loop conditions there is a DC voltage which is dependent upon the free running oscillator and the reference oscillator frequencies. The circuitry between Pins 7 and 6 should be selected for adequate loop filtering necessary to stabilize and filter the loop response. Low pass filtering between Pin 7 and 6 is needed so that the corner frequency is well below the sum of the divider and the reference oscillator frequencies, but high enough to allow for fast response to keep the loop locked. Refer to the Applications Information section regarding loop filtering and FM modulation.

PIN FUNCTION DESCRIPTIONS

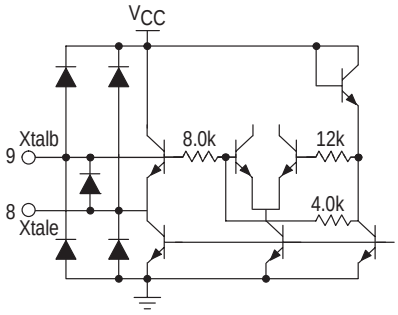
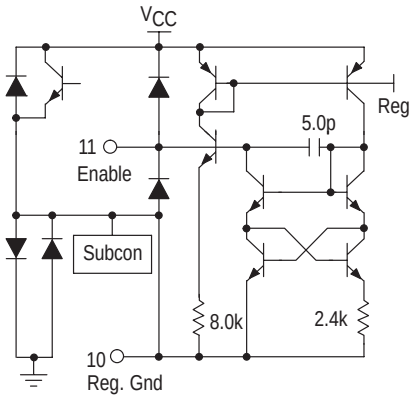
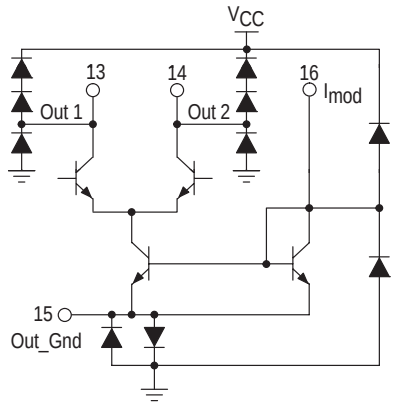
Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
8	Xtale		**Crystal Oscillator Inputs** The internal reference oscillator is configured as a common emitter Colpitts. It may be operated with either a fundamental or overtone crystal depending on the carrier frequency and the internal prescaler. Crystal oscillator circuits and specifications of crystals are discussed in detail in the applications section. With V_{CC} = 3.0 Vdc, the voltage at Pin 8 is approximately 1.8 Vdc and at Pin 9 is approximately 2.3 Vdc. 500 to 1000 mVp–p should be present at Pin 9. The Colpitts is biased at 200 μA; additional drive may be acquired by increasing the bias to approximately 500 μA. Use 6.2 k from Pin 8 to ground.
9	Xtalb		
10	Reg. Gnd		**Regulator Ground** An additional ground pin is provided to enhance the stability of the system. Decoupling to the V_{CC} (RF ground) is essential; it should be done at the ground return for Pin 10. **Device Enable** The potential at Pin 11 is approximately 1.25 Vdc. When Pin 11 is open, the transmitter is disabled in a power down mode and draws less than 1.0 μA I_{CC} if the MOD at Pin 16 is also open (i.e., it has no current driving it). To enable the transmitter a current source of 10 μA to 90 μA is provided. Figures 3 and 4 show the relationship between I_{CC}, V_{CC} and $I_{reg.\ enable}$. Note that I_{CC} is flat at approximately 10 mA for $I_{reg.\ enable}$ = 5.0 to 100 μA (I_{mod} = 0).
11	Enable		
12	V_{CC}		**Supply Voltage (V_{CC})** The operating supply voltage range is from 1.8 Vdc to 5.0 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as possible to minimize inductive reactances along the trace; it is best to have it completely fill around the surface mount components and traces on the circuit side of the PCB.
13 & 14	Out 1 and Out 2		**Differential Output** The output is configured differentially to easily drive a loop antenna. By using a transformer or balun, as shown in the application schematic, the device may then drive an unbalanced low impedance load. Figure 6 shows how much the Output Power and Free–Running Oscillator Frequency change with temperature at 3.0 Vdc; I_{mod} = 2.0 mA. **Output Ground** This additional ground pin provides direct access for the output ground to the circuit board V_{EE}. **AM Modulation/Power Output Level** The DC voltage at this pin is 0.8 Vdc with the current source active. An external resistor is chosen to provide a source current of 1.0 to 3.0 mA, depending on the desired output power level at a given V_{CC}. Figure 27 shows the relationship of Power Output to Modulation Current, I_{mod}. At V_{CC} = 3.0 Vdc, 3.5 dBm power output can be acquired with about 35 mA I_{CC}. For FM modulation, Pin 16 is used to set the desired output power level as described above. For AM modulation, the modulation signal must ride on a positive DC bias offset which sets a static (modulation off) modulation current. External circuitry for various schemes is further discussed in the Applications Information section.
15	Out_Gnd		
16	I_{mod}		

Figure 3. Supply Current versus Supply Voltage

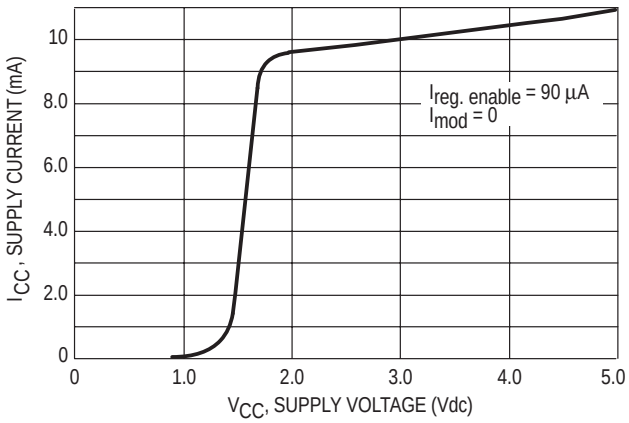


Figure 4. Supply Current versus Regulator Enable Current

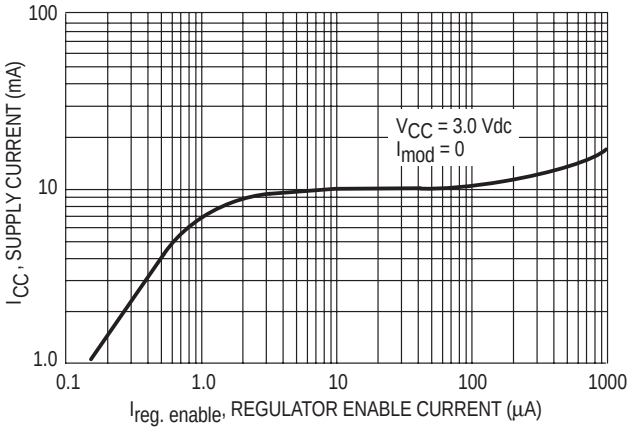


Figure 5. Change Oscillator Frequency versus Oscillator Control Current

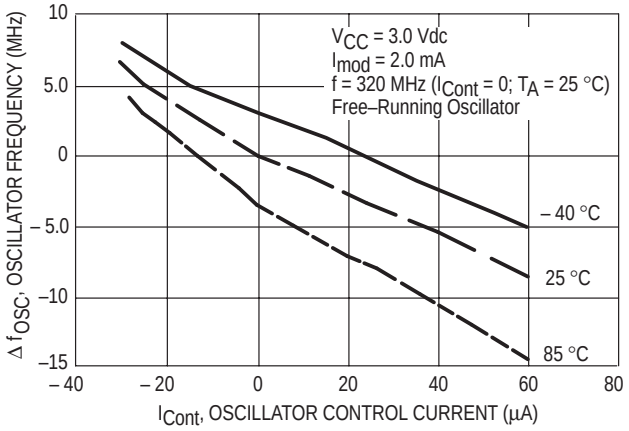


Figure 6. Change in Oscillator Frequency and Output Power versus Ambient Temperature

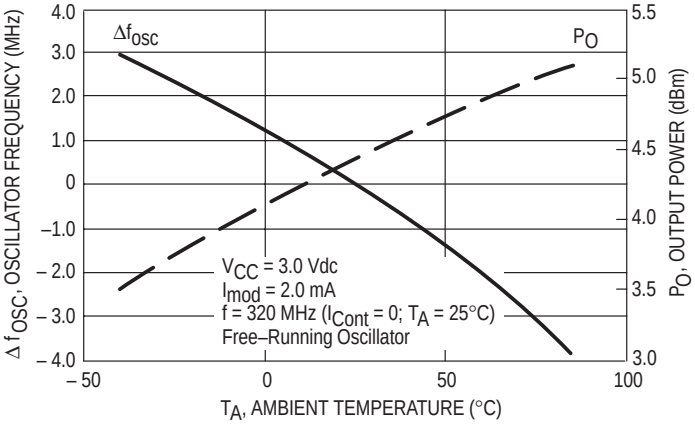


Figure 7. Reference Oscillator Frequency versus Phase Detector Current

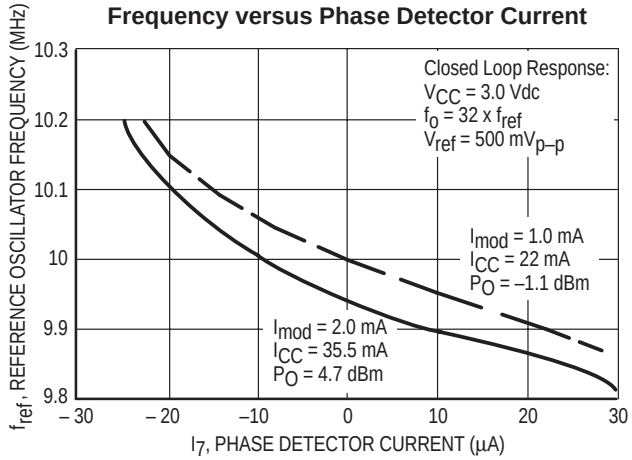


Figure 8. Change in Oscillator Frequency versus Oscillator Control Current

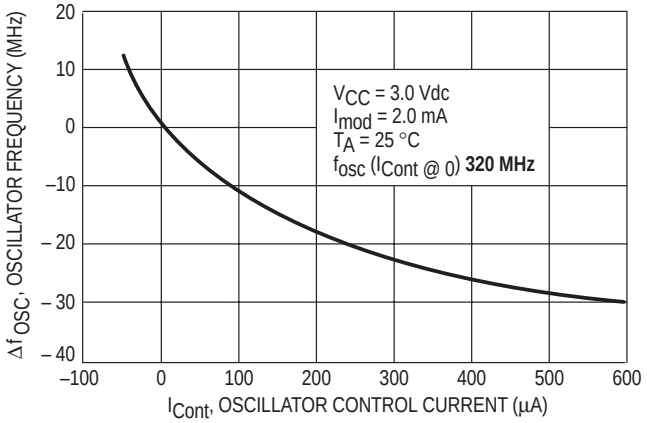
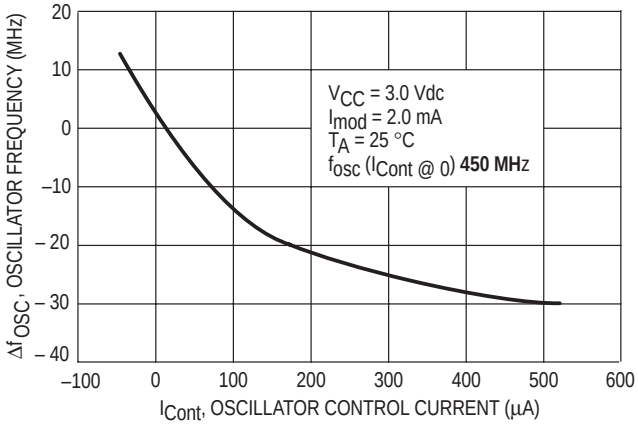


Figure 9. Change in Oscillator Frequency versus Oscillator Control Current



APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB, shown in Figures 32 and 33, is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side of the PCB (see Figures 34 and 35). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Current Controlled Oscillator (Pins 1 to 4)

It is critical to keep the interconnect leads from the CCO (Pins 1 and 4) to the external inductor symmetrical and equal in length. With a minimum inductor, the maximum free running frequency is greater than 1.0 GHz. Since this inductor will be small, it may be either a microstrip inductor, an air wound inductor or a tuneable RF coil. An air wound inductor may be tuned by spreading the windings, whereas tuneable RF coils are tuned by adjusting the position of an aluminum core in a threaded coilform. As the aluminum core coupling to the windings is increased, the inductance is decreased. The temperature coefficient using an aluminum core is better than a ferrite core. The UniCoil™ inductors made by Coilcraft may be obtained with aluminum cores (Part No. 51–129–169).

Ground (Pins 5, 10 and 15)

Ground Returns: It is best to take the grounds to a backside ground plane via plated through holes or eyelets at the pins. The application PCB layout implements this technique. Note that the grounds are located at or less than 100 mils from the devices pins.

Decoupling: Decoupling each ground pin to V_{CC} isolates each section of the device by reducing interaction between sections and by localizing circulating currents.

Loop Characteristics (Pins 6 and 7)

Figure 10 is the component block diagram of the MC13176D PLL system where the loop characteristics are described by the gain constants. Access to individual components of this PLL system is limited, inasmuch as the loop is only pinned out at the phase detector output and the frequency control input for the CCO. However, this allows for characterization of the gain constants of these loop components. The gain constants K_p, K_o and K_n are well defined in the MC13176.

Phase Detector (Pin 7)

With the loop in lock, the difference frequency output of the phase detector is DC voltage that is a function of the phase difference. The sinusoidal type detector used in this IC has the following transfer characteristic:

$$I_e = A \sin \theta_e$$

The gain factor of the phase detector, K_p (with the loop in lock) is specified as the ratio of DC output current, I_e to phase error, θ_e:

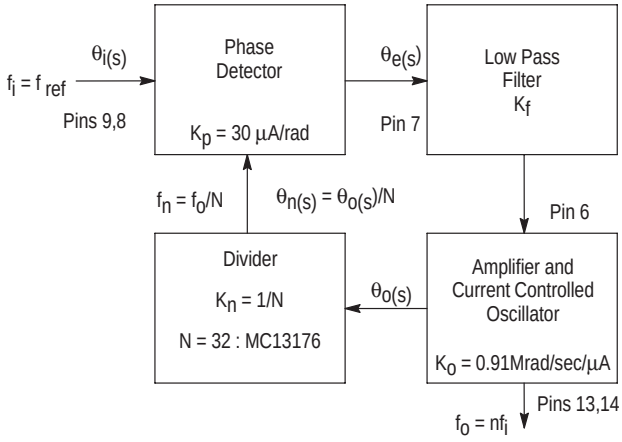
$K_p = I_e/\theta_e$ (Amps/radians)
$K_p = A \sin \theta_e/\theta_e$
$\sin \theta_e \sim \theta_e$ for $\theta_e \leq 0.2$ radians;
thus, $K_p = A$ (Amps/radians)

Figure 7 shows that the detector DC current is approximately 30 μA where the loop loses lock at $\theta_e = \pm \pi/2$ radians; therefore, K_p is 30 μA/radians.

Current Controlled Oscillator, CCO (Pin 6)

Figures 8 and 9 show the non–linear change in frequency of the oscillator over an extended range of control current for 320 and 450 MHz applications. K_o ranges from approximately 6.3×10^5 rad/sec/μA or 100 kHz/μA (Figure 8) to 8.8×10^5 rad/sec/μA or 140 kHz/μA (Figure 9) over a relatively linear response of control current (0 to 100 μA). The oscillator gain factor depends on the operating range of the control current (i.e., the slope is not constant). Included in the CCO gain factor is the internal amplifier which can sink and source at least 30 μA of input current from the phase detector. The internal circuitry at Pin 6 limits the CCO control current to 50 μA of source capability while its sink capability exceeds 200 μA as shown in Figures 8 and 9. Further information to follow shows how to use the full capabilities of the CCO by addition of an external loop amplifier and filter (see Figure 14). This additional circuitry yields at K_o = 0.145 MHz/μA or 9.1×10^5 rad/sec/μA.

Figure 10. Block Diagram of MC1317XD PLL



Where: K_p = Phase detector gain constant in μA/rad; K_p = 30 μA/rad
K_f = Filter transfer function
K_n = 1/N; N = 32
K_o = CCO gain constant in rad/sec/μA

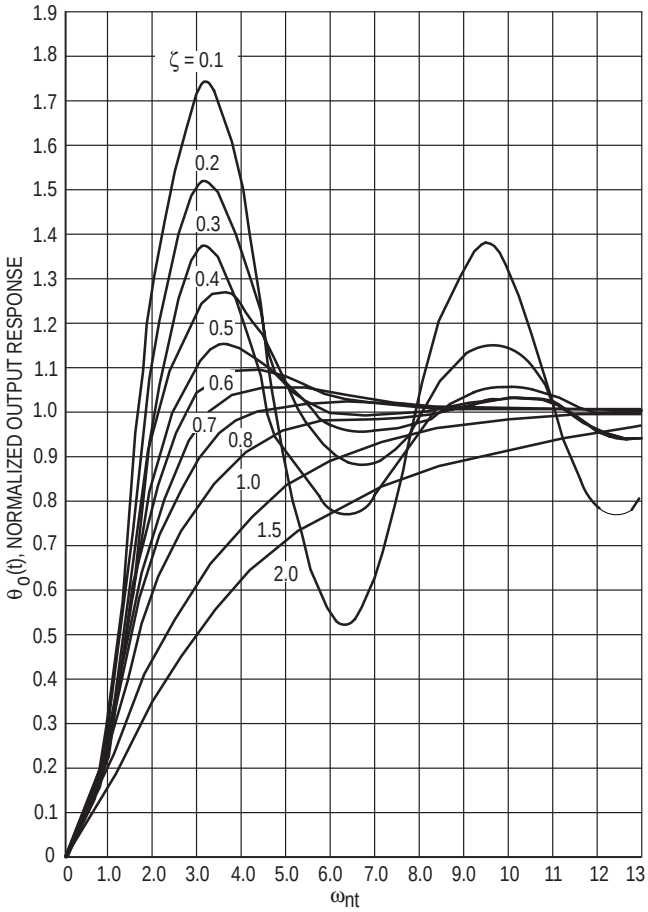
$K_o = 9.1 \times 10^5$ rad/sec/μA

Loop Filtering

The fundamental loop characteristics, such as capture range, loop bandwidth, lock–up time and transient response are controlled externally by loop filtering.

The natural frequency (ω_n) and damping factor (∂) are important in the transient response to a step input of phase or frequency. For a given ∂ and lock time, ω_n can be determined from the plot shown in Figure 11.

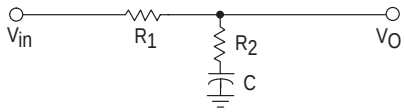
Figure 11. Type 2 Second Order Response



For ∂ = 0.707 and lock time = 1.0 ms;
then ω_n = 5.0/t = 5.0 krad/sec.

The loop filter may take the form of a simple low pass filter or a lag–lead filter which creates an additional pole at origin in the loop transfer function. This additional pole along with that of the CCO provides two pure integrators ($1/s^2$). In the lag–lead low pass network shown in Figure 12, the values of the low pass filtering parameters R_1, R_2 and C determine the loop constants ω_n and ∂. The equations $t_1 = R_1C$ and $t_2 = R_2C$ are related in the loop filter transfer functions $F(s) = 1 + t_2s/1 + (t_1 + t_2)s$.

Figure 12. Lag–Lead Low Pass Filter



The closed loop transfer function takes the form of a 2nd order low pass filter given by,

$$H(s) = K_vF(s)/s + K_vF(s)$$

From control theory, if the loop filter characteristic has F(0) = 1, the DC gain of the closed loop, K_v is defined as,

$$K_v = K_pK_oK_n$$

and the transfer function has a natural frequency,

$$\omega_n = (K_v/t_1 + t_2)^{1/2}$$

and a damping factor,

$$\partial = (\omega_n/2)\ (t_2 + 1/K_v)$$

Rewriting the above equations and solving for the MC13176 with ∂ = 0.707 and ω_n = 5.0 k rad/sec:

$K_v = K_pK_oK_n = (30)\ (0.91 \times 10^6)\ (1/32) = 0.853 \times 10^6$
$t_1 + t_2 = K_v/\omega_n2 = 0.853 \times 10^6/(25 \times 106) = 34.1$ ms
$t_2 = 2\partial/\omega_n = (2)\ (0.707)/(5 \times 10^3) = 0.283$ ms
$t_1 = (K_v/\omega_n2) - t_2 = (34.1 - 0.283) = 33.8$ ms

For C = 0.47 μ;

then, $R_1 = t_1/C = 33.8 \times 10^{-3}/0.47 \times 10^{-6} = 72$ k

dthus, $R_2 = t_2/C = 0.283 \times 10^{-3}/0.47 \times 10^{-6} = 0.60$ k

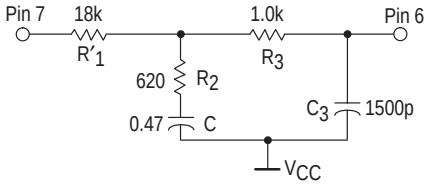
In the above example, the following standard value components are used,

C = 0.47 μ; R_2 = 620 and R'_1 = 72 k – 53 k ~ 18 k

(R'_1 is defined as R_1 – 53 k, the output impedance of the phase detector.)

Since the output of the phase detector is high impedance (~50 k) and serves as a current source, and the input to the frequency control, Pin 6 is low impedance (impedance of the two diode to ground is approximately 500 Ω), it is imperative that the second order low pass filter design above be modified. In order to minimize loading of the R_2C shunt network, a higher impedance must be established to Pin 6. A simple solution is achieved by adding a low pass network between the passive second order network and the input to Pin 6. This helps to minimize the loading effects on the second order low pass while further suppressing the sideband spurs of the crystal oscillator. A low pass filter with R_3 = 1.0 k and C_2 = 1500 p has a corner frequency (f_c) of 106 kHz; the reference sideband spurs are down greater than – 60 dBc.

Figure 13. Modified Low Pass Loop Filter



Hold–In Range

The hold–in range, also called the lock range, tracking range and synchronization range, is the ability of the CCO frequency, f_o to track the input reference signal, $f_{ref} \bullet N$ as it gradually shifted away from the free running frequency, f_f. Assuming that the CCO is capable of sufficient frequency deviation and that the internal loop amplifier and filter are not overdriven, the CCO will track until the phase error, θ_e approaches $\pm\pi/2$ radians. Figures 5 through 7 are a direct measurement of the hold–in range (i.e. $\Delta f_{ref} \times N = \pm\Delta f_H \times 2\pi$). Since sin θ_e cannot exceed ±1.0, as θ_e approaches $\pm\pi/2$ the hold–in range is equal to the DC loop gain, $K_v \times N$.

$$\pm\Delta\omega_H = \pm K_v \times N$$

where, $K_v = K_p K_o K_n$.

In the above example,

$$\pm\Delta\omega_H = \pm 27.3 \text{ Mrad/sec}$$
$$\pm\Delta f_H = \pm 4.35 \text{ MHz}$$

Extended Hold–in Range

The hold–in range of about 3.4% could cause problems over temperature in cases where the free–running oscillator drifts more than 2 to 3% because of relatively high temperature coefficients of the ferrite tuned CCO inductor. This problem might worsen for lower frequency applications where the external tuning coil is large compared to internal capacitance at Pins 1 and 4. To improve hold–in range performance, it is apparent that the gain factors involved must be carefully considered.

K_n = is 1/32 in the MC13176.

K_p = is fixed internally and cannot be altered.

K_o = Figures 8 and 9 suggest that there is capability of greater control range with more current swing. However, this swing must be symmetrical about the center of the dynamic response. The suggested zero current operating point for ±100 μA swing of the CCO is at about + 70 μA offset point.

Ka = External loop amplification will be necessary since the phase detector only supplies ± 30 μA.

In the design example in Figure 14, an external resistor (R_5) of 15 k to V_{CC} (3.0 Vdc) provides approximately 100 μA of current boost to supplement the existing 50 μA internal source current. R_4 (1.0 k) is selected for approximately 0.1 Vdc across it with 100 μA. R_1, R_2 and R_3 are selected to set the potential at Pin 7 and the base of 2N4402 at approximately 0.9 Vdc and the emitter at 1.55 Vdc when error current to Pin 6 is approximately zero μA. C_1 is chosen to reduce the level of the crystal sidebands.

Figure 14. External Loop Amplifier

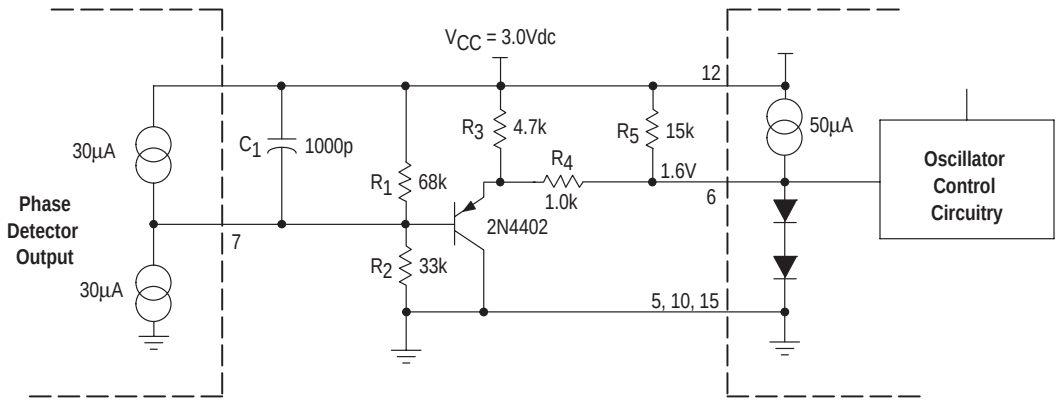
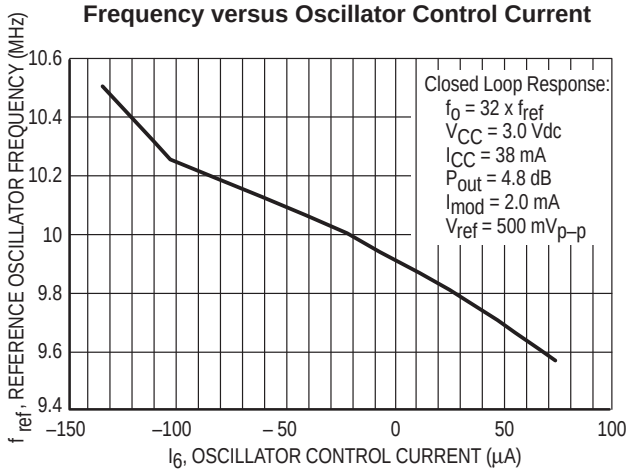


Figure 15 shows the improved hold–in range of the loop. The Δf_{ref} is moved 950 kHz with over 200 μA swing of control current for an improved hold–in range of ±15.2 MHz or ± 95.46 Mrad/sec.

Figure 15. MC13176 Reference Oscillator Frequency versus Oscillator Control Current



Lock–in Range/Capture Range

If a signal is applied to the loop not equal to free running frequency, f_f, then the loop will capture or lock–in the signal by making $f_S = f_O$ (i.e. if the initial frequency difference is not too great). The lock–in range can be expressed as $\Delta\omega_L \sim \pm 2\partial\omega_n$

FM Modulation

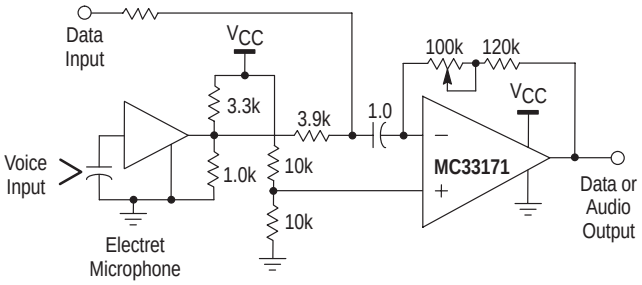
Noise external to the loop (phase detector input) is minimized by narrowing the bandwidth. This noise is minimal in a PLL system since the reference frequency is usually derived from a crystal oscillator. FM can be achieved by applying a modulation current superimposed on the control current of the CCO. The loop bandwidth must be narrow enough to prevent the loop from responding to the modulation frequency components, thus, allowing the CCO to deviate in frequency. The loop bandwidth is related to the natural frequency ω_n. In the lag–lead design example where the natural frequency, ω_n = 5.0 krad/sec and a damping factor, ∂ = 0.707, the loop bandwidth = 1.64 kHz. Characterization data of the closed loop responses at 320 MHz (Figure 7) show satisfactory performance using only a simple low–pass loop filter network. The loop filter response is strongly influenced by the high output impedance of the push–pull current output of the phase detector.

f_c = 0.159/RC;
For R = 1.0 k + R_7 (R_7 = 53 k) and C = 390 pF
f_c = 7.55 kHz or ω_c = 47 krad/sec

The application example in Figure 17 of a 320 MHz FM transmitter demonstrates the FM capabilities of the IC. A high value series resistor (100 k) to Pin 6 sets up the current source to drive the modulation section of the chip. Its value is dependent on the peak to peak level of the encoding data and the maximum desired frequency deviation. The data input is AC coupled with a large coupling capacitor which is selected for the modulating frequency. The component placements on the circuit side and ground side of the PC board are shown in Figures 34 and 35, respectively. Figure 19 illustrates the input data of a 10 kHz modulating signal at 1.6 Vp–p. Figures 20 and 21 depict the deviation and resulting modulation spectrum showing the carrier null at – 40 dBc. Figure 22 shows the unmodulated carrier power output at 3.5 dBm for V_{CC} = 3.0 Vdc.

For voice applications using a dynamic or an electret microphone, an op amp is used to amplify the microphone's low level output. The microphone amplifier circuit is shown in Figure 16. Figure 18 shows an application example for NBFM audio or direct FSK in which the reference crystal oscillator is modulated.

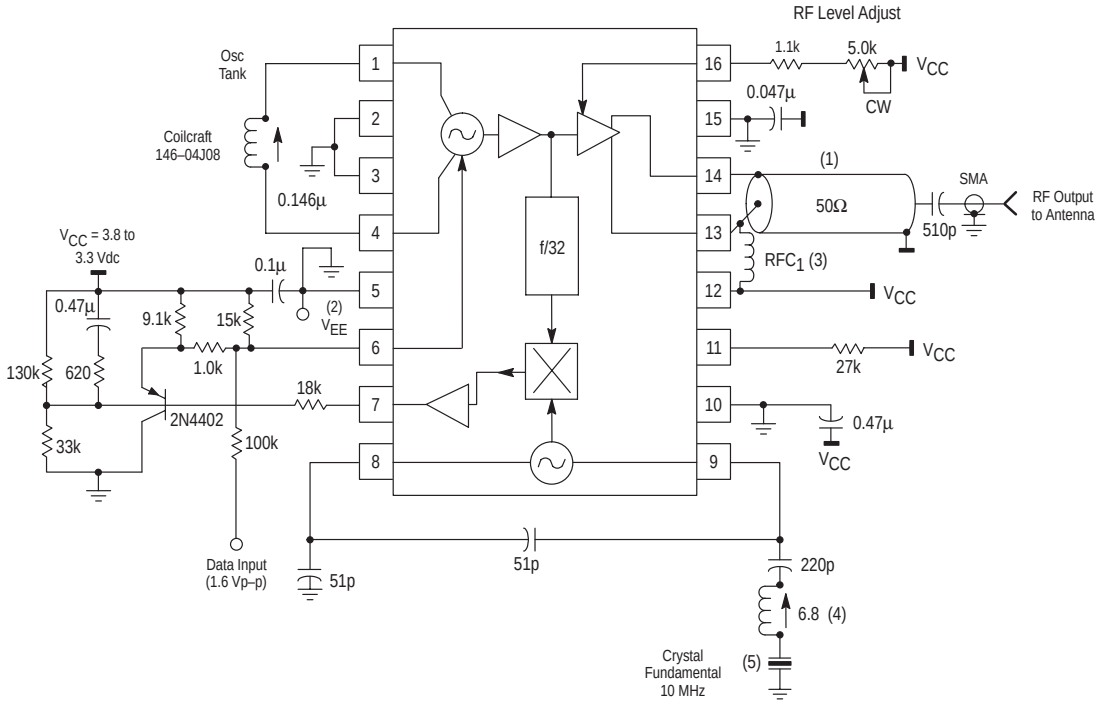
Figure 16. Microphone Amplifier



Local Oscillator Application

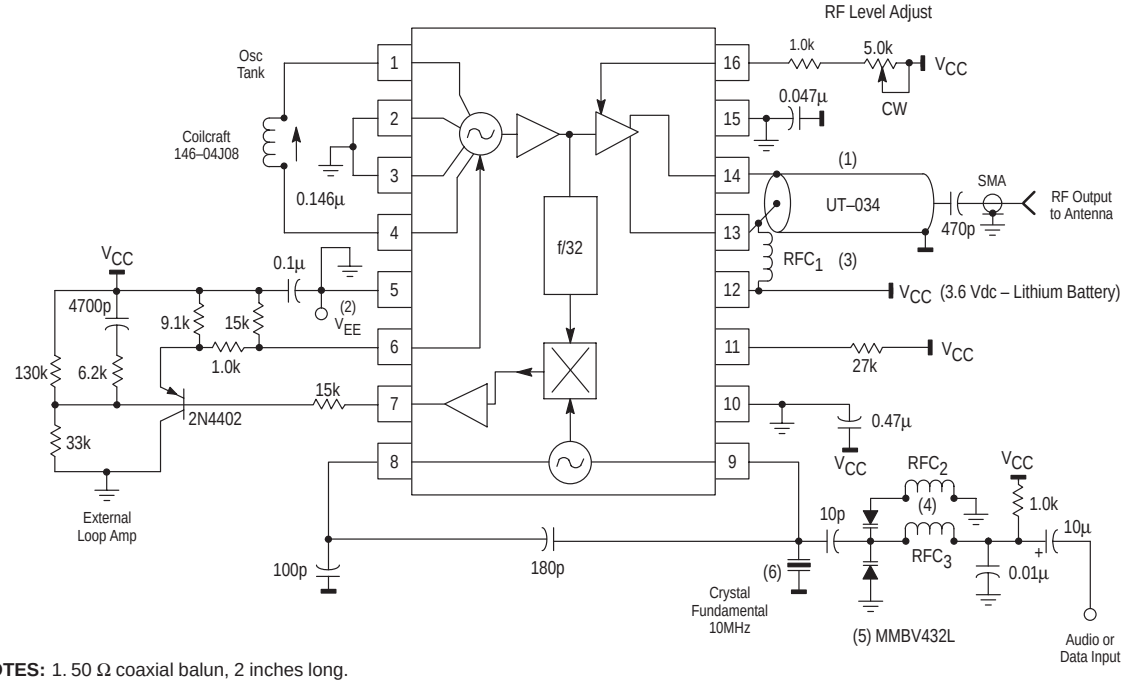
To reduce internal loop noise, a relatively wide loop bandwidth is needed so that the loop tracks out or cancels the noise. This is emphasized to reduce inherent CCO and divider noise or noise produced by mechanical shock and environmental vibrations. In a local oscillator application the CCO and divider noise should be reduced by proper selection of the natural frequency of the loop. Additional low pass filtering of the output will likely be necessary to reduce the crystal sideband spurs to a minimal level.

Figure 17. 320 MHz MC13176D FM Transmitter



NOTES: 1. 50 Ω coaxial balun, 2 inches long.
2. Pins 5, 10 and 15 are grounds and connnected to V_{EE} which is the component's side ground plane. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.
3. RFC_1 is 180 nH Coilcraft surface mount inductor or 190 nH Coilcraft 146–05J08.
4. Recommended source is a Coilcraft "slot seven" 7.0 mm tuneable inductor, part #7M3–682.
5. The crystal is a parallel resonant, fundamental mode calibrated with 32 pF load capacitance.

Figure 18. 320 MHz NBFM Transmitter



NOTES: 1. 50 Ω coaxial balun, 2 inches long.
2. Pins 5, 10 and 15 are grounds and connnected to V_{EE} which is the component's side ground plane. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.
3. RFC_1 is 180 nH Coilcraft surface mount inductor.
4. RFC_2 and RFC_3 are high impedance crystal frequency of 10 MHz; 8.2 µH molded inductor gives XL > 1000 Ω..
5. A single varactor like the MV2105 may be used whereby RFC_2 is not needed.
6. The crystal is a parallel resonant, fundamental mode calibrated with 32 pF load capacitance.

Figure 19. Input Data Waveform

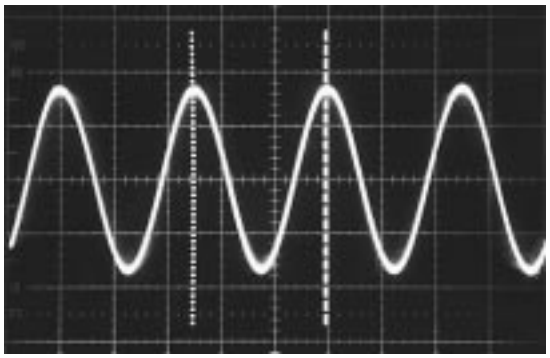


Figure 20. Frequency Deviation

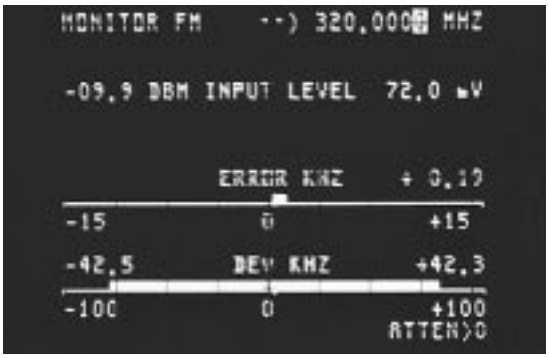


Figure 21. Modulation Spectrum

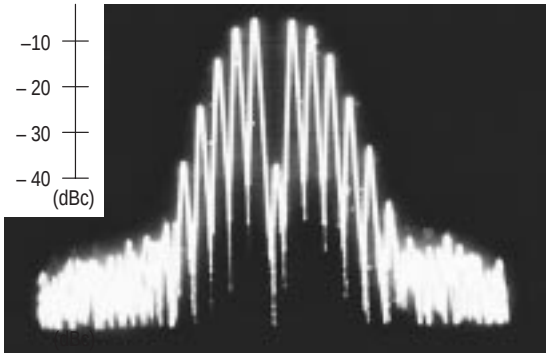
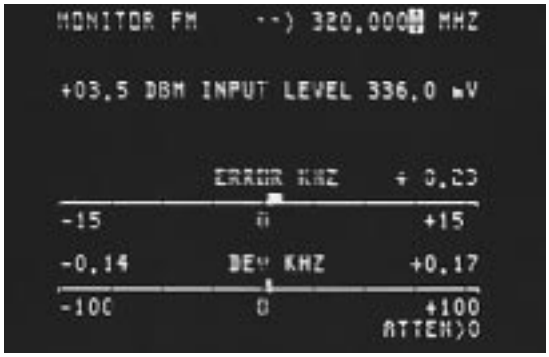


Figure 22. Unmodulated Carrier



Reference Crystal Oscillator (Pins 8 and 9)

Selection of Proper Crystal: A crystal can operate in a number of mechanical modes. The lowest resonant frequency mode is its fundamental while higher order modes are called overtones. At each mechanical resonance, a crystal behaves like a RLC series–tuned circuit having a large inductor and a high Q. The inductor L_S is series resonance with a dynamic capacitor, C_S determined by the elasticity of the crystal lattice and a series resistance R_S, which accounts for the power dissipated in heating the crystal. This series RLC circuit is in parallel with a static capacitance, C_p which is created by the crystal block and by the metal plates and leads that make contact with it.

Figure 23 is the equivalent circuit for a crystal in a single resonant mode. It is assumed that other modes of resonance are so far off frequency that their effects are negligible.

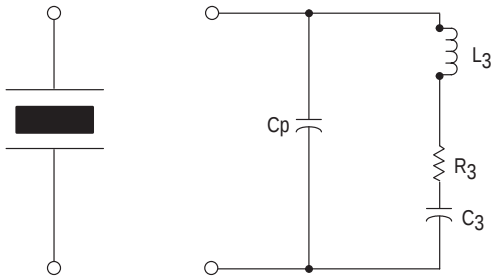
Series resonant frequency, f_S is given by;

$$f_S = 1/2\pi(L_S C_S)^{1/2}$$

and parallel resonant frequency, f_p is given by;

$$f_p = f_S(1 + C_S/C_p)^{1/2}$$

Figure 23. Crystal Equivalent Circuit



the frequency separation at resonance is given by;

$$\Delta f = f_p – f_S = f_S[1 – (1 + C_S/C_p)^{1/2}]$$

Usually f_p is less than 1% higher than f_S, and a crystal exhibits an extremely wide variation of the reactance with frequency between f_p and f_S. A crystal oscillator circuit is very stable with frequency. This high rate of change of impedance with frequency stabilizes the oscillator, because any significant change in oscillator frequency will cause a large phase shift in the feedback loop keeping the oscillator on frequency.

Manufacturers specify crystal for either series or parallel resonant operation. The frequency for the parallel mode is calibrated with a specified shunt capacitance called a “load capacitance.” The most common value is 30 to 32 pF. If the load capacitance is placed in series with the crystal, the equivalent circuit will be series resonance at the specified parallel–resonant frequency. Frequencies up to 20 MHz use parallel resonant crystal operating in the fundamental mode, while above 20 MHz to about 60 MHz, a series resonant crystal specified and calibrated for operation in the overtone mode is used.

Application Examples

Two types of crystal oscillator circuits are used in the applications circuits: 1) fundamental mode common emitter Colpitts (Figures 1, 17, 18, and 24), and 2) third overtone impedance inversion Colpitts (also Figures 1 and 24).

The fundamental mode common emitter Colpitts uses a parallel resonant crystal calibrated with a 32 pf load capacitance. The capacitance values are chosen to provide excellent frequency stability and output power of > 500 mVp–p at Pin 9. In Figures 1 and 24, the fundamental mode reference oscillator is fixed tuned relying on the repeatability of the crystal and passive network to maintain the frequency, while in the circuit shown in Figures 17 and 18, the oscillator frequency can be adjusted with the variable inductor for the precise operating frequency.

The reference oscillator can be operated as high as 60 MHz with a third overtone crystal. Therefore, it is possible to use the MC13176 up to 950 MHz (based on the maximum capability of the divider network).

Enable (Pin 11)

The enabling resistor at Pin 11 is calculated by:

$$R_{eg.\ enable} = V_{CC} - 1.0\ Vdc / I_{reg.\ enable}$$

From Figure 4, $I_{reg.\ enable}$ is chosen to be 75 μA. So, for a V_{CC} = 3.0 Vdc $R_{reg.\ enable}$ = 26.6 kΩ, a standard value 27 kΩ resistor is adequate.

Layout Considerations

Supply (Pin 12): In the PCB layout, the V_{CC} trace must be kept as wide as possible to minimize inductive reactance along the trace; it is best that V_{CC} (RF ground) completely fills around the surface mounted components and interconnect traces on the circuit side of the board. This technique is demonstrated in the evaluation PC board.

Battery/Selection/Lithium Types

The device may be operated from a 3.0 V lithium battery. Selection of a suitable battery is important. Because one of the major problems for long life battery powered equipment is oxidation of the battery terminals, a battery mounted in a clip–in socket is not advised. The battery leads or contact post should be isolated from the air to eliminate oxide build–up. The battery should have PC board mounting tabs which can be soldered to the PCB. Consideration should be given for the peak current capability of the battery. Lithium batteries have current handling capabilities based on the composition of the lithium compound, construction and the battery size. A 1300 mA/hr rating can be achieved in the cylindrical cell battery. The Rayovac CR2/3A lithium–manganese dioxide battery is a crimp sealed, spiral wound 3.0 Vdc, 1300 mA/hr cylindrical cell with PC board mounting tabs. It is an excellent choice based on capacity and size (1.358″ long by 0.665″ in diameter).

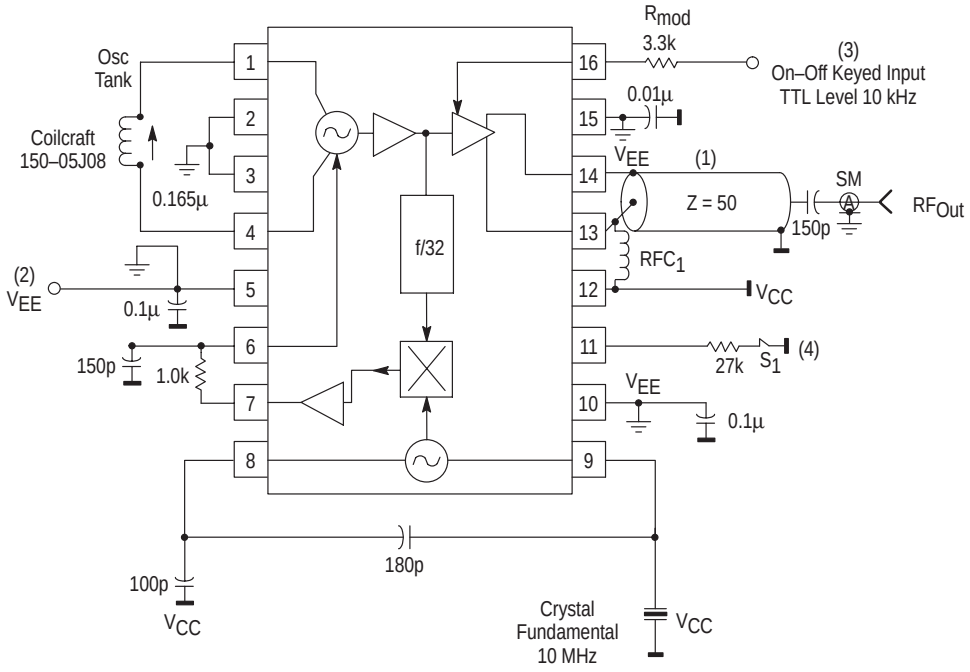
Differential Output (Pins 13, 14)

The availability of micro–coaxial cable and small baluns in surface mount and radial–leaded components allows for simple interface to the output ports. A loop antenna may be directly connected with bias via RFC or 50 Ω resistors. Antenna configuration will vary depending on the space available and the frequency of operation.

AM Modulation (Pin 16)

Amplitude Shift Key: The MC13176 is designed to accommodate Amplitude Shift Keying (ASK). ASK modulation is a form of digital modulation corresponding to AM. The amplitude of the carrier is switched between two or more values in response to the PCM code. For the binary case, the usual choice is On–Off Keying (often abbreviated OOK). The resultant amplitude modulated waveform consists of RF pulses called marks, representing binary 1 and spaces representing binary 0.

Figure 24. ASK 320 MHz Application Circuit



NOTES: 1. 50 Ω coaxial balun, 1/10 wavelength line (1.5″) provides the best match to a 50 Ω load.

2. Pins 5, 10 and 15 are ground and connnected to V_{EE} which is the component/DC ground plane side of PCB. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.

3. The On–Off keyed signal turns the output of the transmitter off and on with TTL level pulses through R_{mod} at Pin 16. The “On” power and I_{CC} is set by the resistor which sets I_{mod} = VTTL – 0.8 / R_{mod}. (see Figure 27).

4. S1 simulates an enable gate pulse from a microprocessor which will enable the transmitter. (see Figure 4 to determine precise value of the enabling resistor based on the potential of the gate pulse and the desired enable.)

Figure 24 shows a typical application in which the output power has been reduced for linearity and current drain. The current draw on the device is 16 mA I_{CC} (average) and – 22.5 dBm (average power output) using a 10 kHz modulating rate for the on–off keying. This equates to 20 mA and – 2.3 dBm “On”, 13 mA and – 41 dBm “Off”. In Figure 25, the device’s modulating waveform and encoded carrier are displayed. The crystal oscillator enable time is needed to set the acquisition timing. It takes typically 4.0 msec to reach full magnitude of the oscillator waveform (see Figure 26, Oscillator Waveform, at Pin 8). A square waveform of 3.0 V peak with a period that is greater than the oscillator enable time is applied to the Enable (Pin 11).

Figure 25. ASK Input Waveform and Modulated Carrier

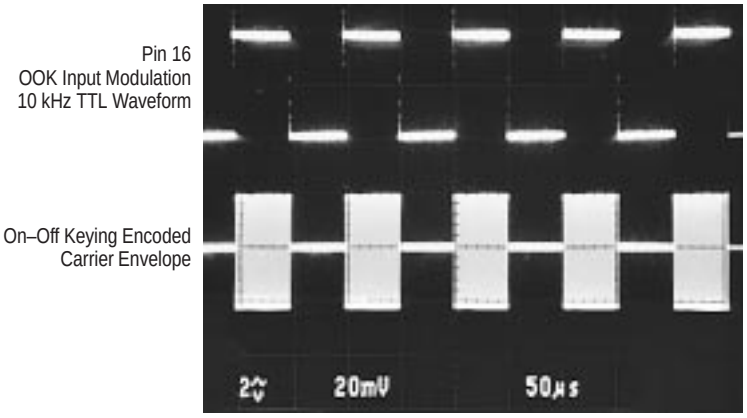


Figure 26. Oscillator Enable Time, T_{enable}

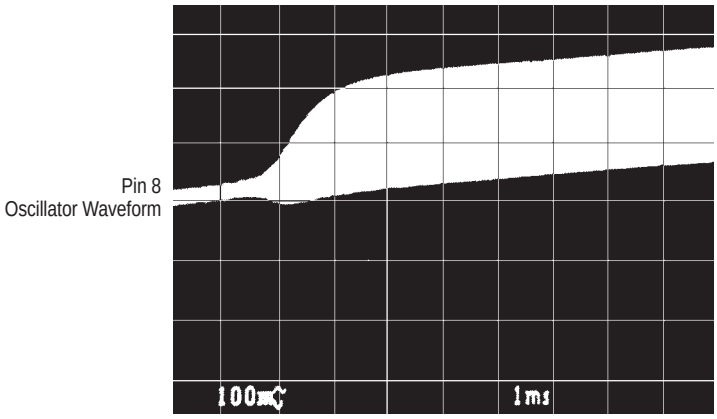
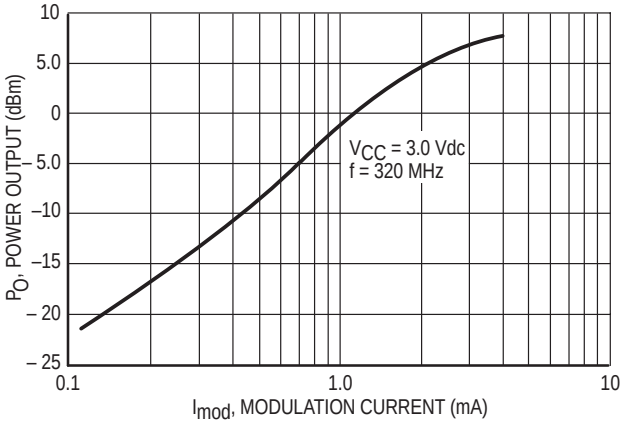


Figure 27. Power Output versus Modulation Current



Analog AM

In analog AM applications, the output amplifier's linearity must be carefully considered. Figure 27 is a plot of Power Output versus Modulation Current at 320 MHz, 3.0 Vdc. In order to achieve a linear encoding of the modulating sinusoidal waveform on the carrier, the modulating signal must amplitude modulate the carrier in the linear portion of its power output response. When using a sinewave modulating signal, the signal rides on a positive DC offset called V_{mod} which sets a static (modulation off) modulation current, I_{mod}. I_{mod} controls the power output of the IC. As the modulating signal moves around this static bias point the modulating current varies causing power output to vary or to be AM modulated. When the IC is operated at modulation current levels greater than 2.0 mAdc the differential output stage starts to saturate.

In the design example, shown in Figure 28, the operating point is selected as a tradeoff between average power output and quality of the AM.

For V_{CC} = 3.0 Vdc; I_{CC} = 18.5 mA and I_{mod} = 0.5 mAdc and a static DC offset of 1.04 Vdc, the circuit shown in Figure 28 completes the design. Figures 29, 30 and 31 show the results of – 6.9 dBm output power and 100% modulation by the 10 kHz and 1.0 MHz modulating sinewave signals. The amplitude of the input signals is approximately 800 mVp–p.

Where R_{mod} = (V_{CC} – 1.04 Vdc)/0.5 mA = 3.92 k, use a standard value resistor of 3.9 k.

Figure 28. Analog AM Transmitter

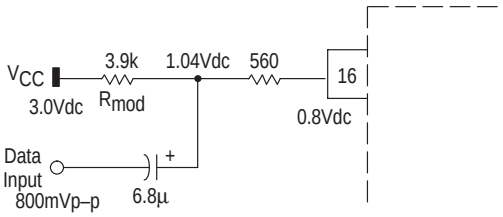


Figure 29. Power Output of Unmodulated Carrier



Figure 30. Input Signal and AM Modulated Carrier for f_{mod} = 10 kHz

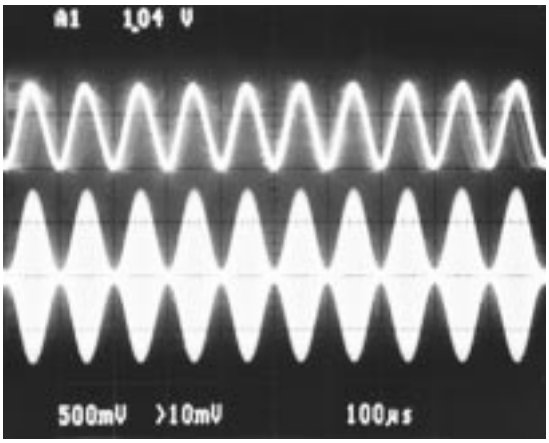


Figure 31. Input Signal and AM Modulated Carrier for f_{mod} = 1.0 MHz

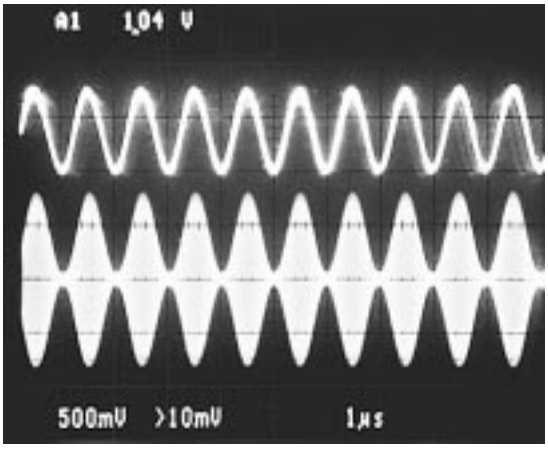


Figure 32. Circuit Side View of MC13176D

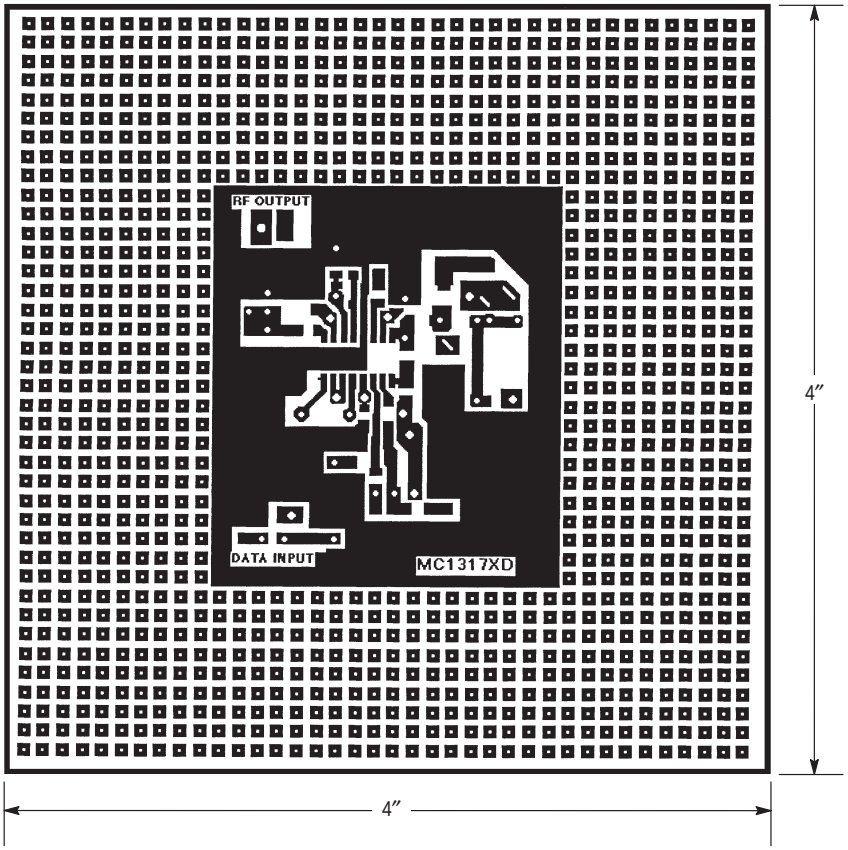


Figure 33. Ground Side View

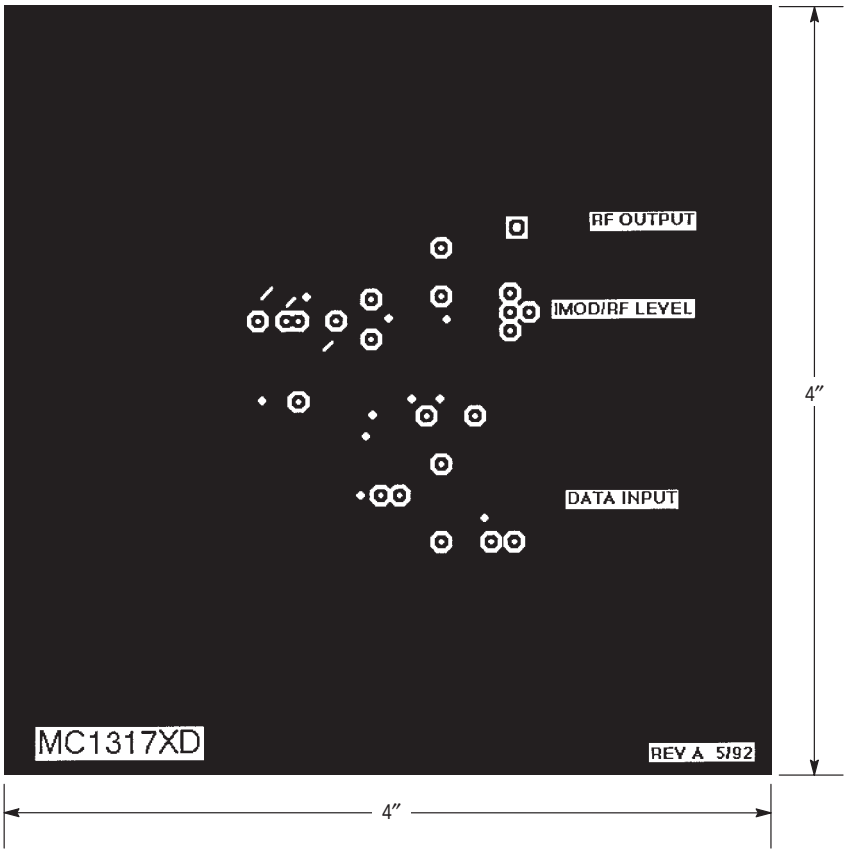


Figure 34. Surface Mounted Components Placement (on Circuit Side)

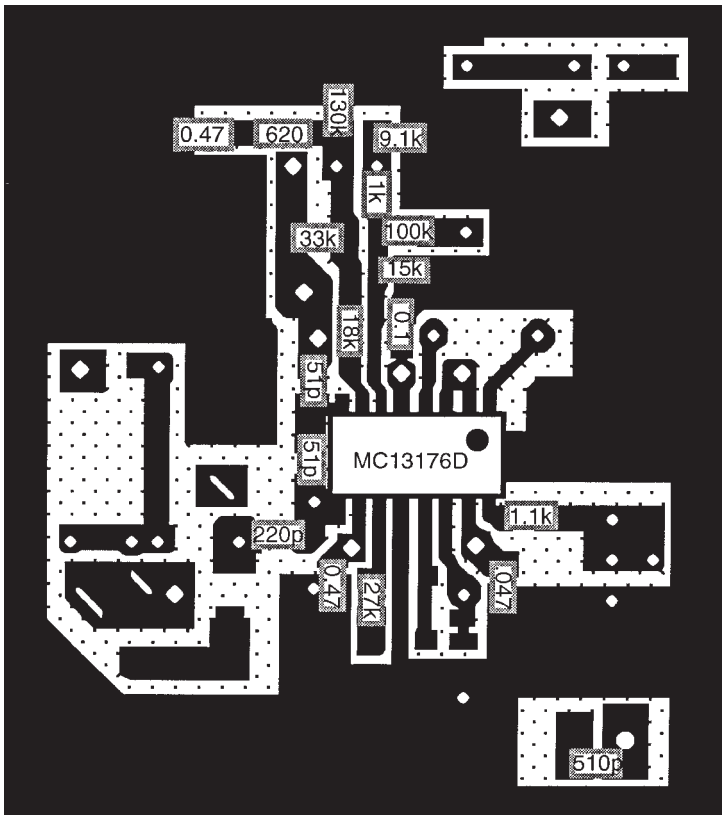
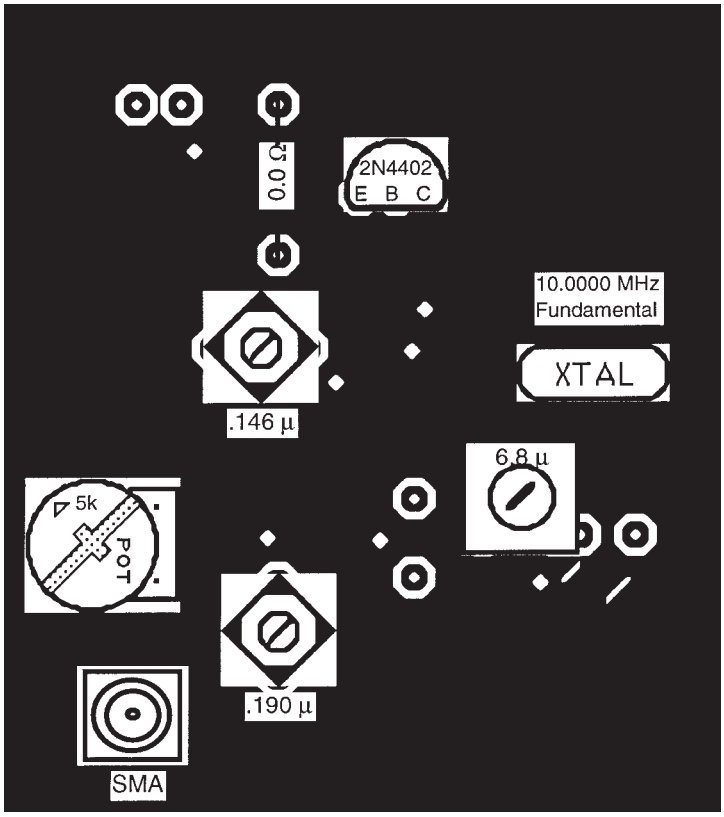


Figure 35. Radial Leaded Components Placement (on Ground Side)



MOTOROLA

MC33410

Advance Information

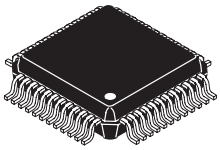
Dual CVSD/PLL Cordless Phone System

DUAL CVSD/PLL CORDLESS PHONE SYSTEM

SEMICONDUCTOR TECHNICAL DATA

The MC33410 Dual CVSD/Cordless Phone system is designed to fit the requirements of a 900 MHz digital cordless telephone system. The device contains a CVSD (Continuously Variable Slope Delta Modulator/Demodulator) Encoder to digitize the speech for the RF transmission, and a CVSD Decoder to reconstruct the received digital speech from the RF receiver. Provisions are made to transmit and receive data as well. Included are three PLLs (Phase–Locked Loops). Two are intended for use with external VCOs and 64/65 or 128/129 dual modulus prescalers, and can control the transmit and receive (LO1) frequencies for the 900 MHz communication. The third PLL is configured as the 2nd local oscillator (LO2), and is functional to 80 MHz. Also included are muting, audio gain adjust (internal and external), low battery/carrier detect, and a wide range for the PLL reference frequency. The power supply range is 2.7 to 5.5 V. A data only (non–voice) mode is also included.

- Two Complete CVSD Sections for Full Duplex Operation
- Two PLLs and an LO Suitable for a 900 MHz System
- Adjustable Detection for Low Battery or Carrier Signal (RSSI)
- Minimal External Components
- Encode Path Includes Adjustable Gain Amplifiers, Filters, Mute, CVSD Encoder, Data Insert, and Scrambler
- Decoder Path Contains Data Slicer, Clock Recovery, Descrambler, Data Detect, CVSD Decoder, Filters, Mute and Power Amplifier
- Data can be Transmitted During Voice Conversation with Minimal or No Noticeable Audio Disruption
- Idle Channel Noise Control
- Independent Power Amplifier with Differential Outputs, Mute
- Selectable Frequency for Switched Capacitor Filters, CVSD Function, PLLs, and the LO
- Reference Frequency Source can be a Crystal or System Clock
- Serial μP Port to Control Gain, Mute, Frequency Selection, Phase Detector Gain, Power Down Modes, Idle Channel Control, Scrambler Operation, Low Battery Detect, and Others
- Mode Available for Data Only Transmission (non–voice)
- Ambient Temperature Range: –20 to 70°C
- Power Supply Range: 2.7 to 5.5 V
- Power Down Modes for Power Conservation
- 48 Pin LQFP with 0.5 mm Lead Pitch

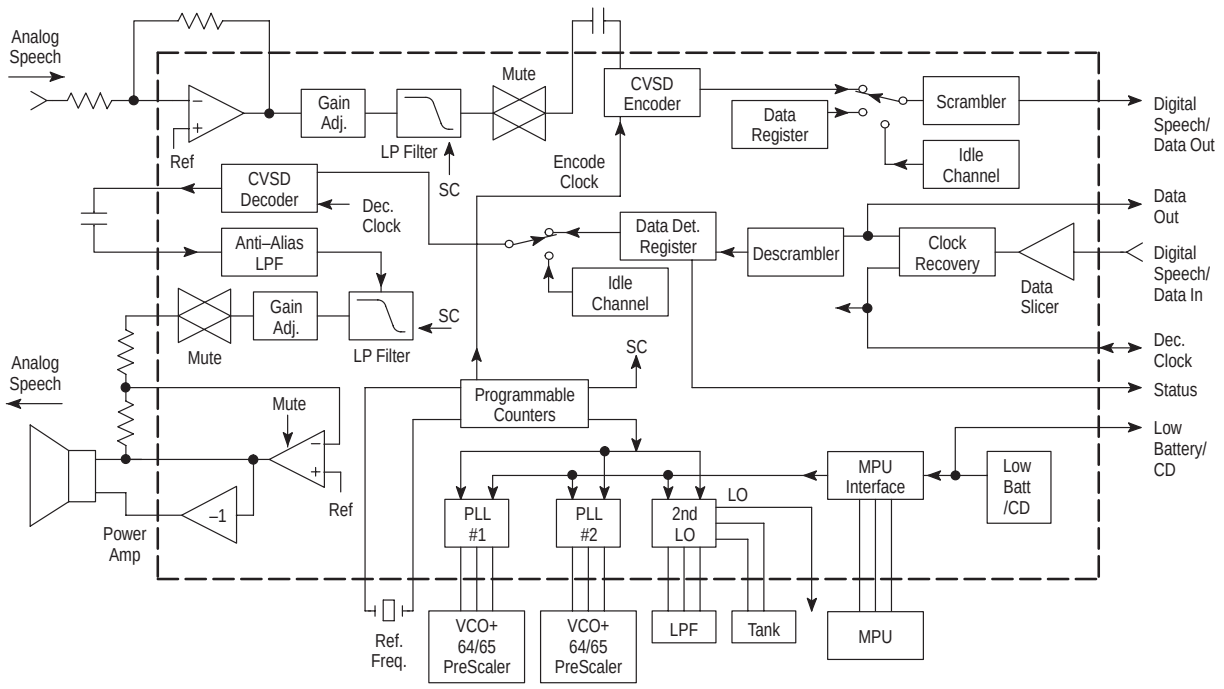


FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(LQFP–48)

ORDERING INFORMATION

Device	Operating Temperature	Package
MC33410FTA	–20 to 70°C	LQFP–48

Simplified Block Diagram



This device contains 19,638 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	V
Input Voltage – All Inputs	V_{in}	V_{CC} + 0.5	V
Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C

NOTES: 1. Meets Human Body Model (HBM) ≤2000 V and Machine Model (MM) ≤200 V.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	–	2.7	–	5.5	V
V_B Load Current	–	–100	0	50	µA
V_B Adjusted Voltage Using Bits 7/20–17	–	–	1.5	–	Vdc
Vag Load Current	–	–500	0	50	µA
CVSD Clock Rate	–	–	32, 50, or 64	–	kHz
Encoder in Signal Level (Pin 19, $V_{CC} \geq 3.0$ V)	–	–	–	2.9	V_{pp}
Rx Audio Input Signal Level (Pin 34)	–	–	–	–	V_{pp}
Peak Output Current at PAO+, PAO–	–	–	–	±10	mA
Reference Frequency Amplitude Applied to Pin 14	–	100	–	V_{CC}	mVpp
Rx Digital Input Signal Amplitude (Pin 38)	–	–	–	0.7	V_{pp}

NOTES: 1. Currents into a pin are positive. Currents out of a pin are negative.
2. All recommended limits are not necessarily functional concurrently.

RECOMMENDED OPERATING CONDITIONS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Sink Current into Low Battery Output (Pin 16)	–	–	–	1.2	mA
Digital Input Voltage (Pins 10–12, 39)	–	–	–	–	–
Maximum Clock/Data Rate at MPU Port (Pins 10–12)	–	–	–	2.0	MHz
Crystal or Reference Frequency at Pin 14	–	4.0	–	18.25	MHz
Maximum Data Rate in Data Modem Mode	–	–	250	–	kbps
LO2 VCO Control Voltage (Pin 44)	–	0	–	V_{CC}	V
Maximum 2nd LO Frequency	–	–	65	80	MHz
12 Bit Reference Counter Range	–	3_d	–	4095_d	–
13 Bit N Counter Range	–	3_d	–	8191_d	–
7 Bit A Counter Range With a 64/65 Modulus Prescaler With a 128/129 Modulus Prescaler	–	 0_d 0_d	 – –	 63_d 127_d	–
14 Bit LO2 Counter Range	–	12_d	–	16383_d	–
6 Bit Counters (for SCF and Encode Clock)	–	3_d	–	63_d	–
Maximum SCF Clock Frequency	–	–	–	512	kHz
Operating Ambient Temperature	–	–20	–	70	°C

NOTES: 1. Currents into a pin are positive. Currents out of a pin are negative.
2. All recommended limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.6 V, f_{ref} = 10.24 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
MICROPHONE AMPLIFIER					
Output Offset with Respect to V_B (RF = 100 kΩ)	–	–	0.5	–	mVdc
Input Bias Current (Pin 23)	–	–	10	–	nA
Open Loop Gain (f < 100 Hz)	–	–	70	–	dB
Gain Bandwidth	–	–	1.0	–	MHz
Maximum Output Voltage Swing (THD < 1%, $V_{CC} \geq$ 3.0 V)	–	–	3.0	–	V_{pp}
Maximum Output Current Capability (V_{CC} = 3.6 V)	–	–	2.2	–	mA pk
Tx AUDIO PATH (Pins 22–20)					
Remote Gain Adjust (f = 1.0 kHz) Gain with Bits 6/15–11 = 00100 Gain Change (Relative to Bits 6/15–11 = 00100) Bits 6/15–11 = 00001 Bits 6/15–11 = 00010 Bits 6/15–11 = 01000 Bits 6/15–11 = 10000	–	 – –8.5 –5.0 3.0 4.0	 ±0.4 –7.6 –4.3 3.6 7.4	 – –6.5 –3.0 5.0 12	dB
Low Pass Filter (SCF Clock = 256 kHz, Gains are Relative to 400 Hz) –3.0 dB Point ΔGain at 3.5 kHz ΔGain at 3.7 kHz Gain Reduction at 20 kHz Ripple (400 Hz to 3.5 kHz)	–	 – 0 – – –	 5.0 – – 40 ±0.1	 – 0.15 –0.15 – –	 kHz dB dB dB dB
Smoothing Filter –3.0 dB point	–	–	30	–	kHz
Muting (Gain Reduction), Bit 6/2 = 1	–	60	95	–	dB
Pin 20 DC Level	–	–	V_B	–	Vdc
Maximum Output Voltage Swing (THD < 1%, $V_{CC} \geq$ 3.0 V)	–	–	2.9	–	V_{pp}
Maximum Output Current Capability (V_{CC} = 3.6 V)	–	–	1.8	–	mA pk

NOTE: Currents into a pin are positive. Currents out of a pin are negative.

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC} = 3.6 V, f_{ref} = 10.24 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CVSD ENCODER AND IDLE CHANNEL DETECTION					
DC Level (Pin 19)	–	–	Vag	–	Vdc
Input Impedance (Pin 19)	–	–	150	–	kΩ
Maximum Input Level	–				V_{pp}
V_{CC} = 2.7 V		–	0.8	–	
V_{CC} ≥ 3.0 V		–	2.9	–	
CVSD DECODER OUTPUT (Pin 35)					
Minimum Step Size	–				mV
Bits 2/22–21 = 01		–	1.4	–	
Bits 2/22–21 = 10		–	5.6	–	
Bits 2/22–21 = 11		–	22.4	–	
Maximum Output Signal	–				V_{pp}
V_{CC} ≤ 3.0 V		–	1.6	–	
V_{CC} > 3.0 V		–	2.6	–	
Output Current Capability	–	–	–	–	mA pk
Clock Noise Content	–	–	–65	–	dBm
Rx AUDIO PATH (Pins 34–32)					
Rx Audio In (Pin 34)	–				
DC Level		–	V_B	–	Vdc
Input Impedance		–	600	–	kΩ
Maximum Input Signal		–	–	–	V
Rx Audio Out (Pin 32)	–				
DC Level		–	V_B	–	Vdc
Maximum Output Current		–	1.8	–	mA
Maximum Output Signal		–	–	–	V
Low Pass Filter (SCF Clock = 256 kHz, Gains are Relative to 400 Hz)	–				
–3.0 dB Point		–	5.0	–	kHz
ΔGain at 3.5 kHz		0	–	0.25	dB
ΔGain at 3.7 kHz		–	–	–0.25	dB
Gain Reduction at 20 kHz		–	40	–	dB
Ripple (400 Hz to 3.5 kHz)		–	±0.1	–	dB
Smoothing Filter –3.0 dB Point	–	–	30	–	kHz
Decoder Clock Noise Reduction	–	–	>20	–	dB
Receive Gain Adjust (Gain From Pins 34–32, f = 1.0 kHz)	–				dB
Bits 6/10–6 = 01111		–3.0	0	3.0	
Bits 6/10–6 = 11001		13	14.7	17	
Bits 6/10–6 = 00110		–15.5	–13.7	–11.5	
Gain Range (Gain at 11001 – Gain at 00110)		27	28.5	30	
Muting (Gain Reduction), Bit 6/1 = 1	–	60	95	–	dB
POWER AMPLIFIERS					
PAI (Pin 31)	–				
DC Level		–	V_B	–	Vdc
Bias Current		–	<10	–	nA
PAO– Offset ($V_{PAO–}$ – V_B, Feedback R = 30 kΩ)	–	–	12	–	mVdc
PAO– to PAO+ Offset	–	–	±5.0	–	mVdc
Open Loop Gain (PAI to PAO–, f < 100 Hz)	–	–	65	–	dB
Gain Bandwidth	–	–	1.0	–	MHz
Closed Loop Gain (PAO– to PAO+)	–	–	±0.1	–	dB
Maximum Output Swing (THD ≤ 1%)	–	–	–	–	–
PAO– High Voltage (I_{out} = –5.0 mA)	–	V_{CC} – 1.2	V_{CC} – 1.0	V_{CC} – 0.2	VDC

NOTE: Currents into a pin are positive. Currents out of a pin are negative.

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC} = 3.6 V, f_{ref} = 10.24 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER AMPLIFIERS					
PAO– Low Voltage (I_{out} = 5.0 mA)	–	50	420	600	mVdc
PAO+ High Voltage (I_{out} = –5.0 mA)	–	V_{CC} – 1.2	V_{CC} – 1.0	V_{CC} – 0.2	VDC
PAO+ Low Voltage (I_{out} = 5.0 mA)	–	50	280	600	mVdc
Muting to PAO– (Gain Reduction), Bit 6/0 = 1	–	60	95	–	dB
V_B REFERENCE (Pin 33)					
Initial Voltage (Bits 3/20–17 = 0111)	–	1.38	1.50	1.62	Vdc
Adjustment Range From Initial Value (Bits 3/20–17 = 0000 to 1111)	–	–	±9.0	–	%
Adjustment per Step (Bits 3/20–17)	–	–	1.2	–	%
Closest Adjustment to 1.5 V (Using Bits 3/20–17)	–	1.47	–	1.53	Vdc
Power Supply Rejection (f = 1.0 kHz, C_{VB} = 4.7 µF)	–	–	84	–	dB
LOW BATTERY/CARRIER DETECT					
Low Battery Mode (Bit 6/5 = 0) – V_{CC} Threshold (1.47 ≥ V_B ≥ 1.53 V, V_{CC} Decreasing)	–				Vdc
Bits 3/23–21 = 000		2.63	2.9	3.18	
Bits 3/23–21 = 001		2.71	2.99	3.27	
Bits 3/23–21 = 010		2.79	3.07	3.36	
Bits 3/23–21 = 011		2.87	3.16	3.45	
Bits 3/23–21 = 100		2.96	3.25	3.54	
Bits 3/23–21 = 101		3.04	3.34	3.64	
Bits 3/23–21 = 110		3.11	3.42	3.73	
Bits 3/23–21 = 111		3.19	3.5	3.81	
Hysteresis	–	–	6.0	–	mV
Step Size (Low Battery Mode)	–	30	85	–	mV
Carrier Detect Mode (6/5 = 1) – Threshold @ Pin 36 (V_B = 1.50 V, ±20 mV, Bits 3/23–21 = 000, 7/5–4 = 11)	–	650	845	1050	mV
Hysteresis	–	–	5.0	–	mV
Output Voltage @ Pin 16 (Output Low, 100 k Pullup Resistor)	–	–	0.02	–	Vdc
Leakage Current @ Pin 16 (Output High)	–	–	<10	–	nA
MP1, MP2, MP3 ENCODE OUT					
Output Levels (I_{out} = ±100 µA)	–				
High Level		–	3.5	–	Vdc
Low Level		–	40	–	mVdc
Input Impdeance @ MP1 (Bits 7/5–4 = 11)	–				
Low Battery Mode (6/5 = 0)		–	>10	–	MΩ
Carrier Detect Mode (6/5 = 1)		–	600	–	kΩ
DC Level @ MP1 (Bist 7/5–4 = 11, Carrier Detect Mode)	–	–	V_B	–	Vdc
MP2 (Bits 7/7–6 = 01 or 1X)	–				
Input Impedance		–	–	–	–
DC Level (I_{in} = 0)		–	0	–	Vdc
Input Threshold					
High		–	V_{CC} – 0.4	–	Vdc
Low		–	0.8	–	Vdc
DATA SLICER (Pin 38)					
DC Level	–	–	V_{CC} – 0.7	–	Vdc
Input Impedance	–	–	250	–	kΩ
Threshold (Increasing Signal)	–	–	V_{CC} – 0.7	–	Vdc
Hysteresis	–	20	35	60	mV

NOTE: Currents into a pin are positive. Currents out of a pin are negative.

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC} = 3.6 V, f_{ref} = 10.24 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Tx/Rx PLL/PHASE DETECTORS					
Phase Detector Output Current (0.5 V ≤ V_{out} ≤ V_{CC} – 0.5 V)	–				µA
100 µA Mode (Bits 1/20, 2/20 = 0)					
Sink		70	100	130	
Source		–130	–100	–70	
400 µA Mode (Bits 1/20, 2/20 = 1)					
Sink		280	400	520	
Source		–520	–400	–280	
Phase Detector Current Ratio (Source/Sink) (V_{out} = V_{CC}/2, ±100 µA and ±400 µA Ranges)	–	0.80	1.0	1.25	µA/µA
Phase Detector Leakage Current (High–Z Mode @ V_{CC}/2)	–	–80	±1.5	80	nA
FRxMC/FTxMC Output Voltage (Bit 7/13 = 1, I_{out} = ±100 µA)	–				V
High		3.4	3.5	–	
Low		–	0.02	0.2	
FRxMC/FTxMC Output Current (Bit 7/13 = 0, V_{out} = 0.8 V)	–				µA
Sink		70	100	130	
Source		–130	–100	–70	
FRx/FTx	–				
Input Current, V_{in} = V_{CC}					µA
FRx		0	10	14	
FTx		0	10	30	
V_{in} = 0 V		–10	–7.5	–	
DC Level		–	1.5	–	Vdc
Input Amplitude		200	–	1200	mVpp
Propagation Delay (FRx to FRxMC and FTx to FTxMC)	–	–	20	–	ns
LO2 PLL (Pins 41–48)					
Maximum Frequency	–	65	80	–	MHz
Input Current @ LO2 Control (0.5 V ≤ V_{in} ≤ V_{CC} – 0.5 V)	–	–1.0	0	1.0	µA
Phase Detector Output Current (0.5 V ≤ V_{out} ≤ V_{CC} – 0.5 V)	–				µA
100 µA Mode (Bit 3/14 = 0)					
Sink		70	100	130	
Source		–130	–100	–70	
400 µA Mode (Bit 3/14 = 1)					
Sink		280	400	520	
Source		–520	–400	–280	
Phase Detector Current Ratio (Source/Sink) (V_{out} = V_{CC}/2, ±100 µA and ±400 µA Ranges)	–	0.80	1.0	1.25	µA/µA
Phase Detector Leakage Current (High–Z Mode @ V_{CC}/2)	–	–80	±1.5	80	nA
LO2 Output Amplitude (Pin 41 with 25 Ω Load)	–	–	58	–	mVpp
Frequency Change (L = 150 nH, C = 27 pF)	–				MHz
Pin 44 Changed from 0.4 to 0.6 V		0.9	1.3	1.7	
Pin 44 Changed from 2.5 to 3.0 V		0.8	1.2	1.6	
Internal Capacitor (Pin 43–45)	–				pF
Bits 7/20–18 = 001		1.0	1.1	1.3	
Bits 7/20–18 = 010		1.9	2.2	3.5	
Bits 7/20–18 = 100		4.0	4.4	6.5	
Bits 7/20–18 = 111		7.0	7.7	10.5	
Internal Capacitor Change (Pin 43–45) (Bits 7/20–18 Increased from 000 to 111)	–	0	1.1	–	pF/Step

NOTE: Currents into a pin are positive. Currents out of a pin are negative.

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC} = 3.6 V, f_{ref} = 10.24 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE OSCILLATOR (Pins 14, 15)					
f_{ref} Out Output Levels (I_{out} = ±100 µA)	–				Vdc
High Level		–	V_{CC} – 0.2	–	
Low Level		–	0.2	–	
DC Bias Voltage @ f_{ref} In	–	–	V_{CC}/2	–	Vdc
Input Current @ f_{ref} In	–				µA
V_{in} = 0 V		–15	–5.0	–2.0	
V_{in} = V_{CC}		2.0	5.6	15	
MPU SERIAL INTERFACE PORT (Pins 10–12)					
Input Switching Threshold @ V_{CC} = 3.6 V	–				Vdc
High		–	3.1	–	
Low		–	0.7	–	
Input Current	–				µA
V_{in} = 3.3 V		0.5	1.6	3.0	
V_{in} = 0.3 V		0.05	0.5	1.5	
Data (Pin 12) Output Levels (I_{out} = ±100 µA)	–				Vdc
High		–	3.5	–	
Low		–	0.1	–	
Timing	–				ns
Enable to Clock Setup Time		–	200	–	
Data to Clock Setup Time		–	100	–	
Data, Clock Hold Time		–	90	–	
Recovery Time		–	90	–	
Data, Clock Pulse Width		–	100	–	
Power On Reset Delay	–	–	100	–	µs
Input Capacitance	–	–	8.0	–	pF
Minimum V_{CC} to Maintain Register Settings	–	–	1.0	–	Vdc
POWER SUPPLY CURRENT					
All Sections Enabled (Bits 5/10–0 = 0)	–	9.0	12.5	16	mA
Wakeup Mode (Bits 5/9–5, 1 = 1)	–	5.5	7.7	10	mA
MPU Port Only Enabled (Bits 5/10–0, 18 = 1)	–				µA
V_{CC} = 3.6 V		–	6.0	15	
V_{CC} = 5.5 V		–	–	50	
AUDIO SYSTEM SPECIFICATIONS					
Gain From Audio In to PAO–	–				dB
V_{in} = –40 dBV, f_{in} = 1.0 kHz, V_{CC} = 3.6 V		17	20.3	23	
V_{in} = –60 dBV, f_{in} = 200 Hz, V_{CC} = 2.7 V		17	19.3	23	
V_{in} = –20 dBV, f_{in} = 3.4 kHz, V_{CC} = 5.5 V		17	18.7	23	

NOTE: Currents into a pin are positive. Currents out of a pin are negative.

Figure 1. Test Circuit

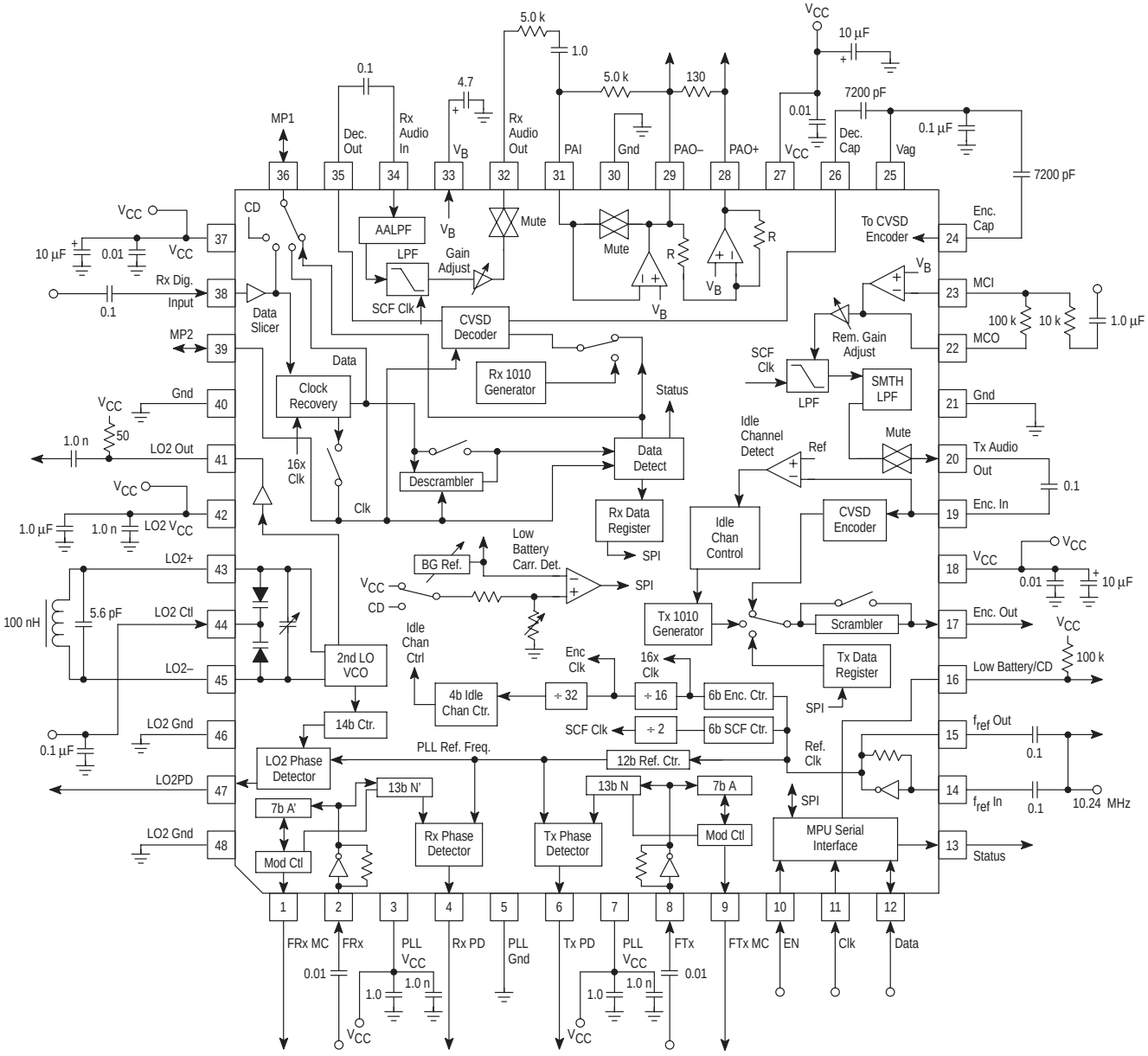
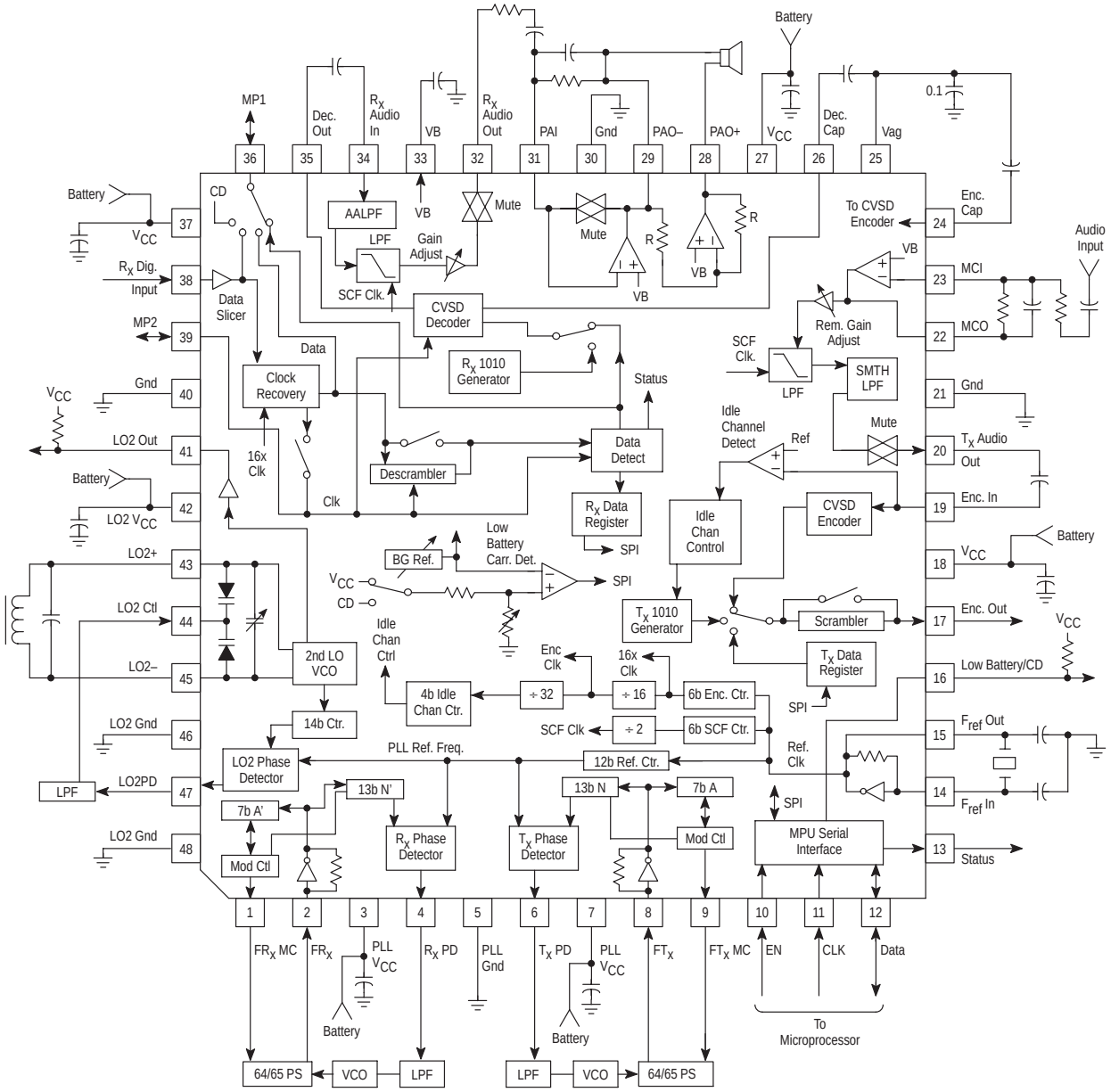


Figure 2. Typical Applications Circuit



PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	FR_X MC	Modulus Control Output to the R_X 64/65 or 128/129 dual modulus prescaler.
2	FR_X	Input to the R_X PLL.
3	PLL V_{CC}	Supply pin for the R_X PLL section. Allowable range is 2.7 to 5.5 V.
4	R_X PD	Phase detector charge pump output of the R_X PLL.
5	PLL Gnd	Ground pin for the PLL sections.
6	T_X PD	Phase detector charge pump output of the T_X PLL.
7	PLL V_{CC}	Supply pin for the T_X PLL section and the MPU Serial Interface section. Allowable range is 2.7 to 5.5 V.
8	FT_X	Input to the T_X PLL.
9	FT_X MC	Modulus Control Output to the T_X 64/65 or 128/129 dual modulus prescaler.
10	EN	Enable input for the μP port. This signal latches in the register address and data.
11	CLK	Clock input for the μP port. Maximum frequency is 2.0 MHz.
12	Data	Bi–directional data line for the μP port. In Data Modem mode, this pin provides the recovered clock.
13	Status	Logic output which indicates that a predetermined 16 or 24–bit code word has been detected in the Data Detect register, and the following data word has been loaded into register 10. In Data Modem mode, this pin provides the Transmit Data clock.
14, 15	F_{ref} In, F_{ref} Out	A crystal, in the range of 4.0 to 18.25 MHz can be connected to these pins to provide the reference frequency. If an external reference source is used, it is to be capacitively coupled to F_{ref} In.
16	Low Battery/CD	An open collector output. When low, indicates either the supply voltage (V_{CC}) is low, or the carrier level is above the threshold. This output is off when disabled.
17	Enc Out	The digital output of the scrambler, which passes data from the CVSD encoder, or the T_X Data register, or the T_X 1010 Generator. Source selection is done through the μP port.
18	V_{CC}	Supply input for the audio sections, filters, and CVSD blocks. Allowable range is 2.7 to 5.5 V. Internally connected to Pins 27 and 37.
19	Enc In	The analog input to the CVSD encoder. Max. input level is 3.0 V_{pp}.
20	T_X Audio Out	Output of the transmit speech processing section.
21	Ground	Ground for the audio sections, filters, and CVSD blocks. Internally connected to Pins 30 and 40.
22	MCO	Output of the microphone amplifier, and input to the filters. This output has rail–to–rail capability.
23	MCI	Inverting input of the microphone amplifier. Gain and frequency response is set with external resistors and capacitors.
24	Enc Cap	This capacitor sets the time constant for the CVSD encoder. This pin is sensitive to leakage.
25	VAG	Analog ground for the audio section and the CVSD encoder and decoder.
26	Dec Cap	The capacitor sets the time constant for the CVSD decoder. This pin is sensitive to leakage.
27	V_{CC}	Supply input for the audio sections, filters, and CVSD blocks. Allowable range is 2.7 to 5.5 V. Internally connected to Pins 18 and 37.
28, 29	PAO+, PAO–	Differential outputs of the power amplifier stage for driving an earpiece or hybrid network. The gain and frequency response are set with external resistors and capacitors.
30	Gnd	Ground for the audio sections, filters, and CVSD blocks. Internally connected to Pins 21 and 40.
31	PAI	Input to the power amplifier stage. This pin is a summing node.
32	R_X Audio Output	Output of the receive speech processing section.
33	VB	The capacitor filters the internal 1.5 V reference voltage. If VB is adjusted, it may be monitored at this pin. Max. load current is 10 μA.
34	R_X Audio In	Input to the receive speech processing section.
35	Dec Out	The analog output of the CVSD decoder.
36	MP1	As an output, provides the recovered R_X data, or the Data Detect output, or the data slicer output. Or it can be set to a high impedance input (600 kΩ) for the carrier detect input signal. Selection is done through the μP port. See Table 6.

NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Description
37	V_{CC}	Supply input for the audio sections, filters, and CVSD blocks. Allowable range is 2.7 to 5.5 V. Internally connected to Pins 18 and 27.
38	R_X Digital Input	The digital stream from the RF receiver is applied to the data slicer at this pin. Minimum amplitude is 200 mVpp. Hysteresis ≈50 mV.
39	MP2	As an output, this pin provides the recovered clock from the Clock Recovery block. As an input, the CVSD decoder clock can be applied to this pin. Or this pin may be set to a disabled state. Selection is done through the μP port. See Table 7. In Data Modem mode, the data to be transmitted is input to this pin.
40	Gnd	Ground for the audio sections, filters, and CVSD blocks. Internally connected to Pins 21 and 30.
41	LO2 Out	Buffered output of the 2nd LO frequency. A pullup resistor is required.
42	LO2 V_{CC}	Supply pin for the 2nd LO. Allowable range is 2.7 to 5.5 V.
43, 45	LO2+, LO2–	A tank circuit is connected to these pins for the 2nd LO.
44	LO2 Ctl	The varactor control pin for the 2nd LO.
46	LO2 Gnd	Ground for the 2nd LO section.
47	LO2 PD	Phase detector charge pump output of the 2nd LO PLL.
48	LO2 Gnd	Ground for the 2nd LO section.

NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

FUNCTIONAL DESCRIPTION

Note: In the following descriptions, control bits in the MPU Serial Interface for the various functions will be identified by register number and bit number. For example, bit 3/19 indicates bit 19 of register 3. Bits 5/14–11 indicates register 5, bits 14 through 11. Please refer to Figure 1.

Transmit Speech Processing Section

This section is made up of the externally adjustable microphone amplifier (Pins 22 to 23), internally adjustable gain stage, two low pass filters, and a mute switch.

The gain of the microphone amplifier is set with external resistors to receive the audio from the microphone (in the handset), or from the hybrid (in the base unit), or from any other audio source. The MCO output has rail–to–rail capability, and the dc bias level is at VB (≈1.5 V).

The adjustable gain stage, referred to as the Remote Gain Adjust, provides 5 levels of gain in 4.0 dB increments. It is controlled with bits 6/15–11 as shown in Table 2.

Table 1. Remote Gain Adjust

Register 6 Bits 15–11	Gain
00001	–8.0 dB
00010	–4.0 dB
00100	0 dB
01000	+4.0 dB
10000	+8.0 dB

Other combinations for the 5 bits are invalid.

The Low Pass Filter after the gain stage is a switched capacitor filter with a corner frequency at 5.0 kHz. The subsequent smoothing low pass filter has a corner frequency at 30 kHz, and is designed to filter out high frequency clock noise from the previously mentioned switched capacitor filter.

The mute switch at Pin 20 will mute a minimum of 60 dB. Bit 6/2 controls the mute.

CVSD Encoder/Idle Channel/T_X Data Register

The analog signals to be digitized are input at Pin 19 to the CVSD Encoder. The output of the encoder will be the digital equivalent of the audio, at the selected clock rate. Based on the reference frequency, bits 4/23–18 are used to set the 6 Bit Encoder Counter, in conjunction with the subsequent ÷16 divider, to set the CVSD Encoder frequency to 32, 50, or 64 kHz. Bits 3/16–15 will set the CVSD for proper operation at the selected frequency, according to Table 2.

Table 2. CVSD Clock/Data Rates

Register 3		
Bit 16	Bit 15	Clock/Data Rate
0	1	32 kHz
1	0	50 kHz
1	1	64 kHz

The Encoder's minimum step size can be selected using bits 2/22–21, according to Table 3.

Table 3. Minimum Step Size

Encoder Register 2 Bits 22, 21	Decoder Register 1 Bits 22, 21	Step Size
00	00	No minimum
01	01	1.4 mV
10	10	5.6 mV
11	11	22.4 mV

The T_X 1010 Generator, when selected, provides an alternating "1–0" pattern (a square wave at half the CVSD clock rate) to the scrambler. This represents the lowest amplitude analog signal, and can be used when it is desired to send a quiet signal. Selection of this block can occur either automatically, or intentionally, as follows:

a. The automatic selection occurs when the Idle Channel Detector senses the average audio signal at Pin 19 is below a threshold which is set with bits 5/17–15 (See Table 4). Bits 5/14–11 select a time delay for the automatic threshold detection to occur. The minimum delay is zero, with these bits set to 0000. Changing the bits provides delay in increments of 32 clock cycles (of the CVSD Encoder clock). The maximum delay is 480 clock cycles, (7.5 mS at 64 kHz). When the average audio signal at Pin 19 increases above the threshold, the T_X 1010 Generator will be deselected with no delay. This automatic switchover feature can be disabled with bit 7/2. Bit 5/21 indicates when an idle channel condition has been detected. This output bit will be functional even when the idle channel detector is disabled with bit 7/2. Bit 5/18 will power down the Idle Channel Detect Circuit as a power saving measure.
b. Bit 6/4 can be used to intentionally select the T_X 1010 Generator at any time.

Table 4. Idle Channel Detection Threshold

Register 5 Bits 17–15	Threshold		Register 5 Bits 17–15	Threshold
000	–50 dBV		100	–60 dBV
001	–52.5		101	–62.5
010	–55		110	–65
011	–57.5		111	–67.5

The T_X Data Register is used for the transmission of data between the handset and base units. The procedure is as follows:

a. At the receiving unit: The code word (16 or 24 bits, set with bit 7/11) identifying that a data transmission is occurring must be loaded into the T_X Data Register (by loading register 8). This is used to detect when a code word is sent from the transmitting unit.
b. At the transmitting unit: The same code word as above is loaded into register 8. It is automatically loaded into the T_X Data Register.

c. The data word (16 or 24 bits, set with bit 7/12) is then loaded into register 9.
d. Upon loading register 9, the MC33410 automatically sends out (at Pin 17) the code word, followed by the data word, at the CVSD clock rate.

When the data word is completely sent out, the MC33410 will then return Pin 17 to its previous source of digital information (CVSD Encoder or T_X 1010 Generator).

Scrambler/Digital Output

The scrambler receives digital data from the CVSD Encoder, or the T_X 1010 Generator, or the T_X Data Register, to be output at Pin 17. The output level is 0 to V_{CC}. The scrambler can be bypassed with Bit 7/1.

The scrambler, better known as a randomizer, provides not only a level of communication security, but also helps ensure the digital output will not contain an abnormally long string of 1s or 0s which can adversely affect the CVSD Decoder operation, as well as the RF section. The scrambler is a maximal–length shift register sequence generator. The length of the shift register is selectable to one of eight values with bits 7/10–8 (the descrambler in the receiving unit must be set the same). Table 5 lists the polynomial associated with each tap selection.

Table 5. Scrambler/Descrambler Tap Selection

Tap No.	Register 7			Shift Register Length	Polynomial
	Bit 10	Bit 9	Bit 8		
0	0	0	0	2	$1 + z^{-1} + z^{-2}$
1	0	0	1	3	$1 + z^{-2} + z^{-3}$
2	0	1	0	4	$1 + z^{-3} + z^{-4}$
3	0	1	1	5	$1 + z^{-3} + z^{-5}$
4	1	0	0	6	$1 + z^{-5} + z^{-6}$
5	1	0	1	7	$1 + z^{-6} + z^{-7}$
6	1	1	0	9	$1 + z^{-5} + z^{-9}$
7	1	1	1	10	$1 + z^{-7} + z^{-10}$

Data Slicer/Clock Recovery

The data slicer will receive the low level digital signal from the RF receiver section at Pin 38. The input signal to the data slicer must be >200 mVpp. Hysteresis of 50 mV is internally provided. The output of the data slicer will be same waveform, but with an amplitude of 0 to V_{CC}, and can be observed at Pin 36 (MP1) if bits 7/5–4 are set to 10. The output can be inverted by setting bit 5/19 = 1.

The clock recovery block will generate a phase locked clock, equal to the CVSD data rate, from the incoming data, as long as the Encoder Counter (bits 4/23–18) is set for that data rate. The recovered clock can be observed at Pin 39 (MP2) if bits 7/7–6 are set to 00. The data from the clock recovery block can be observed at Pin 36 if bits 7/5–4 are set to 00. The clock recovery block may be bypassed by setting bit 7/0 to 1. With this setting the data slicer output will go directly to the descrambler, and the encoder clock will replace the Clock Recovery Clock.

Tables 6 and 7 summarize the options available at MP1 and MP2 (Pins 36 and 39).

Table 6. MP1 Options (Pin 36)

Register 7		Function
Bit 5	Bit 4	
0	0	Data from clock recovery block
0	1	Data Detect Output
1	0	Data Slicer Output
1	1	Hi–Z/ CD Input

Table 7. MP2 Options (Pin 39)

Register 7		Function
Bit 7	Bit 6	
0	0	Output recovered clock
0	1	Input CVSD Decoder clock
1	X	Disabled (Hi–Z)

When MP1 is set to a Hi–Z condition, the pin is an input for the CD (Carrier Detect) function, with an input impedance of 600 KΩ. See the section entitled Low Battery/Carrier Detect for an explanation of this function.

Descrambler

The descrambler receives the scrambled data from the clock recovery block (or the data slicer if bit 7/0 = 1), and descrambles it to the original data as long as the selected taps are the same as those in the transmitting scrambler (see Table 5). The descrambler block is the same configuration as the scrambler, and is self–synchronizing. The descrambler can be bypassed with bit 7/1.

Data Detect Register/Status Output/R_X Data Register

The Data Detect register will continuously compare the descrambled data it receives with the 16 or 24–bit code word stored in the T_X Data Register (loaded through register 8). Upon detecting a match, and after the code word passes through the shift register, the following (16 or 24–bit) data word will be stored into the R_X Data Register, and then loaded into register 10 of the MPU Interface. At this time the Status output at Pin 13, and bit 5/22, will go high. The external microprocessor can then retrieve the data word by reading register 10, at which time the Status pin and bit will go low.

Upon detection of a code word as described above, the CVSD Decoder will be provided with 32, 40, or 48–bits of a 1010 pattern (idle channel) to minimize disturbances to the audio. After the data word is loaded into register 10, the CVSD Decoder resumes receiving data from the descrambler. The audio is therefore interrupted with a low level signal for a maximum of 48 clock cycles (0.75 mSec at 64 kHz).

The Data Detect register can be bypassed by setting bit 7/3 = 1.

CVSD Decoder/Decoder Clock/Idle Channel

The CVSD Decoder will provide the analog equivalent, at Pin 35, of the digital data it receives from the descrambler, or from the 1010 generator (idle channel generator). There is a single pole filter at the Decoder output to reduce the clock noise normally present on a CVSD analog output. The CVSD Decoder is self synchronizing as long as the decoder clock matches the data rate, and the Decoder has been set with bits 3/16–15 according to Table 2.

The Decoder clock is provided from the Clock Recovery block by setting bits 7/7–6 to 00 or 1X. The clock is internally provided to the Decoder, and is available at Pin 39. Alternately, a Decoder clock can be provided from an

external source to Pin 39 by setting bit 7/7–6 to 01 (see Table 7).

The R_X 1010 Generator provides an alternating 1–0 pattern (a square wave at half the CVSD clock rate) to the CVSD Decoder, resulting in the lowest amplitude analog signal at Pin 35. The 1010 Generator is automatically selected whenever data is detected and received by the Data Detection Circuit, as described above. Additionally, the 1010 Generator can be selected with bit 6/3 at any time.

The Decoder's minimum step size can be selected using bits 1/22–21, according to Table 3.

Receive Audio Path

The Receive Audio Path (Pins 34 to 32) consists of an anti–aliasing filter, a low pass filter, a gain adjust stage, and a mute switch.

Since the analog output of the CVSD Decoder (typically input at Pin 34) will contain noise at the CVSD clock rate, the anti–aliasing filter, with a corner frequency at 30 kHz, is provided to prevent aliasing of that clock noise with the subsequent switched capacitor filter.

The switched capacitor low pass filter is a 3 pole filter, with a corner frequency at 5.0 kHz. This is designed to remove the clock noise from the CVSD Decoder output signal, as well as provide bandwidth limiting in the audio range.

The gain stage provides 28.5 dB of gain adjustment in 19 steps (1.5 dB each), measured from Pin 34 to 32. Bits 6/10–6 are used to set the gain according to Table 8.

The mute switch at Pin 32, controlled by bit 6/1, will mute a minimum of 60 dB.

Table 8. Receive Gain Adjustment

Register 6 Bits 10...6	Gain		Register 6 Bits 10...6	Gain
00110	–13.5 dB		10000	+1.5 dB
00111	–12.0 dB		10001	+3.0 dB
01000	–10.5 dB		10010	+4.5 dB
01001	–9.0 dB		10011	+6.0 dB
01010	–7.5 dB		10100	+7.5 dB
01011	–6.0 dB		10101	+9.0 dB
01100	–4.5 dB		10110	+10.5 dB
01101	–3.0 dB		10111	+12.0 dB
01110	–1.5 dB		11000	+13.5 dB
01111	0.0 dB		11001	+15.0 dB

Power Amplifiers

The power amplifiers (Pins 28, 29, 31) are designed to drive the earpiece in a handset, or the telephone line via a hybrid circuit in the base unit. Each output (PAO+ and PAO–) can source and sink 5 mA, and can swing 2.0 V_{pp} each. The gain of the amplifiers is set with a feedback resistor from Pin 29 to 31, and an input resistor at Pin 31. The differential gain is 2x the resistor ratio. Capacitors can be used for frequency shaping. The pins' dc level is VB (≈1.5 V).

The Mute switch, controlled with bit 6/0, will provide 90 dB of muting with a 50 kΩ feedback resistor. The amount of muting will depend on the value of the feedback resistor.

Reference Clock

The reference clock provides the frequency basis for the three PLLs, the switched capacitor filters, and the CVSD Encoder section. The source for the reference clock can be a crystal in the range of 4.0 to 18.25 MHz connected to Pins 14 & 15, or it can be an external source connected to F_{ref} In (Pin 14). The reference frequency is directed to:

a. A programmable 12–bit counter to provide the reference frequency for the three PLLs. The 12–bit counter is to be set such that, in conjunction with the programmable counters within each PLL, the proper frequencies can be produced by each VCO.
b. A programmable 6–bit counter, followed by a ÷2 stage, to set the frequency for the switched capacitor filters to 256 kHz, or as close to that as possible.
c. A programmable 6–bit counter which provides the 16x clock for the Clock Recovery block. This is followed by a ÷16 stage which provides the CVSD Encoder clock. This is followed by a ÷32 stage, and a programmable 4–bit counter which sets the delay for the Idle Channel Detect circuit.

Transmit and Receive (LO1) PLL Sections

The transmit and receive PLLs (Pins 6 to 9 and 1 to 4, respectively) are designed to be part of a 900 MHz system. In a typical application the Transmit PLL section will be set up to generate the transmit frequency, and the Receive PLL section will be set up to generate the LO1 frequency. The two sections are identical, and function independently. External requirements for each include a low pass filter, a 900 MHz VCO, and a 64/65 or 128/129 dual modulus prescaler.

The frequency output of the VCO is to be reduced by the dual modulus prescaler, and then input to the MC33410 (at Pin 2 or 8). That frequency is then further reduced by the programmable 13–bit counter (bits 1/19–7 or 2/19–7), and provided to one side of the Phase Detector, where it is compared with the PLL reference frequency. The output of the phase detector (at Pin 4 or 6) is a bi–directional charge pump which drives the VCO through the low pass filter. Bits 1/20 and 2/20 set the gain of each of the two charge pumps to either 100/2π μA/Radian or 400/2π μA/Radian. The polarity of the two phase detector outputs is set with bits 7/22 and 7/23. If the bit=0, the appropriate PLL is configured to operate with a non–inverting low pass filter/VCO combination. If the low pass filter/VCO combination is inverting, the polarity bit should be set to 1.

The 7–bit A and A' counters (bits 1/6–0 and 2/6–0) are to be set to drive the Modulus Control input of the 64/65 or 128/129 dual modulus prescalers. The Modulus Control outputs (Pins 1 and 9) can be set to either a voltage mode or a current mode with bit 7/13.

To calculate the settings of the N and A registers, the following procedure is used:

$$\frac{f_{VCO}}{f_{PLL}} = Nt \text{ (Nt must be an integer)} \qquad \text{Equation 1}$$

$$\frac{Nt}{P} = N \qquad \text{Equation 2}$$

A = Remainder of Equation 2 (decimal part of N x P) — Equation 3

where: f_{VCO} = the VCO frequency
f_{PLL} = the PLL Reference Frequency set within the MC33410
P = the smaller divisor of the dual modulus prescaler (64 for a 64/65 prescaler)

N = the whole number portion is the setting for the N (or N') counter within the MC33410

A = the setting for the A (or A') counter within the MC33410

For example, if the VCO is to provide 910 MHz, and the internal PLL reference frequency is 50 kHz, then the equations yield:

$$Nt = \frac{910 \times 10^6}{50 \times 10^3} = 18,200$$

$$N = \frac{18,200}{64} = 284.375$$

$$A = 0.375 \times 64 = 24$$

The N register setting is 284_d (0 0001 0001 1100), and the A register setting is 24_d (001 1000).

2nd LO (LO2)

This PLL is designed to be the 2nd Local Oscillator in a typical 900 MHz system, and is designed for frequencies up to 80 MHz. The VCO and varactor diodes are included, and are to be used with an external tank circuit (Pins 43 to 45).

Bits 7/20–18 are used to select an internal capacitor, with a value in the range of 0 to 7.6 pF, to parallel the varactor diodes and the tank's external capacitor. This permits a certain amount of fine tuning of the oscillator's performance. See Table 9.

A buffered output is provided to drive, e.g., a mixer. The frequency is set with the programmable 14–bit counter (bits 3/13–0) in conjunction with the PLL reference frequency. For example, if the reference frequency is 50 kHz, and the 2nd LO frequency is to be 63.3 MHz, the 14–bit counter needs to be set to 1266_d (00 0100 1111 0010). The output level is dependent on the value of the impedance at Pin 41, partly determined by the external pullup resistor.

The output of the phase detector is a bi–directional charge pump which drives the varactor diodes through an external low pass filter. Bit 3/14 sets the gain of the charge pump to either 100/2π μA/Radian or 400/2π μA/Radian. Bit 7/21 sets its polarity – if 0, the PLL is configured to operate with a non–inverting low pass filter/VCO combination. If the low pass filter/VCO combination is inverting, the polarity bit should be set to 1.

Table 9. LO2 Capacitor Selection

Register 7 Bits 20–18	Capacitor Value		Register 7 Bits 20–18	Capacitor Value
000	0 pF		100	4.3 pF
001	1.1 pF		101	5.4 pF
010	2.2 pF		110	6.5 pF
011	3.3 pF		111	7.6 pF

VB Reference Voltage

The VB voltage (≈1.5 V) is available at Pin 33. It will have a production tolerance of ±6%, and can be adjusted over a ±9% range using bits 3/20–17. The adjustment steps will be ≈1.2% each. VB can be used to bias external circuitry, as long as the load current on this pin does not exceed 10 μA.

Low Battery/Carrier Detect

This circuit will provide an indication of either Low Battery voltage, or a low carrier signal applied to Pin 36 (MP1) from an RSSI circuit. The desired mode is selected with bit 6/5.

A) Low Battery Mode (Bit 6/5 = 0)

The supply voltage at Pin 18 is applied to the comparator through an internal resistor divider, and is compared to the internal reference VB (≈1.5 V). The comparator has ≈15 mV of hysteresis, measured at V_{CC}. The resistor divider is adjustable using bits 3/23–21. The Low Battery threshold voltage will then be equal to the VB voltage multiplied by the factor listed in Table 10. For example, if VB = 1.5 V, and bits 3/23–21 = 011, the threshold will be 3.21 V.

B) Carrier Detect Mode (Bit 6/5 = 1)

Pin 36 (MP1) must be set to the Hi–Z/CD Input mode by setting bits 7/5–4 to 11. MP1 will then be an input with an input impedance of ≈600 kΩ, referenced to VB. An analog signal applied to MP1 will be applied to the comparator through an internal adjustable gain stage (adjustable using bits 3/23–21), and is compared to the internal reference VB. The comparator has ≈18.0 mV of hysteresis, measured at Pin 36. The threshold voltage will then be equal to the VB voltage multiplied by the factor listed in Table 10. For example, if VB = 1.5 V, and bits 3/23–21 = 011, the threshold will be 0.576 V.

Table 10. LB/CD Threshold Adjustment Factor

Register 3 Bits 23–21	Low Battery Mode	Carrier Detect Mode
000	1.96	0.574
001	2.02	0.524
010	2.08	0.453
011	2.14	0.384
100	2.19	0.314
101	2.25	0.247
110	2.30	0.177
111	2.37	0.110

The comparator output is at bit 5/23, and at Pin 16 (open collector output). The outputs are high if the monitored V_{CC} voltage is above the threshold, or if the Carrier signal is below the threshold. Pin 16 requires an external pullup resistor. When this circuit is disabled (bit 5/10 = 1), bit 5/23 and Pin 16 will be high.

MPU Serial Interface

The MPU Serial Interface is a 3–wire interface, consisting of a Clock line, an Enable line, and a bi–directional Data line. The interface is always active, i.e. it cannot be powered down as all other sections of the MC33410 are disabled and enabled through this interface.

The clock must be supplied to the MC33410 at Pin 11 to write or read data, and can be any frequency up to 2.0 MHz. The clock need not be present when data is not being transferred. The Enable line must be low when data is not being transferred.

Internally there are 10 data registers, 24 bits each, addressed with four bits ranging from $1 to $A. Register 10, and bits 23–21 of register 5 contain data to be read out by the microprocessor, while all other register bits are to be written to by the microprocessor. The contents of the 10 registers can be read out at any time. All bits are written in, or read out, on the clock's positive transition. The write and read operations are as follows:

a) Write Operation:

To write data to the MC33410, the following sequence is required (see Figure 3):

5. The Enable line is taken high.
6. Five bits are entered:
   – The first bit must be a 0 to indicate a Write operation.
   – The next four bits identify the register address (0001–1010). The MSB is entered first.
7. After the 5th clock pulse is low, the Enable line is taken low. At this transition, the address is latched in and decoded.
8. The Enable line is maintained low while the data bits are clocked in. The MSB is entered first, and the LSB last. If 24 bits are written to a register which has less than 24 active bits (e.g., register 6), the unassigned bits are to be 0.
9. After the last bit is entered, the Enable line is to be taken high and then low. The falling edge of this pulse latches in the just entered data. The clock line can be at a logic high or low, but must not transition in either direction during this Enable pulse.
10. The Enable line must then be kept low until the next communication.

Note: If less than 24 bits are to be written to a data register, it is not necessary to enter the full 24 bits, as long as they are all lower order bits. For example, if bits 0–6 of a register are to be updated, they can be entered as 7 bits with 7 clock cycles in step 4 above. However, if this procedure is used, a minimum of 4 bits, with 4 clock pulses, must be entered.

Figure 3. Writing Data to the MC33410

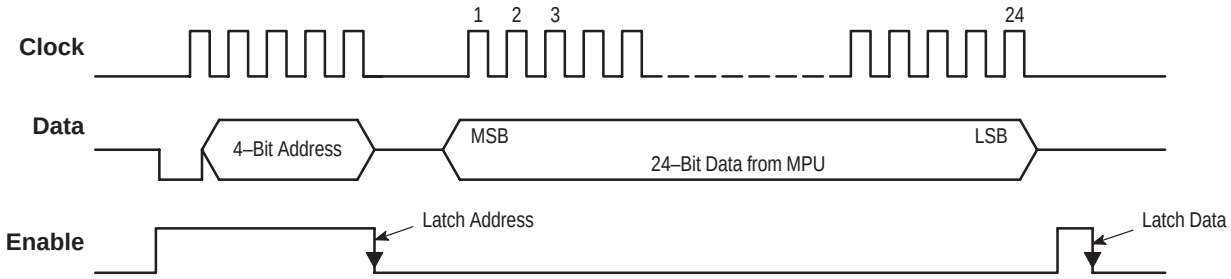
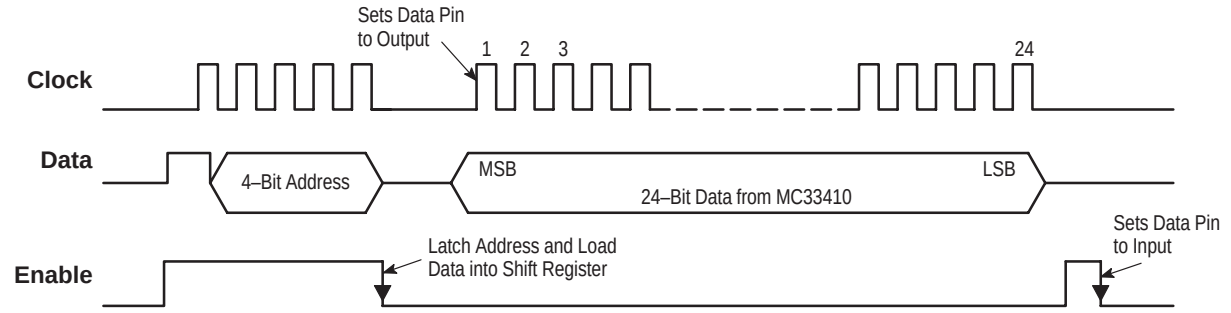


Figure 4. Reading Data from the MC33410



b) Read Operation:

To read the output bits (bits 5/23–21, or all of register 10), or the contents of any register, the following sequence is required (see Figure 4):

1. The Enable line is taken high.
2. Five bits are entered:
   – The first bit must be a 1 to indicate a Read operation.
   – The next four bits identify the register address (0001–1010). The MSB is entered first.
3. After the 5th clock is taken low, the Enable line is taken low. At this transition, the address is latched in and decoded, and the contents of the selected register is loaded into the 24–bit output shift register. At this point, the Data line (Pin 12) is still an input.
4. While maintaining the Enable line low, the data is read out. The first clock rising edge will change the Data line to an output, and the MSB will be present on this line.
5. The full contents of the register are then read out (MSB first, LSB last) with a total of 24 clock rising edges, including the one in step 4 above. It is recommended that the MPU read the bits at the clock's falling edge. If only bit 23, 22, or 21 of register 5 are to be read, this can be done with one, two, or three clock rising edges, respectively.
6. After the last clock pulse, the Enable line is to be taken high and then low. The falling edge of this pulse returns the Data pin to be an input. The clock line can be at a logic high or low, but must not transition in either direction during this Enable pulse.
7. The Enable line must then be kept low until the next communication.

Data Modem Mode

For applications where the MC33410 is to be used in a 900 MHz wireless system for transmitting data only (non–voice), a mode can be set which bypasses the speech digitizing sections. The resulting configuration makes use of those sections associated with data only, i.e., the scrambler, descrambler, and clock recovery section. Also functional are the three PLLs, the audio receive path (Pins 34 to 28), the transmit audio path (Pins 23 to 20), and the Low Battery circuit (but not the Carrier Detect mode).

In this mode, the MC33410 will provide the transmit data clock from the crystal, in conjunction with the internal 6–bit counter (bits 4/23–18) and the ÷16 block associated with that counter. The transmit data clock is available at Pin 13, and can be used to synchronize the external data source. The T_X

data is input at Pin 39, passes through the scrambler, and outputs at Pin 17.

The demodulated data from the RF receiver is input at Pin 38, and is applied to the data slicer, and the clock recovery block. The recovered clock is output at Pin 12. The data passes through the descrambler, and is output at Pin 36.

Figure 5 is a diagram of the data paths through the MC33410.

The procedure for entering the Data Modem mode is in Table 11:

Table 11. Entering Data Modem Mode

Function	Bits	Bit Value
Set T_X Clock to desired frequency T_X Clk = $F_{crystal}$/(16 x Counter).	4/23 – 18	As Desired
Set Scrambler & Descrambler tap setting (Bit 7/1 = 0).	7/10 – 8	As Desired
Bypass Data Detect.	7/3	1
Set MP1 to Data Detect Output.	7/5 – 4	01
Set Test Mode bits to connect Encode Clock to Status (Pin 13).	7/17 – 15	110
Set Data Modem Mode (MP2 to scrambler Input).	5/20	1
Write to Register 11 as shown in Figure 6 to configure Pin 12.	N/A	N/A

The above sequence is not critical, except that the last two steps must be the setting of bit 5/20, and writing to register 11. Writing to register 11 is shown in Figure 6.

Figure 5. Data Modem Mode Configuration

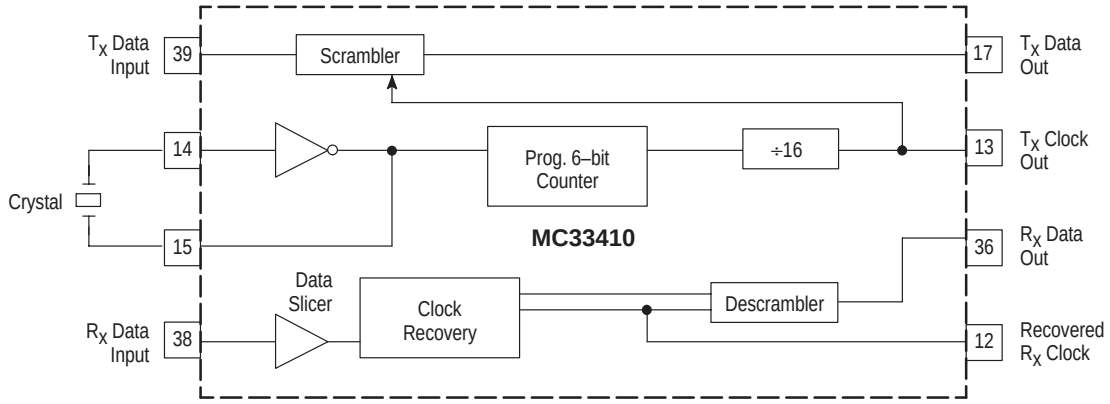
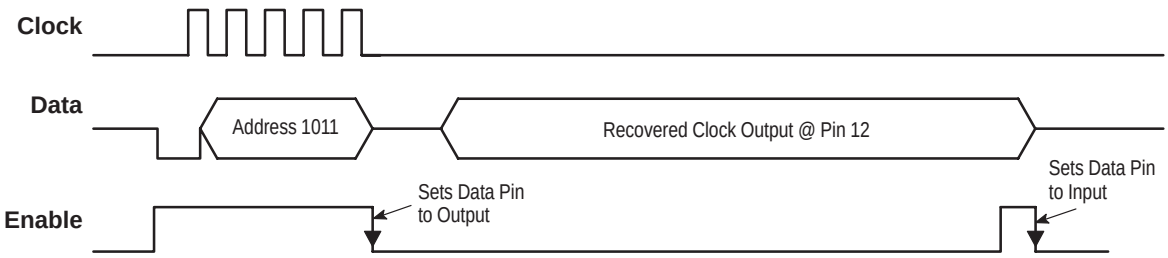


Figure 6. Entering/Exiting Data Modem Mode



After address 11 is clocked in, the Enable falling edge will cause Pin 12 (Data) to switch to an output, providing the recovered clock. The microprocessor's data pin must be changed to an input prior to this falling edge. This sequence is effective only if bit 5/20 is set to a 1.

During the time that recovered clock is available at Pin 12, the microprocessor port is unavailable for any control functions.

To exit the Data Modem mode, the Enable line is to be taken high and low (the clock is to be stable during this active high pulse). The falling edge will set Pin 12 to be an input, allowing normal use of the microprocessor port. The next step is to set bit 5/20 to a 0. Other register bits can then be set as needed.

To prevent inadvertent incorrect operation of the microprocessor port, bit 5/20 must always be set to 0 when the Data Modem mode is not in use.

Power Supply/Power Saving Modes

The power supply voltage, applied to all V_{CC} pins, can range from 2.7 to 5.5 V. All V_{CC} pins must be within ±0.5 V of each other, and each must be bypassed. It is recommended a ground plane be used, and all leads to the MC33410 be as short and direct as possible. The supply and ground pins are distributed as follows:

1. Pins 18, 27 and 37 are internally connected together, and provide power to the audio amplifiers, filters, CVSD encoder and decoder, and the low frequency (CVSD rate) logic circuits. Pins 21, 30 and 40 are the ground pins for these sections.
2. Pin 3 provides power to the R_X PLL section. Pin 5 is the ground pin.
3. Pin 7 provides power to the T_X PLL section, and the MPU interface. Pin 5 is the ground pin.
4. Pin 42 provides power to the 2nd LO section. Pins 46 and 48 are the ground pins.

To conserve power, various sections can be individually disabled, using bits 5/10–0 (setting a bit to 1 disables the section).

1. Reference Oscillator Disable (bit 5/0) – The reference oscillator at Pins 14 and 15 is disabled, thereby denying a clock to the three PLLs, the CVSD Encoder, and the switched capacitor filters.
2. T_X PLL Disable (bit 5/1) – The 13–bit and 7–bit counters, input buffer, phase detector, and modulus control blocks are disabled. The charge pump output at Pin 6 will be in a Hi–Z state.
3. R_X PLL Disable (bit 5/2) – The 13–bit and 7–bit counters, input buffer, phase detector, and modulus control blocks are disabled. The charge pump output at Pin 4 will be in a Hi–Z state.
4. LO2 PLL Disable (bit 5/3) – The VCO, 14–bit counter, output buffer, and phase detector are disabled. The charge pump output at Pin 47 will be in a Hi–Z state.
5. R_X Data Path Disable (bit 5/4) – The data slicer, clock recovery block, descrambler, data detect register, and the status output circuit are disabled. The state of the status line (Pin 13 and bit 5/22) will not change upon disabling this section.
6. CVSD Decoder Disable (bit 5/5) – The CVSD Decoder and the R_X 1010 Generator are disabled.
7. R_X Audio Path Disable (bit 5/6) – The anti–aliasing filter, low pass filter, and variable gain stage are disabled.
8. Power Amplifier Disable (bit 5/7) – The two power amplifiers are disabled. Their outputs will go to a Hi–Z state.
9. T_X Audio Path Disable (bit 5/8) – Disables the microphone amplifier, low pass filter, and smoothing filter.
10. CVSD Encoder Disable (bit 5/9) – The CVSD Encoder, Idle Channel detect circuit, the T_X 1010 Generator, the T_X Data register, and the scrambler are disabled.
11. Low Battery/Carrier Detect Disable (bit 5/10) – The LB/CD circuit is disabled. The output, at bit 5/23 and Pin 16 will be at a logic high.
12. Idle Channel Detect Disable (bit 5/18) – Powers down the Idle Channel Detect circuit.

Note: The 12–bit reference counter is disabled if the three PLLs are disabled (bits 5/1–3 = 1).

Table 12. Control Bit Listing (By Register Number)

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
1 (23 bits total)	6 – 0	1000000	Sets the 7–bit T_X A counter for the T_X PLL.
	19 – 7	10....0	Sets the 13–bit T_X N counter for the T_X PLL.
	20	0	Sets the T_X phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
	22, 21	00	Sets CVSD Decoder minimum step size per Table 3.
2 (23 bits total)	6 – 0	1000000	Sets the 7–bit R_X A' counter for the R_X PLL.
	19 – 7	10....0	Sets the 13–bit R_X N' counter for the R_X PLL.
	20	0	Sets the R_X phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
	22, 21	00	Sets CVSD Encoder minimum step size per Table 3.
3 (24 bits total)	13 – 0	10....0	Sets the 14–bit counter for the 2nd LO.
	14	0	Sets the LO2 phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
	16 – 15	11	Set the CVSD encoder/decoder for the selected clock rate. (Table 2)
	20 – 17	0111	Adjusts the VB reference voltage (≈1.5 V) to improve low battery detection accuracy. Total adjustment range is ≈±9%.
	23 – 21	011	Selects the threshold for Low Battery Detection or Carrier Signal Detection. See Table 10.
4 (24 bits total)	11 – 0	$800	Sets the 12–bit counter for the PLL Reference Clock.
	17 – 12	100000	Sets the 6–bit counter for the Switched Capacitor Filter clock.
	23 – 18	100000	Sets the 6–bit counter to set the CVSD Encoder clock rate.
5 (24 bits total)	0	0	Power down the Reference Oscillator
	1	0	Power down the T_X PLL.
	2	0	Power down the R_X PLL.
	3	0	Power down the LO2 PLL.
	4	0	Power down the R_X Data Path. Includes Data Slicer, Clock Recovery, Descrambler, Data Detect, and Status circuits.
	5	0	Power down the CVSD Decoder.
	6	0	Power down the R_X Audio path (Pin 32 to 30). Includes AALPF, LPF, and Gain Adjust circuits.
	7	0	Power down the Power Amplifiers (Pins 27, 28)
	8	0	Power down the T_X Audio Path (Pin 25 to 22). Includes micro–phone amplifier, LPF, and Smoothing LPF circuits.
	9	0	Power down the CVSD Encoder, Idle Channel Detector, 1010 Generator, T_X Data Register, and Scrambler circuits.
	10	0	Power down the Low Battery/Carrier Detect Circuit.
	14 – 11	0111	Sets the 4–bit counter to set the response delay for the idle channel detect circuit.
	17 – 15	100	Sets the idle channel detect threshold level. See Table 4.
	18	0	Power down the Idle Channel Detect Circuit.
	19	0	Inverts the Data Slicer output.
	20	0	Sets the Data Modem mode of operation.
	21	N/A	Indicates an idle channel condition has been detected (Output). This output is unaffected by bit 7/2.
	22	N/A	The Status Output (same as Pin 13) is read out from this bit.
	23	N/A	The output of the Low Battery/Carrier Detect Circuit is read from this bit.

Table 12. Control Bit Listing (By Register Number) (continued)

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
6 (16 bits total)	0	0	Mutes the power amplifiers (Pins 27 to 29).
	1	0	Mutes the receive speech processing path (Pin 30).
	2	0	Mutes the transmit speech processing path (Pin 22).
	3	0	Selects the R_X 1010 Generator to the CVSD decoder.
	4	0	Selects the T_X 1010 Generator to the scrambler.
	5	0	Sets Carrier Detect Mode vs. Low Battery mode.
	10 – 6	01111	Provides 19 steps, 1.5 dB each (28.5 dB range), of gain adjust in the receive speech audio path (Pins 32 to 30). See Table 8.
	15 – 11	00100	Provides 4 steps of 4.0 dB each, for the remote gain adjust in the transmit speech audio path (Pins 23 to 20).
7 (24 bits total)	0	0	Bypass the Clock Recovery Block (Data slicer output goes directly to the descrambler).
	1	0	Bypass the scrambler and descrambler.
	2	0	Disables the automatic idle channel detect at the CVSD encoder. Bit 5/21 is still active.
	3	0	Bypass the Data Detect block (Descrambler output goes directly to the CVSD Decoder).
	5 – 4	00	Determines the function for Pin 36 (MP1). See Table 6.
	7 – 6	00	Determines the function for Pin 39 (MP2). See Table 7.
	10 – 8	010	Selects one of 8 programmable taps in the scrambler and descrambler. See Table 5.
	11	1	Sets the code word size to be sent out via the T_X Data Register to 24 bits. If this bit is 0, the code word size is 16 bits.
	12	1	Sets the data word size to be sent out via the T_X Data Register to 24 bits. If this bit is 0, the data word size is 16 bits.
	13	0	Sets the FT_X MC and FR_X MC output level to be from ground to V_{CC}. If this bit is 0, the output level is ±100 μA.
	14	0	Disables the CVSD charge compensation circuit.
	17 – 15	000	Test modes for production testing only.
	20 – 18	000	Selects the value of the internal capacitor between Pins 43 to 45, to fine tune the LO2 tank circuit. See Table 9.
	21	0	Sets the polarity of the 2nd LO phase detector charge pump output for an inverting low pass filter/VCO combination.
	22	0	Sets the polarity of the R_X phase detector charge pump output for an inverting low pass filter/VCO combination.
	23	0	Sets the polarity of the T_X phase detector charge pump output for an inverting low pass filter/VCO combination.
8	23 – 0	$000000	Code word for the T_X Data Register is entered into this register.
9	23 – 0	$000000	Data word for the T_X Data Register is entered into this register.
10	23 – 0	$000000	The data word received into the R_X Data Register is read out via the μP port from this register.

Table 13. Control Bit Listing (By Function)

PLL Controls

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
1	6 – 0	1000000	Sets the 7–bit T_X A counter for the T_X PLL.
1	19 – 7	10....0	Sets the 13–bit T_X N counter for the T_X PLL.
2	6 – 0	1000000	Sets the 7–bit R_X A' counter for the R_X PLL.
2	19 – 7	10....0	Sets the 13–bit R_X N' counter for the R_X PLL.
3	13 – 0	10....0	Sets the 14–bit counter for the 2nd LO.
4	11 – 0	$800	Sets the 12–bit counter for the PLL Reference Clock.
7	13	0	Sets the FT_X MC and FR_X MC output level to be from ground to V_{CC}. If this bit is 0, the output level is ±100 μA.

PLL Phase Detectors

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
1	20	0	Sets the T_X phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
2	20	0	Sets the R_X phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
3	14	0	Sets the LO2 phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
7	20 – 18	000	Selects the value of the internal capacitor between Pins 43 to 45, to fine tune the LO2 tank circuit. See Table 9.
7	21	0	Sets the polarity of the 2nd LO phase detector charge pump output for an inverting low pass filter/VCO combination.
7	22	0	Sets the polarity of the R_X phase detector charge pump output for an inverting low pass filter/VCO combination.
7	23	0	Sets the polarity of the T_X phase detector charge pump output for an inverting low pass filter/VCO combination.

CVSD Controls

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
1	22, 21	00	Sets CVSD Decoder minimum step size per Table 3.
2	22, 21	00	Sets CVSD Encoder minimum step size per Table 3.
3	16 – 15	11	Set the CVSD encoder/decoder for the selected clock rate. (Table 2)
4	23 – 18	100000	Sets the 6–bit counter to set the CVSD Encoder clock rate.
6	3	0	Selects the R_X 1010 Generator to the CVSD decoder.
6	4	0	Selects the T_X 1010 Generator to the scrambler.
7	14	0	Disables the CVSD charge compensation circuit, which affects idle channel performance.

Idle Channel Detector

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
5	14 – 11	0111	Sets the 4–bit idle channel counter to set the response delay for the idle channel detect circuit.
5	17 – 15	100	Sets the idle channel detect threshold level. See Table 4.
5	21	N/A	Indicates an idle channel condition has been detected (Output). This output is unaffected by bit 7/2.
7	2	0	Disables the automatic idle channel detect at the CVSD encoder. Bit 5/21 is still active.

Table 13. Control Bit Listing (By Function) (continued)

Data Transmission/Reception

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
5	19	0	Inverts Data Slicer output.
5	20	0	Sets Data Modem mode.
5	22	N/A	The Status Output (same as Pin 13) is read out from this bit. A logic 1 indicates the Data Detect register has detected a code word.
7	0	0	Bypass the Clock Recovery Block (Data slicer output goes directly to the descrambler).
7	3	0	Bypass the Data Detect block (Descrambler output goes directly to the CVSD Decoder).
7	11	1	Sets the code word size to be sent out via the T_X Data Register to 24 bits. If this bit is 0, the code word size is 16 bits.
7	12	1	Sets the data word size to be sent out via the T_X Data Register to 24 bits. If this bit is 0, the data word size is 16 bits.
8	23 – 0	$000000	Code word for the T_X Data Register is entered into this register.
9	23 – 0	$000000	Data word for the T_X Data Register is entered into this register.
10	23 – 0	$000000	The data word received into the R_X Data Register is read out via the µP port from this register.

Scrambler/Descrambler

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
7	1	0	Bypass the scrambler and descrambler.
7	10 – 8	010	Selects one of 8 programmable taps in the scrambler and descrambler. See Table 5.

Multi Purpose Pin Control

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
7	5 – 4	00	Determines the function for Pin 36 (MP1). See Table 6.
7	7 – 6	00	Determines the function for Pin 39 (MP2). See Table 7.

Audio Paths

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
4	17 – 12	100000	Sets the 6–bit counter for the Switched Capacitor Filter clock.
6	0	0	Mutes the power amplifiers (Pins 27 to 29).
6	1	0	Mutes the receive speech processing path (Pin 30).
6	2	0	Mutes the transmit speech processing path (Pin 22).
6	10 – 6	01111	Provides 19 steps, 1.5 dB each (28.5 dB range), of gain adjust in the receive speech audio path (Pins 32 to 30). See Table 8.
6	15 – 11	00100	Provides 4 steps of 4.0 dB each, of gain adjust in the transmit speech audio path (Pins 23 to 20).

Low Battery/Carrier Detection

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
3	20 – 17	0111	Adjusts the VB reference voltage (≈1.5 V) to improve low battery detection accuracy. Total adjustment range is ≈±9%.
3	23 – 21	011	Selects the threshold for Low Battery Detection or Carrier Signal Detection. See Table 10.
5	23	N/A	The output of the Low Battery/Carrier Detect Circuit is read from this bit.
6	5	0	Sets Carrier Detect Mode vs. Low Battery Mode

Table 13. Control Bit Listing (By Function) (continued)

Power Down Control

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
5	0	0	Power down the Reference Oscillator
5	1	0	Power down the T_X PLL.
5	2	0	Power down the R_X PLL.
5	3	0	Power down the LO2 PLL.
5	4	0	Power down the R_X Data Path. Includes Data Slicer, Clock Recovery, Descrambler, Data Detect, and Status circuits.
5	5	0	Power down the CVSD Decoder.
5	6	0	Power down the R_X Audio path (Pin 32 to 30). Includes AALPF, LPF, and Gain Adjust circuits.
5	7	0	Power down the Power Amplifiers (Pins 27, 28)
5	8	0	Power down the T_X Audio Path (Pin 25 to 22). Includes micro–phone amplifier, LPF, and Smoothing LPF circuits.
5	9	0	Power down the CVSD Encoder, Idle Channel Detector, 1010 Generator, T_X Data Register, and Scrambler circuits.
5	10	0	Power down the Low Battery/Carrier Detect Circuit.
5	18	0	Power down the Idle Channel Detection Circuit.

Table 14. Register Map

Register Address	Register Number	MSB 23	22	21	20	19	18	17	16	15	14	13	12
0001	1		CVSD Decoder Minimum Step Size		Tx PhDet. Curr. Sel.	13 Bit Tx N Counter Divide Value (Bits 19 – 7)							
0010	2		CVSD Encoder Minimum Step Size		Rx PhDet. Curr. Sel.	13 Bit Rx N' Counter Divide Value (Bits 19 – 7)							
0011	3	Sets Low Battery/Carrier Detect Threshold			Adjust VB Reference Voltage				Set CVSD for the selected Clock Rate		LO2 PhD Curr. Sel.	14 bit LO2 Counter Divide Value (Bits 13 – 0)	
0100	4	6 Bit Encode Clock Counter Divide Value						6 Bit Switched Capacitor Filter Counter Divide Value					
0101	5	LB/CD Det. Out	Status Output	Idle Chan. Output	Data Modem Mode	Invert Data Slicer	Idle Channel Disable	Sets Idle Channel Threshold Level			4 Bit Idle Channel Counter Delay Value (Bits 14 – 11)		
0110	6									Remote Gain Adjust (Bits 15 – 11)			
0111	7	Tx Phase Detector Polarity	Rx Phase Detector Polarity	LO2 Ph. Detector Polarity	LO2 Capacitor Select			Production Test Modes & Data Modem Mode			Idle Charge Disable	FTxMC/ FRxMC Level	Data Word Size (16/24 bit)
1000	8	16 or 24 Bit Code Word for the Tx Data Register (Bits 23 – 0)											
1001	9	16 or 24 Bit Data Word for the Tx Data Register (Bits 23 – 0)											
1010	10	16 or 24 Bit Data Word Output from the Rx Data Register (Bits 23 – 0)											

Register Address	Register Number	11	10	9	8	7	6	5	4	3	2	1	LSB 0
0001	1	13 Bit Tx N Counter Divide Value (Bits 19 – 7)					7 Bit Tx A Counter Divide Value						
0010	2	13 Bit Rx N' Counter Divide Value (Bits 19 – 7)					7 Bit Rx A' Counter Divide Value						
0011	3	14 bit LO2 Counter Divide Value (Bits 13 – 0)											
0100	4	12 Bit Reference Counter Divide Value											
0101	5	4 Bit Idle Channel Ctr. Value	LB/CD Detect Disable	CVSD Encoder Disable	Tx Audio Path Disable	Power Amplifier Disable	Rx Audio Path Disable	CVSD Decoder Disable	Rx Data Path Disable	LO2 PLL Disable	Rx PLL Disable	Tx PLL Disable	Ref. Osc. Disable
0110	6	Remote Gain Adj.	Rx Audio Path Gain Adjust (28.5 dB range)					Set CD Mode	Tx 1010 Generator	Rx 1010 Generator	Mute Tx Audio	Mute Rx Audio	Mute Pwr. Amps
0111	7	Code Word Size (16/24 bit)	Scrambler/Descrambler Tap Selection			MP2 Mode (See Table 7)		MP1 Mode (See Table 6)		Bypass Data Detect	Disable Idle Chnl. Detection	Bypass Scrambler/ Descrambler	Bypass Clock Recovery
1000	8	16 or 24 Bit Code Word for the Tx Data Register (Bits 23 – 0)											
1001	9	16 or 24 Bit Data Word for the Tx Data Register (Bits 23 – 0)											
1010	10	16 or 24 Bit Data Word Output from the Rx Data Register (Bits 23 – 0)											

Note: Shaded areas represent output bits to be read out.

MOTOROLA

MC33411A/B

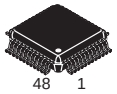
900 MHz Analog Cordless Phone Baseband with Compander

The MC33411 900 MHz Analog Cordless Phone Baseband system is designed to fit the requirements of a 900 MHz analog cordless telephone system. Included are three PLLs (Phase–Locked Loops). Two are intended for use with external VCOs and 64/65 or 128/129 dual modulus prescalers, and can control the transmit and receive (LO1) frequencies for 900 MHz communication. The third PLL is configured as the 2nd local oscillator (LO2), and is functional to 80 MHz. Also included are muting, audio gain adjust (internal and external), low battery/carrier detect, and a wide range for the PLL reference frequency. The power supply range is 2.7 to 5.5 V. ”A” version devices have programmable MCU clock out and reference oscillator disable functions, whereas these functions are always enabled for ”B” version devices.

- Complete Expander/Compressor for Superior Noise Rejection
- Two PLLs and a LO Suitable for a 900 MHz System
- Minimal External Components
- Transmit Path Includes Adjustable Gain Amplifier, Filters, Mute, Compressor with Bypass and Limiter
- Receive Path Contains Data Slicer, Adjustable Gain Amplifier, Sidetone Attenuator, Filters, Expander with Bypass, Mute, Volume Control and Power Amplifier
- Dual A/Ds are Provided to Monitor RSSI and V_{CC}
- Independent Power Amplifier with Differential Outputs and Mute
- Selectable Frequency for Switched Capacitor Filters, PLLs and the LO
- Reference Frequency Source can be a Crystal or System Clock
- Serial µP Port to Control Gain, Mute, Frequency Selection, Phase Detector Gain, Power Down Modes, Low Battery Detect and Others
- Power Supply Range: 2.7 to 5.5 V
- Power Down Modes for Power Conservation

900 MHz ANALOG CORDLESS PHONE BASEBAND WITH COMPANDER

SEMICONDUCTOR TECHNICAL DATA

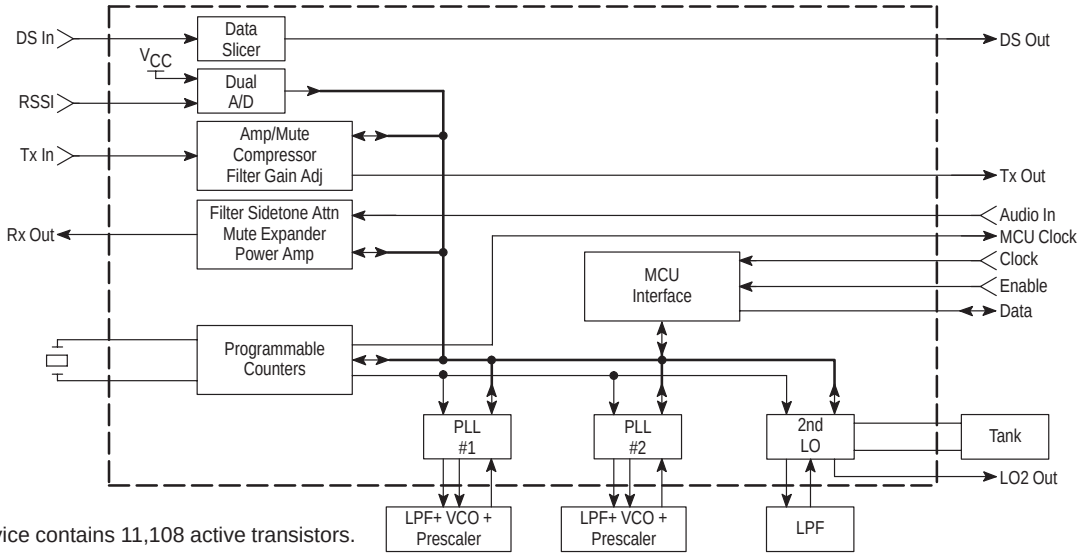


FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(LQFP–48)

ORDERING INFORMATION

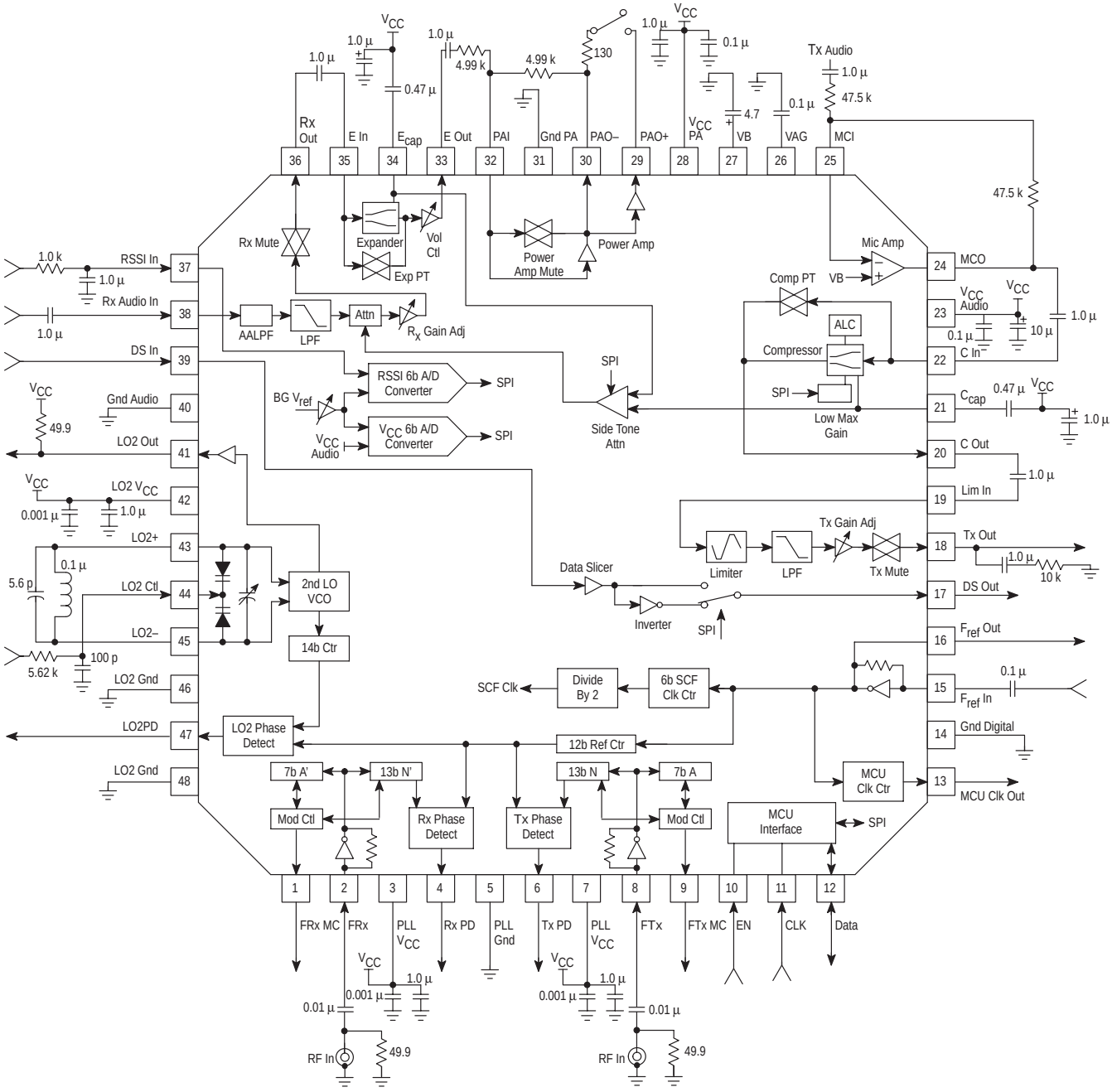
Device	Operating Temperature	Package
MC33411AFTA	T_A = –20 to 70°C	LQFP–48
MC33411BFTA		

Simplified Block Diagram



This device contains 11,108 active transistors.

Figure 1. Test Circuit



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 6.0	V
Junction Temperature	T_J	–6.5 to 150	°C
Maximum Power Dissipation	P_D	150	mW

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions, Electrical Characteristics tables or Pin Descriptions section.
2. Meets Human Body Model (HBM) ≤2000 V and Machine Model (MM) ≤200 V. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.6	5.5	Vdc
Operating Ambient Temperature	T_A	–20	–	70	°C
Input Voltage Low (Data, CLK, EN)	V_{il}	–	–	0.3	V
Input Voltage High (Data, CLK, EN)	V_{ih}	Tx PLL V_{CC} – 0.3	–	–	V
Frequency Range ($F_{ref\ in}$)	F_{range}	4.0	–	18.25	MHz
Bandgap Reference Voltage	V_B	–	1.5	–	V

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Static Current					
Active Mode (R5/8 to 0 = 0; R6/7 = 0)	ACT I_{CC}	–	15	20	mA
Receive Mode (R5/8, 7, 3, 2, 0 = 0; R6/7 = 0; R5/6,5,4,1 = 1)	Rx I_{CC}	–	10	13	mA
Standby Mode (R5/0 = 0; R6/7 = 0; R5/8 to 1 = 1)	STD I_{CC}	–	500	1500	µA
Inactive Mode, A only (R5/8 to 0 =1; R6/7 = 1)	INA I_{CC}	–	10	15	µA
Data Slicer Only	DS I_{CC}	–	100	–	µA
RSSI/Batt A/D Only	AD I_{CC}	–	70	–	µA
Tx Audio Only	TxA I_{CC}	–	1.4	–	mA
Rx Audio Only	RxA I_{CC}	–	1.4	–	mA
PA Only	PA I_{CC}	–	1.0	–	mA
2nd LO/F_{ref} Only	2LO I_{CC}	–	6.0	–	mA
Rx PLL/F_{ref} Only	RxPLL I_{CC}	–	1.0	–	mA
Tx PLL/F_{ref} Only	TxPLL I_{CC}	–	1.0	–	mA
Ref Osc Only, "A" version only	ROSC I_{CC}	–	500	–	µA
Reference Voltage, Unadjusted	V_B	1.38	1.5	1.62	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode, Rx Gain = 01111, Vol Adj = 0111, f_{in} = 1.0 kHz, unless otherwise noted.)

Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Rx AUDIO PATH							
Absolute Gain (V_{in} = –20 dBV)	Rx Audio In	E Out	G	–4.0	0	4.0	dB
Gain Tracking (Referenced to E_{out} for V_{in} = –20 dBV) V_{in} = –30 dBV V_{in} = –40 dBV	E In	E Out	G_t	 –21 –42	 –20 –40	 –19 –38	dB
Total Harmonic Distortion (V_{in} = –20 dBV)	Rx Audio In	PAO–	THD	–	0.7	1.0	%
Maximum Input Voltage (V_{CC} = 2.7 V)	Rx Audio In			–	–11.5	–	dBV
Maximum Output Voltage (Increase input voltage until output voltage THD = 5%, then measure output voltage)	E In	E Out	V_{Omax}	–2.0	0	–	dBV

NOTES: 1. Values specified are pure numbers to the base 10.
2. Typical performance parameters indicate the potential of the device under ideal operating conditions.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode, Rx Gain = 01111, Vol Adj = 0111, f_{in} = 1.0 kHz, unless otherwise noted.)

Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Rx AUDIO PATH (continued)							
Input Impedance		RxAudio In E In	Z_{in}	– –	600 7.5	– –	kΩ
Attack Time E_{cap} = 0.5 μF, R_{filt} = 40 k	E In	E Out	t_a	–	3.0	–	mS
Release Time E_{cap} = 0.5 μF, R_{filt} = 40 k	E In	E Out	t_r	–	13.5	–	mS
Compressor to Expander Crosstalk (V_{in} = –10 dBV, $V_{E\ In}$ = AC Gnd)	MCI	E Out	C_T	–	–90	–60	dB
Rx Muting (V_{in} = –20 dBV, Rx Gain Adj = 01111)	Rx Audio In	E Out	M_e	–	–84	–60	dB
Rx High Frequency Corner (V_{in} = –20 dBV) SCF Counter = 31_d	Rx Audio In	Rx Out	Rx f_{ch}	3.6	3.8	4.0	kHz
Low Pass Filter Passband Ripple (V_{in} = –20 dBV)	Rx Audio In	Rx Out	Ripple	–	0.4	0.6	dB
Rx Gain Adjust Range	Rx Audio In	Rx Out	Rx Range	–	–9.0 to 10	–	dB
Rx Gain Adjust Steps	Rx Audio In	Rx Out	Rx n	–	20	–	
Audio Path Noise, C–Message Weighting (V_{in} = AC Gnd)	Rx Audio In	 Rx Out E Out PA Out	EN	 – – –	 –85 <–95 <–95	 – – –	dBV
Volume Control Adjust Range	Rx Audio In	E Out	$V_{CtRange}$	–	–14 to 16	–	dB
Volume Control Levels	E In	E Out	V_{cn}	–	16	–	
Side Tone Attenuate Selections	Rx Audio In	Rx Out	STA_n	–	4	–	
Side Tone Attenuate (Referenced to E In) Selection = 00 Selection = 01 Selection = 10 Selection = 11		E Out	STA	 – – – –	 0.0 1.5 3.0 5.2	 – – – –	dB
Side Tone Attenuate Threshold (C Out/E In)			STA_{thr}	–	–3.0	–	dB
POWER AMP/MUTE (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode, f_{in} = 1.0 kHz)							
Output Swing, ±5.0 mA load (V_{PAO+} @ –5.0 mA – V_{PAO+}@ 5.0 mA)	PAI	PAO+	V_{Omax}	1.3	2.4	–	V_{pp}
Output Swing, ±5.0 mA load ($V_{PAO–}$ @ –5.0 mA – $V_{PAO–}$@ 5.0 mA)	PAI	PAO–	V_{Omax}	1.3	2.4	–	V_{pp}
Output Swing, No Load	PAI	PAO+	V_{Omax}	–	2.7	–	V_{pp}
Output Swing, No Load	PAI	PAO–	V_{Omax}	–	2.7	–	V_{pp}
Maximum Output Current		PAO–, PAO+	I_{Omax}	–	±5.0	–	mA
Power Amp Mute (V_{in} = –20 dBV, RL = 130 Ω)	PAI	PAO–	M_{sp}	–	–92	–60	dB
MIC AMP (V_{CC} = 3.6 V, T_A = 25°C, Active Mode, f_{in} = 1.0 kHz)							
Open Loop Gain	MCI	MCO	AVOL	–	100.000	–	V/V
Gain Bandwidth	MCI	MCO	GBW	–	100	–	kHz
Maximum Output Swing (RL = 10 kΩ)	MCI	MCO	V_{Omax}	–	3.2	–	V_{pp}

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ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode, Rx Gain = 01111, Vol Adj = 0111, f_{in} = 1.0 kHz, unless otherwise noted.)

Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Tx AUDIO PATH (V_{CC} = 3.6 V, Limiter, Mutes, ALC disabled, T_A = 25°C, Gain = 1, Active Mode, f_{in} = 1.0 kHz)							
Absolute Gain (V_{in} = –10 dBV)	MCI	TX Out	G	–4.0	0	4.0	dB
Gain Tracking (Referenced to Tx Out for V_{in} = –10 dBV) V_{in} = –30 dBV V_{in} = –40 dBV	MCI	Tx Out	G_t	 –11 –17	 –10 –15	 –9.0 –13	dB
Total Harmonic Distortion (V_{in} = –10 dBV)	MCI	Tx Out	THD	–	0.5	1.2	%
Maximum Output Voltage (Increase input voltage until output voltage THD = 5%, then measure output voltage. Tx Gain Adj = 8.0 dB)	MCI	Tx Out	V_{Omax}	–8.0	–5.0	–	dBV
Input Impedance		C In	Z_{in}	–	10	–	kΩ
Attack Time C_{cap} = 0.5 µF, R_{filt} = 40 k	C In	Tx Out	t_a	–	3.0	–	mS
Release Time C_{cap} = 0.5 µF, R_{filt} = 40 k	C In	Tx Out	t_r	–	13.5	–	mS
Expander to Compressor Crosstalk (V_{in} = –20 dBV, PA no load, VC_{in} = AC Gnd)	E In	Tx Out	C_T	–	–60	–40	dB
Tx Muting (V_{in} = –10 dBV)	MCI	Tx Out	M_c	–	–88	–60	dB
ALC Output Level (When Enabled) V_{in} = –10 dBV V_{in} = –2.5 dBV	MCI	Tx Out	ALC_{out}	 –15 –13	 –13 –11	 –8.0 –6.0	dBV
ALC Slope (When Enabled) V_{in} = –10 dBV V_{in} = –2.5 dBV	MCI	Tx Out	Slope	0.1	0.25	0.4	dB/dB
ALC Input Dynamic Range	C In	Tx Out	DR	–	–16 to –2.5	–	dBV
Limiter Output Level (When Enabled, V_{in} = –2.5 dBV)	Lim In	Tx Out	V_{lim}	–10	–7.0	–	dBV
Tx High Frequency Corner (V_{in} = –10 dBV, Unity Gain) SCF Counter = 31_d	Lim In	Tx Out	Tx f_{ch}	3.45	3.65	3.85	kHz
Low Pass Filter Passband Ripple (V_{in} = –10 dBV)	Lim In	Tx Out	Ripple	–	0.4	1.0	dB
MCU Clock or SCF Spurs (V_{in} = –10 dBv, relative to SCF or MCU Fundamental)	Lim In	Tx Out	–	–	–25	–	dBc
Maximum Compressor Gain (V_{in} = –70 dBV) R6/8 = 0 R6/8 = 1	MCI	Tx Out	AV_{max}	 – –	 21 12	 – –	dB
Tx Gain Adjust Range	Lim In	Tx Out	Tx Range	–	–9.0 to 10	–	dB
Tx Gain Adjust Steps	Lim In	Tx Out	Tx N	–	20	–	
DATA AMP COMPARATOR (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or Receive Mode)							
Hysteresis	DS In	DS Out	Hys	20	42	60	mV
Threshold Voltage	DS In	DS Out	V_T	–	V_{CC} – 0.7	–	V
Input Impedance		DS In	Z_{in}	200	250	280	kΩ
Output Impedance		DS Out	Z_{out}	–	100	–	kΩ
Output High Voltage (V_{in} = V_{CC} – 1.0 V, I_{oh} = 0 mA)	DS In	DS Out	V_{oh}	V_{CC} Audio – 0.1	V_{CC} Audio	–	V
Output Low Voltage (V_{in} = V_{CC} – 0.4 V, I_{ol} = 0 mA)	DS In	DS Out	V_{ol}	–	0.1	0.4	V
Maximum Frequency	DS In	DS Out	F_{max}	–	10	–	kHz

NOTES: 1. Values specified are pure numbers to the base 10.
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ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode, Rx Gain = 01111, Vol Adj = 0111, f_{in} = 1.0 kHz, unless otherwise noted.)

Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
RSSI/LOW BATTERY A/D (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or Receive Mode)							
RSSI Voltage Range	RSSI In	SPI	RSSI Range				V
Minimum (R5/17–12 = 0)				–	0	–	
Interim (R5/17–12 = 100000)				.744	–	.792	
Maximum (R5/17–12 = 1)				–	1.6	–	
Low Battery Detect Operating Range	V_{CC} Audio	SPI	LOWB Range				V
Minimum				–	2.7	–	
Interim (R5/23–18 = 101111)				2.7	–	3.1	
Maximum (R5/23–18 = 1)				–	3.75	–	
Differential Non–linearity	RSSI In/ V_{CC} Audio	SPI	A/D DNL	–1.0	±0.5	1.0	LSB
Resolution	RSSI In/ V_{CC} Audio	SPI	Resolution	–	6	–	Bits
Input Current		RSSI In	I_{in}	–80	20	80	nA
REFERENCE FREQUENCY (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode)							
Input Current High (V_{in} = V_{CC})		$F_{ref\ in}$	I_{ih}	2.0	5.0	15	µA
Input Current Low (V_{in} = 0 V)		$F_{ref\ in}$	I_{il}	–15	–5.0	–2.0	µA
Minimum Input Voltage F_{ref} In	$F_{ref\ in}$	$F_{ref\ out}$	V_{in}	300	–	–	mVpp
Input Impedance		$F_{ref\ in}$	Z_{in}	–	2.9 pF||11.6 kΩ	–	
Output Impedance		$F_{ref\ out}$	Z_{out}	–	2.5 pF||4.5 kΩ	–	
MICROPROCESSOR INTERFACE (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or Receive Mode)							
Input Low Voltage	Data/EN /CLK		V_{il}	0	–	0.3	V
Input High Voltage	Data/EN /CLK		V_{ih}	Tx PLL V_{CC} – 0.3	–	Tx PLL V_{CC}	V
Input Current Low (V_{in} = 0.3 V, Standby Mode) Data, EN, CLK		Data, EN, CLK	I_{il}	–5.0	0.4	–	µA
Input Current High (V_{in} = 3.3 V, Standby Mode) Data, EN, CLK		Data, EN, CLK	I_{ih}	–	1.6	5.0	µA
Hysteresis Voltage Data, EN, CLK		Data, EN, CLK	V_{hys}	–	1.0	–	V
Maximum Clock Frequency	CLK		F_{max}	2.0	–	–	MHz
Input Capacitance Data, EN, CLK		Data, CLK, EN	C_{in}	–	8.0	–	pF
EN to CLK Setup Time		EN, CLK	t_{suEC}	–	200	–	nS
Data to CLK Setup Time		Data, CLK	t_{suDC}	–	100	–	nS
Hold Time		Data, CLK	t_h	–	90	–	nS
Recovery Time		EN, CLK	t_{rec}	–	90	–	nS
Input Pulse Width		EN, CLK	t_w	–	100	–	nS
MCU Interface Power–Up Delay			t_{puMCU}	–	100	–	µS
Output High Voltage (I_{oh} = 0 mA)		MCU Clk Out	V_{oh}	Tx PLL V_{CC} – 0.3	3.5	–	V

NOTES: 1. Values specified are pure numbers to the base 10.
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ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode, Rx Gain = 01111, Vol Adj = 0111, f_{in} = 1.0 kHz, unless otherwise noted.)

Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
MICROPROCESSOR INTERFACE (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or Receive Mode)							
Output Low Voltage (I_{ol} = 0 mA)		MCU Clk Out	V_{ol}	–	0.1	0.3	V
Output High Voltage (I_{oh} = 0 mA)		Data	V_{oh}	Tx PLL V_{CC} – 0.3	3.5	–	V
Output Low Voltage (I_{ol} = 0 mA)		Data	V_{ol}	–	0.1	0.3	V
Rx/Tx PLL CHARACTERISTICS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or Receive Mode)							
Output Source Current (V_{PD} = 0.5 V or V_{CC} – 0.5 V) ±100 µA mode ±400 µA mode		 Rx PD & Tx PD	I_{oh}	 –130 –520	 –100 –400	 –70 –280	µA
Output Sink Current (V_{PD} = 0.5 V or V_{CC} – 0.5 V) ±100 µA mode ±400 µA mode		 Rx PD & Tx PD	I_{ol}	 70 280	 100 400	 130 520	µA
Current Match, ±100 µA mode or ±400 µA mode, V_{PD} = V_{CC} / 2 (i.e., 100 x (ABS (I_{oh} / I_{ol})))		Rx PD Tx PD	Match	80	100	125	%
Output Off Current (V_{PD} = V_{CC} /2),±100 µA mode or ±400 µA mode		Rx PD Tx PD	I_{oz}	–80	5.0	80	nA
Input Current Low (V_{in} = 0 V)		FRx FTx	I_{il}	–10	–7.5	–	µA
Input Current High (V_{in} = V_{CC})		FRx FTx	I_{ih}	–	10	14	µA
Input Bias Voltage		FRx FTx	V_{bias}	–	1.5	–	V
Output Voltage High (I_{oh} = 0 mA, Voltage Mode)		FRxMC	V_{oh}	–	Rx PLL V_{CC} – 0.1	–	V
Output Voltage High (I_{oh} = 0 mA, Voltage Mode)		FTxMC	V_{oh}	–	Tx PLL V_{CC} – 0.1	–	V
Output Voltage Low (I_{ol} = 0 mA, Voltage Mode)		FRxMC FTxMC	V_{ol}	–	0.1	–	V
Output Current High (V_{oh} = 0.8 V, Current Mode)		FRxMC FTxMC	I_{oh}	–130	–100	–70	µA
Output Current Low (V_{ol} = 0.8 V, Current Mode)		FRxMC FTxMC	I_{ol}	70	100	130	µA
Maximum Input Frequency		FRx FTx	F_{max}	20	–	–	MHz
Input Voltage Swing		FRx FTx	V_{in}	200	–	1200	mVpp
Modulus Control Prop Delay	FRx FTx	FRxMC FTxMC	–	–	20	–	nS
LO2 PLL CHARACTERISTICS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode)							
Output Source Current (V_{PD} = 0.5 V or V_{CC} – 0.5 V) ±100 µA mode ±400 µA mode		LO2PD	I_{oh}	 –130 –520	 –100 –400	 –70 –280	µA
Output Sink Current (V_{PD} = 0.5 V or V_{CC} – 0.5 V) ±100 µA mode ±400 µA mode		LO2PD	I_{ol}	 70 280	 100 400	 130 520	µA
Current Match, ±100 µA mode or ±400 µA mode, V_{PD} = V_{CC} / 2 (i.e., 100 x (ABS (I_{oh} / I_{ol})))		LO2PD	Match	80	100	125	%

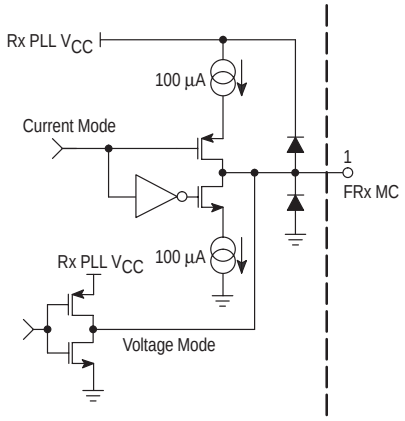
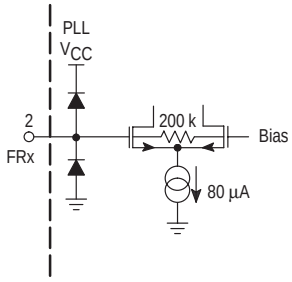
NOTES: 1. Values specified are pure numbers to the base 10.
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ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode, Rx Gain = 01111, Vol Adj = 0111, f_{in} = 1.0 kHz, unless otherwise noted.)

Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
LO2 PLL CHARACTERISTICS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode)							
Output Off Current (V_{PD} = V_{CC} /2)		LO2PD	I_{oz}	–80	5.0	80	nA
Input Current Low (V_{in} = 0.5 V)		LO2Ctl	I_{il}	–1.0	–0.02	–	µA
Input Current High (V_{in} = V_{CC} – 0.5 V)		LO2Ctl	I_{ih}	–	0.02	1.0	µA
Input Voltage Range		LO2Ctl	V_{range}	0.4	–	V_{CC}	V
Maximum 2nd LO Frequency				65	80	–	MHz
LO2 Out Drive (25 Ω load)			V_{out}	112	180	245	mVpp
COUNTERS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode)							
12–Bit Reference Counter Range [Note 1]				–	3 to 4095	–	
13–Bit N Counter Range [Note 1]				–	3 to 8191	–	
7–Bit A Counter Range [Note 1] 64/65 Modulus Prescaler 128/129 Modulus Prescaler				 – –	 0 to 63 0 to 127	 – –	
14–Bit LO2 Counter Range [Note 1]				–	12 to 16383	–	
6–Bit Counters (for SCF) [Note 1]				–	3 to 63	–	

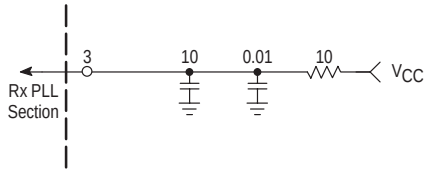
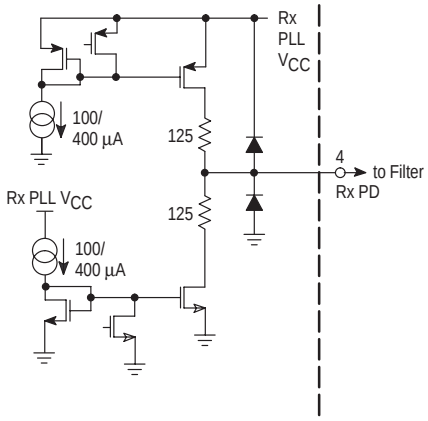
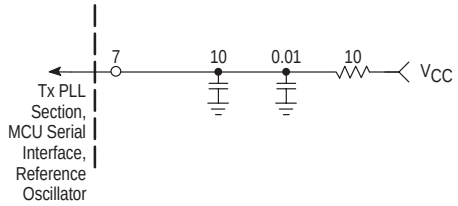
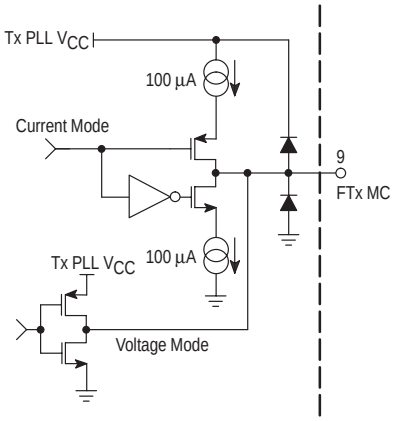
NOTES: 1. Values specified are pure numbers to the base 10.
2. Typical performance parameters indicate the potential of the device under ideal operating conditions.

PIN FUNCTION DESCRIPTION

Pin	Symbol/Type	Description	Description
1	FRx MC (Output)		Modulus Control Output for the Rx PLL section. Can be set to output in current mode or voltage mode, selectable with bit 3/16.
2	FRx (Input)		Receives the signal from the external 64/65 or 128/129 prescaler. DC bias is at 1.3 V.

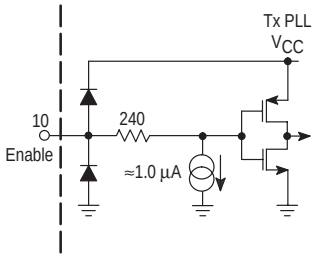
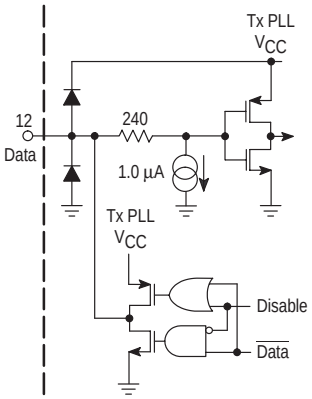
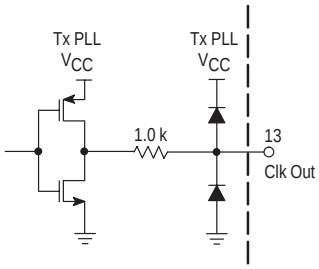
NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
3	Rx PLL V_{CC} (Input)		Supply pin for the Rx PLL section. Allowable range is 2.7 to 5.5 V and must be within 0.5 V of all other V_{CC} pins. Good bypassing is required and isolation with a 10 Ω resistor is recommended.
4	Rx PD (Output)		Rx Phase Detector Output. The output either sources or sinks current, or neither, depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the PLL reference frequency are present. Output current is either ±100 µA or ±400 µA, selectable with bit 2/20.
5	PLL Gnd		Ground pin for the PLL section. A direct connection to a ground plane is strongly recommended.
6	Tx PD (Output)	Same as Pin 4, except powered from Tx PLL V_{CC}.	Tx Phase Detector Output. Description same as for Pin 4, except bit 1/20 controls the current level.
7	Tx PLL V_{CC} (Input)		Supply pin for the Tx PLL section, MCU Serial Interface, MCU Clock Counter, and the Reference Oscillator. Allowable range is 2.7 to 5.5 V and must be within 0.5 V of all other V_{CC} pins. Good bypassing is required and isolation with a 10 Ω resistor is recommended.
8	FTx (Input)	Same as Pin 2.	Receives the signal from the external 64/65 or 128/129 prescaler. DC bias is at 1.5 V.
9	FTx MC (Output)		Modulus Control Output for the Tx PLL section. Can be set to output in a current mode or a voltage mode, selectable with bit 3/16.

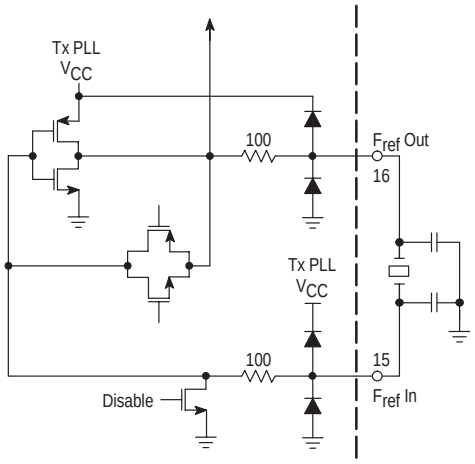
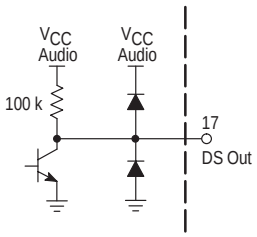
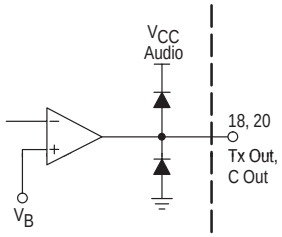
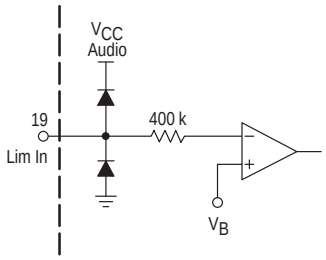
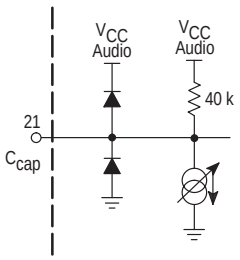
NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
10	EN (Input)		Enable Input for the MCU Interface section. Hysteresis threshold is within 0.5 V of ground and V_{CC}. See text for proper waveform required at this pin.
11	CLK (Input)	Same as Pin 10.	Clock Input for the MCU Interface section. Hysteresis threshold is within 0.5 V of ground and V_{CC}. Data is written or read out on clock's rising edge. Maximum clock rate is 2.0 MHz.
12	Data (I/O)		Data I/O line for the MCU Interface section. Both address and data are provided to/from this pin. Input threshold is within 0.5 V of ground and V_{CC}. Data is written or read out on clock's rising edge.
13	MCU Clk Out (Output)		The microprocessor clock output is derived from the reference oscillator and a programmable divider with divide ratios of 2 to 312.5. It can be used to drive a microprocessor and thereby reduce the number of crystals required in the system design. The driver has an internal resistor in series with the output which can be combined with an external capacitor to form a low–pass filter to reduce radiated noise on the PCB. This output also functions as the output for the counter test modes. 1) For the MC33411A the Clk Out can be disabled via the MCU interface. 2) For the MC33411B this output is always active (on).
14	Gnd Digital		Ground for the Data, MCU Clk Out, and F_{ref} Out digital Outputs. A direct connection to the ground plane is strongly recommended.

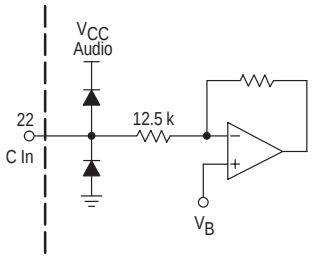
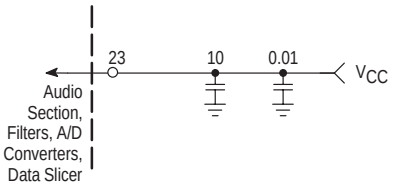
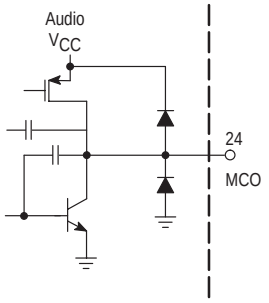
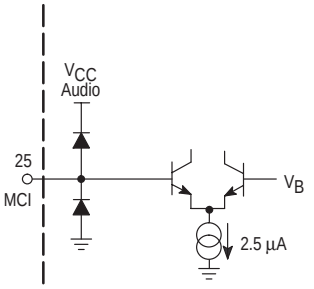
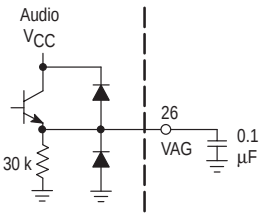
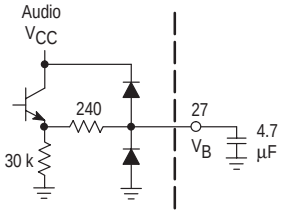
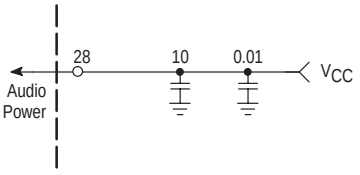
NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
15, 16	F_{ref} In, F_{ref} Out		Reference Frequency Input for various portions of the circuit, including the PLLs, SCF clock, etc. A crystal (4 to 18.25 MHz) may be connected as shown, or an external frequency source may be capacitor coupled to Pin 15. See text for crystal requirements. 1) For the MC33411A the F_{ref} Out can be disabled via the MCU interface. 2) For the MC33411B this output is always active (on).
17	DS Out (Output)		Data Slicer Output (open collector with internal 100 kΩ pull–up resistor).
18	Tx Out (Output)		Tx Out is the Tx path audio output. Internally this pin has a low–pass filter circuitry with –3.0 dB bandwidth of 4.0 kHz. Tx gain and mute are programmable through the MCU interface. This pin is sensitive to load capacitance.
20	C Out (Output)		C Out is the compressor output.
19	Lim In (Input)		Lim In is the limiter input. This pin is internally biased and has an input impedance of 400 kΩ. Lim In must be ac–coupled.
21	C_{cap}		C_{cap} is the compressor rectifier filter capacitor pin. It is recommended that an external filter capacitor to V_{CC} audio be used. A practical capacitor range is 0.1 to 1.0 μF. The recommended value is 0.47 μF.

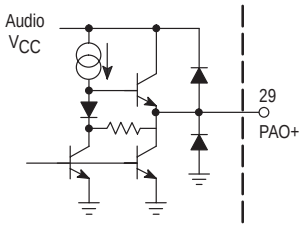
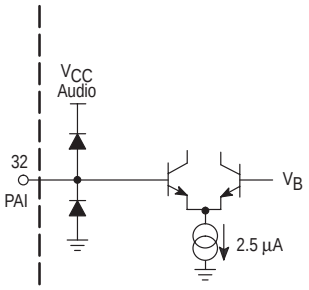
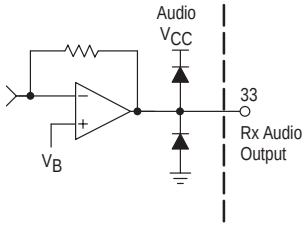
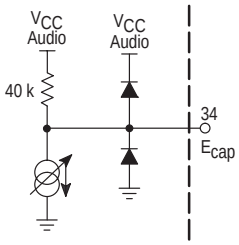
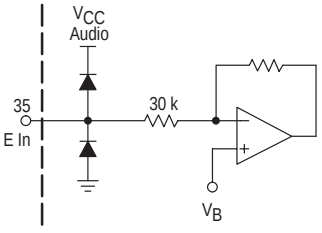
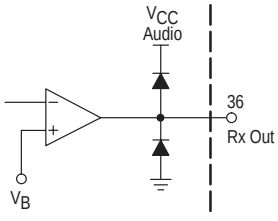
NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
22	C In (Input)		C In is the compressor input. This pin is internally biased and has an input impedance of 12.5 kΩ. C In must be ac–coupled.
23	V_{CC} Audio (Input)		Supply input for the audio section, filters, A/D Converters, and Data Slicer. Allowable range is 2.7 to 5.5 V. Good bypassing is required.
24	MCO (Output)		Output of the Microphone amplifier. Maximum output swing is ≈3.0 V_{pp} for V_{CC} ≥ 3.0 V. Maximum output current is >1.0 mA peak.
25	MCI (Input)		Inverting input of the microphone amplifier. Gain and frequency response are set with external resistors and capacitors from this pin to the audio source and to MCO.
26	VAG (Output)		Analog ground for the audio section filters. VAG is equal to VB and is buffered from VB. Maximum current which can be sourced from this pin is 500 µA.
27	V_B (Output)		An internal 1.5 V reference for several sections. This voltage is adjustable with bits 3/20–17. Maximum source current is 100 µA. PSRR, noise and crosstalk depends on the external capacitor.
28	V_{CC} PA (Input)		Supply pin for the power amplifier outputs. Allowable range is 2.7 to 5.5 V. Good bypassing is required.

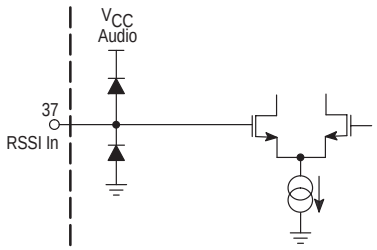
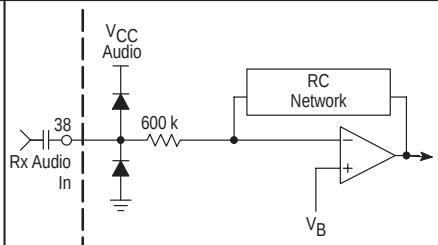
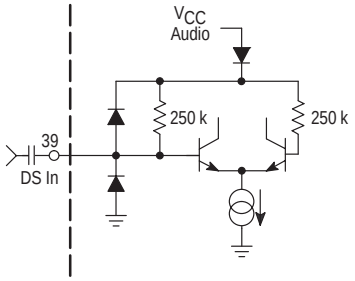
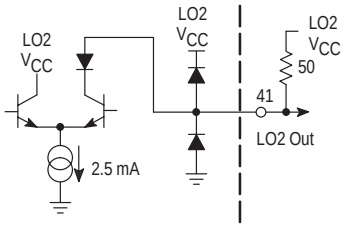
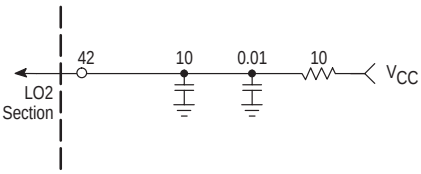
NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
29	PAO+ (Output)		Output of the second power amplifier. This amplifier is set for unity inverting gain and is driven by PAO–. Maximum swing is 2.9 V_{pp} and maximum output current is >5.0 mA peak. DC level is ≈1.5 V.
30	PAO– (Output)	Same as Pin 29.	Output of the first power amplifier. Its gain is set with external resistors and capacitors from this pin to PAI. Output capability is the same as Pin 28.
31	Gnd PA		Ground pin for the power amplifier outputs. A direct connection to a ground plane is strongly recommended.
32	PAI (Input)		Inverting input of the power amplifier. Gain and frequency response are set with external resistors and capacitors from this pin to the audio source and to PAO–.
33	E Out (Output)		Expander output. This output is sensitive to load capacitance. Maximum output signal level is ≈2.5 V_{pp}. Maximum output current is >1.0 mA.
34	E_{cap}		E_{cap} is the expander rectifier filter capacitor pin. Connect an external filter capacitor between V_{CC} audio and E_{cap}. The recommended capacitance range is 0.1 to 1.0 µF. The suggested value is 0.47 µF.
35	E In (Input)		The expander input pin is internally biased and has input impedance of 30 kΩ.
36	Rx Out (Output)		Rx Out is the Rx audio output. An internal low–pass filter has a –3.0 dB bandwidth of 4.0 kHz.

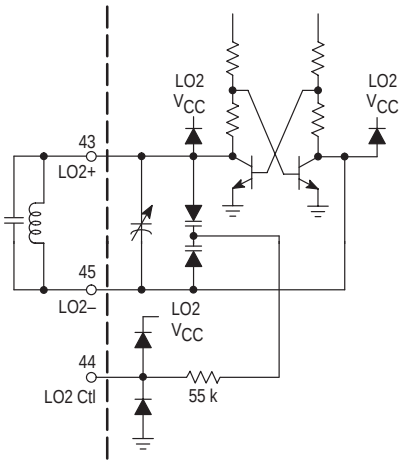
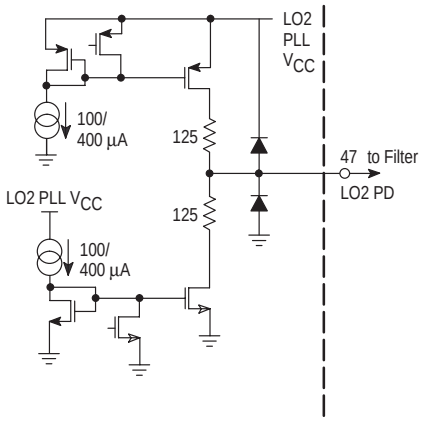
NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
37	RSSI In (Input)		Voltage input to RSSI A/D converter. Full scale is 0 to 1.6 V.
38	Rx Audio In (Input)		Input to the Rx Audio Path. Input impedance is 600 kΩ. Input signal must be capacitor coupled
39	DS In (Input)		Input for the digital data from the RF Receiver section. Input impedance is 250 kΩ. Hysteresis is internally provided. Input signal level must be between 50 and 700 mVpp.
40	Gnd Audio		Ground pin for the audio section. A direct connection to a ground plan is strongly recommended.
41	LO2 Out (Output)		Buffered output of the 2nd LO. This high frequency output is a current, requiring an external pullup resistor.
42	LO2 VCC (Input)		Supply pin for the LO2 section. Allowable range is 2.7 to 5.5 V and must be within 0.5 V of all other VCC pins. Good bypassing is required and isolation with a 10 Ω resistor is recommended.

NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
43, 45	LO2+, LO2–		The 2nd LO. External tank components are required. The internal capacitance across the pins is adjustable from 0 to 7.6 pF for fine tuning performance with bits 7/20–18.
44	LO2 Ctl (Input)		LO2 Control is the dc control input for this VCO. Typically it is the output of the low–pass filter fed from the phase detector output.
46	LO2 Gnd		Ground pin for the LO2 section. A direct connection to a ground plane is strongly recommended.
47	LO2PD (Output)		LO2 Phase Detector Output. The output either sources or sinks current, or neither, depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the PLL reference frequency are present. Output current is either ±100 µA or ±400 µA, selectable with bit 3/14.
48	LO2 Gnd		Ground pin for the LO2 section. A direct connection to a ground plane is strongly recommended.

NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

FUNCTIONAL DESCRIPTION

The following text, graphics, tables and schematics are provided to the user as a source of valuable technical information about the MC33411. This information originates from thorough evaluation of the device performance. This data was obtained by using units from typical wafer lots. It is important to note that the forgoing data and information was from a limited number of units. By no means is the user to assume that the data following is a guaranteed parametric. Only the minimum and maximum limits identified in the electrical characteristics tables found earlier in the spec are guaranteed.

Note: In the following descriptions, control bits in the MCU Serial Interface for the various functions will be identified by register number and bit number. For example, bit 3/19 indicates bit 19 of register 3. Bits 5/14–11 indicates register 5, bits 14 through 11. Please refer to Figure 1.

General Circuit Description

The MC33411A/B is a low power baseband IC designed to interface with the MC13145 UHF Wideband Receiver and MC13146 Transmitter for applications up to 2.0 GHz. The devices are primarily designated to be used for 900 MHz ISM band in a CT–900, low power, dual conversion cordless phone, but other applications such as data links with analog processing could be developed. This device contains complete baseband transmit and receive processing sections, a transmit and receive PLL section, a programmable PLL second local oscillator usable to 80 MHz, RSSI and low battery detect circuitry and serial interface for a microprocessor.

”A” versions of the device have the ability to disable either the reference oscillator or MCU clock outputs. This feature is useful for systems where the MCU has an internal clock, allowing the user to place the MC33411 into Inactive (lowest power consumption) mode. The ”A” version is also useful for systems where the MCU has a dedicated clock source, allowing for lower power consumption from the MC33411 by disabling the MCU clock output.

”B” versions of the device are intended for systems where the MCU clock will always be driven from the MC33411. These bits are purposefully ”hard–wired” to the enable state to ensure proper operation of the reference oscillator and MCU clock output even during battery discharge/recharge cycles.

All internal registers are completely static – no refreshing is required under normal operation conditions.

DC Current

Figures 2 through 5 are the current consumption for Inactive (MC33411 ”A” version only), Standby, Receive, and Active modes versus supply voltages. Figures 6 and 7 show the typical behavior of current consumption in relation to temperature.

Figure 8 illustrates the effect of the MCU clock output frequency to supply current during Active mode.

Figure 2. Supply Current versus Supply Voltage (Inactive Mode)

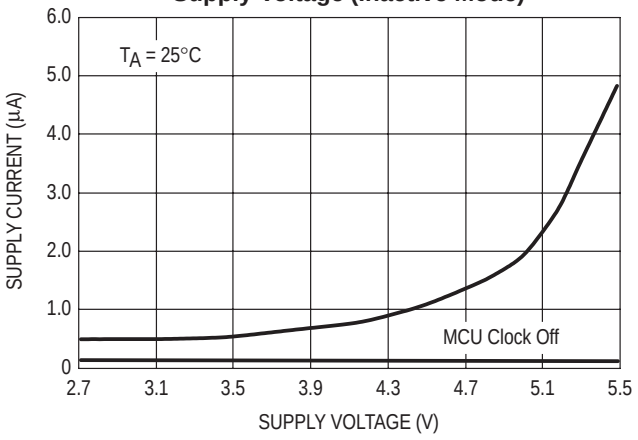


Figure 3. Supply Current versus Supply Voltage (Standby Mode)

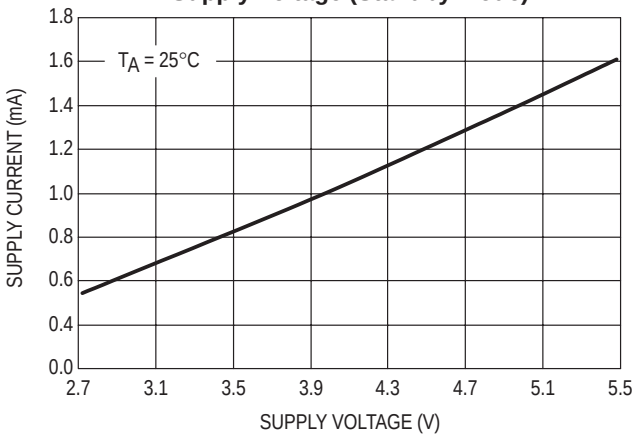


Figure 4. Supply Current versus Supply Voltage (Receive Mode)

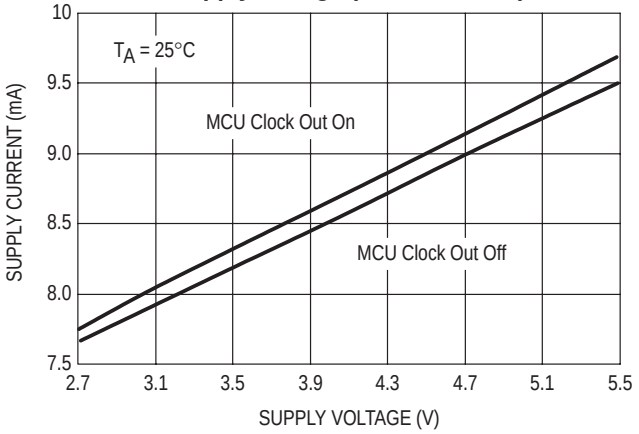


Figure 5. Supply Current versus Supply Voltage (Active Mode)

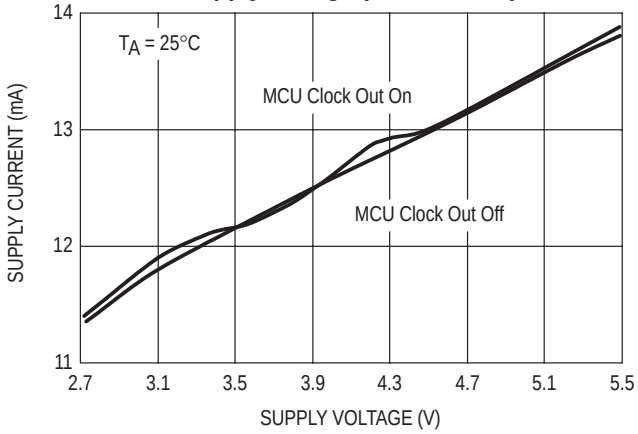


Figure 6. Supply Current versus Temperature Normalized to 25°C (Standby Mode)

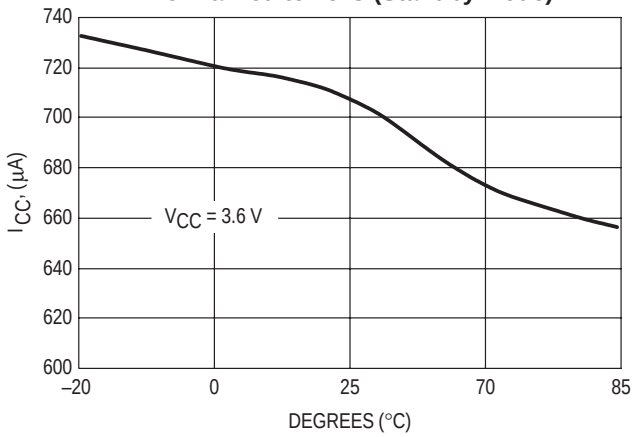


Figure 7. Supply Current versus Temperature Normalized to 25°C (Receive & Active Mode)

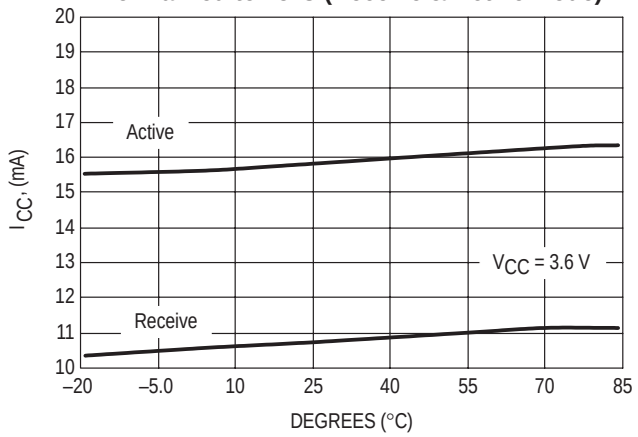


Figure 8. Supply Current versus MCU Clock Output Frequency (Active Mode)

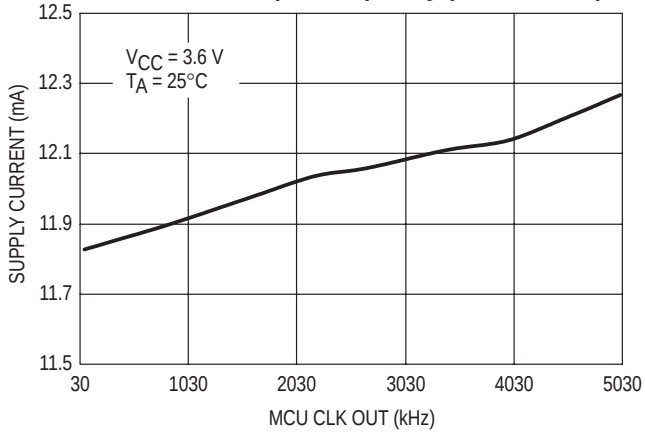


Table 1. Tx Gain Adjust Programming (Register 7)

Gain Control Bit #9	Gain Control Bit #8	Gain Control Bit #7	Gain Control Bit #6	Gain Control Bit #5	Gain Ctl #	Gain/Attenuation Amount
					<6	–9.0 dB
0	0	1	1	0	6	–9.0 dB
0	0	1	1	1	7	–8.0 dB
0	1	0	0	0	8	–7.0 dB
0	1	0	0	1	9	–6.0 dB
0	1	0	1	0	10	–5.0 dB
0	1	0	1	1	11	–4.0 dB
0	1	1	0	0	12	–3.0 dB
0	1	1	0	1	13	–2.0 dB
0	1	1	1	0	14	–1.0 dB
0	1	1	1	1	15	0 dB
1	0	0	0	0	16	1.0 dB
1	0	0	0	1	17	2.0 dB
1	0	0	1	0	18	3.0 dB
1	0	0	1	1	19	4.0 dB
1	0	1	0	0	20	5.0 dB
1	0	1	0	1	21	6.0 dB
1	0	1	1	0	22	7.0 dB
1	0	1	1	1	23	8.0 dB
1	1	0	0	0	24	9.0 dB
1	1	0	0	1	25	10 dB
–	–	–	–	–	>25	10 dB

Transmit Speech Processing System

This portion of the audio path goes from ”Tx Audio” to ”Tx Out”. The gain of the microphone amplifier is set with external resistors to receive the audio from the microphone hybrid or any other audio source. The MCO output has rail–to–rail capability. The ”Tx Audio” pin will be ac–coupled. The audio transmit signal path includes automatic level control (ALC) (also referred to as the Compressor), Tx mute, limiter, filters, and Tx gain adjust. The ALC provides ”soft” limiting to the output signal swing as the input voltage slowly increases. With this technique the gain is slightly lowered to help reduce distortion of the audio signal. The limiter section provides hard limiting due to rapidly changing singal levels, or transients. The ALC, TX mute, and limiter functions can be enabled or disabled vis the MCU serial interface. The Tx gain adjust can also be remotely controlled to set different desired signal levels.

The adjustable gain stage provides 20 levels of gain in 1.0 dB increments. It is controlled with bits 7/9–5 as shown in Table 1. The effect of the gain setting under various ALC/Limiter On/Off settings is shown in Figure 9.

The Low–Pass Filter before the gain stage is a switched capacitor filter with a corner frequency at 3.7 kHz. This frequency is dependent upon the SCF clock, nominaly set to 165 kHz and is directly proportional to the SCF clock. The filter response for inband, ripple, wideband, as well as phase and group delay, are shown in Figures 10 through 14.

The mute switch at Pin 18 will mute a minimum of 60 dB. Bit 6/2 controls the mute. The limiter can be disabled by programming a logic 1 into 6/5.

The compressor with ALC transfer characteristic is shown in Figure 15. The ALC gain is controlled by bits 6/11–12. If both bits are programmed to a logic 0, the ALC gain is set to 5.0 dB. If bit 6/11 is set to a logic 1, the ALC gain will be set to 10 dB, whereas if bit 6/12 is set to a logic 1 the ALC gain will be 25 dB. The ALC function may be disabled by programming a logic 1 into bit 6/6.

The compressor low maximum gain can be set with bit 6/8. Programming this bit to a logic 0 sets the maximum gain to 23 dB. A lower maximum gain, nominally 13.5 dB, is achieved by programming the bit to a logic 1. The entire compressor can be bypassed (i.e., 0 dB) by programming bit 6/4 to a logic 1.

Figures 16 through 22 describe the characteristics of the compressor, ALC, and limiter.

Figure 9. Tx Audio Output Voltage versus Gain Control Setting

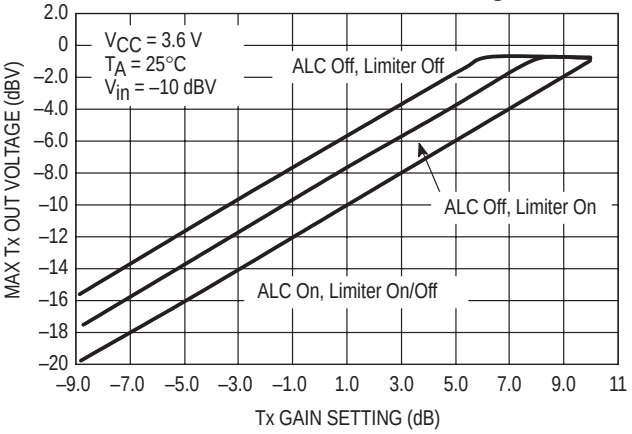


Figure 10. Lim In to Tx Out Gain versus Frequency (Inband)

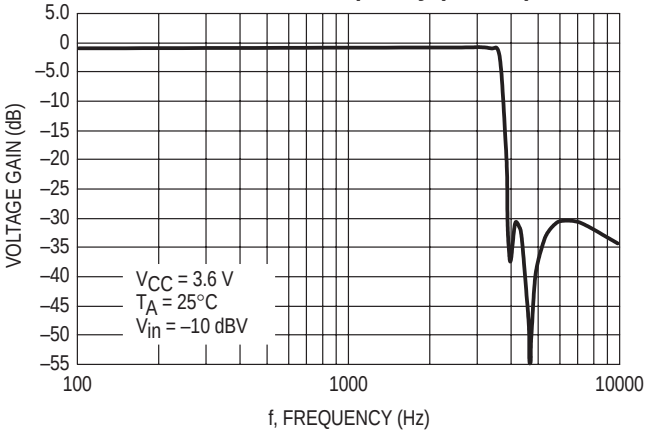


Figure 11. Lim In to Tx Out Gain versus Frequency (Ripple)

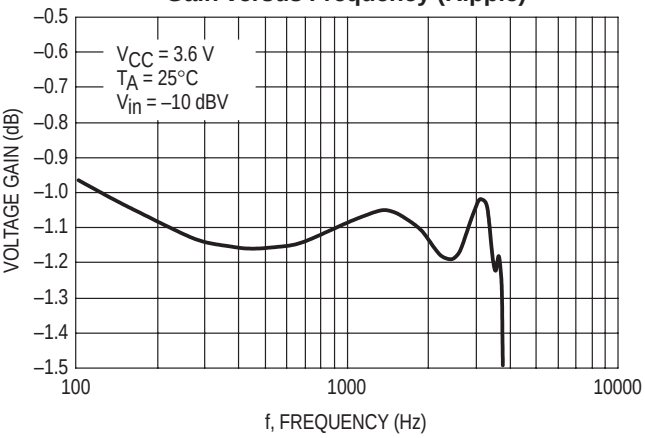


Figure 12. Lim In to Tx Out Gain versus Frequency (Wideband)

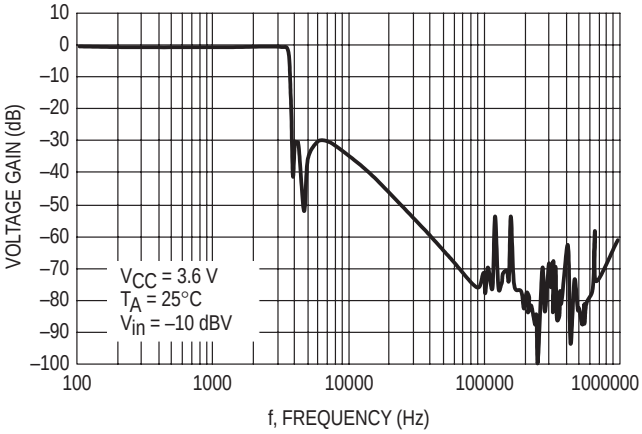


Figure 13. Lim In to Tx Out Phase versus Frequency

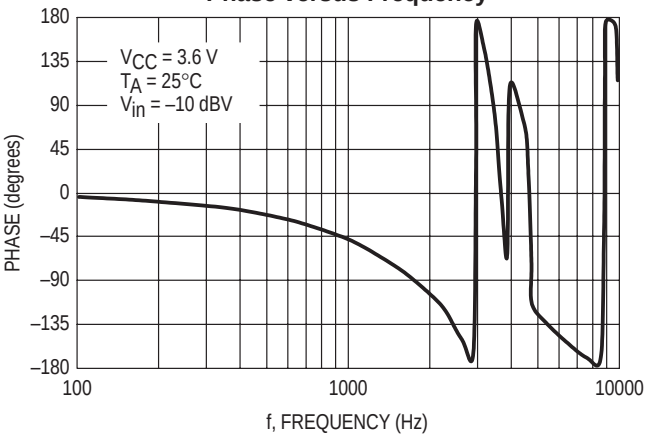


Figure 14. Lim In to Tx Out Group Delay versus Frequency

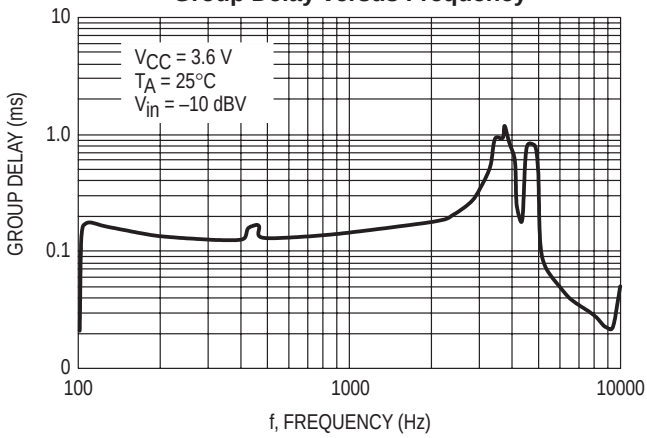


Figure 15. Compressor Characteristic with Programmable Compressor Maximum Gain

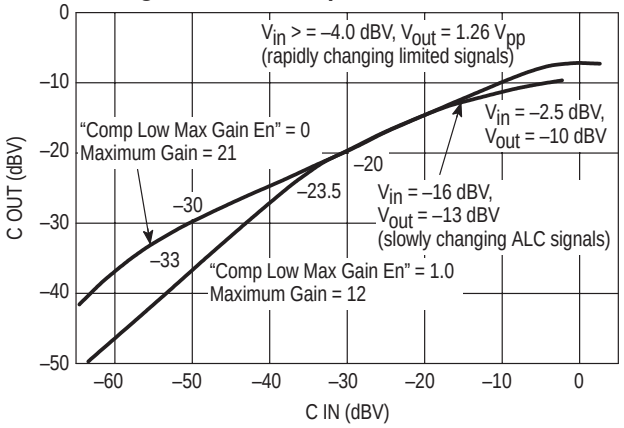


Figure 16. Tx Audio Compressor Response (Distortion & Amplitude, ALC off, Lim off)

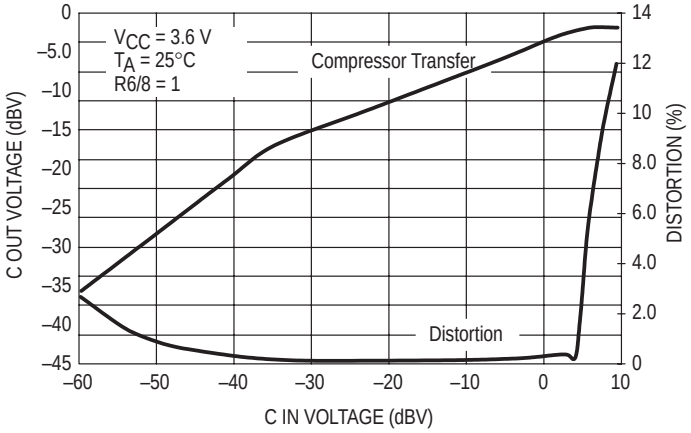


Figure 17. Tx Audio Compressor Response (Distortion & Amplitude, ALC off, Lim off)

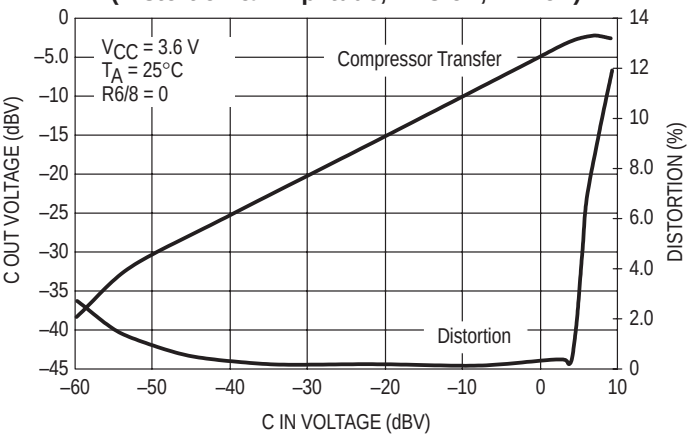


Figure 18. Tx Output Audio Response (Lim & ALC off)

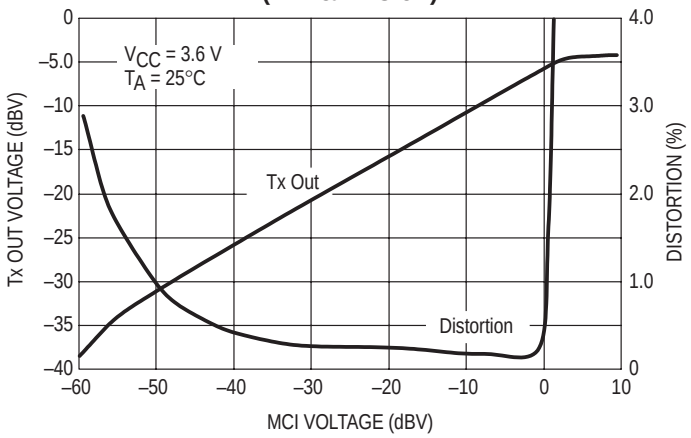


Figure 19. Tx Output Audio Response (Lim on, ALC off)

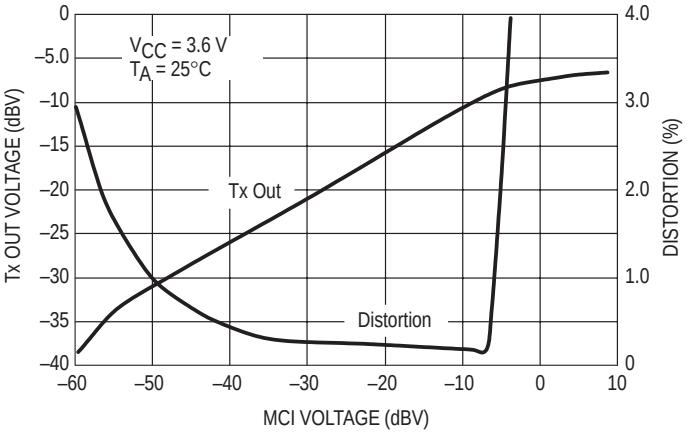


Figure 20. Tx Output Audio Response (Lim off, ALC on)

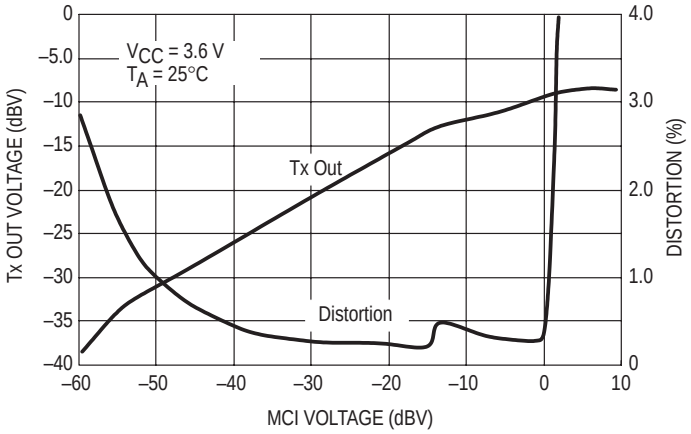


Figure 21. Tx Output Audio Response (Lim off, R6/11 = 1)

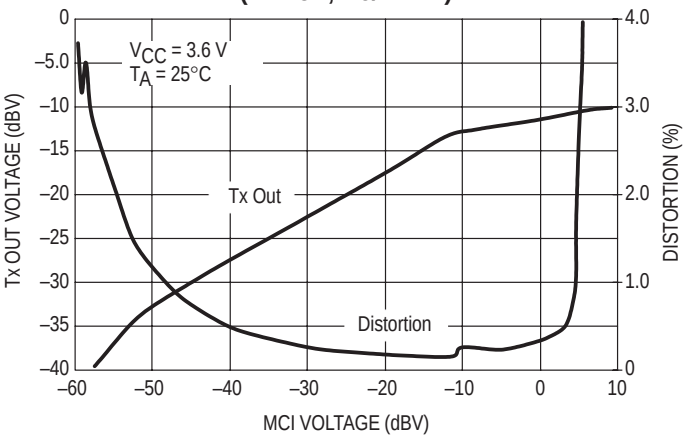
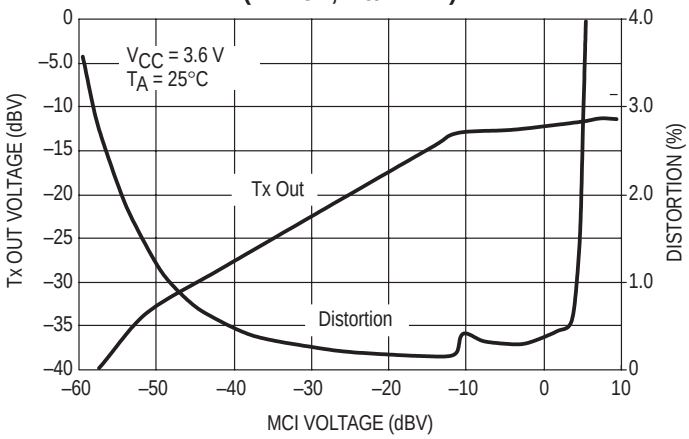


Figure 22. Tx Output Audio Response (Lim off, R6/12 = 1)



Data Slicer

The data slicer will receive the low level digital signal from the RF receiver section at Pin 39. The input signal to the data slicer must be >200 mVpp. Hysteresis of 40 mV is internally provided. The output of the data slicer will be same waveform, but with an amplitude of 0 to V_{CC}, and can be observed at Pin 17 if bits 5/9–8 are set to 00. The output can be inverted by setting bit 5/9 = 1. The data slicer can be disabled by setting bit 5/8 = 1.

Receive Audio Path

The Receive Audio Path (Pins 38, 36–33) consists of an anti–aliasing filter, a low–pass filter, side tone attenuator, gain adjust stage, a mute switch, expander and volume control.

The switched capacitor low–pass filter is an 8 pole filter, with a corner frequency at 3.8 kHz. This is designed to provide bandwidth limiting in the audio range.

The gain stage provides 20 dB of gain adjustment in 1.0 dB steps, measured from Pin 38 to 36. Bits 7/4–0 are used to set the gain according to Table 3. The mute switch, controlled by bit 6/1, will mute a minimum of 60 dB.

When the compressor output is within 3.0 dB of the expander input level, the Rx output (Pin 36) can be attenuated (referenced to the expander output) by bits 6/10–9. For 6/10–9 = 00, the attenuation is 0 dB. For the other combinations, 6/10–9 = 01, attenuation = 3.0 dB; 6/10–9 = 10, attenuation = 6.0 dB; and 6/10–9 = 11, attenuation = 10.4 dB (See Table 2).

The expander can be bypassed by setting bit 6/3 = 1.

Table 3 shows the various gain control settings which can be accessed in Register 7. Table 5 is the volume control settings, also located in Register 7.

Figures 23 through 31 illustrate the various characteristics of the reveive audio path.

Table 2. Side Tone Attenuate Programming

Side Tone Attenuate Bit #1	Side Tone Attenuate Bit #0	Select #	Side Tone Attenuate Amount at Expander Input	Side Tone Attenuate Amount at Expander Output
0	0	0	0 dB	0 dB
0	1	1	1.5 dB	3.0 dB
1	0	2	3.0 dB	6.0 dB
1	1	3	5.2 dB	10.4 dB

Table 3. Rx Gain Adjust Programming (Register 7)

Gain Control Bit #4	Gain Control Bit #3	Gain Control Bit #2	Gain Control Bit #1	Gain Control Bit #0	Gain Ctl #	Gain/Attenuation Amount
–	–	–	–	–	<6	–9.0 dB
0	0	1	1	0	6	–9.0 dB
0	0	1	1	1	7	–8.0 dB
0	1	0	0	0	8	–7.0 dB
0	1	0	0	1	9	–6.0 dB
0	1	0	1	0	10	–5.0 dB
0	1	0	1	1	11	–4.0 dB
0	1	1	0	0	12	–3.0 dB
0	1	1	0	1	13	–2.0 dB

Table 3. Rx Gain Adjust Programming (Register 7) (continued)

Gain Control Bit #4	Gain Control Bit #3	Gain Control Bit #2	Gain Control Bit #1	Gain Control Bit #0	Gain Ctl #	Gain/Attenuation Amount
0	1	1	1	0	14	–1.0 dB
0	1	1	1	1	15	0 dB
1	0	0	0	0	16	1.0 dB
1	0	0	0	1	17	2.0 dB
1	0	0	1	0	18	3.0 dB
1	0	0	1	1	19	4.0 dB
1	0	1	0	0	20	5.0 dB
1	0	1	0	1	21	6.0 dB
1	0	1	1	0	22	7.0 dB
1	0	1	1	1	23	8.0 dB
1	1	0	0	0	24	9.0 dB
1	1	0	0	1	25	10 dB
–	–	–	–	–	>25	10 dB

Table 4. Volume Control Programming

Volume Control Bit #13	Volume Control Bit #12	Volume Control Bit #11	Volume Control Bit #10	Volume Ctl #	Gain/Attenuation Amount
0	0	0	0	0	–14 dB
0	0	0	1	1	–12 dB
0	0	1	0	2	–10 dB
0	0	1	1	3	–8.0 dB
0	1	0	0	4	–6.0 dB
0	1	0	1	5	–4.0 dB
0	1	1	0	6	–2.0 dB
0	1	1	1	7	0 dB
1	0	0	0	8	2.0 dB
1	0	0	1	9	4.0 dB
1	0	1	0	10	6.0 dB
1	0	1	1	11	8.0 dB
1	1	0	0	12	10 dB
1	1	0	1	13	12 dB
1	1	1	0	14	14 dB
1	1	1	1	15	16 dB

Figure 23. Rx Out Maximum Output Voltage versus Gain Control Setting

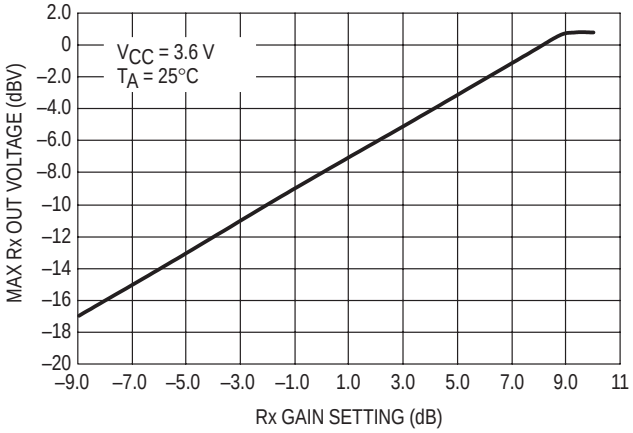


Figure 24. E Out Maximum Output Voltage versus Volume Control Setting

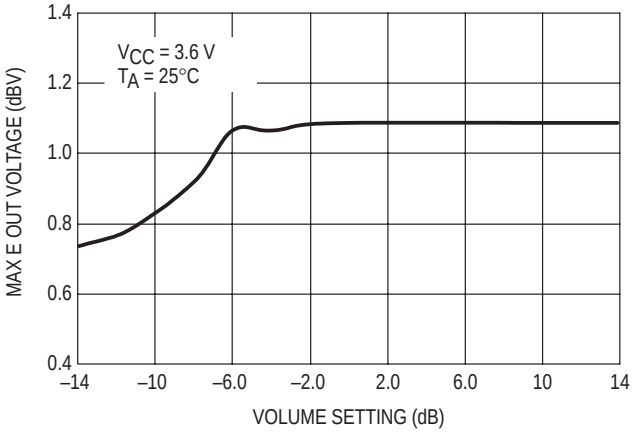


Figure 25. Rx Audio In to Rx Out Gain versus Frequency (Inband)

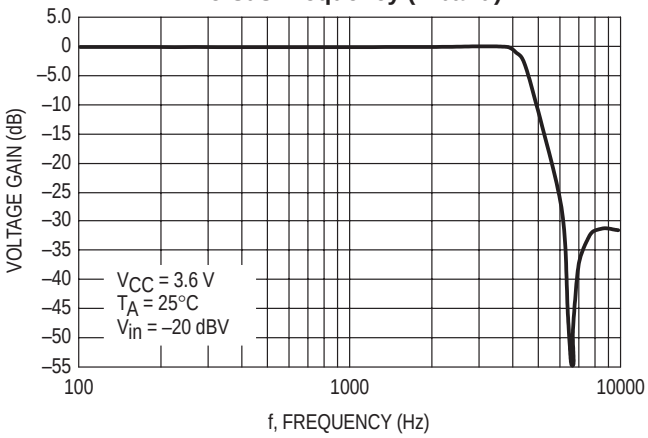


Figure 26. Rx Audio In to Rx Out Gain versus Frequency (Ripple)

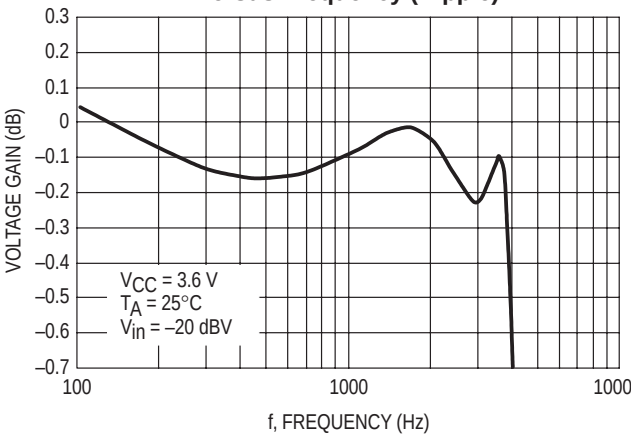


Figure 27. Rx Audio In to Rx Out Gain versus Frequency (Wideband)

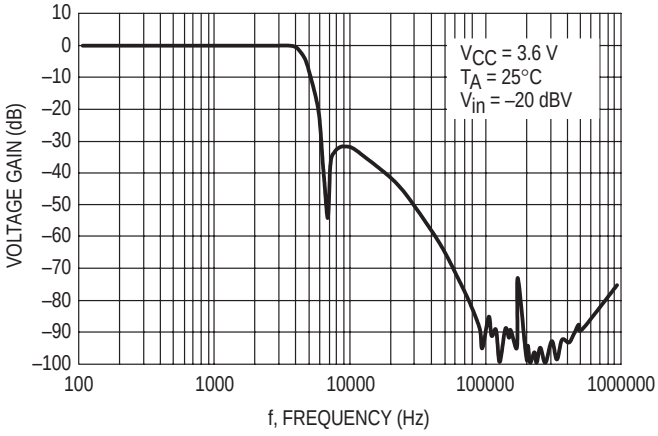


Figure 28. Rx Audio In to Rx Out Phase versus Frequency

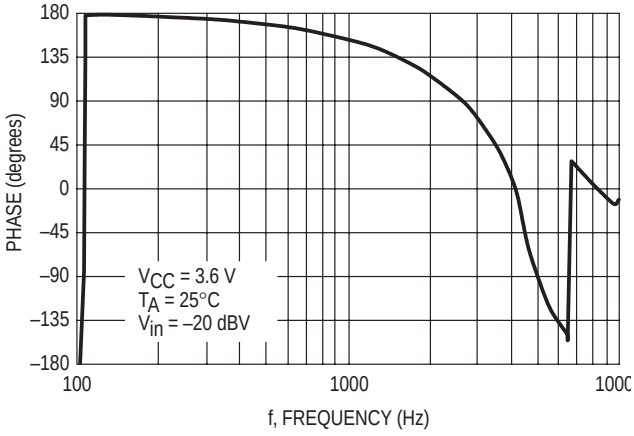


Figure 29. Rx Audio In to Rx Out Group Delay versus Frequency

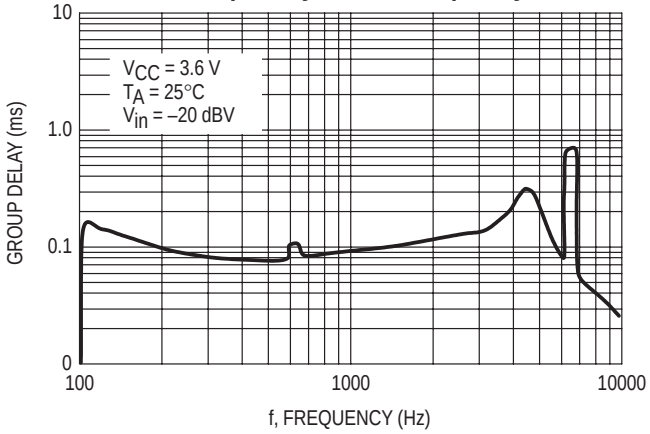


Figure 30. AALPF Response Gain versus Frequency

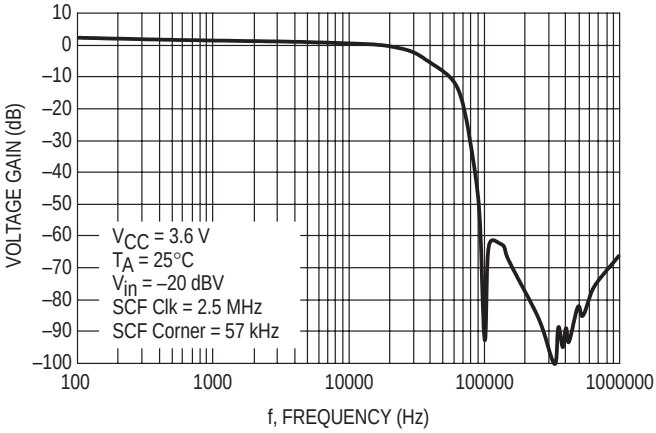
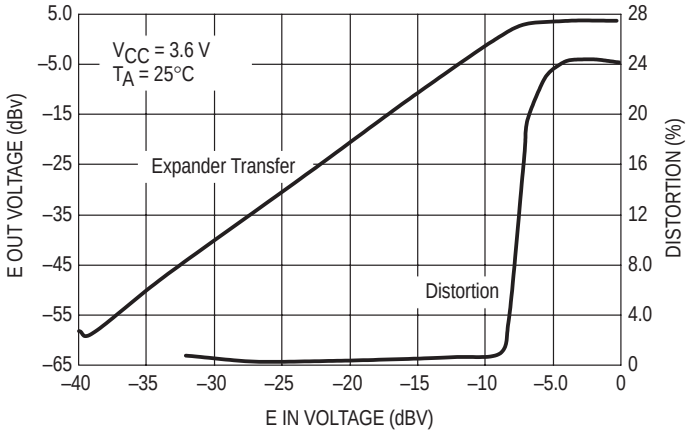


Figure 31. E In to E Out Transfer Curve



Power Amplifiers

The power amplifiers (Pins 29, 30, 32) are designed to drive the earpiece in a handset, or the telephone line via a hybrid circuit in the base unit. Each output (PAO+ and PAO–) can source and sink 5.0 mA, and can swing 1.3 V_{pp} each. For high impedance loads, each output can swing 2.7 V_{pp} (5.4 V_{pp} differential). The gain of the amplifiers is set with a feedback resistor from Pin 30 to 32, and an input resistor at Pin 32. The differential gain is 2x the resistor ratio. Capacitors can be used for frequency shaping. The pins' dc level is VB (≅1.5 V).

The Mute switch, controlled with bit 6/0, will provide 60 dB of muting with a 50 kΩ feedback resistor. The amount of muting will depend on the value of the feedback resistor.

Figures 32 and 33 show the power amplifier swing/distortion for V_{CC} = 3.6 V, and Figure 34 illustrates the maximum swing capability for various value of V_{CC}.

Figure 32. Power Amplifier Maximum Output Swing

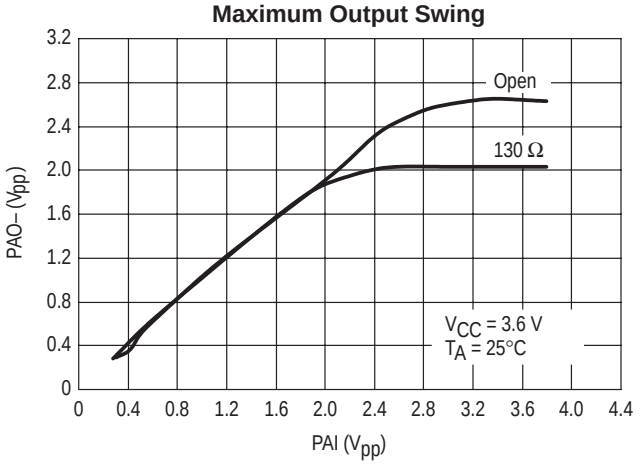


Figure 33. Power Amplifier Distortion

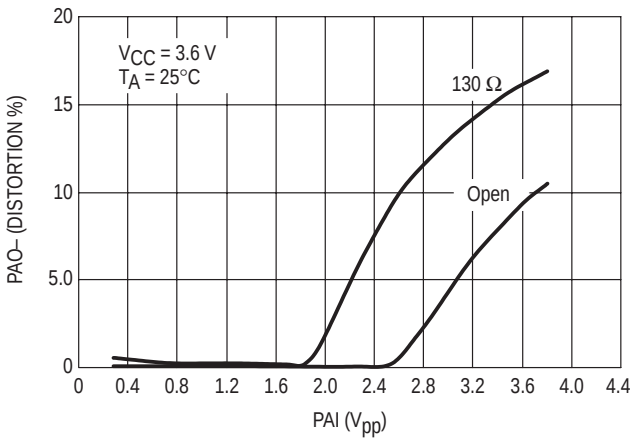
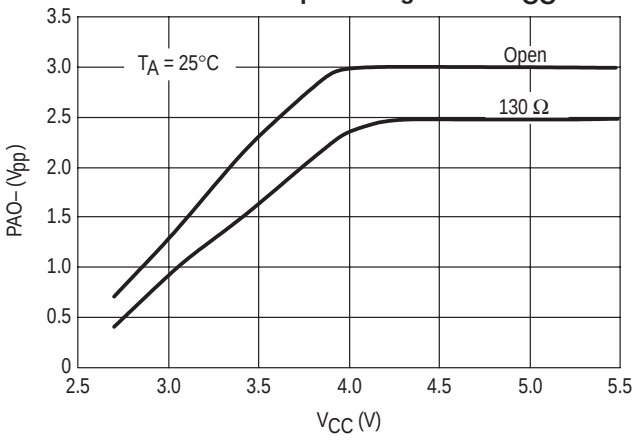


Figure 34. Power Amplifier Maximum Output Swing versus V_{CC}



Reference Oscillator/MCU Clk Out

The reference oscillator provides the frequency basis for the three PLLs, the switched capacitor filters, and the MCU clock output. The source for the reference clock can be a crystal in the range of 4.0 to 18.25 MHz connected to Pins 15 & 16, or it can be an external source connected to F_{ref} In (Pin 15). The reference frequency is directed to:

d. A programmable 12–bit counter (register bits 4/11–0) to provide the reference frequency for the three PLLs. The 12–bit counter is to be set such that, in conjunction with the programmable counters within each PLL, the proper frequencies can be produced by each VCO.

e. A programmable 6–bit counter (register bits 4/17–12), followed by a ÷2 stage, to set the frequency for the switched capacitor filters to 165 kHz, or as close to that as possible.

f. A programmable 3–bit counter (register bits 7/16–14) which provides the MCU clock output (see Tables 6 and 6).

A representation of the reference oscillator is given by Figures 39 and 36.

Figure 35. Reference Oscillator Schematic

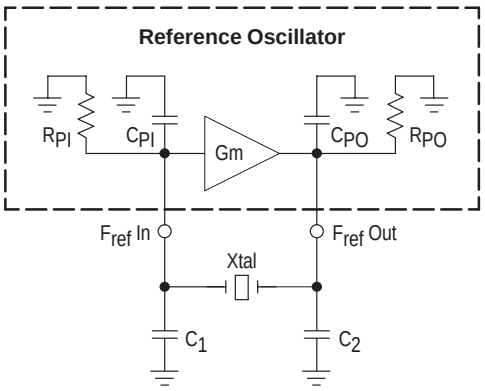


Figure 36. Reference Oscillator Input and Output Impedance

Input Impedance (R_{PI} // C_{PI})	11.6 kΩ // 2.9 pF
Output Impedance (R_{PO} // C_{PO})	4.5 kΩ // 2.5 pF

Figures 37 and 38 show a typical gain/phase response of the oscillator. Load capacitance (C_L), equivalent series resistance (ESR), and even supply voltage will have an effect on the oscillator response as shown in Figures 39 and 40. It should be noted that optimum performance is achieved when C1 equals C2 (C1/C2 = 1).

Figure 41 represents the ESR versus crystal load capacitance for the reference oscillator. This relationship was defined by using a 6.0 dB minimum loop gain margin at 3.6 V. This is considered the minimum gain margin to guarantee oscillator start–up.

Oscillator start–up is also significantly affected by the crystal load capacitance selection. In Figure 39, the relationship between crystal load capacitance and ESR can be seen. The lower the load capacitance the better the performance.

Given the desired crystal load capacitance, C1 and C2 can be determined from Figure 42. It should also be pointed out that current consumption increases when C1 ≠ C2.

Be careful not to overdrive the crystal. This could cause a noise problem. An external series resistor on the crystal output can be added to reduce the drive level, if necessary.

Figure 37. Reference Oscillator Open Loop Gain versus Frequency

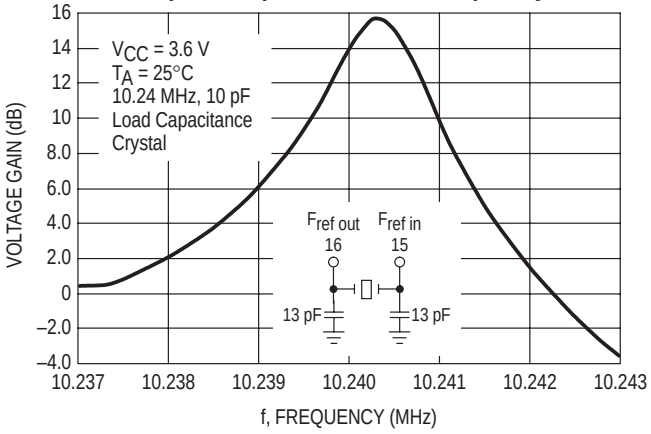


Figure 38. Reference Oscillator Open Loop Phase versus Frequency

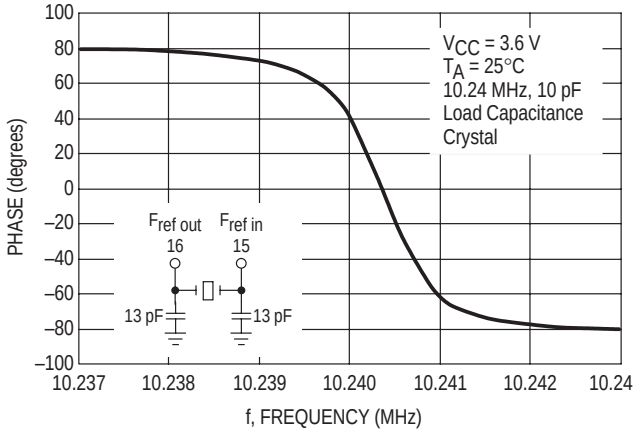


Figure 39. Reference Oscillator Startup Time versus Total ESR – Inactive to Rx Mode

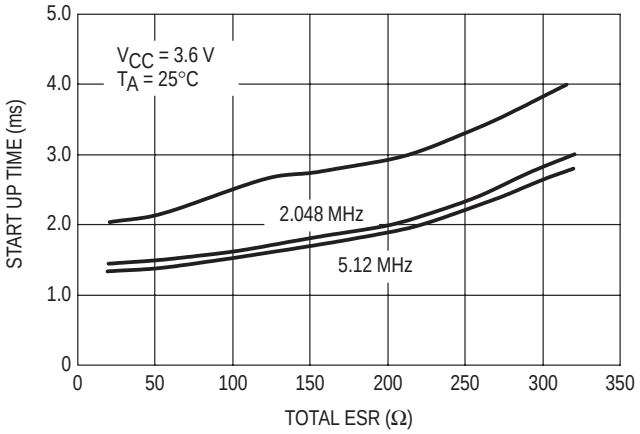


Figure 40. Reference Oscillator Open Loop Gain versus ESR

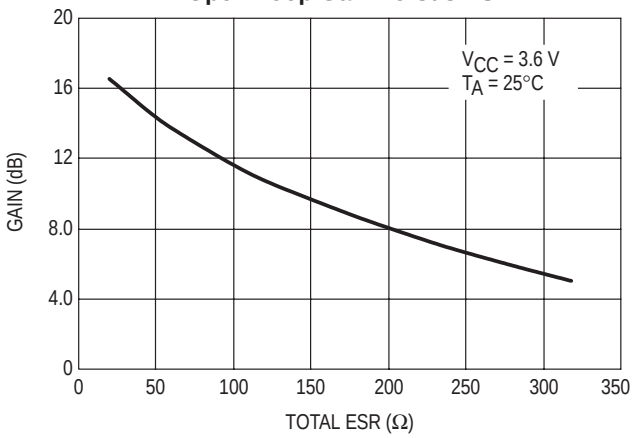


Figure 41. Maximum ESR versus Crystal Load Capacitance (C1 = C2)

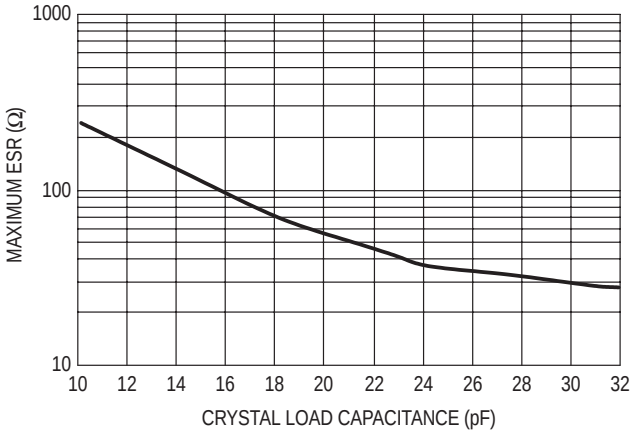


Figure 42. Optimum Values for C1, C2 versus Equivalent Required Parallel Capacitance

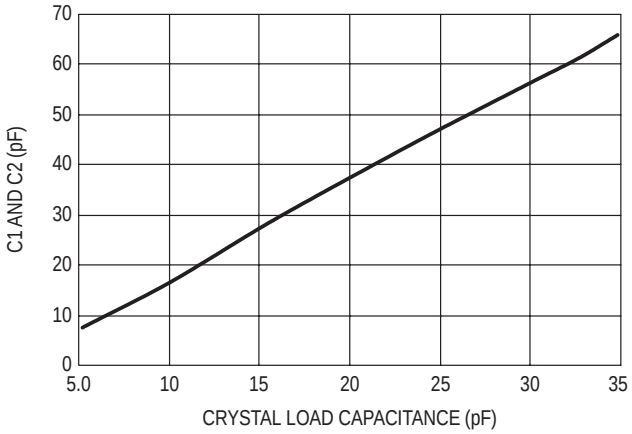


Table 5. MCU Clock Divider Programming

MCU Clk Bit #16	MCU Clk Bit #15	MCU Clk Bit #14	Clk Out Divider Value
0	0	0	2.0
0	0	1	3.0
0	1	0	4.0
0	1	1	5.0
1	0	0	2.5
1	0	1	20
1	1	0	80
1	1	1	312.5

Table 6. MCU Clock Divider Frequencies

Crystal Frequency	Clock Output Divider							
	2.0	2.5	3.0	4.0	5.0	20	80	312.5
10.24 MHz	5.12 MHz	4.096 MHz	3.413 MHz	2.56 MHz	2.048 MHz	512 kHz	128 kHz	32.768 kHz
11.15 MHz	5.575 MHz	4.46 MHz	3.717 MHz	2.788 MHz	2.23 MHz	557 kHz	139 kHz	35.68 kHz
12 MHz	6.0 MHz	4.8 MHz	4.0 MHz	3.0 MHz	2.4 MHz	600 kHz	150 kHz	38.4 kHz

Transmit and Receive (LO1) PLL Sections

The transmit and receive PLLs (Pins 6–9 and 1–4, respectively) are designed to be part of a 900 MHz system. In a typical application the Transmit PLL section will be set up to generate the transmit frequency, and the Receive PLL section will be set up to generate the LO1 frequency. The two sections are identical, and function independently. External requirements for each include a low–pass filter, a 900 MHz VCO, and a 64/65 or 128/129 dual modulus prescaler.

The frequency output of the VCO is to be reduced by the dual modulus prescaler, and then input to the MC33411 (at Pin 8 or 2). That frequency is then further reduced by the programmable 13–bit counter (bits 1/19–7 or 2/19–7), and provided to one side of the Phase Detector, where it is compared with the PLL reference frequency. The output of the phase detector (at Pin 6 or 4) is a Three–State charge pump which drives the VCO through the low–pass filter. Bits 1/20 and 2/20 set the gain of each of the two charge pumps to either 100/2π μA/radian or 400/2π μA/radian. The polarity of the two phase detector outputs is set with bits 1/21 and 2/21. If the bit = 0, the appropriate PLL is configured to operate with a non–inverting low–pass filter/VCO combination. If the low–pass filter/VCO combination is inverting, the polarity bit should be set to 1.

The 7–bit A and A' counters (bits 1/6–0 and 2/6–0) are to be set to drive the Modulus Control input of the 64/65 or 128/129 dual modulus prescalers. The Modulus Control outputs (Pins 9 and 1) can be set to either a voltage mode (logic 1) or a current mode (logic 0) with bit 3/16.

To calculate the settings of the N and A registers, the following procedure is used:

$$\frac{f_{VCO}}{f_{PLL}} = Nt \text{ (Nt must be an integer)} \quad \textbf{(1)}$$

$$\frac{Nt}{P} = N \quad \textbf{(2)}$$

A = Remainder of Equation 2 (decimal part of N x P) **(3)**

where: f_{VCO} = the VCO frequency
f_{PLL} = the PLL Reference Frequency set within the MC33411
P = the smaller divisor of the dual modulus prescaler (64 for a 64/65 prescaler)
N = the whole number portion is the setting for the N (or N') counter within the MC33411
A = the setting for the A (or A') counter within the MC33411

For example, if the VCO is to provide 910 MHz, and the internal PLL reference frequency is 50 kHz, then the equations yield:

$$Nt = \frac{910 \times 10^6}{50 \times 10^3} = 18,200$$

$$N = \frac{18,200}{64} = 284.375$$

$$A = 0.375 \times 64 = 24$$

The N register setting is 284 (0 0001 0001 1100), and the A register setting is 24 (001 1000).

2nd LO (LO2)

This PLL is designed to be the 2nd Local Oscillator in a typical 900 MHz system, and is designed for frequencies up to 80 MHz. The VCO and varactor diodes are included, and are to be used with an external tank circuit (Pins 43–45).

Bits 4/20–18 are used to select an internal capacitor, with a value in the range of 0 to 7.6 pF, to parallel the varactor diodes and the tank's external capacitor. This permits a certain amount of fine tuning of the oscillator's performance. See Table 7.

A buffered output is provided to drive, e.g., a mixer. The frequency is set with the programmable 14–bit counter (bits 3/13–0) in conjunction with the PLL reference frequency. For example, if the reference frequency is 50 kHz, and the 2nd LO frequency is to be 63.3 MHz, the 14–bit counter needs to be set to 1266_d (00 0100 1111 0010). The output level is dependent on the value of the impedance at Pin 41, partly determined by the external pull–up resistor.

The output of the phase detector is a Three–State charge pump which drives the varactor diodes through an external low–pass filter. Bit 3/14 sets the gain of the charge pump to either $100/2\pi$ μA/radian (logic 0) or $400/2\pi$ μA/radian (logic 1). Bit 3/15 sets its polarity – if 0, the PLL is configured to operate with a non–inverting low–pass filter/VCO combination. If the low–pass filter/VCO combination is inverting, the polarity bit should be set to 1. Please note that the 2nd LO VCO on the MC33411 is of the non–inverting type. Figures 43 through 45 describe the response of the 2nd LO.

Table 7. LO2 Capacitor Select Programming

LO2 Capacitor Select Bit #20	LO2 Capacitor Select Bit #19	LO2 Capacitor Select Bit #18	Select #	LO2 Capacitor Select Value
0	0	0	0	0 pF
0	0	1	1	1.1 pF
0	1	0	2	2.2 pF
0	1	1	3	3.3 pF
1	0	0	4	4.3 pF
1	0	1	5	5.4 pF
1	1	0	6	6.5 pF
1	1	1	7	7.6 pF

Figure 43. Varicap Capacitance versus Control Voltage

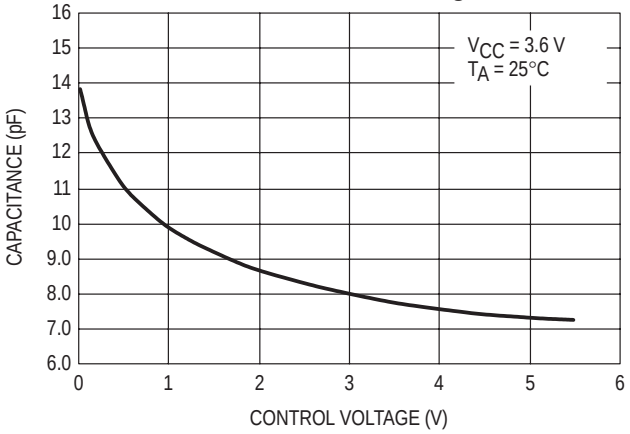


Figure 44. Minimum Overall Q versus Coil Inductance for LO2

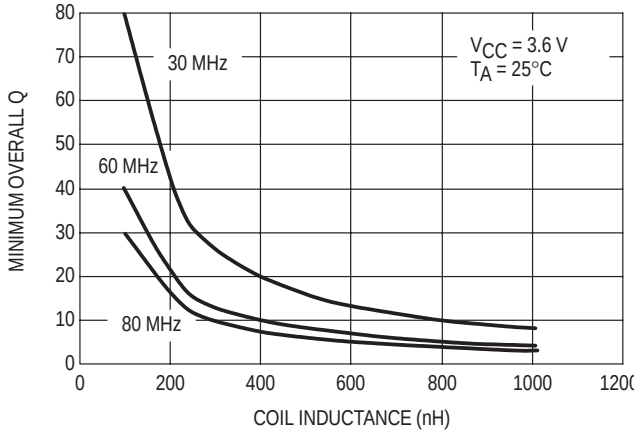
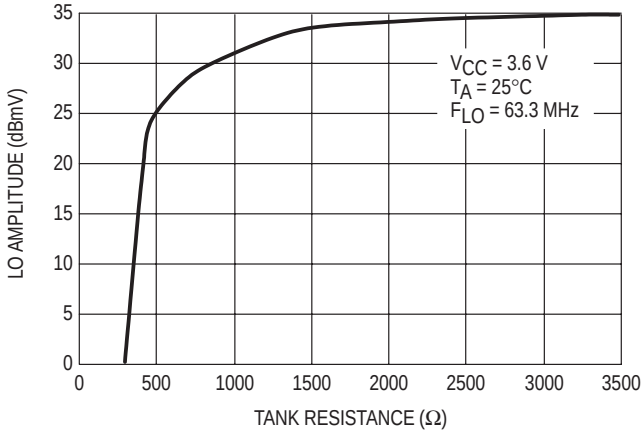


Figure 45. LO2 Amplitude versus Overall Tank Parallel Resistance

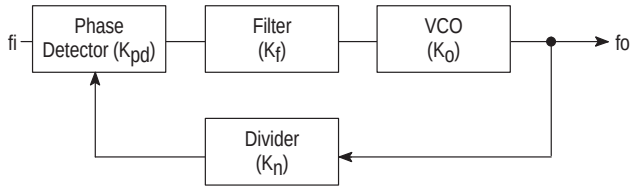


Loop Filter Characteristics

Let's consider the following discussion on loop filters. The fundamental loop characteristics, such as capture range, loop bandwidth, lock–up time, and transient response are controlled externally by loop filtering.

Figure 96 is the general model for a Phase Lock Loop (PLL).

Figure 46. PLL Model



Where:

K_{pd} = Phase Detector Gain Constant
K_f = Loop Filter Transfer Function
K_o = VCO Gain Constant
K_n = Divide Ratio (N)
fi = Input frequency
fo = Output frequency
fo/N = Feedback frequency divided by N

From control theory the loop transfer function can be represented as follows:

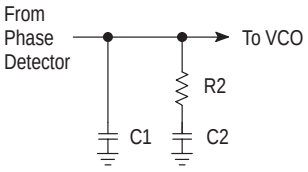
$$A = \frac{K_{pd}\ K_f\ K_o}{K_n} \quad \text{Open loop gain}$$

K_{pd} can be either expressed as being 200 μA/4π or 800 μA/4π. More details about performance of different type PLL loops, refer to Motorola application note AN535.

The loop filter can take the form of a simple low pass filter. A current output, type 2 filter will be used in this discussion since it has the advantage of improved step response, velocity, and acceleration.

The type 2 low pass filter discussed here is represented as follows:

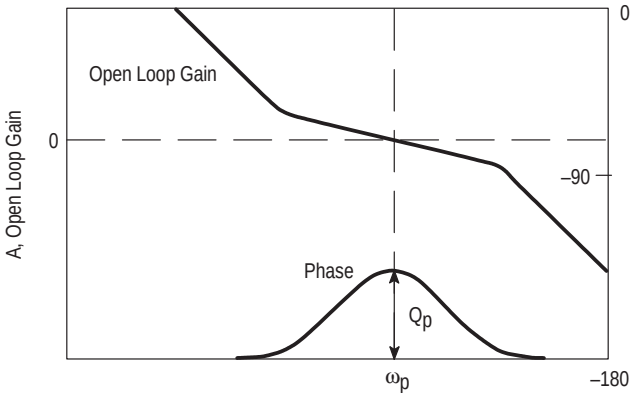
Figure 47. Loop Filter with Additional Integrating Element



From Figure 97, capacitor C1 forms an additional integrator, providing the type 2 response, and filters the discrete current steps from the phase detector output. The function of the additional components R2 and C2 is to create a pole and a zero (together with C1) around the 0 dB point of the open loop gain. This will create sufficient phase margin for stable loop operation.

In Figure 98, the open loop gain and the phase is displayed in the form of a Bode plot. Since there are two integrating functions in the loop, originating from the loopfilter and the VCO gain, the open loop gain response follows a second order slope (–40 dB/dec) creating a phase of –180 degrees at the lower and higher frequencies. The filter characteristic needs to be determined such that it is adding a pole and a zero around the 0 dB point to guarantee sufficient phase margin in this design (Qp in Figure 98).

Figure 48. Bode Plot of Gain and Phase in Open Loop Condition



The open loop gain including the filter response can be expressed as:

$$A_{openloop} = \frac{K_{pd}K_o(1 + j\omega(R2C2))}{j\omega K_n\left(j\omega\left(1 + j\omega\left(\frac{R2C1C2}{C1+C2}\right)\right)\right)} \quad \textbf{(4)}$$

The two time constants creating the pole and the zero in the Bode plot can now be defined as:

$$T1 = \frac{R2C1C2}{C1 + C2} \qquad T2 = R2C2 \quad \textbf{(5)}$$

By substituting equation (5) into (4), it follows:

$$A_{openloop} = \left(\frac{K_{pd}K_oT1}{\omega^2C1K_nT2}\right)\left(\frac{1 + j\omega T2}{1 + j\omega T1}\right) \quad \textbf{(6)}$$

The phase margin (phase + 180) is thus determined by:

$$Q_p = \arctan(\omega T2) - \arctan(\omega T1) \quad \textbf{(7)}$$

At $\omega=\omega_p$, the derivative of the phase margin may be set to zero in order to assure maximum phase margin occurs at ω_p (see also Figure 98). This provides an expression for ω_p:

$$\frac{dQ_p}{d\omega} = 0 = \frac{T2}{1 + (\omega T2)^2} - \frac{T1}{1 + (\omega T1)^2} \quad \textbf{(8)}$$

$$\omega = \omega_p = \frac{1}{\sqrt{T2T1}} \quad \textbf{(9)}$$

Or rewritten:

$$T1 = \frac{1}{\omega_p{}^2T2} \quad \textbf{(10)}$$

By substituting into equation (7), solve for T2:

$$T2 = \frac{\tan\left(\frac{Q_p}{2} + \frac{\pi}{4}\right)}{\omega_p} \quad \textbf{(11)}$$

By choosing a value for ω_p and Q_p, T1 and T2 can be calculated. The choice of Q_p determines the stability of the loop. In general, choosing a phase margin of 45 degrees is a good choice to start calculations. Choosing lower phase margins will provide somewhat faster lock–times, but also generate higher overshoots on the control line to the VCO. This will present a less stable system. Larger values of phase margin provide a more stable system, but also increase lock–times. The practical range for phase margin is 30 degrees up to 70 degrees.

The selection of ω_p is strongly related to the desired lock–time. Since it is quite complicated to accurately calculate lock time, a good first order approach is:

$$T_lock \approx \frac{3}{\omega_p} \quad \textbf{(12)}$$

Equation (12) only provides an order of magnitude for lock time. It does not clearly define what the exact frequency difference is from the desired frequency and it does not show the effect of phase margin. It assumes, however, that the phase detector steps up to the desired control voltage without hesitation. In practice, such step response approach is not really valid. If the two input frequencies are not locked, their phase maybe momentarily zero and force the phase detector into a high impedance mode. Hence, the lock times may be found to be somewhat higher.

In general, ω_p should be chosen far below the reference frequency in order for the filter to provide sufficient attenuation at that frequency. In some applications, the reference frequency might represent the spacing between channels. Any feedthrough to the VCO that shows up as a spur might affect adjacent channel rejection. In theory, with the loop in lock, there is no signal coming from the phase detector. But in practice small current pulses and leakage currents will be supplied to both the VCO and the phase detector. The external capacitors may show some leakage, too. Hence, the lower ω_p, the better the reference frequency is filtered, but the longer it takes for the loop to lock.

As shown in Figure 98, the open loop gain at ω_p is 1 (or 0 dB), and thus the absolute value of the complex open loop gain as shown in equation (6) solves C1:

$$C1 = \left(\frac{K_{pd}K_oT1}{\omega^2K_nT2}\right)\sqrt{\frac{\left(1+\omega_pT2\right)^2}{\left(1+\omega_pT1\right)^2}} \quad \textbf{(13)}$$

With C1 known, and equation (5) solve C2 and R2:

$$C2 = C1\left(\frac{T2}{T1} - 1\right) \quad \textbf{(14)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(15)}$$

The VCO gain is dependent on the selection of the external inductor and the frequency required. The free running frequency of the VCO is determined by:

$$f = \frac{1}{2\pi\sqrt{LC_T}} \quad \textbf{(16)}$$

In which L represents the external inductor value and C_T represents the total capacitance (including internal capacitance) in parallel with the inductor. The VCO gain can be easily calculated via the internal varicap transfer curve shown in Figure 43.

As can be derived from Figure 43, the varicap capacitance changes 2.0 pF over the voltage range from 1.0 V to 3.0 V:

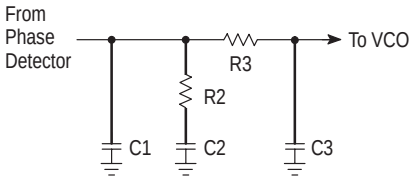
$$\Delta Cvar = \frac{2.0\ pF}{2.0\ V} \quad \textbf{(17)}$$

Combining (16) with (17) the VCO gain can be determined by:

$$K_O = \frac{1}{j2.0V}\left\{\frac{1}{2\pi\sqrt{LC_T}} - \frac{1}{2\pi\sqrt{L\left(C_T + \frac{\Delta Cvar}{2}\right)}}\right\} \quad \textbf{(18)}$$

Although the basic loopfilter previously described provides adequate performance for most applications, an extra pole may be added for additional reference frequency filtering. Given that the channel spacing is based on the reference frequency, and any feedthrough to the first LO may effect parameters like adjacent channel rejection and intermodulation. Figure 100 shows a loopfilter architecture incorporating an additional pole.

Figure 49. Loop Filter with Additional Integrating Element



For the additional pole formed by R3 and C3 to be efficient, the cut–off frequency must be much lower than the reference frequency. However, it must also be higher than ω_p in order not to compromise phase margin too much. The following equations were derived in a similar manner as for the basic filter previously described.

Similarly, it can be shown:

$$A_{openloop} = -\frac{K_{pd}K_o}{K_n\omega^2\left((C1 + C2 + C3) - \omega^2 C1C2C3R2R3\right)} + \frac{1 + j\omega T2}{1 + j\omega T1} \quad \textbf{(19)}$$

In which:

$$T1 = \frac{(C1 + C2)T2 + (C1C2)T3}{C1 + C2 + C3 - \omega^2 C1T2T3} \quad \textbf{(20)}$$

$$T2 = R2C2 \quad \textbf{(21)} \qquad T3 = R3C3 \quad \textbf{(22)}$$

From T1 it can be derived that:

$$C2 = \frac{(T1 + T2)C3 - C1\left(T2 + T3 - T1 + \omega^2 T1T2T3\right)}{T3 - T1} \quad \textbf{(23)}$$

In analogy with (13), by forcing the loopgain to 1 (0 dB) at ω_p, we obtain:

$$C1(T1 + T2) + C2T3 + C3T2 = \left(\frac{K_{pd}K_o}{K_n{\omega_p}^2}\right)\sqrt{\frac{1 + \left(\omega_p T2\right)^2}{1 + \left(\omega_p T1\right)^2}} \quad \textbf{(24)}$$

Solving for C1:

$$C1 = \frac{(T2 - T1)T3C3 - (T3 - T1)T2C3 + (T3 - T1)\left(\frac{K_{pd}K_oT1}{{\omega_p}^2K_n}\right)\sqrt{\frac{1+\left(\omega_p T2\right)^2}{1+\left(\omega_p T1\right)^2}}}{(T3 - T1)T2 + (T3 - T1)T3 - \left(T2 + T3 - T1 + {\omega_p}^2T1T2T3\right)T3} \quad \textbf{(25)}$$

By selecting ω_p via (12), the additional time constant expressed as T3, can be set to:

$$T3 = \frac{1}{K\omega_p} \quad \textbf{(26)}$$

The K–factor shown determines how far the additional pole frequency will be separated from ω_p. Selecting too small of a K–factor, the equations may provide negative capacitance or resistor values. Too large of a K–factor may not provide the maximum attenuation.

By selecting R3 to be 100 kΩ, C3 becomes known and C1 and C2 can be solved from the equations. By using equations (11) and (10), time constants T2 and T1 can be derived by selecting a phase margin. Finally, R2 follows from T2 and C2.

A test circuit with the following components and conditions was constructed with these results:

Loop Filter (See Figure 100):
- C1 = 470 pF
- R2 = 68 kΩ
- C2 = 3.9 nF
- R3 = 270 kΩ
- C3 = 82 pF

LO2 Tank:
- Ctotal = 39.3 pF
- Lext = 150 nH, Q = 50 @ 250 MHz
- Reference Frequency = 10.24 MHz (unadjusted)
- R Counter = 205
- LO2 Counter = 1266
- AC Load = 25 Ω
- Frequency of LO2 = 63.258 MHz
- Phase Noise @ 50 kHz offset = –107 dBc
- Sidebands @ 50 kHz & 100 kHz offsets = –69 dBc

Low Battery/ RSSI Voltage Measurement

Both the Low Battery (bits 5/23–18) and RSSI (bits 5/17–12) measurement circuits have a 6–bit A/D converter whose value may be read back via the SPI. The A/D's sample their voltages at a frequency equal to the internal SCF clock frequency divided by 128. The Low Battery Measurement A/D senses and divides by 2.5 the supply voltage (at Pin 23). Please note that the minimum Low Battery Detect (LBD) voltage is 2.7 V, since there is no guarantee that the device will operate below this value. The RSSI Measurement senses the voltage at Pin 37.

These values are compared to the internal reference VB (≈1.5 V) which is available at Pin 37. The value read back from the LBD A/D will therefor be approximately:

$$N(\text{for LBD}) \approx \frac{63\ (V_{CC})}{2.5(VB)(1.07)} \quad \textbf{(27)}$$

and for the RSSI

$$N(\text{for RSSI}) \approx \frac{63\ (\text{RSSIVoltage})}{(VB)(1.07)} \quad \textbf{(28)}$$

VB Voltage Adjust and Characteristics

VB has a production tolerance of ±8%, and can be adjusted over a ±9% range using bits 3/20–17. The adjustment steps will be ≈1.2% each (See Table 8). If desired, VB can be used to bias external circuitry, as long as the load current on this pin does not exceed 10 μA. V_B varies by less than ±0.5% over supply voltage, referenced to V_{CC} = 3.6 V.

The value of the de–coupling capacitor connected from VB to ground affects both the noise and crosstalk from the receive and transmit audio paths, so the value should be chosen with caution. Figures 50 and 51 show this relationship.

Table 8. VB Voltage Reference Programming

V_{ref} Adjust Bit #20	V_{ref} Adjust Bit #19	V_{ref} Adjust Bit #18	V_{ref} Adjust Bit #17	V_{ref} Adjust #	Voltage Reference Adjustment Amount
0	0	0	0	0	–9.0%
0	0	0	1	1	–7.8%
0	0	1	0	2	–6.6%
0	0	1	1	3	–5.4%
0	1	0	0	4	–4.2%
0	1	0	1	5	–3.0%
0	1	1	0	6	–1.8%
0	1	1	1	7	–0.6%
1	0	0	0	8	0.6%
1	0	0	1	9	1.8%
1	0	1	0	10	3.0%
1	0	1	1	11	4.2%
1	1	0	0	12	5.4%
1	1	0	1	13	6.6%
1	1	1	0	14	7.8%
1	1	1	1	15	9.0%

Figure 50. Crosstalk/Noise from C In to E Out versus VB Capacitor

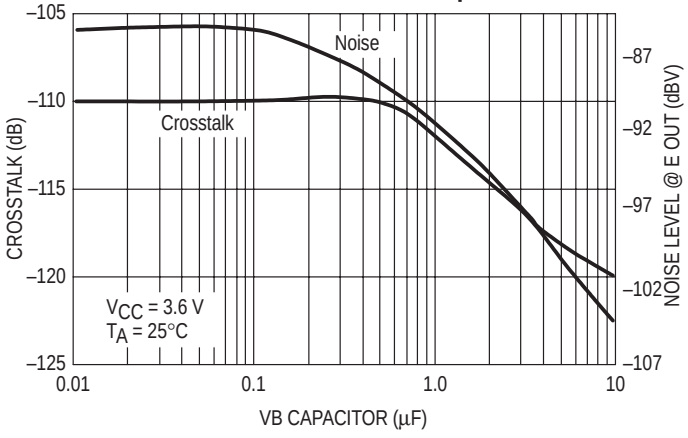
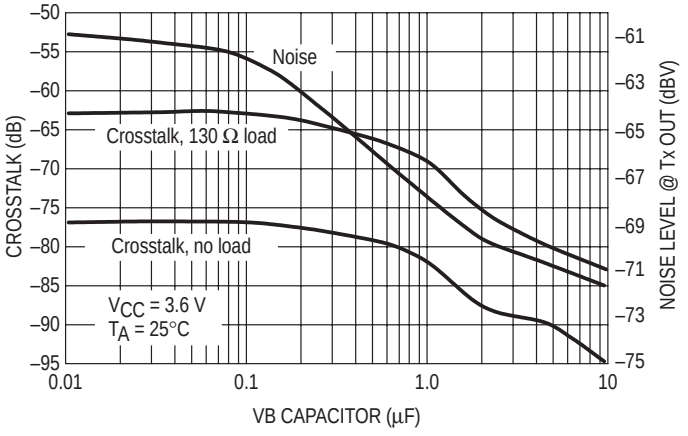


Figure 51. Crosstalk/Noise from E In to Tx Out versus VB Capacitor



MCU Serial Interface

The MCU Serial Interface is a 3–wire interface, consisting of a Clock line, an Enable line, and a bi–directional Data line. The interface is always active, i.e., it cannot be powered down as all other sections of the MC33411 are disabled and enabled through this interface.

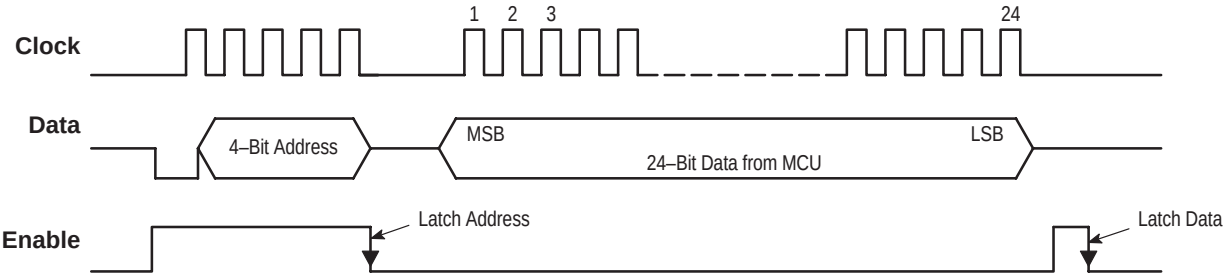
After the device power–up (or whenever a reset condition is required), the MCU should perform the following steps:

13. Initialize the Data line to a high impedance state.
14. Initialize the Clock line to a logic low.
15. Initialize the Enable line to a logic low.
16. Pulse the Clock line a minimum of once (RZ format) while leaving the Enable line continuously low. This places the SPI port into a known condition.
17. Load all registers with their desired initial values.

The clock (Return–to–Zero format) must be supplied to the MC33411 at Pin 11 to write or read data, and can be any frequency up to 2.0 MHz. The clock need not be present when data is not being transferred. The Enable line must be low when data is not being transferred.

Internally there are 7 data registers, 24–bits each, addressed with 4–bits ranging from $h1 to $h7 (see Tables 9 and 10). Register 5, bits 23–12 are read–only bits, while all other register bits are Read/Write. All unused/unimplemented bits are reserved for Motorola use only. The contents of the 7 registers can be read out at any time. All bits are written in, or read out, on the clock's positive transition. The write and read operations are as follows:

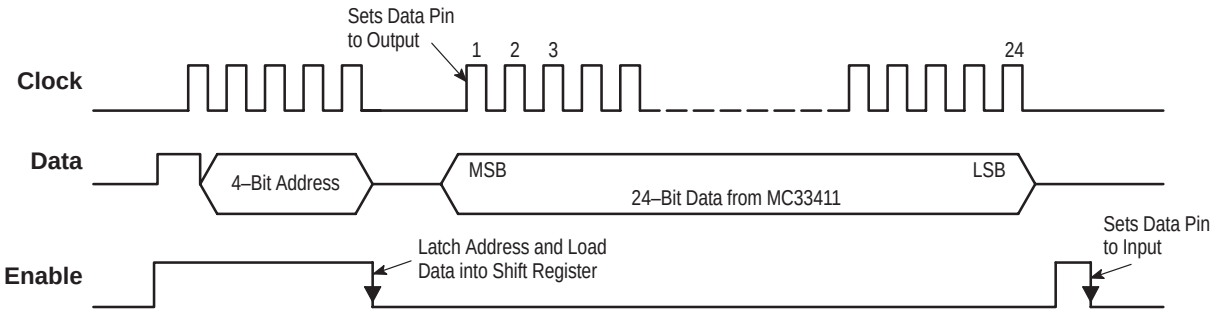
Figure 52. Writing Data to the MC33411



a. Write Operation:
   – To write data to the MC33411, the following sequence is required (see Figure 3):
18. The Enable line is taken high.
19. Five bits are entered:
   – The first bit must be a 0 to indicate a Write operation.
   – The next four bits identify the register address (0001–0111). The MSB is entered first.
20. The Enable line is taken low. At this transition, the address is latched in and decoded.
21. The Enable line is maintained low while the data bits are clocked in. The MSB is entered first, and the LSB last. If 24–bits are written to a register which has less than 24 active bits (e.g., register 6), the unassigned bits are to be 0.
22. After the last bit is entered, the Enable line is to be taken high and then low. The falling edge of this pulse latches in the just entered data. The clock line must be at a logic low and must not transition in either direction during this Enable pulse.
23. The Enable line must then be kept low until the next communication.

Note: If less than 24 bits are to be written to a data register, it is not necessary to enter the full 24 bits, as long as they are all lower order bits. For example, if bits 0–6 of a register are to be updated, they can be entered as 7 bits with 7 clock cycles in step 4 above. However, if this procedure is used, a minimum of 4 bits, with 4 clock pulses, must be entered.

Figure 53. Reading Data from the MC33411



b. Read Operation:
   – To read the output bits (bits 5/23–12), or the contents of any register, the following sequence is required (see Figure 4):

1. The Enable line is taken high.
2. Five bits are entered:
   – The first bit must be a 1 to indicate a Read operation.
   – The next four bits identify the register address (0001–0111). The MSB is entered first.
3. The Enable line is taken low. At this transition, the address is latched in and decoded, and the contents of the selected register is loaded into the 24–bit output shift register. At this point, the Data line (Pin 12) is still an input.
4. While maintaining the Enable line low, the data is read out. The first clock rising edge will change the Data line to an output, and the MSB will be present on this line.
5. The full contents of the register are then read out (MSB first, LSB last) with a total of 24 clock rising edges, including the one in step 4 above. It is recommended that the MCU read the bits after the clock's falling edge.
6. After the last clock pulse, the Enable line is to be taken high and then low. The falling edge of this pulse returns the Data Pin to be an input. The clock line must be at a logic low and must not transition in either direction during this Enable pulse.
7. The Enable line must then be kept low until the next communication.

Power Supply/Power Saving Modes

The power supply voltage, applied to all V_{CC} pins, can range from 2.7 to 5.5 V. All V_{CC} pins must be within ±0.5 V of each other, and each must be bypassed. It is recommended a ground plane be used, and all leads to the MC33411 be as short and direct as possible. To reduce the possibility of device latch–up, it is highly recommended that the Audio, Synthesizer and RF V_{CC} portions of the chip be isolated from the main supply through 10 to 25 Ω resistors (see the Evaluation PCB Schematic, Figure 54). This also provides RF–to–Audio noise isolation. The supply and ground pins are distributed as follows:

1. Pin 23 provides power to the audio section. Pin 40 is the ground pin.
2. Pin 28 provides power to the speaker amplifier section. Pin 31 is the ground pin.
3. Pin 3 provides power to the Rx PLL section. Pin 5 is the ground pin.
4. Pin 7 provides power to the Tx PLL section, and the MCU interface. Pin 5 is the ground pin.
5. Pin 42 provides power to the 2nd LO section. Pins 46 and 48 are the ground pins.
6. Pin 14 is the ground pin for the digital circuitry. Power for the digital circuitry is derived from Pin 23.

To conserve power, various sections can be individually disabled by using bits 5/7–0 and 6/7 (setting a bit to 1 disables the section).

1. Reference Oscillator Disable (bit 5/0) – The reference oscillator at Pins 15 and 16 is disabled, thereby denying a clock to the three PLLs and the switched capacitor filters. This function is not available on the "B" version.
2. Tx PLL Disable (bit 5/1) – The 13–bit and 7–bit counters, input buffer, phase detector, and modulus control blocks are disabled. The charge pump output at Pin 6 will be in a Hi–Z state.
3. Rx PLL Disable (bit 5/2) – The 13–bit and 7–bit counters, input buffer, phase detector, and modulus control blocks are disabled. The charge pump output at Pin 4 will be in a Hi–Z state.
4. LO2 PLL Disable (bit 5/3) – The VCO, 14–bit counter, output buffer, and phase detector are disabled. The charge pump output at Pin 47 will be in a Hi–Z state.
5. Power Amplifier Disable (bit 5/4) – The two speaker amplifiers are disabled. Their outputs will go to a high impedance state.
6. Rx Audio Path Disable (bit 5/5) – The anti–aliasing filter, low–pass filter, and variable gain stage are disabled.
7. Tx Audio Path Disable (bit 5/6) – Disables the microphone amplifier and low–pass filter.
8. Low Battery/RSSI Measurement Disable (bit 5/7) – Both 6–bit A/Ds are disabled.
9. Data Slicer Disable (bit 5/8) – The data slicer is disabled and DS Out goes to high impedance.
10. MCU Clock Disable (bit 6/7) – The MCU clock counter is disabled and the MCU Clock Output will be in a Hi–Z state. This function is not available on the "B" version.

Note: The 12–bit reference counter is disabled if the three PLLs are disabled (bits 5/1–3 = 1).

Table 9. Register Map

Reg Add	Reg Num	MSB Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0
0001	1			Tx Polarity Select	Tx PD Cur Sel	MSB	13–Bit Tx N Counter Divide Value											LSB	MSB	7–Bit Tx A Counter Divide Value					LSB
0010	2			Rx Polarity Select	Rx PD Cur Sel	MSB	13–Bit Rx N' Counter Divide Value											LSB	MSB	7–Bit Rx A' Counter Divide Value					LSB
0011	3				VB Voltage Reference Adjust				FTxMC/ FRxMC Mode	LO2 Polarity Select	2nd LO PD Cur Sel	MSB	14–Bit 2nd LO Counter Divide Value												LSB
0100	4	Test Modes			LO2 Capacitor Select			6–Bit Switched Capacitor Filter Counter Divide Value						MSB	12–Bit Reference Counter Divide Value											LSB
0101	5	6–Bit Battery Voltage A/D Output						6–Bit RSSI A/D Output						Unused Register Bits		Data Slicer Invert	Data Slicer Disable	RSSI & Batt. A/D Disable	Tx Audio Disable	Rx Audio Disable	Power Amp Disable	2nd LO PLL Disable	Rx PLL Disable	Tx PLL Disable	Ref Osc Disable*
0110	6												ALC Gain = 25	ALC Gain = 10	Side Tone Attenuate Select		Comp. Low Max. Gain En.	MCU Clk Disable*	ALC Disable	Limiter Disable	Compres– ser Pass– through	Expander Pass– through	Tx Mute	Rx Mute	Power Amp Mute
0111	7								MCU Clock Divide Select			Volume Control				Tx Gain Adjust					Rx Gain Adjust				

* These bits not included in "B" version.

Table 10. Register Map: Power–Up Defaults

Reg Add	Reg Num	MSB Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0
0001	1			Tx Polarity Select	Tx PD Cur Sel	MSB	13–Bit Tx N Counter Divide Value											LSB	MSB	7–Bit Tx A Counter Divide Value					LSB
				0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0010	2			Rx Polarity Select	Rx PD Cur Sel	MSB	13–Bit Rx N' Counter Divide Value											LSB	MSB	7–Bit Rx A' Counter Divide Value					LSB
				0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0011	3				VB Voltage Reference Adjust				FTxMC/ FRxMC Mode	LO2 Polarity Select	2nd LO PD Cur Sel	MSB	14–Bit 2nd LO Counter Divide Value												LSB
					0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0100	4	Test Modes			LO2 Capacitor Select			6–Bit Switched Capacitor Filter Counter Divide Value						MSB	12–Bit Reference Counter Divide Value											LSB
		0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0101	5	6–Bit Battery Voltage A/D Output						6–Bit RSSI A/D Output						Unused Register Bits		Data Slicer Invert	Data Slicer Disable	RSSI & Batt. A/D Disable	Tx Audio Disable	Rx Audio Disable	Power Amp Disable	2nd LO PLL Disable	Rx PLL Disable	Tx PLL Disable	Ref Osc Disable*
														0	0	0	0	0	0	0	0	0	0	0	0
0110	6												ALC Gain = 25	ALC Gain = 10	Side Tone Attenuate Select		Comp. Low Max. Gain En.	MCU Clk Disable*	ALC Disable	Limiter Disable	Compres– ser Pass– through	Expander Pass– through	Tx Mute	Rx Mute	Power Amp Mute
													0	0	0	0	0	0	0	0	0	0	0	0	0
0111	7								MCU Clock Divide Select			Volume Control				Tx Gain Adjust					Rx Gain Adjust				
									0	1	1	0	1	1	1	0	1	1	1	1	0	1	1	1	1

* These bits not included in "B" version.

Evaluation PCB

The evaluation PCB is a versatile board which allows the MC33411 to be configured to analyze individual operating parameters or the complete audio transmit and receive paths.

The general purpose schematic and associated parts list for the PCB are given in Figure 54. With the jumpers positioned as shown in the parts list (either shunt or open). the PCB is configured to analyze complete transmit and receive audio paths.

Parts lists as ”user defined” can be installed to analyze other functions of the device. Table 3 lists these devices along with their respective functions.

Table 11.

Component(s)	Function	Notes
R20	Microphone Bias	
R19,J24,J27	Pre–emphasis/De–emphasis	
R3,C7,J5	Detector Low–Pass Filter (LPF)	
R4,C8	Data Slicer LPF	
L1,C21	2nd LO Tank	See Equations 16 and 17
C18,R9,C19,R10,C20	2nd LO LPF	See Eq. 10, 11, 12, 21, 23, 25, and 26
C26,R13,C27,R14,C28	Rx 1st LO LPF	See Eq. 10, 11, 12, 21, 23, 25, and 26
C22,R11,C23,R12,C24	Tx 1st LO LPF	See Eq. 10, 11, 12, 21, 23, 25, and 26

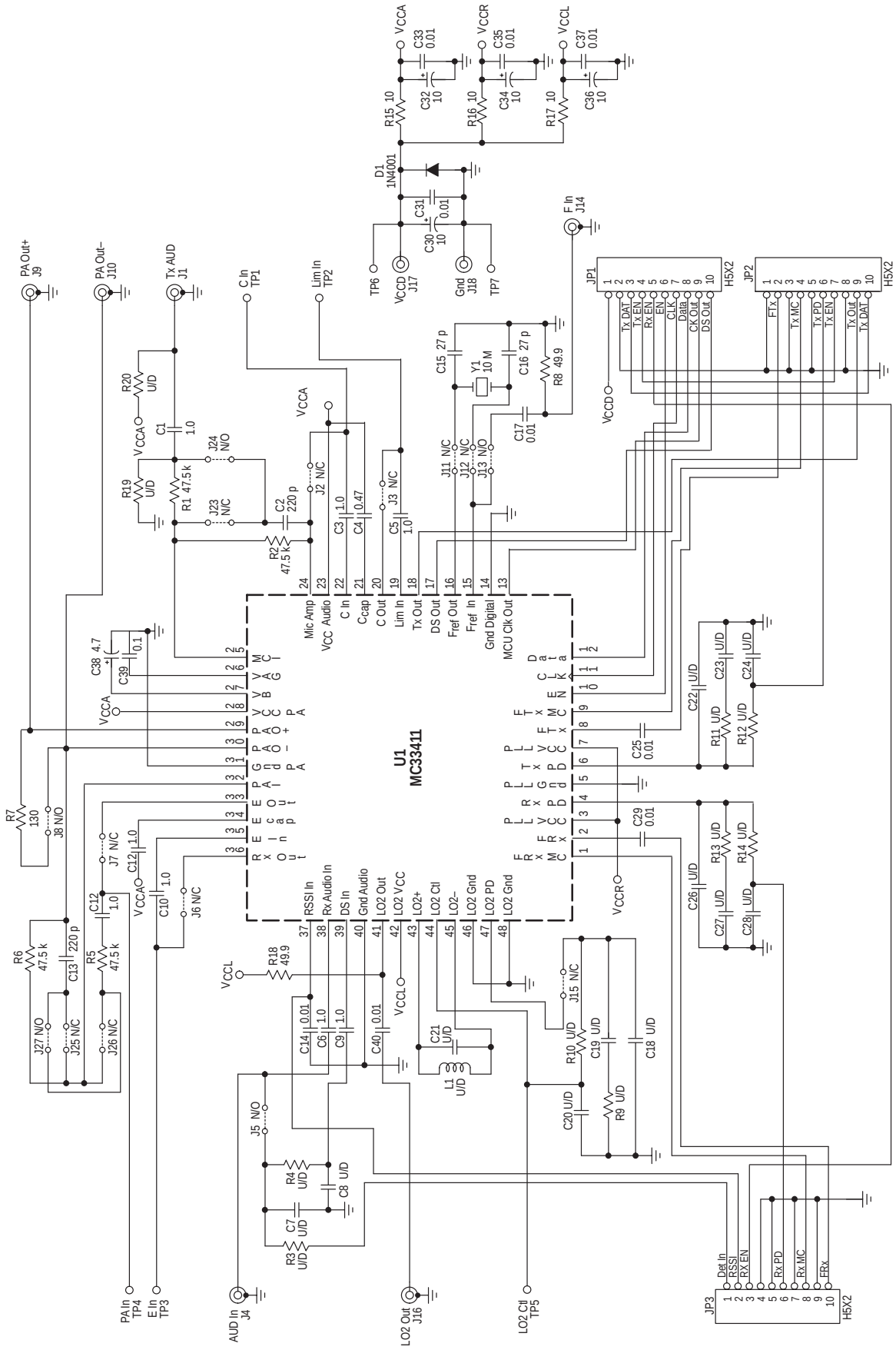
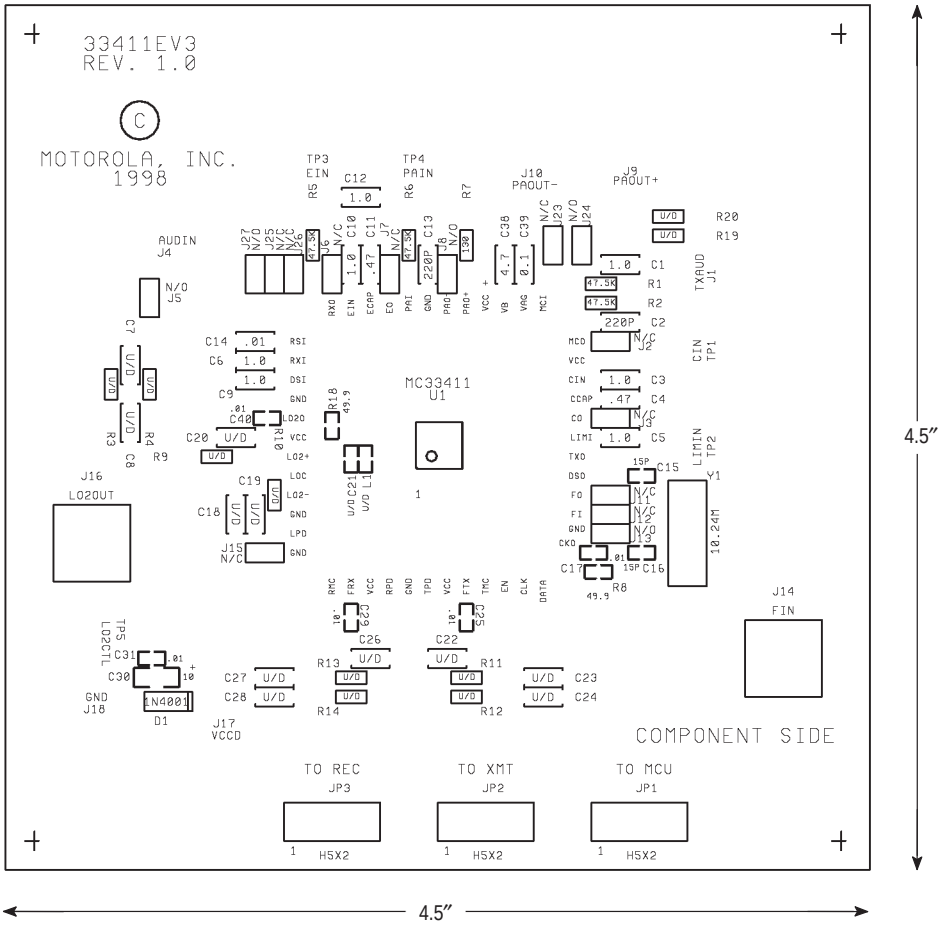


Figure 54. MC33411A/B Evaluation PCB Schematic

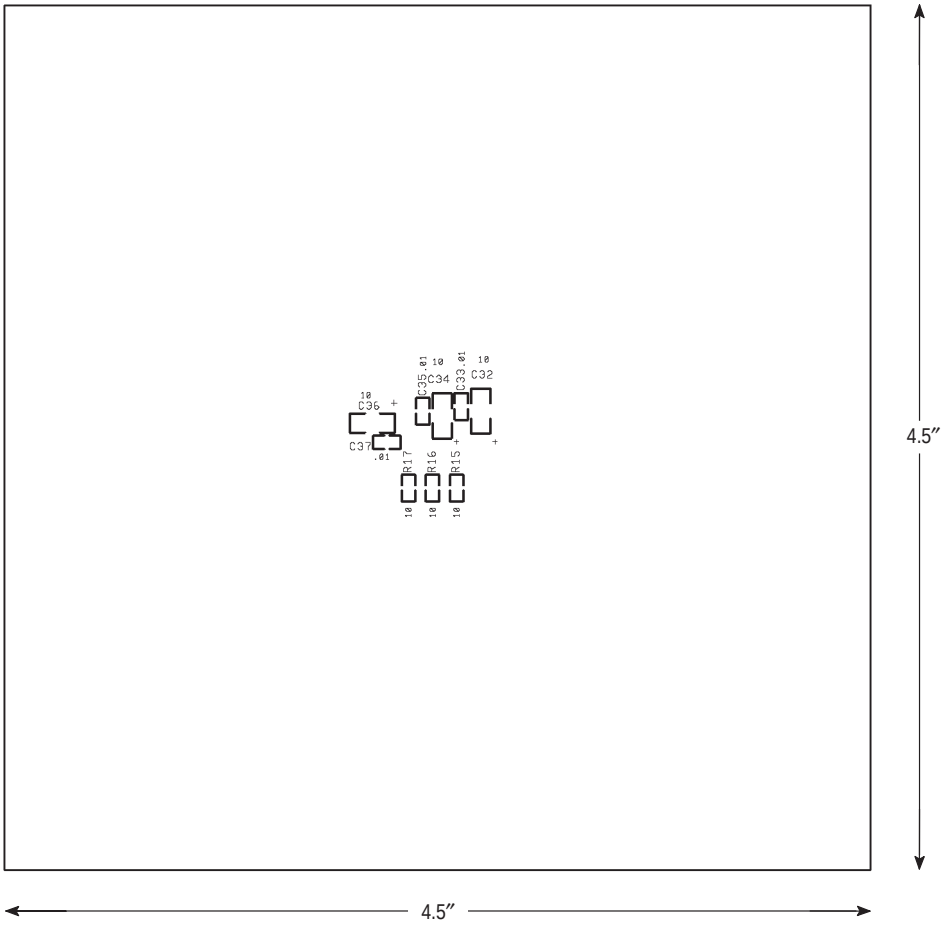
Figure 55. MC33411A/B Evaluation PCB Component Side



C1,C3,C5,C6,C9,C10,C12	1.0	JP1,JP2,JP3	Header, 5x2
C13,C2	220 p	J1,J4,J9,J10	AudioJack
C4,C11	0.47		Switchcroft 3501FP
L1,R3,R4,C7,C8,R9,R10,	User defined	J2,J3,J6,J7,J11,J12,J15,	
R11,R12,R13,R14,C18,R19,		J23,J25,J26	Shunt
C19,R20,C20,C21,C22,C23,		J5,J8,J13,J24,J27	Open
C24,C26,C27,C28		J14,J16	SMA EF Johnson 142–0701–201
C14,C17,C25,C29,C31,C33,	0.01	J17,J18	Bananna Johnson Components
C35,C37,C40			108–0902–001
C15,C16	27 p	R1,R2,R5,R6	47.5 k
C30,C32,C34,C36	10	R7	130
C38	4.7	R8,R18	49.9
C39	0.1	R15,R16,R17	10
D1	1N4001	U1	MC33411AFTA or MC33411BFTA
		Y1	10 M Raltron A–10.000–18

Default Units: Microfarads, Microhenries, and Ohms

Figure 56. MC33411A/B Evaluation PCB Solder Side



MC144110
MC144111

Digital-to-Analog Converters with Serial Interface

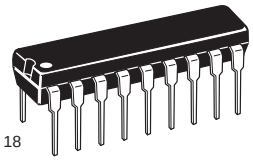
CMOS LSI

The MC144110 and MC144111 are low–cost 6–bit D/A converters with serial interface ports to provide communication with CMOS microprocessors and microcomputers. The MC144110 contains six static D/A converters; the MC144111 contains four converters.

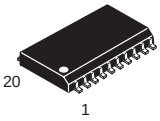
Due to a unique feature of these DACs, the user is permitted easy scaling of the analog outputs of a system. Over a 5 to 15 V supply range, these DACs may be directly interfaced to CMOS MPUs operating at 5 V.

- Direct R–2R Network Outputs
- Buffered Emitter–Follower Outputs
- Serial Data Input
- Digital Data Output Facilitates Cascading
- Direct Interface to CMOS µP
- Wide Operating Voltage Range: 4.5 to 15 V
- Wide Operating Temperature Range: 0 to 85°C
- Software Information is Contained in Document M68HC11RM/AD

MC144110

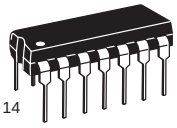


P SUFFIX
PLASTIC DIP
CASE 707

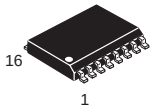


DW SUFFIX
SOG PACKAGE
CASE 751D

MC144111



P SUFFIX
PLASTIC DIP
CASE 646

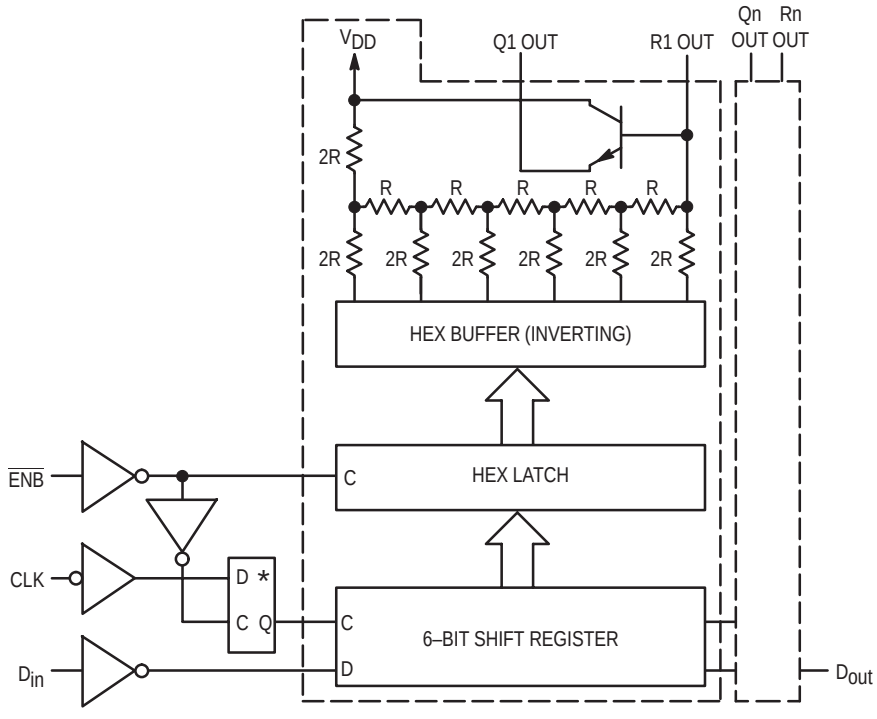


DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

MC144110P	Plastic DIP
MC144110DW	SOG Package
MC144111P	Plastic DIP
MC144111DW	SOG Package

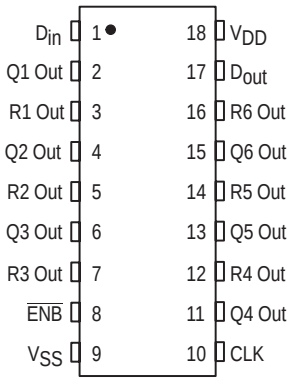
BLOCK DIAGRAM



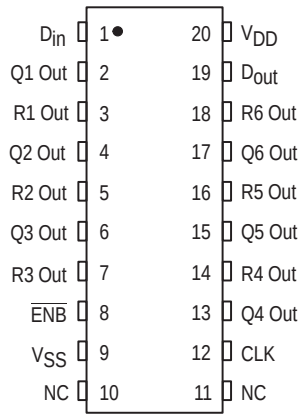
* Transparent Latch

PIN ASSIGNMENTS

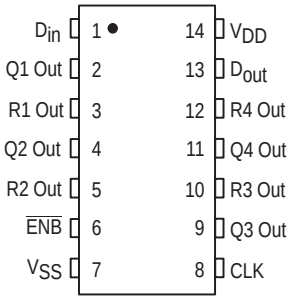
MC144110P



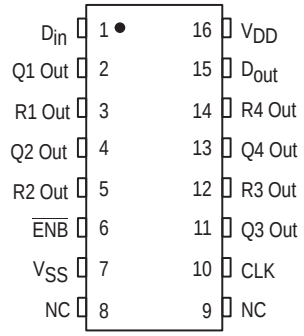
MC144110DW



MC144111P



MC144111DW



NC = NO CONNECTION

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 18	V
Input Voltage, All Inputs	V_{in}	– 0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I	± 10	mA
Power Dissipation (Per Output) T_A = 70°C, MC144110 MC144111 T_A = 85°C, MC144110 MC144111	P_{OH}	 30 50 10 20	mW
Power Dissipation (Per Package) T_A = 70°C, MC144110 MC144111 T_A = 85°C, MC144110 MC144111	P_D	 100 150 25 50	mW
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields; however, it is advised that precautions be taken to avoid application of voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

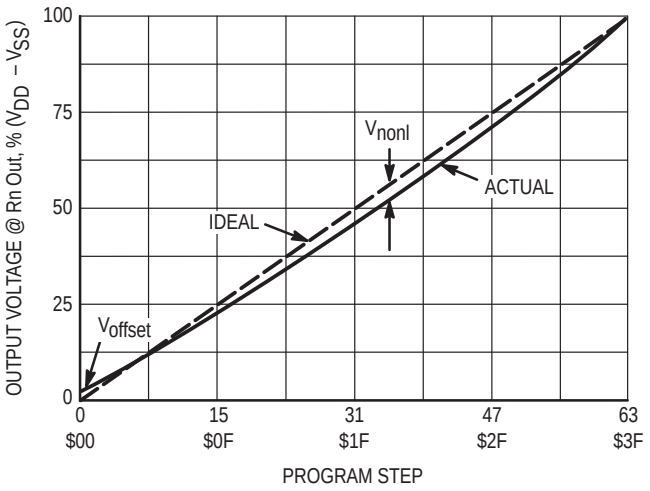
ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS}, T_A = 0 to 85°C unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD}	Min	Max	Unit
V_{IH}	High–Level Input Voltage (D_{in}, $\overline{ENB}$, CLK)		5 10 15	3.0 3.5 4	— — —	V
V_{IL}	Low–Level Input Voltage (D_{in}, $\overline{ENB}$, CLK)		5 10 15	— — —	0.8 0.8 0.8	V
I_{OH}	High–Level Output Current (D_{out})	$V_{out} = V_{DD} – 0.5$ V	5	– 200	—	µA
I_{OL}	Low–Level Output Current (D_{out})	V_{out} = 0.5 V	5	200	—	µA
I_{DD}	Quiescent Supply Current MC144110 MC144111	I_{out} = 0 µA	15 15	— —	12 8	mA
I_{in}	Input Leakage Current (D_{in}, $\overline{ENB}$, CLK)	$V_{in} = V_{DD}$ or 0 V	15	—	± 1	µA
V_{nonl}	Nonlinearity Voltage (Rn Out)	See Figure 1	5 10 15	— — —	100 200 300	mV
V_{step}	Step Size (Rn Out)	See Figure 2	5 10 15	19 39 58	137 274 411	mV
V_{offset}	Offset Voltage from V_{SS}	D_{in} = $00, See Figure 1	—	—	1	LSB
I_E	Emitter Leakage Current	$V_{Rn\ Out}$ = 0 V	15	—	10	µA
h_{FE}	DC Current Gain	I_E = 0.1 to 10.0 mA T_A = 25°C	—	40	—	—
V_{BE}	Base–to–Emitter Voltage Drop	I_E = 1.0 mA	—	0.4	0.7	V

SWITCHING CHARACTERISTICS

(Voltages referenced to V_{SS}, T_A = 0 to 85°C, C_L = 50 pF, Input $t_r = t_f$ = 20 ns unless otherwise indicated)

Symbol	Parameter	V_{DD}	Min	Max	Unit
t_{wH}	Positive Pule Width, CLK (Figures 3 and 4)	5 10 15	2 1.5 1	— — —	µs
t_{wL}	Negative Pulse Width, CLK (Figure 3 and 4)	5 10 15	5 3.5 2	— — —	µs
t_{su}	Setup Time, $\overline{ENB}$ to CLK (Figures 3 and 4)	5 10 15	5 3.5 2	— — —	µs
t_{su}	Setup Time, D_{in} to CLK (Figures 3 and 4)	5 10 15	1000 750 500	— — —	ns
t_h	Hold Time, CLK to $\overline{ENB}$ (Figures 3 and 4)	5 10 15	5 3.5 2	— — —	µs
t_h	Hold Time, CLK to D_{in} (Figures 3 and 4)	5 10 15	5 3.5 2	— — —	µs
t_r, t_f	Input Rise and Fall Times	5 – 15	—	2	µs
C_{in}	Input Capacitance	5 – 15	—	7.5	pF



LINEARITY ERROR (integral linearity). A measure of how straight a device's transfer function is, it indicates the worst–case deviation of linearity of the actual transfer function from the best–fit straight line. It is normally specified in parts of an LSB.

Figure 1. D/A Transfer Function

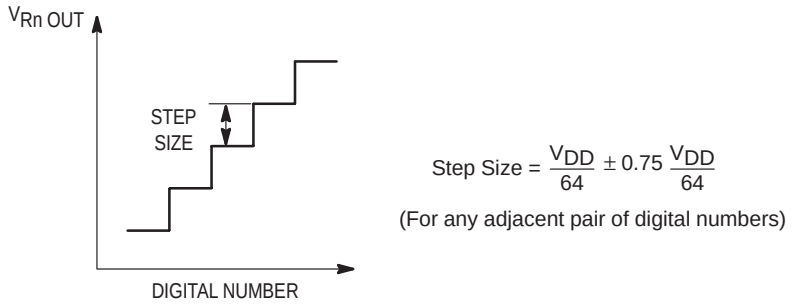


Figure 2. Definition of Step Size

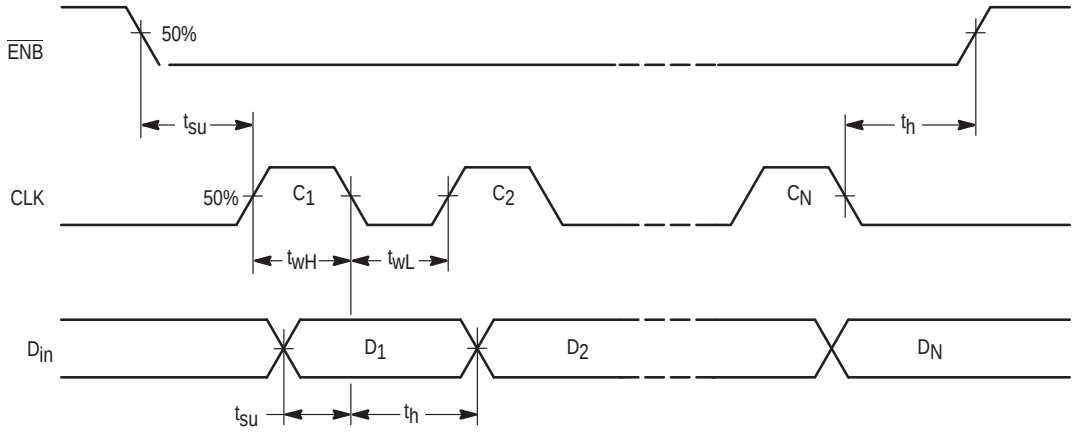


Figure 3. Serial Input, Positive Clock

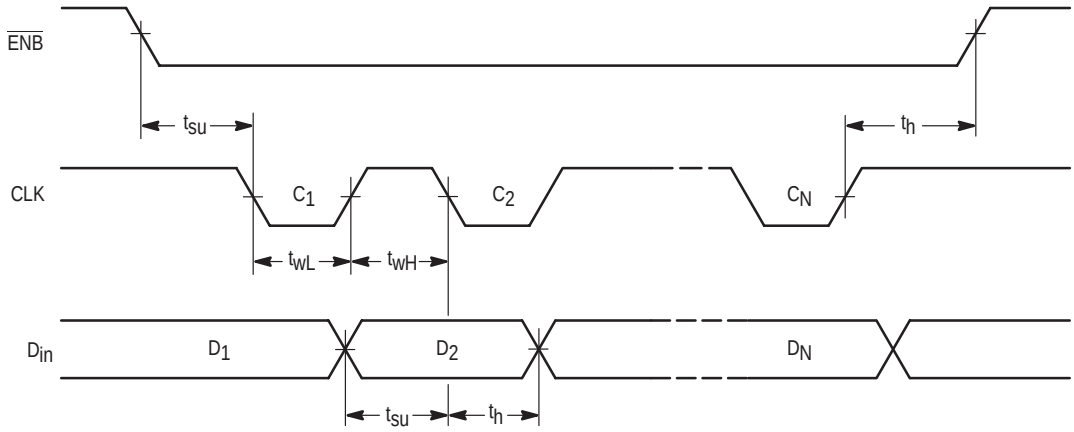


Figure 4. Serial Input, Negative Clock

PIN DESCRIPTIONS

INPUTS

D_{in}
Data Input

Six–bit words are entered serially, MSB first, into digital data input, D_{in}. Six words are loaded into the MC144110 during each D/A cycle; four words are loaded into the MC144111.

The last 6–bit word shifted in determines the output level of pins Q1 Out and R1 Out. The next–to–last 6–bit word affects pins Q2 Out and R2 Out, etc.

$\overline{ENB}$
Negative Logic Enable

The $\overline{ENB}$ pin must be low (active) during the serial load. On the low–to–high transition of $\overline{ENB}$, data contained in the shift register is loaded into the latch.

CLK
Shift Register Clock

Data is shifted into the register on the high–to–low transition of CLK. CLK is fed into the D–input of a transparent latch, which is used for inhibiting the clocking of the shift register when $\overline{ENB}$ is high.

The number of clock cycles required for the MC144110 is usually 36. The MC144111 usually uses 24 cycles. See Table 1 for additional information.

OUTPUTS

D_{out}
Data Output

The digital data output is primarily used for cascading the DACs and may be fed into D_{in} of the next stage.

R1 Out through Rn Out
Resistor Network Outputs

These are the R–2R resistor network outputs. These outputs may be fed to high–impedance input FET op amps to bypass the on–chip bipolar transistors. The R value of the resistor network ranges from 7 to 15 kΩ.

Q1 Out through Qn Out
NPN Transistor Outputs

Buffered DAC outputs utilize an emitter–follower configuration for current–gain, thereby allowing interface to low–impedance circuits.

SUPPLY PINS

V_{SS}
Negative Supply Voltage

This pin is usually ground.

V_{DD}
Positive Supply Voltage

The voltage applied to this pin is used to scale the analog output swing from 4.5 to 15 V p–p.

Table 1. Number of Channels vs Clocks Required

Number of Channels Required	Number of Clock Cycles	Outputs Used on MC144110	Outputs Used on MC144111
1	6	Q1/R1	Q1/R1
2	12	Q1/R1, Q2/R2	Q1/R1, Q2/R2
3	18	Q1/R1, Q2/R2, Q3/R3	Q1/R1, Q2/R2, Q3/R3
4	24	Q1/R1, Q2/R2, Q3/R3, Q4/R4	Q1/R1, Q2/R2, Q3/R3, Q4/R4
5	30	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5	Not Applicable
6	36	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5, Q6/R6	Not Applicable

Encoder and Decoder Pairs
CMOS

MC145026
MC145027
MC145028

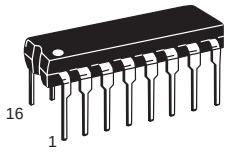
These devices are designed to be used as encoder/decoder pairs in remote control applications.

The MC145026 encodes nine lines of information and serially sends this information upon receipt of a transmit enable ($\overline{TE}$) signal. The nine lines may be encoded with trinary data (low, high, or open) or binary data (low or high). The words are transmitted twice per encoding sequence to increase security.

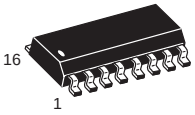
The MC145027 decoder receives the serial stream and interprets five of the trinary digits as an address code. Thus, 243 addresses are possible. If binary data is used at the encoder, 32 addresses are possible. The remaining serial information is interpreted as four bits of binary data. The valid transmission (VT) output goes high on the MC145027 when two conditions are met. First, two addresses must be consecutively received (in one encoding sequence) which both match the local address. Second, the 4 bits of data must match the last valid data received. The active VT indicates that the information at the Data output pins has been updated.

The MC145028 decoder treats all nine trinary digits as an address which allows 19,683 codes. If binary data is encoded, 512 codes are possible. The VT output goes high on the MC145028 when two addresses are consecutively received (in one encoding sequence) which both match the local address.

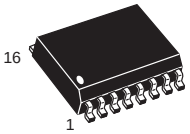
- Operating Temperature Range: – 40 to + 85°C
- Very–Low Standby Current for the Encoder: 300 nA Maximum @ 25°C
- Interfaces with RF, Ultrasonic, or Infrared Modulators and Demodulators
- RC Oscillator, No Crystal Required
- High External Component Tolerance; Can Use ± 5% Components
- Internal Power–On Reset Forces All Decoder Outputs Low
- Operating Voltage Range: MC145026 = 2.5 to 18 V*
  MC145027, MC145028 = 4.5 to 18 V
- For Infrared Applications, See Application Note AN1016/D



P SUFFIX
PLASTIC DIP
CASE 648



D SUFFIX
SOG PACKAGE
CASE 751B



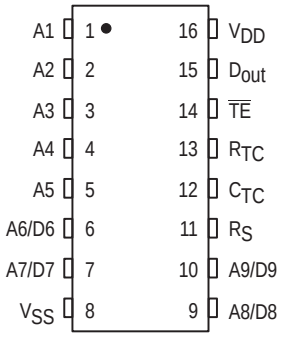
DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

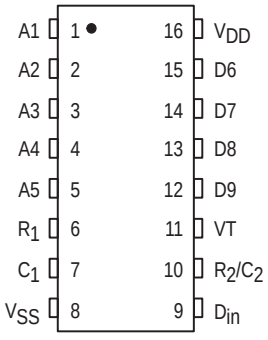
MC145026P	Plastic DIP
MC145026D	SOG Package
MC145027P	Plastic DIP
MC145027DW	SOG Package
MC145028P	Plastic DIP
MC145028DW	SOG Package

PIN ASSIGNMENTS

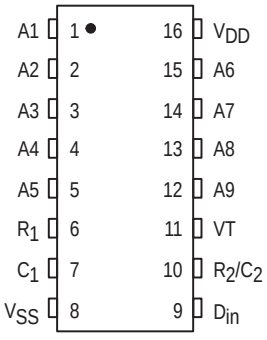
MC145026
ENCODER



MC145027
DECODERS



MC145028
DECODERS



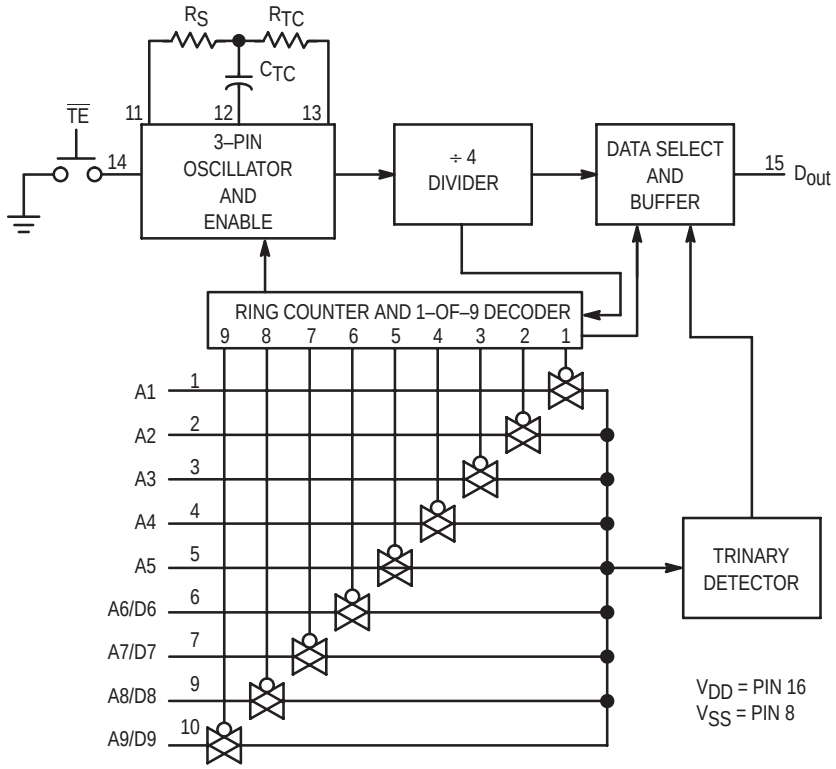


Figure 1. MC145026 Encoder Block Diagram

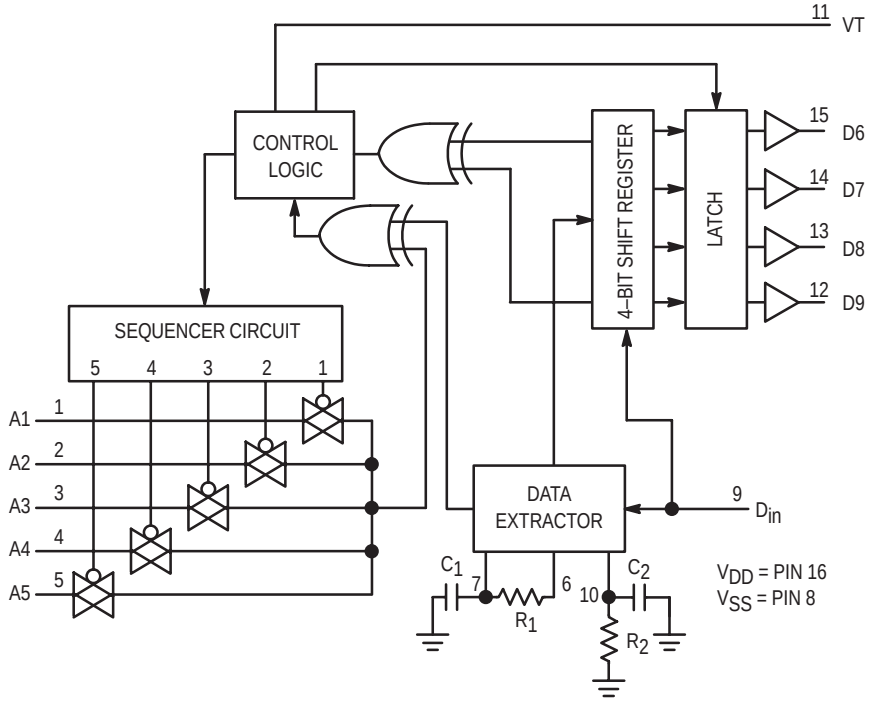


Figure 2. MC145027 Decoder Block Diagram

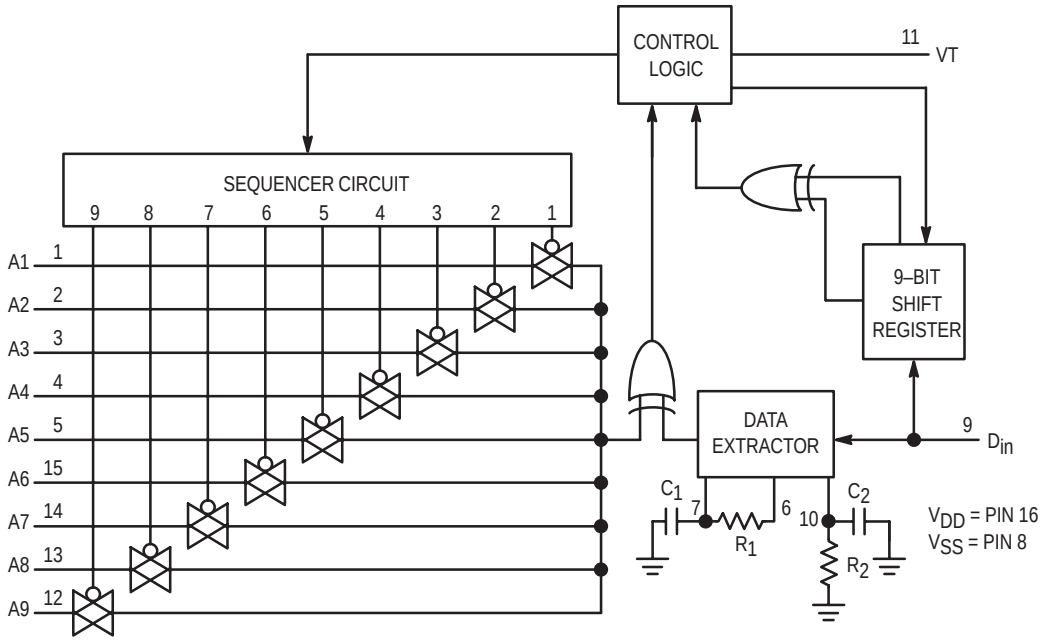


Figure 3. MC145028 Decoder Block Diagram

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
V_{DD}	DC Supply Voltage (except SC41343, SC41344)	– 0.5 to + 18	V
V_{DD}	DC Supply Voltage (SC41343, SC41344 only)	– 0.5 to + 10	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 10	mA
P_D	Power Dissipation, per Package	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS — MC145026*, MC145027, and MC145028 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			– 40°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low–Level Output Voltage (V_{in} = V_{DD} or 0)	5.0	—	0.05	—	0.05	—	0.05	V
		10	—	0.05	—	0.05	—	0.05	
		15	—	0.05	—	0.05	—	0.05	
V_{OH}	High–Level Output Voltage (V_{in} = 0 or V_{DD})	5.0	4.95	—	4.95	—	4.95	—	V
		10	9.95	—	9.95	—	9.95	—	
		15	14.95	—	14.95	—	14.95	—	
V_{IL}	Low–Level Input Voltage								V
	(V_{out} = 4.5 or 0.5 V)	5.0	—	1.5	—	1.5	—	1.5	
	(V_{out} = 9.0 or 1.0 V)	10	—	3.0	—	3.0	—	3.0	
	(V_{out} = 13.5 or 1.5 V)	15	—	4.0	—	4.0	—	4.0	
V_{IH}	High–Level Input Voltage								V
	(V_{out} = 0.5 or 4.5 V)	5.0	3.5	—	3.5	—	3.5	—	
	(V_{out} = 1.0 or 9.0 V)	10	7.0	—	7.0	—	7.0	—	
	(V_{out} = 1.5 or 13.5 V)	15	11	—	11	—	11	—	
I_{OH}	High–Level Output Current								mA
	(V_{out} = 2.5 V)	5.0	– 2.5	—	– 2.1	—	– 1.7	—	
	(V_{out} = 4.6 V)	5.0	– 0.52	—	– 0.44	—	– 0.36	—	
	(V_{out} = 9.5 V)	10	– 1.3	—	– 1.1	—	– 0.9	—	
	(V_{out} = 13.5 V)	15	– 3.6	—	– 3.0	—	– 2.4	—	
I_{OL}	Low–Level Output Current								mA
	(V_{out} = 0.4 V)	5.0	0.52	—	0.44	—	0.36	—	
	(V_{out} = 0.5 V)	10	1.3	—	1.1	—	0.9	—	
	(V_{out} = 1.5 V)	15	3.6	—	3.0	—	2.4	—	
I_{in}	Input Current — $\overline{TE}$	5.0	—	—	3.0	11	—	—	µA
	(MC145026, Pull–Up Device)	10	—	—	16	60	—	—	
		15	—	—	35	120	—	—	
I_{in}	Input Current	15	—	± 0.3	—	± 0.3	—	± 1.0	µA
	R_S (MC145026), D_{in} (MC145027, MC145028)								
I_{in}	Input Current								µA
	A1 – A5, A6/D6 – A9/D9 (MC145026),	5.0	—	—	—	± 110	—	—	
	A1 – A5 (MC145027),	10	—	—	—	± 500	—	—	
	A1 – A9 (MC145028)	15	—	—	—	± 1000	—	—	
C_{in}	Input Capacitance (V_{in} = 0)	—	—	—	—	7.5	—	—	pF
I_{DD}	Quiescent Current — MC145026	5.0	—	—	—	0.1	—	—	µA
		10	—	—	—	0.2	—	—	
		15	—	—	—	0.3	—	—	
I_{DD}	Quiescent Current — MC145027, MC145028	5.0	—	—	—	50	—	—	µA
		10	—	—	—	100	—	—	
		15	—	—	—	150	—	—	
I_{dd}	Dynamic Supply Current — MC145026	5.0	—	—	—	200	—	—	µA
	(f_c = 20 kHz)	10	—	—	—	400	—	—	
		15	—	—	—	600	—	—	
I_{dd}	Dynamic Supply Current — MC145027, MC145028	5.0	—	—	—	400	—	—	µA
	(f_c = 20 kHz)	10	—	—	—	800	—	—	
		15	—	—	—	1200	—	—	

* Also see next Electrical Characteristics table for 2.5 V specifications.

ELECTRICAL CHARACTERISTICS — MC145026 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			– 40°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low–Level Output Voltage (V_{in} = 0 V or V_{DD})	2.5	—	0.05	—	0.05	—	0.05	V
V_{OH}	High–Level Output Voltage (V_{in} = 0 V or V_{DD})	2.5	2.45	—	2.45	—	2.45	—	V
V_{IL}	Low–Level Input Voltage (V_{out} = 0.5 V or 2.0 V)	2.5	—	0.3	—	0.3	—	0.3	V
V_{IH}	High–Level Input Voltage (V_{out} = 0.5 V or 2.0 V)	2.5	2.2	—	2.2	—	2.2	—	V
I_{OH}	High–Level Output Current (V_{out} = 1.25 V)	2.5	0.28	—	0.25	—	0.2	—	mA
I_{OL}	Low–Level Output Current (V_{out} = 0.4 V)	2.5	0.22	—	0.2	—	0.16	—	mA
I_{in}	Input Current ($\overline{TE}$ — Pull–Up Device)	2.5	—	—	0.09	1.8	—	—	µA
I_{in}	Input Current (A1–A5, A6/D6–A9/D9)	2.5	—	—	—	± 25	—	—	µA
I_{DD}	Quiescent Current	2.5	—	—	—	0.05	—	—	µA
I_{dd}	Dynamic Supply Current (f_c = 20 kHz)	2.5	—	—	—	40	—	—	µA

SWITCHING CHARACTERISTICS — MC145026*, MC145027, and MC145028 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure No.	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}, t_{THL}	Output Transition Time	4,8	5.0 10 15	— — —	200 100 80	ns
t_r	D_{in} Rise Time — Decoders	5	5.0 10 15	— — —	15 15 15	µs
t_f	D_{in} Fall Time — Decoders	5	5.0 10 15	— — —	15 5.0 4.0	µs
f_{osc}	Encoder Clock Frequency	6	5.0 10 15	0.001 0.001 0.001	2.0 5.0 10	MHz
f	Decoder Frequency — Referenced to Encoder Clock	12	5.0 10 15	1.0 1.0 1.0	240 410 450	kHz
t_w	$\overline{TE}$ Pulse Width — Encoders	7	5.0 10 15	65 30 20	— — —	ns

* Also see next Switching Characteristics table for 2.5 V specifications.

SWITCHING CHARACTERISTICS — MC145026 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure No.	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}, t_{THL}	Output Transition Time	4, 8	2.5	—	450	ns
f_{osc}	Encoder Clock Frequency	6	2.5	1.0	250	kHz
t_w	$\overline{TE}$ Pulse Width	7	2.5	1.5	—	µs

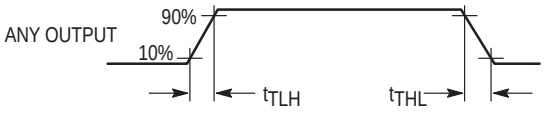


Figure 4.

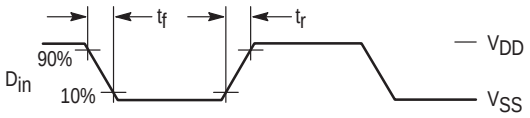


Figure 5.

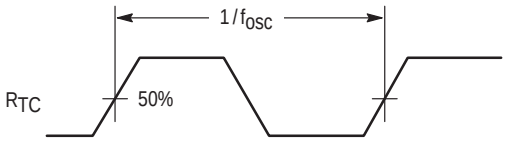


Figure 6.

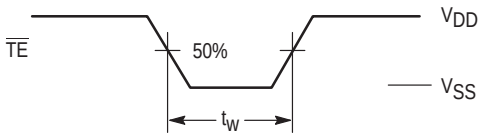
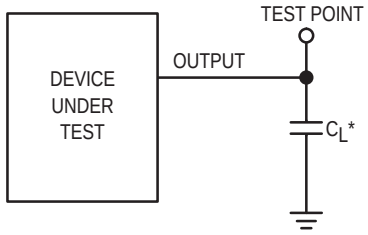


Figure 7.



* Includes all probe and fixture capacitance.

Figure 8. Test Circuit

OPERATING CHARACTERISTICS

MC145026

The encoder serially transmits trinary data as defined by the state of the A1 – A5 and A6/D6 – A9/D9 input pins. These pins may be in either of three states (low, high, or open) allowing 19,683 possible codes. The transmit sequence is initiated by a low level on the $\overline{TE}$ input pin. Upon power–up, the MC145026 can continuously transmit as long as $\overline{TE}$ remains low (also, the device can transmit two–word sequences by pulsing $\overline{TE}$ low). However, no MC145026 application should be designed to rely upon the first data word transmitted immediately after power–up because this word may be invalid. Between the two data words, no signal is sent for three data periods (see Figure 10).

Each transmitted trinary digit is encoded into pulses (see Figure 11). A logic 0 (low) is encoded as two consecutive short pulses, a logic 1 (high) as two consecutive long pulses, and an open (high impedance) as a long pulse followed by a short pulse. The input state is determined by using a weak "output" device to try to force each input high then low. If only a high state results from the two tests, the input is assumed to be hardwired to V_{DD}. If only a low state is obtained, the input is assumed to be hardwired to V_{SS}. If both a high and a low can be forced at an input, an open is assumed and is encoded as such. The "high" and "low" levels are 70% and 30% of the supply voltage as shown in the Electrical Characteristics table. The weak "output" device sinks/sources up to 110 μA at a 5 V supply level, 500 μA at 10 V, and 1 mA at 15 V.

The $\overline{TE}$ input has an internal pull–up device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high and the second–word transmission has timed out, the encoder is completely disabled, the oscillator is inhibited, and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started and the transmit sequence begins. The inputs are then sequentially selected, and determinations are made as to the input logic states. This information is serially transmitted via the D_{out} pin.

MC145027

This decoder receives the serial data from the encoder and outputs the data, if it is valid. The transmitted data, consisting of two identical words, is examined bit by bit during reception. The first five trinary digits are assumed to be the address. If the received address matches the local address, the next four (data) bits are internally stored, but are not transferred to the output data latch. As the second encoded word is received, the address must again match. If a match occurs, the new data bits are checked against the previously stored data bits. If the two nibbles of data (four bits each) match, the data is transferred to the output data latch by VT and remains until new data replaces it. At the same time, the VT output pin is brought high and remains high until an error is received or until no input signal is received for four data periods (see Figure 10).

Although the address information may be encoded in trinary, the data information must be either a 1 or 0. A trinary (open) data line is decoded as a logic 1.

MC145028

This decoder operates in the same manner as the MC145027 except that nine address lines are used and no data output is available. The VT output is used to indicate that a valid address has been received. For transmission security, two identical transmitted words must be consecutively received before a VT output signal is issued.

The MC145028 allows 19,683 addresses when trinary levels are used. 512 addresses are possible when binary levels are used.

PIN DESCRIPTIONS

MC145026 ENCODER

A1 – A5, A6/D6 – A9/D9
Address, Address/Data Inputs (Pins 1 – 7, 9, and 10)

These address/data inputs are encoded and the data is sent serially from the encoder via the D_{out} pin.

R_S, C_{TC}, R_{TC}
(Pins 11, 12, and 13)

These pins are part of the oscillator section of the encoder (see Figure 9).

If an external signal source is used instead of the internal oscillator, it should be connected to the R_S input and the R_{TC} and C_{TC} pins should be left open.

$\overline{TE}$
Transmit Enable (Pin 14)

This active–low transmit enable input initiates transmission when forced low. An internal pull–up device keeps this input normally high. The pull–up current is specified in the Electrical Characteristics table.

D_{out}
Data Out (Pin 15)

This is the output of the encoder that serially presents the encoded data word.

V_{SS}
Negative Power Supply (Pin 8)

The most–negative supply potential. This pin is usually ground.

V_{DD}
Positive Power Supply (Pin 16)

The most–positive power supply pin.

MC145027 AND MC145028 DECODERS

A1 – A5, A1 – A9
Address Inputs (Pins 1 – 5) — MC145027,
Address Inputs (Pins 1 – 5, 15, 14, 13, 12) — MC145028

These are the local address inputs. The states of these pins must match the appropriate encoder inputs for the VT pin to go high. The local address may be encoded with trinary or binary data.

D6 – D9
Data Outputs (Pins 15, 14, 13, 12) — MC145027 Only

These outputs present the binary information that is on encoder inputs A6/D6 through A9/D9. Only binary data is

acknowledged; a trinary open at the MC145026 encoder is decoded as a high level (logic 1).

D_{in}
Data In (Pin 9)

This pin is the serial data input to the decoder. The input voltage must be at CMOS logic levels. The signal source driving this pin must be dc coupled.

R_1, C_1
Resistor 1, Capacitor 1 (Pins 6, 7)

As shown in Figures 2 and 3, these pins accept a resistor and capacitor that are used to determine whether a narrow pulse or wide pulse has been received. The time constant R_1 x C_1 should be set to 1.72 encoder clock periods:

$$R_1 C_1 = 3.95 R_{TC} C_{TC}$$

R_2/C_2
Resistor 2/Capacitor 2 (Pin 10)

As shown in Figures 2 and 3, this pin accepts a resistor and capacitor that are used to detect both the end of a received word and the end of a transmission. The time constant R_2 x C_2 should be 33.5 encoder clock periods (four data periods per Figure 11): $R_2 C_2 = 77 R_{TC} C_{TC}$. This time constant is used to determine whether the D_{in} pin has remained low for four data periods (end of transmission). A separate on–chip comparator looks at the voltage–equivalent two data periods ($0.4 R_2 C_2$) to detect the dead time between received words within a transmission.

VT
Valid Transmission Output (Pin 11)

This valid transmission output goes high after the second word of an encoding sequence when the following conditions are satisfied:

1. the received addresses of both words match the local decoder address, and
2. the received data bits of both words match.

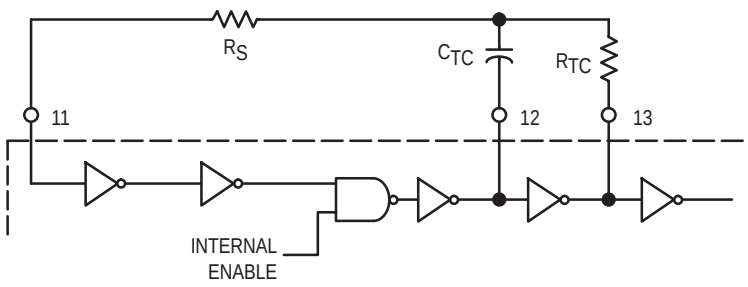
VT remains high until either a mismatch is received or no input signal is received for four data periods.

V_{SS}
Negative Power Supply (Pin 8)

The most–negative supply potential. This pin is usually ground.

V_{DD}
Positive Power Supply (Pin 16)

The most–positive power supply pin.



This oscillator operates at a frequency determined by the external RC network; i.e.,

$$f \approx \frac{1}{2.3\ R_{TC}\ C_{TC}'} \quad \text{(Hz)}$$

for 1 kHz ≤ f ≤ 400 kHz

where: $C_{TC}' = C_{TC} + C_{layout} + 12$ pF

$R_S \approx 2\ R_{TC}$

$R_S \geq 20$ k

$R_{TC} \geq 10$ k

400 pF < C_{TC} < 15 µF

The value for R_S should be chosen to be ≥ 2 times R_{TC}. This range ensures that current through R_S is insignificant compared to current through R_{TC}. The upper limit for R_S must ensure that R_S x 5 pF (input capacitance) is small compared to R_{TC} x C_{TC}.

For frequencies outside the indicated range, the formula is less accurate. The minimum recommended oscillation frequency of this circuit is 1 kHz. Susceptibility to externally induced noise signals may occur for frequencies below 1 kHz and/or when resistors utilized are greater than 1 MΩ.

Figure 9. Encoder Oscillator Information

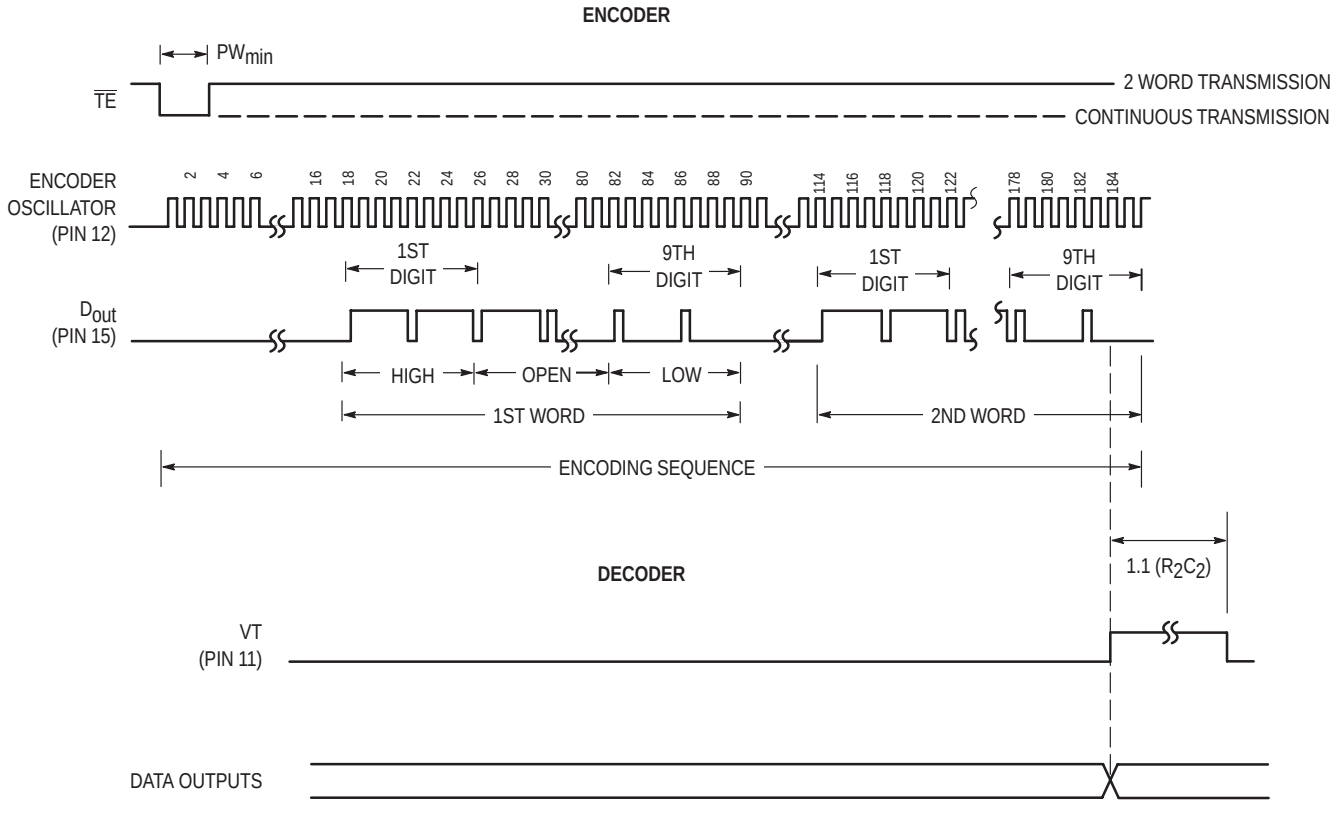


Figure 10. Timing Diagram

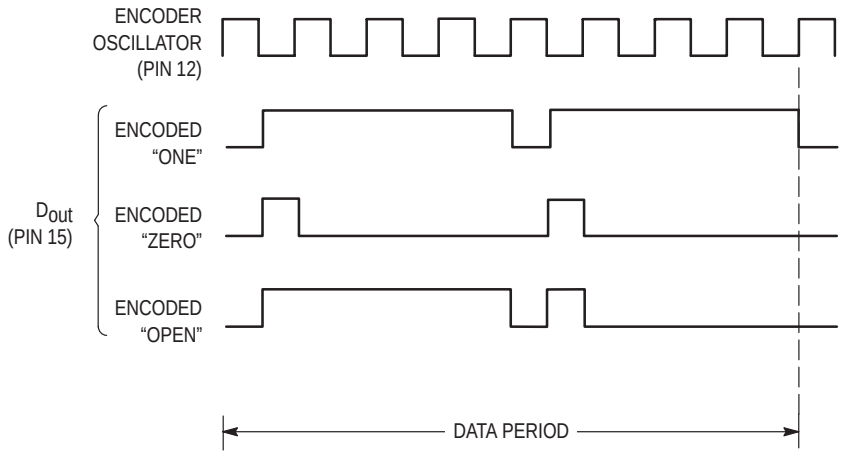


Figure 11. Encoder Data Waveforms

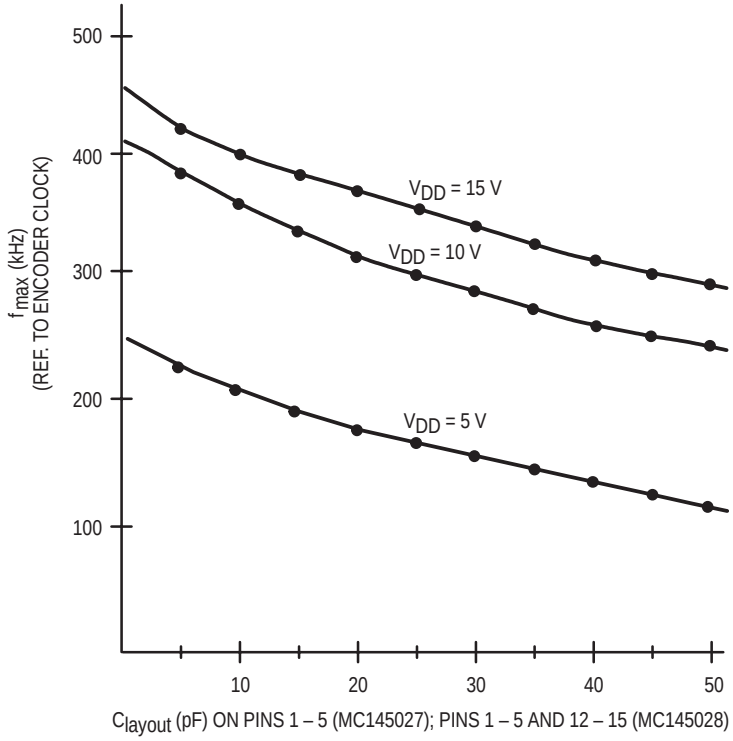


Figure 12. f_{max} vs C_{layout} — Decoders Only

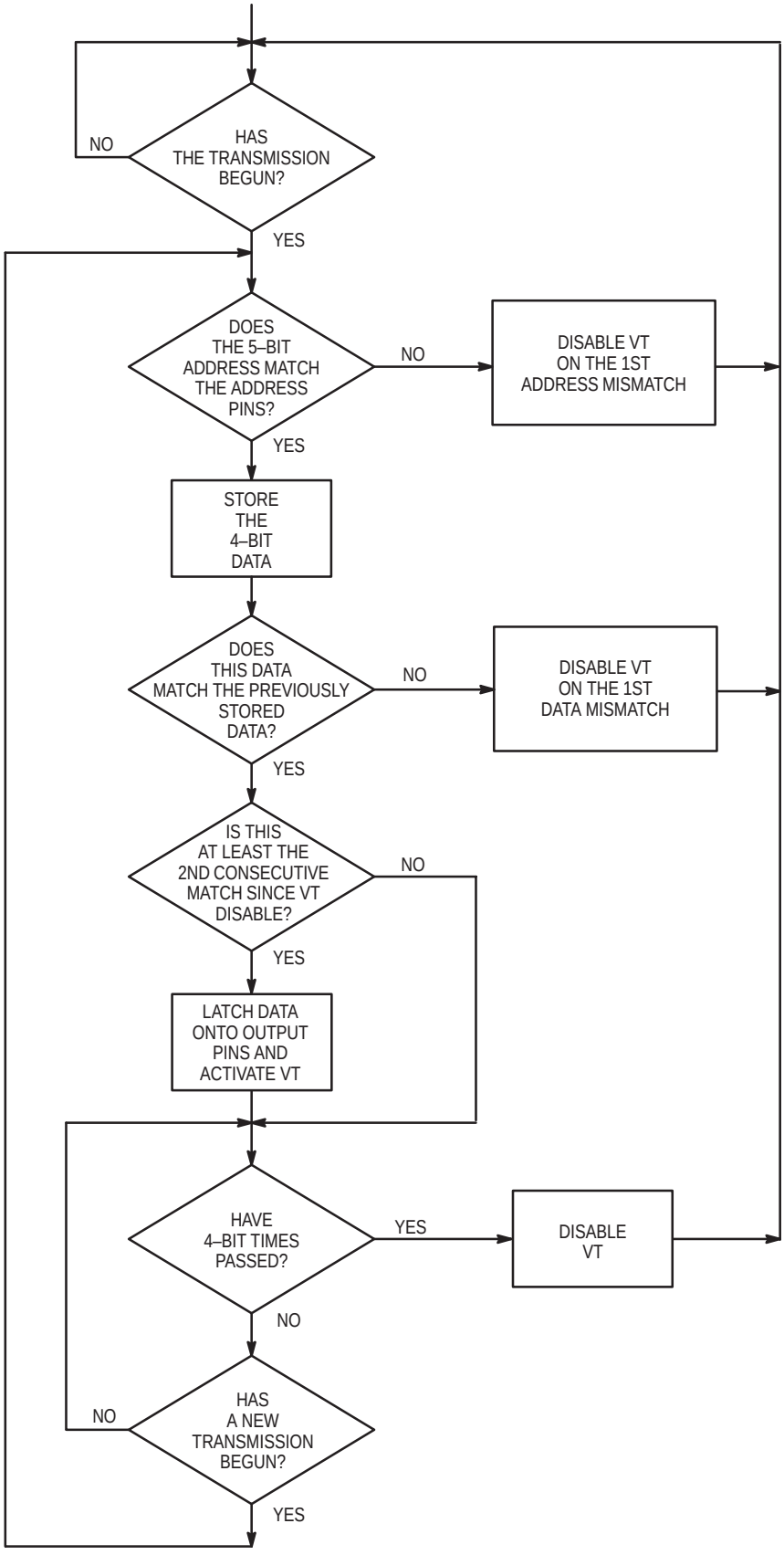


Figure 13. MC145027 Flowchart

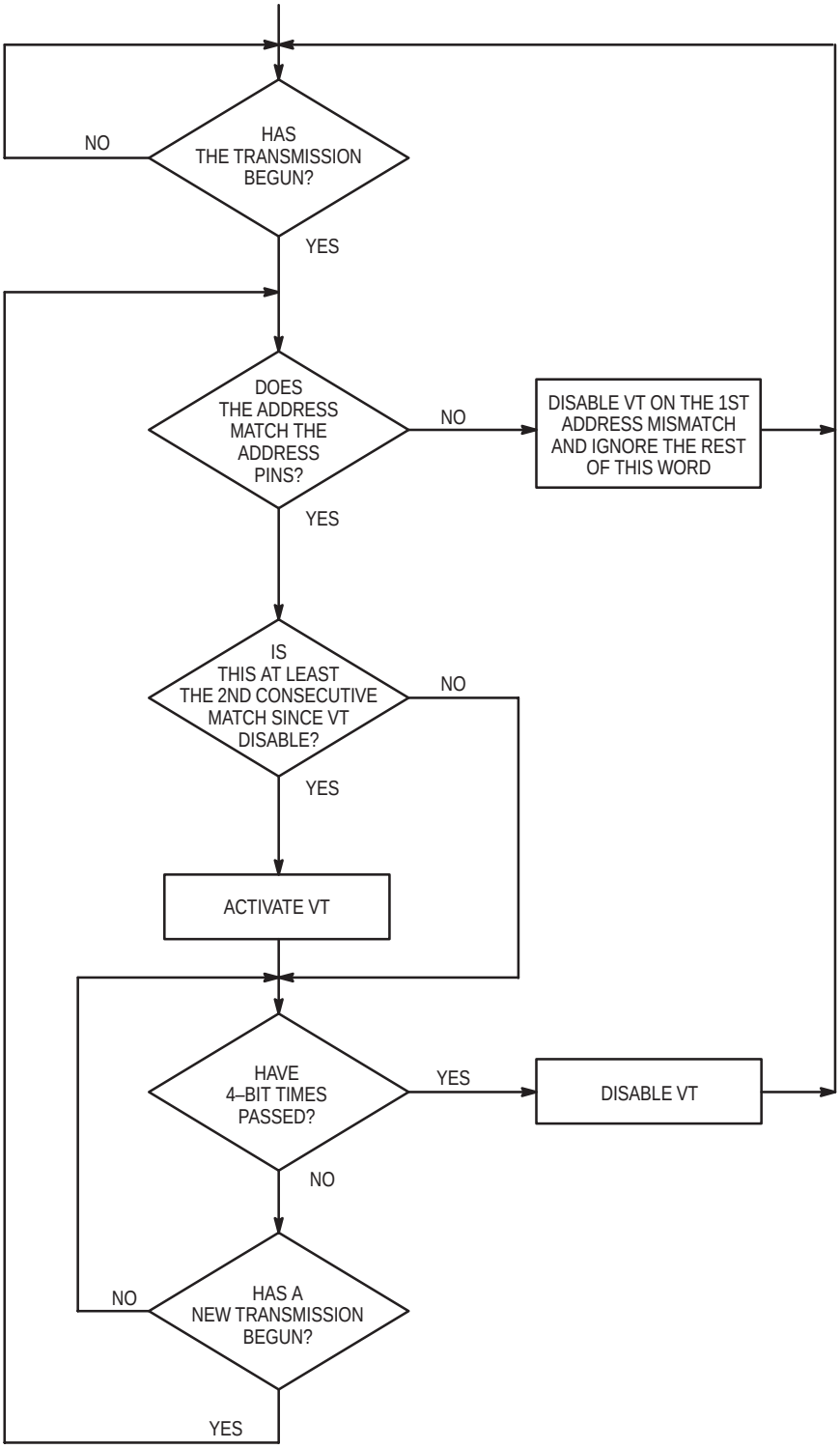


Figure 14. MC145028 Flowchart

MC145027 AND MC145028 TIMING

To verify the MC145027 or MC145028 timing, check the waveforms on C1 (Pin 7) and R2/C2 (Pin 10) as compared to the incoming data waveform on D_{in} (Pin 9).

The R–C decay seen on C1 discharges down to 1/3 V_{DD} before being reset to V_{DD}. This point of reset (labelled “DOS” in Figure 15) is the point in time where the decision is made whether the data seen on D_{in} is a 1 or 0. DOS should not be too close to the D_{in} data edges or intermittent operation may occur.

The other timing to be checked on the MC145027 and MC145028 is on R2/C2 (see Figure 16). The R–C decay is continually reset to V_{DD} as data is being transmitted. Only between words and after the end–of–transmission (EOT) does R2/C2 decay significantly from V_{DD}. R2/C2 can be used to identify the internal end–of–word (EOW) timing edge which is generated when R2/C2 decays to 2/3 V_{DD}. The internal EOT timing edge occurs when R2/C2 decays to 1/3 V_{DD}. When the waveform is being observed, the R–C decay should go down between the 2/3 and 1/3 V_{DD} levels, but not too close to either level before data transmission on D_{in} resumes.

Verification of the timing described above should ensure a good match between the MC145026 transmitter and the MC145027 and MC145028 receivers.

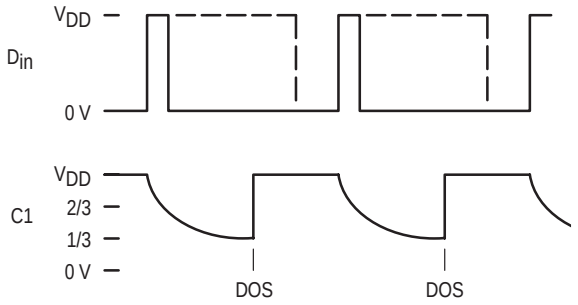


Figure 15. R–C Decay on Pin 7 (C1)

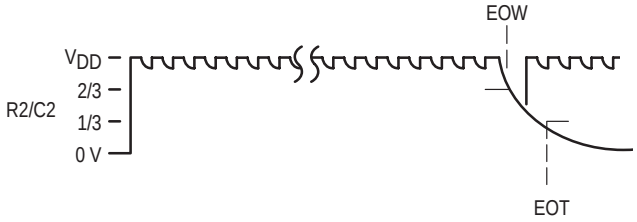
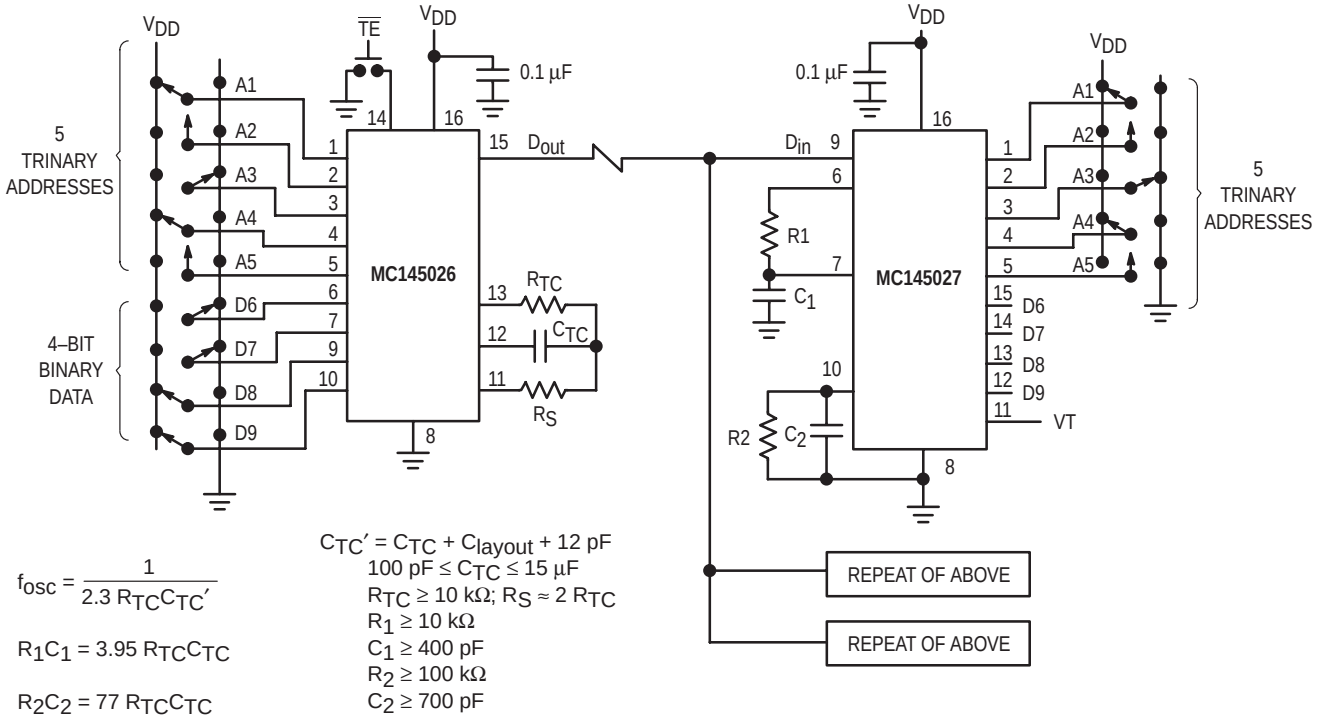


Figure 16. R–C Decay on Pin 10 (R2/C2)



$$f_{osc} = \frac{1}{2.3\ R_{TC}C_{TC}'}$$

$R_1C_1 = 3.95\ R_{TC}C_{TC}$

$R_2C_2 = 77\ R_{TC}C_{TC}$

$C_{TC}' = C_{TC} + C_{layout} + 12$ pF

$100\ pF \le C_{TC} \le 15\ \mu F$

$R_{TC} \ge 10\ k\Omega$; $R_S \approx 2\ R_{TC}$

$R_1 \ge 10\ k\Omega$

$C_1 \ge 400$ pF

$R_2 \ge 100\ k\Omega$

$C_2 \ge 700$ pF

Example R/C Values (All Resistors and Capacitors are ± 5%)

($C_{TC}' = C_{TC}$ + 20 pF)

f_{osc} (kHz)	R_{TC}	$C_{TC'}$	R_S	R_1	C_1	R_2	C_2
362	10 k	120 pF	20 k	10 k	470 pF	100 k	910 pF
181	10 k	240 pF	20 k	10 k	910 pF	100 k	1800 pF
88.7	10 k	490 pF	20 k	10 k	2000 pF	100 k	3900 pF
42.6	10 k	1020 pF	20 k	10 k	3900 pF	100 k	7500 pF
21.5	10 k	2020 pF	20 k	10 k	8200 pF	100 k	0.015 µF
8.53	10 k	5100 pF	20 k	10 k	0.02 µF	200 k	0.02 µF
1.71	50 k	5100 pF	100 k	50 k	0.02 µF	200 k	0.1 µF

Figure 17. Typical Application

APPLICATIONS INFORMATION

INFRARED TRANSMITTER

In Figure 18, the MC145026 encoder is set to run at an oscillator frequency of about 4 to 9 kHz. Thus, the time required for a complete two–word encoding sequence is about 20 to 40 ms. The data output from the encoder gates an RC oscillator running at 50 kHz; the oscillator shown starts rapidly enough to be used in this application. When the “send” button is not depressed, both the MC145026 and oscillator are in a low–power standby state. The RC oscillator has to be trimmed for 50 kHz and has some drawbacks for frequency stability. A superior system uses a ceramic resonator oscillator running at 400 kHz. This oscillator feeds a divider as shown in Figure 19. The unused inputs of the MC14011UB must be grounded.

The MLED81 IRED is driven with the 50 kHz square wave at about 200 to 300 mA to generate the carrier. If desired, two IREDs wired in series can be used (see Application Note AN1016 for more information). The bipolar IRED switch, shown in Figure 18, offers two advantages over a FET. First, a logic FET has too much gate capacitance for the MC14011UB to drive without waveform distortion. Second, the bipolar drive permits lower supply voltages, which are an advantage in portable battery–powered applications.

The configuration shown in Figure 18 operates over a supply range of 4.5 to 18 V. A low–voltage system which operates down to 2.5 V could be realized if the oscillator section of a MC74HC4060 is used in place of the MC14011UB. The data output of the MC145026 is inverted and fed to the RESET pin of the MC74HC4060. Alternately, the MC74HCU04 could be used for the oscillator.

Information on the MC14011UB is in book number DL131/D. The MC74HCU04 and MC74HC4060 are found in book number DL129/D.

INFRARED RECEIVER

The receiver in Figure 20 couples an IR–sensitive diode to input preamp A1, followed by band–pass amplifier A2 with a gain of about 10. Limiting stage A3 follows, with an output of about 800 mV p–p. The limited 50 kHz burst is detected by comparator A4 that passes only positive pulses, and peak–detected and filtered by a diode/RC network to extract the data envelope from the burst. Comparator A5 boosts the signal to logic levels compatible with the MC145027/28 data input. The D_{in} pin of these decoders is a standard CMOS high–impedance input which must ***not*** be allowed to float. Therefore, direct coupling from A5 to the decoder input is utilized.

Shielding should be used on at least A1 and A2, with good ground and high–sensitivity circuit layout techniques applied.

For operation with supplies higher than + 5 V, limiter A4’s positive output swing needs to be limited to 3 to 5 V. This is accomplished via adding a zener diode in the negative feedback path, thus avoiding excessive system noise. The biasing resistor stack should be adjusted such that V3 is 1.25 to 1.5 V.

This system works up to a range of about 10 meters. The gains of the system may be adjusted to suit the individual design needs. The 100 Ω resistor in the emitter of the first 2N5088 and the 1 kΩ resistor feeding A2 may be altered if different gain is required. In general, more gain does not necessarily result in increased range. This is due to noise floor limitations. The designer should increase transmitter power and/or increase receiver aperature with Fresnal lensing to greatly improve range. See Application Note AN1016 for additional information.

Information on the MC34074 is in data book DL128/D.

TRINARY SWITCH MANUFACTURERS

Midland Ross–Electronic Connector Div.
Greyhill
Augat/Alcoswitch
Aries Electronics

The above companies may not have the switches in a DIP. For more information, call them or consult *eem Electronic Engineers Master Catalog* or the *Gold Book*. ***Ask for SPDT with center OFF***.

Alternative: An SPST can be placed in series between a SPDT and the Encoder or Decoder to achieve trinary action.

Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of trinary switch manufacturers.

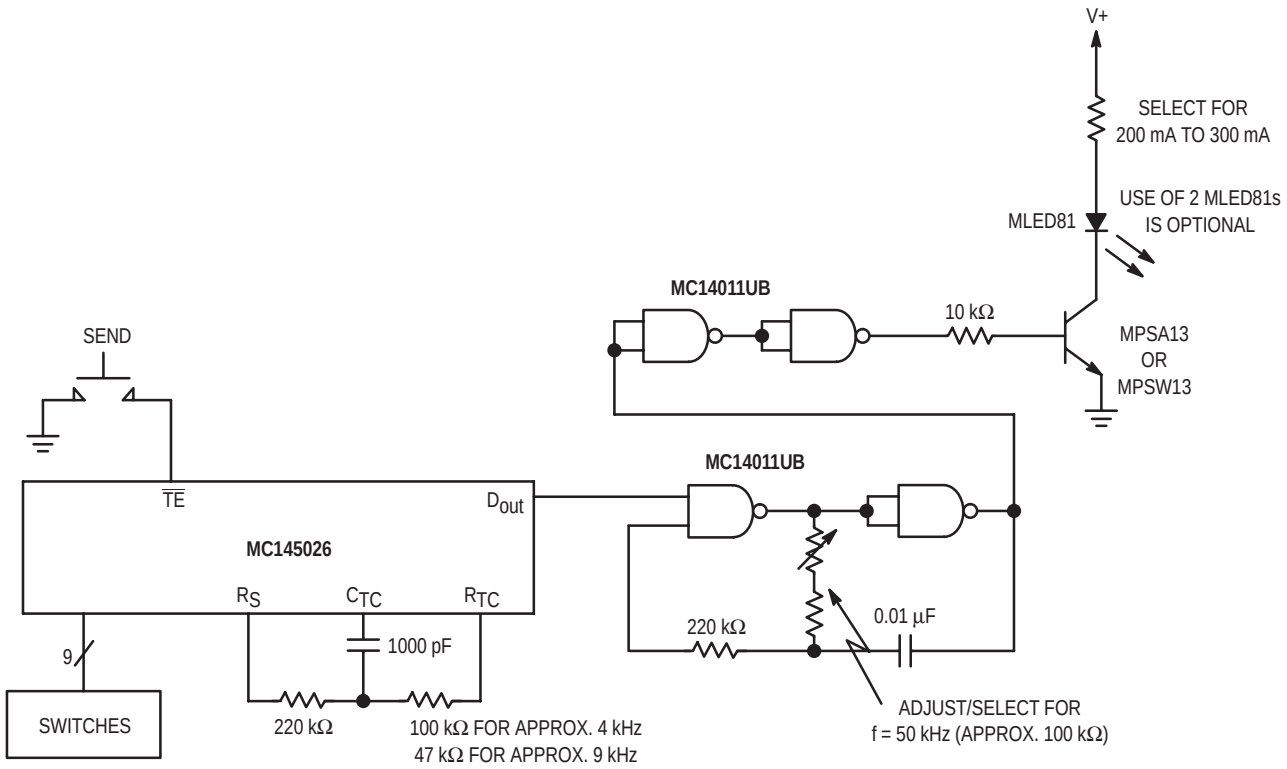


Figure 18. IRED Transmitter Using RC Oscillator to Generate Carrier Frequency

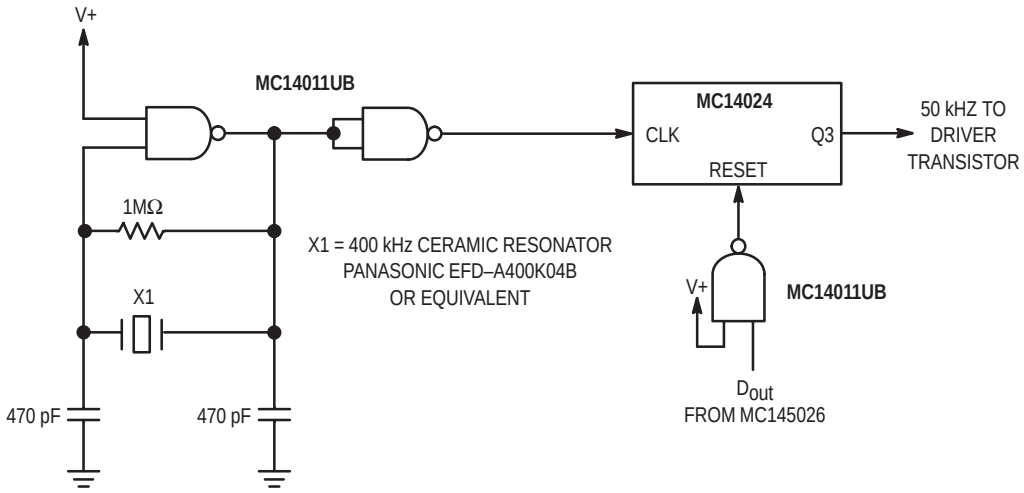


Figure 19. Using a Ceramic Resonator to Generate Carrier Frequency

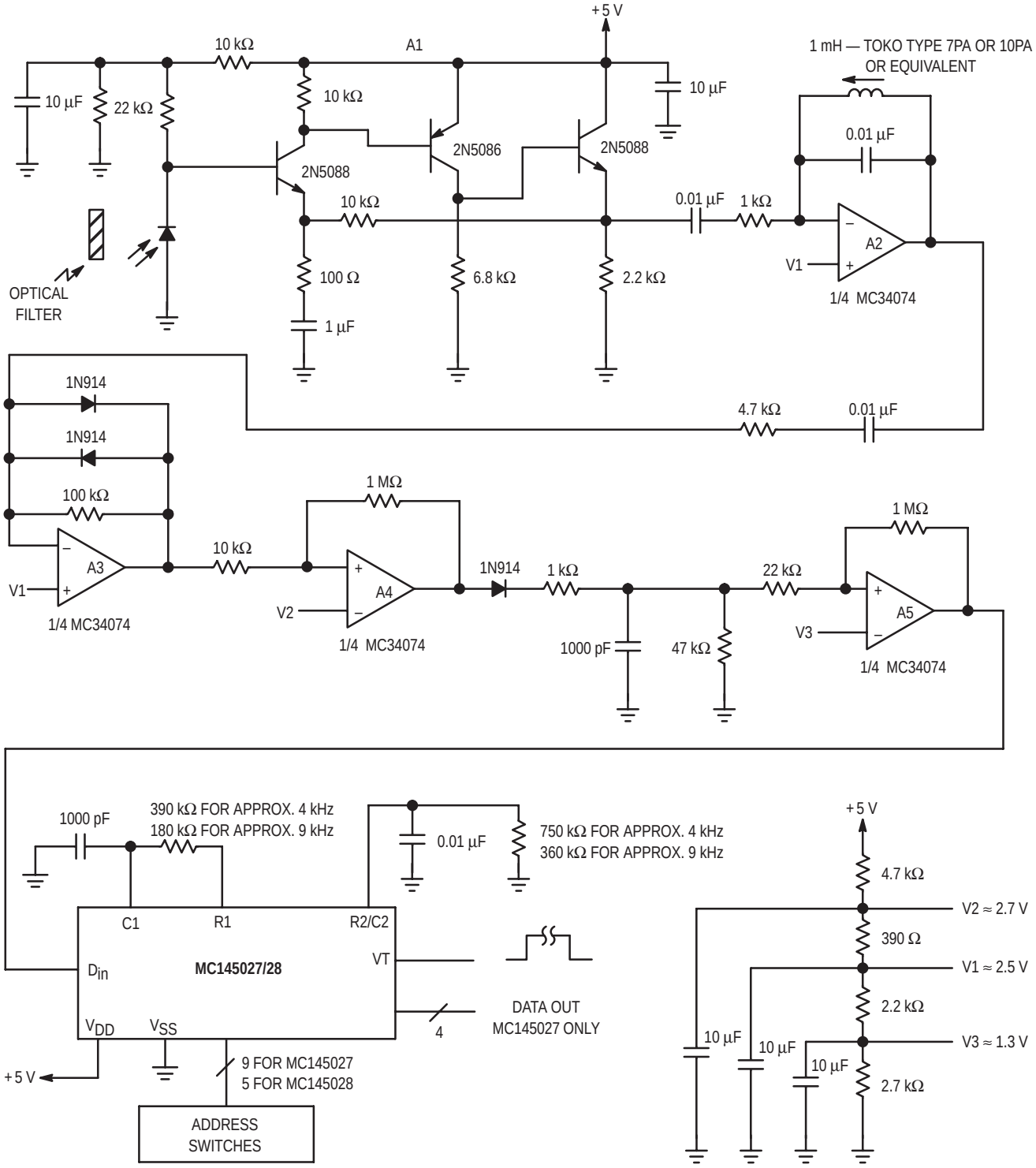


Figure 20. Infrared Receiver

MC145050
MC145051

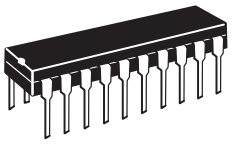
10-Bit A/D Converter with Serial Interface

CMOS

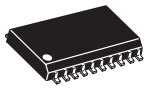
These ratiometric 10-bit ADCs have serial interface ports to provide communication with MCUs and MPUs. *Either a 10- or 16-bit format can be used*. The 16-bit format can be one continuous 16-bit stream or two intermittent 8-bit streams. The converters operate from a single power supply with no external trimming required. Reference voltages down to 4.0 V are accommodated.

The MC145050 has the same pin out as the 8-bit MC145040 which allows an external clock (ADCLK) to operate the dynamic A/D conversion sequence. The MC145051 has the same pin out as the 8-bit MC145041 which has an internal clock oscillator and an end-of-conversion (EOC) output.

- 11 Analog Input Channels with Internal Sample-and-Hold
- Operating Temperature Range: – 40 to 125° C
- Successive Approximation Conversion Time:
  MC145050 — 21 μs (with 2.1 MHz ADCLK)
  MC145051 — 44 μs Maximum
- Maximum Sample Rate: MC145050 — 38 ks/s
  MC145051 — 20.4 ks/s
- Analog Input Range with 5-Volt Supply: 0 to 5 V
- Monotonic with No Missing Codes
- Direct Interface to Motorola SPI and National MICROWIRE Serial Data Ports
- Digital Inputs/Outputs are TTL, NMOS, and CMOS Compatible
- Low Power Consumption: 14 mW
- Chip Complexity: 1630 Elements (FETs, Capacitors, etc.)
- See Application Note AN1062 for Operation with QSPI



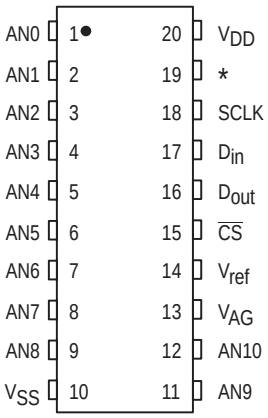
P SUFFIX
PLASTIC
CASE 738



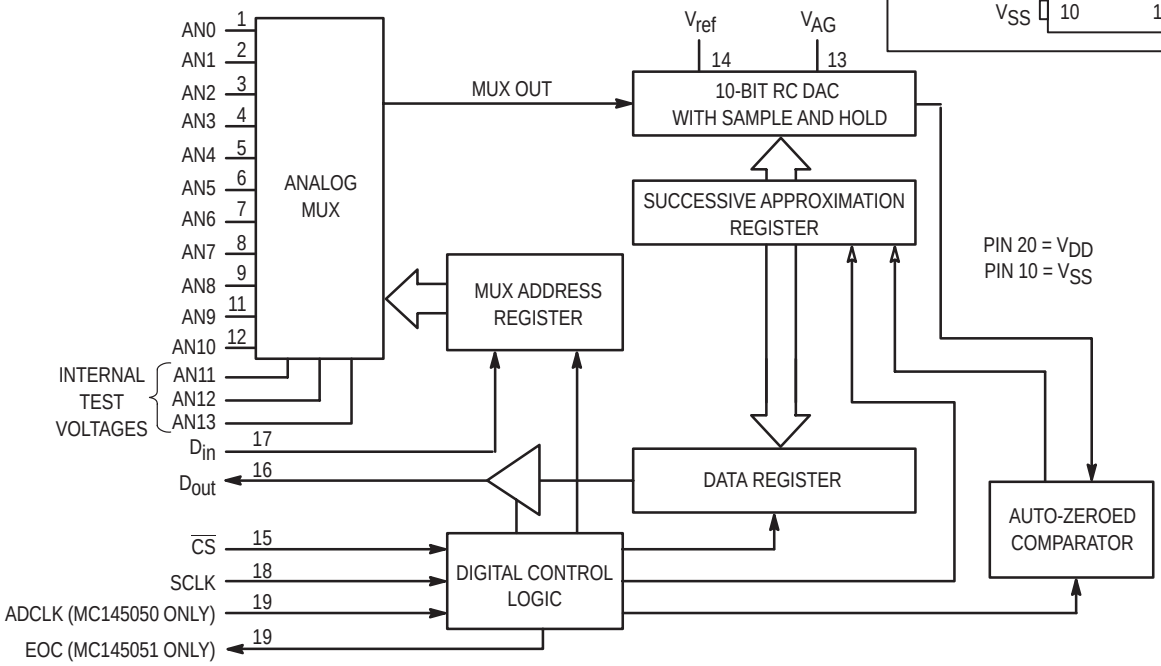
DW SUFFIX
SOG
CASE 751D

ORDERING INFORMATION

PIN ASSIGNMENT
*ADCLK (MC145050); EOC (MC145051)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	– 0.5 to + 6.0	V
V_{ref}	DC Reference Voltage	V_{AG} to V_{DD} + 0.1	V
V_{AG}	Analog Ground	V_{SS} – 0.1 to V_{ref}	V
V_{in}	DC Input Voltage, Any Analog or Digital Input	V_{SS} – 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	V_{SS} – 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{DD}, I_{SS}	DC Supply Current, V_{DD} and V_{SS} Pins	± 50	mA
T_{stg}	Storage Temperature	– 65 to 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges below..

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

OPERATION RANGES (Applicable to Guaranteed Limits)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage, Referenced to V_{SS}	4.5 to 5.5	V
V_{ref}	DC Reference Voltage	V_{AG} + 4.0 to V_{DD} + 0.1	V
V_{AG}	Analog Ground	V_{SS} – 0.1 to V_{ref} – 4.0	V
V_{AI}	Analog Input Voltage (See Note)	V_{AG} to V_{ref}	V
V_{in}, V_{out}	Digital Input Voltage, Output Voltage	V_{SS} to V_{DD}	V
T_A	Ambient Operating Temperature	– 40 to 125	°C

NOTE: Analog input voltages greater than V_{ref} convert to full scale. Input voltages less than V_{AG} convert to zero. See V_{ref} and V_{AG} pin descriptions.

DC ELECTRICAL CHARACTERISTICS

(Voltages Referenced to V_{SS}, Full Temperature and Voltage Ranges per Operation Ranges Table, unless otherwise indicated)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IH}	Minimum High-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$, ADCLK)		2.0	V
V_{IL}	Maximum Low-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$, ADCLK)		0.8	V
V_{OH}	Minimum High-Level Output Voltage (D_{out}, EOC)	I_{out} = – 1.6 mA I_{out} = – 20 µA	2.4 V_{DD} – 0.1	V
V_{OL}	Minimum Low-Level Output Voltage (D_{out}, EOC)	I_{out} = + 1.6 mA I_{out} = 20 µA	0.4 0.1	V
I_{in}	Maximum Input Leakage Current (D_{in}, SCLK, $\overline{CS}$, ADCLK)	$V_{in} = V_{SS}$ or V_{DD}	± 2.5	µA
I_{OZ}	Maximum Three-State Leakage Current (D_{out})	$V_{out} = V_{SS}$ or V_{DD}	± 10	µA
I_{DD}	Maximum Power Supply Current	$V_{in} = V_{SS}$ or V_{DD}, All Outputs Open	2.5	mA
I_{ref}	Maximum Static Analog Reference Current (V_{ref})	$V_{ref} = V_{DD}$, $V_{AG} = V_{SS}$	100	µA
I_{AI}	Maximum Analog Mux Input Leakage Current between all deselected inputs and any selected input (AN0 – AN10)	$V_{AI} = V_{SS}$ to V_{DD}	± 1	µA

A/D CONVERTER ELECTRICAL CHARACTERISTICS

(Full Temperature and Voltage Ranges per Operation Ranges Table; MC145050: 500 kHz ≤ ADCLK ≤ 2.1 MHz, unless otherwise noted)

Characteristic	Definition and Test Conditions	Guaranteed Limit	Unit
Resolution	Number of bits resolved by the A/D converter	10	Bits
Maximum Nonlinearity	Maximum difference between an ideal and an actual ADC transfer function	± 1	LSB
Maximum Zero Error	Difference between the maximum input voltage of an ideal and an actual ADC for zero output code	± 1	LSB
Maximum Full-Scale Error	Difference between the minimum input voltage of an ideal and an actual ADC for full-scale output code	± 1	LSB
Maximum Total Unadjusted Error	Maximum sum of nonlinearity, zero error, and full-scale error	± 1	LSB
Maximum Quantization Error	Uncertainty due to converter resolution	± 1/2	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	± 1-1/2	LSB
Maximum Conversion Time	Total time to perform a single analog-to-digital conversion MC145050 MC145051	44 44	ADCLK cycles µs
Data Transfer Time	Total time to transfer digital serial data into and out of the device	10 to 16	SCLK cycles
Sample Acquisition Time	Analog input acquisition time window	6	SCLK cycles
Minimum Total Cycle Time	Total time to transfer serial data, sample the analog input, and perform the conversion MC145050: ADCLK = 2.1 MHz, SCLK = 2.1 MHz MC145051: SCLK = 2.1 MHz	 26 49	µs
Maximum Sample Rate	Rate at which analog inputs may be sampled MC145050: ADCLK = 2.1 MHz, SCLK = 2.1 MHz MC145051: SCLK = 2.1 MHz	 38 20.4	ks/s

AC ELECTRICAL CHARACTERISTICS

(Full Temperature and Voltage Ranges per Operation Ranges Table)

Figure	Symbol	Parameter		Guaranteed Limit	Unit
1	f	Clock Frequency, SCLK Note: Refer to t_{wH}, t_{wL} below	(10-bit xfer) Min (11- to 16-bit xfer) Min (10- to 16-bit xfer) Max)	0 Note 1 2.1	MHz
1	f	Clock Frequency, ADCLK Note: Refer to t_{wH}, t_{wL} below	Minimum Maximum	500 2.1	kHz MHz
1	t_{wH}	Minimum Clock High Time	ADCLK SCLK	190 190	ns
1	t_{wL}	Minimum Clock Low Time	ADCLK SCLK	190 190	ns
1, 7	t_{PLH}, t_{PHL}	Maximum Propagation Delay, SCLK to D_{out}		125	ns
1, 7	t_h	Minimum Hold Time, SCLK to D_{out}		10	ns
2, 7	t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, $\overline{CS}$ to D_{out} High-Z		150	ns
2, 7	t_{PZL}, t_{PZH}	Maximum Propagation Delay, $\overline{CS}$ to D_{out} Driven	MC145050 MC145051	2 ADCLK cycles + 300 2.3	ns µs
3	t_{su}	Minimum Setup Time, D_{in} to SCLK		100	ns
3	t_h	Minimum Hold Time, SCLK to D_{in}		0	ns
4, 7, 8	t_d	Maximum Delay Time, EOC to D_{out} (MSB)	MC145051	100	ns
5	t_{su}	Minimum Setup Time, $\overline{CS}$ to SCLK	MC145050 MC145051	2 ADCLK cycles + 425 2.425	ns µs
—	t_{CSd}	Minimum Time Required Between 10th SCLK Falling Edge (≤ 0.8 V) and $\overline{CS}$ to Allow a Conversion	MC145050 MC145051	44 Note 2	ADCLK cycles
—	t_{CAs}	Maximum Delay Between 10th SCLK Falling Edge (≤ 2 V) and $\overline{CS}$ to Abort a Conversion	MC145050 MC145051	36 9	ADCLK cycles µs
5	t_h	Minimum Hold Time, Last SCLK to $\overline{CS}$		0	ns
6, 8	t_{PHL}	Maximum Propagation Delay, 10th SCLK to EOC	MC145051	2.35	µs
1	t_r, t_f	Maximum Input Rise and Fall Times	SCLK ADCLK D_{in}, $\overline{CS}$	1 250 10	ms ns µs
1, 4, 6 – 8	t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output		300	ns
—	C_{in}	Maximum Input Capacitance	AN0 – AN10 ADCLK, SCLK, $\overline{CS}$, D_{in}	55 15	pF
—	C_{out}	Maximum Three-State Output Capacitance	D_{out}	15	pF

NOTES:

1. After the 10th SCLK falling edge (≤ 2 V), at least 1 SCLK rising edge (≥ 2 V) must occur within 38 ADCLKs (MC145050) or 18.5 µs (MC145051).
2. On the MC145051, a $\overline{CS}$ edge may be received immediately after an active transition on the EOC pin.

SWITCHING WAVEFORMS

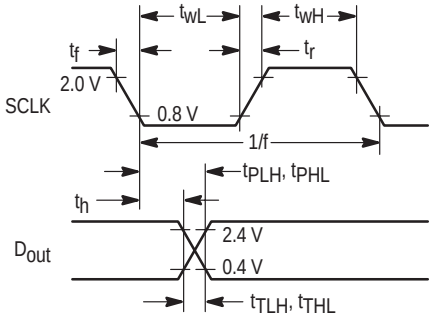


Figure 1.

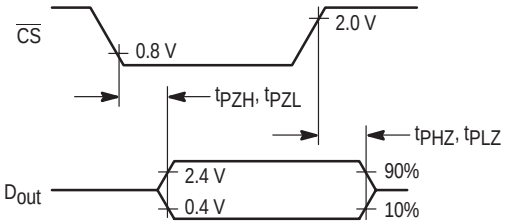


Figure 2.

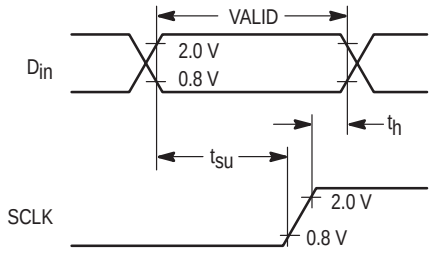
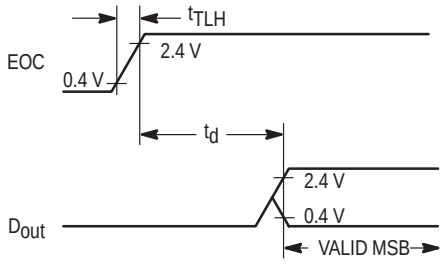


Figure 3.



NOTE: D_{out} is driven only when $\overline{CS}$ is active (low).

Figure 4.

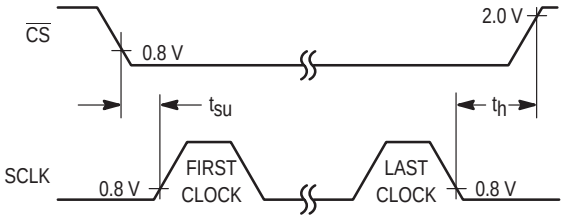


Figure 5.

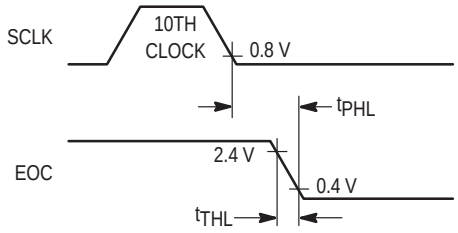


Figure 6.

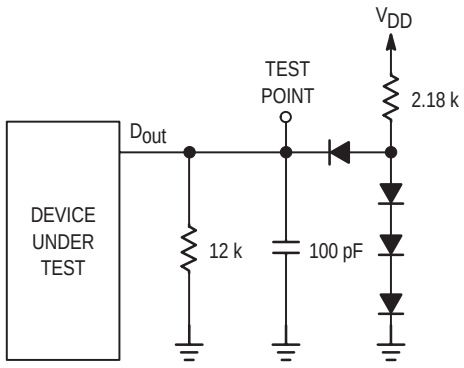


Figure 7. Test Circuit

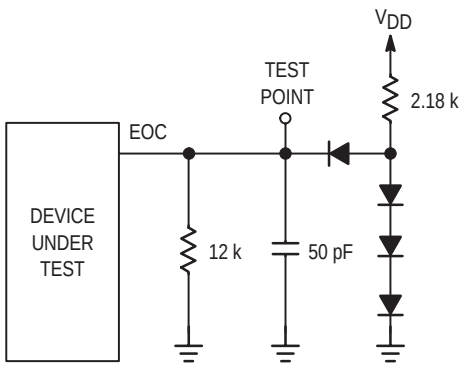


Figure 8. Test Circuit

PIN DESCRIPTIONS

DIGITAL INPUTS AND OUTPUT

The various serial bit-stream formats for the MC145050/51 are illustrated in the timing diagrams of Figures 9 through 14. Table 1 assists in selection of the appropriate diagram. Note that the ADCs accept 16 clocks which makes them SPI (Serial Peripheral Interface) compatible.

Table 1. Timing Diagram Selection

No. of Clocks in Serial Transfer	Using $\overline{CS}$	Serial Transfer Interval	Figure No.
10	Yes	Don't Care	9
10	No	Don't Care	10
11 to 16	Yes	Shorter than Conversion	11
16	No	Shorter than Conversion	12
11 to 16	Yes	Longer than Conversion	13
16	No	Longer than Conversion	14

$\overline{CS}$
Active-Low Chip Select Input (Pin 15)

Chip select initializes the chip to perform conversions and provides 3-state control of the data output pin (D_{out}). While inactive high, $\overline{CS}$ forces D_{out} to the high-impedance state and disables the data input (D_{in}) and serial clock (SCLK) pins. A high-to-low transition on $\overline{CS}$ resets the serial data port and synchronizes it to the MPU data stream. $\overline{CS}$ can remain active during the conversion cycle and can stay in the active low state for multiple serial transfers or $\overline{CS}$ can be inactive high after each transfer. If $\overline{CS}$ is kept active low between transfers, the length of each transfer is limited to either 10 or 16 SCLK cycles. If $\overline{CS}$ is in the inactive high state between transfers, each transfer can be anywhere from 10 to 16 SCLK cycles long. See the SCLK pin description for a more detailed discussion of these requirements.

On the MC145050/51 spurious chip selects caused by system noise are minimized by the internal circuitry.

Any transitions on the MC145050 $\overline{CS}$ pin are recognized as valid only if the level is maintained for a setup time plus two falling edges of ADCLK after the transition.

Transitions on the MC145051 $\overline{CS}$ pin are recognized as valid only if the level is maintained for about 2 μs after the transition.

NOTE

If $\overline{CS}$ is inactive high after the 10th SCLK cycle and then goes active low before the A/D conversion is complete, the conversion is aborted and the chip enters the initial state, ready for another serial transfer/conversion sequence. At this point, the output data register contains the result from the conversion before the aborted conversion. Note that the last step of the A/D conversion sequence is to update the output data register with the result. Therefore, if $\overline{CS}$ goes active low in an attempt to abort the conversion too close to the end of the conversion sequence, the result register may be corrupted and the chip could be thrown out of sync with the processor until $\overline{CS}$ is toggled again (refer to the AC Electrical Characteristics in the spec tables).

D_{out}
Serial Data Output of the A/D Conversion Result (Pin 16)

This output is in the high-impedance state when $\overline{CS}$ is inactive high. When the chip recognizes a valid active low on $\overline{CS}$, D_{out} is taken out of the high-impedance state and is driven with the MSB of the previous conversion result. (For the first transfer after power-up, data on D_{out} is undefined for the entire transfer.) The value on D_{out} changes to the second most significant result bit upon the first falling edge of SCLK. The remaining result bits are shifted out in order, with the LSB appearing on D_{out} upon the ninth falling edge of SCLK. Note that the order of the transfer is MSB to LSB. Upon the 10th falling edge of SCLK, D_{out} is immediately driven low (if allowed by $\overline{CS}$) so that transfers of more than 10 SCLKs read zeroes as the unused LSBs.

When $\overline{CS}$ is held active low between transfers, D_{out} is driven from a low level to the MSB of the conversion result for three cases: Case 1 — upon the 16th SCLK falling edge if the transfer is longer than the conversion time (Figure 14); Case 2 — upon completion of a conversion for a 16-bit transfer interval shorter than the conversion (Figure 12); Case 3 — upon completion of a conversion for a 10-bit transfer (Figure 10).

D_{in}
Serial Data Input (Pin 17)

The four-bit serial input stream begins with the MSB of the analog mux address (or the user test mode) that is to be converted next. The address is shifted in on the first four rising edges of SCLK. After the four mux address bits have been received, the data on D_{in} is ignored for the remainder of the present serial transfer. See Table 2 in **Applications Information**.

SCLK
Serial Data Clock (Pin 18)

This clock input drives the internal I/O state machine to perform three major functions: (1) drives the data shift registers to simultaneously shift in the next mux address from the D_{in} pin and shift out the previous conversion result on the D_{out} pin, (2) begins sampling the analog voltage onto the RC DAC as soon as the new mux address is available, and (3) transfers control to the A/D conversion state machine (driven by ADCLK) after the last bit of the previous conversion result has been shifted out on the D_{out} pin.

The serial data shift registers are completely static, allowing SCLK rates down to the dc. There are some cases, however, that require a minimum SCLK frequency as discussed later in this section. SCLK need not be synchronous to ADCLK. At least ten SCLK cycles are required for each simultaneous data transfer. If the 16-bit format is used, SCLK can be one continuous 16-bit stream or two intermittent 8-bit streams. After the serial port has been initiated to perform a serial transfer*, the new mux address is shifted in on the first

* The serial port can be initiated in three ways: (1) a recognized $\overline{CS}$ falling edge, (2) the end of an A/D conversion if the port is performing either a 10-bit or a 16-bit "shorter-than-conversion" transfer with $\overline{CS}$ active low between transfers, and (3) the 16th falling edge of SCLK if the port is performing 16-bit "longer-than-conversion" transfers with $\overline{CS}$ active low between transfers.

four rising edges of SCLK, and the previous 10-bit conversion result is shifted out on the first nine falling edges of SCLK. After the fourth rising edge of SCLK, the new mux address is available; therefore, on the next edge of SCLK (the fourth falling edge), the analog input voltage on the selected mux input begins charging the RC DAC and continues to do so until the tenth falling edge of SCLK. After this tenth SCLK edge, the analog input voltage is disabled from the RC DAC and the RC DAC begins the "hold" portion of the A/D conversion sequence. Also upon this tenth SCLK edge, control of the internal circuitry is transferred to ADCLK which drives the successive approximation logic to complete the conversion. If 16 SCLK cycles are used during each transfer, then there is a constraint on the minimum SCLK frequency. Specifically, there must be at least one rising edge on SCLK before the A/D conversion is complete. If the SCLK frequency is too low and a rising edge does not occur during the conversion, the chip is thrown out of sync with the processor and $\overline{CS}$ needs to be toggled in order to restore proper operation. If 10 SCLKs are used per transfer, then there is no lower frequency limit on SCLK. Also note that if the ADC is operated such that $\overline{CS}$ is inactive high between transfers, then the number of SCLK cycles per transfer can be anything between 10 and 16 cycles, but the "rising edge" constraint is still in effect if more than 10 SCLKs are used. (If $\overline{CS}$ stays active low for multiple transfers, the number of SCLK cycles must be either 10 or 16.)

ADCLK
A/D Conversion Clock Input (Pin 19, MC145050 Only)

This pin clocks the dynamic A/D conversion sequence, and may be asynchronous to SCLK. Control of the chip passes to ADCLK after the tenth falling edge of SCLK. Control of the chip is passed back to SCLK after the successive approximation conversion sequence is complete (44 ADCLK cycles), or after a valid chip select is recognized. ADCLK also drives the $\overline{CS}$ recognition logic. The chip ignores transitions on $\overline{CS}$ unless the state remains for a setup time plus two falling edges of ADCLK. The source driving ADCLK must be free running.

EOC
End-of-Conversion Output (Pin 19, MC145051 Only)

EOC goes low on the tenth falling edge of SCLK. A low-to-high transition on EOC occurs when the A/D conversion is complete and the data is ready for transfer.

ANALOG INPUTS AND TEST MODE

AN0 through AN10
Analog Multiplexer Inputs (Pins 1 – 9, 11, 12)

The input AN0 is addressed by loading $0 into the mux address register. AN1 is addressed by $1, AN2 by $2, …, AN10 by $A. Table 2 shows the input format for a 16-bit stream. The mux features a break-before-make switching structure to minimize noise injection into the analog inputs. The source resistance driving these inputs must be $\leq$ 1 kΩ.

During normal operation, leakage currents through the analog mux from unselected channels to a selected channel and leakage currents through the ESD protection diodes on the selected channel occur. These leakage currents cause an offset voltage to appear across any series source resistance on the selected channel. Therefore, any source resistance greater than 1 kΩ (Motorola test condition) may induce errors in excess of guaranteed specifications.

There are three tests available that verify the functionality of all the control logic as well as the successive approximation comparator. These tests are performed by addressing $B, $C, or $D and they convert a voltage of $(V_{ref} + V_{AG})/2$, V_{AG}, or V_{ref}, respectively. The voltages are obtained internally by sampling V_{ref} or V_{AG} onto the appropriate elements of the RC DAC during the sample phase. Addressing $B, $C, or $D produces an output of $200 (half scale), $000, or $3FF (full scale), respectively, if the converter is functioning properly. However, deviation from these values occurs in the presence of sufficient system noise (external to the chip) on V_{DD}, V_{SS}, V_{ref}, or V_{AG}.

POWER AND REFERENCE PINS

V_{SS} and V_{DD}
Device Supply Pins (Pins 10 and 20)

V_{SS} is normally connected to digital ground; V_{DD} is connected to a positive digital supply voltage. Low frequency ($V_{DD} – V_{SS}$) variations over the range of 4.5 to 5.5 volts do not affect the A/D accuracy. (See the Operations Ranges Table for restrictions on V_{ref} and V_{AG} relative to V_{DD} and V_{SS}.) Excessive inductance in the V_{DD} or V_{SS} lines, as on automatic test equipment, may cause A/D offsets > ± 1 LSB. Use of a 0.1 μF bypass capacitor across these pins is recommended.

V_{AG} and V_{ref}
Analog Reference Voltage Pins (Pins 13 and 14)

Analog reference voltage pins which determine the lower and upper boundary of the A/D conversion. Analog input voltages ≥ V_{ref} produce a full scale output and input voltages ≤ V_{AG} produce an output of zero. CAUTION: The analog input voltage must be ≥ V_{SS} and ≤ V_{DD}. The A/D conversion result is ratiometric to $V_{ref} – V_{AG}$. V_{ref} and V_{AG} must be as noise-free as possible to avoid degradation of the A/D conversion. Ideally, V_{ref} and V_{AG} should be single-point connected to the voltage supply driving the system's transducers. Use of a 0.22 μF bypass capacitor across these pins is strongly urged.

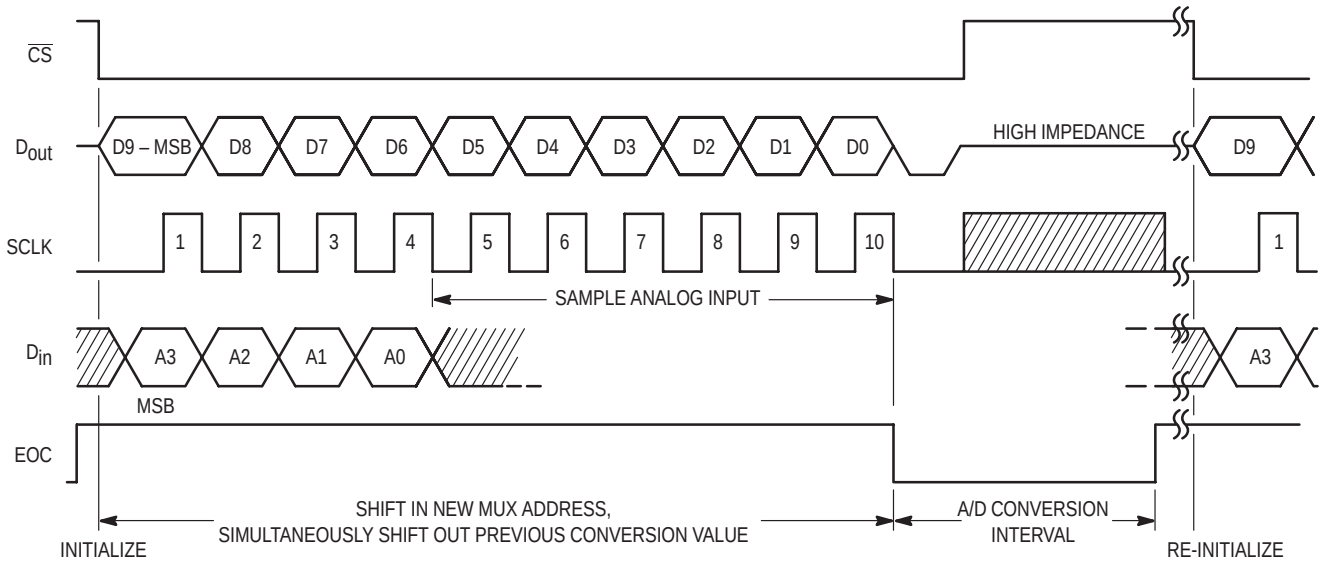


Figure 9. Timing for 10-Clock Transfer Using $\overline{CS}$*

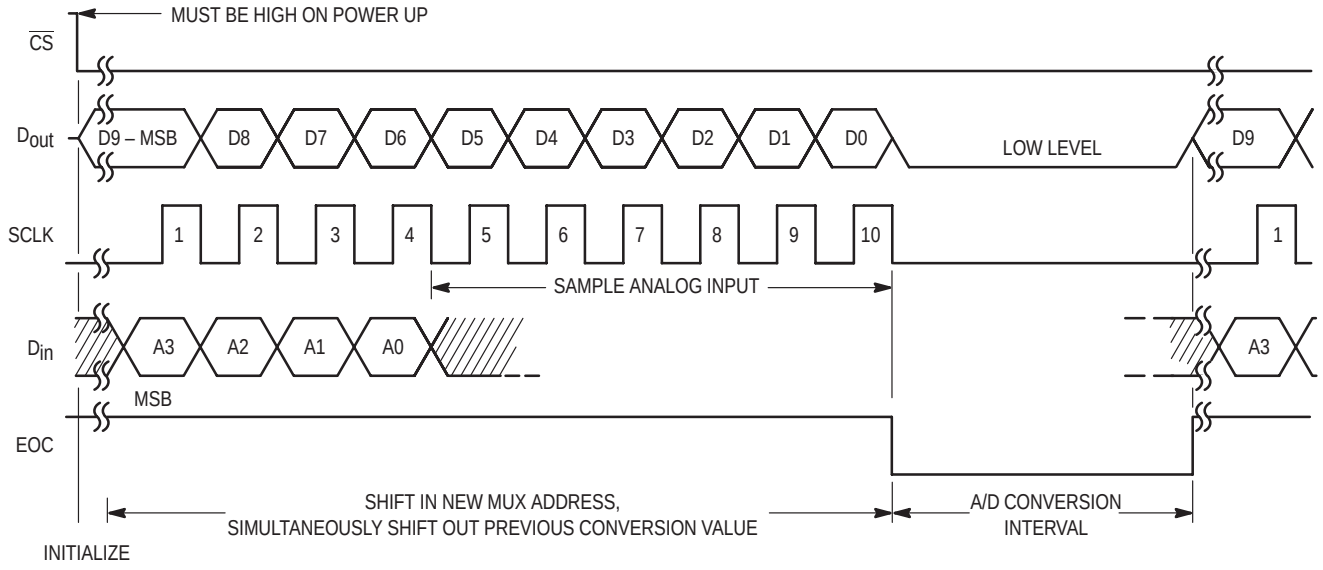


Figure 10. Timing for 10-Clock Transfer Not Using $\overline{CS}$*

NOTES:
1. D9, D8, D7, …, D0 = the result of the previous A/D conversion.
2. A3, A2, A1, A0 = the mux address for the next A/D conversion.

* This figure illustrates the behavior of the MC145051. The MC145050 behaves identically except there is no EOC signal and the conversion time is 44 ADCLK cycles (user-controlled time).

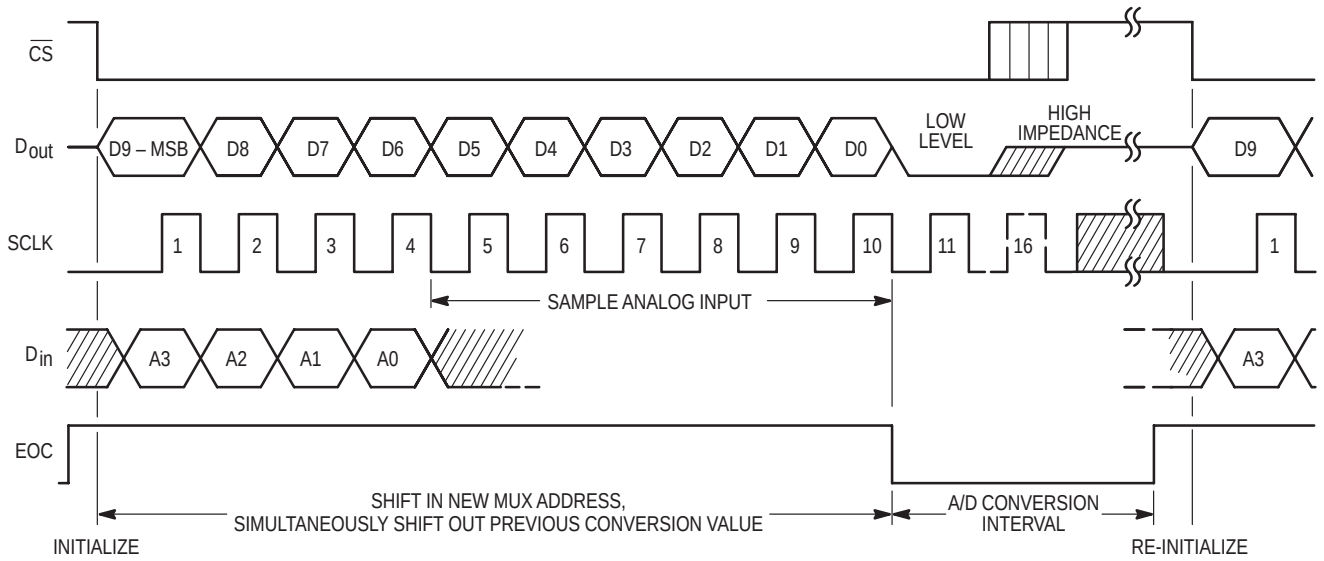


Figure 11. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$* (Serial Transfer Interval Shorter than Conversion)

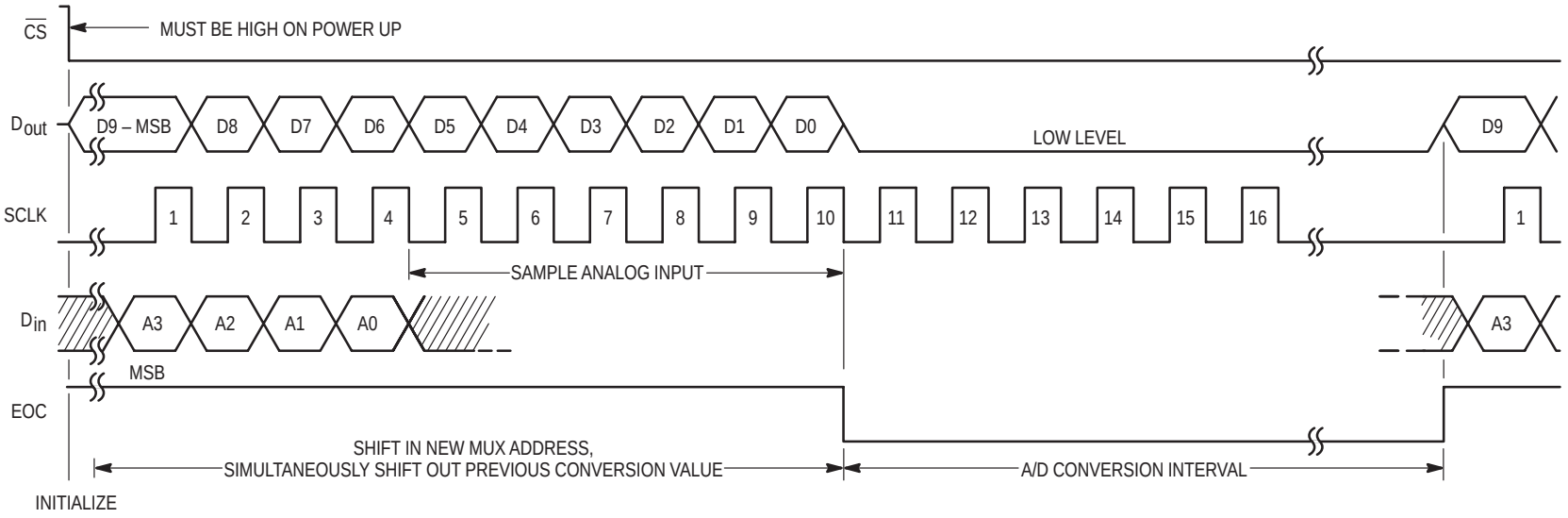


Figure 12. Timing for 16-Clock Transfer Not Using $\overline{CS}$* (Serial Transfer Interval Shorter Than Conversion)

NOTES:
D9, D8, D7, . . . , D0 = the result of the previous A/D conversion.
A3, A2, A1, A0 = the mux address for the next A/D conversion.
*This figure illustrates the behavior of the MC145051. The MC145050 behaves identically except there is no EOC signal and the conversion time is 44 ADCLK cycles (user-controlled time).

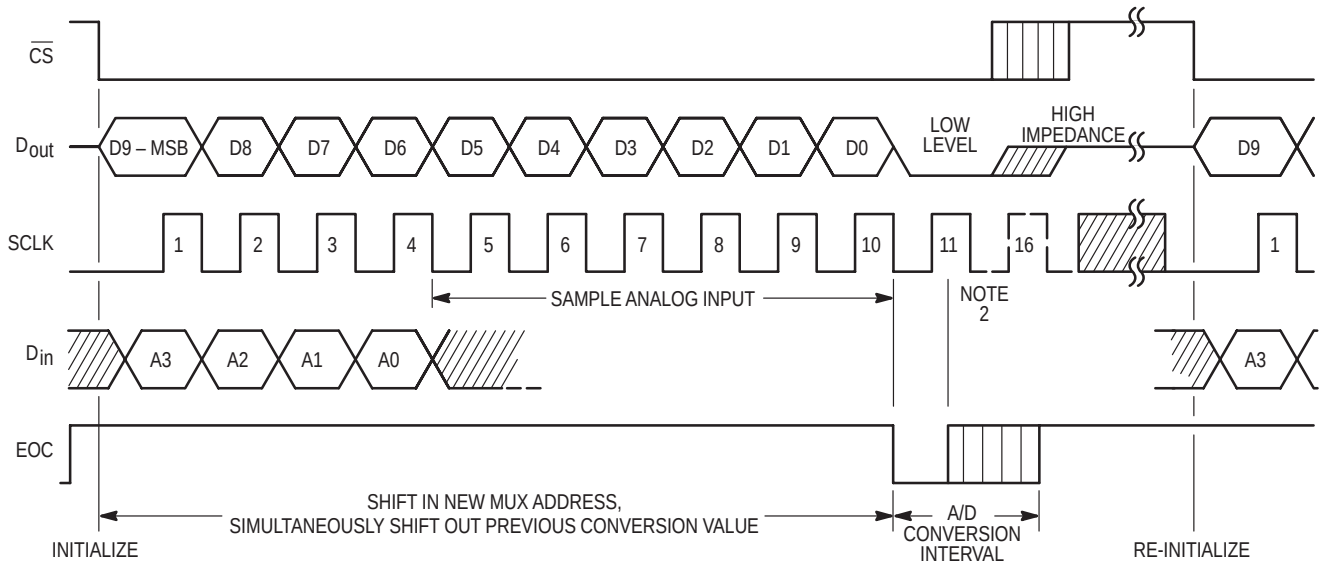


Figure 13. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$* (Serial Transfer Interval Longer Than Conversion)

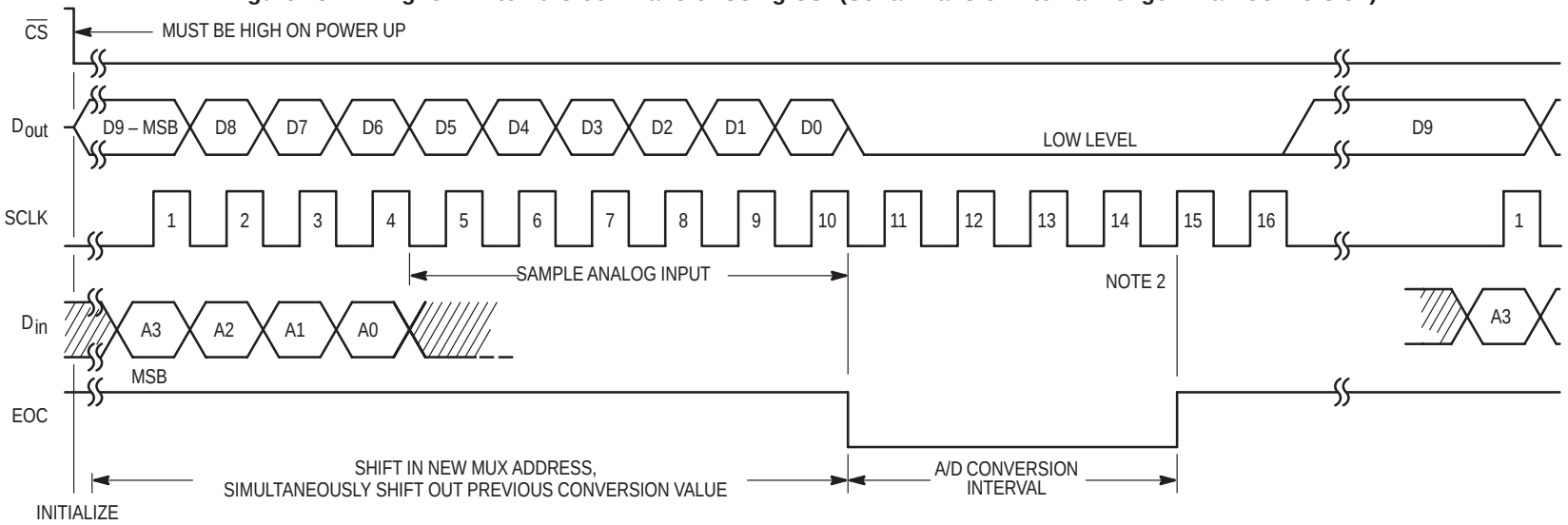


Figure 14. Timing for 16-Clock Transfer Not Using $\overline{CS}$* (Serial Transfer Interval Longer Than Conversion)

NOTES:

D9, D8, D7, . . . , D0 = the result of the previous A/D conversion.

A3, A2, A1, A0 = the mux address for the next A/D conversion.

*NOTES:

1. This figure illustrates the behavior of the MC145051. The MC145050 behaves identically except there is no EOC signal and the conversion time is 44 ADCLK cycles (user-controlled time).
2. The 11th SCLK rising edge must occur before the conversion is complete. Otherwise the serial port is thrown out of sync with the microprocessor for the remainder of the transfer.

APPLICATIONS INFORMATION

DESCRIPTION

This example application of the MC145050/MC145051 ADCs interfaces three controllers to a microprocessor and processes data in real-time for a video game. The standard joystick X-axis (left/right) and Y-axis (up/down) controls as well as engine thrust controls are accommodated.

Figure 15 illustrates how the MC145050/MC145051 is used as a cost-effective means to simplify this type of circuit design. Utilizing one ADC, three controllers are interfaced to a CMOS or NMOS microprocessor with a serial peripheral interface (SPI) port. Processors with National Semiconductor's MICROWIRE serial port may also be used. Full duplex operation optimizes throughput for this system.

DIGITAL DESIGN CONSIDERATIONS

Motorola's MC68HC05C4 CMOS MCU may be chosen to reduce power supply size and cost. The NMOS MCUs may be used if power consumption is not critical. A V_{DD} or V_{SS} 0.1 μF bypass capacitor should be closely mounted to the ADC.

Both the MC145050 and MC145051 accommodate all the analog system inputs. The MC145050, when used with a 2 MHz MCU, takes 27 μs to sample the analog input, perform the conversion, and transfer the serial data at 2 MHz. Forty-four ADCLK cycles (2 MHz at input pin 19) must be provided and counted by the MCU before reading the ADC results. The MC145051 has the end-of-conversion (EOC) signal (at output pin 19) to define when data is ready, but has a slower 49 μs cycle time. However, the 49 μs is constant for serial data rates of 2 MHz independent of the MCU clock frequency. Therefore, the MC145051 may be used with the CMOS MCU operating at reduced clock rates to minimize power consumption without severely sacrificing ADC cycle times, with EOC being used to generate an interrupt. (The MC145051 may also be used with MCUs which do not provide a system clock.)

ANALOG DESIGN CONSIDERATIONS

Controllers with output impedances of less than 1 kΩ may be directly interfaced to these ADCs, eliminating the need for buffer amplifiers. Separate lines connect the V_{ref} and V_{AG} pins on the ADC with the controllers to provide isolation from system noise.

Although not indicated in Figure 15, the V_{ref} and controller output lines may need to be shielded, depending on their length and electrical environment. This should be verified during prototyping with an oscilloscope. If shielding is required, a twisted pair or foil-shielded wire (not coax) is appropriate for this low frequency application. One wire of the pair or the shield must be V_{AG}.

A reference circuit voltage of 5 volts is used for this application. The reference circuitry may be as simple as tying V_{AG} to system ground and V_{ref} to the system's positive supply. (See Figure 16.) However, the system power supply noise may require that a separate supply be used for the voltage reference. This supply must provide source current for V_{ref} as well as current for the controller potentiometers.

A bypass capacitor of approximately 0.22 μF across the V_{ref} and V_{AG} pins is recommended. These pins are adjacent on the ADC package which facilitates mounting the capacitor very close to the ADC.

SOFTWARE CONSIDERATIONS

The software flow for acquisition is straightforward. The nine analog inputs, AN0 through AN8, are scanned by reading the analog value of the previously addressed channel into the MCU and sending the address of the next channel to be read to the ADC, simultaneously.

If the design is realized using the MC145050, 44 ADCLK cycles (at pin 19) must be counted by the MCU to allow time for A/D conversion. The designer utilizing the MC145051 has the end-of-conversion signal (at pin 19) to define the conversion interval. EOC may be used to generate an interrupt, which is serviced by reading the serial data from the ADC. The software flow should then process and format the data, and transfer the information to the video circuitry for updating the display.

When these ADCs are used with a 16-bit (2-byte) transfer, there are two types of offsets involved. In the first type of offset, the channel information sent to the ADCs is offset by 12 bits. That is, in the 16-bit stream, only the first 4 bits (4 MSBs) contain the channel information. The balance of the bits are don't cares. This results in 3 don't-care nibbles, as shown in Table 2. The second type of offset is in the conversion result returned from the ADCs; this is offset by 6 bits. In the 16-bit stream, the first 10 bits (10 MSBs) contain the conversion results. The last 6 bits are zeroes. The hexadecimal result is shown in the first column of Table 3. The second column shows the result after the offset is removed by a microprocessor routine. If the 16-bit format is used, these ADCs can transfer one continuous 16-bit stream or two intermittent 8-bit streams.

Table 2. Programmer's Guide for 16-Bit Transfers: Input Code

Input Address in Hex	Channel to be Converted Next	Comment
$0XXX	AN0	Pin 1
$1XXX	AN1	Pin 2
$2XXX	AN2	Pin 3
$3XXX	AN3	Pin 4
$4XXX	AN4	Pin 5
$5XXX	AN5	Pin 6
$6XXX	AN6	Pin 7
$7XXX	AN7	Pin 8
$8XXX	AN8	Pin 9
$9XXX	AN9	Pin 11
$AXXX	AN10	Pin 12
$BXXX	AN11	Half Scale Test: Output = $8000
$CXXX	AN12	Zero Test: Output = $0000
$DXXX	AN13	Full Scale Test: Output = $FFC0
$EXXX	None	Not Allowed
$FXXX	None	Not Allowed

Table 3. Programmer's Guide for 16-Bit Transfers: Output Code

Conversion Result Without Offset Removed	Conversion Result With Offset Removed	Value
$0000	$0000	Zero
$0040	$0001	Zero + 1 LSB
$0080	$0002	Zero + 2 LSBs
$00C0	$0003	Zero + 3 LSBs
$0100	$0004	Zero + 4 LSBs
$0140	$0005	Zero + 5 LSBs
$0180	$0006	Zero + 6 LSBs
$01C0	$0007	Zero + 7 LSBs
$0200	$0008	Zero + 8 LSBs
$0240	$0009	Zero + 9 LSBs
$0280	$000A	Zero + 10 LSBs
$02C0	$000B	Zero + 11 LSBs
⋮	⋮	⋮
$FF40	$03FD	Full Scale – 2 LSBs
$FF80	$03FE	Full Scale – 1 LSB
$FFC0	$03FF	Full Scale

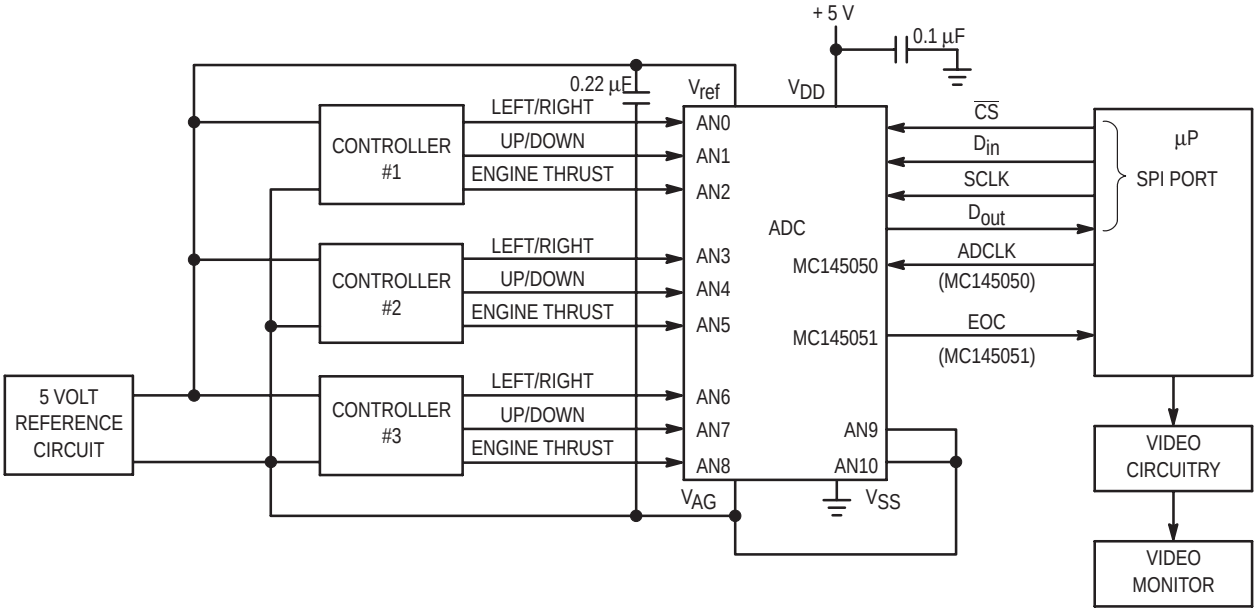


Figure 15. Joystick Interface

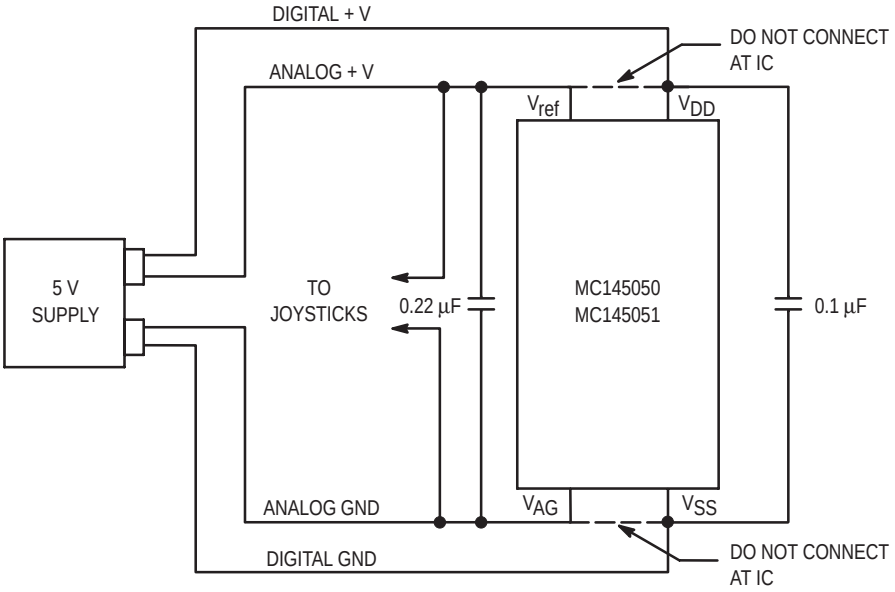


Figure 16. Alternate Configuration Using the Digital Supply for the Reference Voltage

Compatible Motorola MCUs/MPUs

This is not a complete listing of Motorola's MCUs/MPUs.
Contact your Motorola representative if you need
additional information.

Instruction Set	Memory (Bytes)		SPI SCI	Device Number
	ROM	EEPROM		
M6805	2096	—	—	MC68HC05C2
	2096	—	Yes	MC68HC05C3
	4160	—	Yes	MC68HC05C4
	4160	—	Yes	MC68HSC05C5
	8K	—	Yes	MC68HSC05C8
	4160	—	Yes	MC68HCL05C4
	8K	—	Yes	MC68HCL05C8
	7700	—	Yes	MC68HC05C8
	—	4160	—	MC68HC805C5
M68000	—	—	—	MC68HC000

SPI = Serial Peripheral Interface.

SCI = Serial Communication Interface.

High Speed.

Low Power.

MC145053

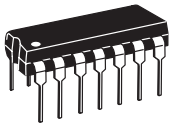
10-Bit A/D Converter with Serial Interface

CMOS

This ratiometric 10-bit ADC has a serial interface port to provide communication with MCUs and MPUs. *Either a 10- or 16-bit format can be used*. The 16-bit format can be one continuous 16-bit stream or two intermittent 8-bit streams. The converter operates from a single power supply with no external trimming required. Reference voltages down to 4.0 V are accommodated.

The MC145053 has an internal clock oscillator to operate the dynamic A/D conversion sequence and an end-of-conversion (EOC) output.

- 5 Analog Input Channels with Internal Sample-and-Hold
- Operating Temperature Range: – 40 to 125° C
- Successive Approximation Conversion Time: 44 μs Maximum
- Maximum Sample Rate: 20.4 ks/s
- Analog Input Range with 5-Volt Supply: 0 to 5 V
- Monotonic with No Missing Codes
- Direct Interface to Motorola SPI and National MICROWIRE Serial Data Ports
- Digital Inputs/Outputs are TTL, NMOS, and CMOS Compatible
- Low Power Consumption: 14 mW
- Chip Complexity: 1630 Elements (FETs, Capacitors, etc.)
- See Application Note AN1062 for Operation with QSPI



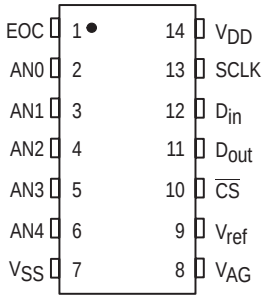
P SUFFIX
PLASTIC
CASE 646



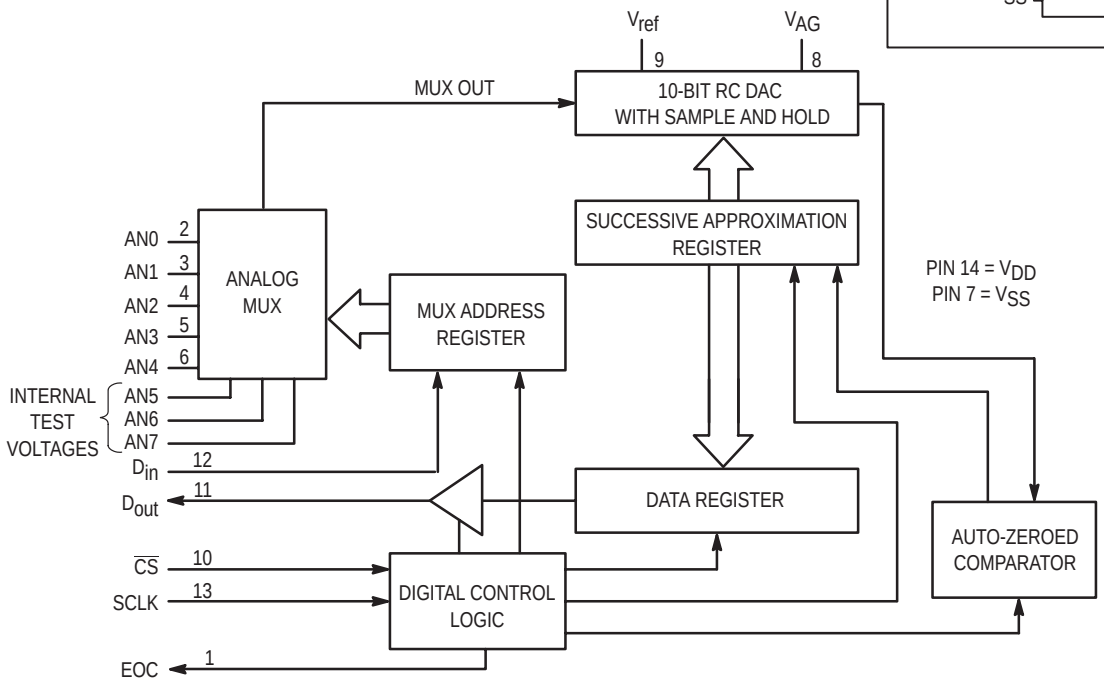
D SUFFIX
SOG
CASE 751A

ORDERING INFORMATION

PIN ASSIGNMENT



BLOCK DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	– 0.5 to + 6.0	V
V_{ref}	DC Reference Voltage	V_{AG} to V_{DD} + 0.1	V
V_{AG}	Analog Ground	V_{SS} – 0.1 to V_{ref}	V
V_{in}	DC Input Voltage, Any Analog or Digital Input	V_{SS} – 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	V_{SS} – 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{DD}, I_{SS}	DC Supply Current, V_{DD} and V_{SS} Pins	± 50	mA
T_{stg}	Storage Temperature	– 65 to 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges below..

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

OPERATION RANGES (Applicable to Guaranteed Limits)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage, Referenced to V_{SS}	4.5 to 5.5	V
V_{ref}	DC Reference Voltage	V_{AG} + 4.0 to V_{DD} + 0.1	V
V_{AG}	Analog Ground	V_{SS} – 0.1 to V_{ref} – 4.0	V
V_{AI}	Analog Input Voltage (See Note)	V_{AG} to V_{ref}	V
V_{in}, V_{out}	Digital Input Voltage, Output Voltage	V_{SS} to V_{DD}	V
T_A	Ambient Operating Temperature	– 40 to 125	°C

NOTE: Analog input voltages greater than V_{ref} convert to full scale. Input voltages less than V_{AG} convert to zero. See V_{ref} and V_{AG} pin descriptions.

DC ELECTRICAL CHARACTERISTICS

(Voltages Referenced to V_{SS}, Full Temperature and Voltage Ranges per Operation Ranges Table, unless otherwise indicated)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IH}	Minimum High-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$)		2.0	V
V_{IL}	Maximum Low-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$)		0.8	V
V_{OH}	Minimum High-Level Output Voltage (D_{out}, EOC)	I_{out} = – 1.6 mA I_{out} = – 20 µA	2.4 V_{DD} – 0.1	V
V_{OL}	Minimum Low-Level Output Voltage (D_{out}, EOC)	I_{out} = + 1.6 mA I_{out} = + 20 µA	0.4 0.1	V
I_{in}	Maximum Input Leakage Current (D_{in}, SCLK, $\overline{CS}$)	V_{in} = V_{SS} or V_{DD}	± 2.5	µA
I_{OZ}	Maximum Three-State Leakage Current (D_{out})	V_{out} = V_{SS} or V_{DD}	± 10	µA
I_{DD}	Maximum Power Supply Current	V_{in} = V_{SS} or V_{DD}, All Outputs Open	2.5	mA
I_{ref}	Maximum Static Analog Reference Current (V_{ref})	V_{ref} = V_{DD}, V_{AG} = V_{SS}	100	µA
I_{AI}	Maximum Analog Mux Input Leakage Current between all deselected inputs and any selected input (AN0 – AN4)	V_{AI} = V_{SS} to V_{DD}	± 1	µA

A/D CONVERTER ELECTRICAL CHARACTERISTICS

(Full Temperature and Voltage Ranges per Operation Ranges Table)

Characteristic	Definition and Test Conditions	Guaranteed Limit	Unit
Resolution	Number of bits resolved by the A/D converter	10	Bits
Maximum Nonlinearity	Maximum difference between an ideal and an actual ADC transfer function	± 1	LSB
Maximum Zero Error	Difference between the maximum input voltage of an ideal and an actual ADC for zero output code	± 1	LSB
Maximum Full-Scale Error	Difference between the minimum input voltage of an ideal and an actual ADC for full-scale output code	± 1	LSB
Maximum Total Unadjusted Error	Maximum sum of nonlinearity, zero error, and full-scale error	± 1	LSB
Maximum Quantization Error	Uncertainty due to converter resolution	± 1/2	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	± 1-1/2	LSB
Maximum Conversion Time	Total time to perform a single analog-to-digital conversion	44	µs
Data Transfer Time	Total time to transfer digital serial data into and out of the device	10 to 16	SCLK cycles
Sample Acquisition Time	Analog input acquisition time window	6	SCLK cycles
Minimum Total Cycle Time	Total time to transfer serial data, sample the analog input, and perform the conversion; SCLK = 2.1 MHz	49	µs
Maximum Sample Rate	Rate at which analog inputs may be sampled; SCLK = 2.1 MHz	20.4	ks/s

AC ELECTRICAL CHARACTERISTICS

(Full Temperature and Voltage Ranges per Operation Ranges Table)

Figure	Symbol	Parameter	Guaranteed Limit	Unit
1	f	Clock Frequency, SCLK (10-bit xfer) Min (11- to 16-bit xfer) Min Note: Refer to t_{wH}, t_{wL} below (10- to 16-bit xfer) Max)	0 Note 1 2.1	MHz
1	t_{wH}	Minimum Clock High Time, SCLK	190	ns
1	t_{wL}	Minimum Clock Low Time, SCLK	190	ns
1, 7	t_{PLH}, t_{PHL}	Maximum Propagation Delay, SCLK to D_{out}	125	ns
1, 7	t_h	Minimum Hold Time, SCLK to D_{out}	10	ns
2, 7	t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, $\overline{CS}$ to D_{out} High-Z	150	ns
2, 7	t_{PZL}, t_{PZH}	Maximum Propagation Delay, $\overline{CS}$ to D_{out} Driven	2.3	µs
3	t_{su}	Minimum Setup Time, D_{in} to SCLK	100	ns
3	t_h	Minimum Hold Time, SCLK to D_{in}	0	ns
4, 7, 8	t_d	Maximum Delay Time, EOC to D_{out} (MSB)	100	ns
5	t_{su}	Minimum Setup Time, $\overline{CS}$ to SCLK	2.425	µs
—	t_{CSd}	Minimum Time Required Between 10th SCLK Falling Edge (≤ 0.8 V) and $\overline{CS}$ to Allow a Conversion	Note 2	
—	t_{CAs}	Maximum Delay Between 10th SCLK Falling Edge (≤ 2 V) and $\overline{CS}$ to Abort a Conversion	9	µs
5	t_h	Minimum Hold Time, Last SCLK to $\overline{CS}$	0	ns
6, 8	t_{PHL}	Maximum Propagation Delay, 10th SCLK to EOC	2.35	µs
1	t_r, t_f	Maximum Input Rise and Fall Times SCLK D_{in}, $\overline{CS}$	1 10	ms µs
1, 4, 6 – 8	t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	300	ns
—	C_{in}	Maximum Input Capacitance AN0 – AN4 SCLK, $\overline{CS}$, D_{in}	55 15	pF
—	C_{out}	Maximum Three-State Output Capacitance D_{out}	15	pF

NOTES:

1. After the 10th SCLK falling edge (≤ 2 V), at least 1 SCLK rising edge (≥ 2 V) must occur within 18.5 µs.
2. A $\overline{CS}$ edge may be received immediately after an active transition on the EOC pin.

SWITCHING WAVEFORMS

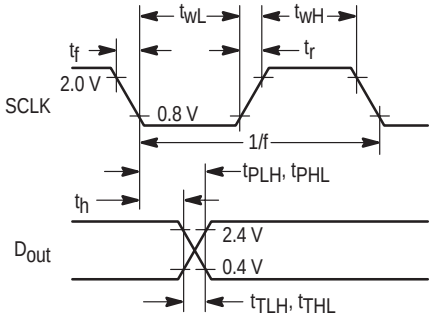


Figure 1.

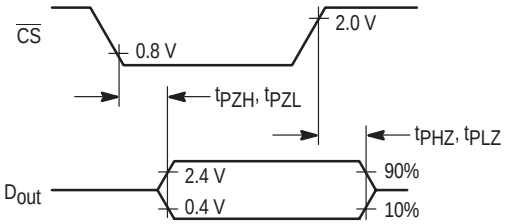


Figure 2.

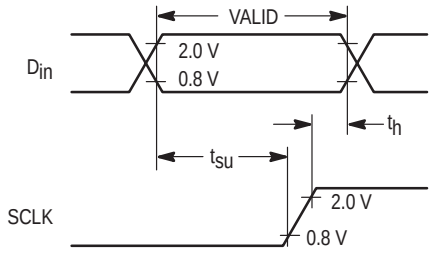
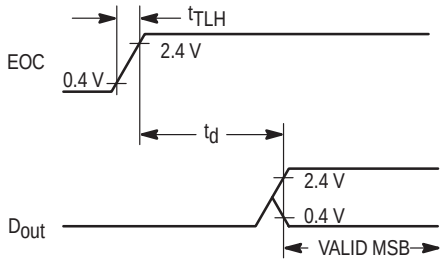


Figure 3.



NOTE: D_{out} is driven only when $\overline{CS}$ is active (low).

Figure 4.

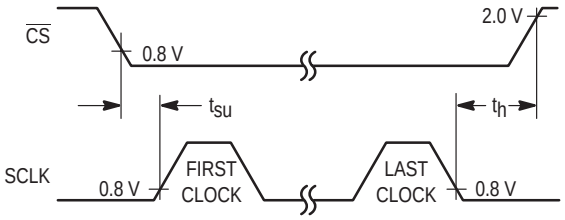


Figure 5.

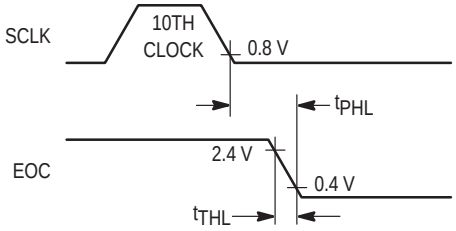


Figure 6.

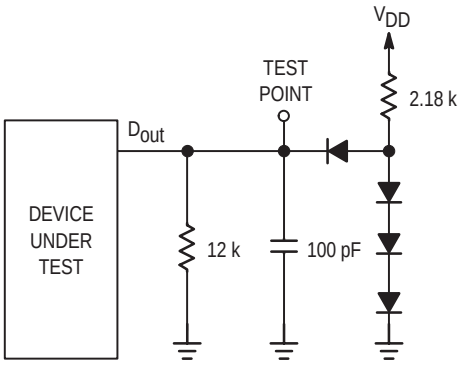


Figure 7. Test Circuit

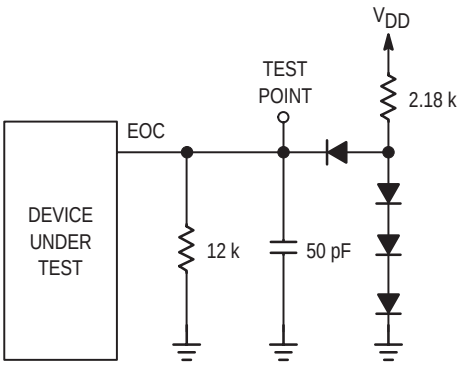


Figure 8. Test Circuit

PIN DESCRIPTIONS

DIGITAL INPUTS AND OUTPUT

The various serial bit-stream formats for the MC145053 are illustrated in the timing diagrams of Figures 9 through 14. Table 1 assists in selection of the appropriate diagram. Note that the ADC accepts 16 clocks which makes it SPI (Serial Peripheral Interface) compatible.

Table 1. Timing Diagram Selection

No. of Clocks in Serial Transfer	Using $\overline{CS}$	Serial Transfer Interval	Figure No.
10	Yes	Don't Care	9
10	No	Don't Care	10
11 to 16	Yes	Shorter than Conversion	11
16	No	Shorter than Conversion	12
11 to 16	Yes	Longer than Conversion	13
16	No	Longer than Conversion	14

$\overline{CS}$
Active-Low Chip Select Input (Pin 10)

Chip select initializes the chip to perform conversions and provides 3-state control of the data output pin (D_{out}). While inactive high, $\overline{CS}$ forces D_{out} to the high-impedance state and disables the data input (D_{in}) and serial clock (SCLK) pins. A high-to-low transition on $\overline{CS}$ resets the serial data port and synchronizes it to the MPU data stream. $\overline{CS}$ can remain active during the conversion cycle and can stay in the active low state for multiple serial transfers or $\overline{CS}$ can be inactive high after each transfer. If $\overline{CS}$ is kept active low between transfers, the length of each transfer is limited to either 10 or 16 SCLK cycles. If $\overline{CS}$ is in the inactive high state between transfers, each transfer can be anywhere from 10 to 16 SCLK cycles long. See the SCLK pin description for a more detailed discussion of these requirements.

Spurious chip selects caused by system noise are minimized by the internal circuitry. Any transitions on the $\overline{CS}$ pin are recognized as valid only if the level is maintained for about 2 μs after the transition.

NOTE

If $\overline{CS}$ is inactive high after the 10th SCLK cycle and then goes active low before the A/D conversion is complete, the conversion is aborted and the chip enters the initial state, ready for another serial transfer/conversion sequence. At this point, the output data register contains the result from the conversion before the aborted conversion. Note that the last step of the A/D conversion sequence is to update the output data register with the result. Therefore, if $\overline{CS}$ goes active low in an attempt to abort the conversion too close to the end of the conversion sequence, the result register may be corrupted and the chip could be thrown out of sync with the processor until $\overline{CS}$ is toggled again (refer to the AC Electrical Characteristics in the spec tables).

D_{out}
Serial Data Output of the A/D Conversion Result (Pin 11)

This output is in the high-impedance state when $\overline{CS}$ is inactive high. When the chip recognizes a valid active low on $\overline{CS}$, D_{out} is taken out of the high-impedance state and is driven with the MSB of the previous conversion result. (For the first transfer after power-up, data on D_{out} is undefined for the entire transfer.) The value on D_{out} changes to the second most significant result bit upon the first falling edge of SCLK. The remaining result bits are shifted out in order, with the LSB appearing on D_{out} upon the ninth falling edge of SCLK. Note that the order of the transfer is MSB to LSB. Upon the 10th falling edge of SCLK, D_{out} is immediately driven low (if allowed by $\overline{CS}$) so that transfers of more than 10 SCLKs read zeroes as the unused LSBs.

When $\overline{CS}$ is held active low between transfers, D_{out} is driven from a low level to the MSB of the conversion result for three cases: Case 1 — upon the 16th SCLK falling edge if the transfer is longer than the conversion time (Figure 14); Case 2 — upon completion of a conversion for a 16-bit transfer interval shorter than the conversion (Figure 12); Case 3 — upon completion of a conversion for a 10-bit transfer (Figure 10).

D_{in}
Serial Data Input (Pin 12)

The four-bit serial input stream begins with the MSB of the analog mux address (or the user test mode) that is to be converted next. The address is shifted in on the first four rising edges of SCLK. After the four mux address bits have been received, the data on D_{in} is ignored for the remainder of the present serial transfer. See Table 2 in **Applications Information**.

SCLK
Serial Data Clock (Pin 13)

This clock input drives the internal I/O state machine to perform three major functions: (1) drives the data shift registers to simultaneously shift in the next mux address from the D_{in} pin and shift out the previous conversion result on the D_{out} pin, (2) begins sampling the analog voltage onto the RC DAC as soon as the new mux address is available, and (3) transfers control to the A/D conversion state machine after the last bit of the previous conversion result has been shifted out on the D_{out} pin.

The serial data shift registers are completely static, allowing SCLK rates down to the dc. There are some cases, however, that require a minimum SCLK frequency as discussed later in this section. At least ten SCLK cycles are required for each simultaneous data transfer. If the 16-bit format is used, SCLK can be one continuous 16-bit stream or two intermittent 8-bit streams. After the serial port has been initiated to perform a serial transfer*, the new mux address is shifted in

* The serial port can be initiated in three ways: (1) a recognized $\overline{CS}$ falling edge, (2) the end of an A/D conversion if the port is performing either a 10-bit or a 16-bit "shorter-than-conversion" transfer with $\overline{CS}$ active low between transfers, and (3) the 16th falling edge of SCLK if the port is performing 16-bit "longer-than-conversion" transfers with $\overline{CS}$ active low between transfers.

on the first four rising edges of SCLK, and the previous 10-bit conversion result is shifted out on the first nine falling edges of SCLK. After the fourth rising edge of SCLK, the new mux address is available; therefore, on the next edge of SCLK (the fourth falling edge), the analog input voltage on the selected mux input begins charging the RC DAC and continues to do so until the tenth falling edge of SCLK. After this tenth SCLK edge, the analog input voltage is disabled from the RC DAC and the RC DAC begins the "hold" portion of the A/D conversion sequence. Also upon this tenth SCLK edge, control of the internal circuitry is transferred to the internal clock oscillator which drives the successive approximation logic to complete the conversion. If 16 SCLK cycles are used during each transfer, then there is a constraint on the minimum SCLK frequency. Specifically, there must be at least one rising edge on SCLK before the A/D conversion is complete. If the SCLK frequency is too low and a rising edge does not occur during the conversion, the chip is thrown out of sync with the processor and $\overline{CS}$ needs to be toggled in order to restore proper operation. If 10 SCLKs are used per transfer, then there is no lower frequency limit on SCLK. Also note that if the ADC is operated such that $\overline{CS}$ is inactive high between transfers, then the number of SCLK cycles per transfer can be anything between 10 and 16 cycles, but the "rising edge" constraint is still in effect if more than 10 SCLKs are used. (If $\overline{CS}$ stays active low for multiple transfers, the number of SCLK cycles must be either 10 or 16.)

EOC
End-of-Conversion Output (Pin 1)

EOC goes low on the tenth falling edge of SCLK. A low-to-high transition on EOC occurs when the A/D conversion is complete and the data is ready for transfer.

ANALOG INPUTS AND TEST MODES

AN0 through AN4
Analog Multiplexer Inputs (Pins 2 – 6)

The input AN0 is addressed by loading $0 into the mux address register. AN1 is addressed by $1, AN2 by $2, AN3 by $3, and AN4 by $4. Table 2 shows the input format for a 16-bit stream. The mux features a break-before-make switching structure to minimize noise injection into the analog inputs. The source resistance driving these inputs must be $\leq$ 1 kΩ.

During normal operation, leakage currents through the analog mux from unselected channels to a selected channel and leakage currents through the ESD protection diodes on the selected channel occur. These leakage currents cause an offset voltage to appear across any series source resistance on the selected channel. Therefore, any source resistance greater than 1 kΩ (Motorola test condition) may induce errors in excess of guaranteed specifications.

There are three tests available that verify the functionality of all the control logic as well as the successive approximation comparator. These tests are performed by addressing $B, $C, or $D and they convert a voltage of $(V_{ref} + V_{AG})/2$, V_{AG}, or V_{ref}, respectively. The voltages are obtained internally by sampling V_{ref} or V_{AG} onto the appropriate elements of the RC DAC during the sample phase. Addressing $B, $C, or $D produces an output of $200 (half scale), $000, or $3FF (full scale), respectively, if the converter is functioning properly. However, deviation from these values occurs in the presence of sufficient system noise (external to the chip) on V_{DD}, V_{SS}, V_{ref}, or V_{AG}.

POWER AND REFERENCE PINS

V_{SS} and V_{DD}
Device Supply Pins (Pins 7 and 14)

V_{SS} is normally connected to digital ground; V_{DD} is connected to a positive digital supply voltage. Low frequency ($V_{DD} - V_{SS}$) variations over the range of 4.5 to 5.5 volts do not affect the A/D accuracy. (See the Operations Ranges Table for restrictions on V_{ref} and V_{AG} relative to V_{DD} and V_{SS}.) Excessive inductance in the V_{DD} or V_{SS} lines, as on automatic test equipment, may cause A/D offsets > ± 1 LSB. Use of a 0.1 μF bypass capacitor across these pins is recommended.

V_{AG} and V_{ref}
Analog Reference Voltage Pins (Pins 8 and 9)

Analog reference voltage pins which determine the lower and upper boundary of the A/D conversion. Analog input voltages $\geq V_{ref}$ produce a full scale output and input voltages $\leq V_{AG}$ produce an output of zero. CAUTION: The analog input voltage must be $\geq V_{SS}$ and $\leq V_{DD}$. The A/D conversion result is ratiometric to $V_{ref} - V_{AG}$. V_{ref} and V_{AG} must be as noise-free as possible to avoid degradation of the A/D conversion. Ideally, V_{ref} and V_{AG} should be single-point connected to the voltage supply driving the system's transducers. Use of a 0.22 μF bypass capacitor across these pins is strongly urged.

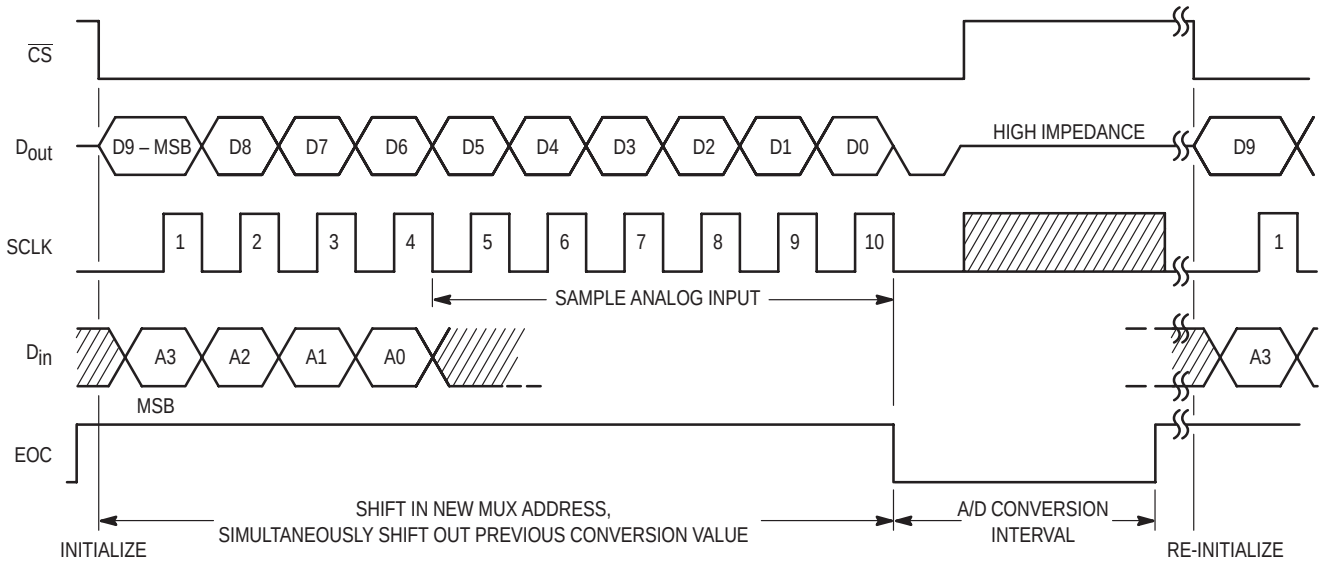


Figure 9. Timing for 10-Clock Transfer Using $\overline{CS}$

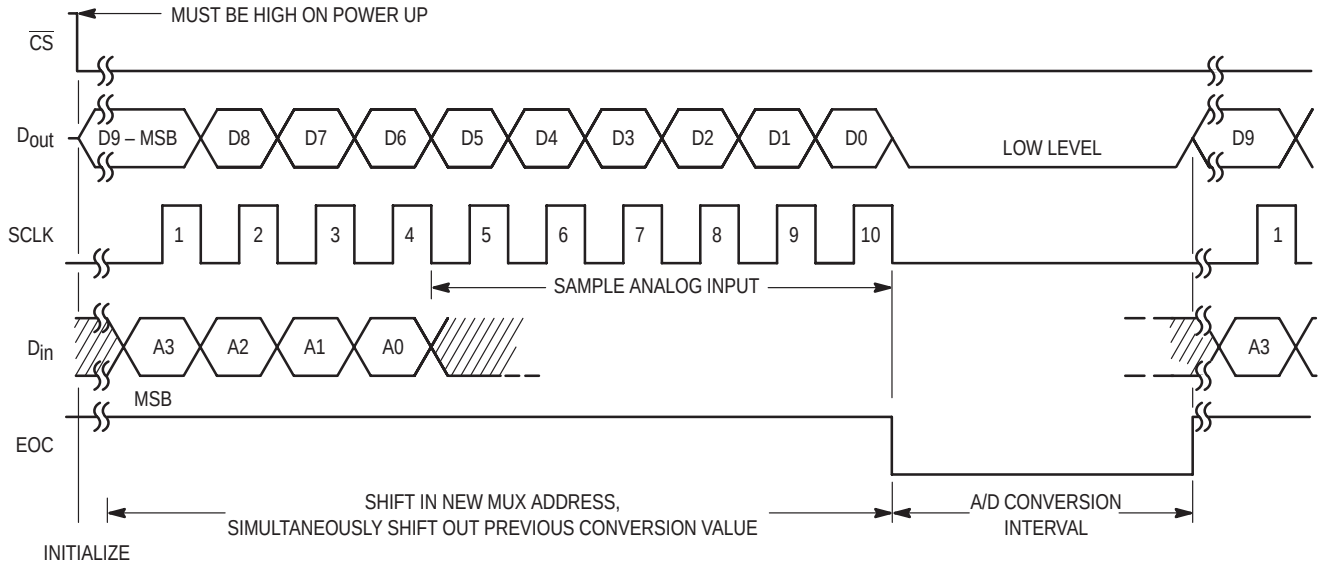


Figure 10. Timing for 10-Clock Transfer Not Using $\overline{CS}$

NOTES:
1. D9, D8, D7, D6, D5, …, D0 = the result of the previous A/D conversion.
2. A3, A2, A1, A0 = the mux address for the next A/D conversion.

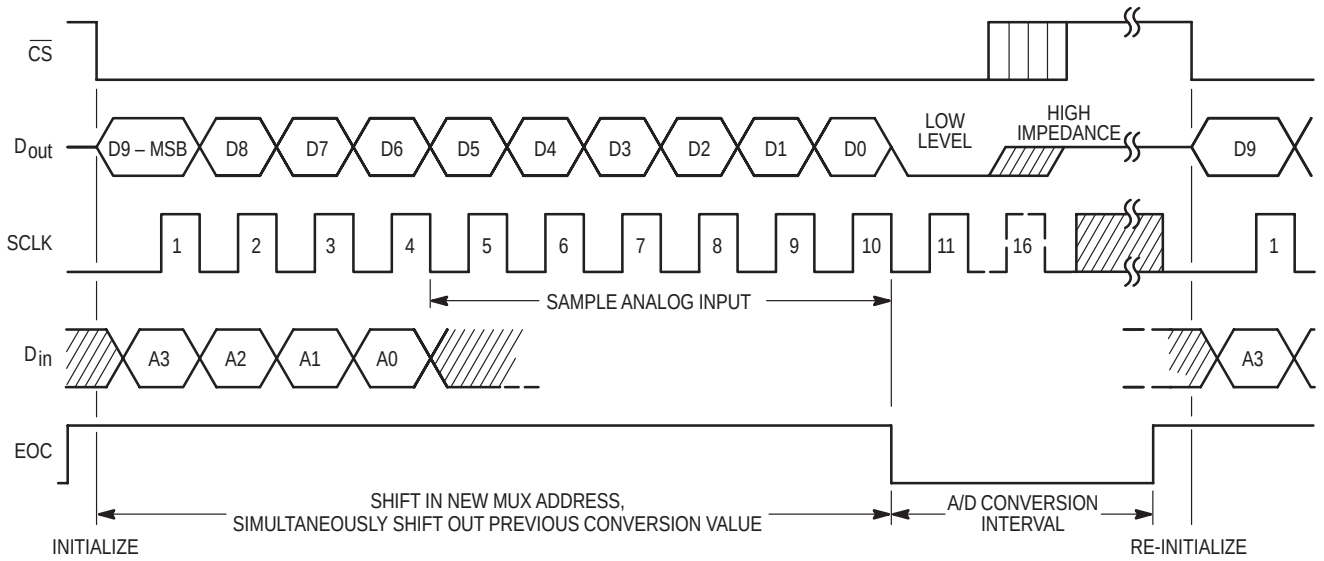


Figure 11. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$* (Serial Transfer Interval Shorter than Conversion)

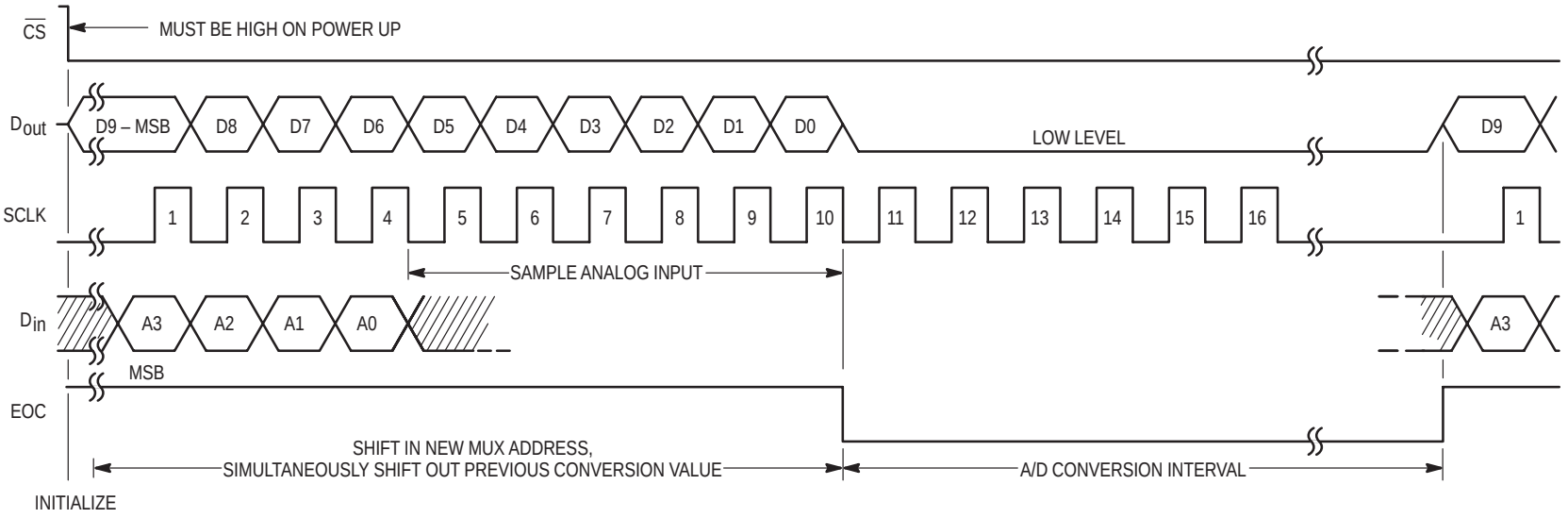


Figure 12. Timing for 16-Clock Transfer Not Using $\overline{CS}$* (Serial Transfer Interval Shorter Than Conversion)

NOTES:
D9, D8, D7, . . . , D0 = the result of the previous A/D conversion.
A3, A2, A1, A0 = the mux address for the next A/D conversion.
*This figure illustrates the behavior of the MC145051. The MC145050 behaves identically except there is no EOC signal and the conversion time is 44 ADCLK cycles (user-controlled time).

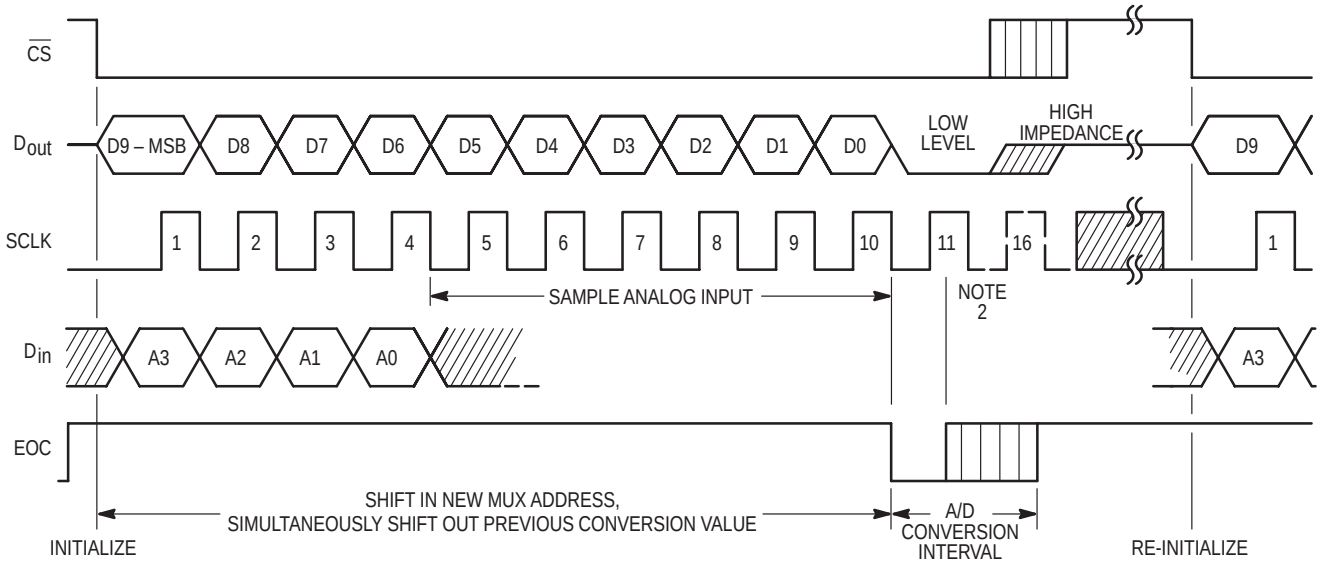


Figure 13. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$* (Serial Transfer Interval Longer Than Conversion)

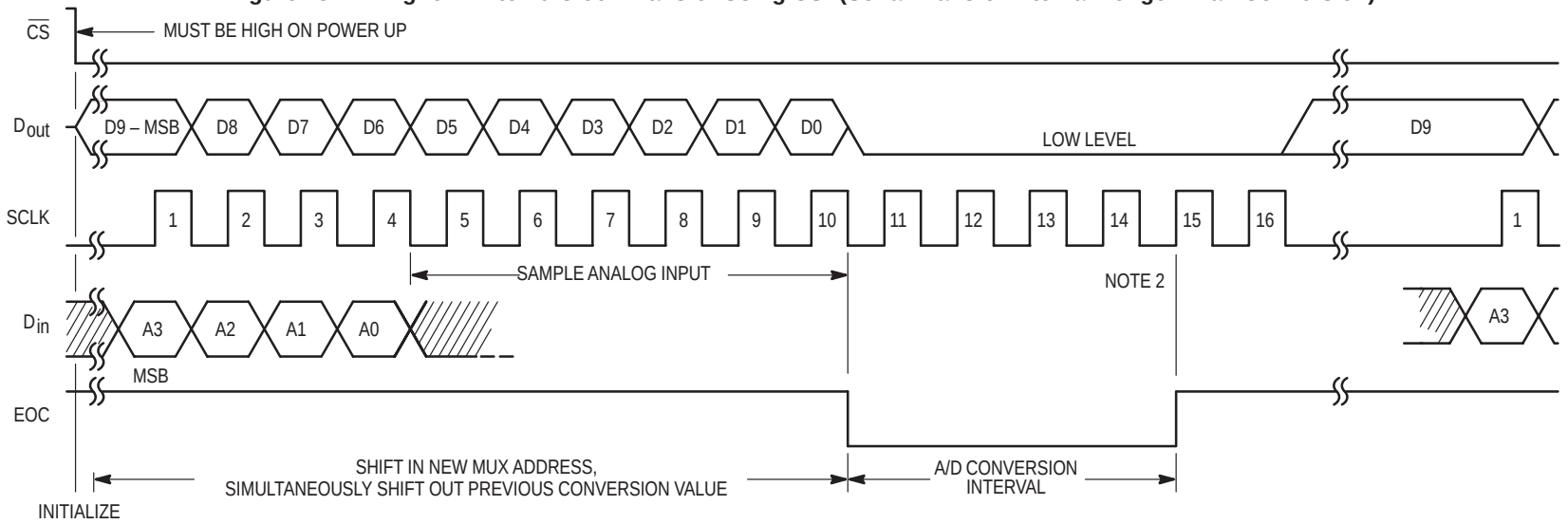


Figure 14. Timing for 16-Clock Transfer Not Using $\overline{CS}$* (Serial Transfer Interval Longer Than Conversion)

NOTES:

D9, D8, D7, . . . , D0 = the result of the previous A/D conversion.

A3, A2, A1, A0 = the mux address for the next A/D conversion.

*NOTES:

1. This figure illustrates the behavior of the MC145051. The MC145050 behaves identically except there is no EOC signal and the conversion time is 44 ADCLK cycles (user-controlled time).
2. The 11th SCLK rising edge must occur before the conversion is complete. Otherwise the serial port is thrown out of sync with the microprocessor for the remainder of the transfer.

APPLICATIONS INFORMATION

DESCRIPTION

This example application of the MC145053 ADC interfaces four analog signals to a microprocessor.

Figure 15 illustrates how the MC145053 is used as a cost-effective means to simplify this type of circuit design. Utilizing one ADC, four analog inputs are interfaced to a CMOS or NMOS microprocessor with a serial peripheral interface (SPI) port. Processors with National Semiconductor's MICROWIRE serial port may also be used. Full duplex operation optimizes throughput for this system.

DIGITAL DESIGN CONSIDERATIONS

Motorola's MC68HC05C4 CMOS MCU may be chosen to reduce power supply size and cost. The NMOS MCUs may be used if power consumption is not critical. A V_{DD} or V_{SS} 0.1 μF bypass capacitor should be closely mounted to the ADC.

The MC145053 has the end-of-conversion (EOC) signal at output pin 1 to define when data is ready.

ANALOG DESIGN CONSIDERATIONS

Analog signal sources with output impedances of less than 1 kΩ may be directly interfaced to the ADC, eliminating the need for buffer amplifiers. Separate lines connect the V_{ref} and V_{AG} pins on the ADC with the controllers to provide isolation from system noise.

Although not indicated in Figure 15, the V_{ref} and sensor output lines may need to be shielded, depending on their length and electrical environment. This should be verified during prototyping with an oscilloscope. If shielding is required, a twisted pair or foil-shielded wire (not coax) is appropriate for this low frequency application. One wire of the pair or the shield must be V_{AG}.

A reference circuit voltage of 5 volts is used for the application shown in Figure 15. However, the reference circuitry may be simplified by tying V_{AG} to system ground and V_{ref} to the system's positive supply. (See Figure 16.)

A bypass capacitor of approximately 0.22 μF across the V_{ref} and V_{AG} pins is recommended. These pins are adjacent on the ADC package which facilitates mounting the capacitor very close to the ADC.

SOFTWARE CONSIDERATIONS

The software flow for acquisition is straightforward. The four analog inputs, AN0 through AN3, are scanned by reading the analog value of the previously addressed channel into the MCU and sending the address of the next channel to be read to the ADC, simultaneously.

The designer utilizing the MC145053 has the end-of-conversion signal (at pin 1) to define the conversion interval. EOC may be used to generate an interrupt, which is serviced by reading the serial data from the ADC. The software flow should then process and format the data.

When this ADC is used with a 16-bit (2-byte) transfer, there are two types of offsets involved. In the first type of offset, the channel information sent to the ADCs is offset by 12 bits. That is, in the 16-bit stream, only the first 4 bits (4 MSBs) contain the channel information. The balance of the bits are don't cares. This results in 3 don't-care nibbles, as shown in Table 2. The second type of offset is in the conversion result returned from the ADC; this is offset by 6 bits. In the 16-bit stream, the first 10 bits (10 MSBs) contain the conversion result. The last 6 bits are zeroes. The hexadecimal result is shown in the first column of Table 3. The second column shows the result after the offset is removed by a microprocessor routine. If the 16-bit format is used, the ADC can transfer one continuous 16-bit stream or two intermittent 8-bit streams.

Table 2. Programmer's Guide for 16-Bit Transfers: Input Code

Input Address in Hex	Channel to be Converted Next	Comment
$0XXX	AN0	Pin 2
$1XXX	AN1	Pin 3
$2XXX	AN2	Pin 4
$3XXX	AN3	Pin 5
$4XXX	AN4	Pin 6
$5XXX	None	Not Allowed
$6XXX	None	Not Allowed
$7XXX	None	Not Allowed
$8XXX	None	Not Allowed
$9XXX	None	Not Allowed
$AXXX	None	Not Allowed
$BXXX	AN5	Half Scale Test: Output = $8000
$CXXX	AN6	Zero Test: Output = $0000
$DXXX	AN7	Full Scale Test: Output = $FFC0
$EXXX	None	Not Allowed
$FXXX	None	Not Allowed

Table 3. Programmer's Guide for 16-Bit Transfers: Output Code

Conversion Result Without Offset Removed	Conversion Result With Offset Removed	Value
$0000	$0000	Zero
$0040	$0001	Zero + 1 LSB
$0080	$0002	Zero + 2 LSBs
$00C0	$0003	Zero + 3 LSBs
$0100	$0004	Zero + 4 LSBs
$0140	$0005	Zero + 5 LSBs
$0180	$0006	Zero + 6 LSBs
$01C0	$0007	Zero + 7 LSBs
$0200	$0008	Zero + 8 LSBs
$0240	$0009	Zero + 9 LSBs
$0280	$000A	Zero + 10 LSBs
$02C0	$000B	Zero + 11 LSBs
⋮	⋮	⋮
$FF40	$03FD	Full Scale – 2 LSBs
$FF80	$03FE	Full Scale – 1 LSB
$FFC0	$03FF	Full Scale

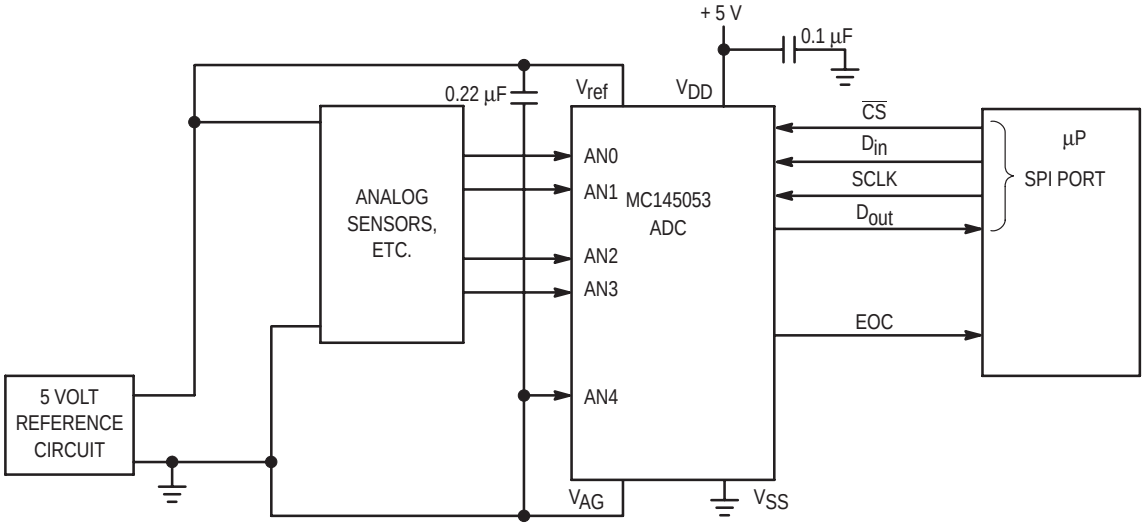


Figure 15. Example Application

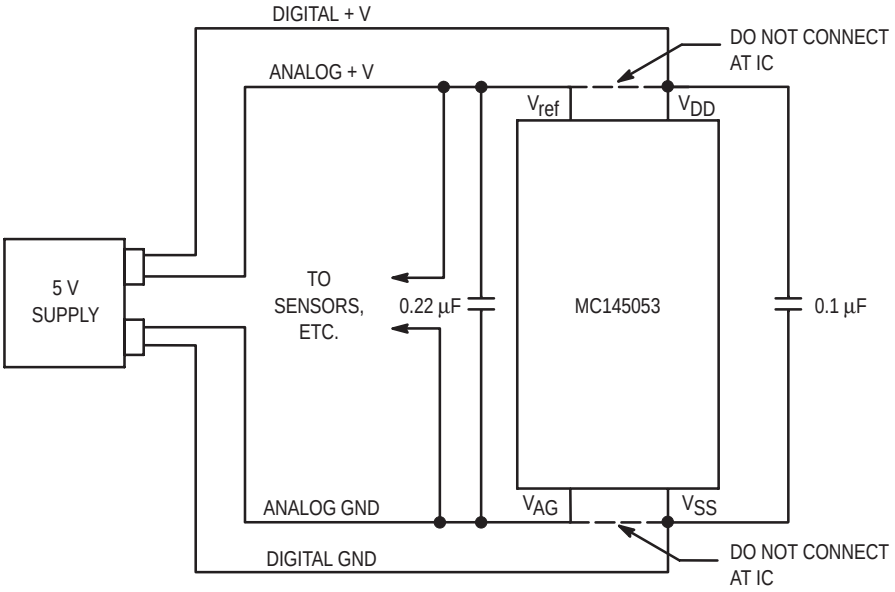


Figure 16. Alternate Configuration Using the Digital Supply for the Reference Voltage

Compatible Motorola MCUs/MPUs

This is not a complete listing of Motorola's MCUs/MPUs.
Contact your Motorola representative if you need
additional information.

Instruction Set	Memory (Bytes)		SPI SCI	Device Number
	ROM	EEPROM		
M6805	2096	—	—	MC68HC05C2
	2096	—	Yes	MC68HC05C3
	4160	—	Yes	MC68HC05C4
	4160	—	Yes	MC68HSC05C4
	8K	—	Yes	MC68HSC05C8
	4160	—	Yes	MC68HCL05C4
	8K	—	Yes	MC68HCL05C8
	7700	—	Yes	MC68HC05C8
	—	4160	—	MC68HC805C4
M68000	—	—	—	MC68HC000

SPI = Serial Peripheral Interface.

SCI = Serial Communication Interface.

High Speed.

Low Power.

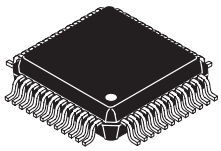
The MRFIC Line
Integrated GPS Downconverter

MRFIC1502

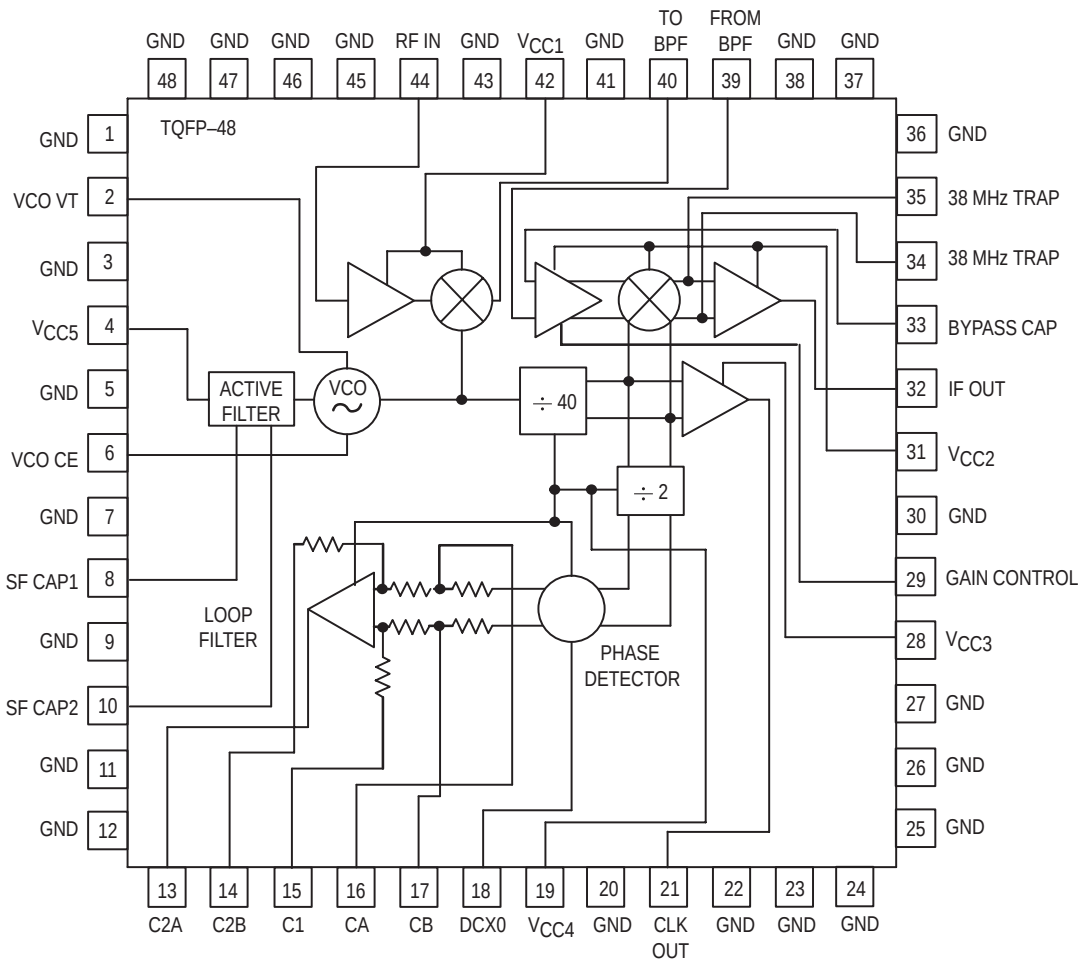
1.575 GHz GPS DOWNCONVERTER

This integrated circuit is intended for GPS receiver applications. The dual conversion design is implemented in Motorola's low–cost high performance MOSAIC 3 silicon bipolar process and is packaged in a low–cost surface mount TQFP–48 package. In addition to the mixers, a VCO, a PLL and a loop filter are integrated on–chip. Output IF is nominally 9.5 MHz.

- 65 dB Minimum Conversion Gain
- 5 Volts Operation
- 50 mA Typical Current Consumption
- Low–Cost, Low Profile Plastic LQFP Package
- Order MRFIC1502R2 for Tape and Reel.
  R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1502



CASE 932–02
(LQFP–48)



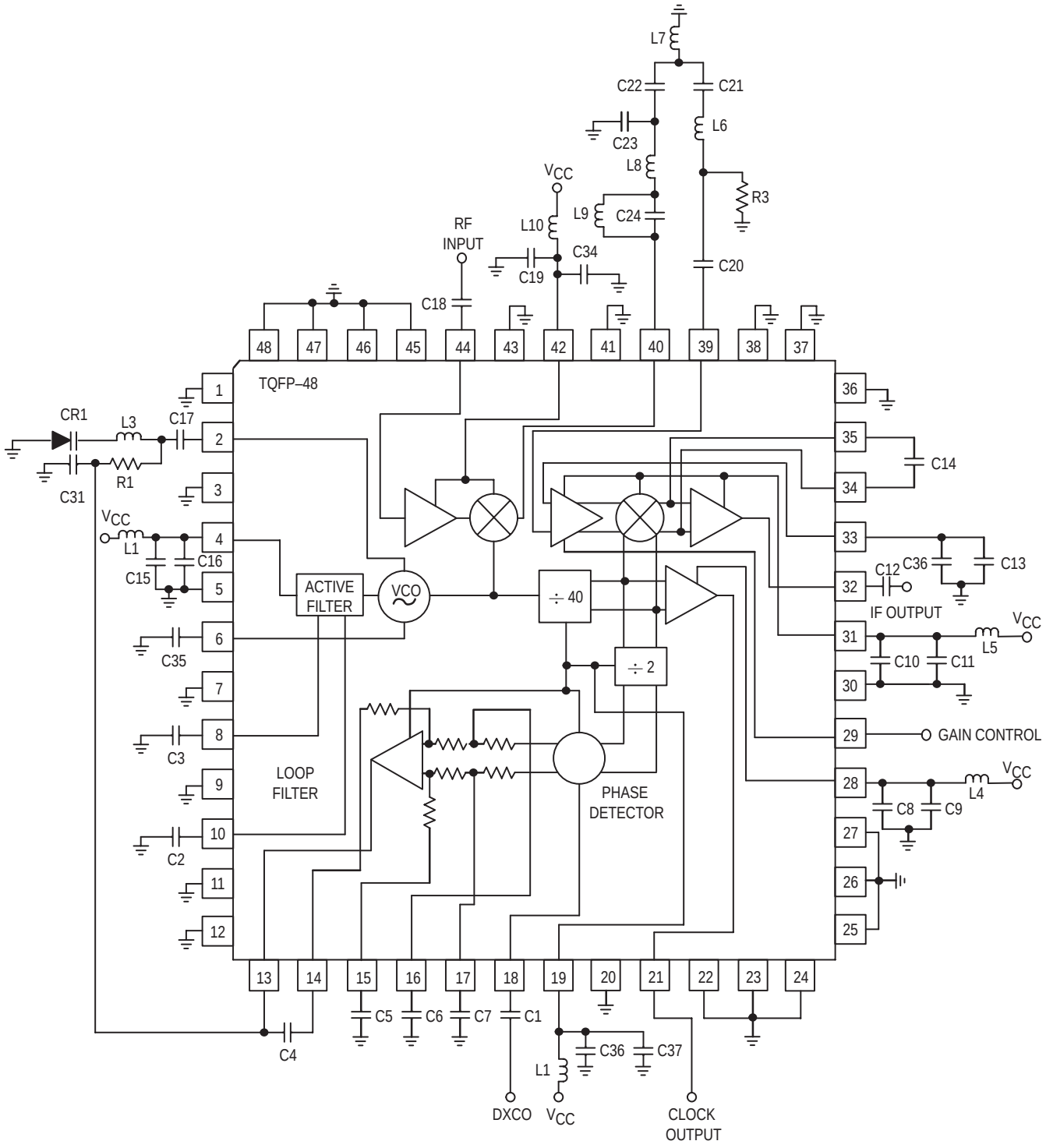
Pin Connections and Functional Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Limit	Unit
DC Supply Voltage	V_{DD}	+6.0	Vdc
DC Supply Current	I_{DD}	60	mA
Operating Ambient Temperature	T_A	– 40 to + 100	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Lead Soldering Temperature Range (10 seconds)	—	+260	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, and V_{CC} = 5 V, Tested in Circuit shown in Figure 1 unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Supply Voltage	4.75	—	5.25	Vdc
Supply Current	—	—	60	mA
L–Band Gain (Measured from L–Band Input to 47 MHz Output)	—	20	—	dB
IF Gain (Measured from 47 MHz Input to 9.5 MHz Output with Gain Control at Maximum)	—	45	—	dB
Conversion Gain (Measured from L–Band Input to 9.5 MHz Output with Gain Control at Maximum)	65	—	—	dB
Gain Control (Externally Adjustable 0 to 5.0 V, Maximum at 0 V)	—	40	—	dB
Noise Figure (Double Sideband)	—	9.5	—	dB
L–Band Input VSWR (Measured into 50 Ω; 1575.42 ± 5.0 MHz)	—	2:1	—	—
First IF Output VSWR (Measured into 50 Ω; 47.74 ± 5.0 MHz)	—	2:1	—	—
Second IF Output VSWR (Measured into 50 Ω; 9.5 ± 5.0 MHz)	—	2:1	—	—
Input Impedance @ 1st IF 47.7 ± 5 MHz (For Reference Only)	—	2000	—	Ω
Output 1.0 dB Compression Point	—	–7	—	dBm
First LO (Measured at the First IF Output)	—	–20	—	dBm
All Other Harmonics (Measured at the First IF Output)	—	–45	—	dBm
38.1915 MHz Leakage at First IF Output	—	–50	—	dBm
Second LO (Measured at the Second IF Output)	—	–25	—	dBm
All Other Harmonics (Measured at Second IF Output)	—	–45	—	dBm
Reference Oscillator Input	400	—	4500	mVpp
Clock Output Frequency Amplitude Low HIgh (Clock Amplitude Measured with the Output Loaded in 15 pF and 40 kΩ) Duty Cycle	$2Xf_{ref}$ — 2.0 45	—	$2Xf_{ref}$ 0.8 — 55	 V V %
VCO Lock Voltage	1.2	—	3.0	V
Phase Detector Gain	—	0.16	—	V/Radian
VCO Modulation Sensitivity	—	15	—	MHz/V



C1, C8, C10, C12, C13, C15, C19, C20, C37	10,000 pF	C24	68 pF, ATC
		C35	0.4 pF, ATC
C4, C5	5600 pF	CR1	2.7 pF, MA45233–123, MACOM
C6, C7, C31	1000 pF	L1, L4, L5, L10	2.2 μH, 1008CS–222XKBC, COILCRAFT
C2, C3	1.0 μF	L3	2.2 nH, LL2012–F2N2S, TOKO
C14	3.9 pF, ATC	L6	2.2 μH
C16, C18, C36	27 pF, ATC	L7	220 nH
C17	15 pF, ATC	L8	0.56 μH
C21	5.6 pF, ATC	L9	0.27 μH
C9, C11, C34, C36	47 pF, ATC	R1	10 kΩ
C22, C23	120 pF, ATC	R3	220 Ω

Figure 1. Test Circuit Configuration

Table 1. Port Impedance Derived from Circuit Characterization

Pin Number	Pin Name	f (MHz)	Z_{in} Ohms	
			R	jX
44	RF IN	1575.42	38.3	–16.09
40	TO BPF	47.74	54.45	11.3
39	FROM BPF	47.74	43	1.5
32	IF OUT	9.5	560	–850

Z_{in} represents the input impedance of the pin.

APPLICATION INFORMATION

Design Philosophy

The MRFIC1502 design is a standard dual downconversion configuration with an integrated fixed frequency phase–locked loop to generate the two local oscillators and the buffer to generate the sampling clock for a digital correlator and decimator. The active device for the L–band VCO is also integrated on the chip. This chip is designed in the third generation of Motorola's Oxide Self Aligned Integrated Circuits (MOSAIC 3) silicon bipolar process.

Circuit Considerations

The RF input to the MRFIC1502 is internally matched to 50 ohms. Therefore, only AC coupling is required on the input. The output of the amplifier is fed directly into the first mixer. This mixer is an active Gilbert Cell configuration. The output of the mixer is brought off–chip for filtering of the unwanted mixer products. The amplifier and mixer have their own V_{CC} supply (pin 42) in order to reduce the amount of coupling to the other circuits. There are two bypass capacitors on this pin, one for the high frequency components and one for the lower frequency components. These two capacitors should be placed physically as close to the bias pin as possible to reduce the inductance in the path. The capacitors should also be grounded as close to the ground of the IC as possible, preferably through a ground plane.

The output impedance of the first mixer is 50 ohms, while the input impedance to the first IF amplifier is 1 kΩ. There is a trap (zero) designed in at the second LO frequency to limit the amount of LO leakage into the high gain first IF amplifier.

The first IF amplifier is a variable gain amplifier with 25 dB of gain and 40 dB of gain control. The gain control pin can be grounded to provide the maximum gain out of the amplifier. If the baseband design utilizes a multi–bit A/D converter in the digital signal processing chip, this amplifier could be used to control the input to the A/D converter. The amplifier has an external bypassing capacitor. This capacitor should be on the order of 0.01 μF, and again should be located near the package pin.

The second mixer design is also a Gilbert Cell configuration. The interface between the mixer and the second IF amplifier is differential in order to increase noise immunity. This differential interface is also brought off–chip so that some additional filtering could be added in parallel between the output of the mixer and input to the amplifier. This filtering is primarily to reduce the amount of LO leakage into the final IF amplifier and is achieved using a single 3.9 pF capacitor across the differential ports. The value of the capacitor determines the high frequency of the low pass structure.

The supply pin for the IF circuits is pin 33. This supply pin should be isolated from the other chip supplies in order to reduce the amount of coupling. The recommended capacitors are a 47 pF and a 0.01 μF, in parallel to bypass the supply to ground and should be placed physically as close to the pin as possible.

The output of the second IF amplifier is 50 ohms with a bandwidth of ±5.0 MHz. This signal must be filtered before being digitized in order to limit the noise entering the A/D converter.

VCO Resonator Design

The design and layout of the circuits around the voltage controlled oscillator (VCO) are the most sensitive of the entire layout. The active device and biasing resistors are integrated on the MRFIC1502. The external circuits consist of the power supply decoupling, the capacitors for the integrated supply superfilter, the resonator and frequency adjusting elements, and the bypassing capacitor on the emitter of the active device.

The VCO supply is isolated from the rest of the PLL circuits in order to reduce the amount of noise that could cause frequency/phase noise in the VCO. The supply should be filtered using a 22 μH inductor in series and a 27 pF and 0.01 μF in parallel. The 27 pF capacitor should be series resonant at least as high as the VCO frequency to get the most L–band bypassing as possible. The on–chip supply filter requires two capacitors off–chip to filter the supply. The capacitors on the input (pin 8) and output (pin 10) of the filter are 1.0 μF, and the output also has a high frequency bypass capacitor in parallel. The input capacitor should not be smaller than a 1.0 μF to insure stability of the supply filter.

The VCO design is a standard negative resistance cell with a buffer amplifier. The resonating structure is connected to the base of the active device and consists of a coupling capacitor, a hyper–abrupt varactor diode, and a wire wound chip inductor. With the values shown on the application

circuit, the VCO is centered at 1527.7 MHz, and the gain of the VCO is approximately 20 MHz/Volt.

The above performance is heavily dependent on the capacitive structure that is used as the emitter bypass on pin 6. The total capacitance should be approximately 1.0 pF; that can be achieved using either a discrete element or a microstrip open circuited stub. The evaluation circuit shown uses a 0.4 pF capacitor.

Phase–locked Loop Design

The VCO signal at 1527.68 MHz is divided by 40 to get the second LO frequency of 38.19 MHz. In addition to providing the LO to the second mixer, the 38 MHz signal is output through a translator and is used as the sampling clock for the digital correlator and decimator circuits. There is an additional divide by two so the signal used by the phase detector is at 19.096 MHz. The reference input to the phase detector (pin 18) has an input sensitivity of 400 mVpp minimum and 2.5 Vpp maximum.

The loop filter design is the standard op–amp loop filter, resulting in a type 2 second order loop. The layout of the discrete components around the loop filter and VCO is very critical to the performance of the phase–locked loop. Care should be taken in routing the VCO control voltage line from the output of the loop filter to the varactor diode.

The output of the divide by 40 is buffered by a clock translator that converts the low level sine wave into a TTL level square wave. The loading on the buffer is high so the peak currents can reach as high as 50 mA with the maximum load of 1.0 kΩ in parallel with 40 pF on the output. Therefore, the translator has a dedicated V_{CC} supply, pin 28, which requires external bypassing and isolation. The recommended bypassing uses two capacitors in parallel, a 47 pF and a 0.01 μF capacitor.

Conclusion

The MRFIC1502 offers a highly integrated downconverter solution for GPS receivers. For more detailed applications information on GPS system design refer to application note AN1610, “Using Motorola’s MRFIC1502 in Global Positioning System Receivers.”

MOTOROLA

MRFIC1504

Advance Information

Integrated GPS Downconverter

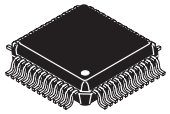
This integrated circuit is intended for GPS receiver applications. The dual conversion design is implemented in Motorola's low–cost, high–performance MOSAIC 5™ silicon bipolar process and is packaged in a low–cost surface mount LQFP–48 package. In addition to the mixers, a VCO, PLL, Crystal Oscillator, optional bandpass IF filter, A/D converter and a loop filter are integrated on–chip. Output IF is nominally 4.1 MHz.

- 105 dB Typical Conversion Gain
- 2.7 V Operation
- 27 mA Typical Current Consumption
- Low–Cost, Low–Profile Plastic LQFP Package

MOSAIC 5 is a trademark of Motorola, Inc.

1.575 GHz GPS DOWNCONVERTER

SEMICONDUCTOR TECHNICAL DATA

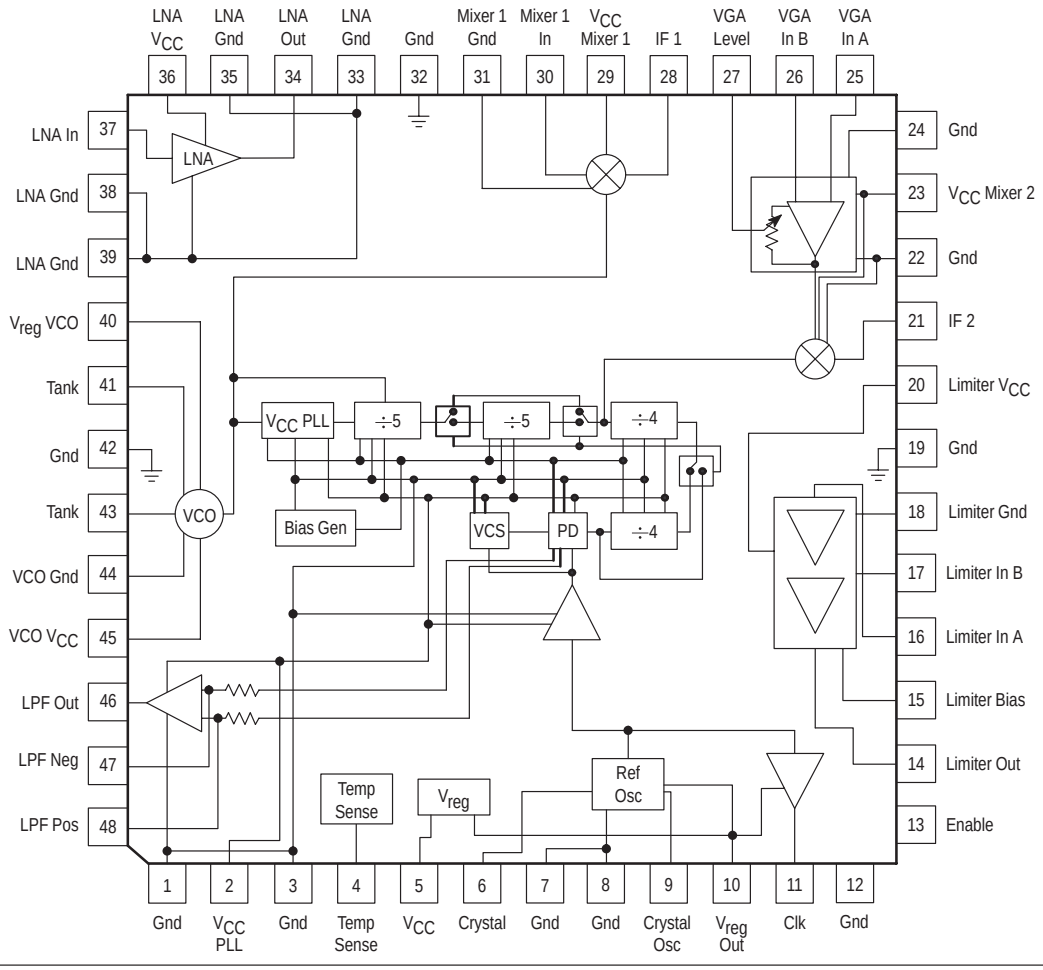


PLASTIC PACKAGE
CASE 932
(LQFP–48, Tape & Reel Only)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MRFIC1504R2	T_A = –40 to 85°C	LQFP–48

Pin Connections and Functional Block Diagram



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	5.0	Vdc
DC Supply Current	I_{DD}	60	mA
Operating Ambient Temperature	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Lead Soldering Temperature Range (10 seconds)	–	260	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables.
2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) up to 150 V and Machine Model (MM) up to 30 V. Additional ESD data available upon request.

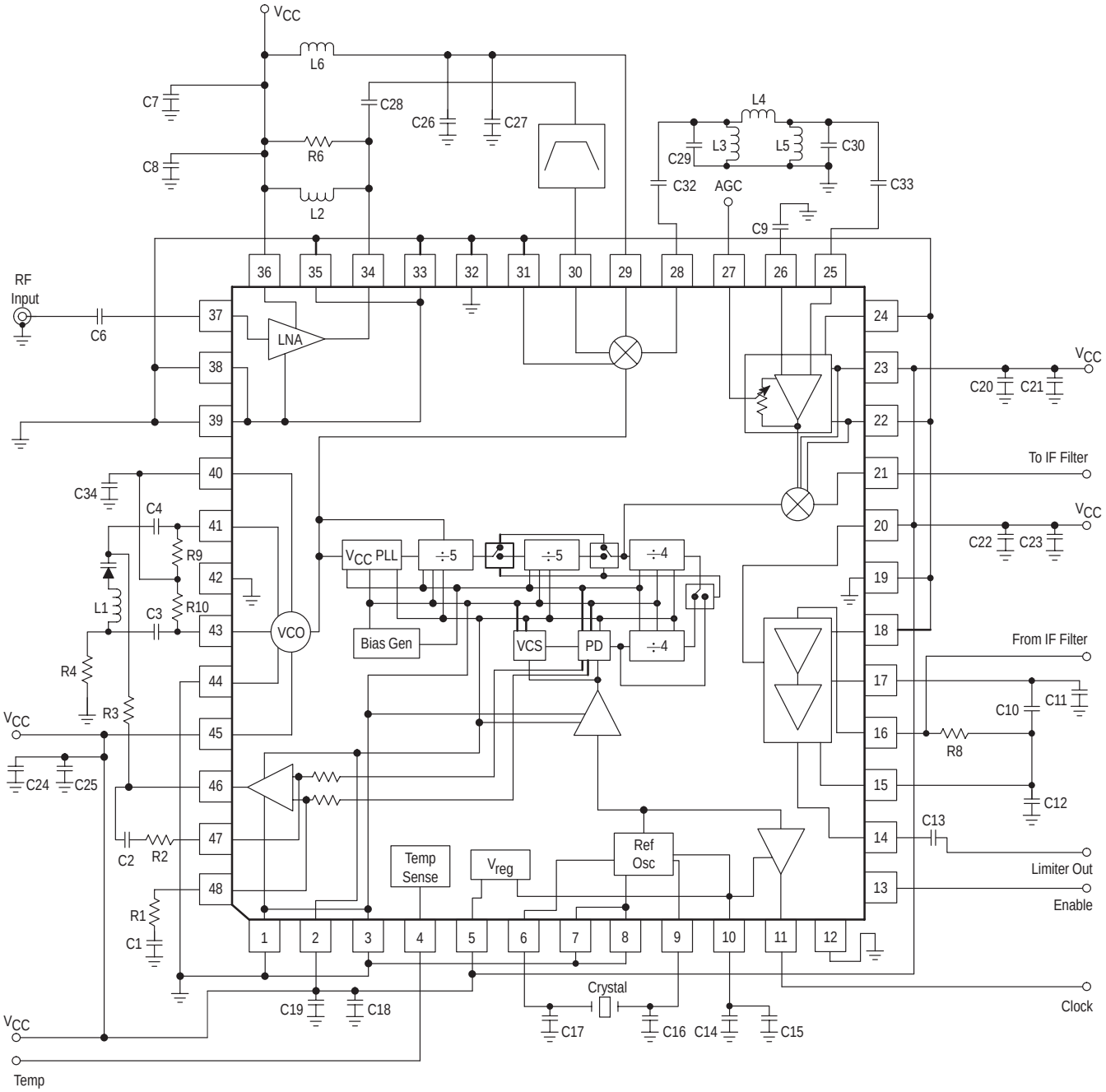
ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 3.3 V; T_A = –40 to 85°C; Enable = 2.7 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
TOTAL DEVICE					
Supply Voltage	V_{CC}	2.7	3.0	3.3	V
Supply Current (T_A = 25°C, V_{CC} = 2.7 V, Enable = 2.7 V)	I_{CC}	–	28	36	mA
Supply Current (T_A = 25°C, V_{CC} = 2.7 V, Enable = 0 V)	I_{CC}	–	2.0	4.0	mA
RF AMPLIFIER					
RF Input Frequency	f_{in}	–	1575.42	–	MHz
Input Impedance	Z_{in}	–	50	–	Ω
Input VSWR	$VSWR_{in}$	–	2.0	–	–
Gain	G	13	15	–	dB
Noise Figure	NF	–	2.0	–	dB
1.0 dB Compression (Measured at Output)	P_{1dB}	–	1.0	–	dBm
FIRST MIXER					
Input Frequency	f_{in}	–	1575.42	–	MHz
Gain	G	10	14	–	dB
Noise Figure	NF	–	13	–	dB
1.0 dB Compression (Measured at Output)	P_{1dB}	–	–13	–	dBm
First Local Oscillator Frequency	f_{LO1}	–	1636.8	–	MHz
First Intermediate Frequency	f_{IF1}	–	61.38	–	MHz
LO Leakage at IF Port	–	–	–40	–	dBm
LO Leakage at RF Port	–	–	–50	–	dBm
Output Impedance	Z_{out}	–	50	–	Ω
FIRST IF AMPLIFIER and SECOND MIXER					
Input Frequency	f_{in}	–	61.38	–	MHz
Imput Impedance	Z_{in}	–	230	–	Ω
Output Impedance	Z_{out}	–	50	–	Ω
Second Local Oscillator Frequency	f_{LO2}	–	65.47	–	MHz
Second Intermediate Frequency	f_{IF2}	–	4.092	–	MHz
LO Leakage at IF Port	–	–	–40	–	dBm
Gain	G	40	43	–	dB
Cascaded Noise Figure	NF	–	9.3	–	dB
1.0 dB Compression Point (Measured at Output)	P_{1dB}	–	–13	–	dBm

ELECTRICAL CHARACTERISTICS — continued (V_{CC} = 2.7 to 3.3 V; T_A = –40 to 85°C; Enable = 2.7 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
LIMITING AMPLIFIER					
Second Intermediate Frequency	f_{IF2}	–	4.092	–	MHz
Input Signal Level	–	4.0	11	31	mV
Output Voltage Swing (Into 10 pf ‖ 100 kΩ)	V_{out}	800	–	–	mVpp
DC Output Level	–	–	1.4	–	V
Gain	G	–	50	–	dB
REFERENCE OSCILLATOR					
Reference Frequency	f_r	–	16.368	–	MHz
Reference Frequency Input Level (Crystal Output Pin)	–	–	500	–	mVpp
Reference Oscillator Output Voltage Level (Into 15 pF ‖ 10 kΩ)	–	750	–	–	mVpp
Reference Clock Input Drive Level	–	400	800	1500	mVpp
PLL					
First Local Oscillator Frequency	f_{LO1}	–	1636.8	–	MHz
Second Local Oscillator Frequency	f_{LO2}	–	65.47	–	MHz
VCO C/N (at 10 kHz Offset)	–	–	–80	–	dBc/Hz
VCO Gain (TBD Varactor)	–	–	20	–	MHz/V
ENABLE					
Enable Active Level	–	0.8 × V_{CC}	V_{CC}	–	V
Disable Active Level	–	–	0	0.2 × V_{CC}	V
VOLTAGE REGULATOR					
Regulator Output Voltage (V_{CC} = 2.7 to 3.3 V, I_{out} = 3.0 mA)	V_o	2.1	2.3	2.5	V
TEMPERATURE SENSE SPECS					
Temperature Sensor Output Voltage @ 25°C	–	1.2	1.28	1.35	V
Temperature Sensor Slope over Temperature	–	–	5.0	–	mV/°C

Figure 1. Applications Schematic (1636.8 MHz LO)



C1, C2	220 pF	C29, C30	91 pF
C3, C4	1.7 pF	C32, C33	1.0 nF
C6	10 pF	L1	10 nH
C7, C14, C18, C20, C22, C24, C34	0.01 µF	L2	3.9 nH
C8, C15, C19, C21, C23, C25, C27	1000 pF	L3, L5	82 nH
C9	1.0 µF	L4	0.62 µH
C10, C11, C12	1.0 npF	L6	TBD
C13	2.7 nF	R1, R2, R4	10 k
C16, C17	27 pF	R3	2 k
C26	470 pF	R6	1.2 k
C28	0.6 pF	R8	5.0 k
		R9, R10	20 k

NOTES: 1. R8 must be set to match your 2nd IF filter impedance.
2. Layout of capacitors C10, C11, C12 is critical for stability of Limiter.

900 MHz ISM Band Transceiver Demonstration and Evaluation System

INTRODUCTION

The DataRadioEVS1 is comprised of two individual components, the YS1CTLR (i.e. controller) and RFMOD2 Transceiver with Baseband (i.e. target). This system allows an individual to quickly evaluate and prototype a 902–928MHz ISM band, low–power transceiver for either full–duplex voice or data applications and can be used with a Motorola MC74HC05 based M68MMEVS05 system to develop and debug assembly code for the final product.

The controller is a MC68HC705C8A MCU based design complete with numeric keypad and display. The controller is used to access, read and set the internal registers of the baseband IC located on the target, and enable or disable the receiver and transmitter ICs. Additionally, revisions 2.0 and greater of the MCU support a simple data transmission/reception scheme which can be used to investigate low data rate operation.

The target is a MC13145 RF Receiver, MC13146 RF Transmitter, and MC33411 Analog Baseband system. This system supports low–power, FM transmission and reception in the unlicensed (i.e. FCC Part 15) 900 MHz ISM band and contains complete audio processing sections for both transmit and receive paths.

Additional literature, including the MC33411A/D or MC33410A/D, MC13145/D and MC13146/D data sheets, and AN1687/D and AN1691/D application notes should be consulted in conjunction with this manual. Please refer to the schematics, parts lists, and assembly diagrams at the end of this manual for additional detailed information.

GETTING STARTED: CONTROLLER

The controller requires a 5.0 V power supply to operate the LCD display and a 3.0 to 5.5 V supply to operate the MCU. Since the MCU is specified to operate at about 2.0 MHz at lower supplies and about 4.0 MHz at higher supplies, it is recommended that the controller be operated at 5.0 V only.

Power and ground to the LCD display are connected to J1/J2, respectively, and power/ground for the MCU is connected to JP1, pins 1 and 2, respectively. Under normal operating conditions, the target will supply the MCU power requirements through a ribbon cable connected to this header.

If the target is a MC33411 based system, jumper J3 should be removed. If the target is labeled “Baseset”, jumper J5 should be installed. If the target is labeled “Handset”, jumper J5 should be removed. Jumper J6 can be used to reset the MCU, but should be removed for normal operation.

The controller’s MCU system clock can either be provided by the target or by an on–board crystal. In general, it is recommended that the on–board crystal be used for prototyping and debugging purposes. If the on–board crystal will be used, jumpers J7 and J9 should be installed and jumper J8 removed. If the target will supply the MCU system clock, remove jumpers J7 and J9 and install jumper J8.

Trimpot R1 is used to adjust the LCD contrast for best readability. If the LCD appears blank, the trimpot should be adjusted counterclockwise. If the LCD appears too dark, adjust the trimpot in the clockwise direction.

The 10–pin, 1:1 ribbon cable supplied with the system should be connected from JP1 of the controller to JP1 of the target before power is applied to either board.

GETTING STARTED: TARGET

The target requires a 2.7 to 5.5 V supply. Since this supply is usually used to power the controller MCU, it should be limited to 3.0 to 5.5 V, and it is recommended that 5.0 V be used. Power and ground are connected to J4 and J5, respectively.

As shipped, the RF signals to/from the target are presented at the SMA (J3) for ease of connection to standard lab equipment. If actual transmission/reception is desired, connect the antenna supplied to the ANT hole using the nut/bolt and insulated washers provided, and remove C5 and re–solder it in C4’s position. This redirects the matched RF source from the SMA to the ANT connection.

The target is optimized for 9,600 NRZ (4,800 RZ) data applications with no voice. If data will be supplied by the controller or controller emulator, a jumper should be placed between MTX/TXD and another jumper placed between MRX/RXD. If the data source will be to/from external equipment, transmitted data/ground can be connected to TXD and the ground contact located next to him, and received data can be observed at RXD and the ground contact located next to him.

Most data applications will not require the audio processing sections of the baseband IC. If, however, it is desired to use these audio processing sections in the data path, resistor R35 should be removed and a 1.0 μF capacitor should be installed in C121’s position (for received data), C120 should be removed and re–installed in C119’s location, R41 should be removed, and a low value (<51 Ω) resistor placed in R39’s location (for transmit data).

Trimmer capacitor C83 is used to adjust the 10 MHz reference crystal to as close to 10 MHz as possible. Use extreme caution if adjusting this capacitor, as any capacitive load appearing on the Fref test point can affect the reference frequency. Trimpot R40 is used to set the desired transmit peak deviation to a nominal ±40 kHz.

CONTROLLER OPERATION

Once all connections have been made as outlined above, power can be applied to the system. If separate supplies are being used for the controller 5.0 V supply and target V_{CC}, turn the 5.0 V supply on first.

The controller will respond with a short message (YS1CTLR MCU Rx.x), followed by either “Handset” or “Baseset”, depending upon jumper J5’s setting. Next, the baseband device selected will be displayed (i.e. J3). The first register option will then appear. (See Table 2, Register Commands Table).

Once this sequence is complete, the keypad is used to scroll up or down through the register commands until the desired command is reached. The “#” key will scroll down and the “*” key will scroll up. The “0” key can be depressed to read the contents of the current register. Pressing the “*” or “#” keys will return the menu back to the previous register command. Entering any digit will begin entry of a new value to download to the device. The controller uses/displays Base 10 values.

When a new value has been entered, the “*” key can be depressed to abort the download, or the “#” key can be depressed to download the value to the baseband IC. If the value is within the baseband’s acceptable range, the message “Download done!” will be briefly displayed, and the menu will return to the original register selected. If the value is out of range, the message “Error!! Too big!” will be displayed, and the download will be aborted.

Using these features, all of the individual functions associated with the baseband can be observed and modified, if desired. The user should refer to the baseband register map found in the respective baseband data sheet for additional information about these functions.

The baseband transmit, receive, 2nd LO PLL and internal reference counters are initialized to channel 2 operation (see Table 1, Channel Frequencies Table) upon power–up.

TARGET OPERATION

The RFMOD2 target is arbitrarily referred to as either a “Baseset” or “Handset” unit, and is optimized to receive and transmit on opposite ends of the 900 MHz ISM band. Baseset units can only communicate with handset units, and vise versa.

The target is designed specifically for medium data rate applications, and is useful as configured to observe data communications from about 1,200 Bits/S to about 9,600 Bits/S if Manchester encoding is used. Audio path components have been installed, and audio applications can be investigated but require several modifications to the transmitter (peak deviation), receiver (bandwidth and demodulator/detector), and baseband (PLL filters). Of course, the controller will have to set and modify the baseband registers for proper and acceptable audio performance.

DATA MODE

Controller command #47 may be used to transfer a data byte to another receiving controller. A seven–bit data byte is transmitted as a start bit, data byte (LSB to MSB), odd parity bit, and stop bits. Prior to the start of the transmission, a preamble of zeros is transmitted to allow the receiver and transmitter to stabilize.

Controller command #48 is used to place the receiving controller in the data capture mode. This should be executed prior to transmitting the data. The message ”Waiting for data” will be displayed once this command has been entered.

Five types of errors can occur with the receiver:

3. The preamble is not properly detected and the receiver will not acknowledge the data transfer. The ”*” (i.e., escape) key can be depressed to abort the receive operation and the receiver will display ”Rx Data Aborted!”.
4. The preamble has initialized the receiver but a pulse of too short a duration is detected. The receiver will display ”Timing Err Short”.
5. The preamble has initialized the receiver but a pulse of too long a duration is detected. The receiver will display ”Timing Err Long”.
6. An even parity byte is detected. The receiver will display ”Parity Error!”.
7. A framing error is detected, usually caused by the absence of the stop bit. The receiver will display ”Framing error!”.

GENERAL INFORMATION

With a careful study of the RFMOD2 design, the user will see that the system is very flexible and able to operate under many different conditions. Ultimately, each user’s individual requirements will have to be factored into a final design, and should include considerations such as channel spacing, image rejection, bandwidth, frequency band, tuning range, etc. The system, by its nature, has not been optimized for any one application but rather to be more general purpose in nature and as a vehicle for fast evaluation of the RF chipset and easy of prototyping.

Table 1. Channel Frequencies Table

Ch #	Baseset Tx (MHz)	Baseset Rx (MHz)	Handset Tx (MHz)	Handset (MHz)Rx
0	903.0	924.9	924.9	903.0
1	903.5	925.4	925.4	903.5
2	904.0	925.9	925.9	904.0
3	904.5	926.4	926.4	904.5
4	905.0	926.9	926.9	905.0

SYSTEM CHARACTERISTICS

Transmitter:

- Transmission Type: FM
- Data Modulation: FSK
- Normal Baseset Operating RF Frequency Range: 904 MHz
- Normal Handset Operating RF Frequency Range: 926 MHz
- Tuning Sensitivity: 13 MHz/V, 0.5 to 2.5 V range
- Modulation Sensitivity: ±50 kHz @ –10 dBv
- RF Output Power: –3.0 to –1.0 dBm

Receiver:

- Normal Baseset Operating RF Frequency Range: 926 MHz
- Normal Handset Operating RF Frequency Range: 904 MHz
- 12 dB SINAD Sensitivity: –110 dBm
- 20 dB SINAD Sensitivity: –106 dBm
- 1st LO Tuning Sensitivity: 15 MHz/V, 0.5 to 2.5 V range
- Normal Baseset 1st LO Frequency: 999.7 MHz
- Normal Handset 1st LO Frequency: 977.7 MHz
- 1st IF Frequency: 73.7 MHz
- 2nd LO Frequency: 63 MHz
- 2nd IF Frequency: 10.7 MHz
- 2nd IF Bandwidth: 150 kHz
- Recovered Audio: –10 dBV for ±40 kHz Deviation

Baseband:

- 2nd LO Frequency: 63 MHz
- 2nd LO Output Voltage: 180 mVpp, 25 Ω Load
- 2nd LO Tuning Sensitivity: 1.1 MHz/V, 0.5 to 2.5 V range
- External Reference Frequency: 10 MHz, crystal controlled
- Internal Reference Frequency: 100 kHz

Table 2. Register Commands Table

No.	Command	No.	Command
1	Set Test Mode	26	Set ALC Disable
2	Set Ref Counter	27	Set Lim Disable
3	Set Tx PD Cur	28	Set Comp Disable
4	Set Rx PD Cur	29	Set Expn Disable
5	Set LO PD Cur	30	Set TxA Disable
6	Set LO Counter	31	Set RxA Disable
7	Set LO2 Cap	32	Set PA Disable
8	Set SCF Counter	33	Set LO Disable
9	Disable Ref Osc	34	Set RxP Disable
10	Set MCU Clk Div	35	Set TxP Disable
11	Disable MCU Clk	36	Set Tx N Counter
12	Set VB Reference	37	Set Tx A Counter
13	Set Tx Gain	38	Set Rx N Counter
14	Set Rx Gain	39	Set Rx A Counter
15	Set DS Invert	40	Set Vol Control
16	Set Comp Low MxG	41	Set Tx Mute
17	Set Sidetone Atn	42	Set Rx Mute
18	Set ALC Gain = 10	43	Set PA Mute
19	Set ALC Gain = 25	44	Set Channel
20	Set Tx Polarity	45	Set Xmtr Enable
21	Set Rx Polarity	46	Set Rcvr Enable
22	Set LO2 Polarity	47	TX DATA (0–127)
23	Set Modulus Mode	48	Receive Data
24	Set DS Disable	49	Read Batt A/D
25	Set A/D Disable	50	Read RSSI A/D

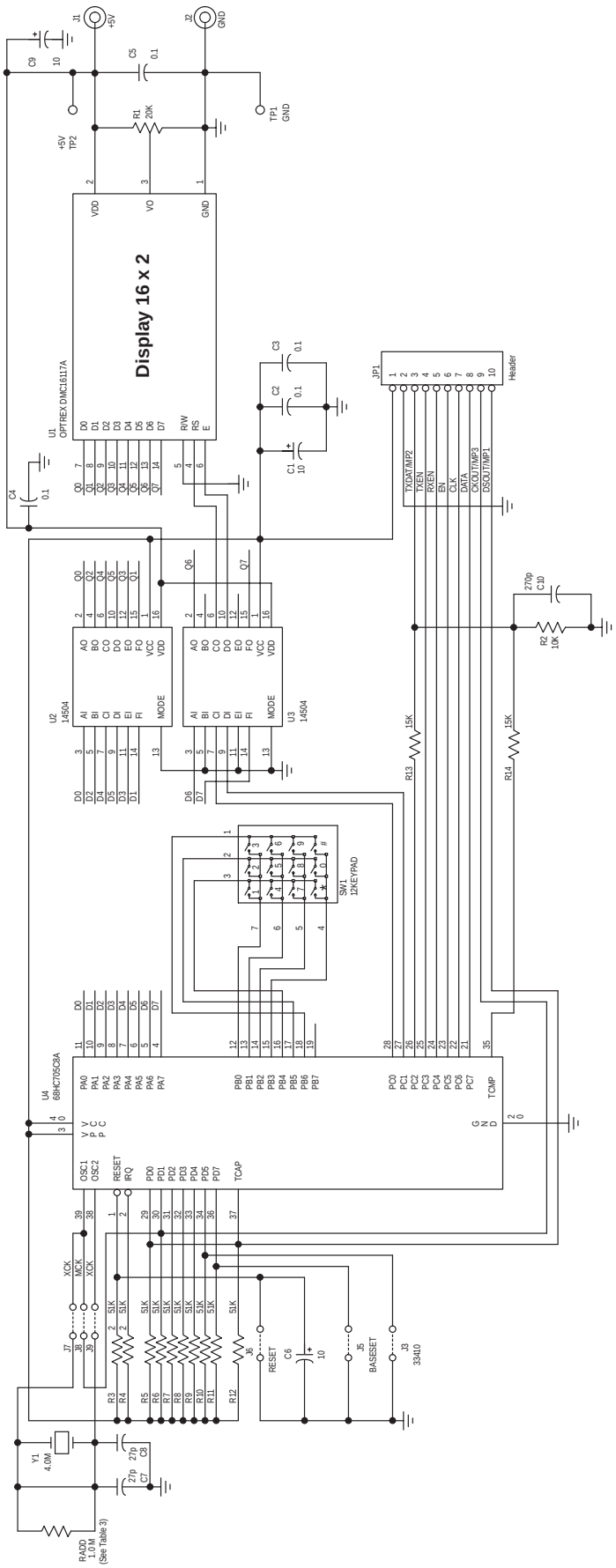


Figure 1. YS1CTRL Schematic

Figure 2. YS1CTRL Component Side

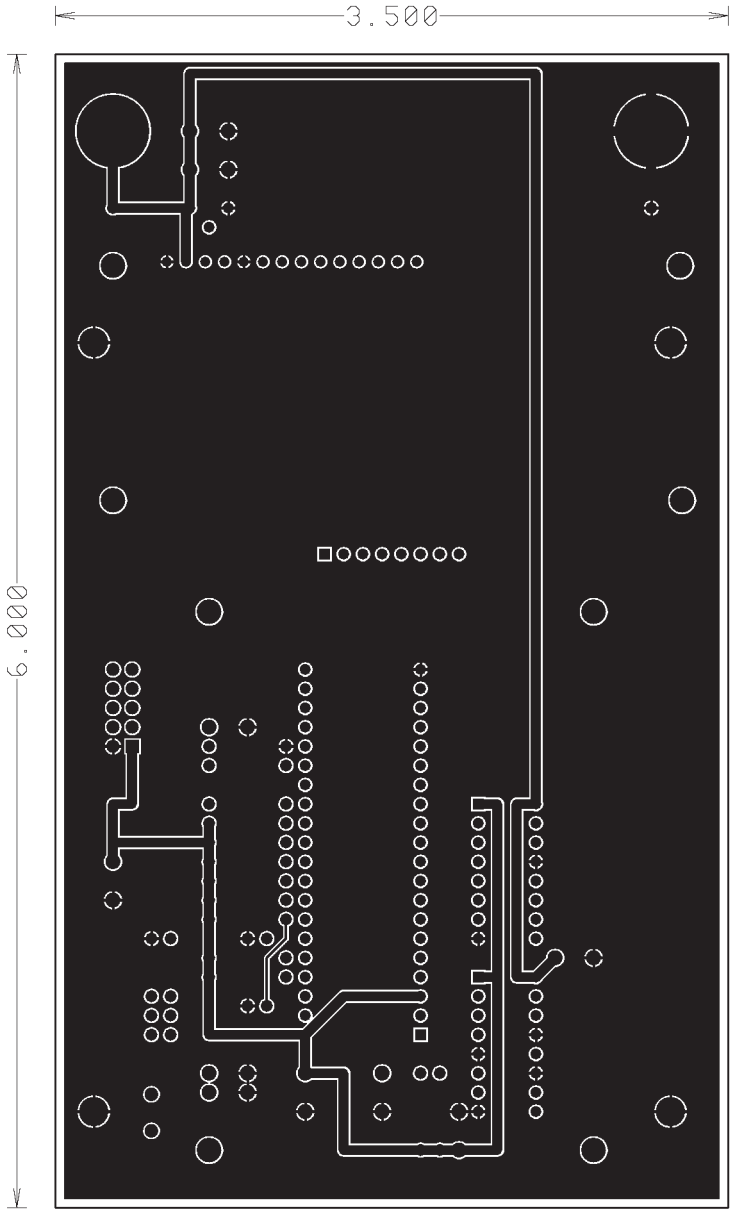


Figure 3. YS1CTRL Solder Side

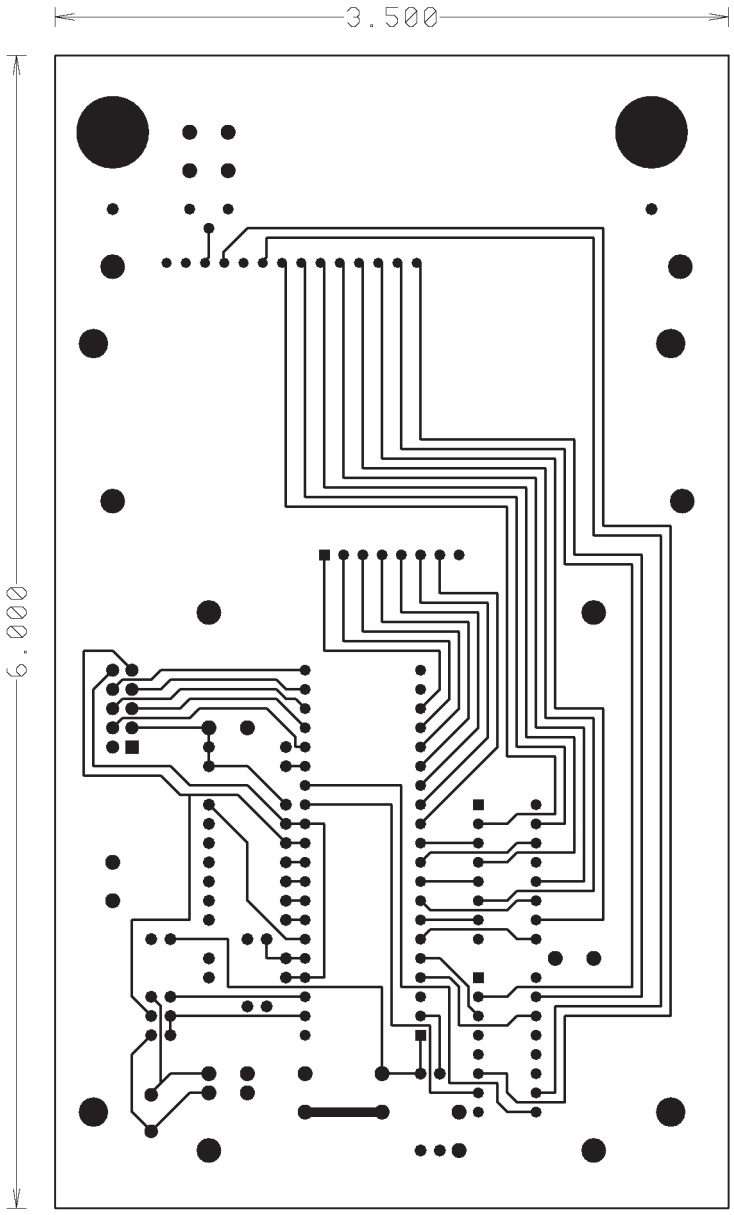


Figure 4. YS1CTRL Assembly

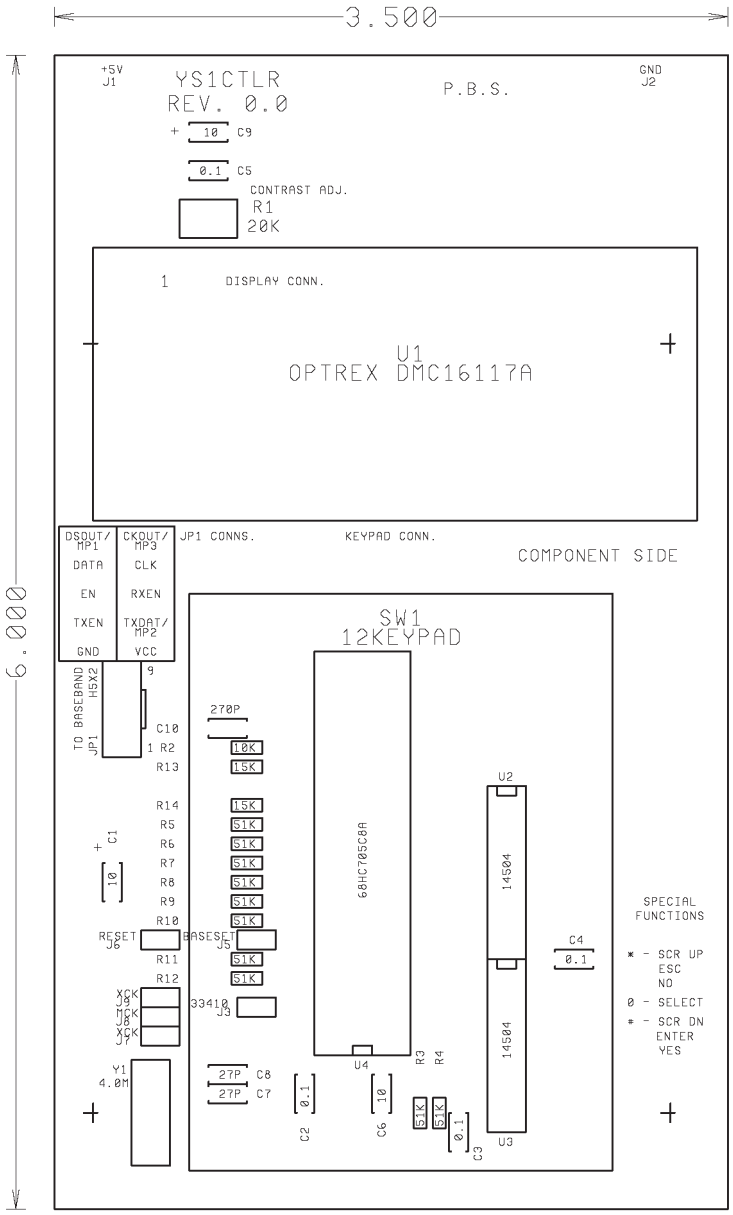


Table 3. YS1CTRL Bill of Materials

Item	Qty	Reference	Part Description
1	3	C1, C6, C9	10 µ, CK05
2	4	C2, C3, C4, C5	0.1 µ, CK05
3	2	C7, C8	27 p, CK05
4	1	C10	270 p, CK05
5	1	–	40 Pin, 600 Mil DIP Socket for U4
6	1	JP1	Sullins, PTC10DAAN
7	1	J1	Johnson Components, 108–0902–001
8	1	J2	Johnson Components, 108–0903–001
9	1	R1	Clarostat, 364–20K, Contrast Adjust
10	1	R2	10 k, RC05
11	10	R3, R4, R5, R6, R7, R8, R9, R10, R11, R12	51 k, RC05
12	2	R13, R14	15 k, RC05
13	1	SW1	C&K, 4A01T322NCFQ
14	1	U1	Optrex, DMC–16117A
15	2	U2, U3	Motorola, MC14504BCP
16	1	U4	Motorola, MC68HC705C8AP
17	1	Y1	Raltron, A–4.000–18, use insulated washer
18	1	RADD	1.0 M, 0603, Add on where shown in Figure 1.

Figure 5. RFMOD2 Transceiver Block Diagram

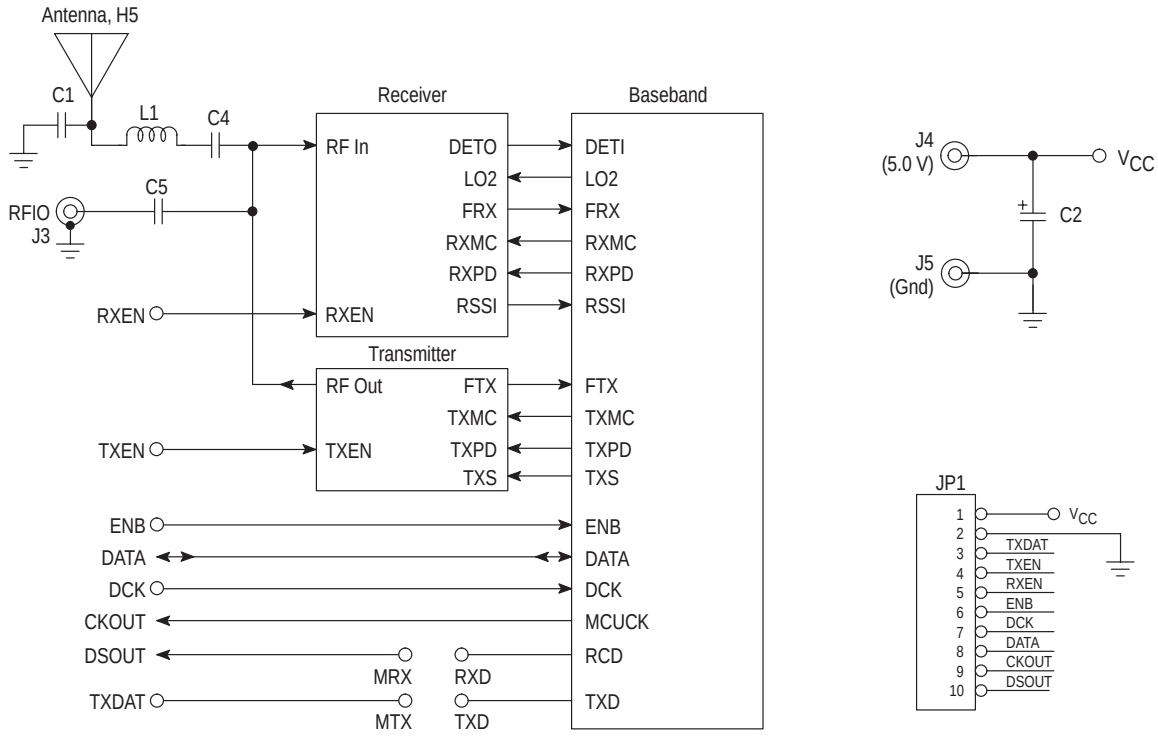


Figure 6. RFMOD2 Baseband

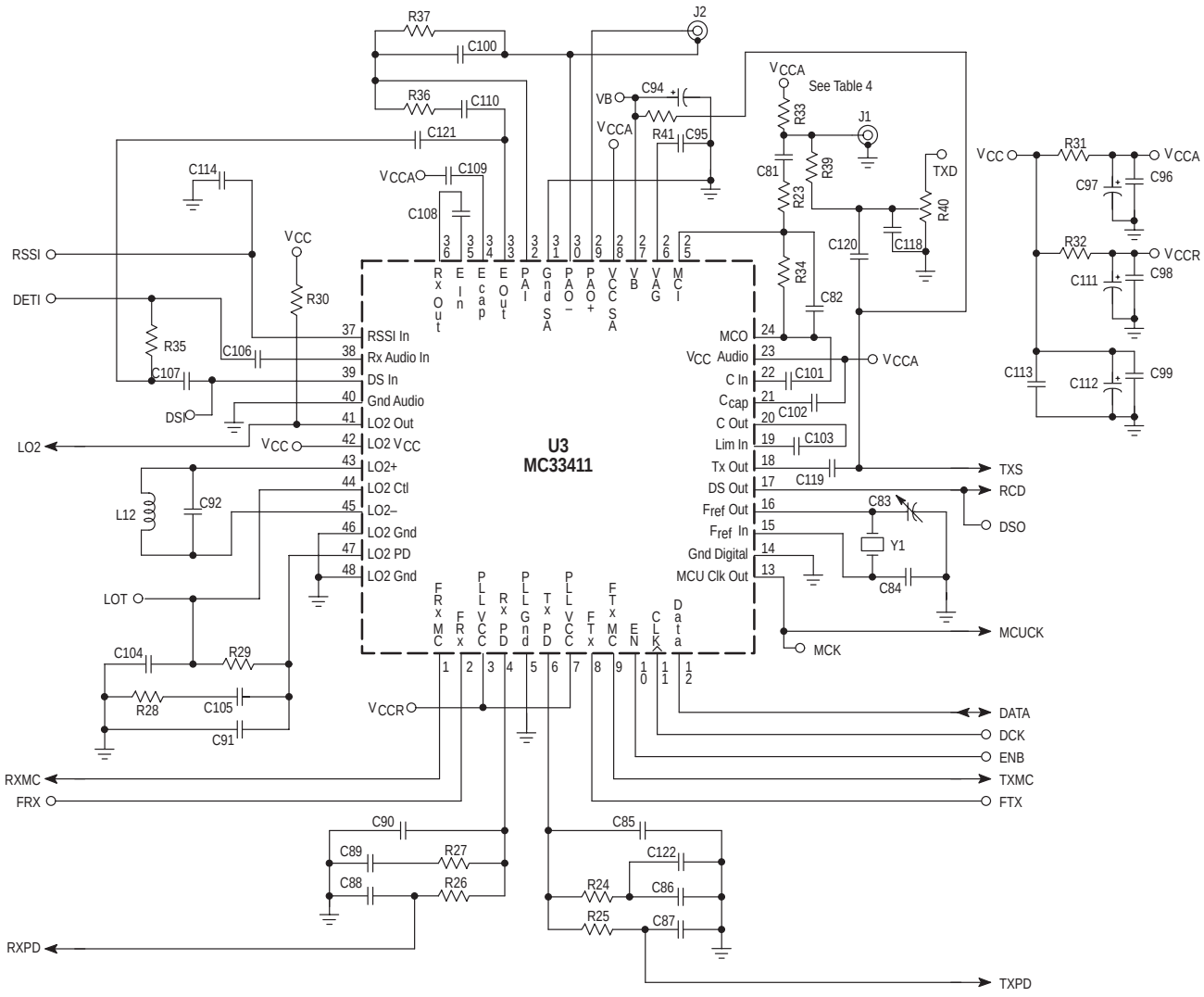


Figure 7. RFMOD2 Receiver

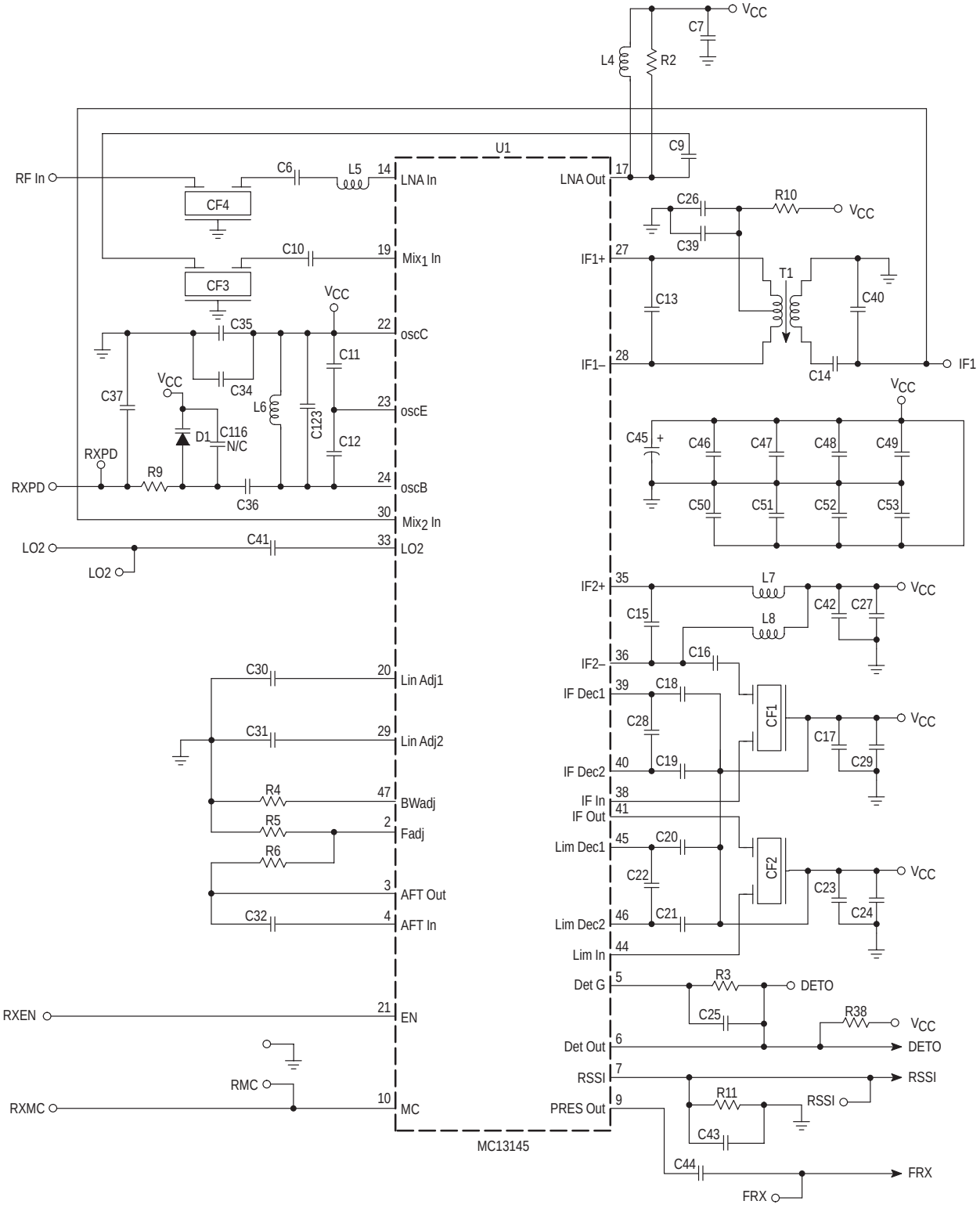


Figure 8. RFMOD2 Transmitter

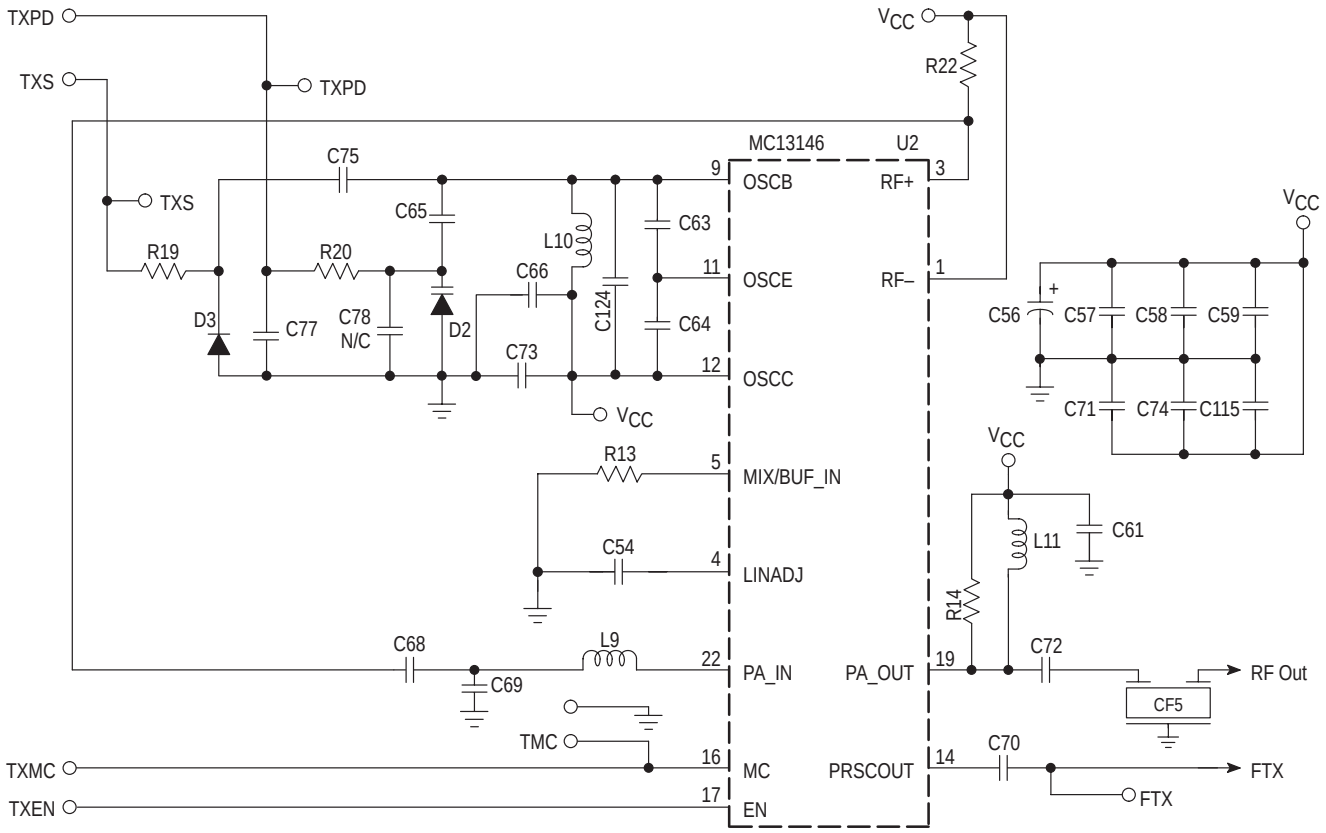


Figure 9. RFMOD2 Component Side Baseset
(Handset not shown)

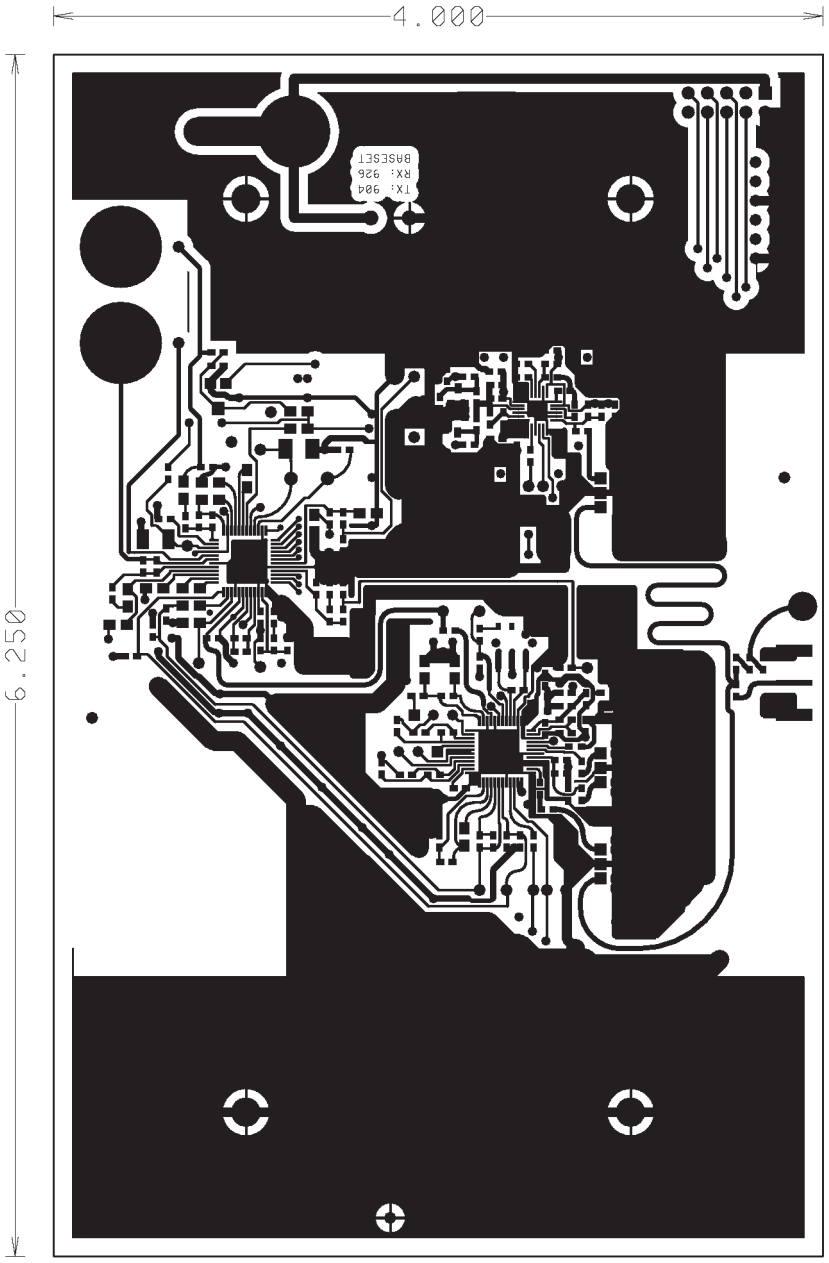


Figure 10. RFMOD2 Ground Plane

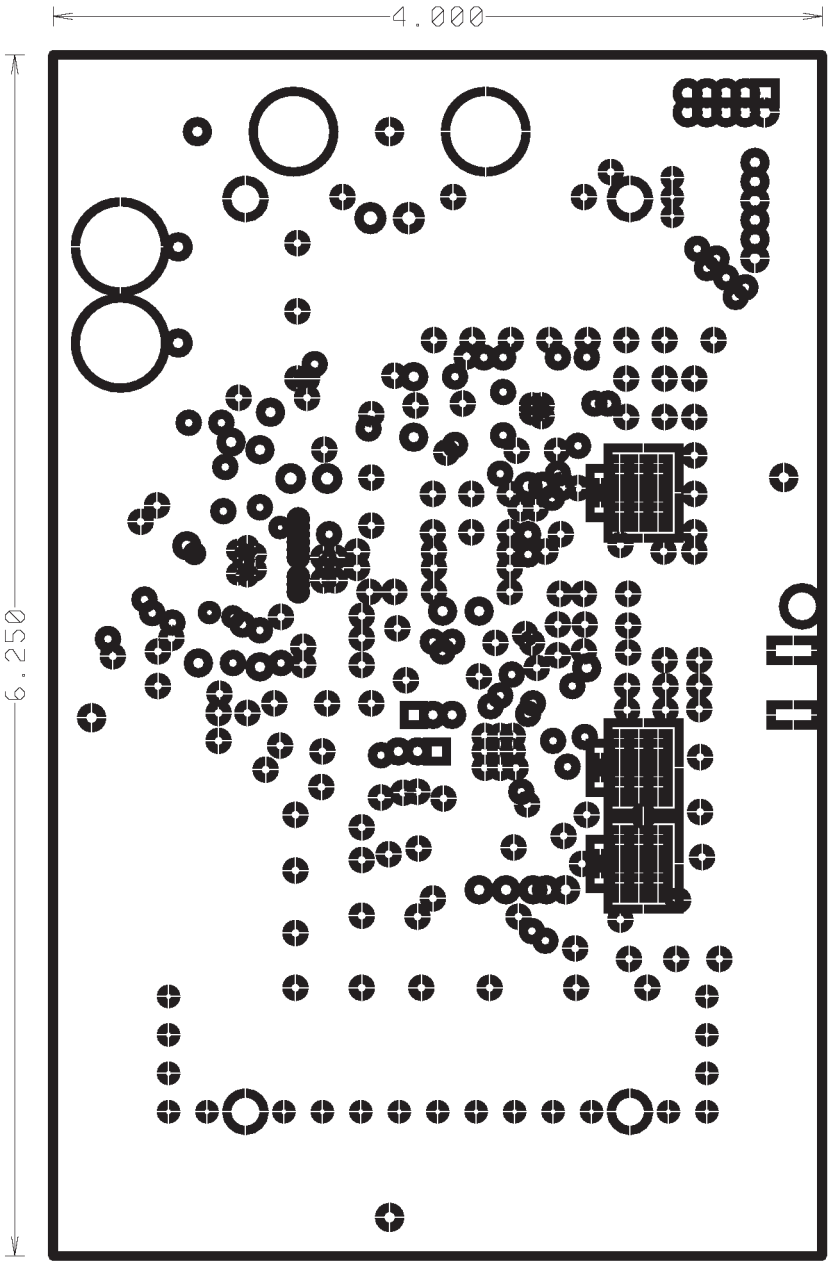


Figure 11. RFMOD2 Power Plane

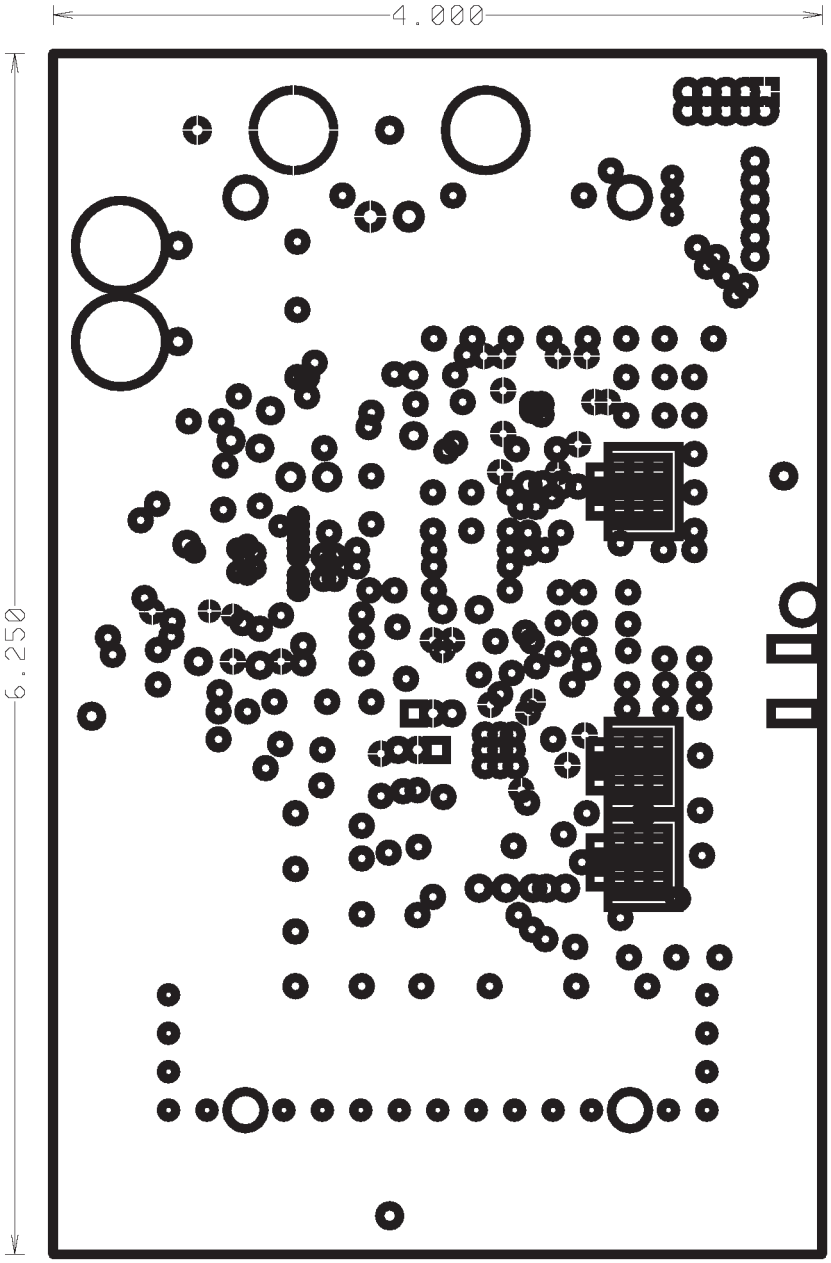


Figure 12. RFMOD2 Solder Side

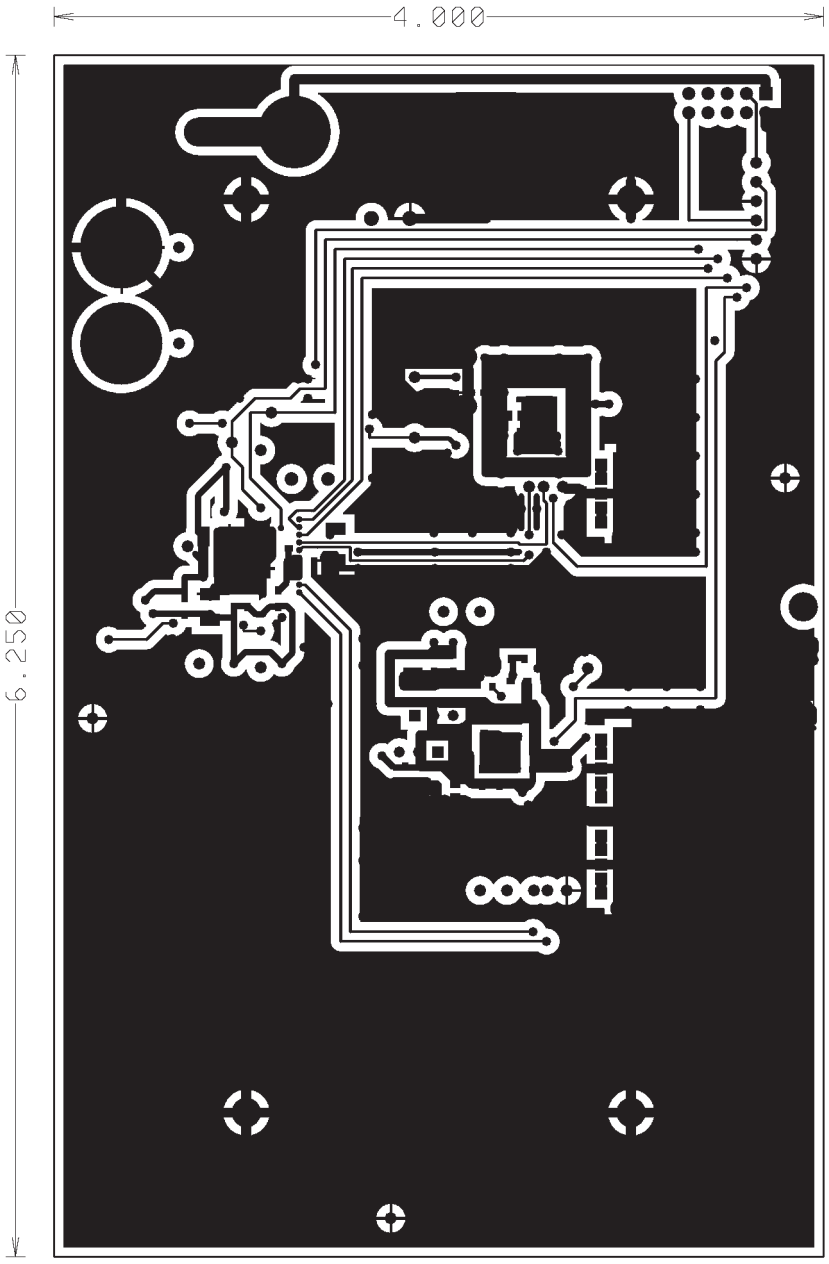


Figure 13. RFMOD2 Component Side Assembly

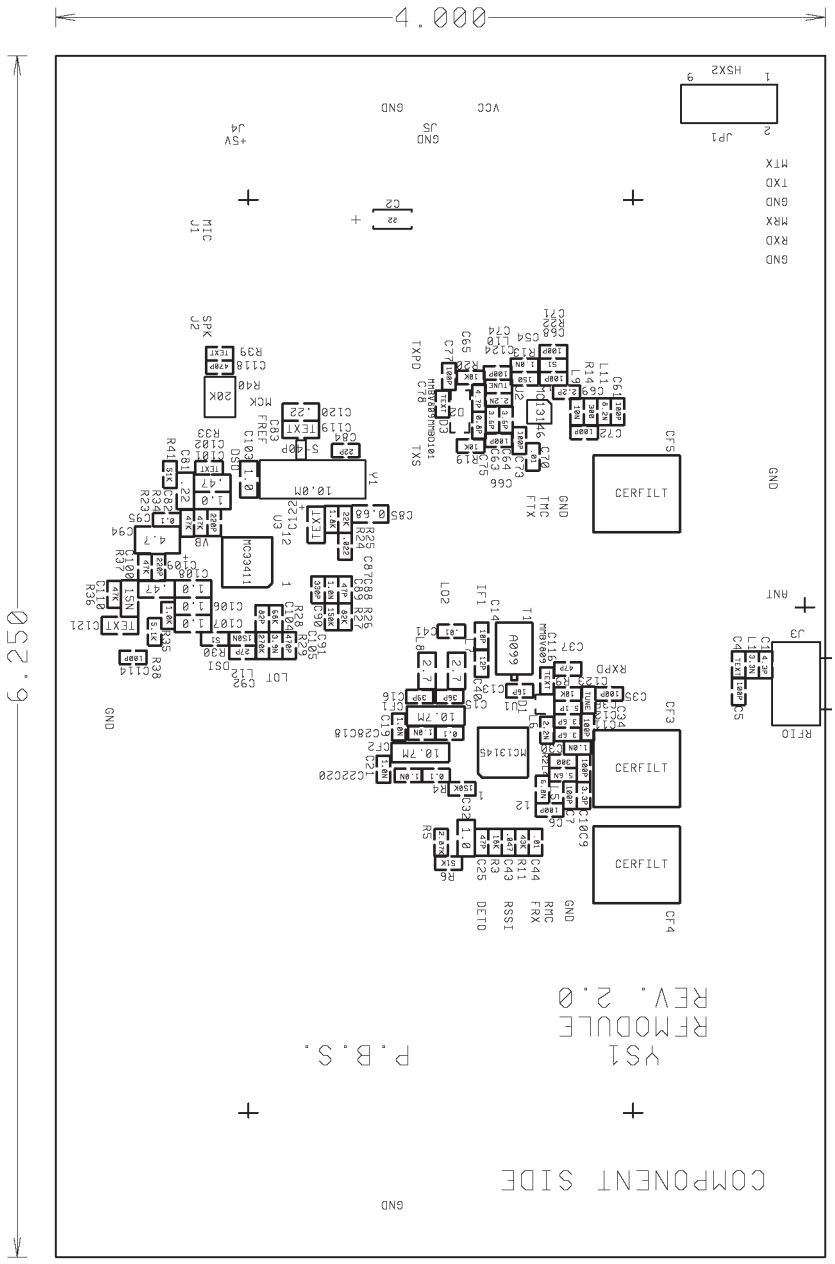


Figure 14. RFMOD2 Solder Side Assembly

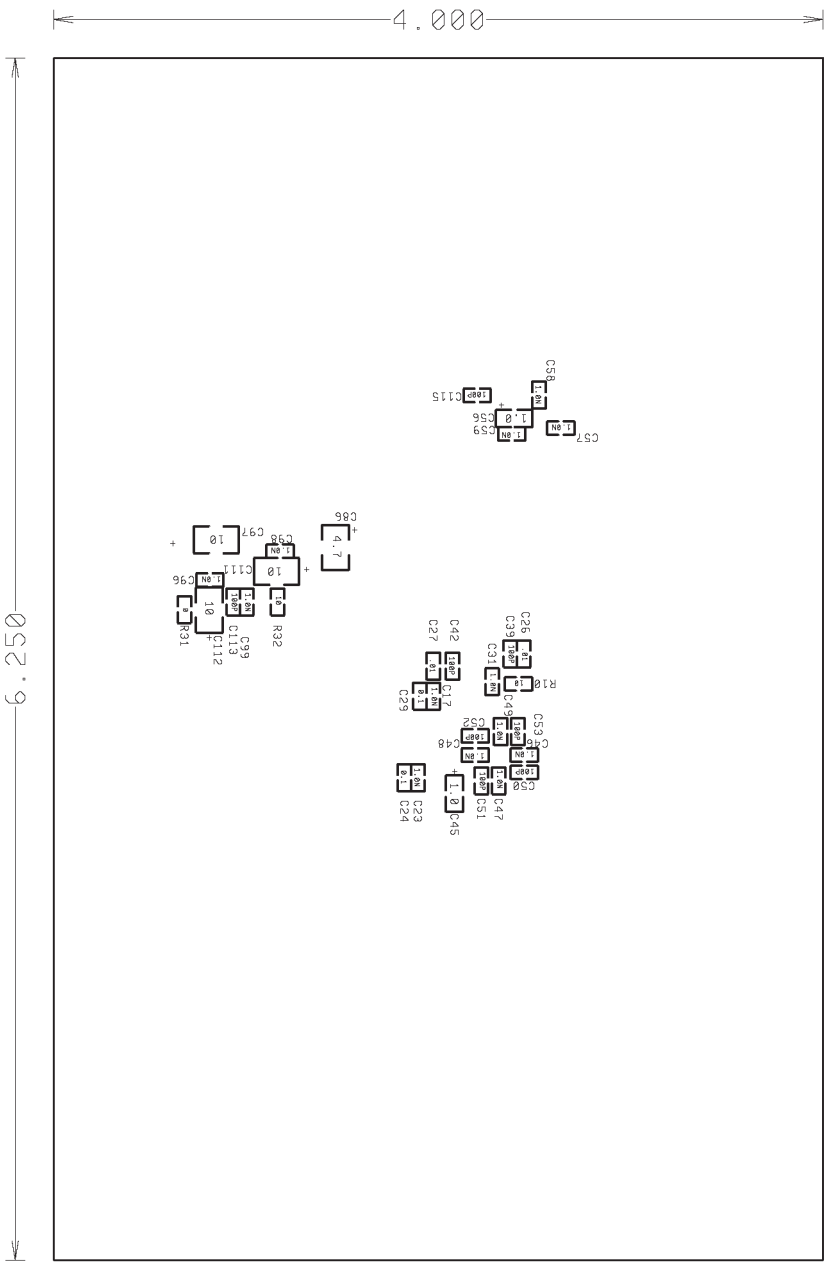


Table 4. RFMOD2 Bill of Materials

Item	Qty	Reference	Part Description
1	2	CF1, CF2	10.7 Mm CFSK Series, CK107M4–AE–20X, Toko
2	2	CF4, CF3	Cerfilt, H–CF6118702/B–CF6118902, TDK
3	1	CF5	Cerfilt, B–CF6118702/H–CF6118902, TDK
4	1	C1	4.3 p, 0603
5	1	C2	22 µ, CK05
6	4	C4, C78, C116, R39	See text, 0603, C78 & C116 are no component
7	23	C5, C6, C7, C10, C34, C35, C39,C42,C50, C51, C52, C53, C61, C66, C68, C71, C72, C73, C74, C77, C113, C114, C115	100 p, 0603
8	1	C9	3.3 p, 0603
9	4	C11, C12, C63, C64	3.6 p, 0603
10	1	C13	16 p, 0603
11	1	C14	10 p, 0603
12	1	C15	36 p, 0603
13	1	C16	39 p, 0603
14	20	C17, C18, C19, C20, C21, C23, C30, C31, C46, C47, C48, C49, C54, C57, C58, C59, C89, C96, C98, C99	1.0 n, 0603
15	5	C22, C24, C28, C29, C95	0.1 µ, 0603
16	3	C25, C37, C88	47 p, 0603
17	5	C26, C27, C41, C44, C70	0.01 µ, 0603
18	8	C32, C45, C56, C101, C103, C106, C107, C108	1.0 µ, 0805
19	1	C36	5.1 p, 0603
20	1	C40	12 p, 0603
21	1	C43	0.047 µ, 0603
22	1	C65	4.7 p, 0603
23	1	C69	2.2 p, 0603
24	1	C75	0.8 p, 0603
25	2	C81, C120	0.22 µ, 0805
26	2	C82, C100	220 p, 0603
27	1	C83	5–40 p, 9343–9, Johanson
28	1	C84	27 p, 0603
29	1	C85	0.68 µ, 0805
30	2	C86, C94	4.7 µ, 1210, C86 can be placed in C122’s place
31	1	C87	0.022 µ, 0603
32	1	C90	330 p, 0603
33	2	C91, C118	470 p, 0603
34	1	C92	27 p, 0603
35	3	C97, C111, C112	10 µ, 1210
36	2	C109, C102	0.47 µ, 0805
37	1	C104	82 p, 0603
38	1	C105	3.9 n, 0603
39	1	C110	15 n, 0603

Table 4. RFMOD2 Bill of Materials – (continued)

Item	Qty	Reference	Part Description
40	3	C119, C121, C122	See text, 0805, C122 can be placed in C86's place
41	2	C123, C124	Tuning Cap, H ≈ 1.2 p, B ≈ 0.8 p (C123), H ≈ 3.9 p, B ≈ 4.3 p (C124), 0603
42	2	D1, D2	MMBV809, MMBV809LT1
43	1	D3	MMBD101, MMBD101LT1
44	1	H5	Antenna Hole, HEA–101–EZ–200–00, Toko
45	1	JP1	Header, 5x2
46	1	J1	MIC, 3501FP, Switchcraft
47	1	J2	SPK, 3501FP, Switchcraft
48	1	J3	RFIO, 142–0701–851, EF Johnson
49	1	J4	5.0 V, 108–0902–001, Johnson Components
50	1	J5	GND, 108–0903–001, Johnson Components
51	1	L1	3.3 n, 0603
52	1	L4	5.6 n, 0603
53	1	L5	6.8 n, 0603
54	1	L6, L10	2.2 n, 0603
55	2	L7, L8	2.7 μ, 0805
56	1	L9	10 n, 0603
57	1	L11	8.2 n, 0603
58	1	L12	150 n, 0603
59	2	R2, R14	300, 0603
60	1	R3	18 k, 0603
61	2	R4, R27	150 k, 0603
62	1	R5	2.87 k, 0603
63	2	R6, R41	51 k, 0603
64	3	R9, R19, R20	10 k, 0603
65	2	R10, R32	10, 0603
66	1	R11	43 k, 0603
67	1	R13	150, 0603
68	2	R22, R30	51, 0603
69	4	R23, R34, R36, R37	47 k, 0603
70	1	R24	1.8 k, 0603
71	1	R25	22 k, 0603
72	1	R26	82 k, 0603
73	1	R28	68 k, 0603
74	1	R29	270 k, 0603
75	1	R31	0, 0603
76	1	R33	1.2 k, 0603 – used for Mic Bias and Voice only
77	1	R35	1.0 k, 0603
78	1	R38	5.1 k, 0603
79	1	R40	20 k, ST3A203CT, Phillips
80	1	TP25 thru TP30	Header, 6x1
81	1	T1	A638AN–A099YWN, Toko
82	1	U1	MC13145, MC13145FTA

Table 4. RFMOD2 Bill of Materials – (continued)

Item	Qty	Reference	Part Description
83	1	U2	MC13146. MC13146FTA
84	1	U3	MC33411, MC33411BFTA
85	1	Y1	10 M, A–10.000–18, Raltron

Chapter Four
Frequency Synthesis

Section One 4.1–0
Frequency Synthesis – Selector Guide

Section Two 4.2–0
Frequency Synthesis – Data Sheets

Section One
Selector Guide

Frequency Synthesis

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Frequency Synthesis

Single PLL Synthesizers

Maximum Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Features	Device	Suffix/ Case
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Parallel Interface	MC145151–2	DW/751F
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Parallel Interface, Uses External Dual–Modulus Prescaler	MC145152–2	DW/751F
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Serial Interface	MC145157–2	DW/751G
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Serial Interface, Uses External Dual–Modulus Prescaler	MC145158–2	DW/751G
100 @ 3.0 V 185 @ 4.5 V	2.7 to 5.5	2 @ 3 V 6 @ 5 V	Serial Interface, Auxiliary Reference Divider, Evaluation Kit – MC145170EVK	MC145170–2	P/648, D/751B, DT/948C
1000	2.7 to 5.5	4.25	4–Line Parallel Interface	MC12181	D/751B
1100	2.7 to 5.5	7 @ 5 V	Serial Interface, Standby, Auxiliary Reference Divider, Evaluation Kit – MC145191EVK	MC145193(46a)	F/751J, DT/948D
2000	2.7 to 5.5	4 @ 3 V	Serial Interface, Standby, Auxiliary Reference Device, Evaluation Kit – MC145202EVK	MC145202–1(46a)	F/751J, DT/948D
2500	2.7 to 5.5	9.5	Serial Interface	MC12210	D/751B, DT/948E
2800	4.5 to 5.5	3.5	Fixed Divider	MC12179	D/751

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

Dual PLL Synthesizers

Maximum Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Phase Detector	Device	Suffix/ Case
60 @ 3.0 V both loops	2.5 to 5.5	3 @ 3 V	Serial Interface, Standby	MC145162	P/648, D/751B
85 @ 3.0 V both loops	2.5 to 5.5	3 @ 3 V	Serial Interface, Standby	MC145162–1	D/751B
550, 60	1.8 to 3.6	3	10 MHz Serial Interface, Multiple Standby Modes, Dual 8–Bit DACs, Voltage Multiplier for Phase Detectors (See Note).	MC145181	FTA/873C
1100 both loops	2.7 to 5.5	12	Serial Interface, Standby, Evaluation Kit – MC145220EVK	MC145220	F/803C, DT/948D
1200, 550	1.8 to 3.6	4	10 MHz Serial Interface, Multiple Standby Modes, Dual 8–Bit DACs, Voltage Multiplier for Phase Detectors (See Note).	MC145225	FTA/873C
2200, 550	1.8 to 3.6	5	10 MHz Serial Interface, Multiple Standby Modes, Dual 8–Bit DACs, Voltage Multiplier for Phase Detectors (See Note).	MC145230	FTA/873C

NOTE: The MC145230EVK development system may be used with the MC145181, MC145225, or MC145230. The MC145230 is soldered to a tested board; MC145181, MC145225 and MC145230 device samples are included. The user must supply the VCOs for the MC145181.

PLL Building Blocks

Prescalers

Frequency (MHz)	Divide Ratios	Single or Dual Modulus	Supply Voltage (V)	Supply Current (mA)	Features	Device	Suffix/ Case
1100	64/65, 128/129	Dual	2.7 to 5.5	2.0 max	Low Power	MC12052A	D/751
1100	64/65, 128/129	Dual	2.7 to 5.5	2.5 max	Low Power, Standby	MC12053A	D/751
1100	126/128, 254/256	Dual	2.7 to 5.5	2.0 max	Low Power	MC12058	D/751
1100	10,20,40,80	Single	4.5 to 5.5	5.0 max		MC12080	D/751
1100	2, 4, 8	Single	2.7 to 5.5	4.5 max	Standby	MC12093	D/751
2000	64/65, 128/129	Dual	2.7 to 5.5	2.6 max	Low Power	MC12054A	D/751
2500	2, 4	Single	2.7 to 5.5	14 max	Standby	MC12095	D/751
2800	64, 128, 256	Single	4.5 to 5.5	11.5 max		MC12079	D/751
2800	64, 128	Single	4.5 to 5.5	14.5 max		MC12089	D/751

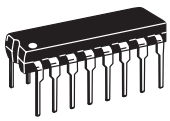
Voltage Control Oscillators

Frequency (MHz)	Supply Voltage (V)	Features	Device	Suffix/ Case
1300	2.7 to 5.5	Two high drive open collector outputs (Q, QB), Adjustable output amplitude, Low drive output for prescaler	MC12149	D/751

Phase–Frequency Detectors

Frequency (MHz)	Supply Voltage (V)	Features	Device	Suffix/ Case
800 (Typ)	4.75 to 5.5	MECL10H compatible	MCH12140	D/751
800 (Typ)	4.2 to 5.5	100K ECL compatible	MCK12140	D/751

RF/IF Integrated Circuits Packages



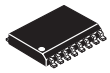
CASE 648
P SUFFIX
(DIP–16)



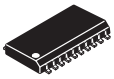
CASE 751
D SUFFIX
(SO–8)



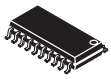
CASE 751B
D SUFFIX
(SO–16)



CASE 751G
DW SUFFIX
(SO–16W)



CASE 751J
F SUFFIX
(SO–20)



CASE 803C
F SUFFIX
(SO–20)



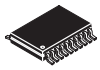
CASE 873C
FTA SUFFIX
(LQFP–32)



CASE 948C
DT SUFFIX
(TSSOP–16)



CASE 948D
DT SUFFIX
(TSSOP–20)



CASE 948E
DT SUFFIX
(TSSOP–20)

Section Four

Frequency Synthesis – Data Sheets

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MOTOROLA

MC12015
MC12016
MC12017

Dual Modulus Prescaler

The MC12015, MC12016 and MC12017 are dual modulus prescalers which will drive divide by 32 and 33, 40 and 41, and 64 and 65, respectively. An internal regulator is provided to allow these devices to be used over a wide range of power–supply voltages. The devices may be operated by applying a supply voltage of 5.0 Vdc ±10% at Pin 7, or by applying an unregulated voltage source from 5.5Vdc to 9.5 Vdc to Pin 8.

- 225 MHz Toggle Frequency
- Low–Power 7.5 mA Maximum at 6.8 V
- Control Input and Output Are Compatible With Standard CMOS
- Connecting Pins 2 and 3 Allows Driving One TTL Load
- Supply Voltage 4.5 V to 9.5 V

NOT RECOMMENDED FOR NEW DESIGN
DEVICES TO BE PHASED OUT.
For the MC12015 and MC12016 no replacement available.
For the MC12017 consider MC12054A for New Designs.

MECL PLL COMPONENTS
DUAL MODULUS PRESCALER

SEMICONDUCTOR
TECHNICAL DATA

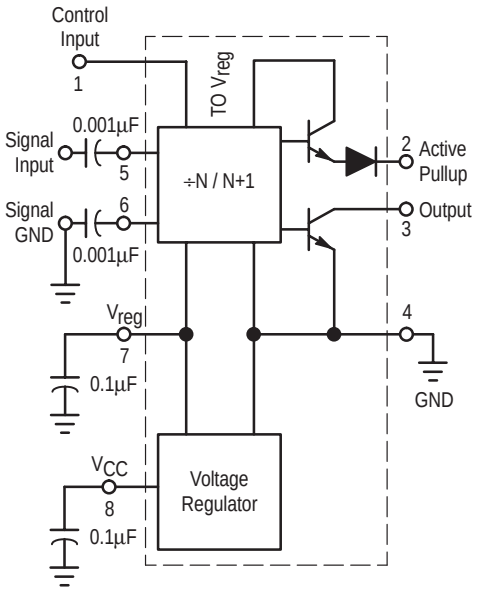


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12015D	T_A = –40 to 85°C	SO–8
MC12016D		
MC12017D		

SIMPLIFIED BLOCK DIAGRAM



1. V_{reg} at Pin 7 is not guaranteed to be between 4.5 and 5.5V when V_{CC} is being applied to Pin 8
2. Pin 7 is not to be used as a source of regulated output voltage

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Regulated Voltage, Pin 7	V_{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	V_{CC}	10	Vdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +175	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.5 to 9.5 V; V_{reg} = 4.5 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input) f_{max} f_{min}		 225 –	 – –	 – 35	MHz
Supply Current	I_{CC}	–	6.0	7.8	mA
Control Input HIGH (÷32, 40 or 64)	V_{IH}	2.0	–	–	V
Control Input LOW (÷33, 41 or 65)	V_{IL}	–	–	0.8	V
Output Voltage HIGH (I_{source} = 50μA) [Nofe 1]	V_{OH}	2.5	–	–	V
Output Voltage LOW (I_{sink} = 2mA) [Note 1]	V_{OL}	–	–	0.5	V
Input Voltage Sensitivity 35 MHz 50 to 225 MHz	V_{in}	 400 200	 – –	 800 800	mVpp
PLL Response Time [Notes 2 and 3]	t_{PLL}	–	–	t_{out} to 70	ns

NOTES: 1. Pin 2 connected to Pin 3.
2. t_{PLL} = the period of time the PLL has from the prescaler rising output tranistion (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
3. t_{out} = period of output waveform.

MOTOROLA

MC12019

Dual Modulus Prescaler

The MC12019 is a divide by 20 and 21 dual modulus prescaler. It will divide by 20 when the modulus control input is HIGH and divide by 21 when the modulus control input is LOW.

- 225 MHz Toggle Frequency
- Low-Power 7.5 mA Maximum at 5.5 V
- Control Input is Compatible with Standard Motorola CMOS Synthesizers
- Emitter Follower Output

NOT RECOMMENDED FOR NEW DESIGN
DEVICE TO BE PHASED OUT.
No replacement available.

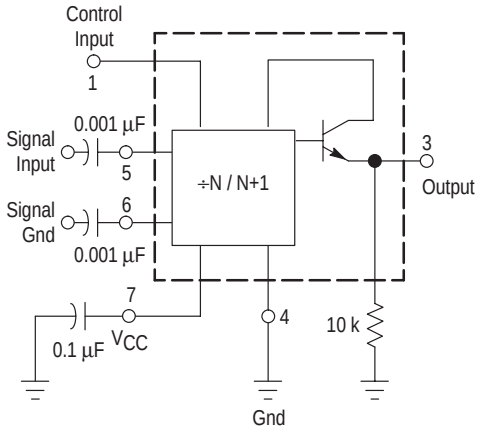
MECL PLL COMPONENTS
÷20/21 DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

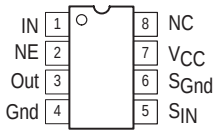


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

SIMPLIFIED BLOCK DIAGRAM



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12019D	T_A = – 40 to 85°C	SO–8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 7	V_{CC}	8.0	Vdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +175	°C

NOTE; ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; T_A = –40 to 85°C), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input) 	f_{max} f_{min}	225 –	– –	– 20	MHz
Supply Current	I_{CC}	–	–	7.5	mA
Control Input HIGH (÷20)	V_{IH}	2.0	–	–	V
Control Input LOW (÷21)	V_{IL}	–	–	0.8	V
Output Swing Voltage (10 kΩ to ground)	V_{out}	600	–	1200	mVpp
Input Voltage Sensitivity 20 MHz to 225 MHz	V_{in}	 200	 –	 800	mV_{PP}
PLL Response Time (Notes 1 and 2)	t_{PLL}	–	–	t_{out}–70	ns

NOTES: 1. t_{PLL} = the period of time the PLL has from the prescaler rising output tranistion (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform.

MOTOROLA

1.1 GHz Dual Modulus Prescaler

MC12026A
MC12026B

MECL PLL COMPONENTS
÷8/9, ÷16/17
DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

The MC12026 is a high frequency, low voltage dual modulus prescaler used in phase–locked loop (PLL) applications.

The MC12026A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

The MC12026B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of an 8/9 or 16/17 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

NOTE: The "B" Version Is Not Recommended for New Designs

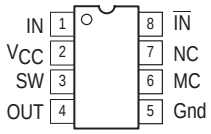
- 1.1 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- Low Power 4.0 mA Typical
- Operating Temperature Range of –40 to 85°C
- The MC12026 is Pin Compatible With the MC12022
- Short Setup Time (t_{set}) 6ns Typical @ 1.1 GHz
- Modulus Control Input Level is Compatible With Standard CMOS and TTL

MC12026A IS NOT RECOMMENDED FOR NEW DESIGN
DEVICE TO BE PHASED OUT.
No replacement available.
MC12026B is on Life Time Buy



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	8
H	L	9
L	H	16
L	L	17

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grouunding this pin, but this is not recommended due to increased power soncumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

MAXIMUM RATINGS

Characteristics	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc
Maximum Output Current, Pin 4	I_O	10.0	mA

NOTE: ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12026AD	T_A =–40 to 85°C	SO–8
MC12026BD		

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5; T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sin Wave)	f_t	0.1	1.4	1.1	GHz
Supply Current Output Unloaded (Pin 2)	I_{CC}	–	4.0	5.3	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC}	V
Modulus Control Input Low (MC)	V_{IL1}	GND	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC} – 0.5 V	V_{CC}	V_{CC} + 0.5 V	V
Divide Ratio Control Input Low (SW)	V_{IL2}	OPEN	OPEN	OPEN	–
Output Voltage Swing (R_L = 560 Ω; I_O = 5.5 mA)[1] (R_L = 1.1 kΩ; I_O = 2.9 mA)[2]	V_{out}	1.0	1.6	–	V_{pp}
Modulus Setup Time MC to Out[3]	t_{SET}	–	6	9	ns
Input Voltage Sensitivity 100–25 0MHz 250–1100 MHz	V_{in}	 400 100	 – –	 1000 1000	mVpp

notes: 1. Divide Ratio of ÷8/9 at 1.1 GHz, C_L = 8.0 pF
2. Divide Ratio of ÷16/17 at 1.1 GHz, C_L = 8.0 pF
3. Assuming R_L = 560 Ω at 1.1 GHz

Figure 1. Logic Diagram (MC12026A)

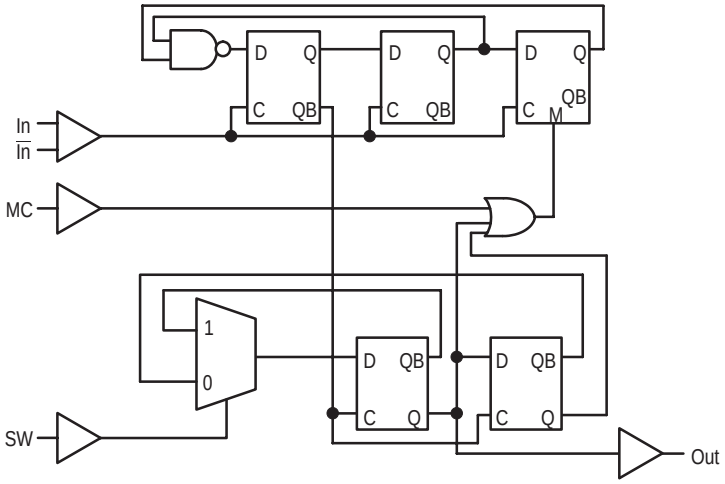
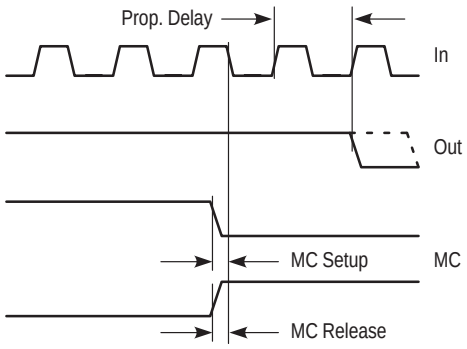


Figure 2. Modulus Setup Time



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. AC Test Circuit

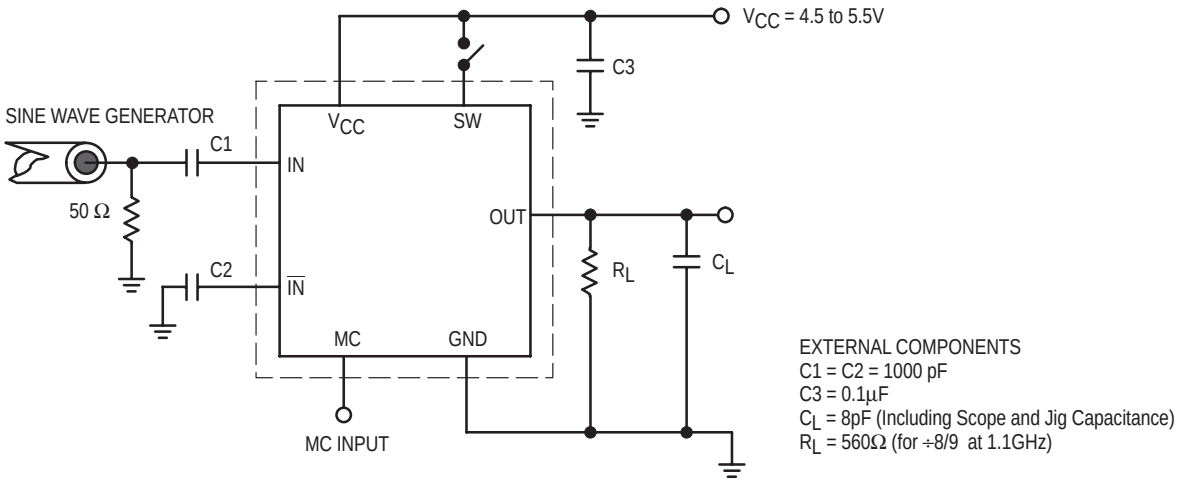
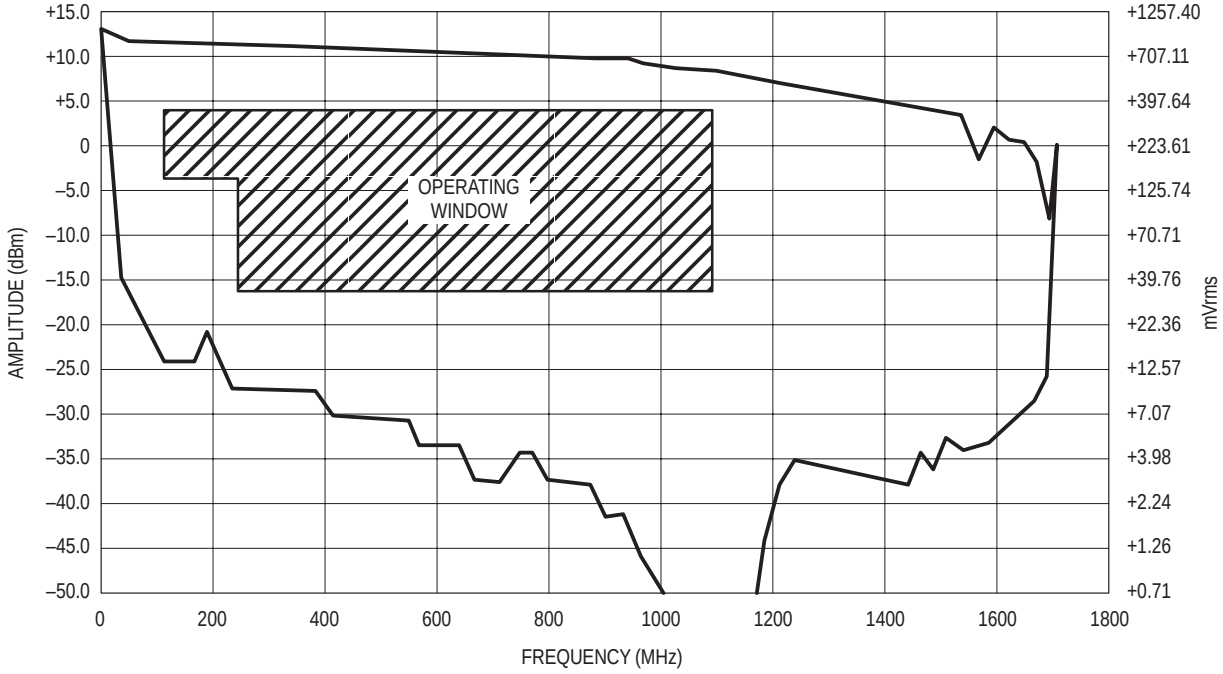


Figure 4. Input Signal Amplitude versus Input Frequency



Divide Ratio = 8; V_{CC} = 5.0 V; T_A = 25°C

Figure 5. Output Amplitude versus Input Frequency

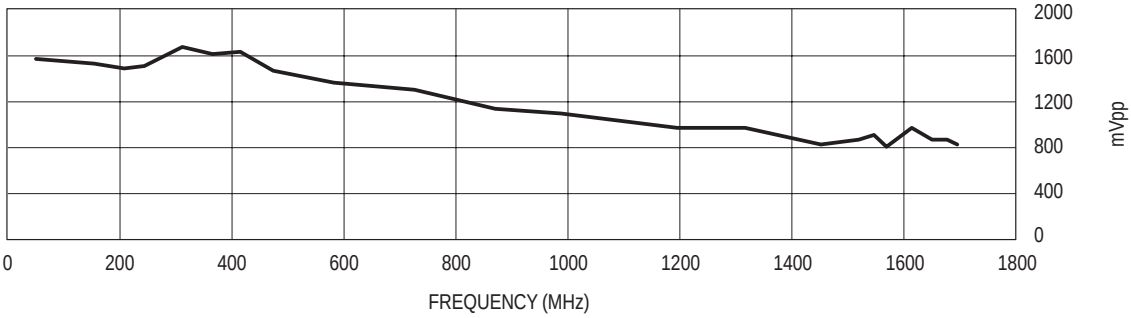
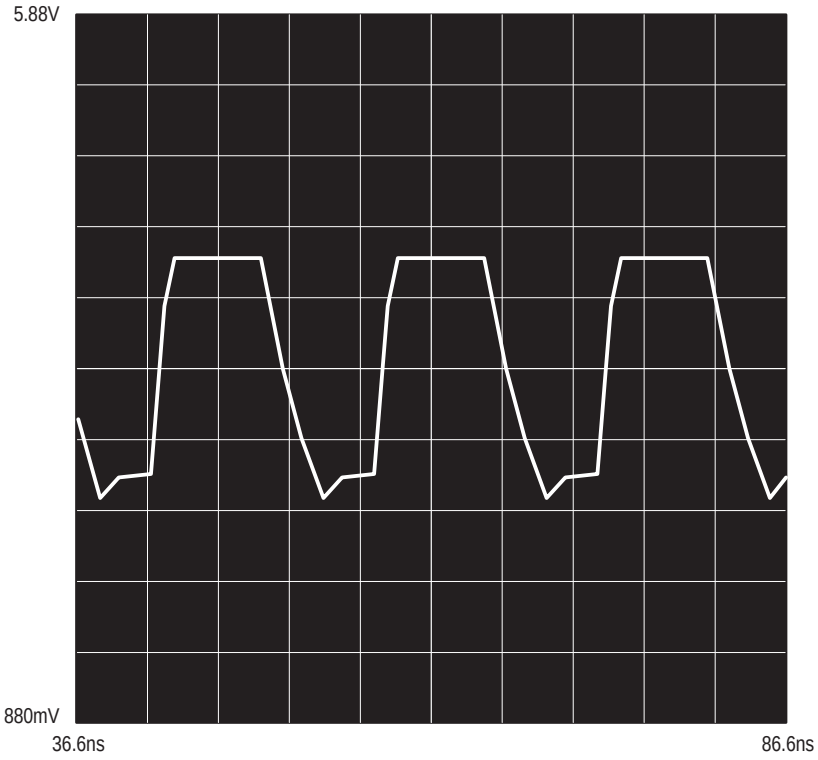
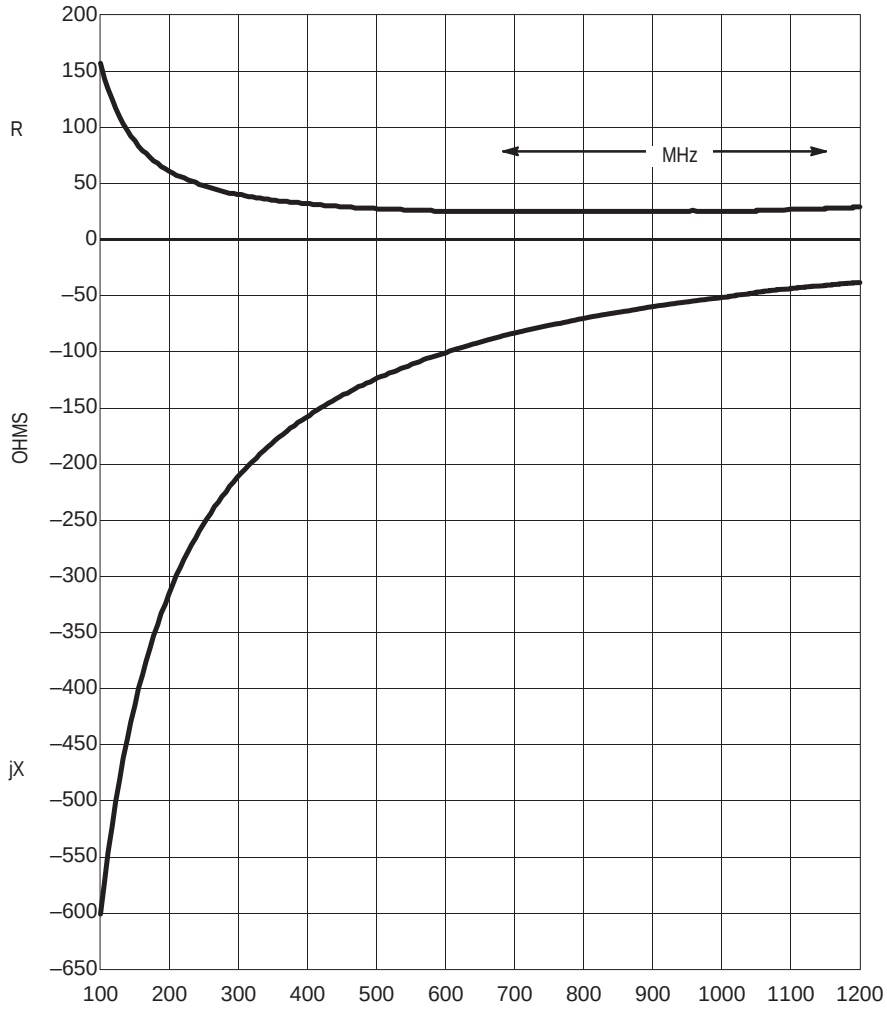


Figure 6. Typical Output Waveform



(÷8, 1.1 GHz Input Frequency, V_{CC} = 5.0, T_A = 25°C, Output Loaded With 8.0pF)

Figure 7. Typical Input Impedance versus Input Frequency



MOTOROLA

MC12038A

1.1 GHz Low Power Dual Modulus Prescaler

MECL PLL COMPONENTS
÷127/128, ÷255/256
DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

The MC12038A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 127/128 or 255/256 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

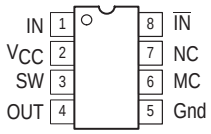
- 1.1 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5 V
- Low–Power 4.8 mA Typical
- Operating Temperature Range of –40 to 85°C
- Short Setup Time (t_{set}) 16ns Maximum @ 1.1 GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL
- On–Chip Output Termination

NOT RECOMMENDED FOR NEW DESIGN
DEVICE TO BE PHASED OUT.
No replacement available.



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	127
H	L	128
L	H	255
L	L	256

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

NOTE: * Equivalent to a two–input NAND gate

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc

NOTE: ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12038AD	T_A = – 40 to 85°C	SO–8

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5V; T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current Output Unloaded (Pin 2) at 5.0 Vdc	I_{CC}	–	4.8	6.5	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC}	V
Modulus Control Input Low (MC)	V_{IL1}	–	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	–
Output Voltage Swing (C_L = 8.0 pF)	V_{out}	1.0	1.6	–	V_{pp}
Modulus Setup Time MC to Out	t_{set}	–	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	$V_{in(min)}$	100 400	– –	1500 1500	mVpp

Figure 1. Logic Diagram (MC12038A)

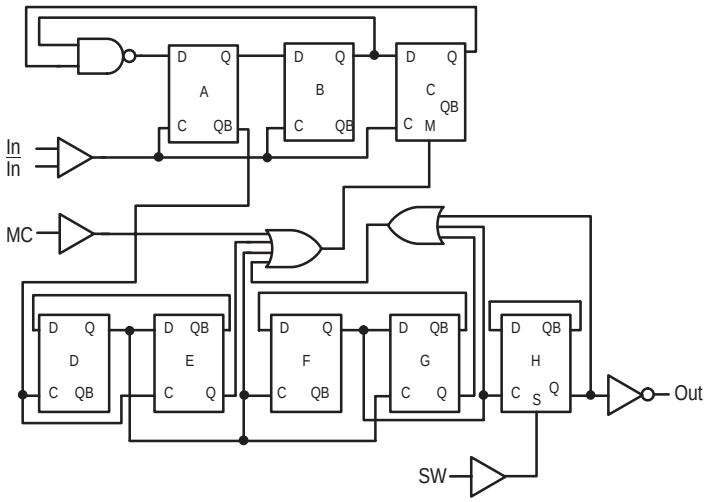
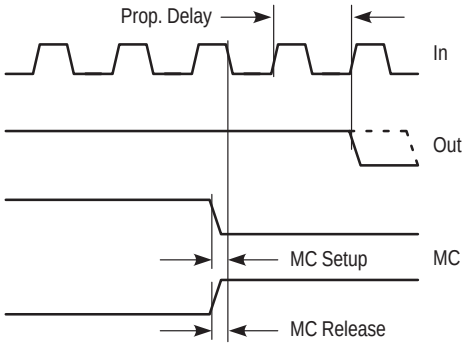
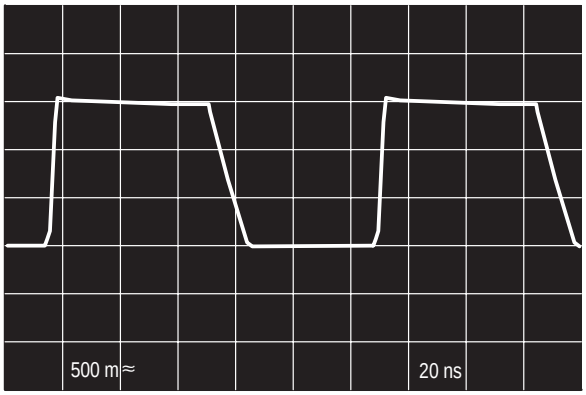


Figure 2. Modulus Setup Time



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. Typical Output Waveforms



(÷128, 1.1 GHz Input Frequency, V_{CC} = 5.0 V, T_A = 25°C, Output Loaded)

Figure 4. AC Test Circuit

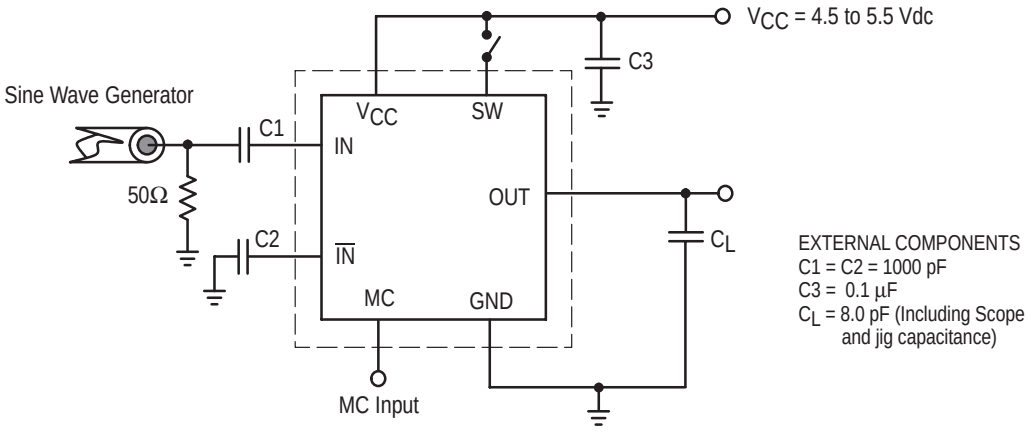
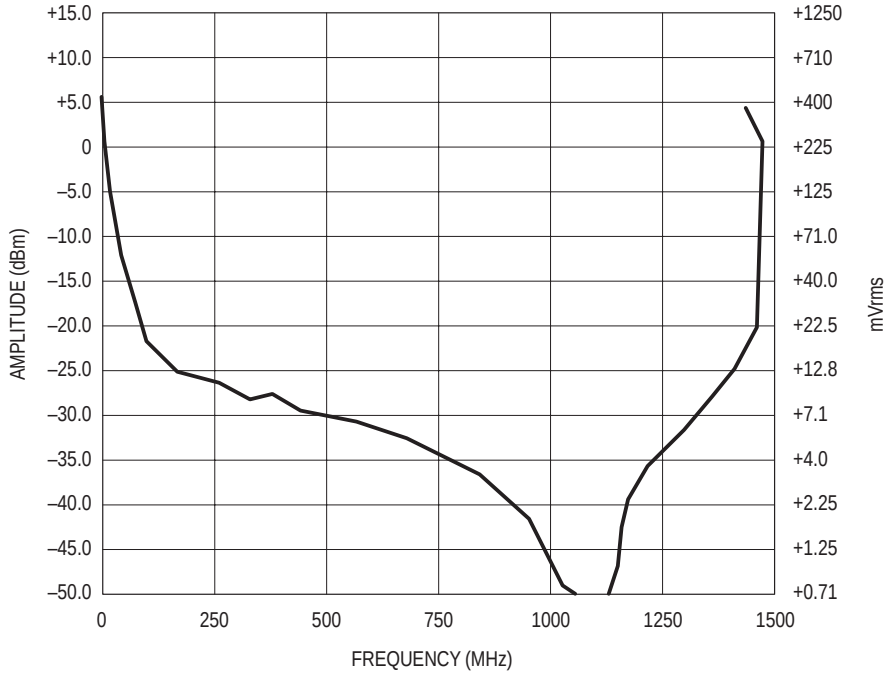


Figure 5. Input Signal Amplitude versus Input Frequency



Divide Ratio = 128; V_{CC} = 5.0 V; T_A = 25°C

Figure 6. Output Amplitude versus Input Frequency

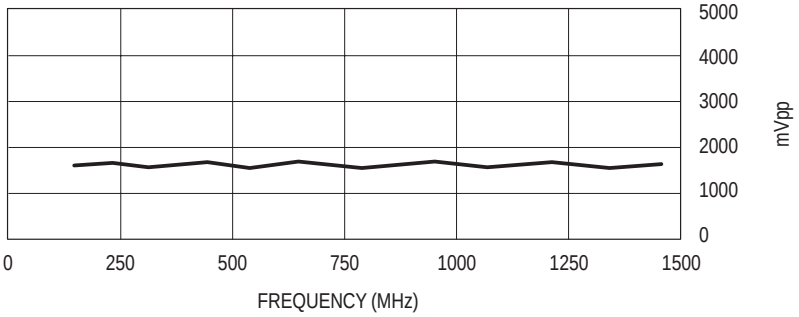
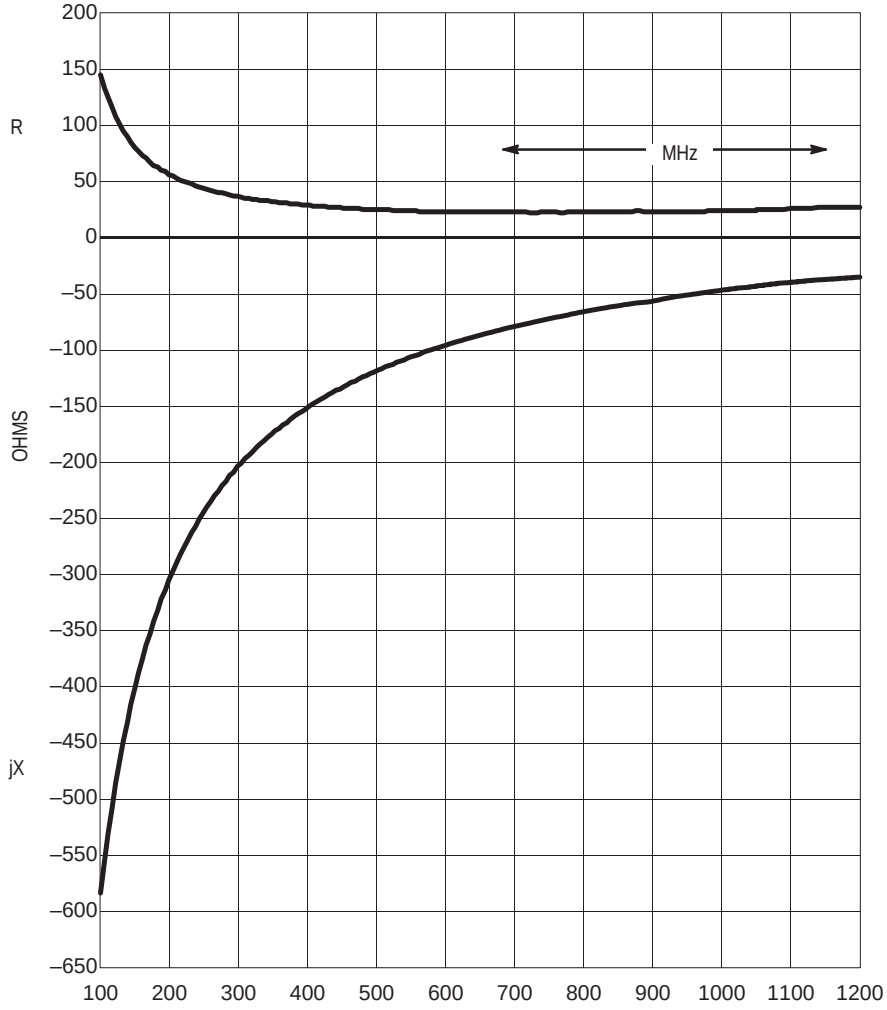


Figure 7. Typical Input Impedance versus Input Frequency



MOTOROLA

MC12052A

1.1 GHz Super Low Power Dual Modulus Prescaler

MECL PLL COMPONENTS ÷64/65, ÷128/129 LOW POWER DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

The MC12052A is a super low power dual modulus prescaler used in phase–locked loop applications. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 2.7 mW at a minimum supply voltage of 2.7 V.

The MC12052A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

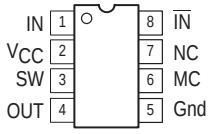
- 1.1 GHz Toggle Frequency
- The MC12052 is Pin and Functionally Compatible with the MC12022
- Low Power 1.0 mA Typical
- 2.0 mA Maximum, –40 to 85°C, V_{CC} = 2.7 to 5.5 Vdc
- Short Setup Time (t_{set}) 16 ns Maximum @ 1.1 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Maximum Input Voltage Should Be Limited to 6.5 Vdc

MOSAIC V is a trademark of Motorola



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12052AD	T_A =–40 to 85°C	SO–8

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 VDC, T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current (Pin 2)	I_{CC}	–	1.0	2.0	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC} + 0.5 V	V
Modulus Control Input Low (MC)	V_{IL1}	Gnd	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC} – 0.5 V	V_{CC}	V_{CC} + 0.5 V	VDC
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	–
Output Voltage Swing (Note 2) (C_L = 8.0 pF, R_L = 3.3 kΩ)	V_{out}	0.8	1.1	–	V_{PP}
Modulus Setup Time MC to Out @ 1100 MHz	t_{set}	–	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	V_{in}	100 400	– –	1000 1000	mV_{PP}
Output Current (Note 1) V_{CC} = 2.7 V, C_L = 8.0 pF, R_L = 3.3 kΩ V_{CC} = 5.0 V, C_L = 8.0 pF, R_L = 7.2 kΩ	I_O	 – –	 0.5 0.5	 3.0 3.0	mA

NOTES: 1. Divide ratio of ÷64/65 @ 1.1 GHz
2. Valid over voltage range 2.7 to 5.5 V; R_L = 3.3 kΩ @ V_{CC} = 2.7 V; R_L = 7.2 kΩ @ V_{CC} = 5.0 V

Figure 1. Logic Diagram (MC12052A)

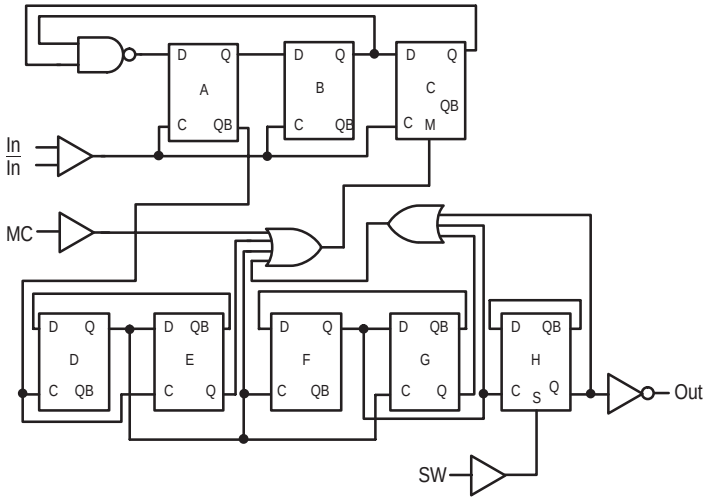
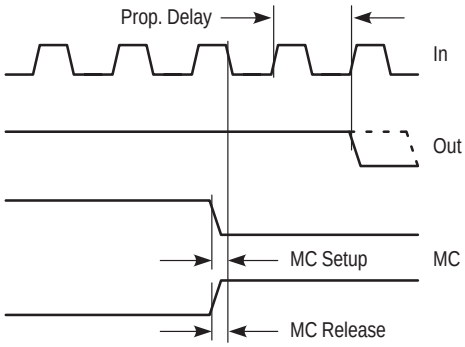
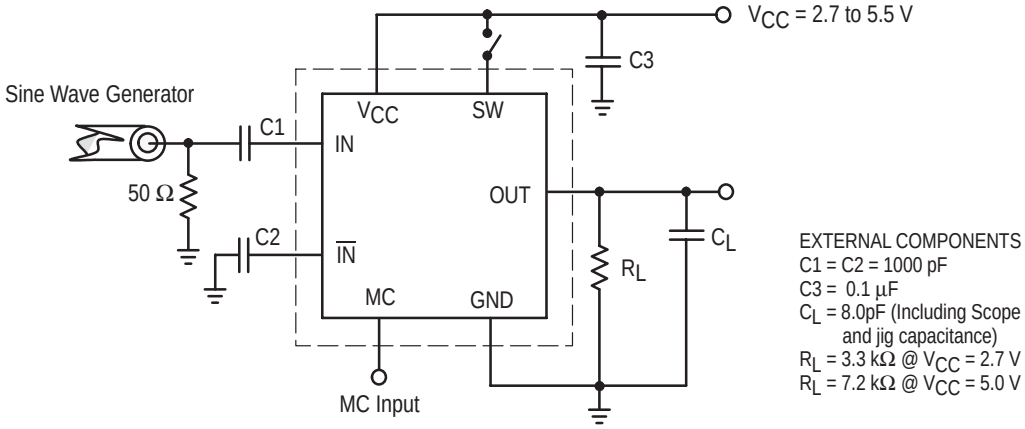


Figure 2. Modulus Setup Time



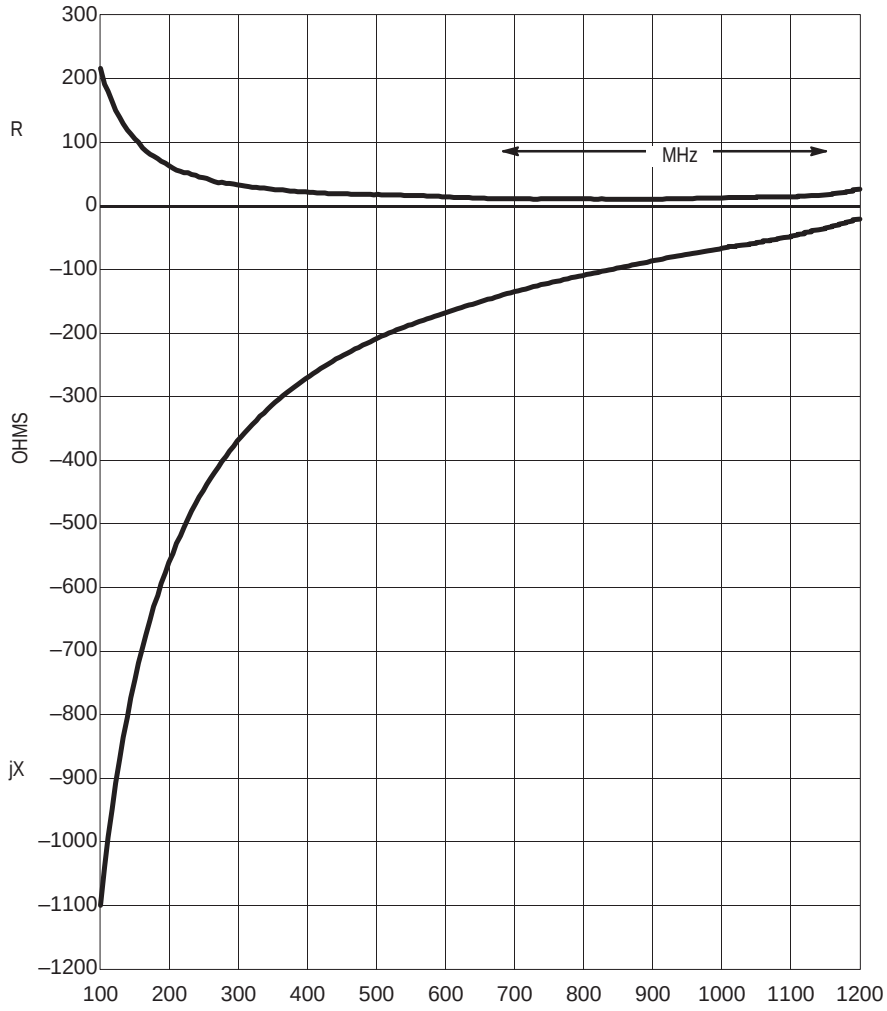
Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. AC Test Circuit



EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 µF
C_L = 8.0pF (Including Scope and jig capacitance)
R_L = 3.3 kΩ @ V_{CC} = 2.7 V
R_L = 7.2 kΩ @ V_{CC} = 5.0 V

Figure 4. Typical Input Impedance versus Input Frequency



MOTOROLA

MC12053A

1.1 GHz Super Low Power Dual Modulus Prescaler With Stand-By Mode

MECL PLL COMPONENTS ÷64/65, ÷128/129 LOW POWER DUAL MODULUS PRESCALER WITH STAND–BY MODE

SEMICONDUCTOR TECHNICAL DATA

The MC12053A is a super low power ÷64/65, ÷128/129 dual modulus prescaler. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 4.3 mW at a minimum supply voltage of 2.7 V.

The Divide Ratio Control input, SW, permits selection of divide ratio as desired. A HIGH on SW selects ÷64/65; an OPEN on SW selects ÷128/129. The Modulus Control input, MC, selects the proper divide number after SW has been biased to select the desired divide ratio.

Stand–by mode is featured to reduce current drain to 50 μA typical at 2.7 V when the stand–by pin, SB, is switched LOW, disabling the prescaler. On–chip output termination provides 500 μA (typical) output current, which is sufficient to drive a CMOS synthesizer input high impedance load (8.0 pF typical).

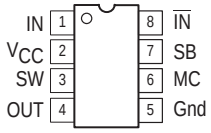
- 1.1 GHz Toggle Frequency
- Supply Voltage of 2.7 to 5.5 V
- Low Power 1.5 mA Typical at V_{CC} = 2.7 V
- Operating Temperature Range of –40 to 85°C
- On–Chip Output Termination
- The MC12053A Is Pin and Functionally Compatible With the MC12036
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL

MOSAIC V is a trademark of Motorola



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

NOTES: 1. SW: H = V_{CC} – 0.5 to V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC & SB: H = 2.0 V to V_{CC}, L = Gnd to 0.8 V.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to V_{CC}	Vdc
Maximum Output Current, Pin 4	I_O	4.0	mA

NOTE: ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12053AD	T_A = –40 to 85°C	SO–8

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; T_A = –40 to 85°C, unless otherwise notex.)

Characteristic		Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)		f_t	0.1	1.4	1.1	GHz
Supply Current Output (Pin 2)	V_{CC} = 2.7 V V_{CC} = 5.0 V	I_{CC}	– –	1.60 1.75	2.5 2.5	mA
Stand–By Current	V_{CC} = 2.7 V V_{CC} = 5.0 V	I_{SB}	– –	50 100	250 250	µA
Modulus Control & Stand–By Input HIGH (MC & SB)		V_{IH1}	2.0	–	V_{CC} + 0.5	V
Modulus Control & Stand–By Input LOW (MC & SB)		V_{IL1}	Gnd	–	0.8	V
Divide Ratio Control Input HIGH (SW)		V_{IH2}	V_{CC} – 0.5	V_{CC}	V_{CC} + 0.5	V
Divide Ratio Control Input LOW (SW)		V_{IH2}	Open	Open	Open	
Output Voltage Swing (Note 1)		V_{out}	0.8	1.1	–	V_{pp}
Modulus Setup Time MC to OUT at 1100 MHz		t_{set}	–	11	16	ns
Input Voltage Sensitivity	250–1100 MHz 100–250 MHz	V_{in}	100 400	– –	1000 1000	mVpp

NOTE: Assumes 8.0 pF high impedance load.

Figure 1. Logic Diagram (MC12053A)

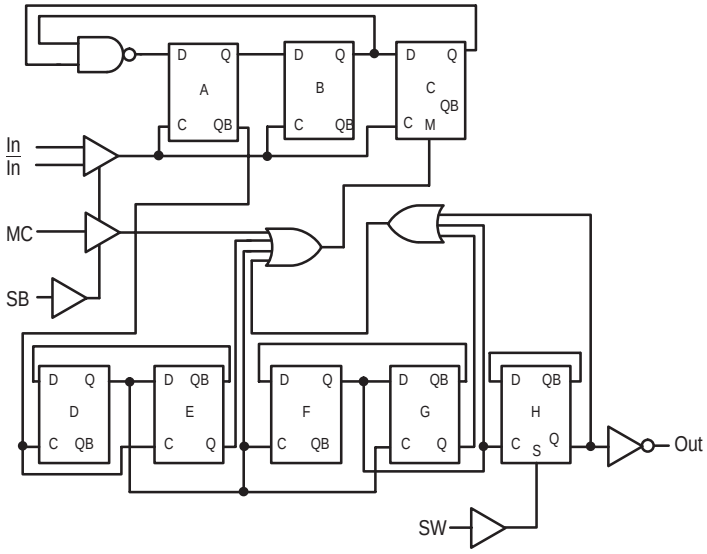
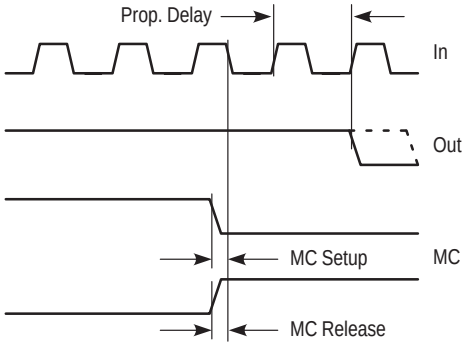
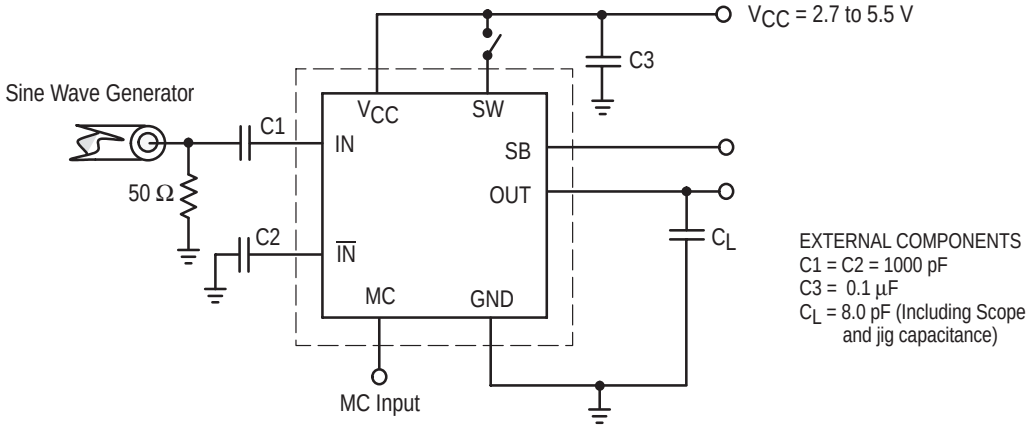


Figure 2. Modulus Setup Time



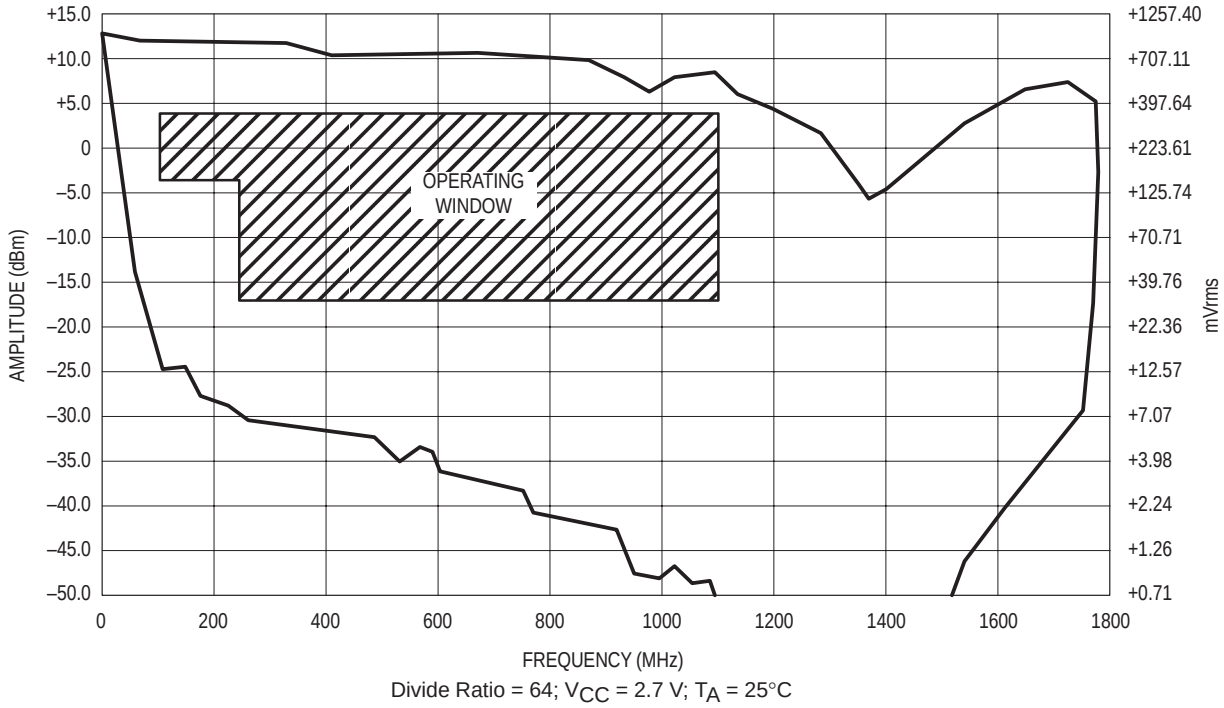
Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. AC Test Circuit



EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 µF
C_L = 8.0 pF (Including Scope and jig capacitance)

Figure 4. Input Signal Amplitude versus Input Frequency



Divide Ratio = 64; V_{CC} = 2.7 V; T_A = 25°C

Figure 5. Output Amplitude versus Input Frequency

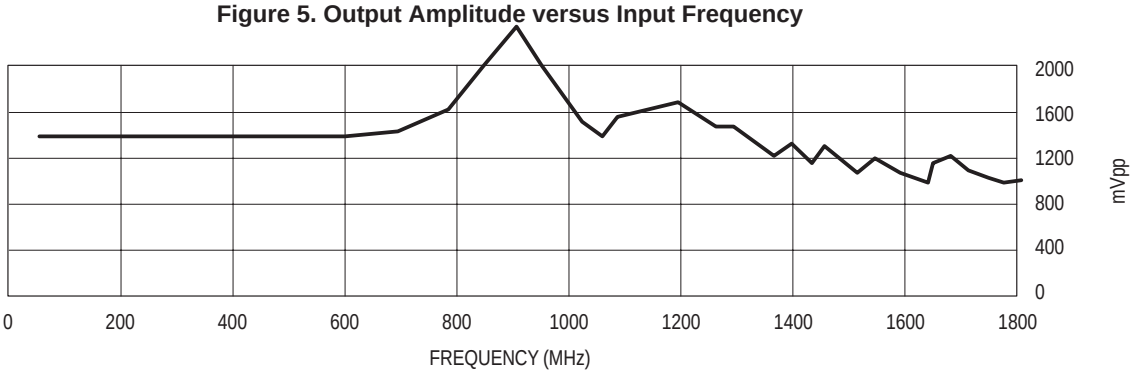
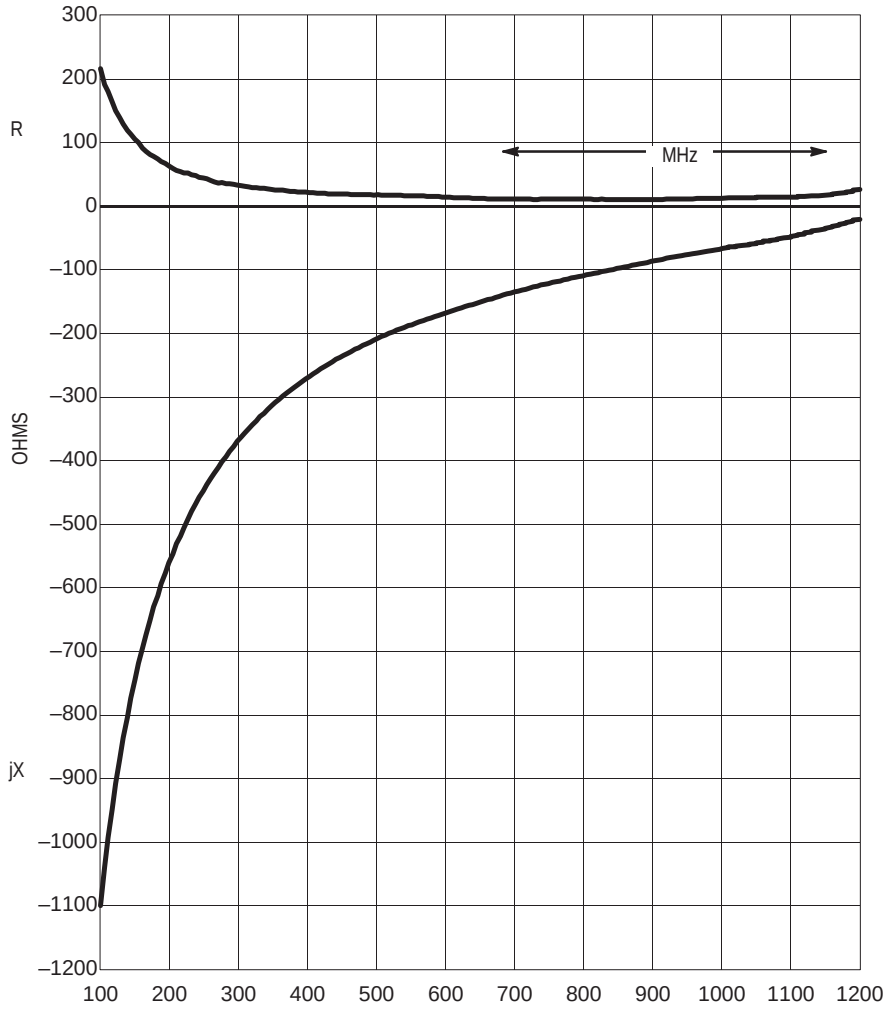


Figure 6. Typical Input Impedance versus Input Frequency



MOTOROLA

MC12054A

2.0 GHz Super Low Power Dual Modulus Prescaler

MECL PLL COMPONENTS ÷64/65, ÷128/129 LOW POWER DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

The MC12054A is a super low power dual modulus prescaler used in phase-locked loop applications. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 5.4 mW at a minimum supply voltage of 2.7 V.

The MC12054A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 2.0 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

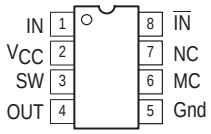
- 2.0 GHz Toggle Frequency
- The MC12054 is Pin and Functionally Compatible with the MC12031
- Low Power 2.0 mA Typical
- 2.6mA Maximum, –40 to 85°C, V_{CC} = 2.7 to 5.5 Vdc
- Short Setup Time (t_{set}) 10ns Maximum @ 2.0 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Maximum Input Voltage Should Be Limited to 6.5 Vdc

MOSAIC V is a trademark of Motorola



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc

NOTE: ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12054AD	T_A = –40 to 85°C	SO–8

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 Vdc, T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	2.5	2.0	GHz
Supply Current (Pin 2)	I_{CC}	–	2.0	2.6	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC} + 0.5 V	V
Modulus Control Input Low (MC)	V_{IL1}	Gnd	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC} – 0.5 V	V_{CC}	V_{CC} + 0.5 V	VDC
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	–
Output Voltage Swing (Note 2) (C_L = 8.0 pF, R_L = 1.65 kΩ)	V_{out}	0.8	1.1	–	V_{pp}
Modulus Setup Time MC to Out @ 2000 MHz	t_{set}	–	8.0	10	ns
Input Voltage Sensitivity 250–2000 MHz 100–250 MHz	V_{in}	100 400	– –	1000 1000	mVpp
Output Current (Note 1) V_{CC} = 2.7 V, C_L = 8.0 pF, R_L = 1.65 kΩ V_{CC} = 5.0 V, C_L = 8.0 pF, R_L = 3.6 kΩ	I_O	 – –	 1.0 1.0	 4.0 4.0	mA

NOTES: 1. Divide ratio of ÷64/65 @ 2.0 GHz
2. Valid over voltage range 2.7 to 5.5 V; R_L = 1.65 kΩ @ V_{CC} = 2.7 V; R_L = 3.6 kΩ @ V_{CC} = 5.0 V

Figure 1. Logic Diagram (MC12054A)

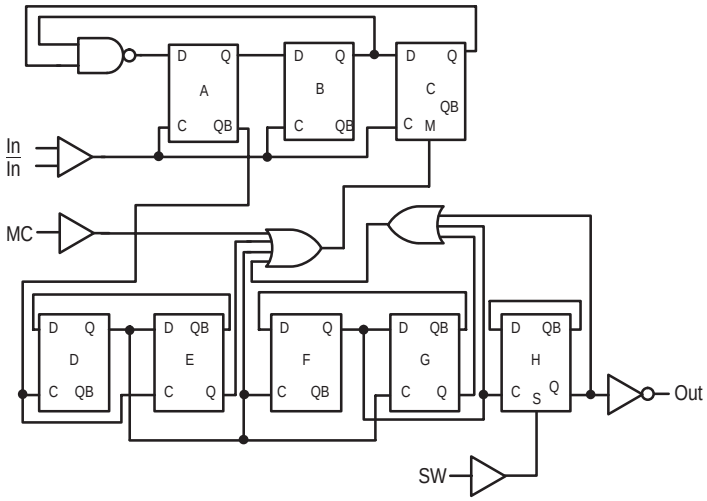
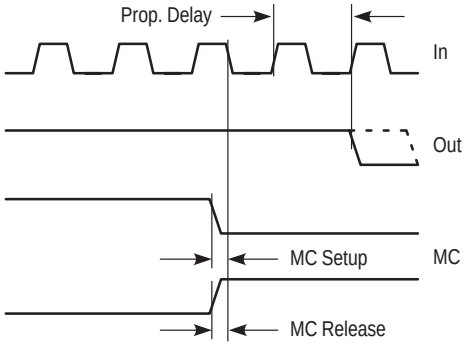
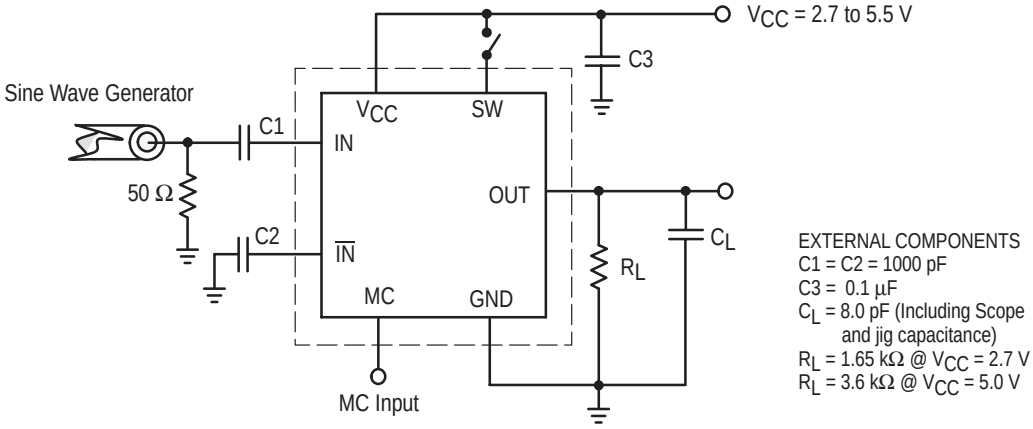


Figure 2. Modulus Setup Time



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. AC Test Circuit



EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 µF
C_L = 8.0 pF (Including Scope and jig capacitance)
R_L = 1.65 kΩ @ V_{CC} = 2.7 V
R_L = 3.6 kΩ @ V_{CC} = 5.0 V

MOTOROLA

MC12058

1.1 GHz Low Power Dual Modulus Prescaler

The MC12058 is a low power ÷126/128, ÷254/256 dual modulus prescaler. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 3.0 mW at a minimum supply voltage of 2.7 V. The MC12058 can be operated down to a minimum supply voltage of 2.7 V required for battery operated portable systems.

On–chip output termination provides 250 μA (typical) output current to drive a 8.0 pF (typical) high impedance load. The Divide Ratio Control input, SW, permits selection of divide ratio as desired. A HIGH on SW selects ÷126/128; an OPEN on SW selects ÷254/256. The Modulus Control input, MC, selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage 2.7 to 5.5 V
- Low Power 1.1 mA Typical at V_{CC} = 3.0 V
- Operating Temperature Range of –40 to 85°C
- On–Chip Output Termination

MOSAIC V is a trademark of Motorola

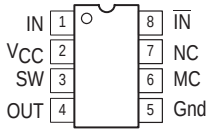
MECL PLL COMPONENTS
÷126/128, ÷254/256
LOW POWER
DUAL MODULUS PRESCALER

SEMICONDUCTOR
TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	126
H	L	128
L	H	254
L	L	256

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to V_{CC}	Vdc
Maximum Output Current, Pin 4	I_O	4.0	mA

NOTE: ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12058D	T_A = – 40 to 85°C	SO–8

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current Output (Pin 2)	I_{CC}	–	1.1	2.0	mA
Modulus Control Input HIGH (MC)	V_{IH1}	2.0	–	V_{CC} + 0.5	V
Modulus Control Input LOW (MC)	V_{IL1}	Gnd	–	0.8	V
Divide Ratio Control Input HIGH (SW)	V_{IH2}	V_{CC} – 0.5	V_{CC}	V_{CC} + 0.5	V
Divide Ratio Control Input LOW (SW)	V_{IH2}	Open	Open	Open	–
Output Voltage Swing (Note 1)	V_{out}	0.8	1.1	–	V_{pp}
Modulus Setup Time MC to OUT at 1100 MHz	t_{set}	–	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	V_{in}	100 400	– –	1000 1000	mVpp

NOTE: Assumes 8.0 pF high impedance load.

Figure 1. Logic Diagram (MC12058)

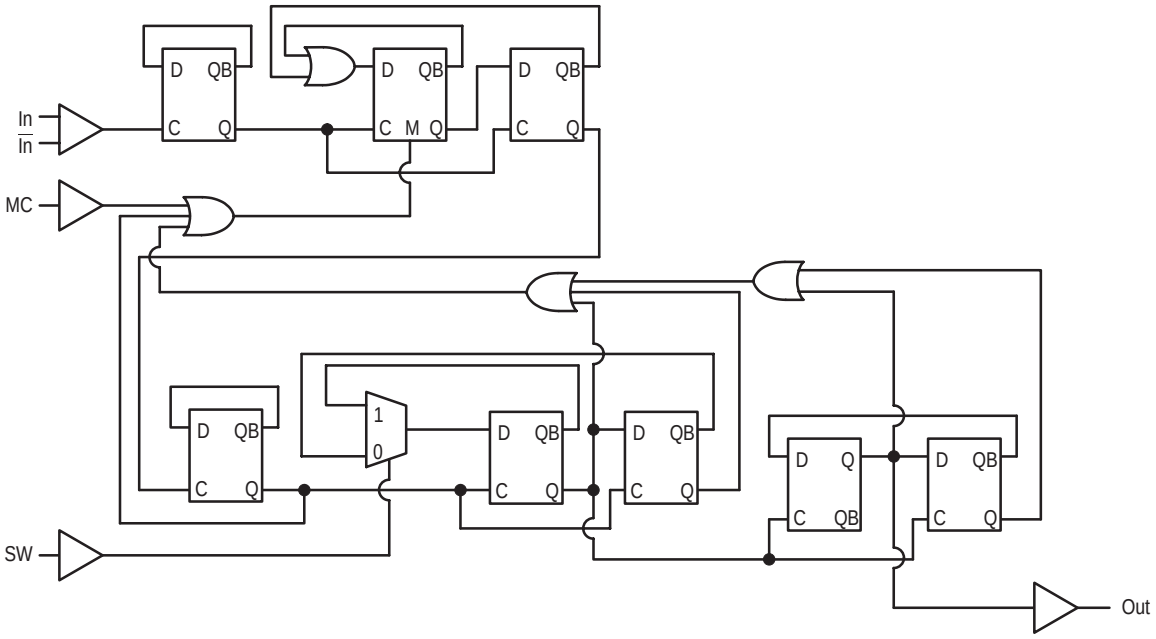
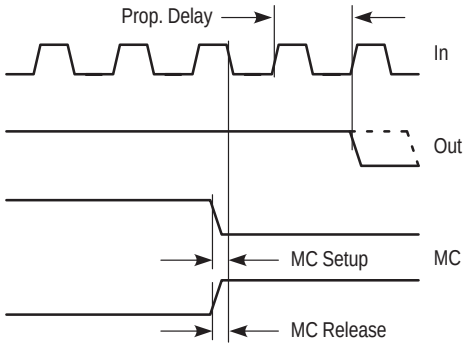
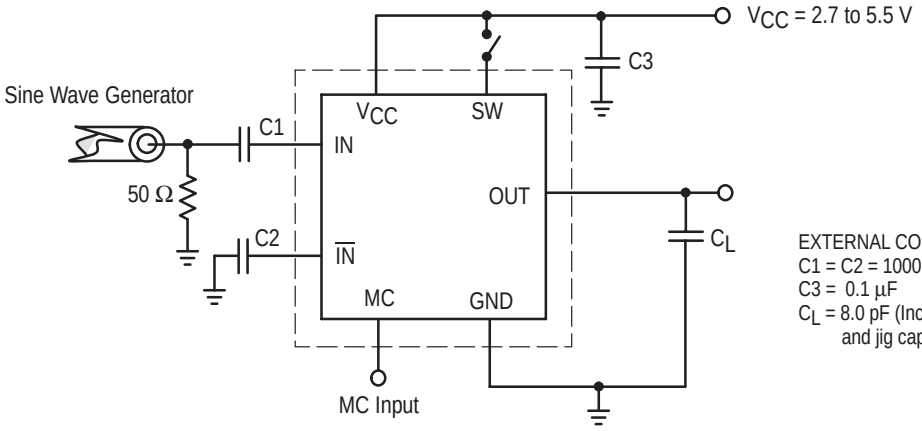


Figure 2. Modulus Setup Time



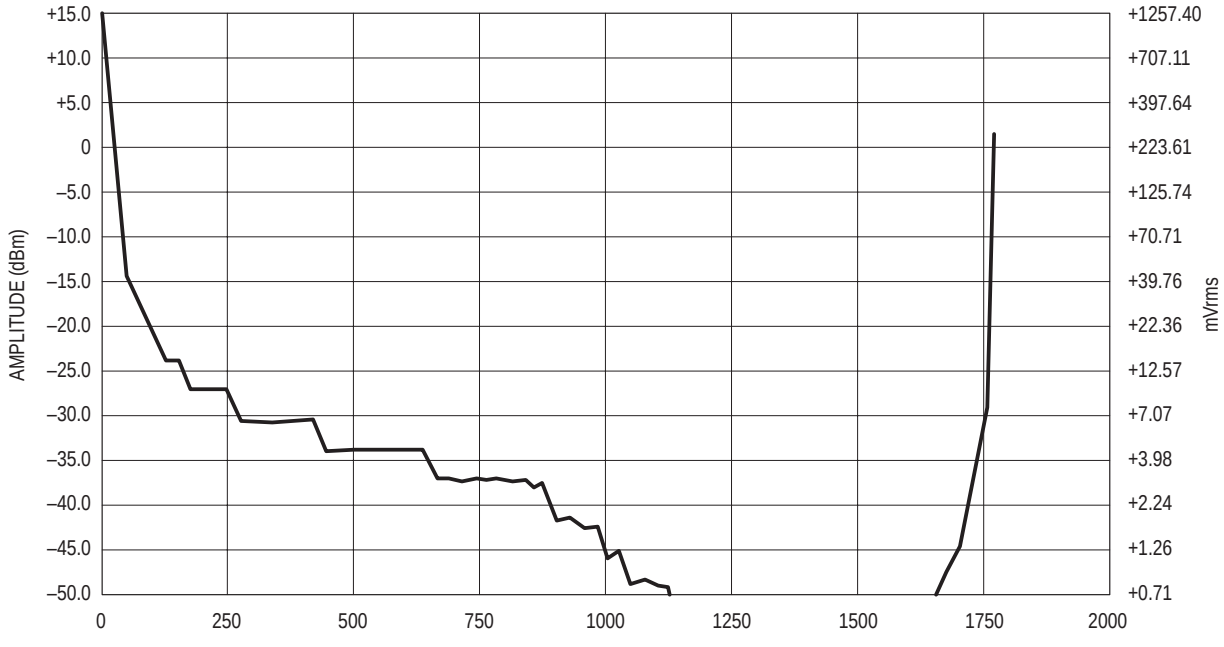
Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. AC Test Circuit



EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 μF
C_L = 8.0 pF (Including Scope and jig capacitance)

Figure 4. Input Signal Amplitude versus Input Frequency



Divide Ratio = 126; V_{CC} = 5.5 V; T_A = 25°C

Figure 5. Output Amplitude versus Input Frequency

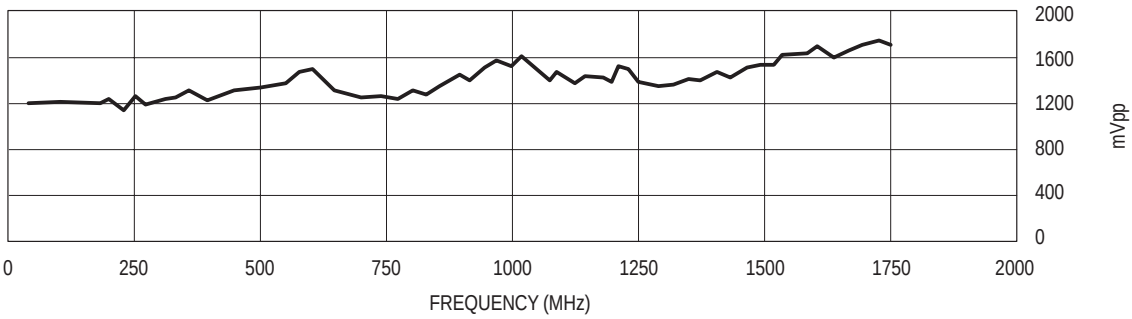
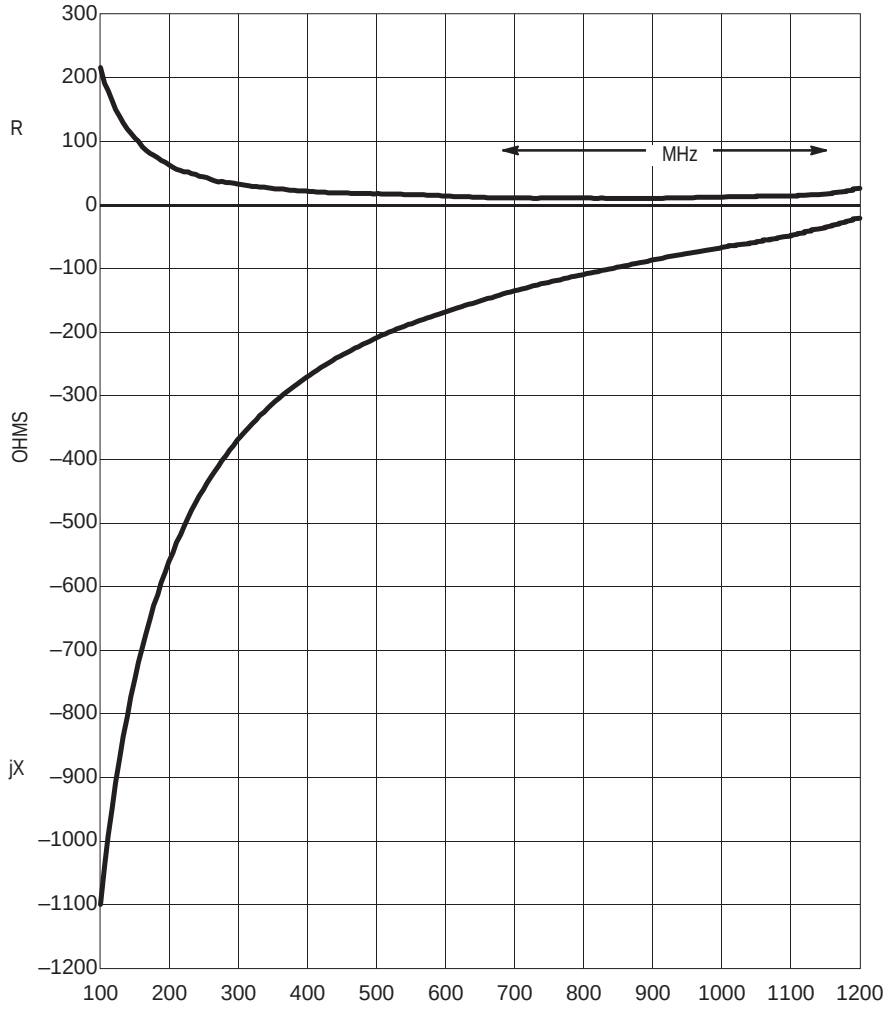


Figure 6. Typical Input Impedance versus Input Frequency



MOTOROLA

MC12079

2.8 GHz Prescaler

The MC12079 is a single modulus divide by 64, 128, 256 prescaler for low power frequency division of a 2.8 GHz (typical) high frequency input signal. Divide ratio control inputs SW1 and SW2 select the required divide ratio of ÷64, ÷128, or ÷256.

An external load resistor is required to terminate the output. A 1.2 kΩ resistor is recommended to achieve a 1.6 V_{pp} output swing, when dividing a 1.1 GHz input signal by the minimum divide ratio of 64, assuming a 12 pF load. Output current can be minimized dependent on conditions such as output frequency, capacitive load being driven, and output voltage swing required. Typical values for load resistors are included in the V_{out} specification for various divide ratios at 2.8 GHz input frequency.

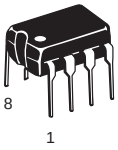
- 2.8 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- Low Power 9mA Typical at V_{CC} = 5.0 V
- Operating Temperature Range of –40 to 85°C

MECL PLL COMPONENTS
÷64/128/256 PRESCALER

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



P SUFFIX
PLASTIC PACKAGE
CASE 626

FUNCTIONAL TABLE

SW1	SW2	Divide Ratio
H	H	64
H	L	128
L	H	128
L	L	256

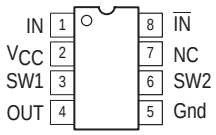
NOTE: SW1 & SW2: H = V_{CC}, L = Open.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Maximum Output Current, Pin 4	I_O	4.0	mA

NOTE: ESD data available upon request.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12079D	T_A = – 40° to +85°C	SO–8
MC12079P		Plastic

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)	ft	0.25	3.4	2.8	GHz
Supply Current Output (Pin 2)	I_{CC}	–	9.0	11.5	mA
Input Voltage Sensitivity 250–500 MHz 500–2800 MHz	V_{in}	400 100	– –	1000 1000	mVpp
Divide Ratio Control Input High (SW)	V_{IH}	V_{CC}	V_{CC}	V_{CC}	V
Divide Ratio Control Input Low (SW)	V_{IL}	Open	Open	Open	–
Output Voltage Swing (C_L = 12 pF; R_L = 1.2 kΩ; I_O = 2.7 mA)[1] (C_L = 12 pF; R_L = 2.2 kΩ; I_O = 1.5 mA)[2] (C_L = 12 pF; R_L = 3.9 kΩ; I_O = 0.85 mA)[3]	V_{out}	1.0	1.6	–	V_{pp}

NOTES: 1. Divide ratio of ÷64 at 2.8 GHz.
2. Divide ratio of ÷128 at 2.8 GHz.
3. Divide ratio of ÷256 at 2.8 GHz.

Figure 1. Logic Diagram (MC12079)

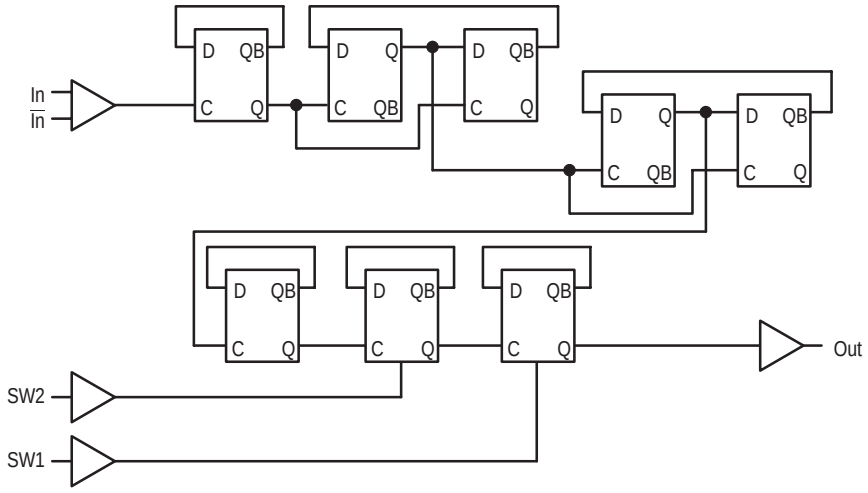
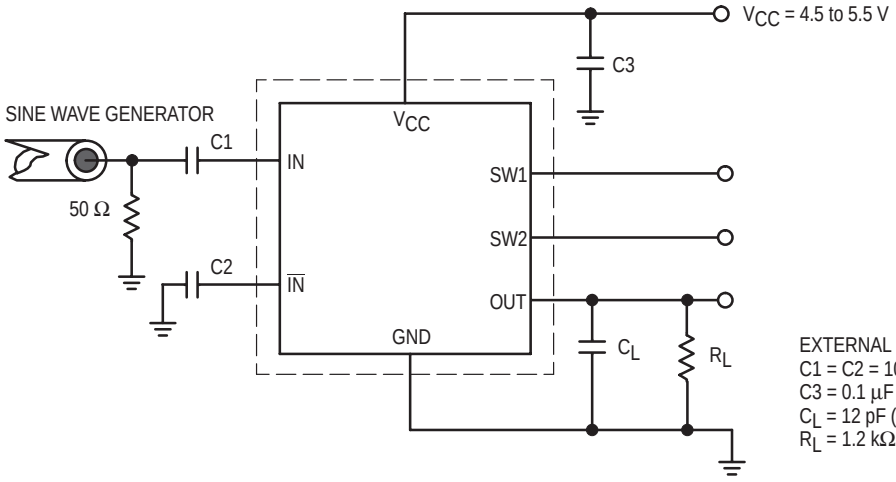
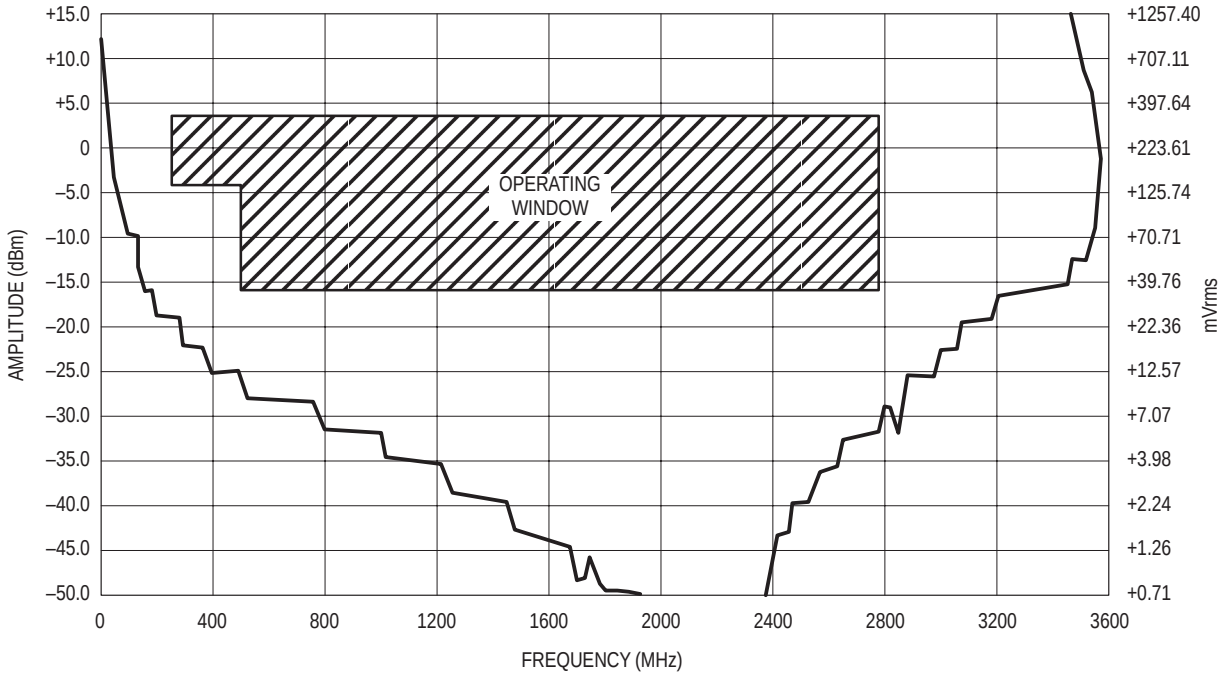


Figure 2. AC Test Circuit



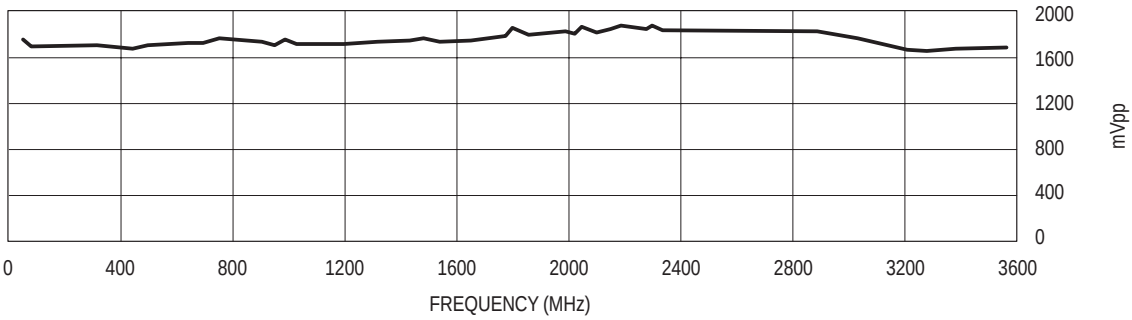
EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 µF
C_L = 12 pF (Including Scope and Jig Capacitance)
R_L = 1.2 kΩ (for ÷64 at 2.8 GHz)

Figure 3. Input Signal Amplitude versus Input Frequency



Divide Ratio = 64; V_{CC} = 5.0 V; T_A = 25°C

Figure 4. Output Amplitude versus Input Frequency



MOTOROLA

MC12080

1.1 GHz Prescaler

The MC12080 is a single modulus divide by 10, 20, 40, 80 prescaler for low power frequency division of a 1.1 GHz high frequency input signal. Divide ratio control inputs SW1, SW2 and SW3 select the required divide ratio of ÷10, ÷20, ÷40, or ÷80.

An external load resistor is required to terminate the output. A 820 Ω resistor is recommended to achieve a 1.2 V_{pp} output swing, when dividing a 1.1 GHz input signal by the minimum divide by ratio of 10, assuming a 8.0 pF load. Output current can be minimized dependent on conditions such as output frequency, capacitive load being driven, and output voltage swing required. Typical values for load resistors are included in the V_{out} specification for various divide ratios at 1.1 GHz input frequency.

- 1.1 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- Low Power 3.7mA Typical at V_{CC} = 5.0 V
- Operating Temperature Range of –40 to 85°C

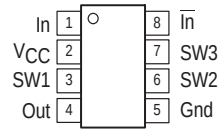
MECL PLL COMPONENTS
÷10/20/40/80 PRESCALER

SEMICONDUCTOR
TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8, Tape and Reel Only)

PIN CONNECTIONS



(Top View)

FUNCTIONAL TABLE

SW1	SW2	SW3	Divide Ratio
L	L	L	80
L	L	H	40
L	H	L	40
L	H	H	20
H	L	L	40
H	L	H	20
H	H	L	20
H	H	H	10

NOTE: SW1, SW2 and SW3: H = V_{CC}, L = Open.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Maximum Output Current, Pin 4	I_O	10	mA

NOTE: ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12080DR2	T_A = – 40 to 85°C	SO–8

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)	ft	0.1	1.4	1.1	GHz
Supply Current Output (Pin 2)	I_{CC}	–	3.7	5.0	mA
Input Voltage Sensitivity 100 to 250 MHz 250 to 1100 MHz	V_{in}	 400 100	 – –	 1000 1000	mVpp
Divide Ratio Control Input High (SW1, SW2, SW3)	V_{IH}	V_{CC} – 0.5 V	V_{CC}	V_{CC} + 0.5 V	V
Divide Ratio Control Input Low (SW1, SW2, SW3)	V_{IL}	Open	Open	Open	–
Output Voltage Swing [Note] R_L = 820 Ω, I_O = 4.0 mA for ÷10 R_L = 1.6 kΩ, I_O = 2.1 mA for ÷20 R_L = 3.3 kΩ, I_O = 1.1 mA for ÷40 R_L = 6.2 kΩ, I_O = 0.57 mA for ÷80	V_{out}	0.8	1.2	–	V_{pp}

NOTE: Assumes 8.0 pF load and 1.1 GHz input frequency (typical), I_O at V_{CC} = 5.0 V and T_A = 25°C

Figure 1. Logic Diagram

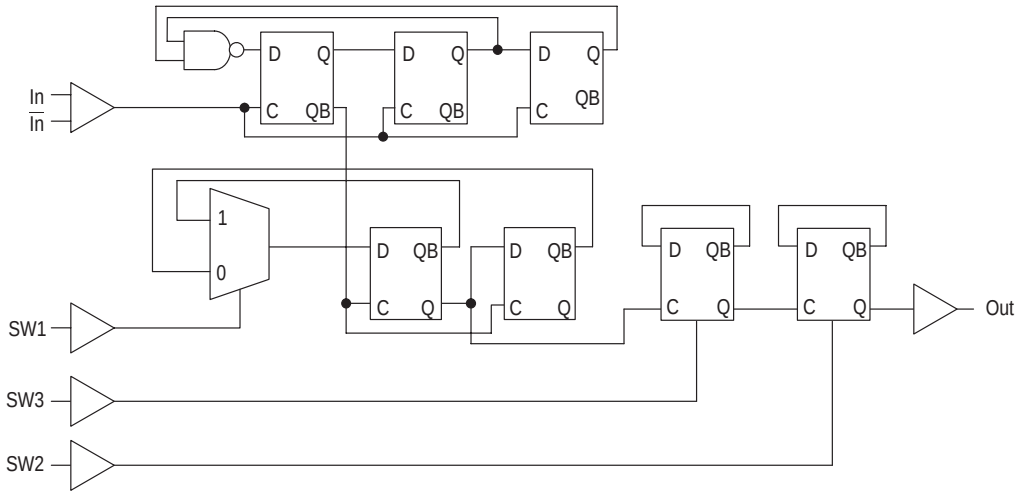
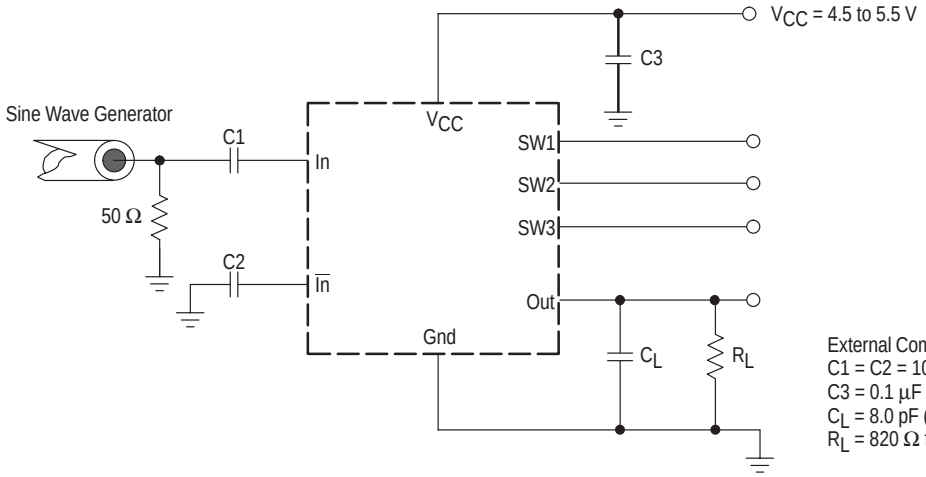
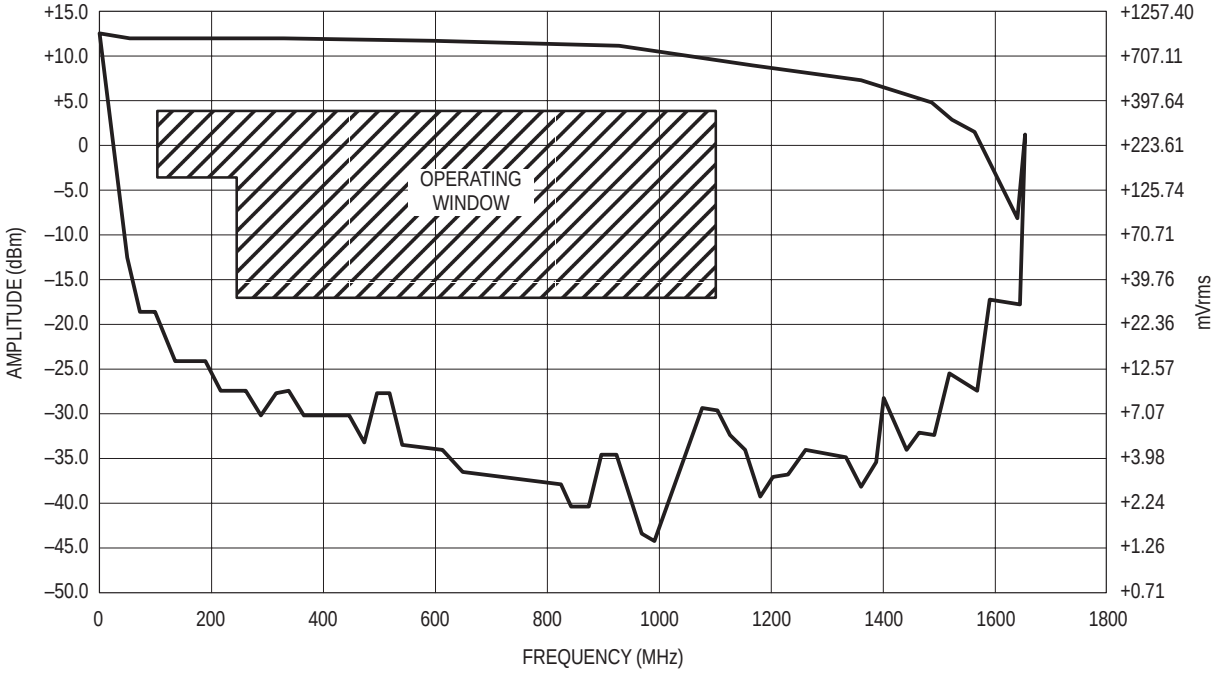


Figure 2. AC Test Circuit



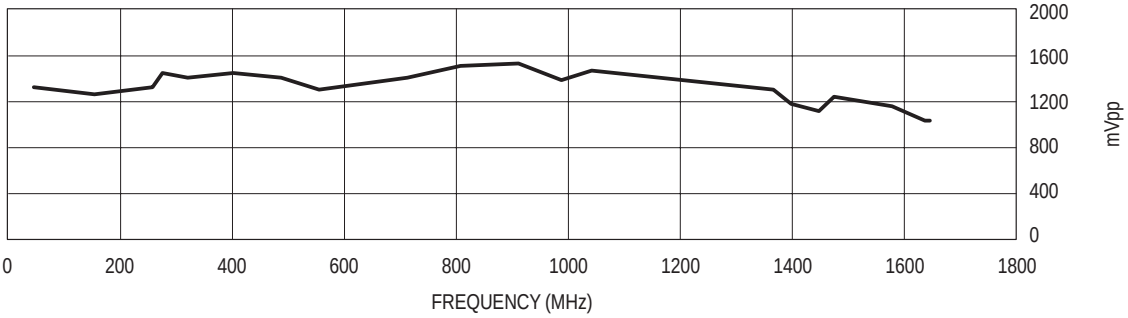
External Components
C1 = C2 = 1000 pF
C3 = 0.1 μF
C_L = 8.0 pF (Including Scope and Jig Capacitance)
R_L = 820 Ω for ÷10 at 1.1 GHz

Figure 3. Input Signal Amplitude versus Input Frequency



Divide Ratio = 10; V_{CC} = 5.0 V; T_A = 25°C

Figure 4. Output Amplitude versus Input Frequency



MOTOROLA

MC12089

2.8 GHz Prescaler

The MC12089 is a single modulus divide by 64 and 128 prescaler for low power frequency division of a 2.8 GHz high frequency input signal. The low power (10.2 mA typical at 5.0 V) and high operating frequency features make this prescaler ideal in satellite TV receiver applications.

Divide ratio control input SW selects the required divide ratio of ÷64 or ÷128.

On–chip output termination provides 2.5 mA of output current to drive a 12 pF (typical) high impedance load. The output voltage swing under typical supply voltage and temperature conditions is 1.2 V. If additional drive is required for the prescaler output, an external resistor can be added in parallel from the OUT pin to Gnd to increase the output power. Care must be taken not to exceed the maximum allowable current through the output.

- 2.8 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- Low Power Dissipation 51 mW Typical
- Operating Temperature Range of –40 to 85°C

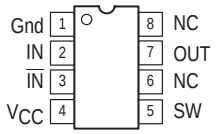
MECL PLL COMPONENTS
÷64/128 PRESCALER

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

FUNCTIONAL TABLE

SW	Divide Ratio
H	64
L	128

NOTE: H = V_{CC}, L = Open.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 4	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Maximum Output Current, Pin 7	I_O	4.0	mA

NOTE: ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12089D	T_A = –40 to 85°C	SO–8

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)		ft	0.25	3.4	2.8	GHz
Supply Current Output (Pin 2)		I_{CC}	–	10.2	14.5	mA
Input Voltage Sensitivity	250–500 MHz 500–2800 MHz	V_{in}	400 100	– –	1000 1000	mVpp
Divide Ratio Control Input High (SW)		V_{IH}	V_{CC}	V_{CC}	V_{CC}	V
Divide Ratio Control Input Low (SW)		V_{IL}	Open	Open	Open	–
Output Voltage Swing (Note 1)		V_{out}	0.8	1.2	–	V_{pp}

NOTE: 1. Assumes C_L = 12 pF

Figure 1. Logic Diagram (MC12089)

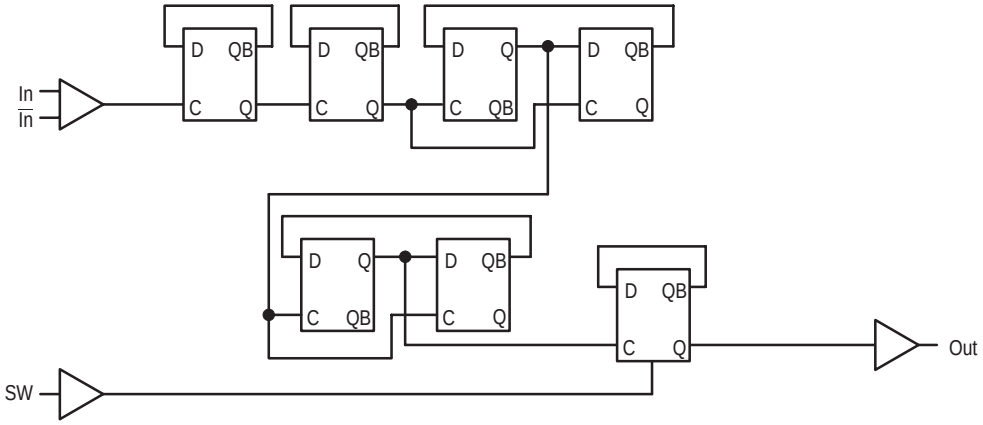
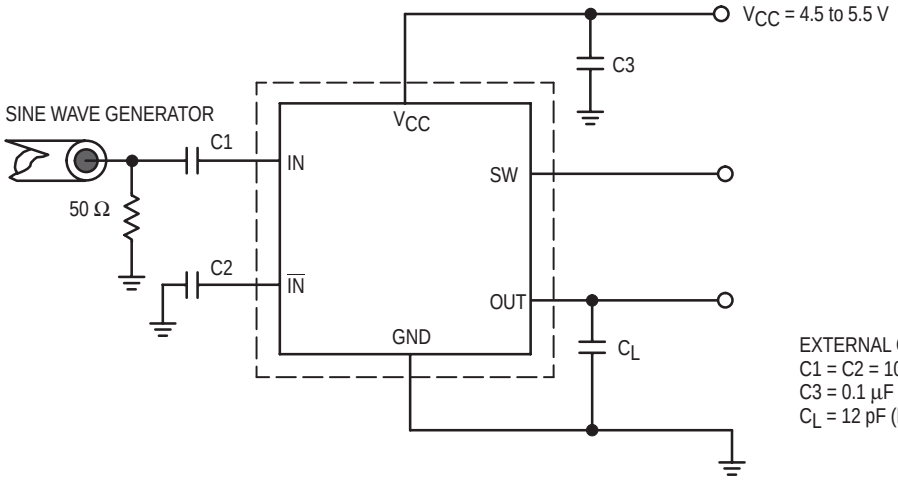
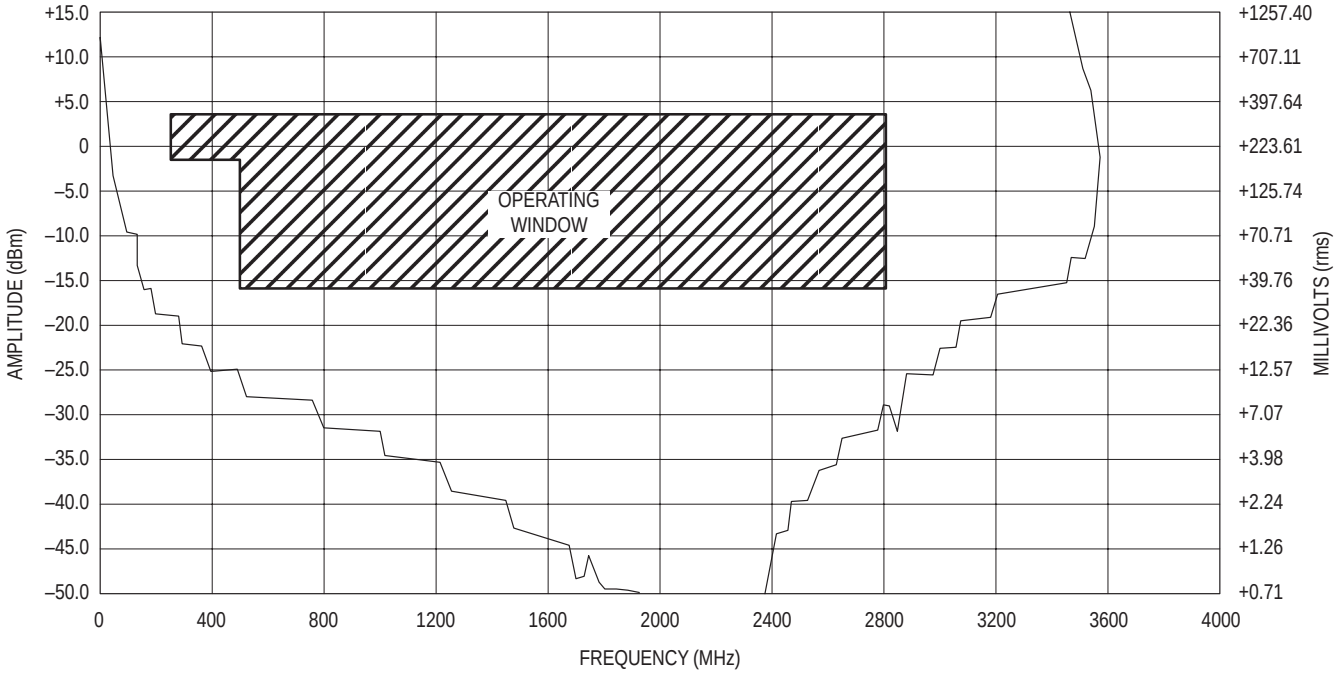


Figure 2. AC Test Circuit



EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 µF
C_L = 12 pF (Including Scope and Jig Capacitance)

Figure 3. Input Signal Amplitude versus Input Frequency



Divide Ratio = 64; V_{CC} = 5.0 V; T_A = 25°C

MOTOROLA

MC12093

÷2, ÷4, ÷8 1.1GHz Low Power Prescaler with Stand-By Mode

MECL PLL COMPONENTS
÷2, ÷4, ÷8 LOW POWER PRESCALER WITH STAND–BY MODE

SEMICONDUCTOR TECHNICAL DATA

The MC12093 is a single modulus prescaler for low power frequency division of a 1.1 GHz high frequency input signal. Motorola's advanced MOSAIC™ V technology is utilized to acheive low power dissipation of 6.75 mW at a minimum supply voltage of 2.7 V.

On–chip output termination provides output current to drive a 2.0 pF (typical) high impedance load. If additional drive is required for the prescaler output, an external resistor can be added parallel from the OUT pin to GND to increase the output power. Care must be taken not to exceed the maximum allowable current through the output.

Divide ratio control inputs SW1 and SW2 select the required divide ratio of ÷2, ÷4, or ÷8.

Stand–By mode is featured to reduce current drain to 50 µA typical when the standby pin SB is switched LOW disabling the prescaler.

- 1.1 GHz Toggle Frequency
- Supply Voltage 2.7 V to 5.5 Vdc
- Low Power 3.0 mA Typical
- Operating Temperature –40 to 85°C
- Divide by 2, 4 or 8 Selected by SW1 and SW2 Pins
- On–Chip Termination

MOSAIC V is a trademark of Motorola



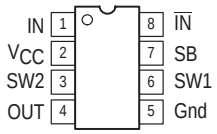
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

FUNCTIONAL TABLE

SW	SW2	Divide Ratio
L	L	8
H	L	4
L	H	4
H	H	2

NOTES: 1. SW1 & SW2: H = (V_{CC} – 0.5 V) to V_{CC}; L = Open.
2. SB: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

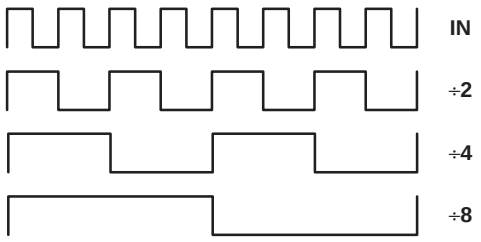
PIN CONNECTIONS



(Top View)

A LOW on the Stand–By Pin 7 disables the device.

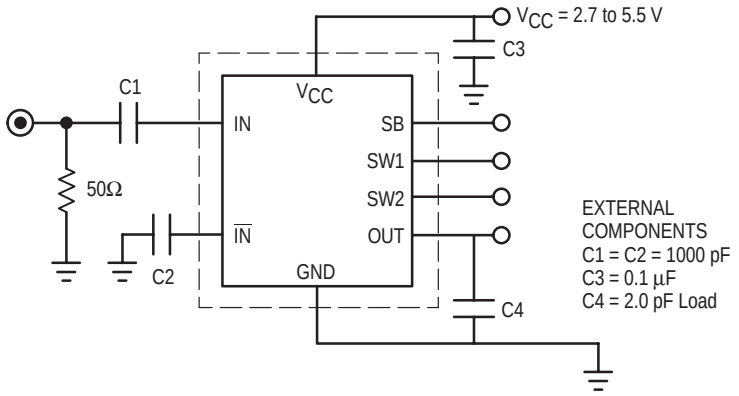
Function Chart



ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12093D	T_A = –40 to 85°C	SO–8

Figure 1. AC Test Circuit



MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 6.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	Tstg	–65 to 150	°C
Maximum Output Current, Pin 4	I_O	4.0	mA

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; T_A = –40 to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)	ft	0.1	1.4	1.1	GHz
Supply Current	I_{CC}	–	3.0	4.5	mA
Stand–By Current	ISB	–	120	200	µA
Stand–By Input HIGH (SB)	V_{IH1}	2.0	–	V_{CC}	V
Stand–By Input LOW (SB)	V_{IL1}	Gnd	–	0.8	V
Divide Ratio Control Input HIGH (SW1 & SW2)	V_{IH2}	V_{CC} – 0.5	V_{CC}	V_{CC} + 0.5	V
Divide Ratio Control Input LOW (SW1 & SW2)	V_{IL2}	OPEN	OPEN	OPEN	
Output Voltage Swing (2.0 pF Load) Output Frequency 12.5–350 MHz (Note 1) Output Frequency 350–400 MHz (Note 2) Output Frequency 400–450 MHz (Note 3) Output Frequency 450–550 MHz (Note 4)	V_{OUT}	 0.6 0.5 0.4 0.3	 0.80 0.70 0.55 0.45	 – – – –	V_{pp}
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	V_{IN}	100 400	– –	1000 1000	mVpp

NOTES: 1. Input frequency 1.1 GHz, ÷8, minimum output frequency of 12.5 MHz.
2. Input frequency 700–800 MHz, ÷2.
3. Input frequency 800–900 MHz, ÷2.
4. Input frequency 900–1100 MHz, ÷2.

MOTOROLA

MC12095

2.5 GHz Low Power Prescaler With Stand-By Mode

MECL PLL COMPONENTS
÷2, ÷4 LOW POWER PRESCALER WITH STAND–BY MODE

SEMICONDUCTOR TECHNICAL DATA

The MC12095 is a single modulus prescaler for low power frequency division of a 2.5 GHz high frequency input signal. Motorola's advanced MOSAIC™ V technology is utilized to acheive low power dissipation of 24 mW at a minimum supply voltage of 2.7 V.

On–chip output termination provides output current to drive a 2.0 pF (typical) high impedance load. If additional drive is required for the prescaler output, an external resistor can be added in parallel from the OUT pin to GND to increase the output power. Care must be taken not to exceed the maximum allowable current through the output.

Divide ratio control input (SW) selects the required divide ratio of ÷2 or ÷4. Stand–By mode is available to reduce current drain to 100µA typical when the standby pin SB is switched LOW disabling the prescaler.

- 2.5 GHz Toggle Frequency
- Supply Voltage 2.7 V to 5.5 Vdc
- Low Power 8.7 mA Typical
- Operating Temperature –40 to 85°C
- Divide by 2 or 4 Selected by the SW Pin

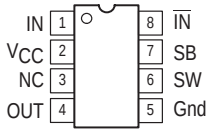
NOTE: For applications up to 1.1 GHz, please consult the MC12093 datasheet.

MOSAIC V is a trademark of Motorola



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



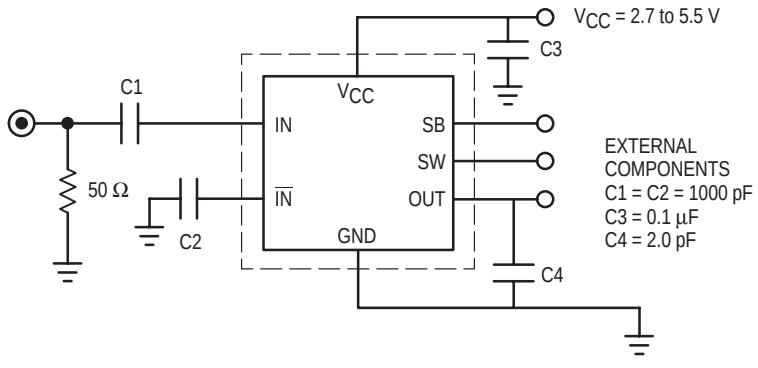
(Top View)

FUNCTIONAL TABLE

SW	Divide Ratio
H	2
L	4

NOTES: 1. SW: H = (V_{CC} – 0.4 V) to V_{CC}; L = OPEN
2. SB: H = 2.0 V to V_{CC}; L = GND to 0.8 V

AC Test Circuit



ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12095D	T_A = –40 to 85°C	SO–8

MAXIMUM RATINGS

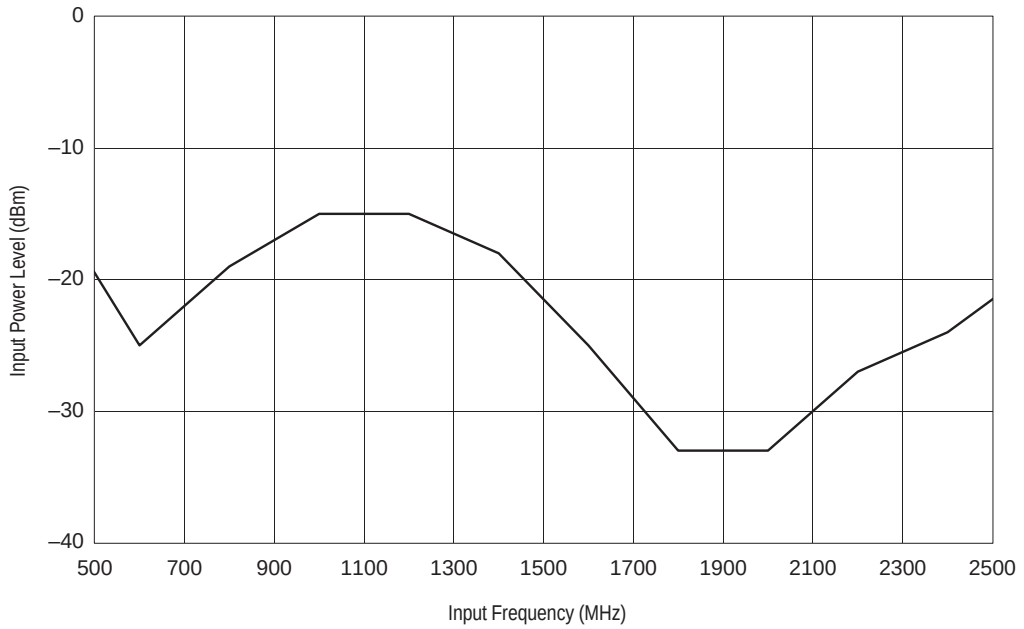
Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 6.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	Tstg	–65 to 150	°C
Maximum Output Current, Pin 4	I_O	8.0	mA

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

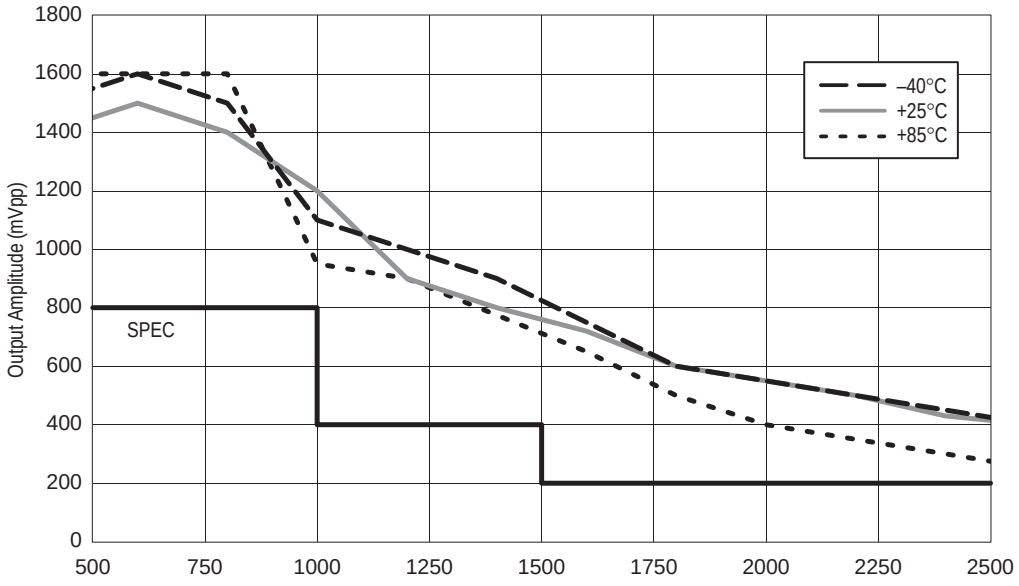
Parameter		Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)		f_t	500	3.0	2.5	GHz
Supply Current		I_{CC}	–	8.7	14	mA
Stand–By Current		ISB	–	100	200	µA
Stand–By Input HIGH (SB)		V_{IH1}	2.0	–	V_{CC} + 0.5 V	V
Stand–By Input LOW (SB)		V_{IL1}	GND	–	0.8	V
Divide Ratio Control Input HIGH (SW)		V_{IH2}	V_{CC} – 0.4	V_{CC}	V_{CC} + 0.5 V	V
Divide Ratio Control Input LOW (SW)		V_{IL2}	OPEN	OPEN	OPEN	
Output Voltage Swing (2pF Load)	500–1000 MHz Input 1000–1500 MHz Input 1500–2500 MHz Input	V_{OUT}	800 400 200	– 450 250	– – –	mVpp
Input Voltage Sensitivity		V_{IN}	200	–	1000	mVpp

Figure 1. Typical Minimum Input Sensitivity versus Input Frequency



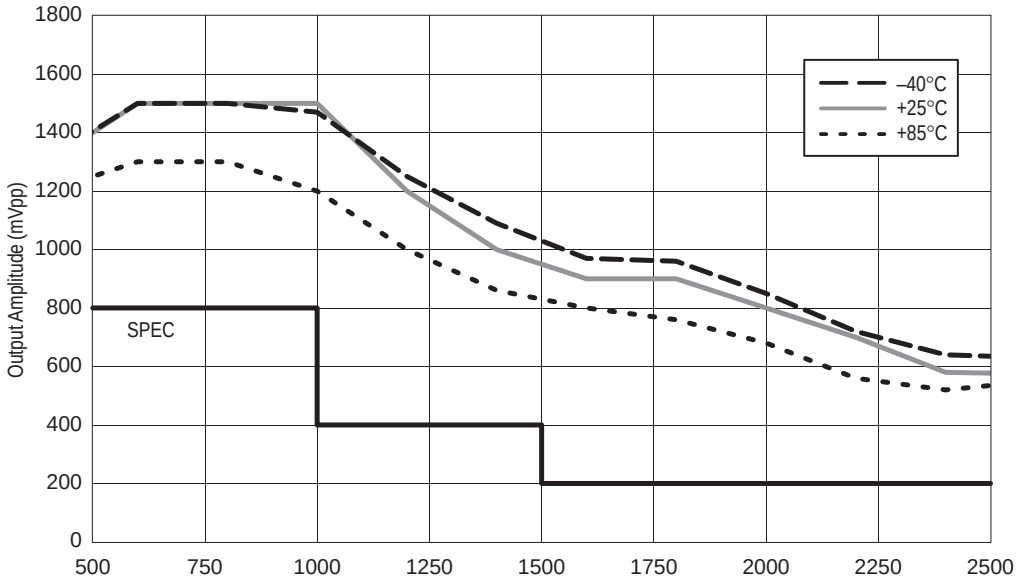
(Divide By 2 Mode, T = 25°C, V_{CC} = 2.7 V)

Figure 2. Typical Output Amplitude versus Frequency over Temperature



(Divide By 2 Mode, V_{CC} = 2.7 V)

Figure 3. Typical Output Amplitude versus Frequency over Temperature



(Divide By 4 Mode, V_{CC} = 2.7 V)

Figure 4. Input Impedance versus Frequency

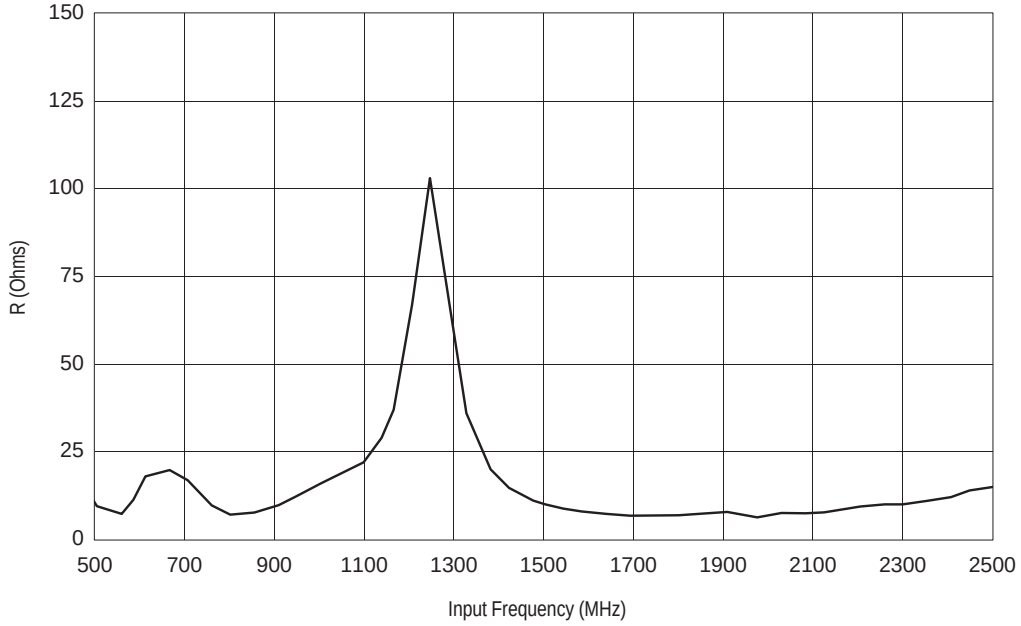
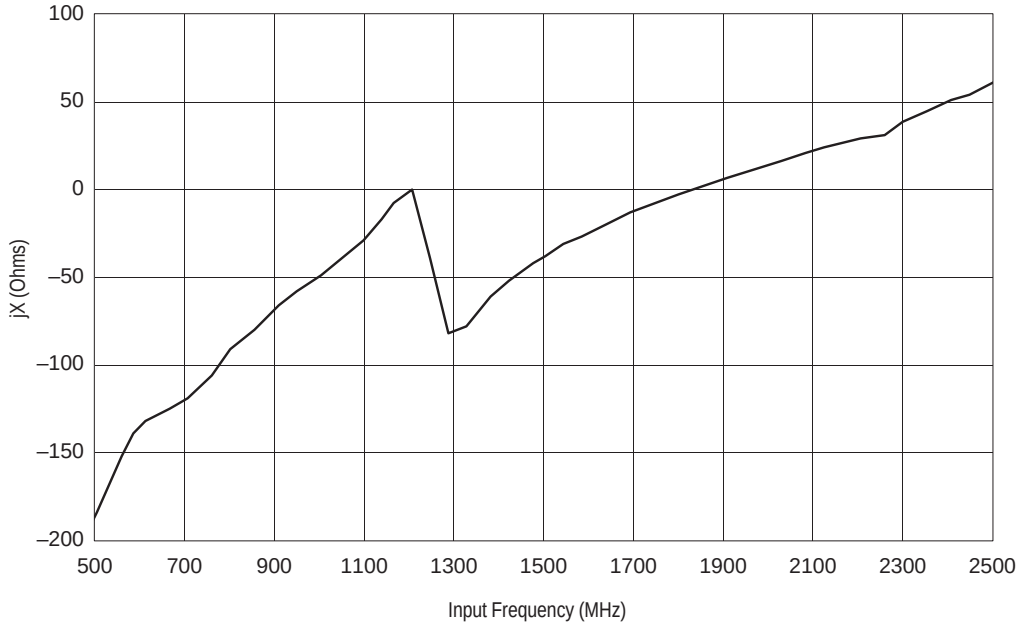


Figure 5. Input Impedance versus Frequency



MOTOROLA

MC12147

Low Power Voltage Controlled Oscillator Buffer

The MC12147 is intended for applications requiring high frequency signal generation up to 1300 MHz. An external tank circuit is used to determine the desired frequency of operation. The VCO is realized using an emitter–coupled pair topology. The MC12147 can be used with an integrated PLL IC such as the MC12202 1.1 GHz Frequency Synthesizer to realize a complete PLL sub–system. The device is specified to operate over a voltage supply range of 2.7 to 5.5 V. It has a typical current consumption of 13 mA at 3.0 V which makes it attractive for battery operated handheld systems.

NOT RECOMMENDED FOR NEW DESIGN
DEVICE TO BE PHASED OUT.
Consider MC12149 for New Designs.

NOTE: The MC12147 is NOT suitable as a crystal oscillator.

- Operates Up to 1.3 GHz
- Space–Efficient 8–Pin SOIC or SSOP Package
- Low Power 13 mA Typical @ 3.0 V Operation
- Supply Voltage of 2.7 to 5.5 V
- Typical 900MHz Performance
  - – Phase Noise –105 dBc/Hz @ 100 kHz Offset
  - – Tuning Voltage Sensitivity of 20 MHz/V
- Output Amplitude Adjustment Capability
- Two High Drive Outputs With a Typical Range from –8.0 to –2.0 dBm

The device has two high frequency outputs which make it attractive for transceiver applications which require both a transmit and receive local oscillator (LO) signal. The outputs Q and QB are available for servicing the receiver IF and transmitter up–converter single–ended. In receiver applications, the outputs can be used together if it is necessary to generate a differential signal for the receiver IF. Because the Q and QB outputs are open collector, terminations to the V_{CC} supply are required for proper operation. Since the outputs are complementary, BOTH outputs must be terminated even if only one is needed. The Q and QB outputs have a nominal drive level of –8dBm to conserve power. If addition signal amplitude is needed, a level adjustment pin (CNTL) is available, which when tied to ground, boosts the nominal output levels to –2.0 dBm.

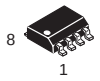
External components required for the MC12147 are: (1) tank circuit (LC network); (2) Inductor/capacitor to provide the termination for the open collector outputs; and (3) adequate supply voltage bypassing. The tank circuit consists of a high–Q inductor and varactor components. The preferred tank configuration allows the user to tune the VCO across the full supply range. VCO performance such as center frequency, tuning voltage sensitivity, and noise characteristics are dependent on the particular components and configuration of the VCO tank circuit.

PIN NAMES

Pin	Function
V_{CC}	Power Supply
CNTL	Amplitude Control for Q, QB Output Pair
TANK	Tank Circuit Input
V_{REF}	Bias Voltage Output
QB	Open Collector Output
GND	Ground
Q	Open Collector Output

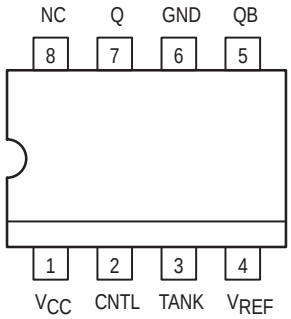
LOW POWER VOLTAGE CONTROLLED OSCILLATOR BUFFER

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12147D	T_A = –40 to 85°C	SO–8

MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 1	V_{CC}	-0.5 to +7.0	V
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Maximum Output Current, Pin 5,7	I_O	12	mA

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 VDC, T_A = -40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (CNTL=GND) V_{CC} = 3.3 V V_{CC} = 5.5 V	I_{CC}	– –	14.0 23.5	18 28	mA
Supply Current (CNTL=OPEN) V_{CC} = 3.3 V V_{CC} = 5.5 V	I_{CC}	– –	8 13	13.0 22.5	mA
Output Amplitude (Pin 5 & 7) {Note 1] V_{CC} = 2.7 V 50Ω to V_{CC} V_{CC} = 2.7 V	 V_{OH}, V_{OL}	 2.6 2.1	 2.7 2.3	 – 2.4	V
Output Amplitude (Pin 5 & 7) [Note 1] V_{CC} = 5.5 V 50Ω to V_{CC} V_{CC} = 5.5 V	 V_{OH}, V_{OL}	 5.4 4.8	 5.5 5.0	 – 5.1	V
Tuning Voltage Sensitivity [Notes 2 and 3]	T_{stg}	–	20	–	MHz/V
Frequency of Operation	F_C	100	–	1300	MHz
CSR at 10 kHz Offset, 1.0 Hz BW [Notes 2 and 3]	ℒ(f)	–	–85	–	dBc/Hz
CSR at 100 kHz Offset, 1.0 Hz BW [Notes 2 and 3]	ℒ(f)	–	–105	–	dBc/Hz
Frequency Stability [Notes 2 and 3] Supply Drift Thermal Drift	 F_{sts} f_{stt}	 – –	 0.8 50	 – –	 MHz/V KHz/°C

NOTES: 1. CNTL pin tied to ground.
2. Actual performance depends on tank components selected.
3. See Figure 12, 750 MHz tank.
4. T = 25°C, V_{CC} = 5.0 V ±10%

OPERATIONAL CHARACTERISTICS

A simplified schematic of the MC12147 is found in Figure 1. The oscillator incorporates positive feedback by coupling the base of transistor Q2 to the collector of transistor Q1. In order to minimize interaction between the VCO outputs and the oscillator tank transistor pair, a buffer is incorporated into the circuit. This differential buffer is realized by the Q3 and Q4 transistor pair. The differential buffer drives the gate which contains the primary open collector outputs, Q and QB. The output is actually a current which has been set by an internal bias driver to a nominal current of 4mA. Additional circuitry is incorporated into the tail of the current source which allows the current source to be increased to approximately 10mA. This is accommodated by the addition of a resistor which is brought out to the CNTL pin. When this pin is tied to ground, the additional current is sourced through the current source thus increasing the output amplitude of the Q/QB output pair. If less than 10 mA of current is needed, a resistor can be added to ground which reduces the amount of current.

APPLICATION INFORMATION

Figure 2 illustrates the external components necessary for the proper operation of the VCO buffer. The tank circuit configuration in this figure allows the VCO to be tuned across the full operating voltage of the power supply. This is very important in 3V applications where it is desirable to utilize as much of the operating supply range as possible so as to minimize the VCO sensitivity (MHz/V). In most situations, it is desirable to keep the sensitivity low so the circuit will be less susceptible to external noise influences. An additional benefit to this configuration is that additional regulation/ filtering can be incorporated into the V_{CC} line without compromising the tuning range of the VCO. With the AC–coupled tank configuration, the V_{tune} voltage can be greater than the V_{CC} voltage supplied to the device.

There are four main areas that the user directly influences the performance of the VCO. These include Tank Design, Output Termination Selection, Power Supply Decoupling, and Circuit Board Layout/Grounding.

The design of the tank circuit is critical to the proper operation of the VCO. This tank circuit directly impacts the main VCO operating characteristics:

1) Frequency of Operation
2) Tuning Sensitivity
3) Voltage Supply Pushing
4) Phase Noise Performance

The tank circuit, in its simplest form, is realized as an LC circuit which determines the VCO operating frequency. This is described in Equation 1.

$$f_o = \frac{1}{2\pi \sqrt{LC}} \qquad \text{Equation 1}$$

In the practical case, the capacitor is replaced with a varactor diode whose capacitance changes with the voltage applied, thus changing the resonant frequency at which the VCO tank operates. The capacitive component in Equation 1 also needs to include the input capacitance of the device and other circuit and parasitic elements. Typically, the inductor is realized as a surface mount chip or a wound–coil. In addition, the lead inductance and board inductance and capacitance also have an impact on the final operating point.

Figure 1. Simplified Schematic

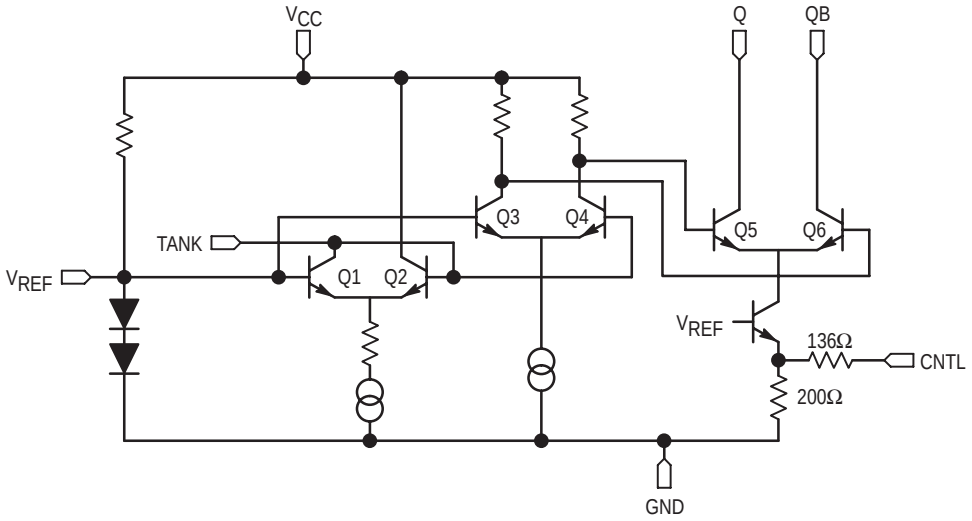
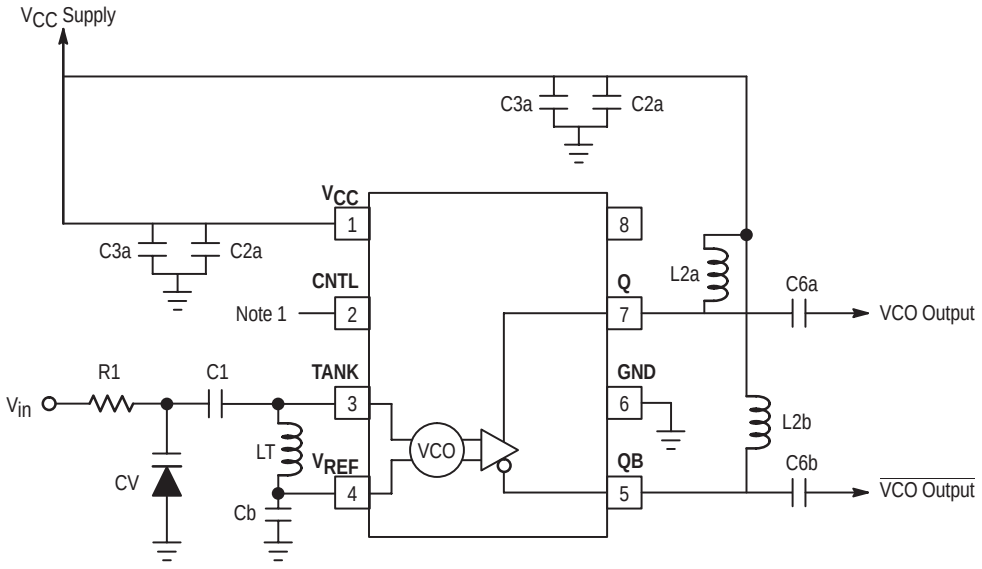


Figure 2. MC12147 Typical External Component Connections



1. This input can be left open, tied to ground, or tied with a resistor to ground, depending on the desired output amplitude needed at the Q and QB output pair.
2. Typical values for R1 range from 5.0 kΩ to 10 kΩ.

A simplified linear approximation of the device, package, and typical board parasitics has been developed to aid the designer in selecting the proper tank circuit values. All the parasitic contributions have been lumped into a parasitic capacitive component and a parasitic inductive component. While this is not entirely accurate, it gives the designer a solid starting point for selecting the tank components.

Below are the parameters used in the model.

Cp Parasitic Capacitance
Lp Parasitic Inductance
LT Inductance of Coil
C1 Coupling Capacitor Value
Cb Capacitor for decoupling the Bias Pin
CV Varactor Diode Capacitance (Variable)

The values for these components are substituted into the following equations:

$$Ci = \frac{C1 \times CV}{C1 + CV} + Cp \qquad \text{Equation 2}$$

$$C = \frac{Ci \times Cb}{Ci + Cb} \qquad \text{Equation 3}$$

$$L = Lp + LT \qquad \text{Equation 4}$$

From Figure 2, it can be seen that the varactor capacitance (CV) is in series with the coupling capacitor (C1). This is calculated in Equation 2. For analysis purposes, the parasitic capacitances (CP) are treated as a lumped element and placed in parallel with the series combination of C1 and CV. This compound capacitance (Ci) is in series with the bias capacitor (Cb) which is calculated in Equation 3. The influences of the various capacitances; C1, CP, and Cb, impact the design by reducing the variable capacitance effects of the varactor which controls the tank resonant frequency and tuning range.

Now the results calculated from Equation 2, Equation 3 and Equation 4 can be substituted into Equation 1 to calculate the actual frequency of the tank.

To aid in analysis, it is recommended that the designer use a simple spreadsheet based on Equation 1 through Equation 4 to calculate the frequency of operation for various varactor/inductor selections before determining the initial starting condition for the tank.

The two main components at the heart of the tank are the inductor (LT) and the varactor diode (CV). The capacitance of a varactor diode junction changes with the amount of reverse bias voltage applied across the two terminals. This is the element which actually “tunes” the VCO. One characteristic of the varactor is the tuning ratio which is the ratio of the capacitance at specified minimum and maximum voltage points. For characterizing the MC12147, a Matsushita (Panasonic) varactor – MA393 was selected. This device has a typical capacitance of 11 pF at 1V and 3.7 pF at 4V and the C–V characteristic is fairly linear over that range. Similar performance was also acheived with Loral varactors. A multi–layer chip inductor was used to realize the LT component. These inductors had typical Q values in the 35–50 range for frequencies between 500 and 1000MHz.

Note: There are many suppliers of high performance varactors and inductors an Motorola can not recommend one vendor over another.

The Q (quality factor) of the components in the tank circuit has a direct impact on the resulting phase noise of the oscillator. In general, the higher the Q, the lower the phase noise of the resulting oscillator. In addition to the LT and CV components, only high quality surface–mount RF chip capacitors should be used in the tank circuit. These capacitors should have very low dielectric loss (high–Q). At a minimum, the capacitors selected should be operating 100 MHz below their series resonance point. As the desired frequency of operation increases, the values of the C1 and Cb capacitors will decrease since the series resonance point

is a function of the capacitance value. To simplify the selection of C1 and Cb, a table has been constructed based on the intended operating frequency to provide recommended starting points. These may need to be altered depending on the value of the varactor selected.

Frequency	C1	Cb
200 – 500 MHz	47 pF	47 pF
500 – 900 MHz	5.1 pF	15 pF
900 – 1200 MHz	2.7 pF	15 pF

The value of the Cb capacitor influences the VCO supply pushing. To minimize pushing, the Cb capacitor should be kept small. Since C1 is in series with the varactor, there is a strong relationship between these two components which influences the VCO sensitivity. Increasing the value of C1 tends to increase the sensitivity of the VCO.

The parasitic contributions Lp and Cp are related to the MC12147 as well as parasitics associated with the layout, tank components, and board material selected. The input capacitance of the device, bond pad, the wire bond, package/lead capacitance, wire bond inductance, lead inductance, printed circuit board layout, board dielectric, and proximity to the ground plane all have an impact on these parasitics. For example, if the ground plane is located directly below the tank components, a parasitic capacitor will be formed consisting of the solder pad, metal traces, board dielectric material, and the ground plane. The test fixture used for characterizing the device consisted of a two sided copper clad board with ground plane on the back. Nominal values where determined by selecting a varactor and characterizing the device with a number of different tank/ frequency combinations and then performing a curve fit with the data to determine values for Lp and Cp. The nominal values for the parasitic effects are seen below:

Parasitic Capacitance	Cp	4.2 pF
Parasitic Inductance	Lp	2.2 nH

These values will vary based on the users unique circuit board configuration.

Basic Guidelines:

1. Select a varactor with high Q and a reasonable capacitance versus voltage slope for the desired frequency range.
2. Select the value of Cb and C1 from the table above .
3. Calculate a value of inductance (L) which will result in achieving the desired center frequency. Note that L includes both LT and Lp.
4. Adjust the value of C1 to achieve the proper VCO sensitivity.
5. Re–adjust value of L to center VCO.
6. Prototype VCO design using selected components. It is important to use similar construction techniques and materials, board thickness, layout, ground plane spacing as intended for the final product.
7. Characterize tuning curve over the voltage operation conditions.
8. Adjust, as necessary, component values – L,C1, and Cb to compensate for parasitic board effects.
9. Evaluate over temperature and voltage limits.
10. Perform worst case analysis of tank component variation to insure proper VCO operation over full temperature and voltage range and make any adjustments as needed.

Outputs Q and QB are open collector outputs and need a inductor to V_{CC} to provide the voltage bias to the output transistor. In most applications, dc–blocking capacitors are placed in series with the output to remove the dc component before interfacing to other circuitry. These outputs are complementary and should have identical inductor values for each output. This will minimize switching noise on the V_{CC} supply caused by the outputs switching. It is important that both outputs be terminated, even if only one of the outputs is used in the application.

Referring to Figure 2, the recommended value for L2a and L2b should be 47 nH and the inductor components resonance should be at least 300 MHz greater than the maximum operating frequency. For operation above 1100 MHz, it may be necessary to reduce that inductor value to 33 nH. The recommended value for the coupling capacitors C6a, C6b, and C7 is 47 pF. Figure 2 also includes decoupling capacitors for the supply line as well as decoupling for the output inductors. Good RF decoupling practices should be used with a series of capacitors starting with high quality 100 pF chip capacitors close to the device. A typical layout is shown below in Figure 3.

The output amplitude of the Q and QB can be adjusted using the CNTL pin. Refering to Figure 1, if the CNTL pin is connected to ground, additional current will flow through the current source. When the pin is left open, the nominal current flowing through the outputs is 4 mA. When the pin is grounded, the current increases to a nominal value of 10 mA. So if a 50 ohm resistor was connected between the outputs and VCC, the output amplitude would change from 200 mV pp to 500 mV pp with an additional current drain for the device of 6 mA. To select a value between 4 and 10 mA, an external resistor can be added to ground. The equation below is used to calculate the current.

$$I_{out}(nom) = \frac{(200 + 136 + R_{ext}) \times 0.8V}{200 \times (136 + R_{ext})}$$

Figure 4 through Figure 13 illustrate typical performance achieved with the MC12147. The curves illustrate the tuning curve, supply pushing characteristics, output power, current drain, output spectrum, and phase noise performance. In most cases, data is present for both a 750 MHz and 1200 MHz tank design. The table below illustrates the component values used in the designs.

Component	750MHz Tank	1200MHz Tank	Units
R1	5000	5000	Ω
C1	5.1	2.7	pF
LT	4.7	1.8	nH
CV	3.7 @ 1.0 V 11 @ 4.0 V	3.7 @ 1.0 V 11 @ 4.0 V	pF
Cb	100*	15	pF
C6, C7	47	33	pF
L2	47	47	nH

* The value of Cb should be reduced to minimize pushing.

Figure 3. MC12147 Typical Layout
(Not to Scale)

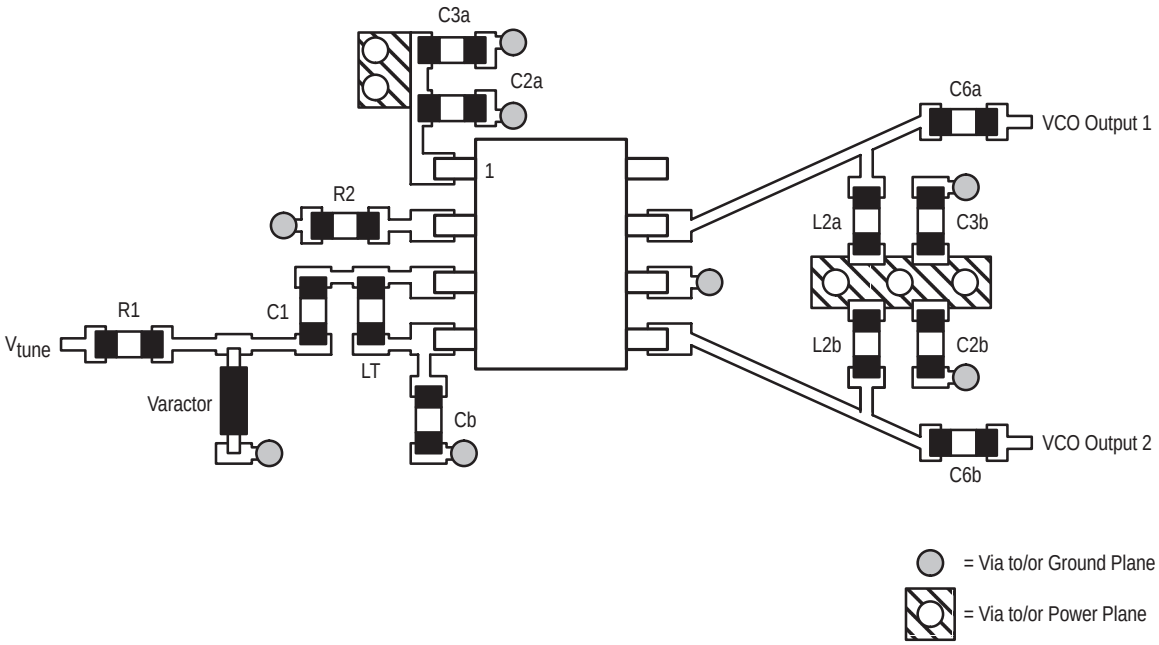


Figure 4. Typical VCO Tuning Curve, 750 MHz Tank

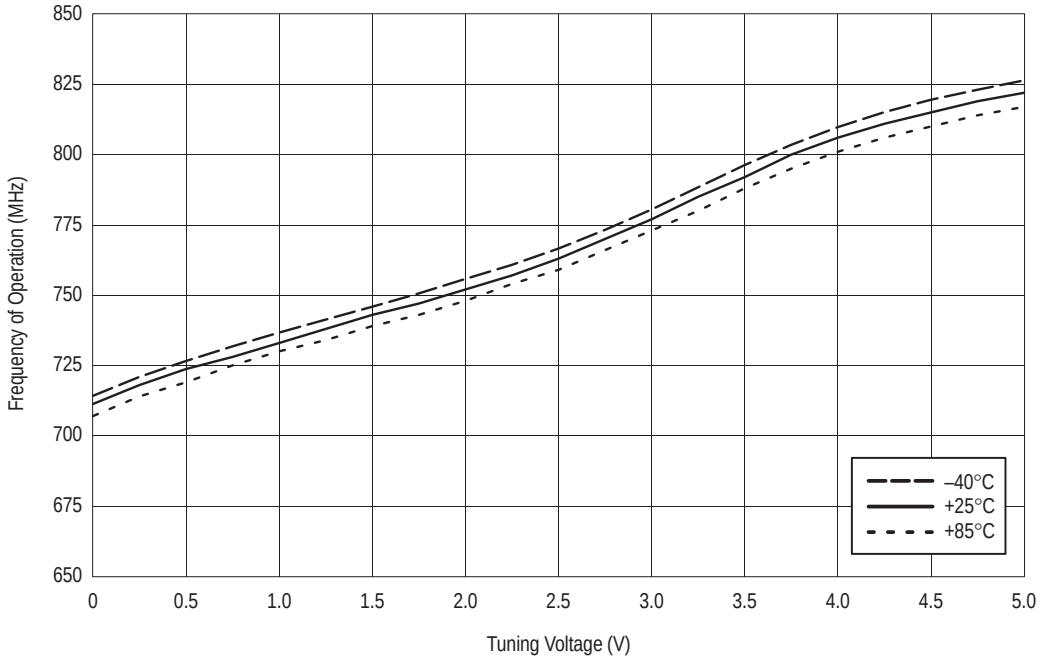


Figure 5. Typical Supply Pushing, 750MHz Tank

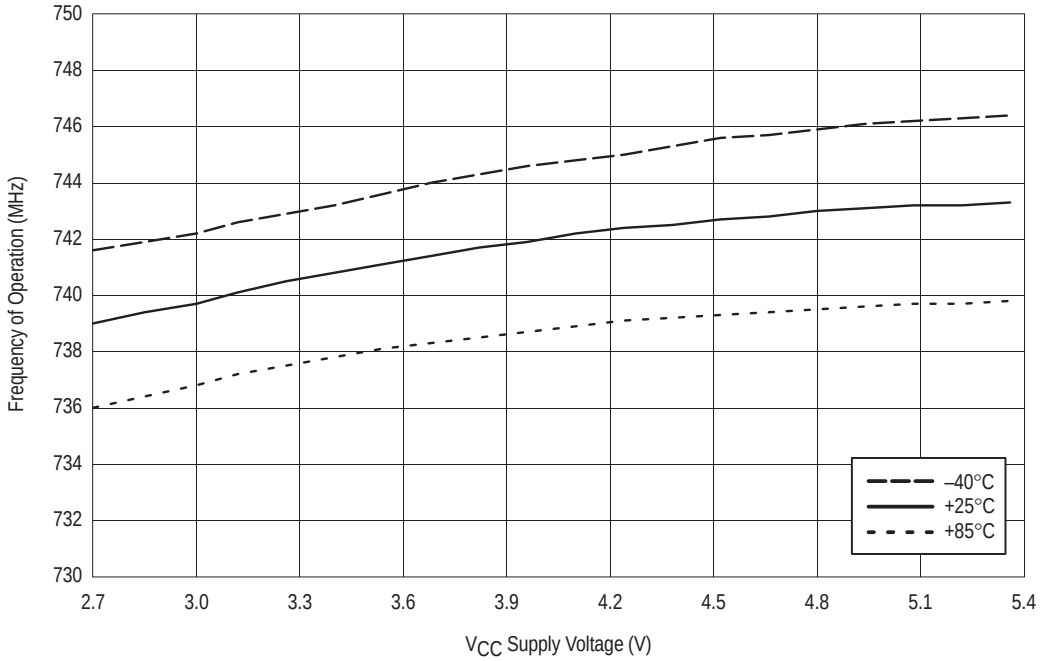


Figure 6. Typical Q/QB Output Power versus Supply, 750 MHz Tank

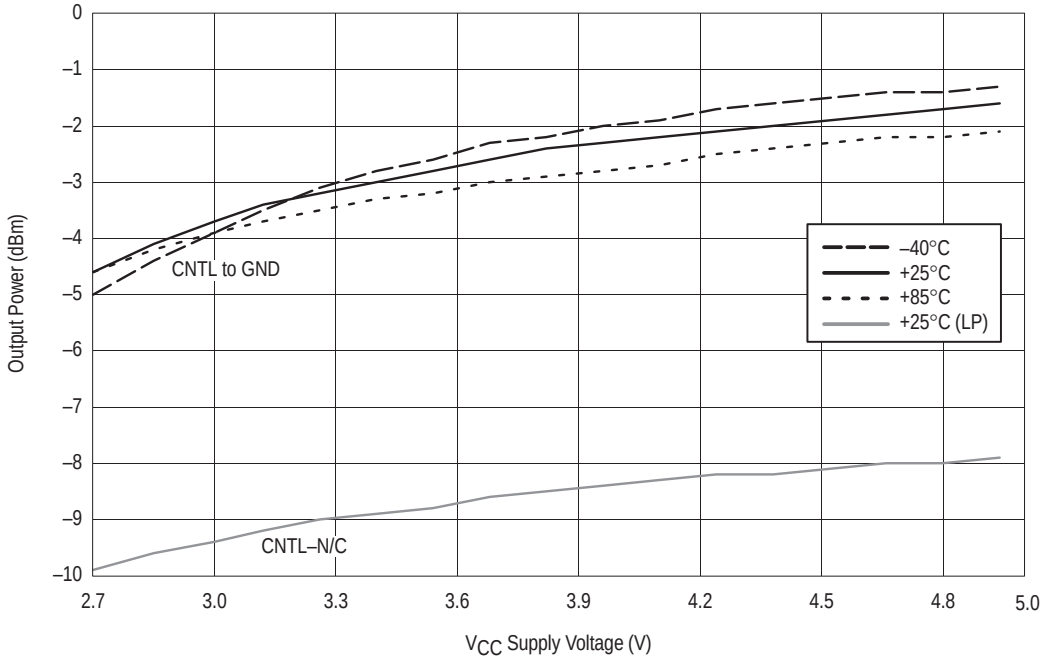


Figure 7. Typical Current Drain versus Supply, 750 MHz Tank

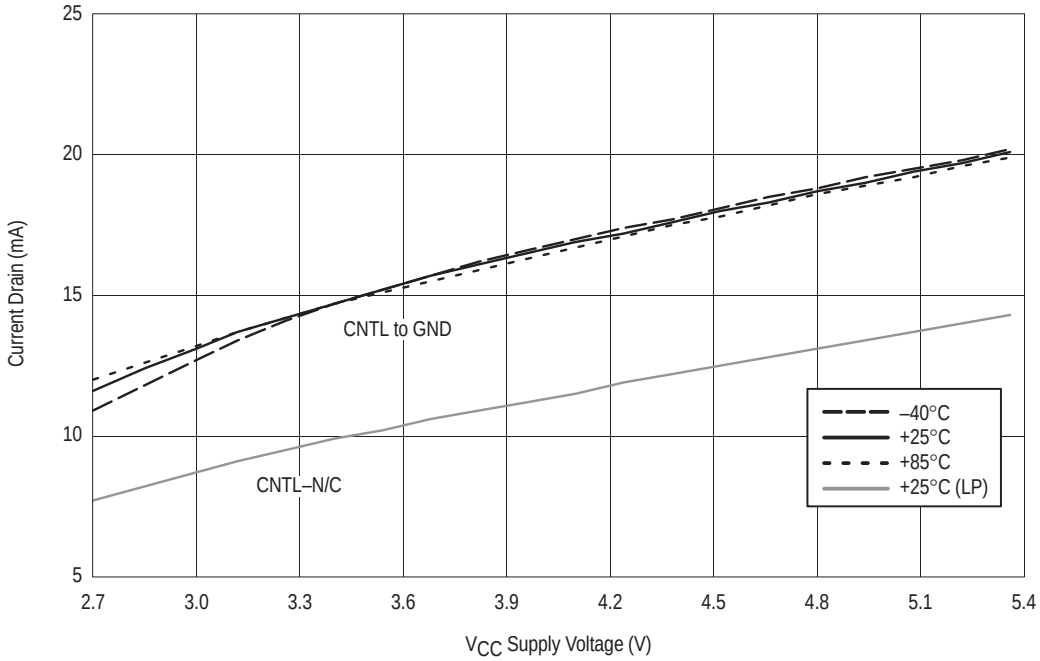


Figure 8. Typical VCO Tuning Curve, 1200 MHz Tank
(V_{CC} = 5.0 V)

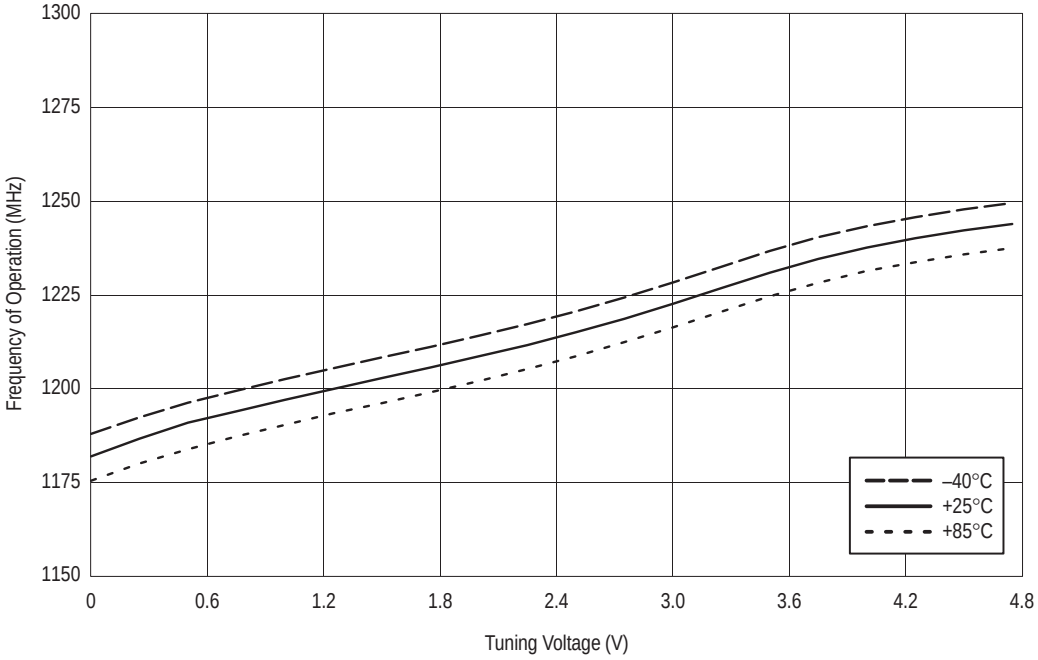


Figure 9. Typical Supply Pushing, 1200 MHz Tank

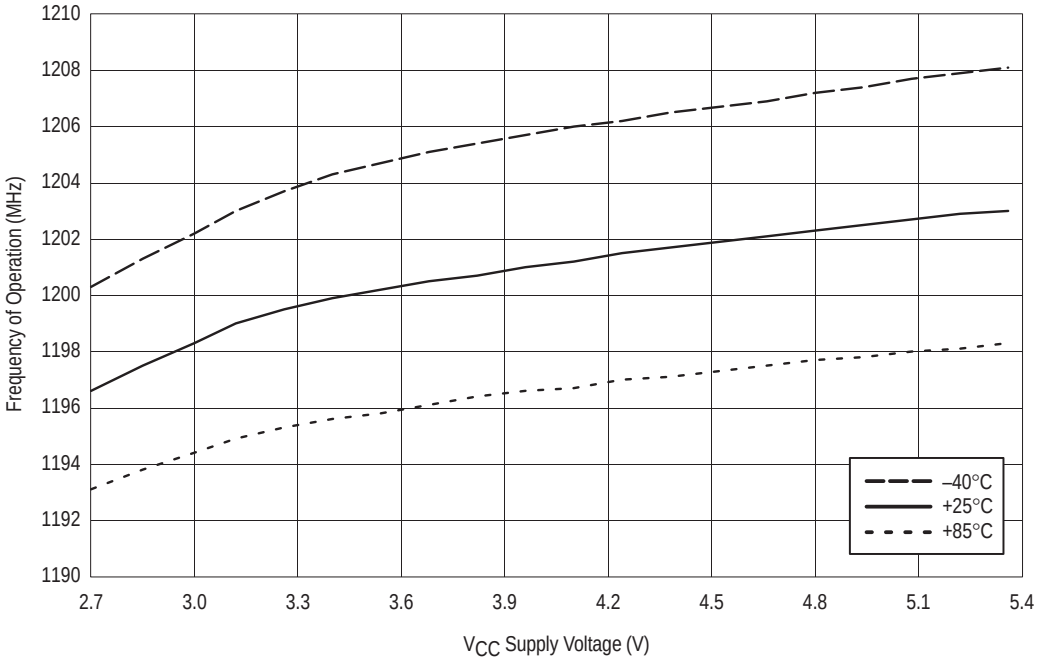


Figure 10. Q/QB Output Power versus Supply, 1200 MHz Tank

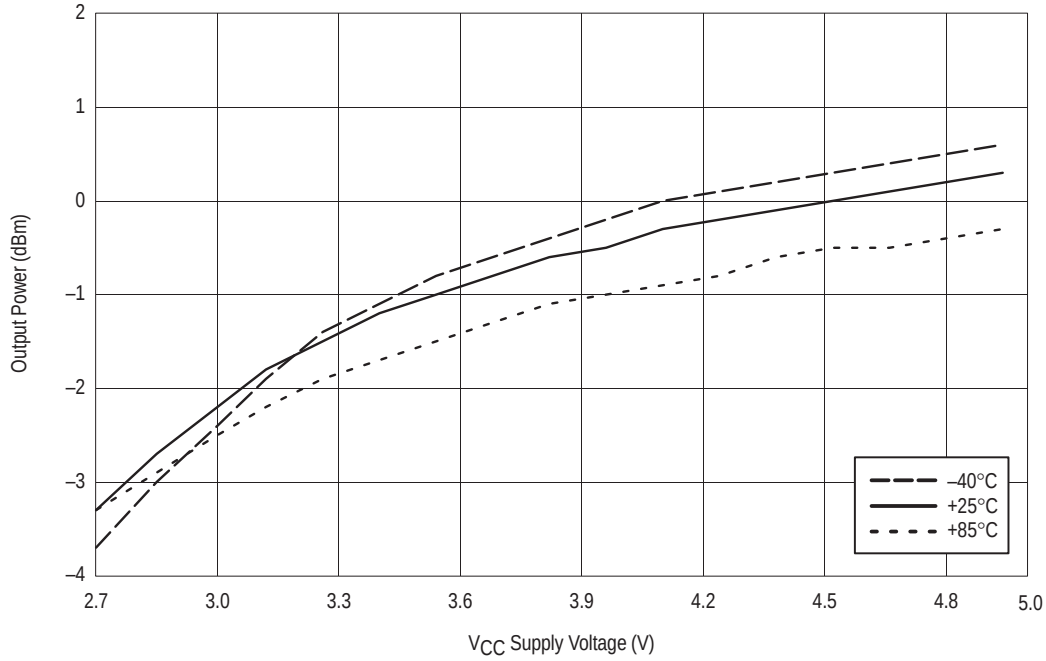


Figure 11. Typical VCO Output Spectrum

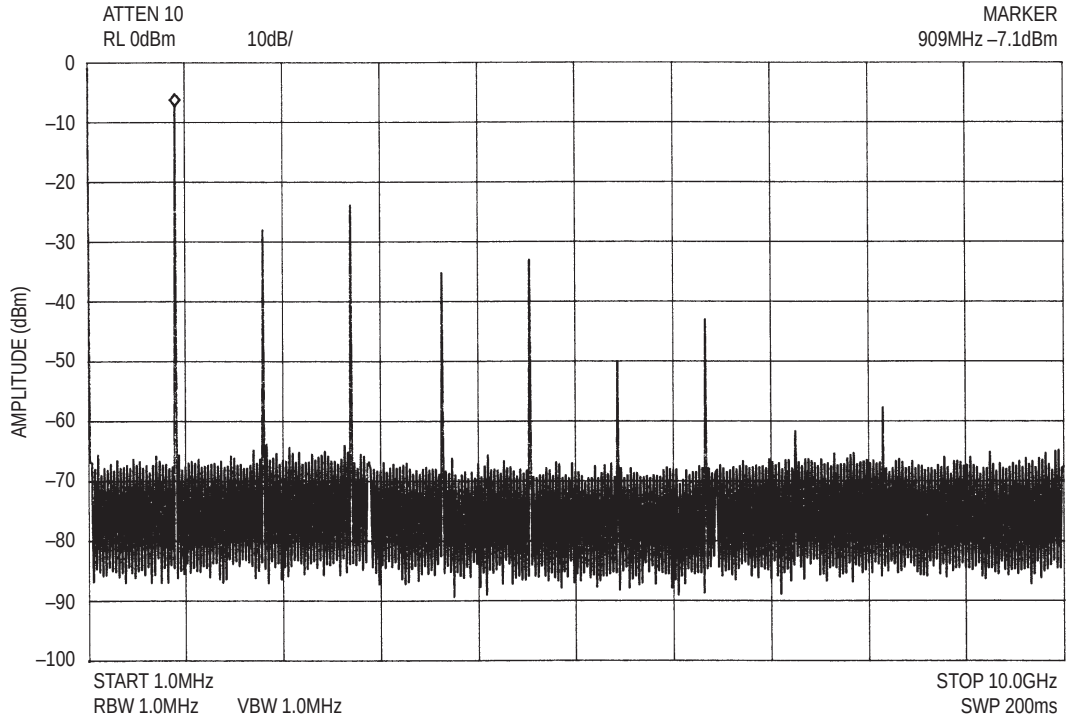


Figure 12. Typical Phase Noise Plot, 750 MHz Tank

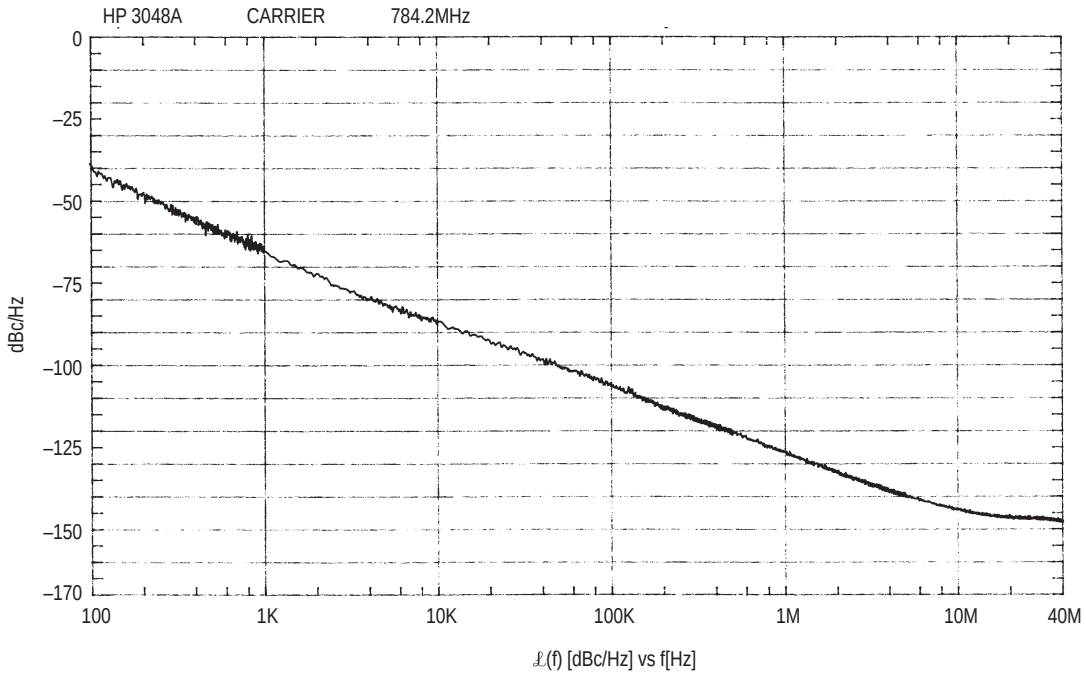
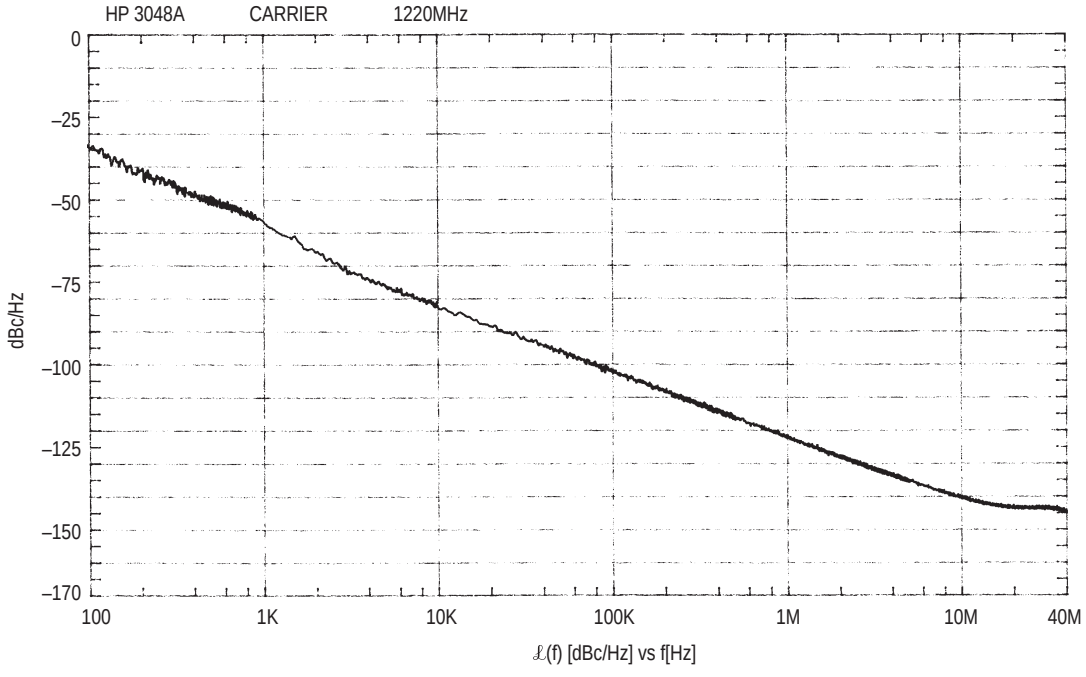


Figure 13. Typical Phase Noise Plot, 1200 MHz Tank



MOTOROLA

MC12148

Low Power Voltage Controlled Oscillator

The MC12148 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C). A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). This device may also be used in many other applications requiring a fixed frequency clock.

The MC12148 is ideal in applications requiring a local oscillator. Systems include electronic test equipment and digital high–speed telecommunications.

The MC12148 is based on the VCO circuit topology of the MC1648. The MC12148 has been realized utilizing Motorola's MOSAIC III advanced bipolar process technology which results in a design which can operate at a much higher frequency than the MC1648 while utilizing half the current. Please consult with the MC1648 data sheet for additional background information.

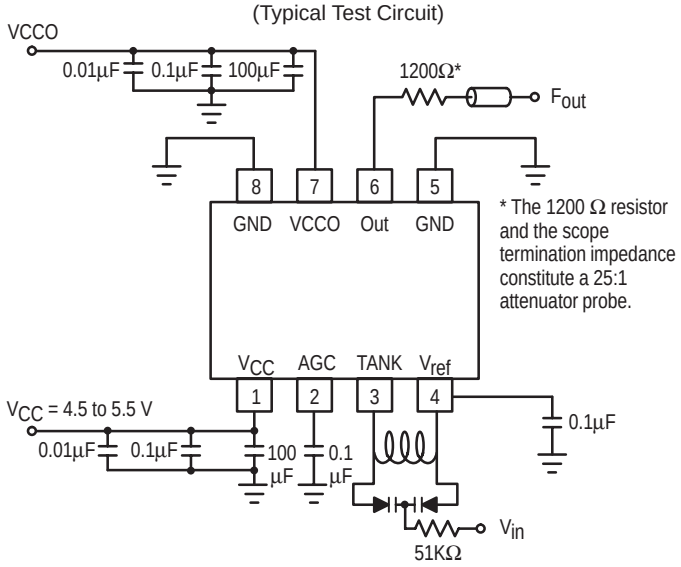
The ECL output circuitry of the MC12148 is not a traditional open emitter output structure and instead has an on–chip termination resistor with a nominal value of 500 ohms. This facilitates direct ac–coupling of the output signal into a transmission line. Because of this output configuration, an external pull–down resistor is not required to provide the output with a dc current path. This output is intended to drive one ECL load. If the user needs to fanout the signal, an ECL buffer such as the MC10EL16 Line Receiver/Driver should be used.

NOTE: The MC12148 is NOT useable as a crystal oscillator.

- Typical Operating Frequency Up to 1100 MHz
- Low–Power 20 mA at 5.0 Vdc Power Supply
- 8–Pin SOIC Package
- Phase Noise –90 dBc/Hz at 25 kHz Typical

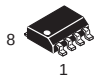
NOT RECOMMENDED FOR NEW DESIGN
DEVICE TO BE PHASED OUT.
Consider MC12149 for New Designs.

BLOCK DIAGRAM
(Typical Test Circuit)



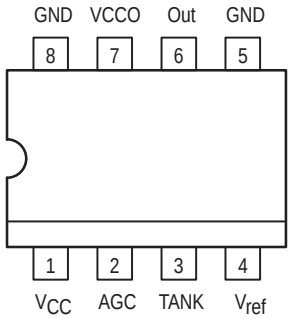
LOW POWER VOLTAGE CONTROLLED OSCILLATOR

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12148D	T_A = –40 to 85°C	SO–8

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage, Pins 1, 7	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V; T_A = –40 to 85°C, unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{CC}	–	19	25	mA
Output Level HIGH (1.0 MΩ Impedance)		V_{OH}	3.95	4.17	4.61	V
Output Level LOW (1.0 MΩ Impedance)		V_{OL}	3.04	3.41	3.60	V
CSR @ 25 kHz Offset, 1.0 Hz BW		$\mathcal{L}$(f)	–	–90	–	dBc/Hz
CSR @ 1.0 MHz Offset, 1.0 Hz BW		$\mathcal{L}$(f)	–	–120	–	dBc/Hz
SNR (Signal to Noise Ratio from Carrier)		SNR	–	40	–	dB
Frequency Stability	Supply Drift	Fsts	–	3.6	–	KHz/mV
	Thermal Drift	Fstt	–	0.1	–	KHz/°C
Second Harmonic (from Carrier)		H2	–	–25	–	dBc

Figure 1. Circuit Schematic

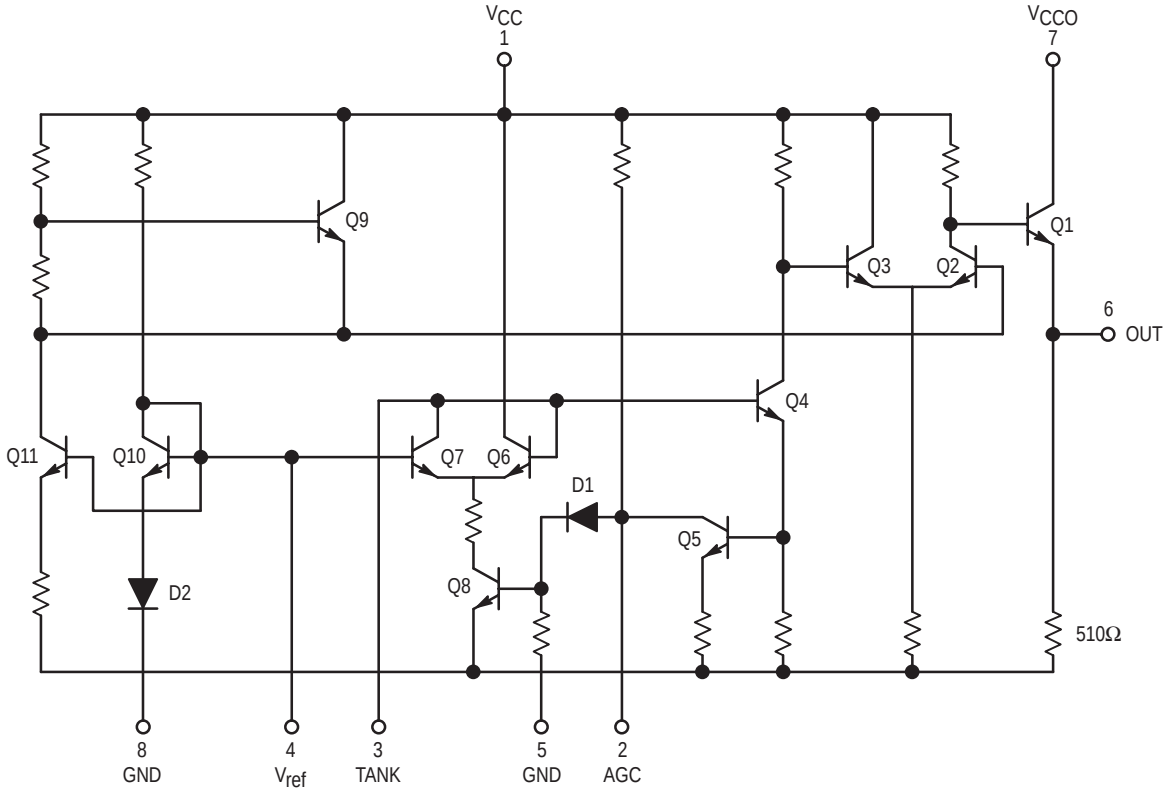
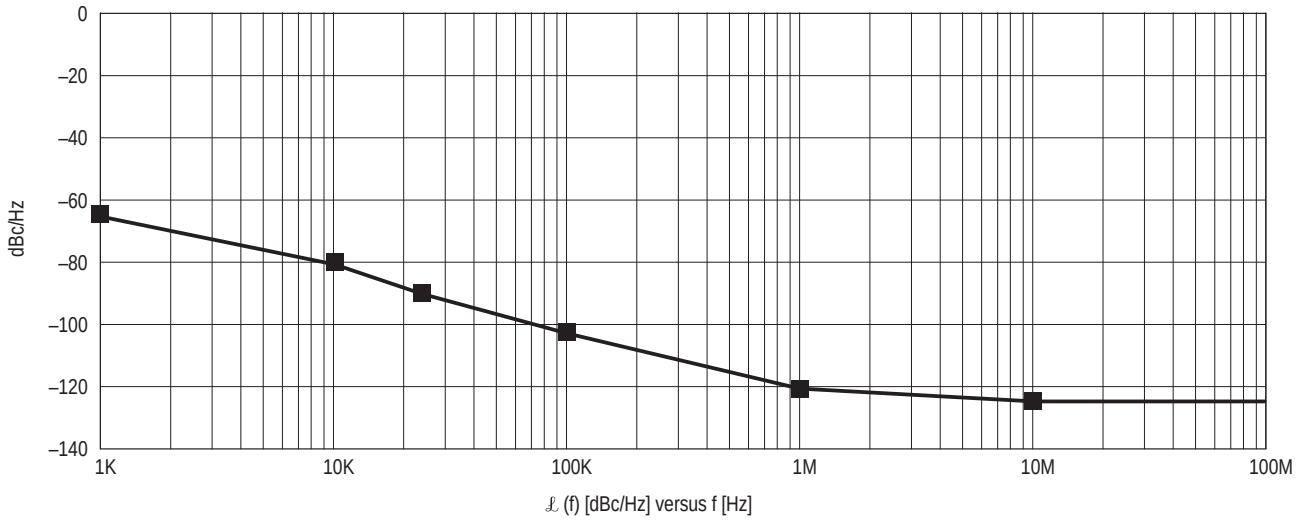


Figure 2. Typical Evaluation Results
(CSR MC12148 5.0 Vdc; V_{CC} @ 25°C; 930 MHz CW)



Tank Component Suppliers

Below are suppliers who manufacture tuning varactors and inductors which can be used to build an external tank circuit. Motorola has used these varactors and inductors for evaluation purposes, however, there are other vendors who manufacture similar products.

Coilcraft Inductors A01T thru A05T
Coilcraft–Coilcraft, Inc.
1102 Silver Lake Rd.
Gary, Illinois 60013
708–639–6400

Loral Tuning Varactors GC1500 Series
Loral
16 Maple Road
Chelmsford, Massachusetts 01824
508–256–8101 or 508–256–4113

Alpha Tuning Diodes DVH6730 Series
Alpha Semiconductor Devices Division
20 Sylvan Road
Woburn, MA 01801
617–935–5150

* At 1.1 GHz, use a Coilcraft A0IT Springair coil at 2.5 nH and a Loral Varactor 3.0 to 8.0 pF at V_{IN} = 1.0 to 5.0 V.

MOTOROLA

MC12149

Low Power Voltage Controlled Oscillator Buffer

The MC12149 is intended for applications requiring high frequency signal generation up to 1300 MHz. An external tank circuit is used to determine the desired frequency of operation. The VCO is realized using an emitter–coupled pair topology. The MC12149 can be used with an integrated PLL IC such as the MC12202 1.1 GHz Frequency Synthesizer to realize a complete PLL sub–system. The device is specified to operate over a voltage supply range of 2.7 to 5.5 V. It has a typical current consumption of 15 mA at 3.0 V which makes it attractive for battery operated handheld systems.

NOTE: The MC12149 is NOT suitable as a crystal oscillator.

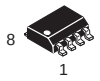
- Operates Up to 1.3 GHz
- Space–Efficient 8–Pin SOIC or SSOP Package
- Low Power 15 mA Typical @ 3.0 V Operation
- Supply Voltage of 2.7 to 5.5 V
- Typical 900 MHz Performance
  - Phase Noise –105 dBc/Hz @ 100 kHz Offset
  - Tuning Voltage Sensitivity of 20 MHz/V
- Output Amplitude Adjustment Capability
- Two High Drive Outputs With a Typical Range from –8.0 to –2.0 dBm
- One Low–Drive Output for Interfacing to a Prescaler

The device has three high frequency outputs which make it attractive for transceiver applications which require both a transmit and receive local oscillator (LO) signal as well as a lower amplitude signal to drive the prescaler input of the frequency synthesizer. The outputs Q and QB are available for servicing the receiver IF and transmitter up–converter single–ended. In receiver applications, the outputs can be used together if it is necessary to generate a differential signal for the receiver IF. Because the Q and QB outputs are open collector, terminations to the V_{CC} supply are required for proper operation. Since the outputs are complementary, BOTH outputs must be terminated even if only one is needed. The Q and QB outputs have a nominal drive level of –8dBm to conserve power. If addition signal amplitude is needed, a level adjustment pin (CNTL) is available, which when tied to ground, boosts the nominal output levels to –2.0 dBm. A low power VCO output (Q2) is also provided to drive the prescaler input of the PLL. The amplitude of this signal is nominally 500 mV which is suitable for most prescalers.

External components required for the MC12149 are: (1) tank circuit (LC network); (2) Inductor/capacitor to provide the termination for the open collector outputs; and (3) adequate supply voltage bypassing. The tank circuit consists of a high–Q inductor and varactor components. The preferred tank configuration allows the user to tune the VCO across the full supply range. VCO performance such as center frequency, tuning voltage sensitivity, and noise characteristics are dependent on the particular components and configuration of the VCO tank circuit.

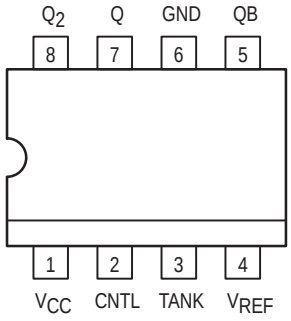
LOW POWER VOLTAGE CONTROLLED OSCILLATOR BUFFER

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12149D	T_A = –40 to 85°C	SO–8

PIN NAMES

Pin	Function
V_{CC}	Power Supply
CNTL	Amplitude Control for Q, QB Output Pair
TANK	Tank Circuit Input
V_{REF}	Bias Voltage Output
QB	Open Collector Output
GND	Ground
Q	Open Collector Output
Q_2	Low Power Output

MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 1	V_{CC}	-0.5 to 7.0	V
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C
Maximum Output Current, Pin 8	I_O	7.5	mA
Maximum Output Current, Pin 5,7	I_O	12	mA

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 VDC, T_A = -40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (CNTL=GND) V_{CC} = 3.3 V V_{CC} = 5.5 V	I_{CC}	– –	16 23.5	20 30	mA
Supply Current (CNTL=OPEN) V_{CC} = 3.3 V V_{CC} = 5.5 V	I_{CC}	– –	10 15	15.0 24.5	mA
Output Amplitude (Pin 8) V_{CC} = 2.7 V High Impedance Load V_{CC} = 2.7 V	V_{OH}, V_{OL}	1.75 1.20	1.85 1.35	1.95 1.50	V
Output Amplitude (Pin 8) V_{CC} = 5.5 V High Impedance Load V_{CC} = 5.5 V	V_{OH}, V_{OL}	4.50 3.85	4.6 4.0	4.70 4.15	V
Output Amplitude (Pin 5 & 7) [Note 1] V_{CC} = 2.7 V 50 Ω to V_{CC} V_{CC} = 2.7 V	V_{OH}, V_{OL}	2.6 2.1	2.7 2.3	– 2.4	V
Output Amplitude (Pin 5 & 7) [Note 1] V_{CC} = 5.5 V 50Ω to V_{CC} V_{CC} = 5.5V	V_{OH}, V_{OL}	5.4 4.8	5.5 5.0	– 5.1	V
Tuning Voltage Sensitivity [Notes 2 and 3]	T_{stg}	–	20	–	MHz/V
Frequency of Operation	F_C	100	–	1300	MHz
CSR at 10 kHz Offset, 1Hz BW [Notes 2 and 3]	ℒ(f)	–	–85	–	dBc/Hz
CSR at 100 kHz Offset, 1Hz BW [Notes 2 and 3]	ℒ(f)	–	–105	–	dBc/Hz
Frequency Stability [Notes 3 and 4] Supply Drift Thermal Drift	 F_{sts} f_{stt}	 – –	 0.8 50	 – –	 MHz/V KHz/°C

NOTES: 1. CNTL pin tied to ground.
2. Actual performance depends on tank components selected.
3. See Figure 12, 750 MHz tank.
4. T = 25°C, V_{CC} = 5.0 V ±10%

OPERATIONAL CHARACTERISTICS

A simplified schematic of the MC12149 is found in Figure 1. The oscillator incorporates positive feedback by coupling the base of transistor Q2 to the collector of transistor Q1. In order to minimize interaction between the VCO outputs and the oscillator tank transistor pair, a buffer is incorporated into the circuit. This differential buffer is realized by the Q3 and Q4 transistor pair. The differential buffer drives the gate which contains the primary open collector outputs, Q and QB. The output is actually a current which has been set by an internal bias driver to a nominal current of 4mA. Additional circuitry is incorporated into the tail of the current source which allows the current source to be increased to approximately 10 mA. This is accommodated by the addition of a resistor which is brought out to the CNTL pin. When this pin is tied to ground, the additional current is sourced through the current source thus increasing the output amplitude of the Q/QB output pair. If less than 10mA of current is needed, a resistor can be added to ground which reduces the amount of current.

The Q/QB outputs drive an additional differential buffer which generate the Q2 output signal. To minimize current, the circuit is realized as an emitter–follower buffer with an on chip pull down resistor. This output is intended to drive the prescaler input of the PLL synthesizer block.

APPLICATION INFORMATION

Figure 2 illustrates the external components necessary for the proper operation of the VCO buffer. The tank circuit configuration in this figure allows the VCO to be tuned across the full operating voltage of the power supply. This is very important in 3.0 V applications where it is desirable to utilize as much of the operating supply range as possible so as to minimize the VCO sensitivity (MHz/V). In most situations, it is desirable to keep the sensitivity low so the circuit will be less susceptible to external noise influences. An additional benefit to this configuration is that additional regulation/ filtering can be incorporated into the V_{CC} line without compromising the tuning range of the VCO. With the ac–coupled tank configuration, the V_{tune} voltage can be greater than the V_{CC} voltage supplied to the device.

There are four main areas that the user directly influences the performance of the VCO. These include Tank Design, Output Termination Selection, Power Supply Decoupling, and Circuit Board Layout/Grounding.

The design of the tank circuit is critical to the proper operation of the VCO. This tank circuit directly impacts the main VCO operating characteristics:

1) Frequency of Operation
2) Tuning Sensitivity
3) Voltage Supply Pushing
4) Phase Noise Performance

The tank circuit, in its simplest form, is realized as an LC circuit which determines the VCO operating frequency. This is described in Equation 1.

$$f_o = \frac{1}{2\pi \sqrt{LC}} \qquad \text{Equation 1}$$

In the practical case, the capacitor is replaced with a varactor diode whose capacitance changes with the voltage applied, thus changing the resonant frequency at which the VCO tank operates. The capacitive component in Equation 1 also needs to include the input capacitance of the device and other circuit and parasitic elements. Typically, the inductor is realized as a surface mount chip or a wound–coil. In addition, the lead inductance and board inductance and capacitance also have an impact on the final operating point.

Figure 1. Simplified Schematic

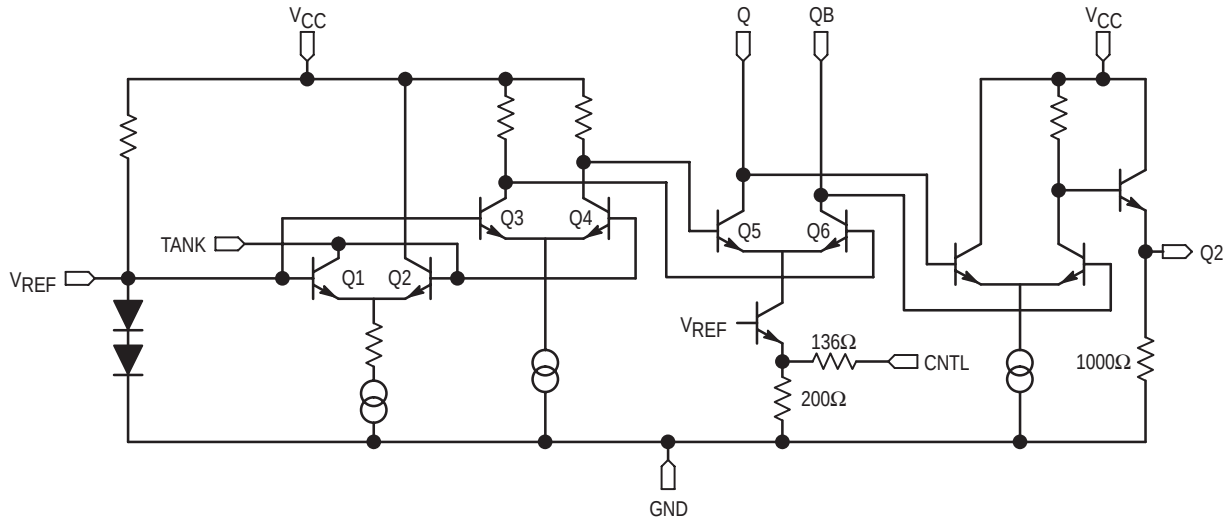
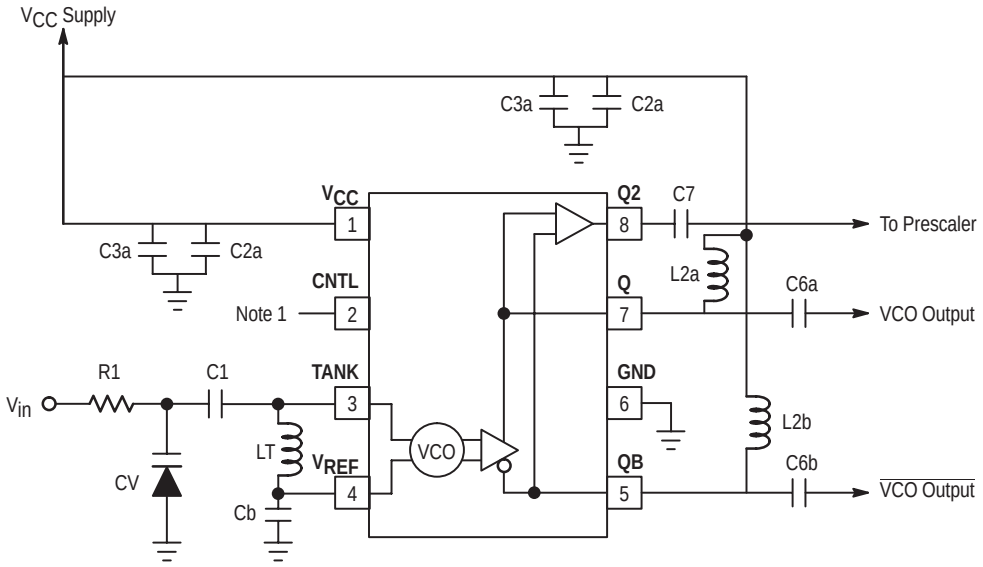


Figure 2. MC12149 Typical External Component Connections



1. This input can be left open, tied to ground, or tied with a resistor to ground, depending on the desired output amplitude needed at the Q and QB output pair.
2. Typical values for R1 range from 5.0 kΩ to 10 kΩ.

A simplified linear approximation of the device, package, and typical board parasitics has been developed to aid the designer in selecting the proper tank circuit values. All the parasitic contributions have been lumped into a parasitic capacitive component and a parasitic inductive component. While this is not entirely accurate, it gives the designer a solid starting point for selecting the tank components.

Below are the parameters used in the model.

Cp Parasitic Capacitance
Lp Parasitic Inductance
LT Inductance of Coil
C1 Coupling Capacitor Value
Cb Capacitor for decoupling the Bias Pin
CV Varactor Diode Capacitance (Variable)

The values for these components are substituted into the following equations:

$$Ci = \frac{C1 \times CV}{C1 + CV} + Cp \qquad \text{Equation 2}$$

$$C = \frac{Ci \times Cb}{Ci + Cb} \qquad \text{Equation 3}$$

$$L = Lp + LT \qquad \text{Equation 4}$$

From Figure 2, it can be seen that the varactor capacitance (CV) is in series with the coupling capacitor (C1). This is calculated in Equation 2. For analysis purposes, the parasitic capacitances (CP) are treated as a lumped element and placed in parallel with the series combination of C1 and CV. This compound capacitance (Ci) is in series with the bias capacitor (Cb) which is calculated in Equation 3. The influences of the various capacitances; C1, CP, and Cb, impact the design by reducing the variable capacitance effects of the varactor which controls the tank resonant frequency and tuning range.

Now the results calculated from Equation 2, Equation 3 and Equation 4 can be substituted into Equation 1 to calculate the actual frequency of the tank.

To aid in analysis, it is recommended that the designer use a simple spreadsheet based on Equation 1 through Equation 4 to calculate the frequency of operation for various varactor/inductor selections before determining the initial starting condition for the tank.

The two main components at the heart of the tank are the inductor (LT) and the varactor diode (CV). The capacitance of a varactor diode junction changes with the amount of reverse bias voltage applied across the two terminals. This is the element which actually “tunes” the VCO. One characteristic of the varactor is the tuning ratio which is the ratio of the capacitance at specified minimum and maximum voltage points. For characterizing the MC12149, a Matsushita (Panasonic) varactor – MA393 was selected. This device has a typical capacitance of 11 pF at 1.0 V and 3.7 pF at 4.0 V and the C–V characteristic is fairly linear over that range. Similar performance was also acheived with Loral varactors. A multi–layer chip inductor was used to realize the LT component. These inductors had typical Q values in the 35 to 50 range for frequencies between 500 and 1000 MHz.

Note: There are many suppliers of high performance varactors and inductors and Motorola can not recommend one vendor over another.

The Q (quality factor) of the components in the tank circuit has a direct impact on the resulting phase noise of the oscillator. In general, the higher the Q, the lower the phase noise of the resulting oscillator. In addition to the LT and CV components, only high quality surface–mount RF chip capacitors should be used in the tank circuit. These capacitors should have very low dielectric loss (high–Q). At a minimum, the capacitors selected should be operating 100 MHz below their series resonance point. As the desired frequency of operation increases, the values of the C1 and Cb capacitors will decrease since the series resonance point

is a function of the capacitance value. To simplify the selection of C1 and Cb, a table has been constructed based on the intended operating frequency to provide recommended starting points. These may need to be altered depending on the value of the varactor selected.

Frequency	C1	Cb
200 – 500 MHz	47 pF	47 pF
500 – 900 MHz	5.1 pF	15 pF
900 – 1200 MHz	2.7 pF	15 pF

The value of the Cb capacitor influences the VCO supply pushing. To minimize pushing, the Cb capacitor should be kept small. Since C1 is in series with the varactor, there is a strong relationship between these two components which influences the VCO sensitivity. Increasing the value of C1 tends to increase the sensitivity of the VCO.

The parasitic contributions Lp and Cp are related to the MC12149 as well as parasitics associated with the layout, tank components, and board material selected. The input capacitance of the device, bond pad, the wire bond, package/lead capacitance, wire bond inductance, lead inductance, printed circuit board layout, board dielectric, and proximity to the ground plane all have an impact on these parasitics. For example, if the ground plane is located directly below the tank components, a parasitic capacitor will be formed consisting of the solder pad, metal traces, board dielectric material, and the ground plane. The test fixture used for characterizing the device consisted of a two sided copper clad board with ground plane on the back. Nominal values where determined by selecting a varactor and characterizing the device with a number of different tank/ frequency combinations and then performing a curve fit with the data to determine values for Lp and Cp. The nominal values for the parasitic effects are seen below:

Parasitic Capacitance	Cp	4.2 pF
Parasitic Inductance	Lp	2.2 nH

These values will vary based on the users unique circuit board configuration.

Basic Guidelines:

1. Select a varactor with high Q and a reasonable capacitance versus voltage slope for the desired frequency range.
2. Select the value of Cb and C1 from the table above .
3. Calculate a value of inductance (L) which will result in achieving the desired center frequency. Note that L includes both LT and Lp.
4. Adjust the value of C1 to achieve the proper VCO sensitivity.
5. Re–adjust value of L to center VCO.
6. Prototype VCO design using selected components. It is important to use similar construction techniques and materials, board thickness, layout, ground plane spacing as intended for the final product.
7. Characterize tuning curve over the voltage operation conditions.
8. Adjust, as necessary, component values – L,C1, and Cb to compensate for parasitic board effects.
9. Evaluate over temperature and voltage limits.
10. Perform worst case analysis of tank component variation to insure proper VCO operation over full temperature and voltage range and make any adjustments as needed.

Outputs Q and QB are open collector outputs and need a inductor to VCC to provide the voltage bias to the output transistor. In most applications, DC–blocking capacitors are placed in series with the output to remove the DC component before interfacing to other circuitry. These outputs are complementary and should have identical inductor values for each output. This will minimize switching noise on the VCC supply caused by the outputs switching. It is important that both outputs be terminated, even if only one of the outputs is used in the application.

Referring to Figure 2, the recommended value for L2a and L2b should be 47 nH and the inductor components resonance should be at least 300 MHz greater than the maximum operating frequency. For operation above 1100 MHz, it may be necessary to reduce that inductor value to 33 nH. The recommended value for the coupling capacitors C6a, C6b, and C7 is 47 pF. Figure 2 also includes decoupling capacitors for the supply line as well as decoupling for the output inductors. Good RF decoupling practices should be used with a series of capacitors starting with high quality 100 pF chip capacitors close to the device. A typical layout is shown below in Figure 3.

The output amplitude of the Q and QB can be adjusted using the CNTL pin. Refering to Figure 1, if the CNTL pin is connected to ground, additional current will flow through the current source. When the pin is left open, the nominal current flowing through the outputs is 4 mA. When the pin is grounded, the current increases to a nominal value of 10 mA. So if a 50 ohm resistor was connected between the outputs and VCC, the output amplitude would change from 200 mV pp to 500 mV pp with an additional current drain for the device of 6 mA. To select a value between 4 and 10 mA, an external resistor can be added to ground. The equation below is used to calculate the current.

$$I_{out(nom)} = \frac{(200 + 136 + R_{ext}) \times 0.8V}{200 \times (136 + R_{ext})}$$

Figure 4 through Figure 13 illustrate typical performance achieved with the MC12149. The curves illustrate the tuning curve, supply pushing characteristics, output power, current drain, output spectrum, and phase noise performance. In most cases, data is present for both a 750 MHz and 1200 MHz tank design. The table below illustrates the component values used in the designs.

Component	750MHz Tank	1200MHz Tank	Units
R1	5000	5000	Ω
C1	5.1	2.7	pF
LT	4.7	1.8	nH
CV	3.7 @ 1.0 V 11 @ 4.0 V	3.7 @ 1.0 V 11 @ 4.0 V	pF
Cb	100*	15	pF
C6, C7	47	33	pF
L2	47	47	nH

NOTE: * The value of Cb should be reduced to minimize pushing.

Figure 3. MC12149 Typical Layout
(Not to Scale)

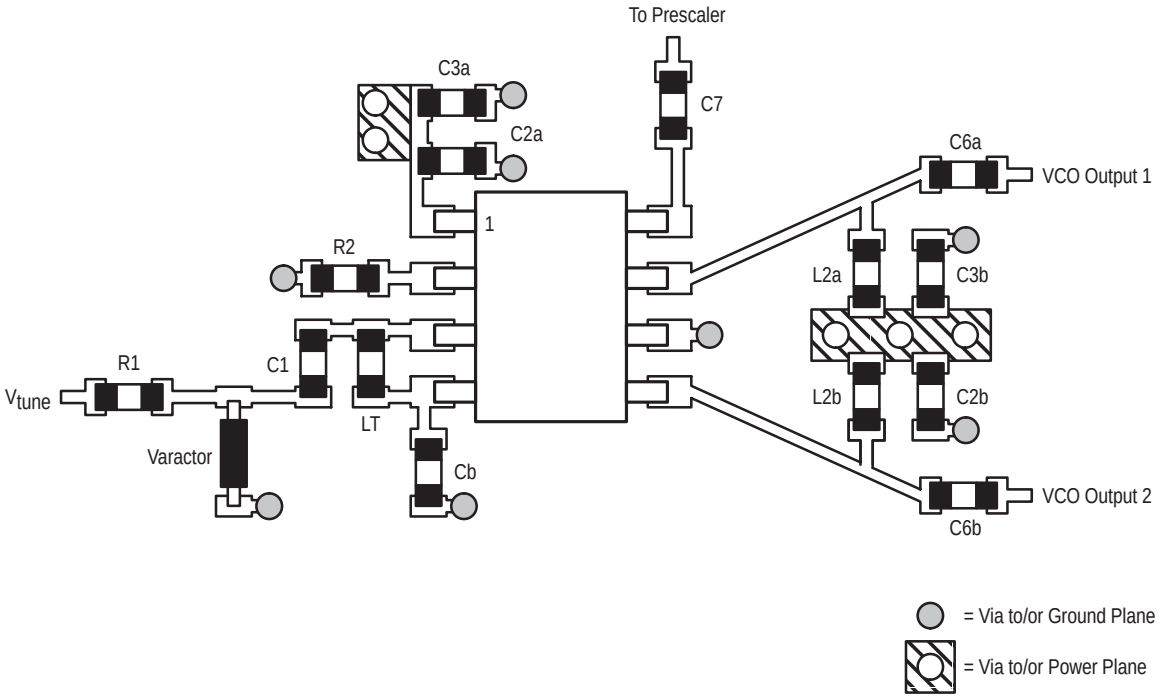


Figure 4. Typical VCO Tuning Curve, 750 MHz Tank

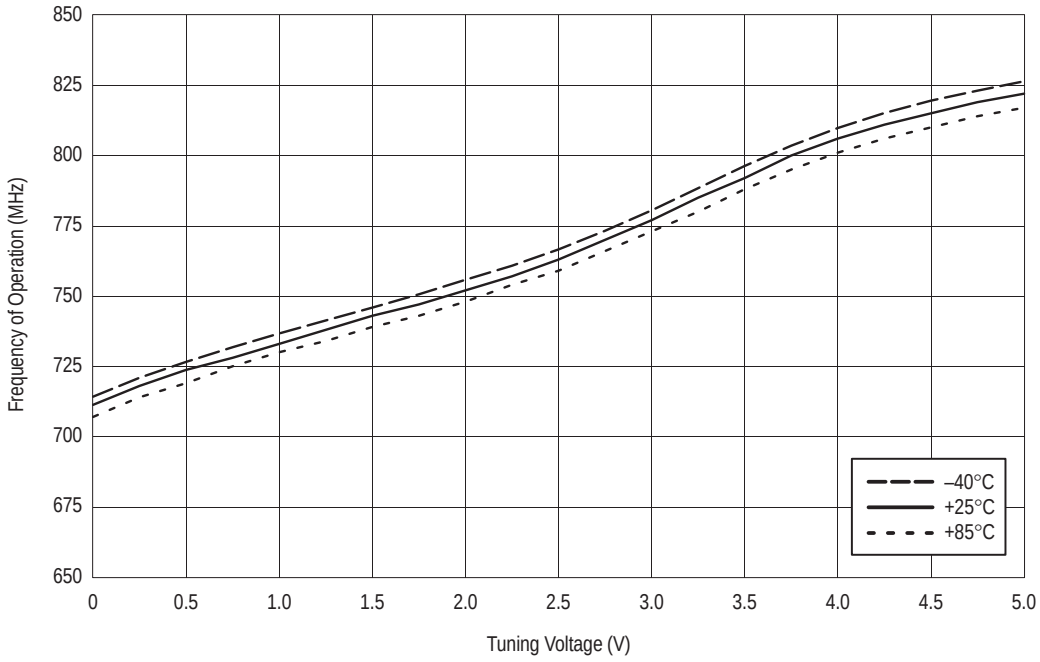


Figure 5. Typical Supply Pushing, 750 MHz Tank

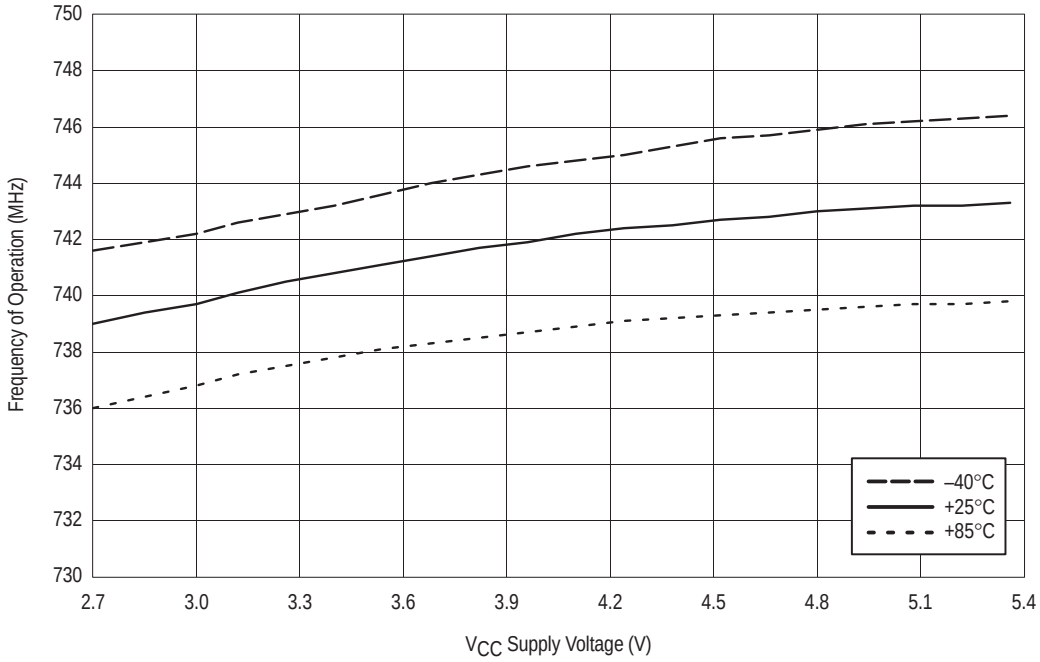


Figure 6. Typical Q/QB Output Power versus Supply, 750 MHz Tank

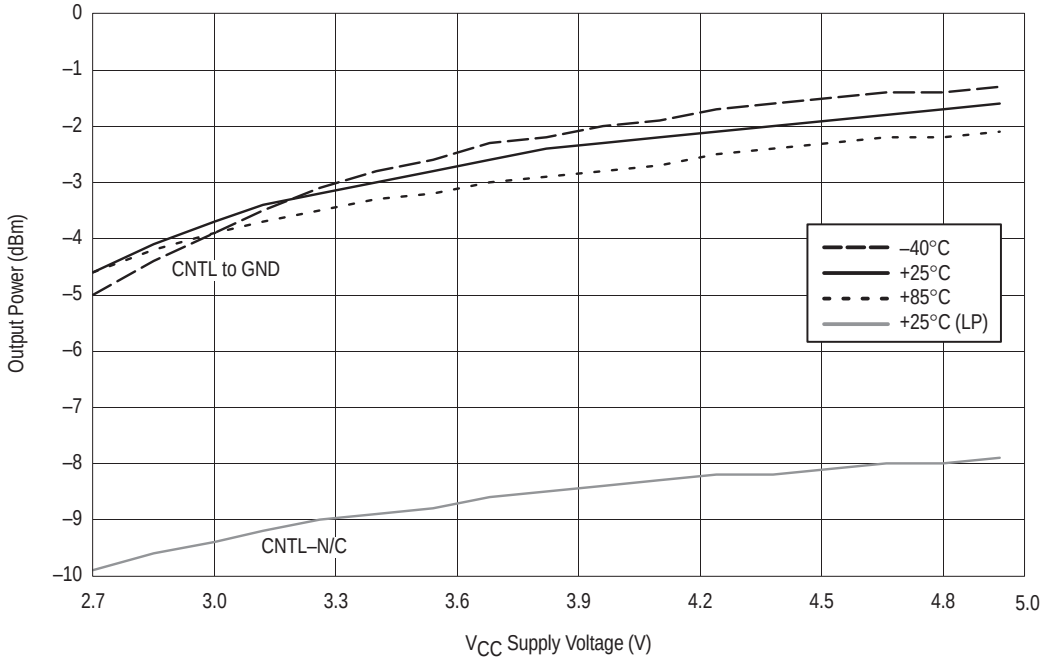


Figure 7. Typical Current Drain versus Supply, 750 MHz Tank

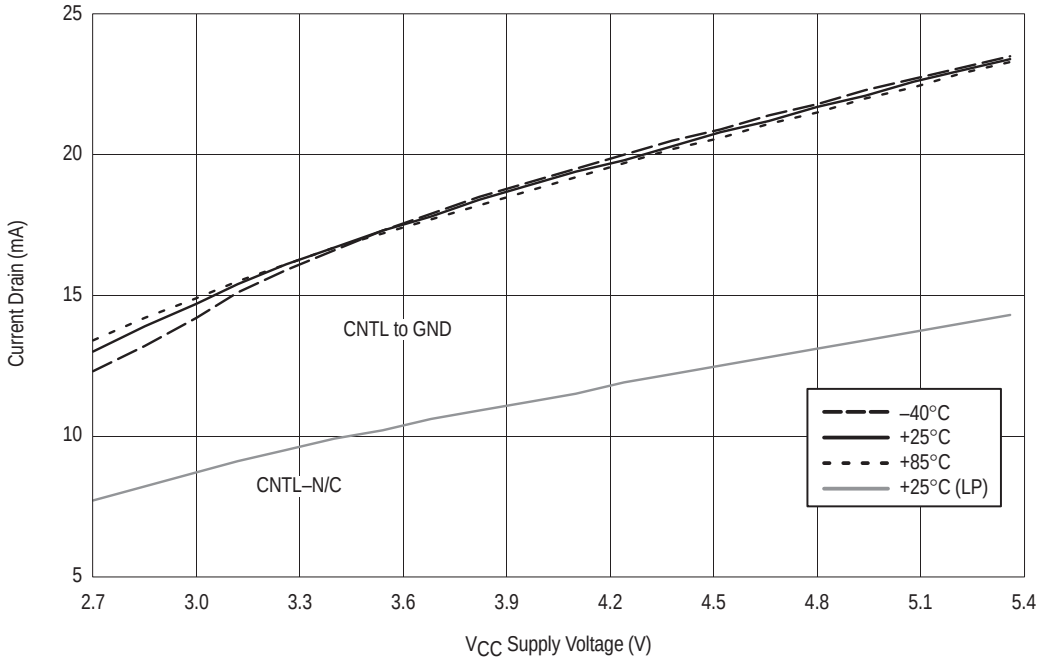


Figure 8. Typical VCO Tuning Curve, 1200 MHz Tank
(V_{CC} = 5.0 V)

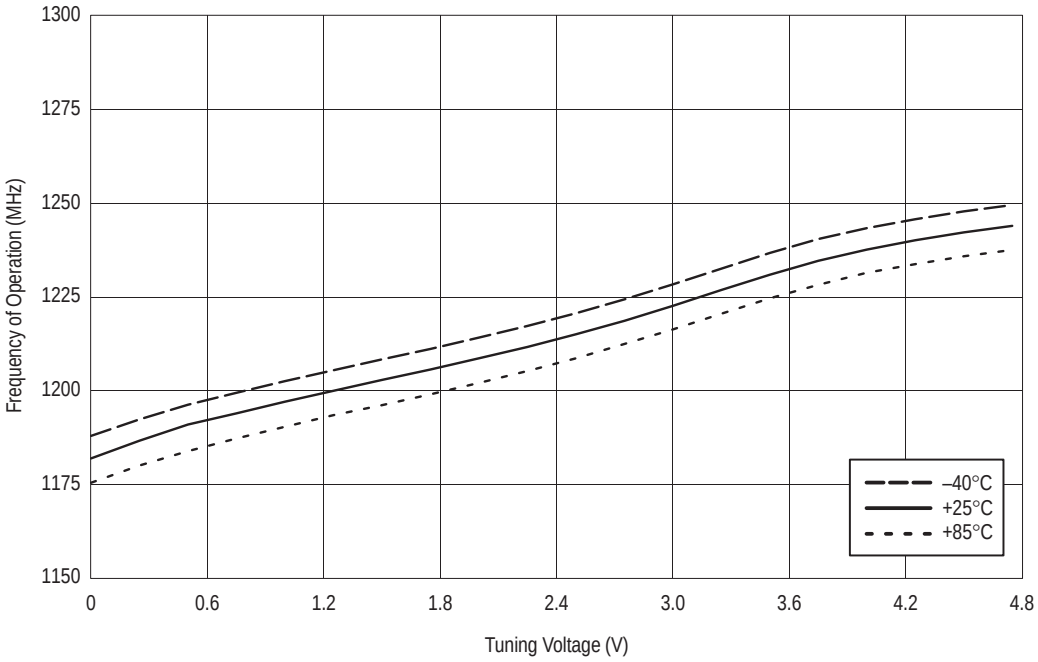


Figure 9. Typical Supply Pushing, 1200 MHz Tank

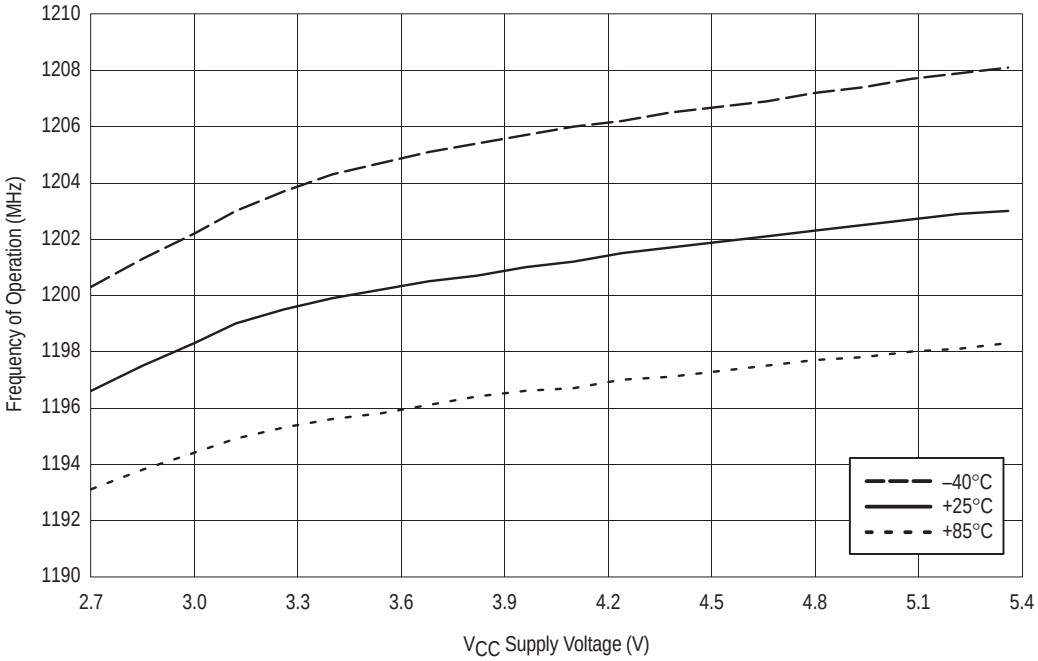


Figure 10. Q/QB Output Power versus Supply, 1200 MHz Tank

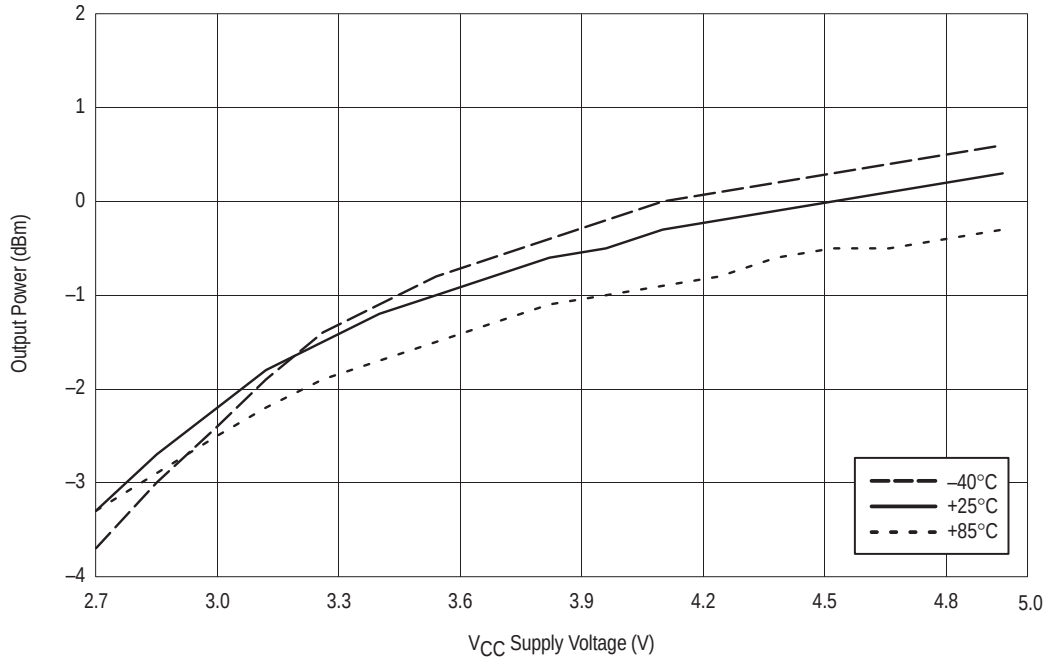


Figure 11. Typical VCO Output Spectrum

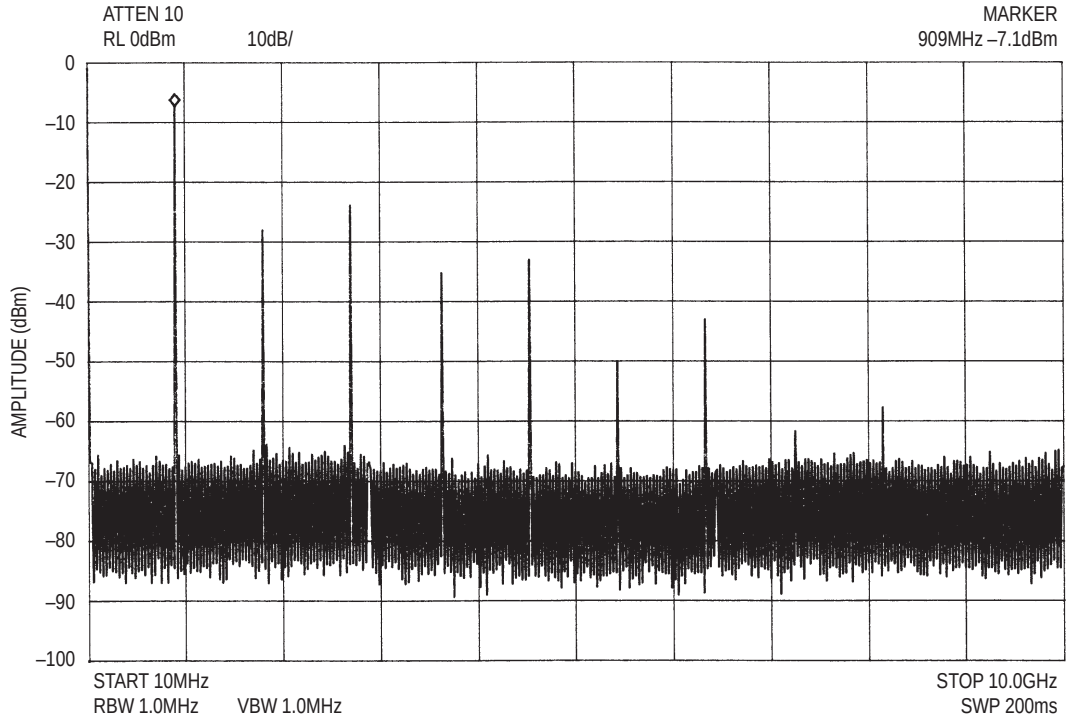


Figure 12. Typical Phase Noise Plot, 750 MHz Tank

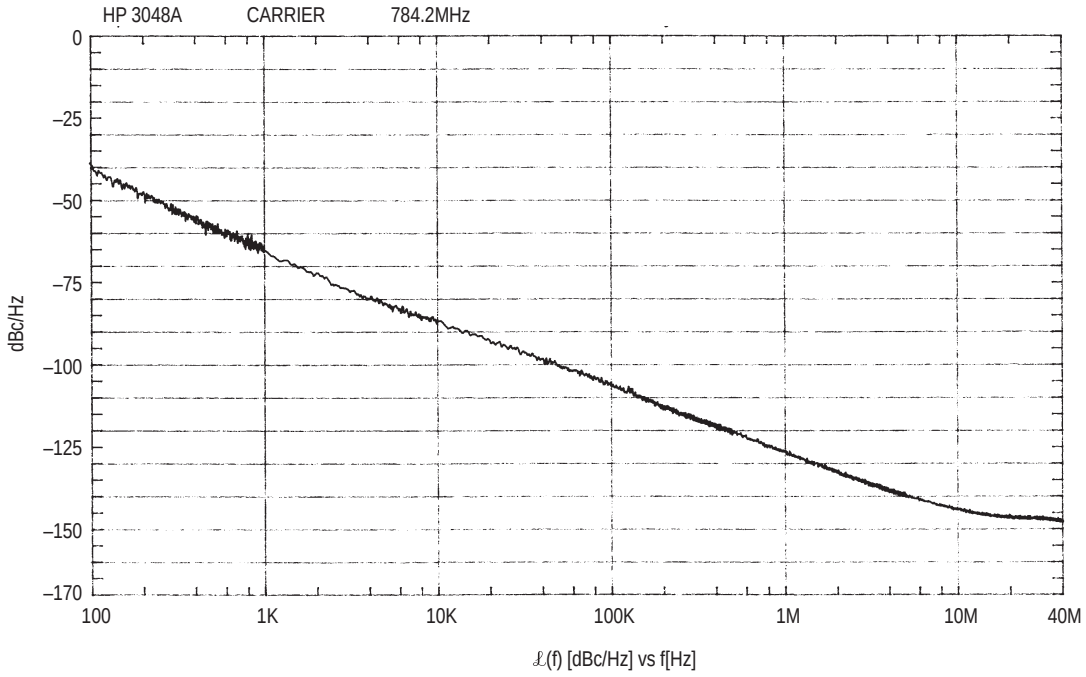
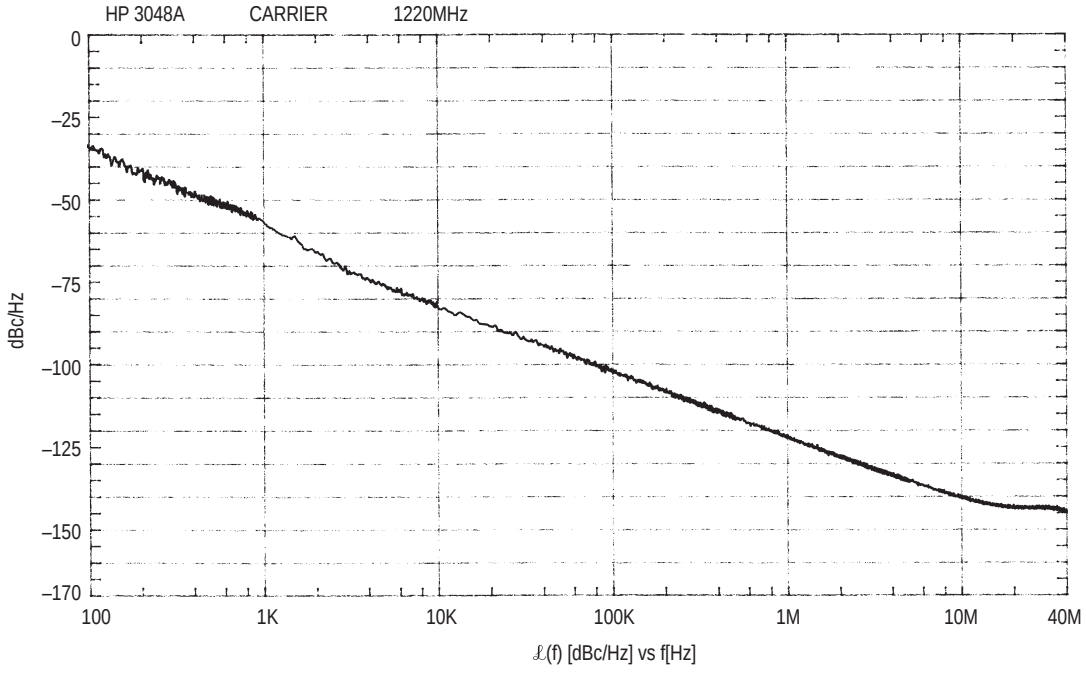


Figure 13. Typical Phase Noise Plot, 1200 MHz Tank



MOTOROLA

MC12179

500–2800 MHz Single Channel Frequency Synthesizer

The MC12179 is a monolithic Bipolar synthesizer integrating the high frequency prescaler, phase/frequency detector, charge pump, and reference oscillator/buffer functions. When combined with an external loop filter and VCO, the MC12179 serves as a complete PLL subsystem. Motorola's advanced MOSAIC™ V technology is utilized for low power operation at a 5.0 V supply voltage. The device is designed for operation up to 2.8 GHz for high frequency applications such as CATV down converters and satellite receiver tuners.

- 2.8 GHz Maximum Operating Frequency
- Low Power Supply Current of 3.5 mA Typical, Including I_{CC} and I_P Currents
- Supply Voltage of 5.0 V Typical
- Integrated Divide by 256 Prescaler
- On–Chip Reference Oscillator/Buffer
  - 2.0 to 11 MHz Operation When Driven From Reference Source
  - 5.0 to 11 MHz Operation When Used With a Crystal
- Digital Phase/Frequency Detector with Linear Transfer Function
- Balanced Charge Pump Output
- Space Efficient 8–Lead SOIC
- Operating Temperature Range of –40 to 85°C

For additional information on calculating the loop filter components, an *InterActiveApNote*™ document containing software (based on a Microsoft Excel spreadsheet) and an Application Note is available. Please order DK306/D from the Motorola Literature Distribution Center.

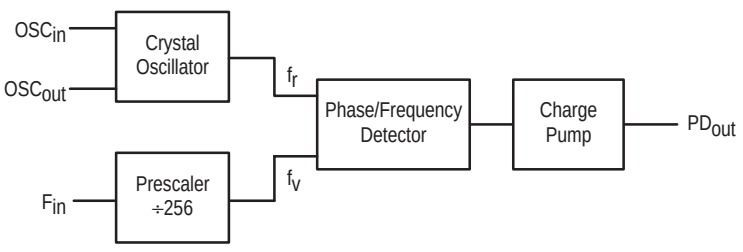
MOSAIC V, Mfax and *InterActiveApNote* are trademarks of Motorola, Inc.

MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 6.0	Vdc
Power Supply Voltage, Pin 7	V_P	V_{CC} to 6.0	Vdc
Storage Temperature Range	Tstg	–65 to 150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions as identified in the Electrical Characteristics table.
2. ESD data available upon request.

Block Diagram



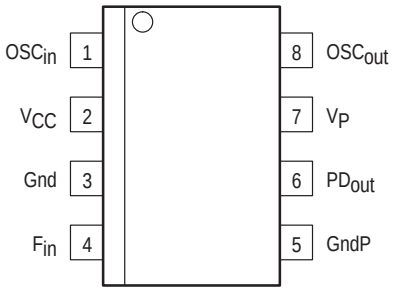
500 – 2800 MHz SINGLE CHANNEL FREQUENCY SYNTHESIZER

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12179D	T_A = –40° to +85°C	SO–8

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; V_P = V_{CC} to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

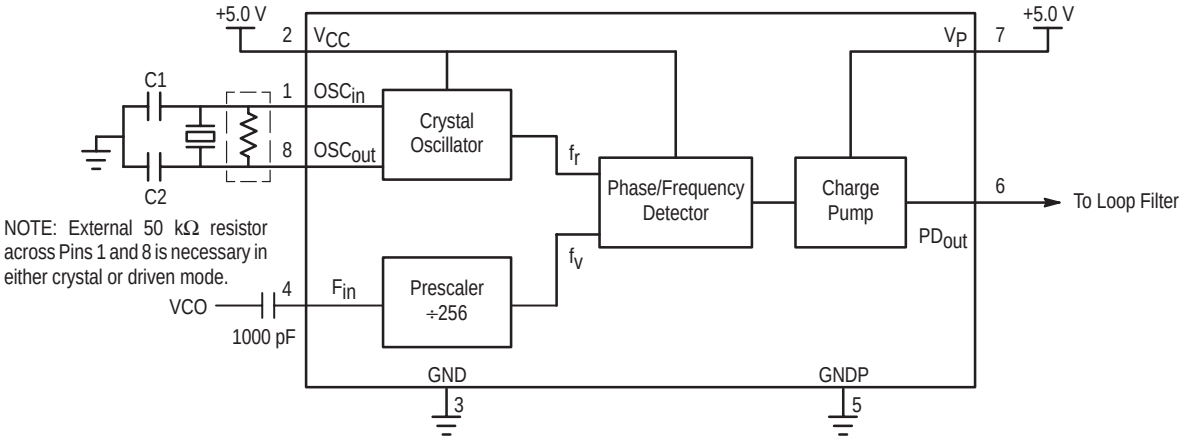
Characteristic	Symbol	Min	Typ	Max	Unit	Condition
Supply Current for V_{CC}	I_{CC}	–	3.1	5.6	mA	Note 1
Supply Current for V_P	I_P	–	0.4	1.3	mA	Note 1
Operating Frequency $f_{IN}max$ $f_{IN}min$	F_{IN}	2800 –	– –	– 500	MHz	Note 2
Operating Frequency Crystal Mode External Oscillator OSC_{in}	F_{OSC}	5 2	– –	11 11	MHz	Note 3 Note 4
Input Sensitivity F_{in}	V_{IN}	200	–	1000	$mV_{P–P}$	Note 2
Input Sensitivity External Oscillator OSC_{in}	V_{OSC}	500	–	2200	$mV_{P–P}$	Note 4
Output Source Current[5] (PD_{out})	I_{OH}	–2.8	–2.2	–1.6	mA	V_P = 4.5 V, V_{PDout} = V_P/2
Output Sink Current[5] (PD_{out})	I_{OL}	1.6	2.2	2.8	mA	V_P = 4.5 V, V_{PDout} = V_P/2
Output Leakage Current (PD_{out})	I_{OZ}	–	0.5	15	nA	V_P = 5.0 V, V_{PDout} = V_P/2

NOTES: 1. V_{CC} and V_P = 5.5 V; F_{IN} = 2.56 GHz; F_{OSC} = 10 MHz crystal; PD_{out} open.
2. AC coupling, F_{IN} measured with a 1000 pF capacitor.
3. Assumes C_1 and C_2 (Figure 1) limited to ≤30 pF each including stray and parasitic capacitances.
4. AC coupling to OSC_{in}.
5. Refer to Figure 15 and Figure 16 for typical performance curves over temperature and power supply voltage.

PIN FUNCTION DESCRIPTION

Pin	Symbol	I/O	Function
1	OSCin	I	Oscillator Input — An external parallel–resonant, fundamental crystal is connected between OSC_{in} and OSC_{out} to form an internal reference oscillator (crystal mode). External capacitors C1 and C2, as shown in Figure 1, are required to set the proper crystal load capacitance and oscillator frequency. For an external reference oscillator, an external signal is AC–coupled to the OSC_{in} pin with a 1000 pF coupling capacitor, with no connection to OSC_{out}. In either mode, a resistor with a nominal value of 50 kΩ MUST be placed across the OSC_{in} and OSC_{out} pins for proper operation.
2	V_{CC}	—	Positive Power Supply. Bypass capacitors should be placed as close as possible to the pin and be connected directly to the ground plane.
3	Gnd	—	Ground.
4	F_{in}	I	Prescaler Input — The VCO signal is AC coupled into the F_{in} pin.
5	GndP	—	Ground — For charge pump circuitry.
6	PD_{out}	O	Single ended phase/frequency detector output (charge pump output). Three–state current sink/source output for use as a loop error signal when combined with an external low pass filter. The phase/frequency detector is characterized by a linear transfer function.
7	V_P	—	Positive power supply for charge pump. V_P MUST be equal or greater than V_{CC}. Bypass capacitors should be placed as close as possible to the pin and be connected directly to the ground plane.
8	OSCout	O	Oscillator output, for use with an external crystal as shown in Figure 1.

Figure 1. MC12179 Expanded Block Diagram



PHASE CHARACTERISTICS

The phase comparator in the MC12179 is a high speed digital phase/frequency detector circuit. The circuit determines the "lead" or "lag" phase relationship and time difference between the leading edges of the VCO (f_V) signal and the reference (f_r) input. The detector can cover a range of $\pm 2\pi$ radian of f_V/f_r phase difference. The operation of the charge pump output is shown in Figure 2.

fr lags fv in phase OR fv>fr in frequency

When the phase of f_r lags that of fv or the frequency of f_V is greater than f_r, the Do output will sink current. The pulse width will be determined by the time difference between the two rising edges.

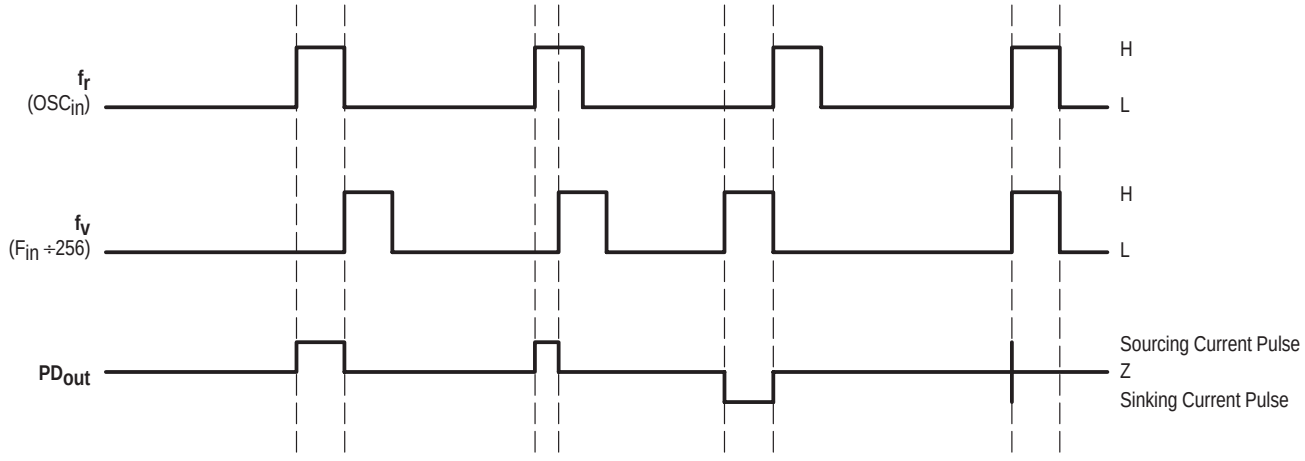
fr leads fv in phase OR fv<fr in frequency

When the phase of f_r leads that of fv or the frequency of f_V is less than f_r, the Do output will source current. The pulse width will be determined by the time difference between the two rising edges.

$f_r = f_V$ in phase and frequency

When the phase and frequency of fr and fv are equal, the charge pump will be in a quiet state, except for current spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

Figure 2. Phase/Frequency Detector and Charge Pump Waveforms



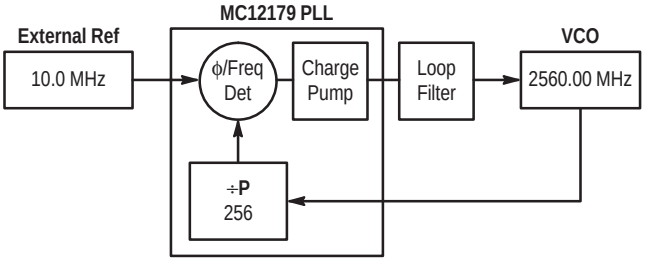
H = High voltage level; L = Low voltage level; Z = High impedance
NOTES: Phase difference detection range: ~ -2π to 2π

$$K_p\text{–Charge Pump Gain} \approx \frac{|I_{source}| + |I_{sink}|}{4\pi} = \frac{|2.2| + |-2.2|}{4\pi} = \frac{1.1\ \text{mA}}{\pi\text{radian}}$$

APPLICATIONS INFORMATION

The MC12179 is intended for applications where a fixed local oscillator is required to be synthesized. The prescaler on the MC12179 operates up to 2.8GHz which makes the part ideal for many satellite receiver applications as well as applications in the 2nd ISM (Industrial, Scientific, and Medical) band which covers the frequency range of 2400MHz to 2483MHz. The part is also intended for MMDS (Multi–channel Multi–point Distribution System) block downconverter applications. Below is a typical block diagram of the complete PLL.

Figure 3. Typical Block Diagram of Complete PLL



As can be seen from the block diagram, with the addition of a VCO, a loop filter, and either an external oscillator or crystal, a complete PLL sub–system can be realized. Since most of the PLL function is integrated into the MC12179, the user's primary focus is on the loop filter design and the crystal reference circuit. Figure 13 and Figure 14 illustrate typical VCO spectrum and phase noise characteristics. Figure 17 and Figure 18 illustrate the typical input impedance versus frequency for the prescaler input.

Crystal Oscillator Design

The MC12179 is used as a multiply–by–256 PLL circuit which transfers the high stability characteristic of a low frequency reference source to the high frequency VCO in the PLL loop. To facilitate this, the device contains an input circuit which can be configured as a crystal oscillator or a buffer for accepting an external signal source.

In the external reference mode, the reference source is AC–coupled into the OSC_{in} input pin. The input level signal should be between 500–2200 mVpp. When configured with an external reference, the device can operate with input frequencies down to 2MHz, thus allowing the circuit to control the VCO down to 512 MHz. To optimize the phase noise of the PLL when used in this mode, the input signal amplitude should be closer to the upper specification limit. This maximizes the slew rate of the input signal as it switches against the internal voltage reference.

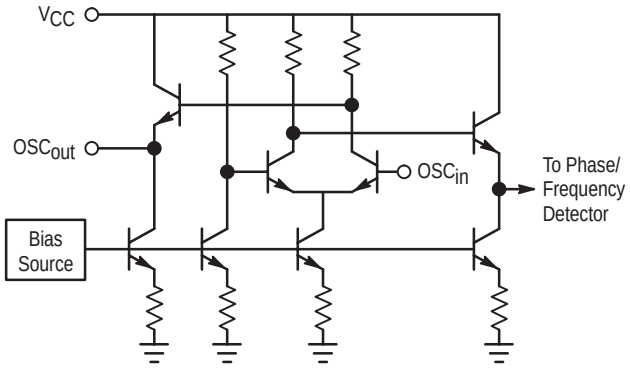
In the crystal mode, an external parallel–resonant fundamental mode crystal is connected between the OSC_{in} and OSC_{out} pins. This crystal must be between 5.0 MHz and 11 MHz. External capacitors, C1 and C2 as shown in Figure 1, are required to set the proper crystal load capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal chosen and the input capacitance of the device and any stray board capacitance.

In either mode, a 50kΩ resistor must be connected between the OSC_{in} and the OSC_{out} pins for proper device operation. The value of this resistor is not critical so a 47kΩ or 51kΩ ±10% resistor is acceptable.

Since the MC12179 is realized with an all–bipolar ECL style design, the internal oscillator circuitry is different from more traditional CMOS oscillator designs which realize the crystal oscillator with a modified inverter topology. These CMOS designs typically excite the crystal with a rail–to–rail signal which may overdrive the crystal resulting in damage or unstable operation. The MC12179 design does not exhibit these phenomena because the swing out of the OSC_{out} pin is less than 600mV. This has the added advantage of minimizing EMI and switching noise which can be generated by rail–to–rail CMOS outputs. The OSC_{out} output should not be used to drive other circuitry.

The oscillator buffer in the MC12179 is a single stage, high speed, differential input/output amplifier; it may be considered to be a form of the Pierce oscillator. A simplified circuit diagram is seen in Figure 4.

Figure 4. Simplified Crystal Oscillator/Buffer Circuit



OSC_{in} drives the base of one input of an NPN transistor differential pair. The non–inverting input of the differential pair is internally biased. OSC_{out} is the inverted input signal and is buffered by an emitter follower with a 70 μA pull–down current and has a voltage swing of about 600 mVpp. Open loop output impedance is about 425Ω. The opposite side of the differential amplifier output is used internally to drive another buffer stage which drives the phase/frequency detector. With the 50 kΩ feedback resistor in place, OSC_{in} and OSC_{out} are biased to approximately 1.1V below V_{CC}. The amplifier has a voltage gain of about 15 dB and a bandwidth in excess of 150 MHz. Adherence to good RF design and layout techniques, including power supply pin decoupling, is strongly recommended.

A typical crystal oscillator application is shown in Figure 1. The crystal and the feedback resistor are connected directly between OSC_{in} and OSC_{out}, while the loading capacitors, C1 and C2, are connected between OSC_{in} and ground, and OSC_{out} and ground respectively. It is important to understand that as far as the crystal is concerned, the two loading capacitors are in series (albeit through ground). So when the crystal specification defines a specific loading capacitance, this refers to the total external (to the crystal) capacitance seen across its two pins.

This capacitance consists of the capacitance contributed by the amplifier (IC and packaging), layout capacitance, and the series combination of the two loading capacitors. This is illustrated in the equation below:

$$C_I = C_{AMP} + C_{STRAY} + \frac{C1 \times C2}{C1 + C2}$$

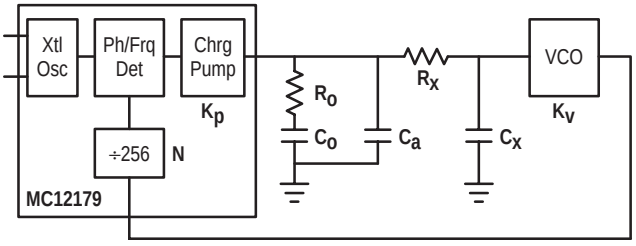
Provided the crystal and associated components are located immediately next to the IC, thus minimizing the stray capacitance, the combined value of C_{AMP} and C_{STRAY} is approximately 5pF. Note that the location of the OSC_{in} and OSC_{out} pins at the end of the package, facilitates placing the crystal, resistor and the C1 and C2 capacitors very close to the device. Usually, one of the capacitors is in parallel with an adjustable capacitor used to trim the frequency of oscillation. It is important that the total external (to the IC) capacitance seen by either OSC_{in} or OSC_{out}, be no greater than 30pF.

In operation, the crystal oscillator will start up with the application of power. If the crystal is in a can that is not grounded it is often possible to monitor the frequency of oscillation by connecting an oscilloscope probe to the can; this technique minimizes any disturbance to the circuit. If a malfunction is indicated, a high impedance, low capacitance, FET probe may be connected to either OSC_{in} or OSC_{out}. Signals typically seen at those points will be very nearly sinusoidal with amplitudes of roughly 300 to 600 mVpp. Some distortion is inevitable and has little bearing on the accuracy of the signal going to the phase detector.

Loop Filter Design

Because the device is designed for a non–frequency agile synthesizer (i.e., how fast it tunes is not critical) the loop filter design is very straight forward. The current output of the charge pump allows the loop filter to be realized without the need of any active components. The preferred topology for the filter is illustrated below in Figure 5.

Figure 5. Loop Filter



The R_O/C_O components realize the primary loop filter. C_a is added to the loop filter to provide for reference sideband suppression. If additional suppression is needed, the R_X/C_X realizes an additional filter. In most applications, this will not be necessary. If all components are used, this results in a 4th order PLL, which makes analysis difficult. To simplify this, the loop design will be treated as a 2nd order loop (R_O/C_O) and additional guidelines are provided to minimize the influence of the other components. If more rigorous analysis is needed, mathematical/system simulation tools can be used.

Component	Guideline
C_a	$<0.1 \times C_O$
R_X	$>10 \times R_O$
C_X	$<0.1 \times C_O$

The focus of the design effort is to determine what the loop's natural frequency, ω_O, should be. This is determined by R_O, C_O, K_p, K_V, and N. Because K_p, K_V, and N are given, it is only necessary to calculate values for R_O and C_O. There are 3 considerations in selecting the loop bandwidth:

1) Maximum loop bandwidth for minimum tuning speed
2) Optimum loop bandwidth for best phase noise performance
3) Minimum loop bandwidth for greatest reference sideband suppression

Usually a compromise is struck between these 3 cases, however, for the fixed frequency application, minimizing the tuning speed is not a critical parameter.

To specify the loop bandwidth for optimal phase noise performance, an understanding of the sources of phase noise in the system and the effect of the loop filter on them is required. There are 3 major sources of phase noise in the phase–locked loop – the crystal reference, the VCO, and the loop contribution. The loop filter acts as a low–pass filter to the crystal reference and the loop contribution equal to the total divide–by–N ratio. This is mathematically described in Figure 10. The loop filter acts as a high–pass filter to the VCO with an in–band gain equal to unity. This is described in Figure 11. The loop contribution includes the PLL IC, as well as noise in the system; supply noise, switching noise, etc. For this example, a loop contribution of 15 dB has been selected, which corresponds to data in Figure 14.

The crystal reference and the VCO are characterized as high–order 1/f noise sources. Graphical analysis is used to determine the optimum loop bandwidth. It is necessary to have noise plots from the manufacturer. This method provides a straightforward approximation suitable for quickly estimating the optimal bandwidth. The loop contribution is characterized as white–noise or low–order 1/f noise given in the form of a noise factor which combines all the noise effects into a single value. The phase noise of the Crystal Reference is increased by the noise factor of the PLL IC and related circuitry. It is further increased by the total divide–by–N ratio of the loop. This is illustrated in Figure 6.

The point at which the VCO phase noise crosses the amplified phase noise of the Crystal Reference is the point of the optimum loop bandwidth. In the example of Figure 6, the optimum bandwidth is approximately 15 KHz.

Figure 6. Graphical Analysis of Optimum Bandwidth

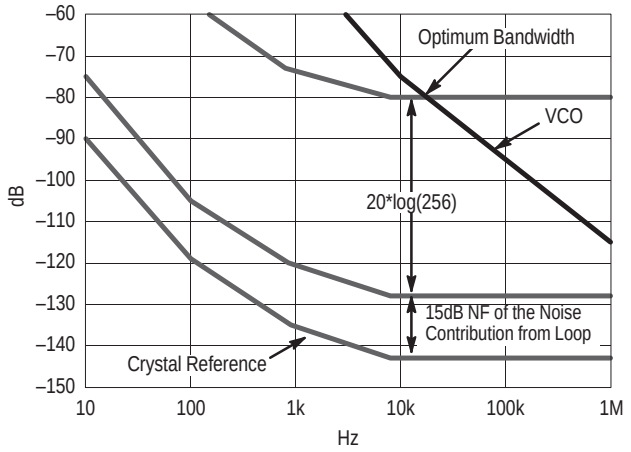
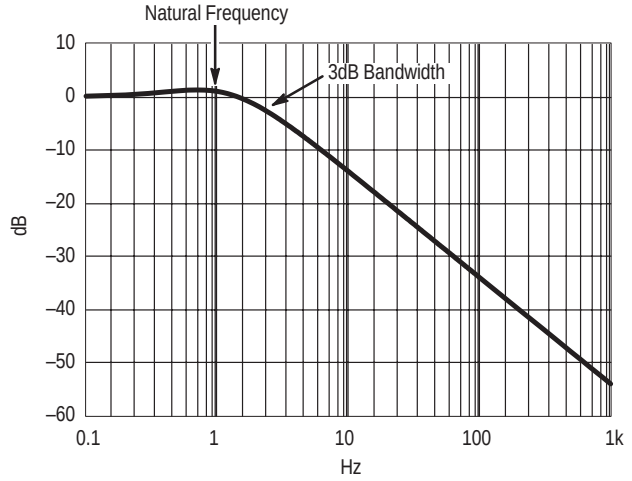


Figure 7. Closed Loop Frequency Response for ζ = 1



To simplify analysis further a damping factor of 1 will be selected. The normalized closed loop response is illustrated in Figure 7 where the loop bandwidth is 2.5 times the loop natural frequency (the loop natural frequency is the frequency at which the loop would oscillate if it were unstable). Therefore the optimum loop bandwidth is 15kHz/2.5 or 6kHz (37.7krads) with a damping coefficient, $\zeta \approx 1$. T(s) is the transfer function of the loop filter.

Figure 8. Design Equations for the 2nd Order System

$$T(s) = \frac{R_oC_os + 1}{\left(\frac{NC_o}{K_pK_v}\right)s^2 + R_oC_os + 1} = \frac{\left(\frac{2\zeta}{\omega_o}\right)s + 1}{\left(\frac{1}{\omega_o{}^2}\right)s^2 + \left(\frac{2\zeta}{\omega_o}\right)s + 1}$$

$$\left(\frac{NC_o}{K_pK_v}\right) = \left(\frac{1}{\omega_o{}^2}\right) \rightarrow \omega_o = \sqrt{\frac{K_pK_v}{NC_o}} \rightarrow \boxed{C_o \approx \left(\frac{K_pK_v}{N\omega_o{}^2}\right)}$$

$$R_oC_o = \left(\frac{2\zeta}{\omega_o}\right) \rightarrow \zeta = \left(\frac{\omega_oR_oC_o}{2}\right) \rightarrow \boxed{R_o = \left(\frac{2\zeta}{\omega_oC_o}\right)}$$

In summary, follow the steps given below:

Step 1: Plot the phase noise of crystal reference and the VCO on the same graph.

Step 2: Increase the phase noise of the crystal reference by the noise contribution of the loop.

Step 3: Convert the divide–by–N to dB (20log 256 – 48 dB) and increase the phase noise of the crystal reference by that amount.

Step 4: The point at which the VCO phase noise crosses the amplified phase noise of the Crystal Reference is the point of the optimum loop bandwidth. This is approximately 15 kHz in Figure 6.

Step 5: Correlate this loop bandwidth to the loop natural frequency and select components per Figure 8. In this case the 3.0 dB bandwidth for a damping coefficient of 1 is 2.5 times the loop's natural frequency. The relationship between the 3.0 dB loop bandwidth and the loop's "natural" frequency will vary for different values of ζ. Making use of the equations defined above in a math tool or spread sheet is useful. To aid in the use of such a tool the equations are summarized in Figures 9 through 11.

Figure 9. Loop Parameter Relations

Let: $\frac{NC_o}{K_pK_v} = \frac{1}{\omega_o{}^2}$, $R_oC_o = \frac{2\zeta}{\omega_o}$

Let: $C_a = aC_o$, $C_x = bC_o$, $A = 1 + a$, and $B = 1 + a + b$

Let: $R_oC_o = \frac{1}{\omega_3}$, $R_xC_x = \frac{1}{\omega_4}$, $R_o(C_a + C_x) = \frac{1}{\omega_5}$

Let: $K_3\omega_3 = \omega_o$, $K_4\omega_4 = \omega_o$, $K_5\omega_5 = \omega_o$

Figure 10. Transfer Function for the Crystal Noise in the Frequency Plane

$$T(j\omega) = N \cdot \frac{1 + j\left(2\zeta\frac{\omega}{\omega_o}\right)}{\left(1 + K_3K_4\frac{\omega^4}{\omega_o{}^4} - B\frac{\omega^2}{\omega_o{}^2}\right) + j\left(2\zeta\frac{\omega}{\omega_o} - (AK_4 + K_5)\frac{\omega^3}{\omega_o{}^3}\right)}$$

Figure 11. Transfer Function for the VCO Noise in the Frequency Plane

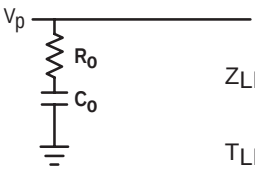
$$T(j\omega) = \frac{\left(K_3K_4\frac{\omega^4}{\omega_o{}^4} - B\frac{\omega^2}{\omega_o{}^2}\right) - j\left((AK_4 + K_5)\frac{\omega^3}{\omega_o{}^3}\right)}{\left(1 + K_3K_4\frac{\omega^4}{\omega_o{}^4} - B\frac{\omega^2}{\omega_o{}^2}\right) + j\left(2\zeta\frac{\omega}{\omega_o} - (AK_4 + K_5)\frac{\omega^3}{\omega_o{}^3}\right)}$$

Appendix: Derivation of Loop Filter Transfer Function

The purpose of the loop filter is to convert the current from the phase detector to a tuning voltage for the VCO. The total transfer function is derived in two steps. Step 1 is to find the voltage generated by the impedance of the loop filter. Step 2 is to find the transfer function from the input of the loop filter to its output. The “voltage” times the “transfer function” is the overall transfer function of the loop filter. To use these equations in determining the overall transfer function of a PLL multiply the filter’s impedance by the gain constant of the phase detector then multiply that by the filter’s transfer function (which is unity in the 2nd and 3rd order cases below).

Figure 12. Overall Transfer Function of the PLL

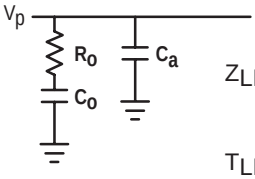
For the 2nd Order PLL:



$$Z_{LF}(s) = \frac{R_oC_os + 1}{C_os}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1\ ,\ V_p(s) = K_p(s)Z_{LF}(s)$$

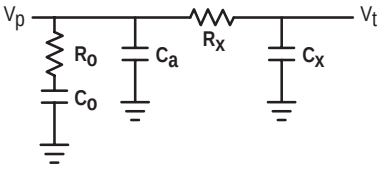
For the 3rd Order PLL:



$$Z_{LF}(s) = \frac{R_oC_os + 1}{C_oR_oC_as^2 + (C_o + C_a)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1\ ,\ V_p(s) = K_p(s)Z_{LF}(s)$$

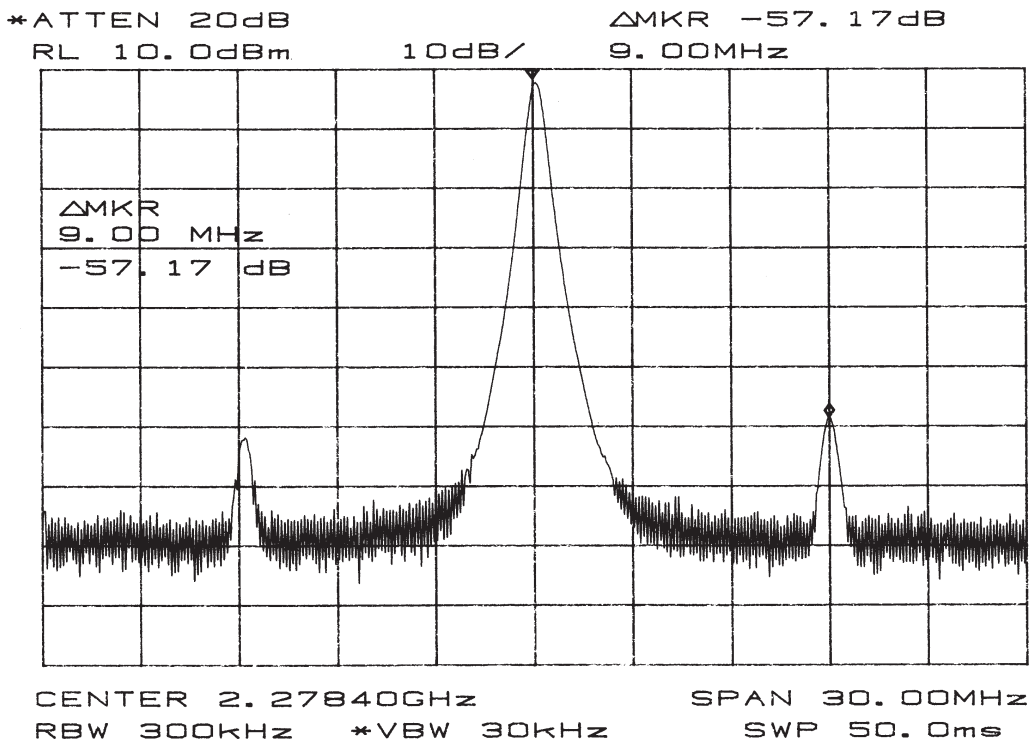
For the 4th Order PLL:



$$Z_{LF}(s) = \frac{(R_oC_os + 1)\ (R_xC_xs + 1)}{C_oR_oC_aR_xC_xs^3 + [\ (C_o + C_a)R_xC_x + C_oR_o(C_x + C_a)\ ]\ s^2 + (C_o + C_a + C_x)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = \frac{1}{(R_xC_xs + 1)}\ ,\ V_p(s) = K_p(s)Z_{LF}(s)$$

Figure 13. VCO Output Spectrum with MC12179, V_{CC} = 5.0 V
(ECLiPTEK 8.9 MHz Crystal and ZCOM 2500 VCO)



NOTE: Spurs can be reduced further by narrowing the loop bandwidth of the PLL loop filter and/or adding an extra filter (R_X/C_X)

Figure 14. Typical Phase Noise Plot, 2200 MHz VCO
(With the MC12179 in a Closed Loop)

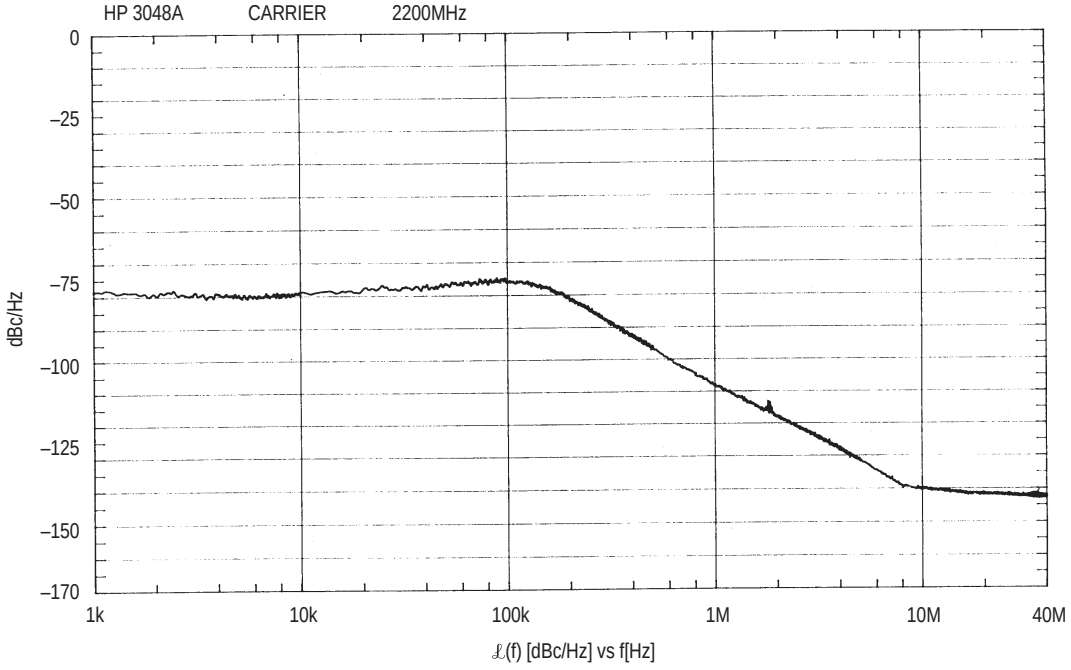


Figure 15. Typical Charge Pump Current versus Temperature
(V_{CC} = V_{pp} = 5.0 V)

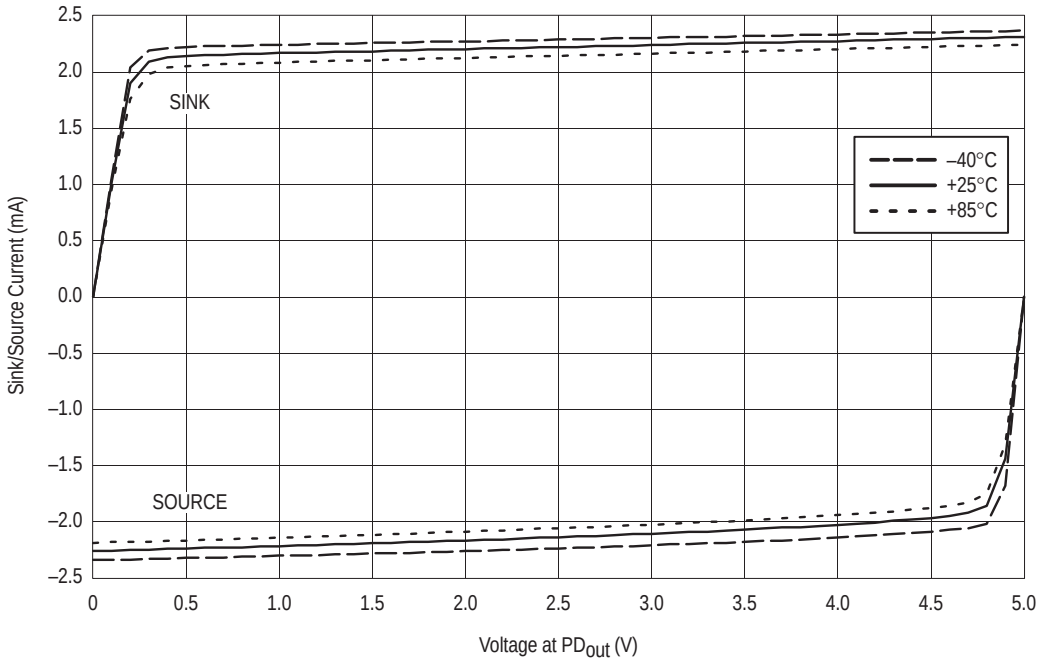


Figure 16. Typical Charge Pump Current versus Voltage
(T = 25°C)

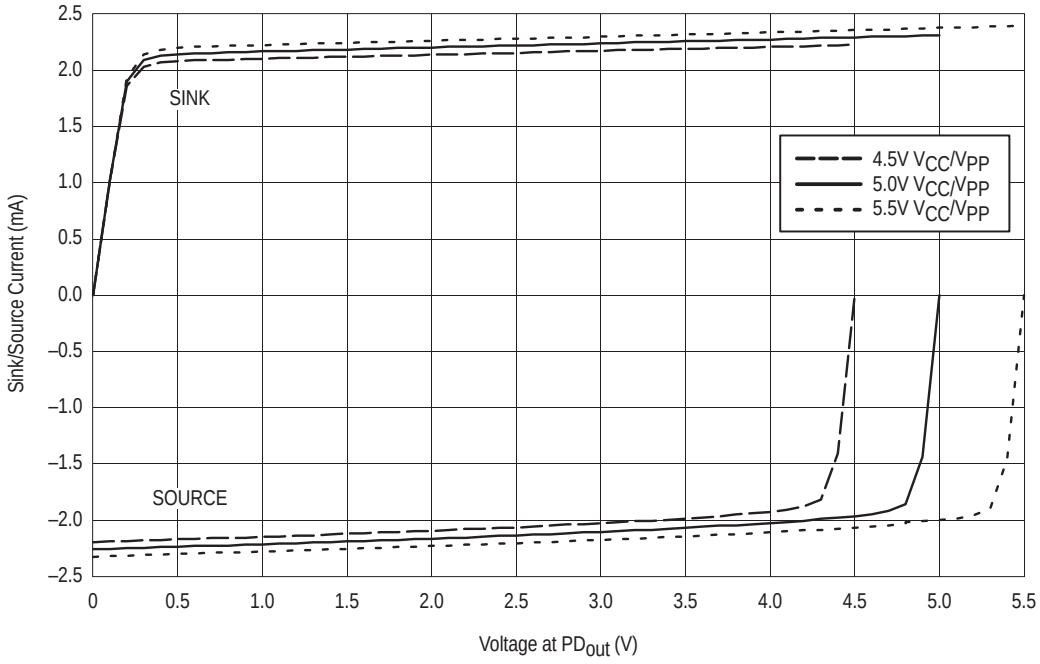


Figure 17. Typical Real Input Impedance versus Input Frequency
(For the F_{in} Input)

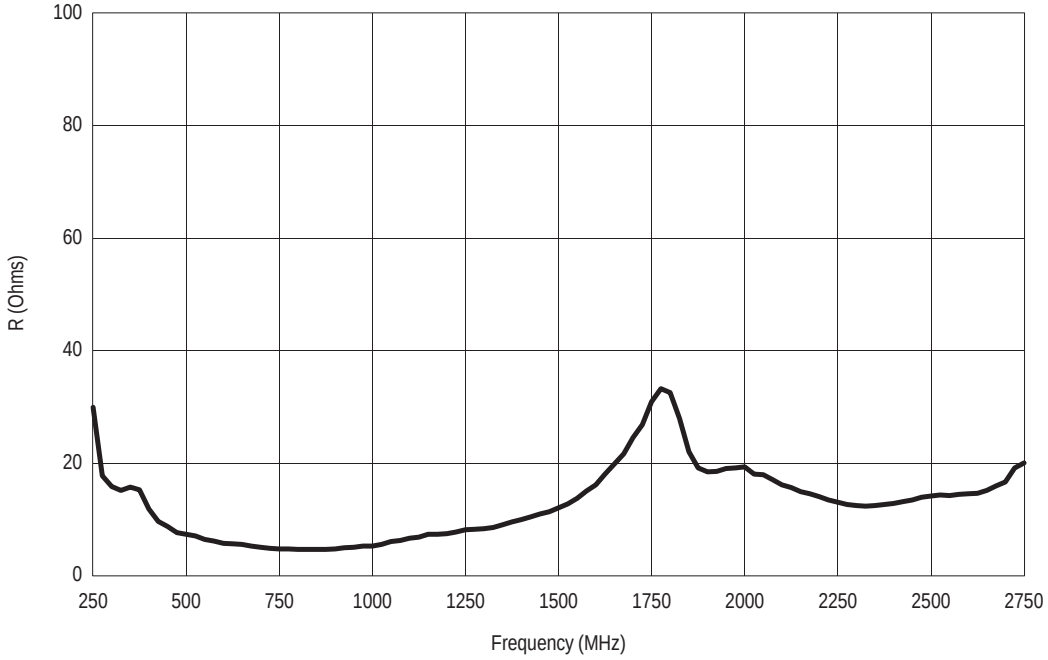
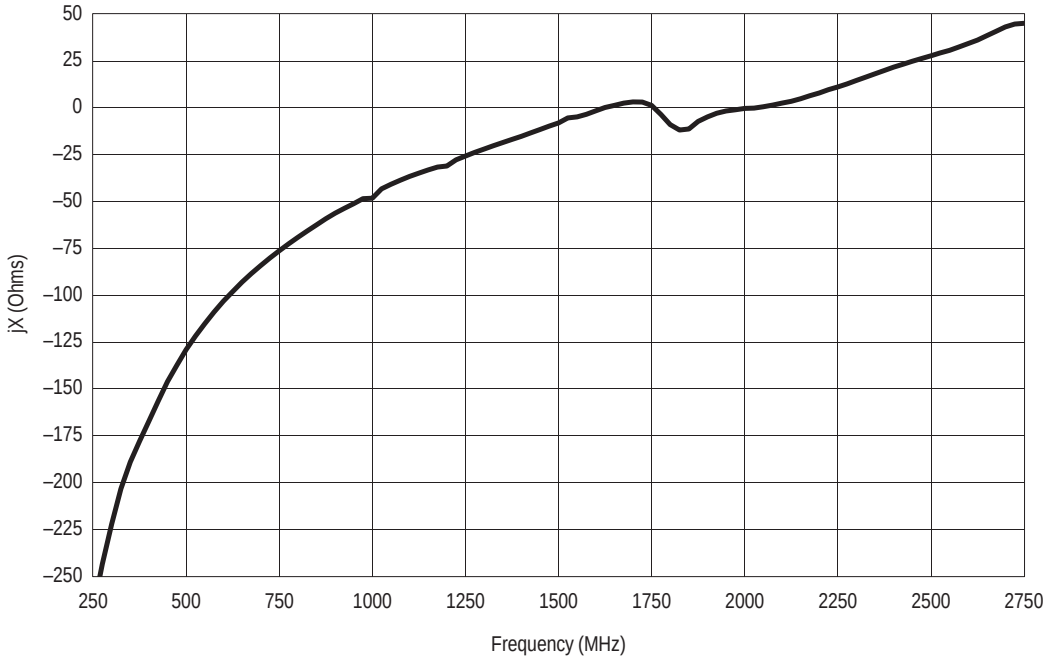


Figure 18. Typical Imaginary Input Impedance versus Input Frequency
(For the F_{in} Input)



MOTOROLA

MC12181

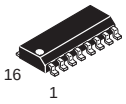
125-1000 MHz Frequency Synthesizer

125 – 1000 MHZ FREQUENCY SYNTHESIZER

SEMICONDUCTOR TECHNICAL DATA

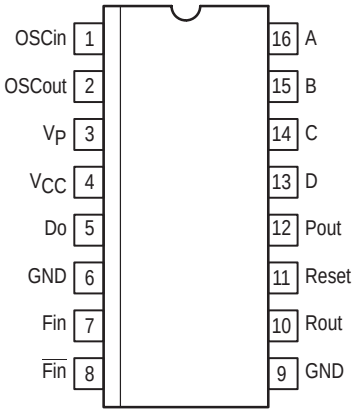
The MC12181 is a monolithic bipolar synthesizer integrating a high performance prescaler, programmable divider, phase/frequency detector, charge pump, and reference oscillator/buffer functions. The device is capable of synthesizing a signal which is 25 to 40 times the input reference signal. The device has a 4–bit parallel interface to set the proper total multiplication which can range from 25 to 40. When combined with an external passive loop filter and VCO, the MC12181 serves as a complete PLL subsystem.

- 2.7 to 5.5 V Operation
- Low power supply current of 4.25 mA typical
- On chip reference oscillator/buffer supporting wide frequency operating range from 5 to 25 MHz
- 4–bit parallel interface for programming divider (N = 25 .... 40)
- Wide 125 – 1000 MHz frequency of operation
- Digital phase/frequency detector with linear transfer function
- Balanced Charge Pump Output
- Space efficient 16 lead SOIC package
- Operating Temperature Range of –40 to 85°C
- > 1000 V ESD Protection (I/O to Ground, I/O to V_{CC})



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS



(Top View)

The device is suitable for applications where a fixed local oscillator (LO) needs to be synthesized or where a limited number of LO frequencies need to be generated. The device also has auxiliary open emitter outputs (Pout and Rout) for observing the inputs to the phase detector for verification purposes. In normal use the pins should be left open. The Reset input is normally LOW. When this input is placed in the HIGH state the reference prescaler is reset and the charge pump output (Do) is placed in the OFF state.

The 4–bit programming interface maps into divider states ranging from 25 to 40. A is the LSB and D is the MSB. The data inputs (A,B,C, and D) are CMOS compatible and have pull–up resistors. The inputs can be tied directly to Vcc or Ground for programming or can be interfaced to an external data latch/register. Table 1 below has a mapping of the programming states.

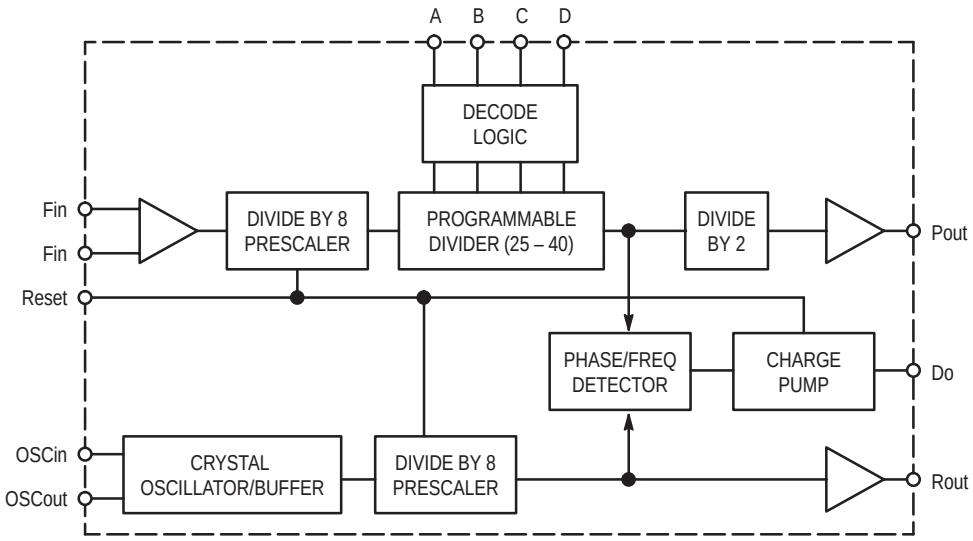
Table 1. Programming States

D	C	B	A	Divider
L	L	L	L	25
L	L	L	H	26
L	L	H	L	27
L	L	H	H	28
L	H	L	L	29
L	H	L	H	30
L	H	H	L	31
L	H	H	H	32
H	L	L	L	33
H	L	L	H	34
H	L	H	L	35
H	L	H	H	36
H	H	L	L	37
H	H	L	H	38
H	H	H	L	39
H	H	H	H	40

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12181D	T_A = –40° to +85°C	SO–16

Figure 1. MC12181 Programmable Synthesizer



PIN NAMES

Pin No.	Pin	Function
1	OSCin	An external parallel resonant, fundamental crystal is connected between OSCin and OSCout to form an internal reference crystal oscillator. External capacitors C1 and C2 are required to set the proper crystal load capacitance and oscillator frequency (Figure 2). For an external reference oscillator, a signal is ac–coupled into the OSCin pin. In either mode a 50 kΩ resistor MUST be connected between OSCin and OSCout.
2	OSCout	Oscillator output, for use with an external crystal as shown in Figure 2.
3	V_P	Positive power supply for charge pump. V_P MUST be greater than or equal to V_{CC}. Bypassing should be placed as close as possible to this pin and be connected directly to the ground plane.
4	V_{CC}	Positive power supply. Bypassing should be placed as close as possible to this pin and be connected directly to the ground plane.
5	Do	Single ended phase/frequency detector output. Three–state current sink/source output for use as a loop error signal when combined with an external low pass filter. The phase/frequency detector is characterized by a linear transfer function.
6	GND	Ground. This pin should be directly tied to the ground plane.
7	Fin	Prescaler input – The VCO signal is ac–coupled into the Fin Pin.
8	Fin	Complementary prescaler input – This pin should be capacitively coupled to ground.
9	GND	Ground. This pin should be directly tied to the ground plane.
10	Rout	Open emitter test point used to verify proper operation of the reference divider chain. In normal operation this pin should be left OPEN.
11	Reset	Test pin used to clear the prescalers (Reset = H). When the Reset is in the HIGH state, the charge pump output is disabled. The Reset input has an internal pulldown. In normal operation it can be left open or tied to ground.
12	Pout	Open emitter test point used to verify proper operation of the programmable divider chain. The output is a divide–by–2 version of the programmable input to the phase/frequency detector. In normal operation this pin should be left OPEN.
13 14 15 16	D C B A	Digital control inputs for setting the value of the programmable divider. A is the LSB and D is the MSB. In normal operation these pins can be tied to V_{CC} and/or ground to program a fixed divide or they can be driven by a CMOS logic level when used in a programmable mode. There is an internal pull–up resistor to V_{CC} on each input.

Figure 2. Typical Applications Example

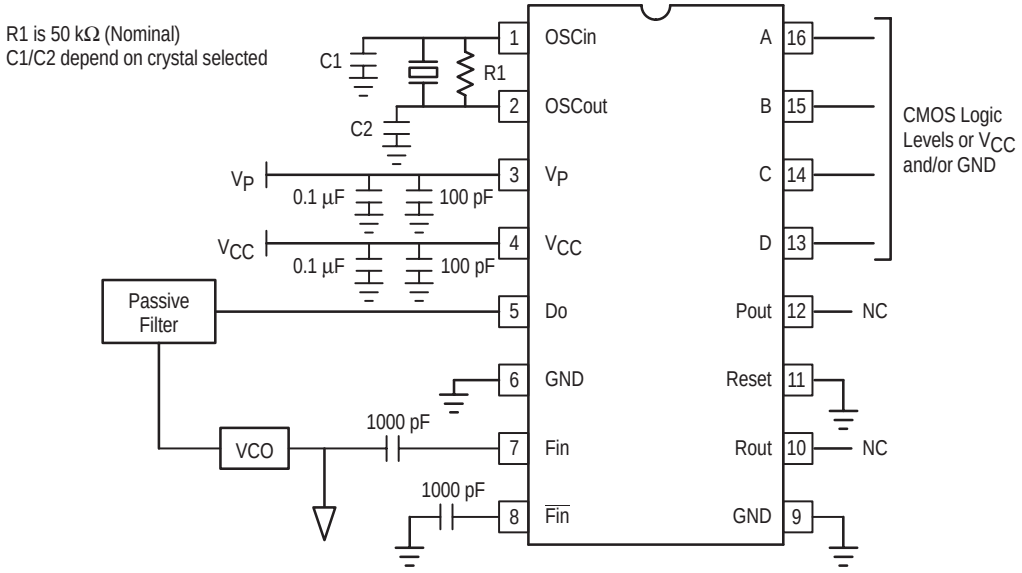
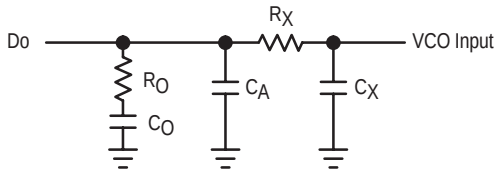


Figure 3. Typical Passive Loop Filter Topology



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Range	V_{CC}	2.7	5.5	VDC
Maximum Supply Range	V_{CC}max	–	–6.0	VDC
Maximum Charge Pump Voltage	$V_P$max	–	V_{CC} to +6.0	VDC
Temperature Ambient	T_A	–40	85	°C
Storage Temperature	T_{STG}	–65	150	°C
Maximum Input Signal (Any Pin)	V_{in}max	–	V_{CC}+0.5 V	VDC

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; V_P = V_{CC} to 6.0 V; T_A = –40 to +85°C, unless otherwise noted.)

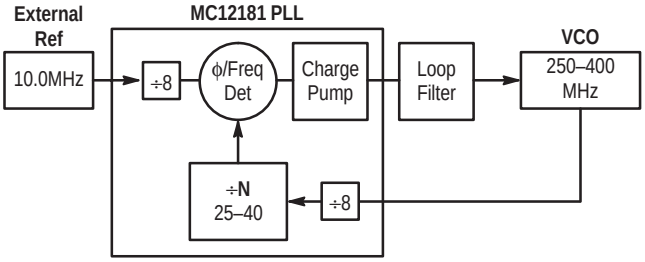
Characteristic	Symbol	Min	Typ	Max	Unit	Condition
Supply Current for V_{CC}	I_{CC}	–	4.0	5.5	mA	Note 1
Supply Current for V_P	I_P	–	0.25	0.5	mA	Note 1
Input Frequency Range	OSCin	5	–	25	MHz	Note 2
RF Input Frequency Range	Fin	125	–	1000	MHz	Note 3
Fin Input Sensitivity	Vin	100	–	1000	mVpp	Note 4
OSCin Input Sensitivity	V_{OSC}	500	–	2200	mVpp	Note 4
Output Source Current (Do)	I_{OH}	–2.8	–2.2	–2.0	mA	Note 5
		–2.4	–2.0	–1.6		Note 6
Output Sink Current (Do)	I_{OL}	2.0	2.4	2.8	mA	Note 5
		1.6	2.0	2.4		Note 6
Output Leakage Current (Do)	I_{OZ}	–	0.5	10	nA	V_{CC}=5.5; V_P = 6.0 V; VDo=0.5 to 5.5 V
Charge Pump Operating Volt	VDo	0.5	–	V_P–0.5	V	
Input HIGH Voltage Reset, A, B, C, D	V_{IH}	0.7 V_{CC}	–	–	V	
Input LOW Voltage Reset, A, B, C, D	V_{IL}	–	–	0.3 V_{CC}	V	
Input HIGH Current A, B, C, D	I_{IH}	–	–	+1	µA	
Reset		–	–	+100		
Input LOW Current A, B, C, D	I_{IL}	–100	–	–	µA	
Reset		–1	–	+1		
Output Amplitude (Pout, Rout)	Vout	250	400	–	mVpp	Note 7

NOTES: 1. V_{CC} and V_P = 5.5 V; Fin = 1.0 GHz; OSCin = 25 MHz; Do open.
2. Assumes C_1 and C_2 (Figure 2) limited to ≤30 pF each including stray capacitance in crystal mode, ac coupled input for external reference mode.
3. AC coupling, Fin measured with a 1000pF capacitor.
4. Signal ac coupling in input.
5. V_{CC} = 5.5 V; V_P = 6.0 V; V_{DO} = 3.0 V.
6. V_P = V_{CC} = 3.0 V; V_{DO} = 1.5 V.
7. Minimum resistor value of 25 kΩ to ground.

APPLICATIONS INFORMATION

The MC12181 is intended for applications where a fixed LO, or a limited number of local oscillator frequencies is required to be synthesized. The device acts as a x25 – 40 PLL. The 4–bit parallel interface allows 1 of 16 divide ratios to be selected. Internally there are fixed divide by 8 prescalers in the reference and programmable paths of the PLL. The MC12181 operates from 125 MHz to 1000 MHz which makes the part ideal for FCC Title 47; Part 15 applications in the 260 MHz to 470 MHz band and the 902 to 928 MHz Band. Figure 4 shows a typical block diagram of the application.

Figure 4. Typical Block Diagram of Complete PLL



As can be seen from the block diagram, with the addition of a VCO, a loop filter, and either an external oscillator or crystal, a complete PLL sub–system can be realized. Since most of the PLL functions are integrated into the 12181, the users focus is on the loop filter design and the crystal reference oscillator circuit.

Crystal Oscillator Design

The PLL is used to transfer the high stability characteristic of a low frequency reference source to the high frequency VCO within the PLL loop. To facilitate this, the device contains an input circuit which can be configured as a crystal oscillator or a buffer for accepting an external signal source.

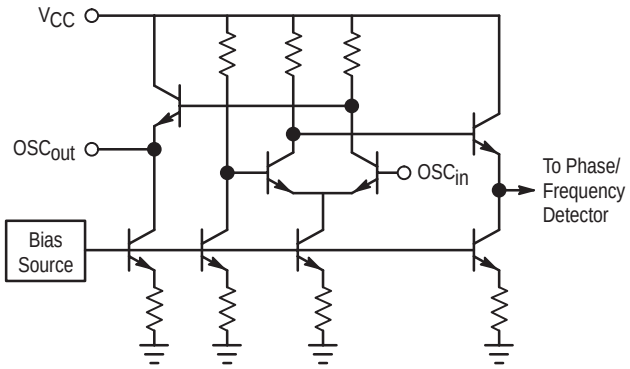
In the external reference mode, the reference source is ac–coupling into the OSCin input pin. The level of this signal should be between 500 – 2200 mVp–p. An external low noise reference should be used when it is desired to obtain the best close–in phase noise performance for the PLL. In addition the input reference amplitude should be close to the upper amplitude specification. This maximizes the slew rate of the input signal as it switches against the internal voltage reference.

In the crystal mode, an external parallel–resonant fundamental mode crystal should be connected between the OSCin and OSCout pins. This crystal must be between 5 and 25 MHz. External capacitors C1 and C2, as shown in Figure 2, are required to set the proper crystal load capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal choosen and the input capacitance of the device as well as stray board capacitance.

Since the MC12181 is realized with an all–bipolar ECL style design, the internal oscillator circuitry is different from more traditional CMOS oscillator designs which realize the crystal oscillator with a modified inverter topology. These CMOS designs typically excite the crystal with a rail–to–rail signal which may overdrive the crystal resulting in damage or unstable operation. The MC12181 design does not exhibit this phenomena because the swing out of the OSCout pin is less than 600 mVp–p. This has the added advantage of minimizing EMI and switching noise which can be generated by rail–to–rail CMOS outputs. The OSCout output should not be used to drive other circuitry.

The oscillator buffer in the MC12181 is a single stage, high speed, differential input/output amplifier; it may be considered to be a form of the Pierce oscillator. A simplified circuit diagram is seen in Figure 5.

Figure 5. Simplified Crystal Oscillator/Buffer Circuit



OSC_{in} drives the base of one input of an NPN transistor differential pair. The non–inverting input of the differential pair is internally biased. OSC_{out} is the inverted input signal and is buffered by an emitter follower with a 70 μA pull–down current and has a voltage swing of about 600mVp–p. Open loop output impedance is approximately 425 Ω. The opposite side of the differential amplifier output is used internally to drive another buffer stage which drives the phase/frequency detector. With the 50 kΩ feedback resistor in place, OSC_{in} and OSC_{out} are biased to approximately 1.1 V below V_{CC}. The amplifier has a voltage gain of about 15dB and a bandwidth in excess of 150 MHz. Adherence to good RF design and layout techniques, including power supply pin decoupling, is strongly recommended.

A typical crystal oscillator application is shown in Figure 2. The crystal and the feedback resistor are connected directly between OSC_{in} and OSC_{out}, while the loading capacitors, C1 and C2, are connected between OSC_{in} and ground, and OSC_{out} and ground respectively. It is important to understand that as far as the crystal is concerned, the two loading capacitors are in series (albeit through ground). So when the crystal specification defines a specific loading capacitance, this refers to the total external (to the crystal) capacitance seen across its two pins.

This capacitance consists of the capacitance contributed by the amplifier (IC and packaging), layout capacitance, and the series combination of the two loading capacitors. This is illustrated in the equation below:

$$C_I = C_{AMP} + C_{STRAY} + \frac{C1 \times C2}{C1 + C2}$$

Provided the crystal and associated components are located immediately next to the IC, thus minimizing the stray capacitance, the combined value of C_{AMP} and C_{STRAY} is approximately 5pF. Note that the location of the OSC_{in} and OSC_{out} pins at the end of the package, facilitates placing the crystal, resistor and the C1 and C2 capacitors very close to the device. Usually, one of the capacitors is in parallel with an adjustable capacitor used to trim the frequency of oscillation.

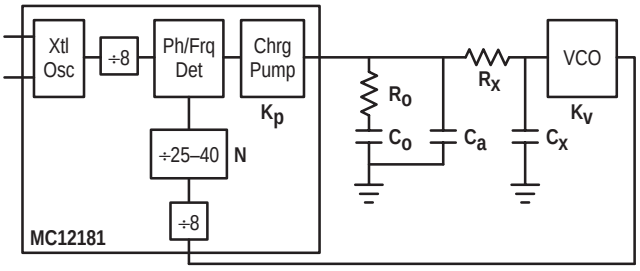
It is important that the total external (to the IC) capacitance seen by either OSC_{in} or OSC_{out}, be no greater than 30pF.

In operation, the crystal oscillator will start up with the application of power. If the crystal is in a can that is not grounded it is often possible to monitor the frequency of oscillation by connecting an oscilloscope probe to the can; this technique minimizes any disturbance to the circuit. If this is not possible, a high impedance, low capacitance, FET probe can be connected to either OSC_{in} or OSC_{out}. Signals typically seen at those points will be very nearly sinusoidal with amplitudes of roughly 300–600mVp–p. Some distortion is inevitable and has little bearing on the accuracy of the signal going to the phase detector.

Loop Filter Design

Because the device is designed for a non–frequency agile synthesizer (i.e., how fast it tunes is not critical) the loop filter design is very straight forward. The current output of the charge pump allows the loop filter to be realized without the need of any active components. The preferred topology for the filter is illustrated in Figure 6.

Figure 6. Loop Filter



The R_O/C_O components realize the primary loop filter. C_a is added to the loop filter to provide for reference sideband suppression. If additional suppression is needed, the R_X/C_X realizes an additional filter. In most applications, this will not be necessary. If all components are used, this results in a 4th order PLL, which makes analysis difficult. To simplify this, the loop design will be treated as a 2nd order loop (R_O/C_O) and additional guidelines are provided to minimize the influence of the other components. If more rigorous analysis is needed, mathematical/system simulation tools should be used.

Component	Guideline
C_a	$<0.1 \times C_O$
R_X	$>10 \times R_O$
C_X	$<0.1 \times C_O$

The focus of the design effort is to determine what the loop's natural frequency, ω_o, should be. This is determined by R_O, C_O, K_p, K_V, and N_t. Because K_p, K_V, and N_t are given, it is only necessary to calculate values for R_O and C_O. There are 3 considerations in selecting the loop bandwidth:

4) Maximum loop bandwidth for minimum tuning speed
5) Optimum loop bandwidth for best phase noise performance
6) Minimum loop bandwidth for greatest reference sideband suppression

Usually a compromise is struck between these 3 cases, however, for a fixed frequency application, minimizing the tuning speed is not a critical parameter.

To specify the loop bandwidth for optimal phase noise performance, an understanding of the sources of phase noise in the system and the effect of the loop filter on them is required. There are 3 major sources of phase noise in the phase–locked loop – the crystal reference, the VCO, and the loop contribution. The loop filter acts as a low–pass filter to the crystal reference and the loop contribution. The loop filter acts as a high–pass filter to the VCO with an in–band gain equal to unity. The loop contribution includes the PLL IC, as well as noise in the system; supply noise, switching noise, etc. For this example, a loop contribution of 15dB has been selected, which corresponds to data in Figure 17.

The crystal reference and the VCO are characterized as high–order 1/f noise sources. Graphical analysis is used to determine the optimum loop bandwidth. It is necessary to have noise plots from the manufacturers of both devices. This method provides a straightforward approximation suitable for quickly estimating the optimal bandwidth. The loop contribution is characterized as white–noise or low–order 1/f noise given in the form of a noise factor which combines all the noise effects into a single value. The phase noise of the Crystal Reference is increased by the noise factor of the PLL IC and related circuitry. It is further increased by the total divide–by–N ratio of the loop. This is illustrated in Figure 7.

The point at which the VCO phase noise crosses the amplified phase noise of the Crystal Reference is the point of the optimum loop bandwidth. In the example of Figure 7, the optimum bandwidth is approximately 15 KHz.

Figure 7. Graphical Analysis of Optimum Bandwidth

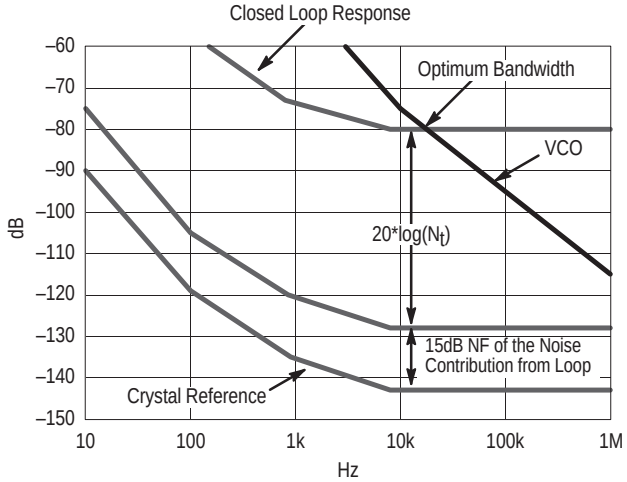
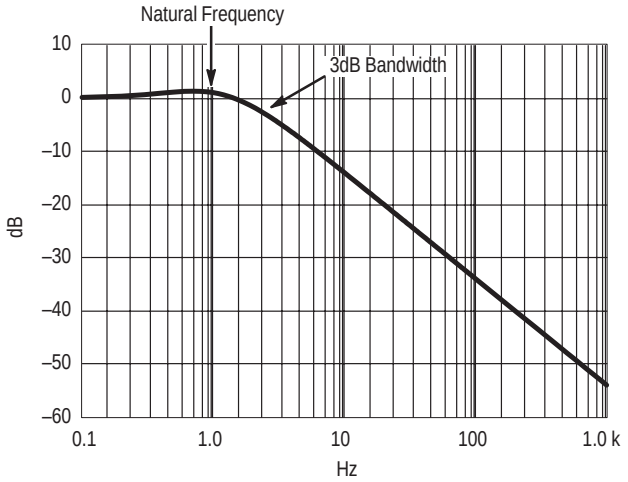


Figure 8. Closed Loop Frequency Response for ζ = 1



To simplify analysis further a damping factor of 1 will be selected. The normalized closed loop response is illustrated in Figure 8 where the loop bandwidth is 2.5 times the loop natural frequency (the loop natural frequency is the frequency at which the loop would oscillate if it were unstable). Therefore the optimum loop bandwidth is 15 kHz/2.5 or 6.0 kHz (37.7 krads) with a damping coefficient, $\zeta \approx 1$. T(s) is the transfer function of the loop filter.

$$T(s) = \frac{R_oC_os + 1}{\left(\frac{NC_o}{K_pK_v}\right)s^2 + R_oC_os + 1} = \frac{\left(\frac{2\zeta}{\omega_o}\right)s + 1}{\left(\frac{1}{\omega_o{}^2}\right)s^2 + \left(\frac{2\zeta}{\omega_o}\right)s + 1}$$

$$\left(\frac{NC_o}{K_pK_v}\right) = \left(\frac{1}{\omega_o{}^2}\right) \rightarrow \omega_o = \sqrt{\frac{K_pK_v}{NC_o}} \rightarrow \boxed{C_o = \left(\frac{K_pK_v}{N\omega_o{}^2}\right)}$$

$$R_oC_o = \left(\frac{2\zeta}{\omega_o}\right) \rightarrow \zeta = \left(\frac{\omega_oR_oC_o}{2}\right) \rightarrow \boxed{R_o = \left(\frac{2\zeta}{\omega_oC_o}\right)}$$

where N_t = Total PLL Divide Ratio — 8×N where (N = 25...40)
K_v = VCO Gain — Hz/V
K_p = Phase Detector/Charge Pump Gain — A
= ($|I_{OH}| + |I_{OL}|$) / 2

Technically, K_v and K_p should be expressed in Radian units [K_v (RAD/V), K_p (A/RAD)]. Since the component design equation contains the $K_v \times K_p$ term. the 2π cancels and the values can be epressed as above.

Figure 9. Design Equations for the 2nd Order System

In summary, follow the steps given below:

Step 1: Plot the phase noise of crystal reference and the VCO on the same graph.

Step 2: Increase the phase noise of the crystal reference by the noise contribution of the loop.

Step 3: Convert the divide–by–N to dB (20log 8 × N) and increase the phase noise of the crystal reference by that amount.

Step 4: The point at which the VCO phase noise crosses the amplified phase noise of the Crystal Reference is the point of the optimum loop bandwidth. This is approximately 15 kHz in Figure 7.

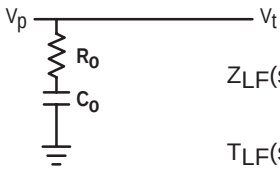
Step 5: Correlate this loop bandwidth to the loop natural frequency per Figure 8. In this case the 3.0 dB bandwidth for a damping coefficient of 1 is 2.5 times the loop's natural frequency. The relationship between the 3.0 dB loop bandwidth and the loop's "natural" frequency will vary for different values of ζ. Making use of the equations defined in Figure 9, a math tool or spread sheet is useful to select the values for R_o and C_o.

Appendix: Derivation of Loop Filter Transfer Function

The purpose of the loop filter is to convert the current from the phase detector to a tuning voltage for the VCO. The total transfer function is derived in two steps. Step 1 is to find the voltage generated by the impedance of the loop filter. Step 2 is to find the transfer function from the input of the loop filter to its output. The "voltage" times the "transfer function" is the overall transfer function of the loop filter. To use these equations in determining the overall transfer function of a PLL multiply the filter's impedance by the gain constant of the phase detector then multiply that by the filter's transfer function (Figure 10 contains the transfer function equations for 2nd, 3rd and 4th order PLL filters.)

Figure 10. Overall Transfer Function of the PLL

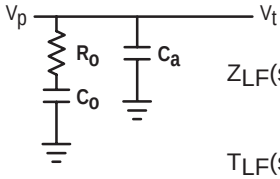
For the 2nd Order PLL:



$$Z_{LF}(s) = \frac{R_oC_os + 1}{C_os}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1\ ,\ V_p(s) = K_p(s)Z_{LF}(s)$$

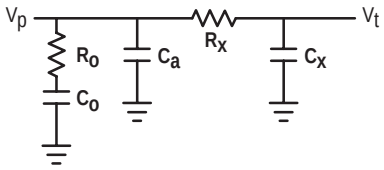
For the 3rd Order PLL:



$$Z_{LF}(s) = \frac{R_oC_os + 1}{C_oR_oC_as^2 + (C_o + C_a)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1\ ,\ V_p(s) = K_p(s)Z_{LF}(s)$$

For the 4th Order PLL:



$$Z_{LF}(s) = \frac{(R_oC_os + 1)\ (R_xC_xs + 1)}{C_oR_oC_aR_xC_xs^3 + [\ (C_o + C_a)R_xC_x + C_oR_o(C_x + C_a)\ ]\ s^2 + (C_o + C_a + C_x)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = \frac{1}{(R_xC_xs + 1)}\ ,\ V_p(s) = K_p(s)Z_{LF}(s)$$

Figure 11. Typical Charge Pump Current versus Temperature
(V_{CC} = 5.5 V; V_P = 6.0 V)

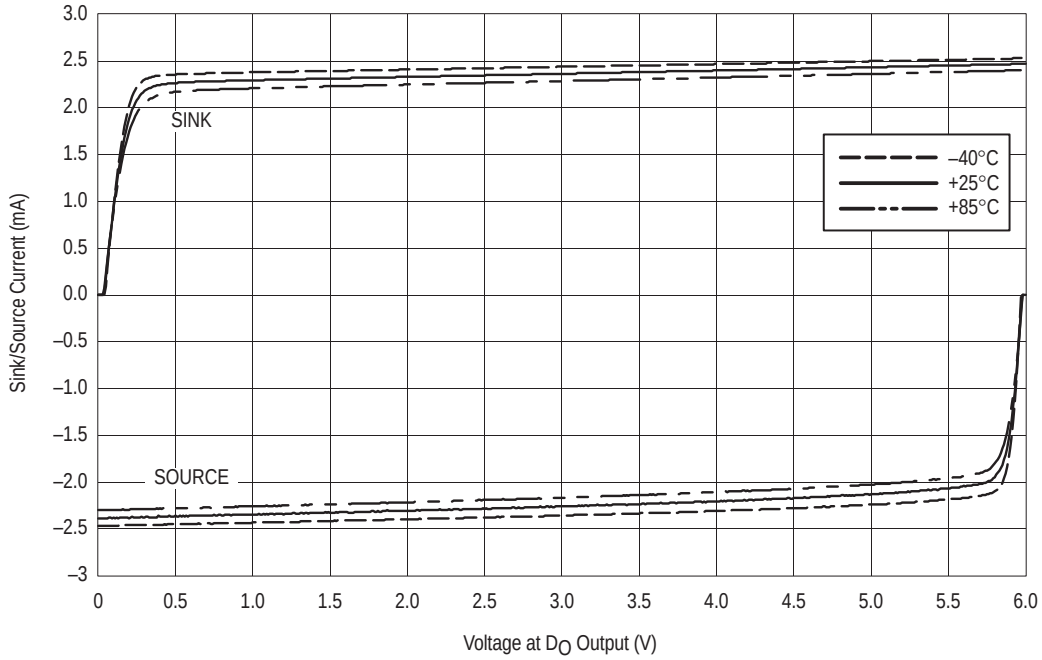


Figure 12. Typical Leakage Current at D_O Over V_{DO} Range
(V_{CC} = 5.5 V; V_P = 6.0 V; T = 25°C)

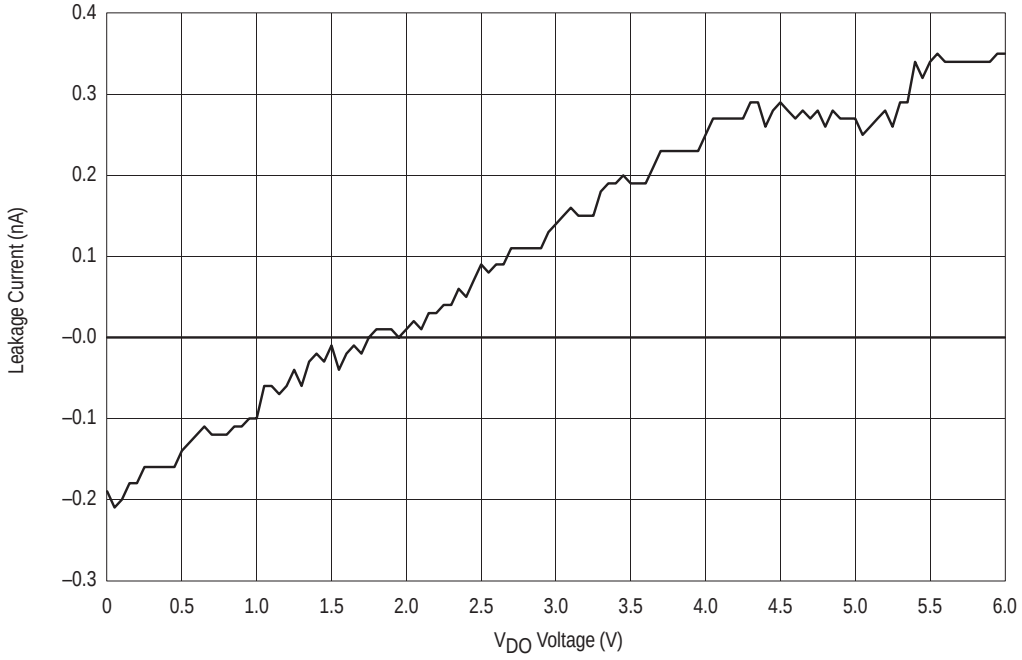


Figure 13. Typical F_{in} Input Impedance versus Input Frequency

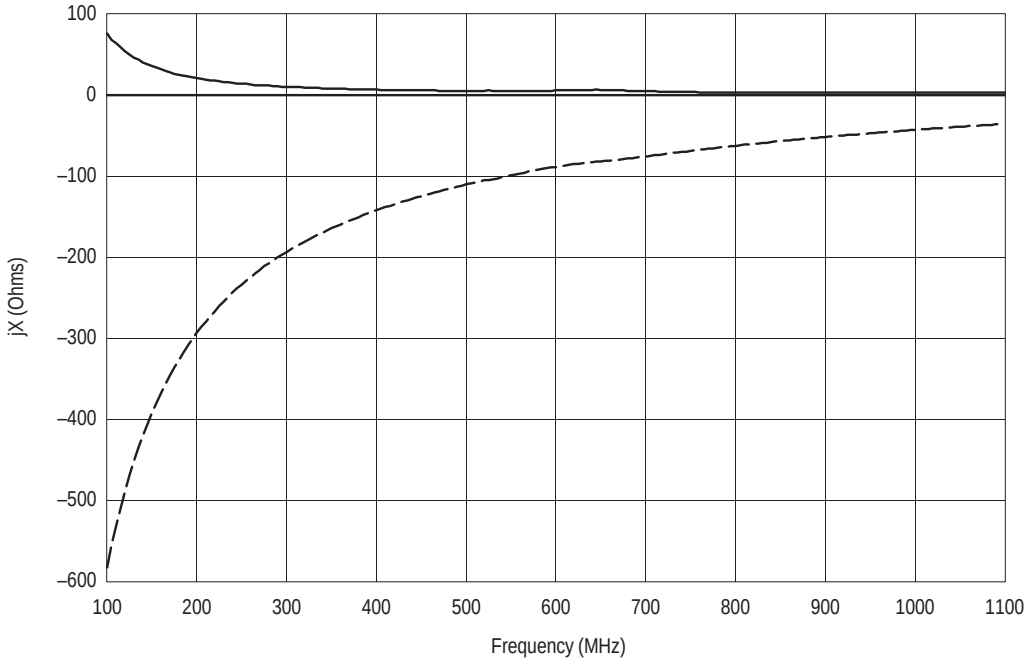


Figure 14. F_{in} Input Signal Sensitivity versus Input Frequency

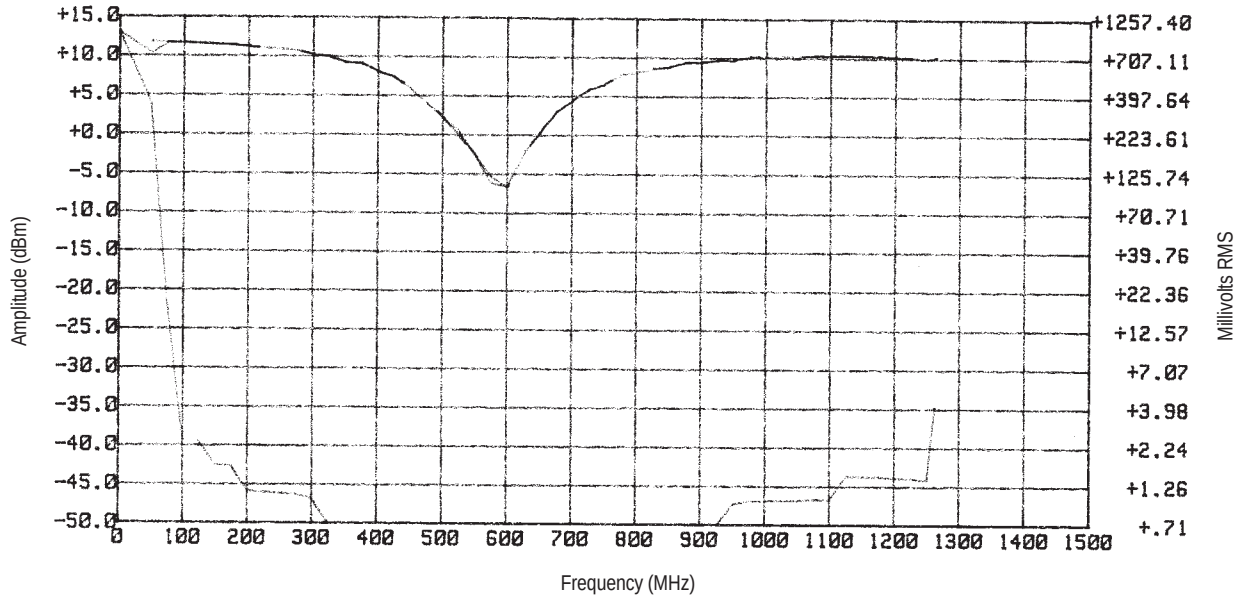


Figure 15. OSCin Input Sensitivity versus Input Frequency

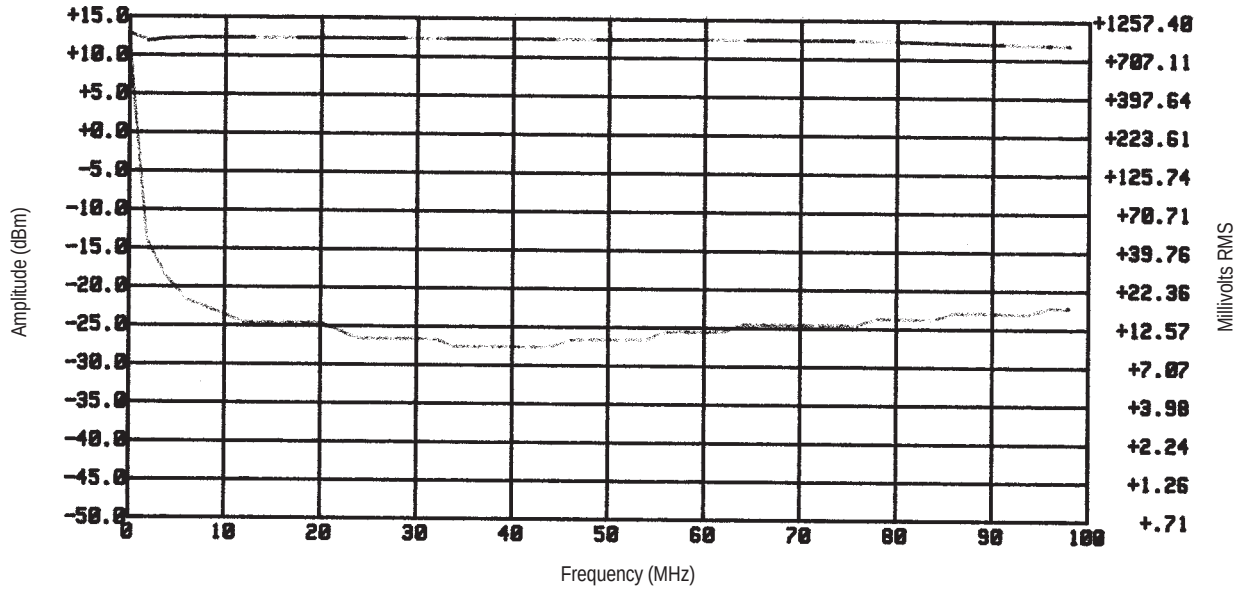


Figure 16. VCO Output Spectrum
(P=30, 8.0 MHz ECLiPTEK Crystal)

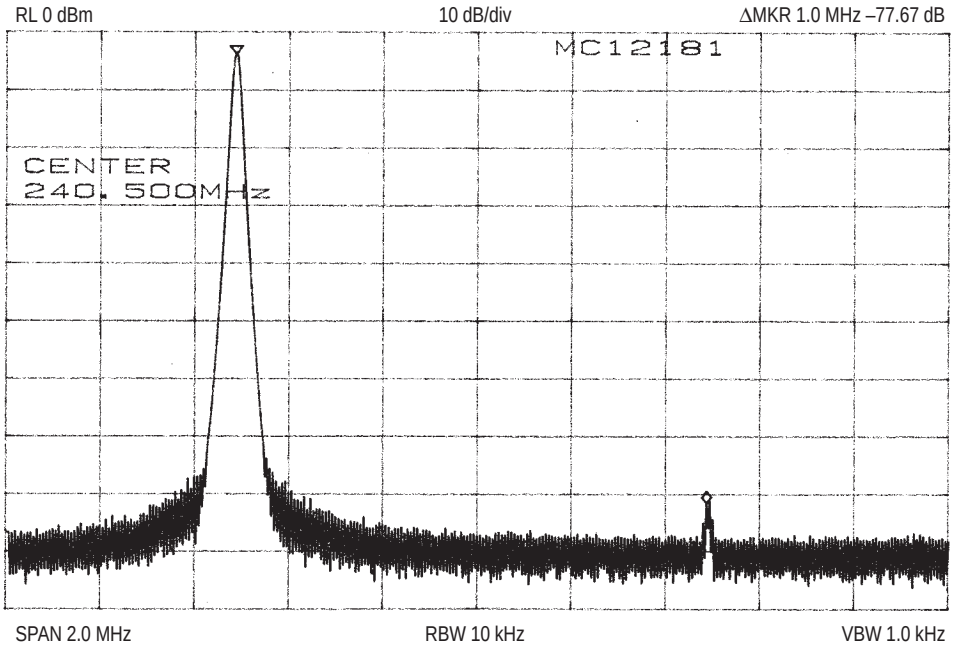
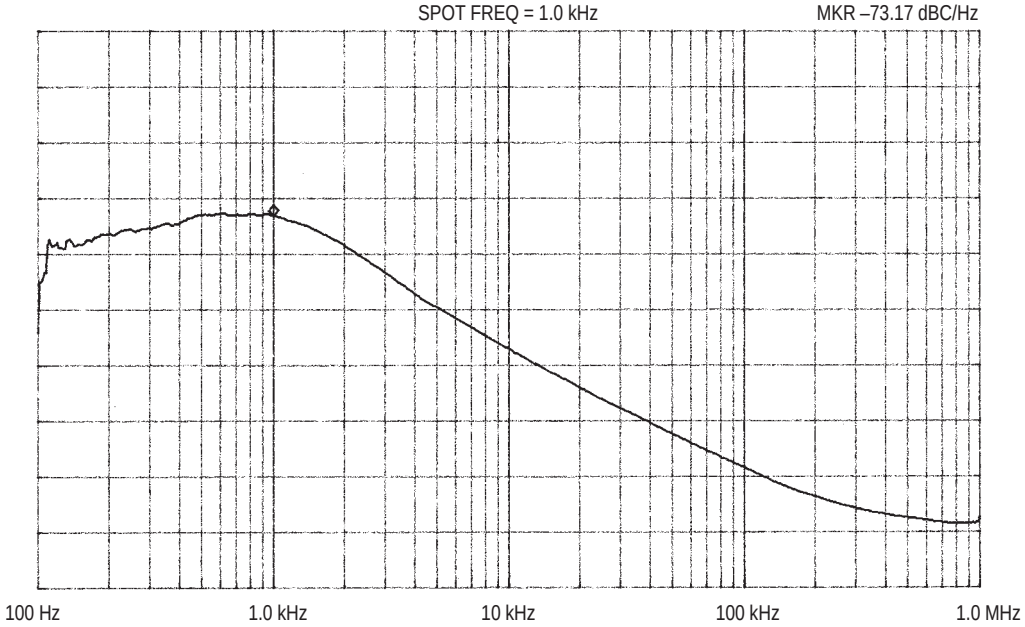


Figure 17. Typical Phase Noise Plot, 240MHz
(Low Noise 10 MHz Reference Input)



MOTOROLA

MC12210

Serial Input PLL Frequency Synthesizer

MECL PLL COMPONENTS
SERIAL PLL
FREQUENCY SYNTHESIZER

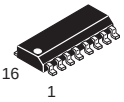
SEMICONDUCTOR
TECHNICAL DATA

The MC12210 is a 2.5 GHz Bipolar monolithic serial input phase locked loop (PLL) synthesizer with pulse–swallow function. It is designed to provide the high frequency local oscillator signal of an RF transceiver in handheld communication applications.

Motorola's advanced Bipolar MOSAIC™ V technology is utilized for low power operation at a minimum supply voltage of 2.7 V. The device is designed for operation over 2.7 to 5.5 V supply range for input frequencies up to 2.5 GHz with a typical current drain of 9.5 mA. The low power consumption makes the MC12210 ideal for handheld battery operated applications such as cellular or cordless telephones, wireless LAN or personal communication services. A dual modulus prescaler is integrated to provide either a 32/33 or 64/65 divide ratio.

For additional applications information, two *InterActiveApNote*™ documents containing software (based on a Microsoft Excel spreadsheet) and an Application Note are available. Please order DK305/D and DK306/D from the Motorola Literature Distribution Center.

- Low Power Supply Current of 8.8 mA Typical for I_{CC} and 0.7 mA Typical for I_P
- Supply Voltage of 2.7 to 5.5 V
- Dual Modulus Prescaler With Selectable Divide Ratios of 32/33 or 64/65
- On–Chip Reference Oscillator/Buffer
- Programmable Reference Divider Consisting of a Binary 14–Bit Programmable Reference Counter
- Programmable Divider Consisting of a Binary 7–Bit Swallow Counter and an 11–Bit Programmable Counter
- Phase/Frequency Detector With Phase Conversion Function
- Balanced Charge Pump Outputs
- Dual Internal Charge Pumps for Bypassing the First Stage of the Loop Filter to Decrease Lock Time
- Outputs for External Charge Pump
- Operating Temperature Range of –40 to 85°C
- Space Efficient Plastic Surface Mount SOIC or TSSOP Packages



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



DT SUFFIX
PLASTIC PACKAGE
CASE 948E
(TSSOP–20)

MOSAIC V, Mfax and *InterActiveApNote* are trademarks of Motorola, Inc.

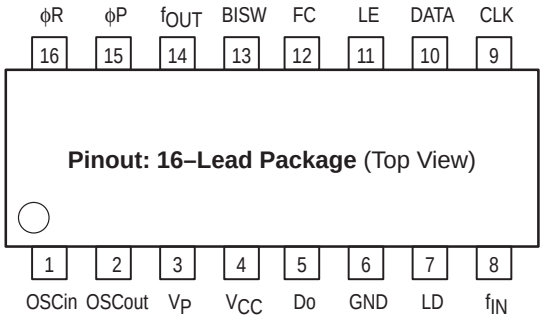
MAXIMUM RATINGS (Note 1)

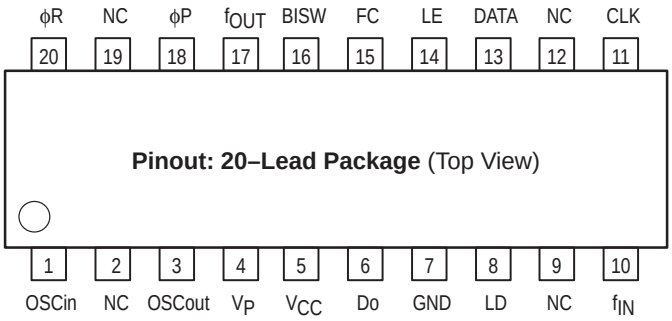
Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 4 (Pin 5 in 20–lead package)	V_{CC}	–0.5 to 6.0	Vdc
Power Supply Voltage, Pin 3 (Pin 4 in 20–lead package)	V_p	V_{CC} to 6.0	Vdc
Storage Temperature Range	Tstg	–65 to 150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
2. ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12210D	T_A = – 40° to +85°C	SO–16
MC12210DT		TSSOP–20

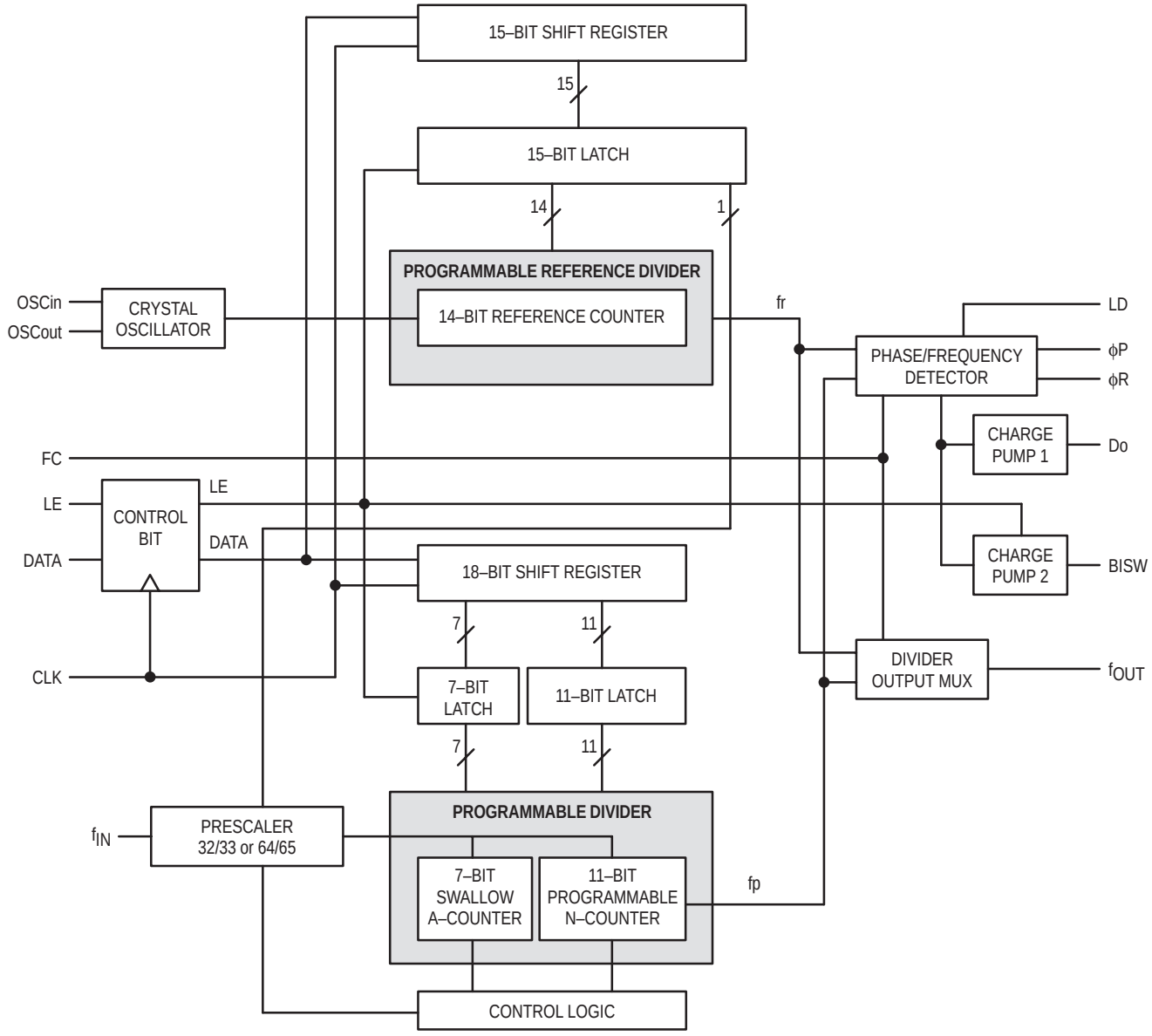




PIN NAMES

Pin	I/O	Function	16–Lead Pkg Pin No.	20–Lead Pkg Pin No.
OSCin	I	Oscillator input. A crystal may be connected between OSCin and OSCout. It is highly recommended that an external source be ac coupled into this pin (see text).	1	1
OSCout	O	Oscillator output. Pin should be left open if external source is used	2	3
V_P	—	Power supply for charge pumps (V_P should be greater than or equal to V_{CC}) V_P provides power to the Do, BISW and ϕP outputs	3	4
V_{CC}	—	Power supply voltage input. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.	4	5
Do	O	Internal charge pump output. Do remains on at all times	5	6
GND	—	Ground	6	7
LD	O	Lock detect, phase comparator output	7	8
f_{IN}	I	Prescaler input. The VCO signal is AC–coupled into this pin	8	10
CLK	I	Clock input. Rising edge of the clock shifts data into the shift registers	9	11
DATA	I	Binary serial data input	10	13
LE	I	Load enable input (with internal pull up resistor). When LE is HIGH or OPEN, data stored in the shift register is transferred into the appropriate latch (depending on the level of control bit). Also, when LE is HIGH or OPEN, the output of the second internal charge pump is connected to the BISW pin	11	14
FC	I	Phase control select (with internal pull up resistor). When FC is LOW, the characteristics of the phase comparator and charge pump are reversed. FC also selects fp or fr on the f_{OUT} pin	12	15
BISW	O	Analog switch output. When LE is HIGH or OPEN (“analog switch is ON”) the output of the second charge pump is connected to the BISW pin. When LE is LOW, BISW is high impedance	13	16
f_{OUT}	O	Phase comparator input signal. When FC is HIGH, f_{OUT}=fr, programmable reference divider output; when FC is LOW, f_{OUT}=fp, programmable divider output	14	17
ϕP	O	Output for external charge pump. Standard CMOS output level	15	18
ϕR	O	Output for external charge pump. Standard CMOS output level	16	20
NC	—	No connect	—	2, 9, 12, 19

Figure 1. MC12210 Block Diagram



DATA ENTRY FORMAT

The three wire interface of DATA pin, CLK (clock) pin and LE (load enable) pin controls the serial data input of the 14–bit programmable reference divider plus the prescaler setting bit, and the 18–bit programmable divider. A rising edge of the clock shifts one bit of serial data into the internal shift registers. Depending upon the level of the control bit, stored data is transferred into the latch when load enable pin is HIGH or OPEN.

Control bit: "H" = data is transferred into 15–bit latch of programmable reference divider

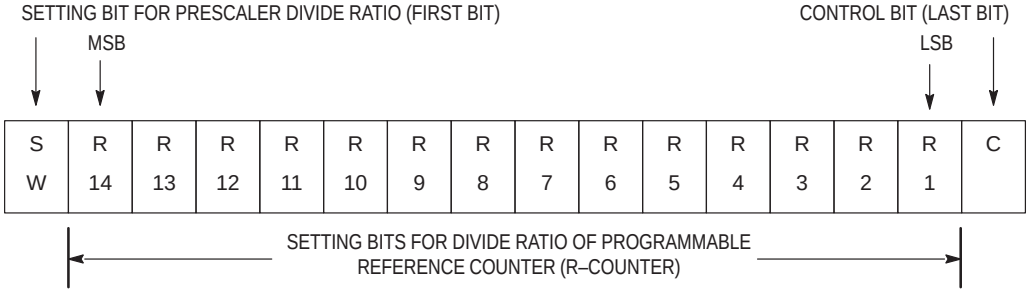
"L" = data is transferred into 18–bit latch of programmable divider

WARNING: Switching CLK or DATA after the device is programmed may generate noise on the charge pump outputs which will affect the VCO.

PROGRAMMABLE REFERENCE DIVIDER

16–bit serial data format for the programmable reference counter, "R–counter", and prescaler select bit (SW) is shown below. If the control bit is HIGH, data is transferred from the 15–bit shift register into the 15–bit latch which specifies the R divide ratio (8 to 16383) and the prescaler divide ratio (SW=0 for ÷64/65, SW=1 for ÷32/33). An R divide ratio less than 8 is prohibited.

For Control bit (C) = HIGH:



DIVIDE RATIO OF PROGRAMMABLE REFERENCE (R) COUNTER

Divide Ratio R	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

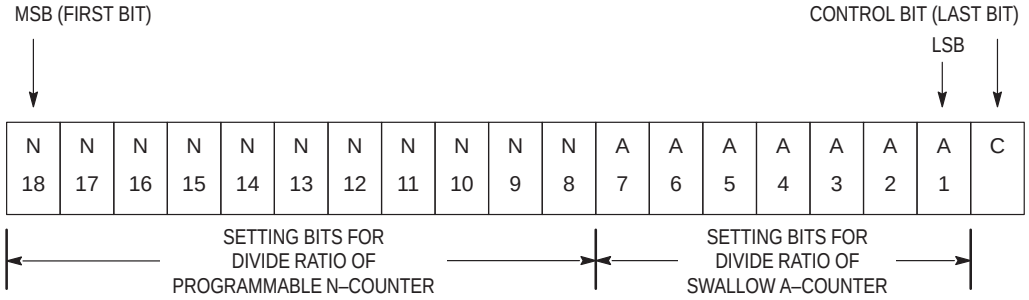
PRESCALER SELECT BIT

Prescaler Divide Ratio P	SW
64/65	0
32/33	1

PROGRAMMABLE DIVIDER

19–bit serial data format for the programmable divider is shown below. If the control bit is LOW, data is transferred from the 18–bit shift register into the 18–bit latch which specifies the swallow A–counter divide ratio (0 to 127) and the programmable N–counter divide ratio (16 to 2047). An N–counter divide ratio less than 16 is prohibited.

For Control bit (C) = LOW:



DIVIDE RATIO OF PROGRAMMABLE N–COUNTER **DIVIDE RATIO OF SWALLOW A–COUNTER**

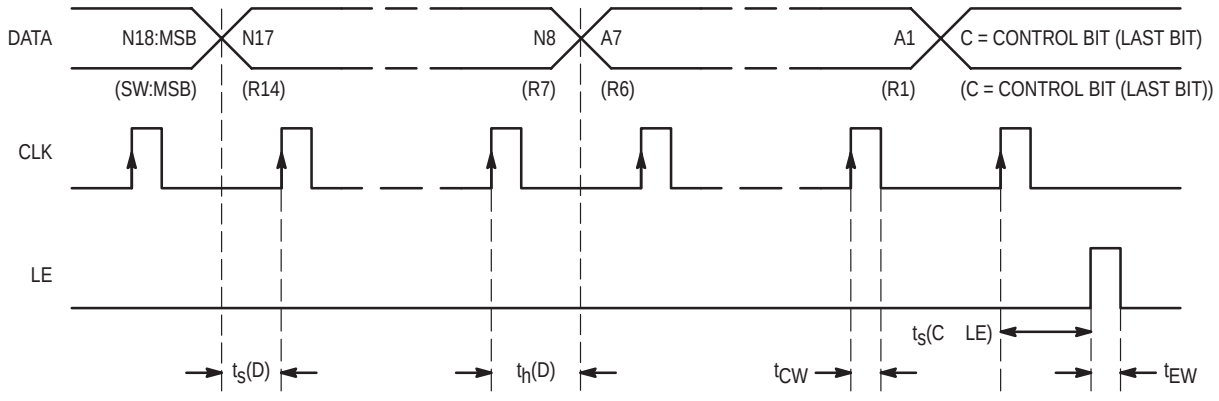
Divide Ratio N	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8	Divide Ratio A	A 7	A 6	A 5	A 4	A 3	A 2	A 1
16	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1	127	1	1	1	1	1	1	1

DIVIDE RATIO SETTING

fvco = [(P•N)+A]•fosc ÷ R with A<N

- fvco: Output frequency of external voltage controlled oscillator (VCO)
- N: Preset divide ratio of binary 11–bit programmable counter (16 to 2047)
- A: Preset divide ratio of binary 7–bit swallow counter (0 to 127, A<N)
- fosc: Output frequency of the external frequency oscillator
- R: Preset divide ratio of binary 14–bit programmable reference counter (8 to 16383)
- P: Preset mode of dual modulus prescaler (32 or 64)

Figure 2. Serial Data Input Timing



NOTES:Programmable reference divider data shown in parenthesis. Data shifted into register on rising edge of CLK.

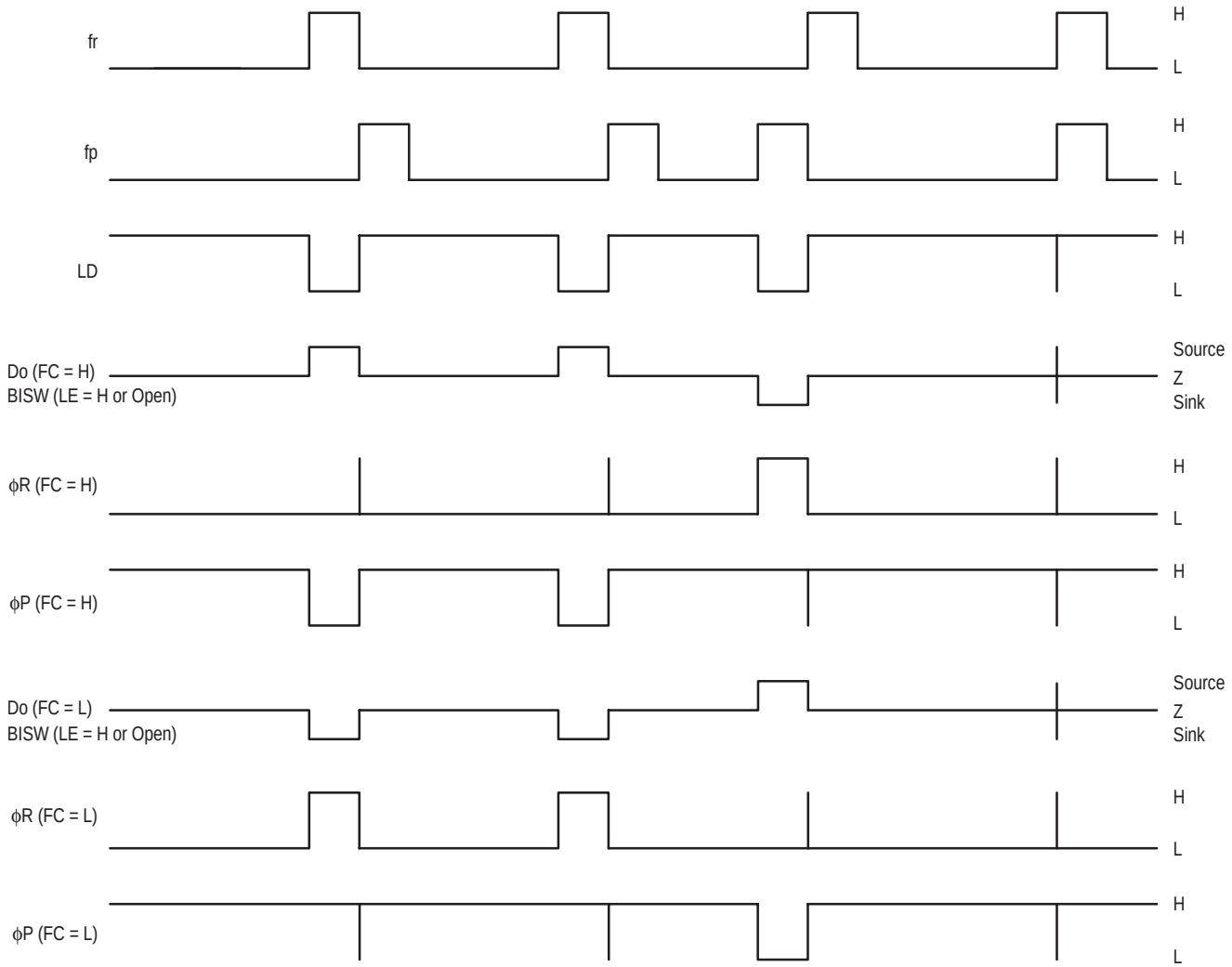
$t_S(D)$ = Setup Time DATA to CLK	$t_S(D) \geq 10$ ns
$t_h(D)$ = Hold Time DATA to CLK	$t_h(D) \geq 20$ ns
t_{CW} = CLK Pulse Width	$t_{CW} \geq 30$ ns
t_{EW} = LE Pulse Width	$t_{EW} \geq 20$ ns
t_S(C LE) = Setup Time CLK to LE	t_S(C LE) ≥ 30 ns

PHASE CHARACTERISTICS/VCO CHARACTERISTICS

The phase comparator in the MC12210 is a high speed digital phase frequency detector circuit. The circuit determines the “lead” or “lag” phase relationship and time difference between the leading edges of the VCO (fp) signal and the reference (fr) input. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians. The phase comparator outputs are standard CMOS rail–to–rail levels (V_P to GND for ϕP and V_{CC} to GND for ϕR), designed for up to 20MHz operation into a 15pF load. These phase comparator outputs can be used along with an external charge pump to enhance the PLL characteristics.

The operation of the phase comparator is shown in Figures 3 and 5. The phase characteristics of the phase comparator are controlled by the FC pin. The polarity of the phase comparator outputs, ϕR and ϕP, as well as the charge pump output Do can be reversed by switching the FC pin.

Figure 3. Phase/Frequency Detector, Internal Charge Pump and Lock Detect Waveforms



NOTES: Do and BISW are current outputs.
Phase difference detection range: -2π to $+2\pi$
Spike difference depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When fr > fp or fr < fp, spike might not appear depending upon charge pump characteristics.

$$\text{Internal Charge Pump Gain} \approx \left| \frac{I_{source} + I_{sink}}{4\pi} \right| = \frac{4mA}{4\pi}$$

For FC = HIGH:

fr lags fp in phase OR fp>fr in frequency

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the ϕP output will remain in a HIGH state while the ϕR output will pulse from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕR indicates to the VCO to decrease in frequency to bring the loop into lock.

fr leads fp in phase OR fp<fr in frequency

When the phase of fr leads that of fp or the frequency of fp is less than fr, the ϕR output will remain in a LOW state while the ϕP output pulses from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕP indicates to the VCO to increase in frequency to bring the loop to lock.

fr = fp in phase and frequency

When the phase and frequency of fr and fp are equal, the output ϕP will remain in a HIGH state and ϕR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

When FC = LOW, the operation of the phase comparator is reversed from the above explanation.

For FC = LOW:

fr lags fp in phase OR fp>fr in frequency

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the ϕR output will remain in a LOW state while the ϕP output will pulse from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕP indicates to the VCO to increase in frequency to bring the loop into lock.

fr leads fp in phase OR fp<fr in frequency

When the phase of fr leads that of fp or the frequency of fp is less than fr, the ϕP output will remain in a HIGH state while the ϕR output pulses from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕR indicates to the VCO to decrease in frequency to bring the loop to lock.

fr = fp in phase and frequency

When the phase and frequency of fr and fp are equal, the output ϕP will remain in a HIGH state and ϕR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

The FC pin controls not only the phase characteristics, but also controls the f_{OUT} test pin. The FC pin permits the user to monitor either of the phase comparator input signals, fr or fp, at the f_{OUT} output providing a test mode where the programming of the dividers and the output of the counters can be checked. When FC is HIGH, f_{OUT} = fr, the programmable reference divider output. When FC is LOW, f_{OUT} = fp, the programmable divider output.

Hence,

If VCO characteristics are like (1), FC should be set HIGH or OPEN. f_{OUT} = fr

If VCO characteristics are like (2), FC should be set LOW. f_{OUT} = fp

Figure 4. VCO Characteristics

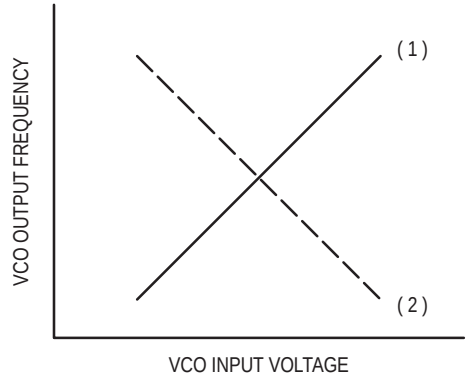


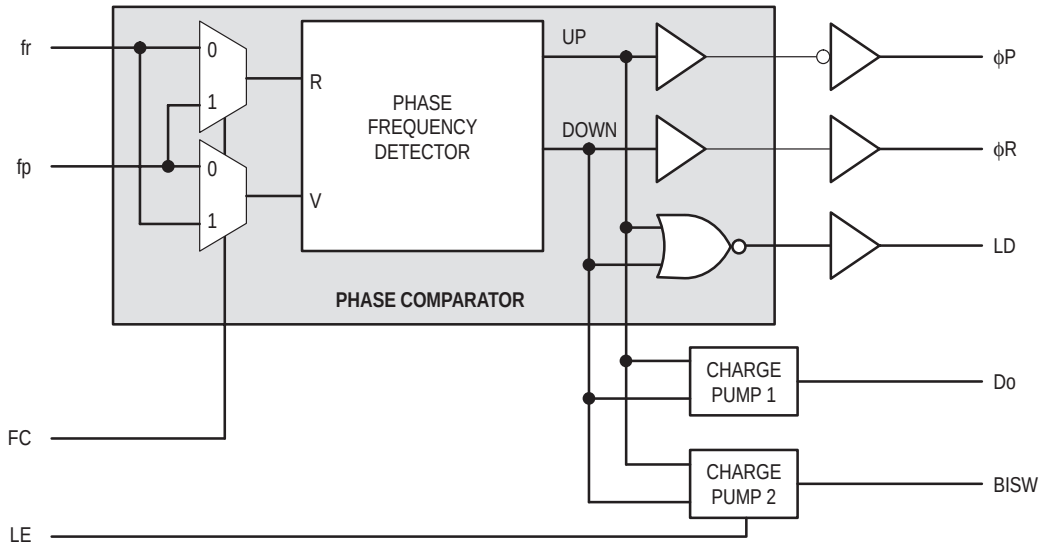
Figure 5. Phase Comparator, Internal Charge Pump, and f_{OUT} Characteristics

	FC = HIGH or OPEN				FC = LOW			
	Do	**ϕR**	**ϕP**	**f_{OUT}**	**Do**	**ϕR**	**ϕP**	**f_{OUT}**
fp < fr	H	L	L	fr	L	H	H	fp
fp > fr	L	H	H	fr	H	L	L	fp
fp = fr	Z	L	H	fr	Z	L	H	fp

NOTES: Z = High impedance

When LE is HIGH or Open, BISW has the same characteristics as Do.

Figure 6. Detailed Phase Comparator Block Diagram



LOCK DETECT

The Lock Detect (LD) output pin provides a LOW pulse when fr and fp are not equal in phase or frequency. The output is normally HIGH. LD is designed to be the logical NORing of the phase frequency detector's outputs UP and DOWN. See Figure 6. In typical applications the output signal drives external circuitry which provides a steady LOW signal when the loop is locked. See Figure 9.

OSCILLATOR INPUT

For best operation, an external reference oscillator is recommended. The signal should be AC–coupled to the OSCin pin through a coupling capacitor. In this case, no connection to OSCout is required. The magnitude of the AC–coupled signal must be between 500 and 2200 mV peak–to–peak. To optimize the phase noise of the PLL when used in this mode, the input signal amplitude should be closer to the upper specification limit. This maximizes the slew rate of the signal as it switches against the internal voltage reference.

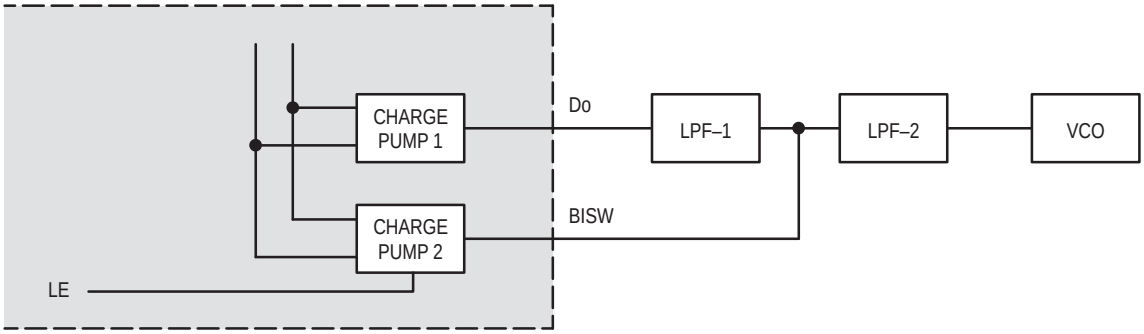
The device incorporates an on–chip reference oscillator/buffer so that an external parallel–resonant fundamental crystal can be connected between OSCin and OSCout. External capacitor C1 and C2 as shown in Figure 10 are required to set the proper crystal load capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal chosen (up to a maximum of 30 pF each including parasitic and stray capacitance). However, using the on–chip reference oscillator greatly increases the synthesized phase noise.

DUAL INTERNAL CHARGE PUMPS ("ANALOG SWITCH")

Due to the pure Bipolar nature of the MC12210 design, the "analog switch" function is implemented with dual internal charge pumps. The loop filter time constant can be decreased by bypassing the first stage of the loop filter with the charge pump output BISW as shown in Figure 7 below. This enables the VCO to lock in a shorter amount of time.

When LE is HIGH or OPEN ("analog switch is ON"), the output of the second internal charge pump is connected to the BISW pin, and the Do output is ON. The charge pump 2 output on BISW is essentially equal to the charge pump 1 output on Do. When LE is LOW, BISW is in a high impedance state and Do output is active.

Figure 7. "Analog Switch" Block Diagram



ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; T_A = –40 to +85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Current for V_{CC}	I_{CC}	–	8.8	13.0	mA	Note 1
		–	10.2	16.0		Note 2
Supply Current for V_P	I_P	–	0.7	1.1	mA	Note 3
		–	0.8	1.3		Note 4
Operating Frequency f_{IN}max f_{IN}min	F_{IN}	2500 –	– –	– 500	MHz	Note 5
Operating Frequency (OSCin)	F_{OSC}	–	12	20	MHz	Crystal Mode
		–	–	40	MHz	External Reference Mode
Input Sensitivity f_{IN}	V_{IN}	200	–	1000	mVpp	
OSCin	V_{OSC}	500	–	2200	mVpp	
Input HIGH Voltage CLK, DATA, LE, FC	V_{IH}	0.7 V_{CC}	–	–	V	
Input LOW Voltage CLK, DATA, LE, FC	V_{IL}	–	–	0.3 V_{CC}	V	V_{CC} = 5.5 V
Input HIGH Current (DATA and CLK)	I_{IH}	–	1.0	2.0	µA	V_{CC} = 5.5 V
Input LOW Current (DATA and CLK)	I_{IL}	–10	–5.0	–	µA	V_{CC} = 5.5 V
Input Current (OSCin)	I_{OSC}	– –	130 –310	– –	µA	OSCin = V_{CC} OSCin = V_{CC} – 2.2 V
Input HIGH Current (LE and FC)	I_{IH}	–	1.0	2.0	µA	
Input LOW Current (LE and FC)	I_{IL}	–75	–60	–	µA	
Charge Pump Output Current	I_{Source}[6]	–2.6	–2.0	–1.4	mA	V_{Do} = V_p/2; V_p = 2.7 V
Do and BISW	I_{Sink}[6]	+1.4	+2.0	+2.6		V_{BISW} = V_p/2; V_p = 2.7 V
	I_{Hi-Z}	–15	–	+15	nA	0.5< V_{DO} < V_p – 0.5 0.5 < V_{BISW} < V_p – 0.5
Output HIGH Voltage (LD, ϕR, ϕP, f_{OUT})	V_{OH}	4.4	–	–	V	V_{CC} = 5.0 V
		2.4	–	–	V	V_{CC} = 3.0 V
Output LOW Voltage (LD, ϕR, ϕP, f_{OUT})	V_{OL}	–	–	0.4	V	V_{CC} = 5.0 V
		–	–	0.4	V	V_{CC} = 3.0 V
Output HIGH Current (LD, ϕR, ϕP, f_{OUT})	I_{OH}	–1.0	–	–	mA	
Output LOW Current (LD, ϕR, ϕP, f_{OUT})	I_{OL}	1.0	–	–	mA	

1. V_{CC} = 3.3 V, all outputs open.
2. V_{CC} = 5.5 V, all outputs open.
3. V_P = 3.3 V, all outputs open.
4. V_p = 6.0 V, all outputs open.
5. AC coupling, F_{IN} measured with a 1000 pF capacitor.
6. Source current flows out of the pin and sink current flows into the pin.

Figure 8. Typical External Charge Pump Circuit

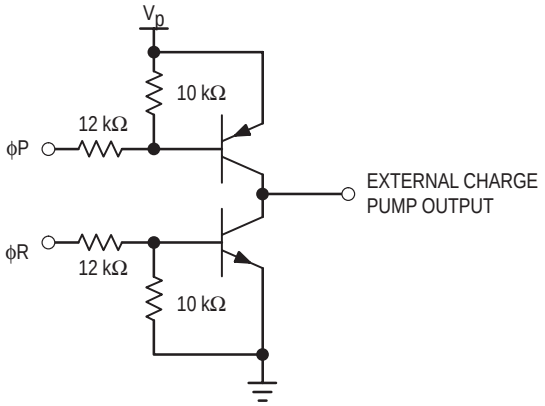


Figure 9. Typical Lock Detect Circuit

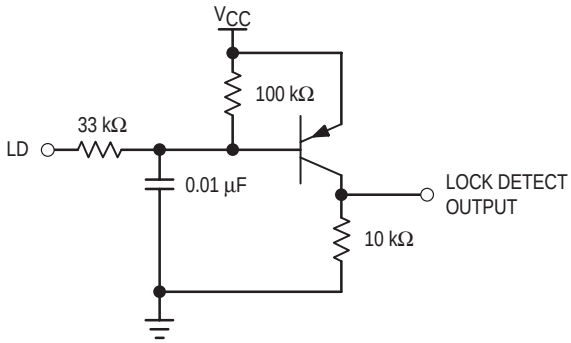
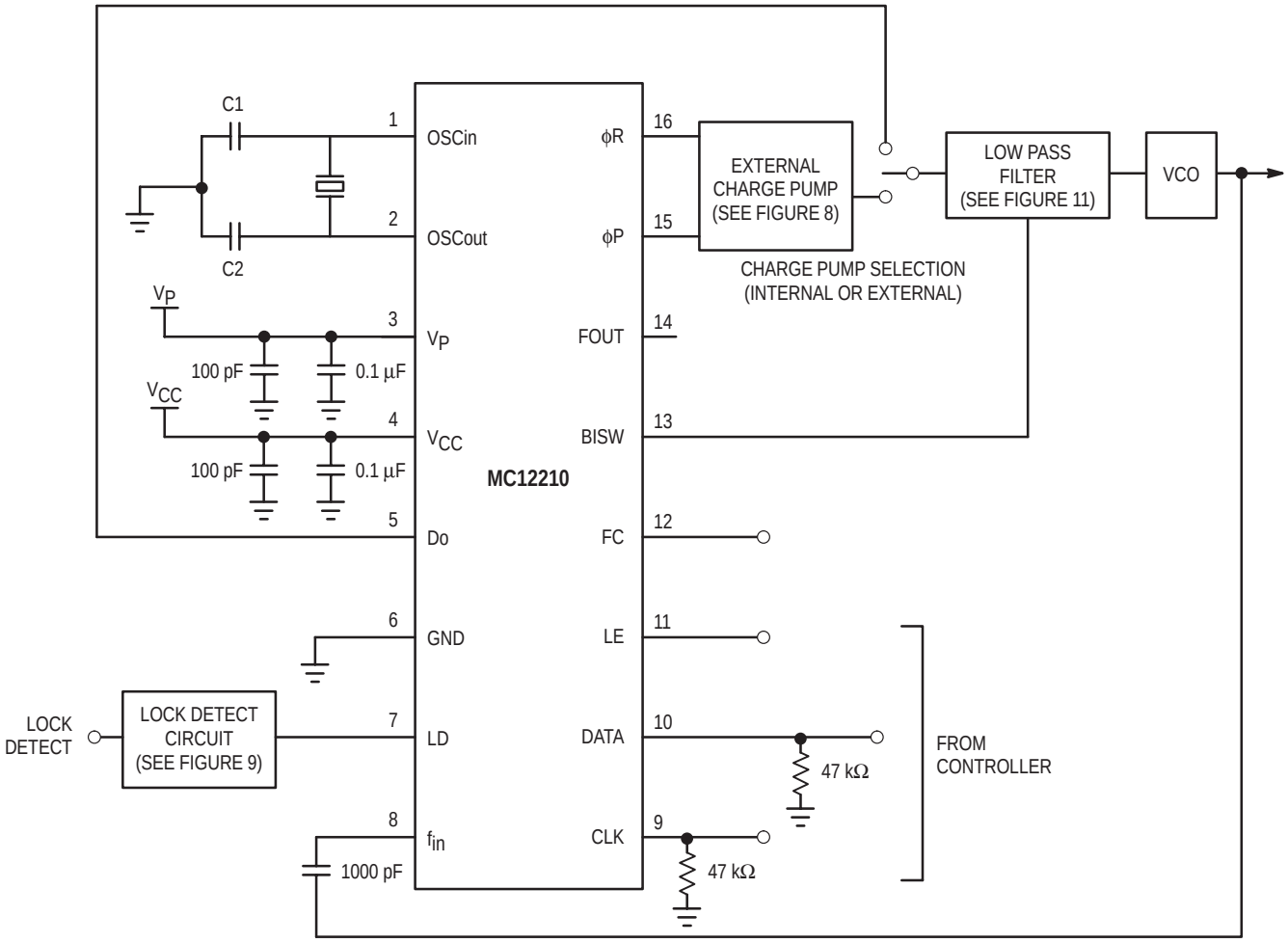
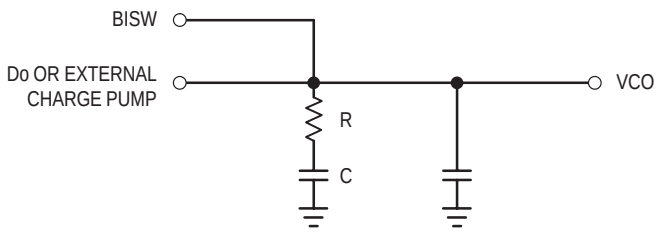


Figure 10. Typical Applications Example (16–Pin Package)



C1, C2: Dependent on Crystal Oscillator

Figure 11. Typical Loop Filter



MOTOROLA

Phase-Frequency Detector

MCH12140
MCK12140

PHASE–FREQUENCY DETECTOR

SEMICONDUCTOR TECHNICAL DATA

The MCH/K12140 is a phase frequency-detector intended for phase-locked loop applications which require a minimum amount of phase and frequency difference at lock. When used in conjunction with the MC12147, MC12148 or MC12149 VCO, a high bandwidth PLL can be realized. The device is functionally compatible with the MC12040 phase-frequency detector, however the MOSAIC™ III process is used to push the maximum frequency to 800 MHz and significantly reduce the dead zone of the detector. When the Reference (R) and VCO (V) inputs are unequal in frequency and/or phase, the differential UP (U) and DOWN (D) outputs will provide pulse streams which when subtracted and integrated provide an error voltage for control of a VCO.

The device is packaged in a small outline, surface mount 8-lead SOIC package. There are two versions of the device to provide I/O compatibility to the two existing ECL standards. The MCH12140 is compatible with MECL10H™ logic levels while the MCK12140 is compatible to 100K ECL logic levels. This device can also be used in +5.0 V systems. Please refer to Motorola Application Note AN1406/D, “Designing with PECL (ECL at +5.0 V)” for more information.

- 800 MHz Typical Bandwidth
- Small Outline 8-Lead SOIC Package
- 75 kΩ Internal Input Pulldown Resistors
- >1000 V ESD Protection

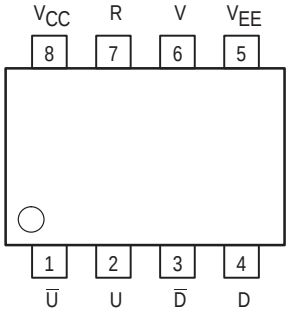
For proper operation, the input edge rate of the R and V inputs should be less than 5ns.

MOSAIC III and MECL 10H are trademarks of Motorola



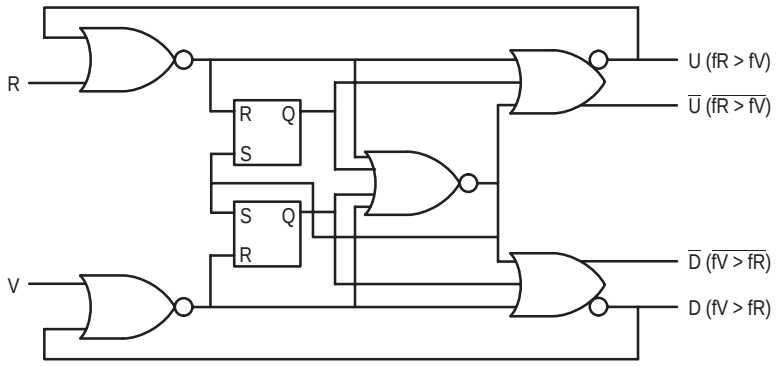
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

LOGIC DIAGRAM



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MCH1214OD	T_A = –40° to +70°C	SO–8
MCK12140D		

TRUTH TABLE*

Input		Output				Input		Output			
R	V	U	D	$\overline{U}$	$\overline{D}$	R	V	U	D	$\overline{U}$	$\overline{D}$
0	0	X	X	X	X	1	1	0	0	1	1
0	1	X	X	X	X	1	0	0	0	1	1
1	1	X	X	X	X	1	1	0	1	1	0
0	1	X	X	X	X	1	0	0	1	1	0
1	1	1	0	0	1	1	1	0	1	1	0
0	1	1	0	0	1	0	1	0	1	1	0
1	1	1	0	0	1	1	1	0	1	1	0
1	0	1	0	0	1	1	1	0	0	1	1

NOTE: * This is not strictly a functional table; i.e., it does not cover all possible modes of operation. However, it gives a sufficient number of tests to ensure that the device will function properly.

H–SERIES DC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND[1], unless otherwise noted.)

Characteristic	Symbol	–40°C		0°C		25°C		70°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Output HIGH Voltage	V_{OH}	–1080	–890	–1020	–840	–980	–810	–910	–720	mV
Output LOW Voltage	V_{OL}	–1950	–1650	–1950	–1630	–1950	–1630	–1950	–1595	mV
Input HIGH Voltage	V_{IH}	–1230	–890	–1170	–840	–1130	–810	–1060	–720	mV
Input LOW Voltge	V_{IL}	–1950	–1500	–1950	–1480	–1950	–1480	–1950	–1445	mV
Input LOW Current	I_{IL}	0.5	—	0.5	—	0.5	—	0.3	—	μA

NOTE: 1. 10H circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

K–SERIES DC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND[1], unless otherwise noted.)

Characteristic	Symbol	–40°C			0°C to 70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max		
Output HIGH Voltage	V_{OH}	–1085	–1005	–880	–1025	–955	–880	mV	V_{IN} = V_{IH}(max)
Output LOW Voltage	V_{OL}	–1830	–1695	–1555	–1810	–1705	–1620	mV	or V_{IL}(min)
Output HIGH Voltage	V_{OHA}	–1095	—	—	–1035	—	—	mV	V_{IN} = V_{IH}(min)
Output LOW Voltage	V_{OLA}	—	—	–1555	—	—	–1610	mV	or V_{IL}(max)
Input HIGH Voltage	V_{IH}	–1165	—	–880	–1165	—	–880	mV	
Input LOW Voltge	V_{IL}	–1810	—	–1475	–1810	—	–1475	mV	
Input LOW Current	I_{IL}	0.5	—	—	0.5	—	—	μA	V_{IN} = V_{IL}(max)

NOTE: 1. This table replaces the three tables traditionally seen in ECL 100K data books. The same DC parameter values at V_{EE} = –4.5V now apply across the full V_{EE} range of –4.2V to –5.5V. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0V)	V_{EE}	–8.0 to 0	VDC
Input Voltage (V_{CC} = 0V)	V_I	0 to –6.0	VDC
Output Current Continuous Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	–40 to +70	°C
Operating Range[1,2]	V_{EE}	–5.7 to –4.2	V

NOTES: 1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
2. Parametric values specified at: H–Series: –4.20 V to –5.50 V
K–Series: –4.94 V to –5.50 V
3. ESD data available upon request.

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND, unless otherwise noted.)

Characteristic		Symbol	–40°C			0°C			25°C			70°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply Current	H	I_{EE}		45		38	45	52	38	45	52	38	45	52	mA
	K			45		38	45	52	38	45	52	42	50	58	
Power Supply Voltage	H	V_{EE}	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	V
	K		–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
Input HIGH Current		I_{IH}			150			150			150			150	μA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND, unless otherwise noted.)

Characteristic		Symbol	–40°C			0°C			25°C			70°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Maximum Toggle Frequency		F_{MAX}		800		650	800		650	800		650	800		
Propagation Delay to Output	R to D	t_{PLH} t_{PHL}		440		320	440	580	320	440	580	360	480	620	ps
	R to U			330		210	330	470	210	330	470	240	360	500	
	V to D			330		210	330	470	210	330	470	240	360	500	
	V to U			440		320	440	580	320	440	580	360	480	620	
Output Rise/Fall Times Q (20 to 80%)		t_r t_f		225		100	225	350	100	225	350	100	225	350	ps

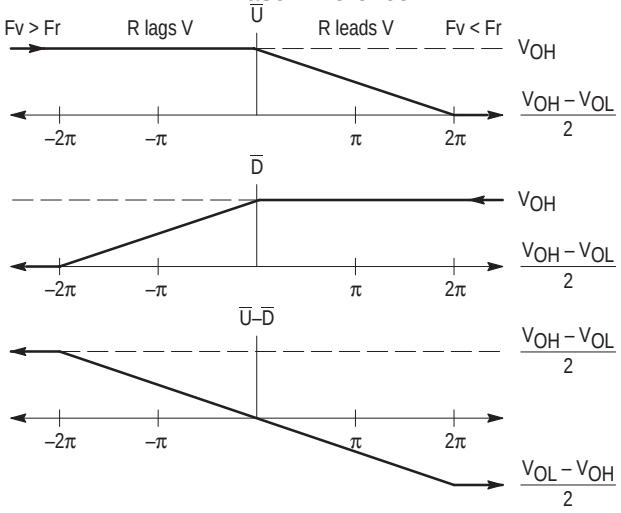
APPLICATIONS INFORMATION

The 12140 is a high speed digital circuit used as a phase comparator in an analog phase-locked loop. The device determines the “lead” or “lag” phase relationship and time difference between the leading edges of a VCO (V) signal and a Reference (R) input. Since these edges occur only once per cycle, the detector has a range of ±2π radians.

The operation of the 12140 can best be described using the plots of Figure 1. Figure 1 plots the average value of $\overline{U}$, $\overline{D}$ and the difference between $\overline{U}$ and $\overline{D}$ versus the phase difference between the V and R inputs.

There are four potential relationships between V and R: R lags or leads V and the frequency of R is less than or greater than the frequency of V. Under these four conditions the 12140 will function as follows:

Figure 1. Average Output Voltage versus Phase Difference



R lags V in phase

When the R and V inputs are equal in frequency and the phase of R lags that of V the $\overline{U}$ output will stay HIGH while the $\overline{D}$ output will pulse from HIGH to LOW. The magnitude of the pulse will be proportional to the phase difference between the V and R inputs reaching a minimum 50% duty cycle under a 180° out of phase condition. The signal on $\overline{D}$ indicates to the VCO to decrease in frequency to bring the loop into lock.

V frequency > R frequency

When the frequency of V is greater than that of R the 12140 behaves in a simlar fashion as above. Again the signal on $\overline{D}$ indicates that the VCO frequency must be decreased to bring the loop into lock.

R leads V in phase

When the R and V inputs are equal in frequency and the phase of R leads that of V the $\overline{D}$ output will stay HIGH while the $\overline{U}$ output pulses from HIGH to LOW. The magnitude of the pulse will be proportional to the phase difference between the V and R inputs reaching a minimum 50% duty cycle under a 180° out of phase condition. The signal on $\overline{U}$ indicates to the VCO to increase in frequency to bring the loop into lock.

V frequency < R frequency

When the frequency of V is less than that of R the 12140 behaves in a simlar fashion as above. Again the signal on $\overline{U}$ indicates that the VCO frequency must be decreased to bring the loop into lock.

From Figure 1 when V and R are at the same frequency and in phase the value of $\overline{U}$ – $\overline{D}$ is zero thus providing a zero error voltage to the VCO. This situation indicates the loop is in lock and the 12140 action will maintain the loop in its locked state.

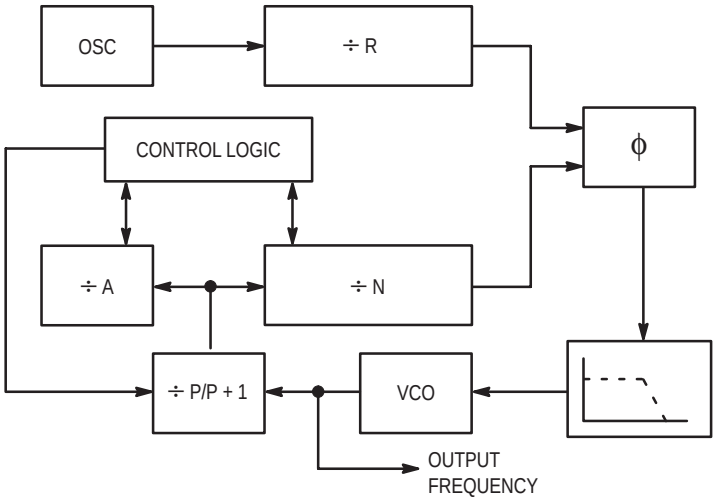
PLL Frequency Synthesizer Family
CMOS

MC145151-2
MC145152-2
MC145157-2
MC145158-2

The devices described in this document are typically used as low–power, phase–locked loop frequency synthesizers. When combined with an external low–pass filter and voltage–controlled oscillator, these devices can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a prescaler can be used between the VCO and the synthesizer IC.

These frequency synthesizer chips can be found in the following and other applications:

CATV	TV Tuning
AM/FM Radios	Scanning Receivers
Two–Way Radios	Amateur Radio



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REV 4
12/99

MC145151-2

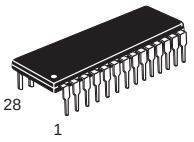
Parallel-Input PLL Frequency Synthesizer

Interfaces with Single–Modulus Prescalers

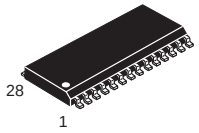
The MC145151–2 is programmed by 14 parallel–input data lines for the N counter and three input lines for the R counter. The device features consist of a reference oscillator, selectable–reference divider, digital–phase detector, and 14–bit programmable divide–by–N counter.

The MC145151–2 is an improved–performance drop–in replacement for the MC145151–1. The power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Lock Detect Signal
- ÷ N Counter Output Available
- Single Modulus/Parallel Programming
- 8 User–Selectable ÷ R Values: 8, 128, 256, 512, 1024, 2048, 2410, 8192
- ÷ N Range = 3 to 16383
- “Linearized” Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single–Ended (Three–State) or Double–Ended
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 710

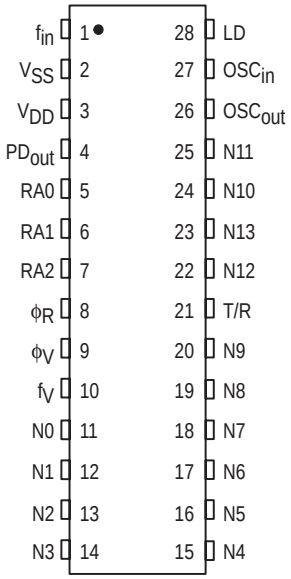


DW SUFFIX
SOG PACKAGE
CASE 751F

ORDERING INFORMATION

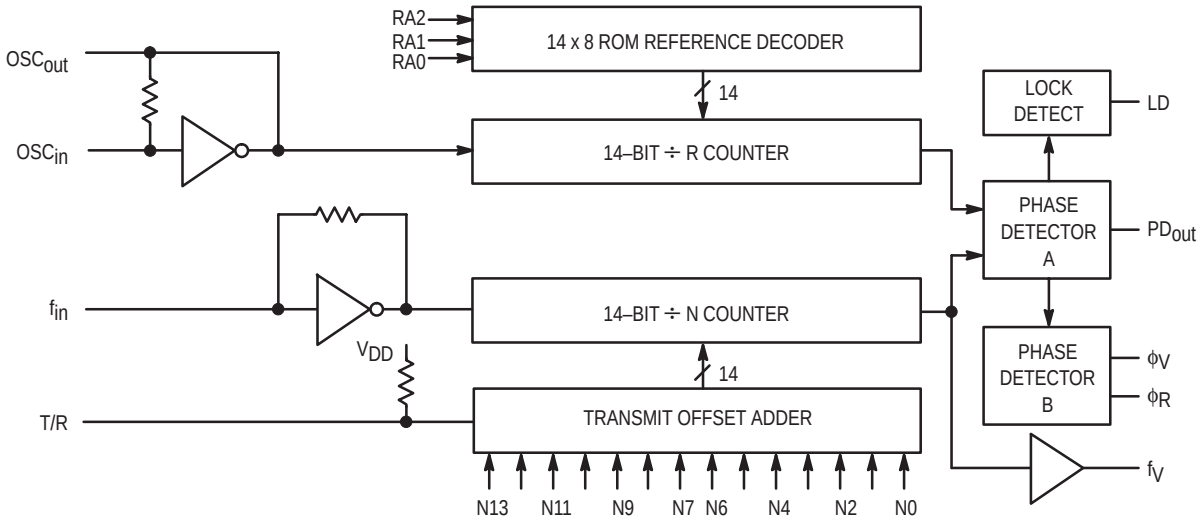
MC145151P2	Plastic DIP
MC145151DW2	SOG Package

PIN ASSIGNMENT



REV 1
8/95

MC145151–2 BLOCK DIAGRAM



NOTE: N0 – N13 inputs and inputs RA0, RA1, and RA2 have pull–up resistors that are not shown.

PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 1)

Input to the ÷ N portion of the synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0 – RA2
Reference Address Inputs (Pins 5, 6, 7)

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below.

Pull–up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	128
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	2410
1	1	1	8192

N0 – N11
N Counter Programming Inputs (Pins 11 – 20, 22 – 25)

These inputs provide the data that is preset into the ÷ N counter when it reaches the count of zero. N0 is the least significant and N13 is the most significant. Pull–up resistors ensure that inputs left open remain at a logic 1 and require only an SPST switch to alter data to the zero state.

T/R
Transmit/Receive Offset Adder Input (Pin 21)

This input controls the offset added to the data provided at the N inputs. This is normally used for offsetting the VCO frequency by an amount equal to the IF frequency of the transceiver. This offset is fixed at 856 when T/R is low and gives no offset when T/R is high. A pull–up resistor ensures that no connection will appear as a logic 1 causing no offset addition.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Phase Detector A Output (Pin 4)

Three–state output of phase detector for use as loop–error signal. Double–ended outputs are also available for this purpose (see ϕ_V and ϕ_R).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕR, ϕV
Phase Detector B Outputs (Pins 8, 9)

These phase detector outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_V
N Counter Output (Pin 10)

This is the buffered output of the ÷ N counter that is internally connected to the phase detector input. With this output available, the ÷ N counter can be used independently.

LD
Lock Detector Output (Pin 28)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 2)

The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS

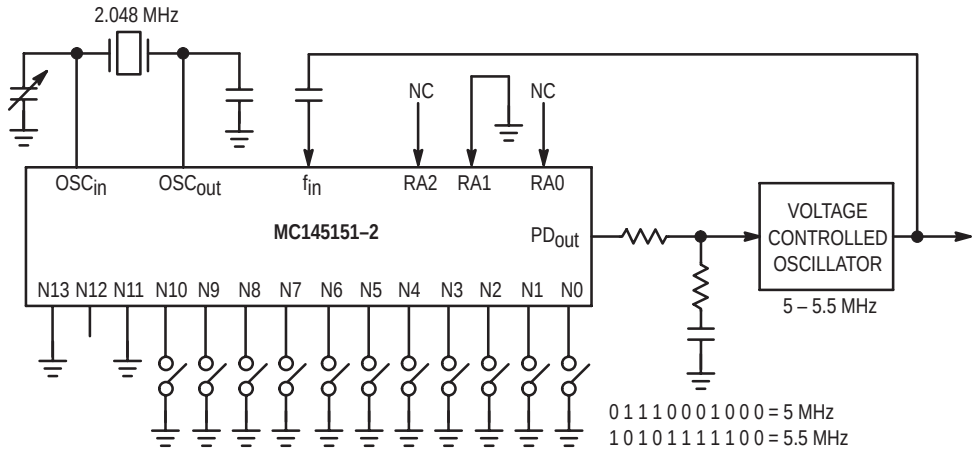
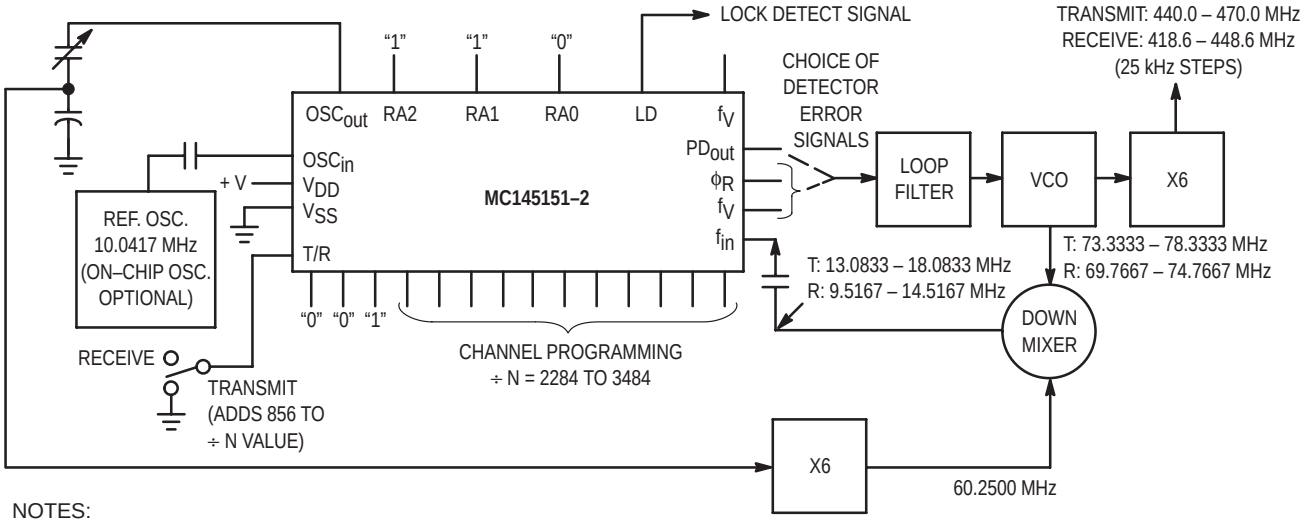


Figure 1. 5 MHz to 5.5 MHz Local Oscillator Channel Spacing = 1 kHz



NOTES:
1. f_R = 4.1667 kHz; ÷ R = 2410; 21.4 MHz low side injection during receive.
2. Frequency values shown are for the 440 – 470 MHz band. Similar implementation applies to the 406 – 440 MHz band. For 470 – 512 MHz, consider reference oscillator frequency X9 for mixer injection signal (90.3750 MHz).

Figure 2. Synthesizer for Land Mobile Radio UHF Bands

MC145151–2 Data Sheet Continued on Page 4.2–118

MC145152-2

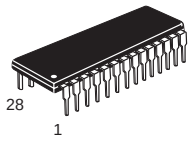
Parallel-Input PLL Frequency Synthesizer

Interfaces with Dual–Modulus Prescalers

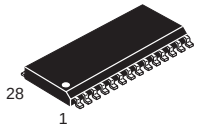
The MC145152–2 is programmed by sixteen parallel inputs for the N and A counters and three input lines for the R counter. The device features consist of a reference oscillator, selectable–reference divider, two–output phase detector, 10–bit programmable divide–by–N counter, and 6–bit programmable ÷ A counter.

The MC145152–2 is an improved–performance drop–in replacement for the MC145152–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- 8 User–Selectable ÷ R Values: 8, 64, 128, 256, 512, 1024, 1160, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 63
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates
- See Application Note AN980



P SUFFIX
PLASTIC DIP
CASE 710

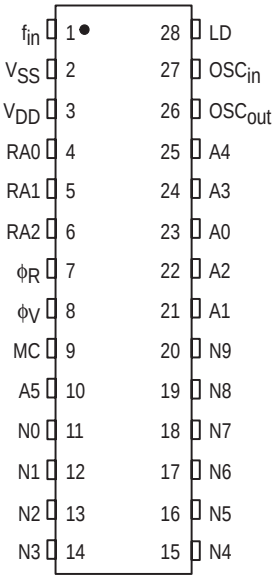


DW SUFFIX
SOG PACKAGE
CASE 751F

ORDERING INFORMATION

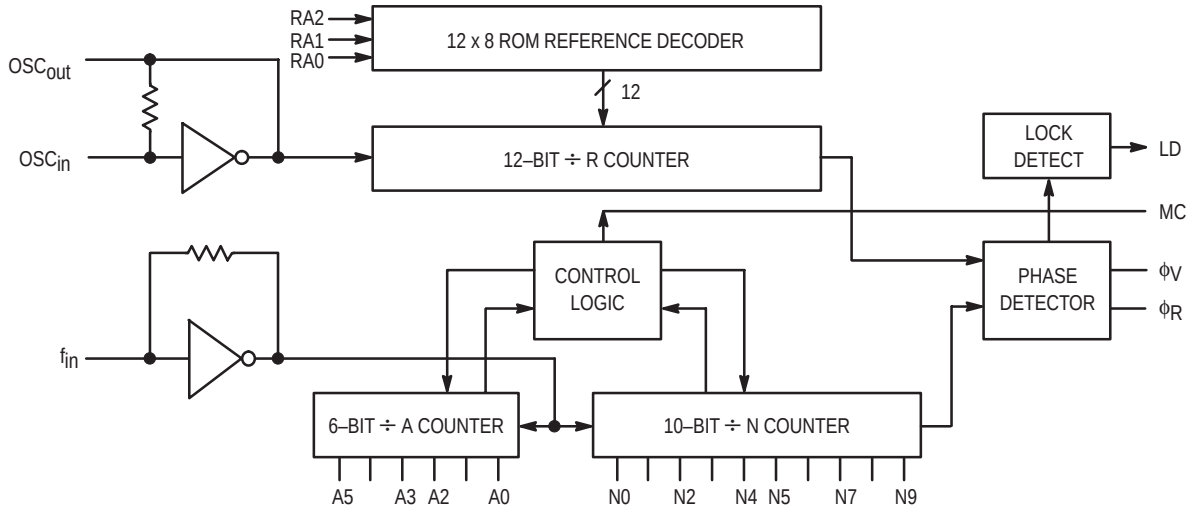
MC145152P2	Plastic DIP
MC145152DW2	SOG Package

PIN ASSIGNMENT



REV 1
8/95

MC145152–2 BLOCK DIAGRAM



NOTE: N0 – N9, A0 – A5, and RA0 – RA2 have pull–up resistors that are not shown.

PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 1)

Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual–modulus prescaler and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0, RA1, RA2
Reference Address Inputs (Pins 4, 5, 6)

These three inputs establish a code defining one of eight possible divide values for the total reference divider. The total reference divide values are as follows:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

N0 – N9
N Counter Programming Inputs (Pins 11 – 20)

The N inputs provide the data that is preset into the ÷ N counter when it reaches the count of 0. N0 is the least significant digit and N9 is the most significant. Pull–up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

A0 – A5
A Counter Programming Inputs
(Pins 23, 21, 22, 24, 25, 10)

The A inputs define the number of clock cycles of f_{in} that require a logic 0 on the MC output (see **Dual–Modulus Prescaling** section). The A inputs all have internal pull–up resistors that ensure that inputs left open will remain at a logic 1.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

ϕ_R, ϕ_V
Phase Detector B Outputs (Pins 7, 8)

These phase detector outputs can be combined externally for a loop–error signal.

If the frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

MC
Dual–Modulus Prescale Control Output (Pin 9)

Signal generated by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The MC level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first

portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low MC levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

LD
Lock Detector Output (Pin 28)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY

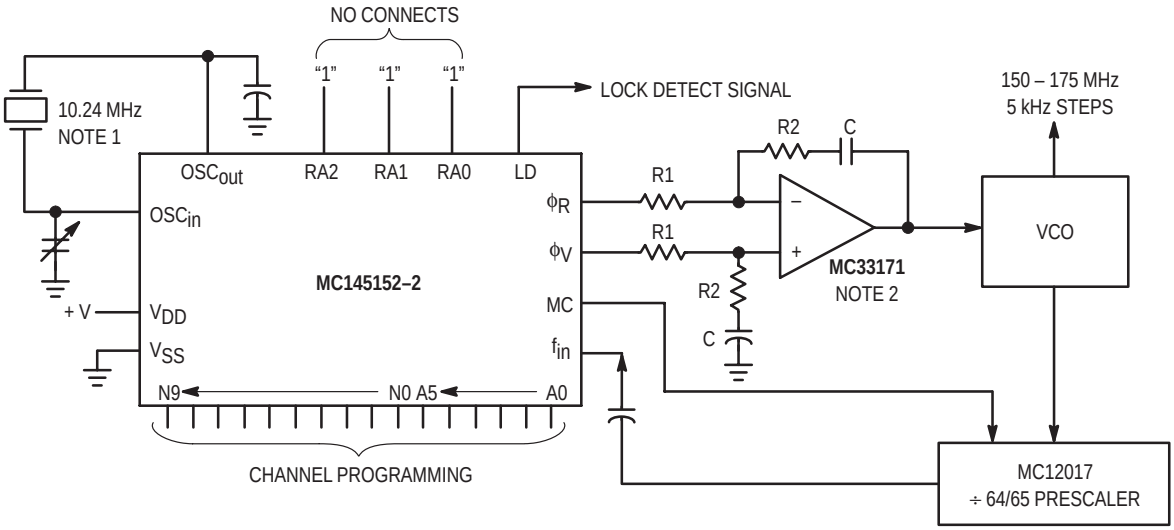
V_{DD}
Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 2)

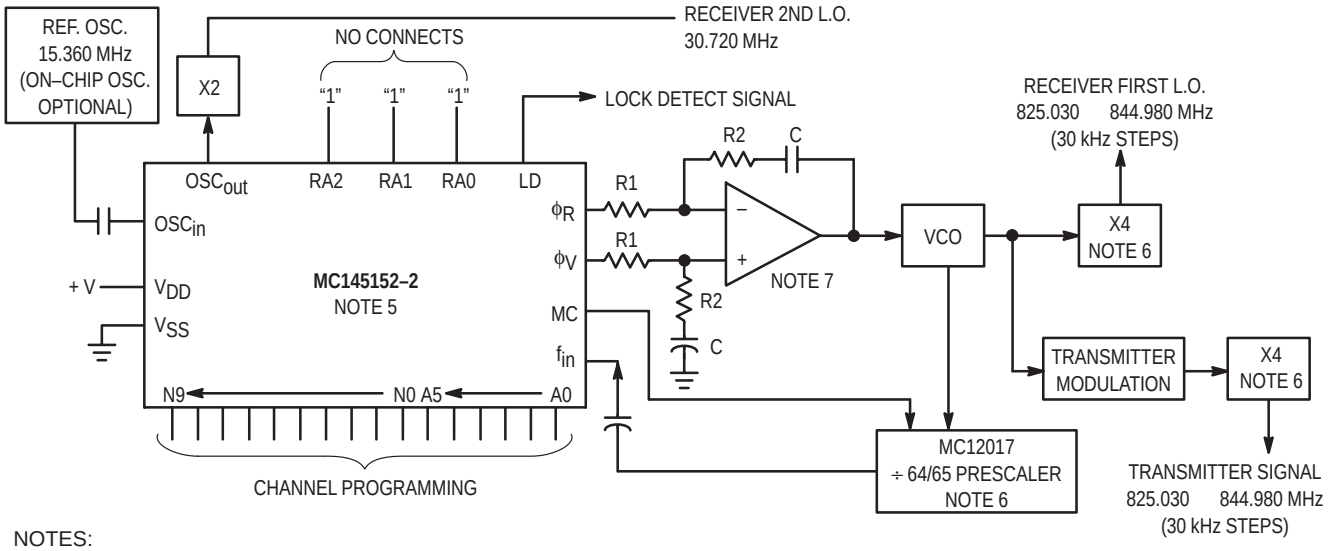
The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



NOTES:
1. Off–chip oscillator optional.
2. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 1. Synthesizer for Land Mobile Radio VHF Bands



NOTES:

1. Receiver 1st I.F. = 45 MHz, low side injection; Receiver 2nd I.F. = 11.7 MHz, low side injection.
2. Duplex operation with 45 MHz receiver/transmit separation.
3. f_R = 7.5 kHz; ÷ R = 2048.
4. N_{total} = N • 64 + A = 27501 to 28166; N = 429 to 440; A = 0 to 63.
5. MC145158–2 may be used where serial data entry is desired.
6. High frequency prescalers (e.g., MC12018 [520 MHz] and MC12022 [1 GHz]) may be used for higher frequency VCO and f_{ref} implementations.
7. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 2. 666–Channel, Computer–Controlled, Mobile Radiotelephone Synthesizer for 800 MHz Cellular Radio Systems

MC145152–2 Data Sheet Continued on Page 4.2–118

MC145157-2

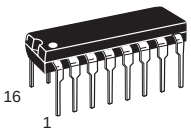
Serial-Input PLL Frequency Synthesizer

Interfaces with Single–Modulus Prescalers

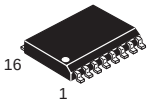
The MC145157–2 has a fully programmable 14–bit reference counter, as well as a fully programmable ÷ N counter. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

The MC145157–2 is an improved–performance drop–in replacement for the MC145157–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 16383
- f_V and f_R Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- “Linearized” Digital Phase Detector
- Single–Ended (Three–State) or Double–Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 648

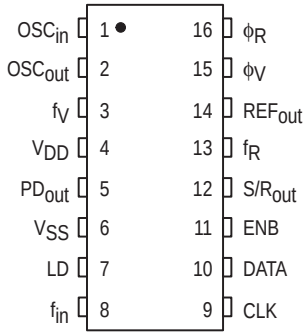


DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

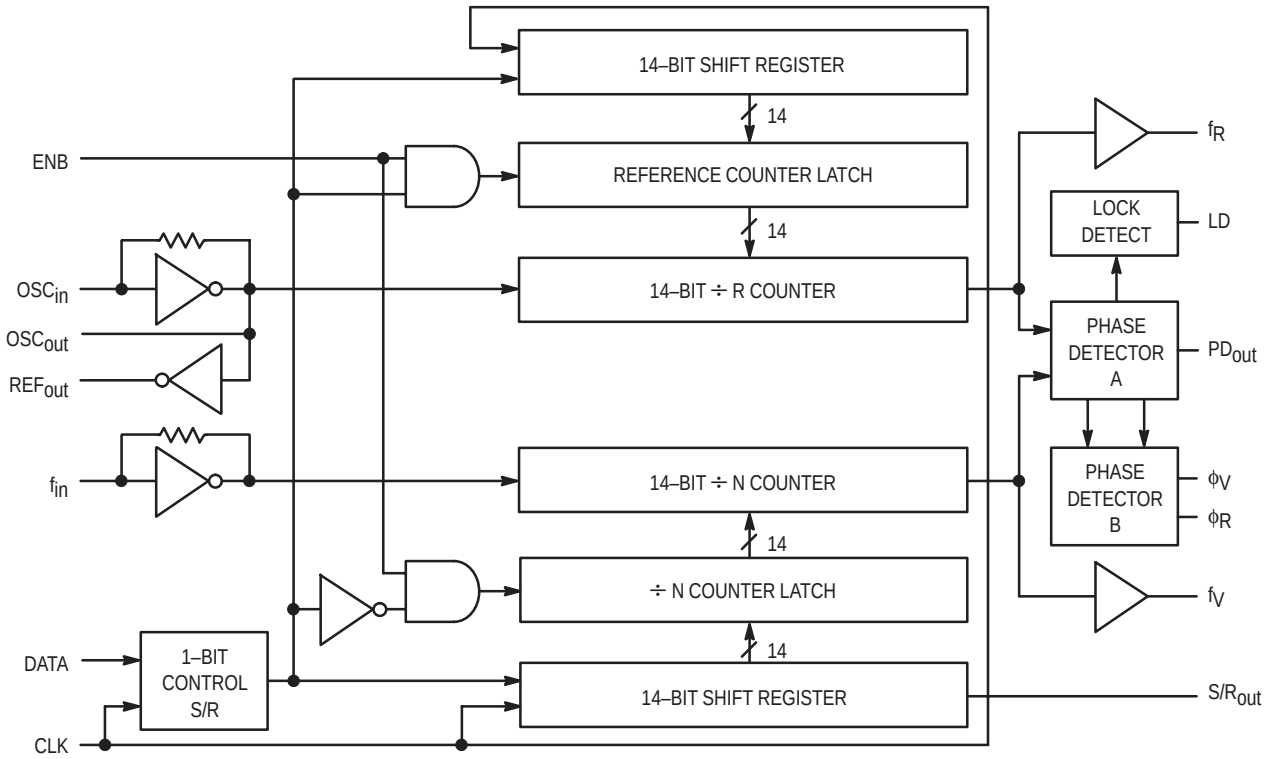
MC145157P2	Plastic DIP
MC145157DW2	SOG Package

PIN ASSIGNMENT



REV 1
8/95

MC145157–2 BLOCK DIAGRAM



PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 8)

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ N counter. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mV p–p. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

CLK, DATA
Shift Clock, Serial Data Inputs (Pins 9, 10)

Each low–to–high transition of the clock shifts one bit of data into the on–chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic 1 selects the reference counter latch and a logic 0 selects the ÷ N counter latch. The entry format is as follows:



ENB
Latch Enable Input (Pin 11)

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Single–Ended Phase Detector A Output (Pin 5)

This single–ended (three–state) phase detector output produces a loop–error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕR, ϕV
Double–Ended Phase Detector B Outputs (Pins 16, 15)

These outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_R, f_V
R Counter Output, N Counter Output (Pins 13, 3)

Buffered, divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

LD
Lock Detector Output (Pin 7)

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

REF_{out}
Buffered Reference Oscillator Output (Pin 14)

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

S/R_{out}
Shift Register Output (Pin 12)

This output can be connected to an external shift register to provide band switching, control information, and counter programming code checking.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 4)

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 6)

The most negative supply potential. This pin is usually ground.

MC145157–2 Data Sheet Continued on Page 4.2–118

MC145158-2

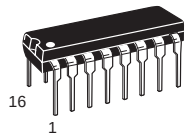
Serial-Input PLL Frequency Synthesizer

Interfaces with Dual–Modulus Prescalers

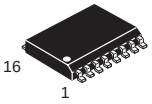
The MC145158–2 has a fully programmable 14–bit reference counter, as well as fully programmable ÷ N and ÷ A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

The MC145158–2 is an improved–performance drop–in replacement for the MC145158–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 1023
- Dual Modulus Capability; ÷ A Range = 0 to 127
- f_V and f_R Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- “Linearized” Digital Phase Detector
- Single–Ended (Three–State) or Double–Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 648

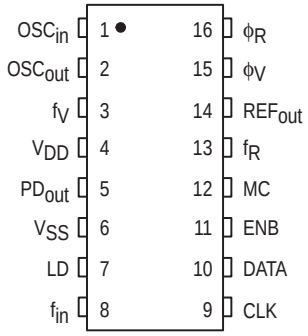


DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

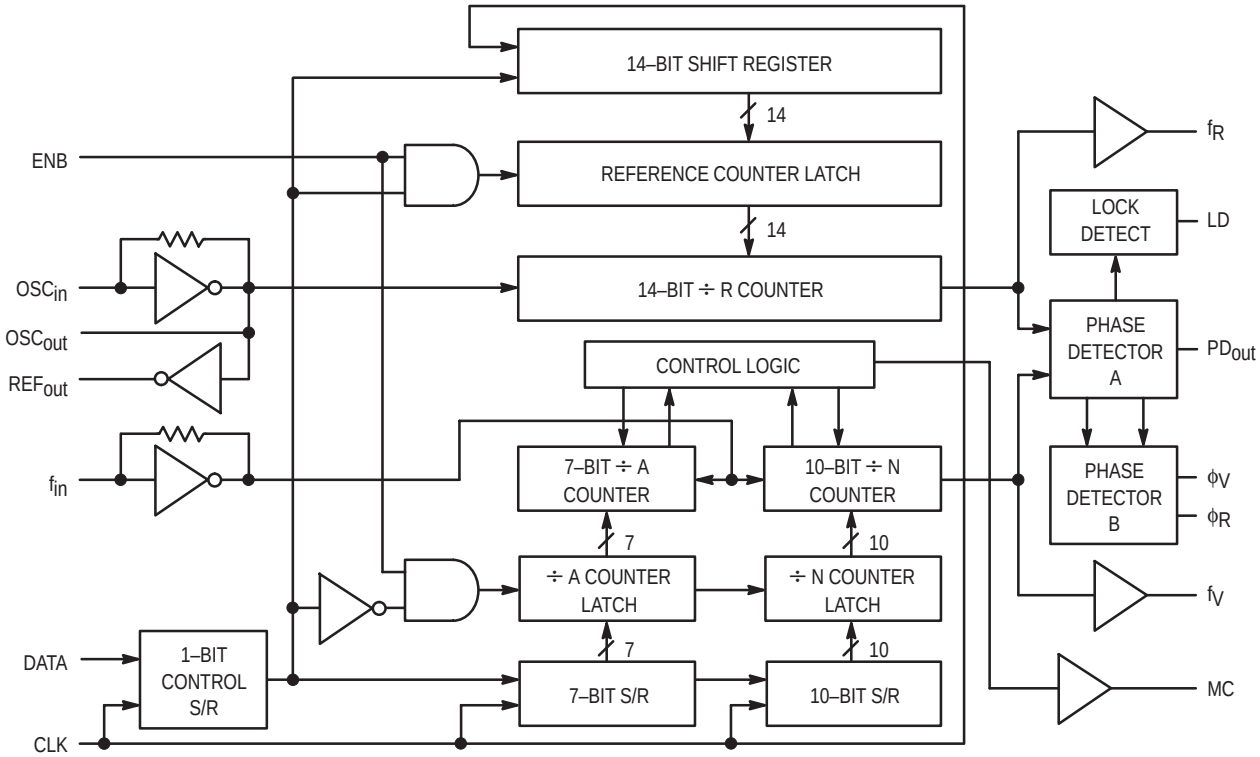
MC145158P2	Plastic DIP
MC145158DW2	SOG Package

PIN ASSIGNMENT



REV 1
8/95

MC145158–2 BLOCK DIAGRAM



PIN DESCRIPTIONS

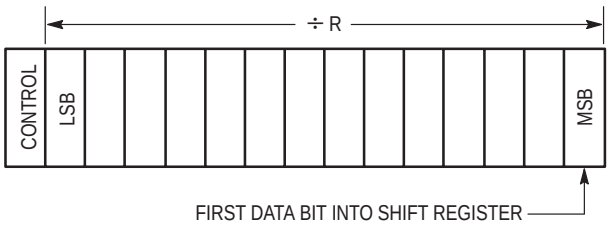
INPUT PINS

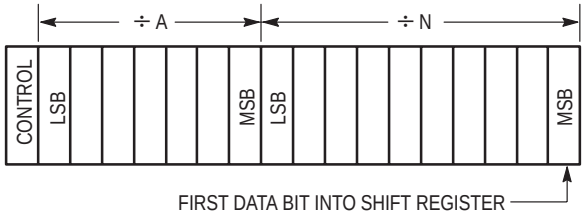
f_{in}
Frequency Input (Pin 8)

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ A and ÷ N counters. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mV p–p. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

CLK, DATA
Shift Clock, Serial Data Inputs (Pins 9, 10)

Each low–to–high transition of the CLK shifts one bit of data into the on–chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic 1 selects the reference counter latch and a logic 0 selects the ÷ A, ÷ N counter latch. The data entry format is as follows:





ENB
Latch Enable Input (Pin 11)

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N, ÷ A latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N, ÷ A latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Phase Detector A Output (Pin 5)

This single–ended (three–state) phase detector output produces a loop–error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕ_R, ϕ_V
Phase Detector B Outputs (Pins 16, 15)

Double–ended phase detector outputs. These outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

MC
Dual–Modulus Prescale Control Output (Pin 12)

This output generates a signal by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The MC level is low at the beginning of a count cycle and remains low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter. Note that when a prescaler is needed, the dual–modulus version offers a distinct advantage. The dual–modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter design.

f_R, f_V
R Counter Output, N Counter Output (Pins 13, 3)

Buffered, divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

LD
Lock Detector Output (Pin 7)

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

REF_{out}
Buffered Reference Oscillator Output (Pin 14)

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 4)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 6)

The most negative supply potential. This pin is usually ground.

MC14515X–2 FAMILY CHARACTERISTICS AND DESCRIPTIONS

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 10.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) except SW1, SW2	– 0.5 to V_{DD} + 0.5	V
V_{out}	Output Voltage (DC or Transient), SW1, SW2 ($R_{pull–up}$ = 4.7 kΩ)	– 0.5 to + 15	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

†Power Dissipation Temperature Derating:
Plastic DIP: – 12 mW/°C from 65 to 85°C
SOG Package: – 7 mW/°C from 65 to 85°C

These devices contain protection circuitry to protect against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high–impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ except for SW1 and SW2.

SW1 and SW2 can be tied through external resistors to voltages as high as 15 V, independent of the supply voltage.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pull–up devices. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	– 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage Range		—	3	9	3	9	3	9	V
I_{SS}	Dynamic Supply Current	f_{in} = OSC_{in} = 10 MHz, 1 V p–p ac coupled sine wave R = 128, A = 32, N = 128	3 5 9	— — —	3.5 10 30	— — —	3 7.5 24	— — —	3 7.5 24	mA
I_{SS}	Quiescent Supply Current (not including pull–up current component)	V_{in} = V_{DD} or V_{SS} I_{out} = 0 µA	3 5 9	— — —	800 1200 1600	— — —	800 1200 1600	— — —	1600 2400 3200	µA
V_{in}	Input Voltage — f_{in}, OSC_{in}	Input ac coupled sine wave	—	500	—	500	—	500	—	mV p–p
V_{IL}	Low–Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \ge 2.1$ V Input dc coupled $V_{out} \ge 3.5$ V square wave $V_{out} \ge 6.3$ V	3 5 9	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	V
V_{IH}	High–Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \le 0.9$ V Input dc coupled $V_{out} \le 1.5$ V square wave $V_{out} \le 2.7$ V	3 5 9	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	V
V_{IL}	Low–Level Input Voltage — except f_{in}, OSC_{in}		3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{IH}	High–Level Input Voltage — except f_{in}, OSC_{in}		3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
I_{in}	Input Current (f_{in}, OSC_{in})	V_{in} = V_{DD} or V_{SS}	9	± 2	± 50	± 2	± 25	± 2	± 22	µA
I_{IL}	Input Leakage Current (Data, CLK, ENB — without pull–ups)	V_{in} = V_{SS}	9	—	– 0.3	—	– 0.1	—	– 1.0	µA
I_{IH}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	V_{in} = V_{DD}	9	—	0.3	—	0.1	—	1.0	µA

(continued)

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	V_{DD} V	– 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
I_{IL}	Pull–up Current (all inputs with pull–ups)	$V_{in} = V_{SS}$	9	– 20	– 400	– 20	– 200	– 20	– 170	μA
C_{in}	Input Capacitance		—	—	10	—	10	—	10	pF
V_{OL}	Low–Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ μA $V_{in} = V_{DD}$	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{OH}	High–Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ μA $V_{in} = V_{SS}$	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
V_{OL}	Low–Level Output Voltage — Other Outputs	$I_{out} \approx 0$ μA	3 5 9	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}	High–Level Output Voltage — Other Outputs	$I_{out} \approx 0$ μA	3 5 9	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	V
$V_{(BR)DSS}$	Drain–to–Source Breakdown Voltage — SW1, SW2	$R_{pull–up} = 4.7$ kΩ	—	15	—	15	—	15	—	V
I_{OL}	Low–Level Sinking Current — MC	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	1.30 1.90 3.80	— — —	1.10 1.70 3.30	— — —	0.66 1.08 2.10	— — —	mA
I_{OH}	High–Level Sourcing Current — MC	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	– 0.60 – 0.90 – 1.50	— — —	– 0.50 – 0.75 – 1.25	— — —	– 0.30 – 0.50 – 0.80	— — —	mA
I_{OL}	Low–Level Sinking Current — LD	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.25 0.64 1.30	— — —	0.20 0.51 1.00	— — —	0.15 0.36 0.70	— — —	mA
I_{OH}	High–Level Sourcing Current — LD	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	– 0.25 – 0.64 – 1.30	— — —	– 0.20 – 0.51 – 1.00	— — —	– 0.15 – 0.36 – 0.70	— — —	mA
I_{OL}	Low–Level Sinking Current — SW1, SW2	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.80 1.50 3.50	— — —	0.48 0.90 2.10	— — —	0.24 0.45 1.05	— — —	mA
I_{OL}	Low–Level Sinking Current — Other Outputs	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.44 0.64 1.30	— — —	0.35 0.51 1.00	— — —	0.22 0.36 0.70	— — —	mA
I_{OH}	High–Level Sourcing Current — Other Outputs	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	– 0.44 – 0.64 – 1.30	— — —	– 0.35 – 0.51 – 1.00	— — —	– 0.22 – 0.36 – 0.70	— — —	mA
I_{OZ}	Output Leakage Current — PD_{out}	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9	—	± 0.3	—	± 0.1	—	± 1.0	μA
I_{OZ}	Output Leakage Current — SW1, SW2	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9	—	± 0.3	—	± 0.1	—	± 3.0	μA
C_{out}	Output Capacitance — PD_{out}	PD_{out} — Three–State	—	—	10	—	10	—	10	pF

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit – 40 to 85°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, f_{in} to MC (Figures 1 and 4)	3 5 9	110 60 35	120 70 40	ns
t_{PHL}	Maximum Propagation Delay, ENB to SW1, SW2 (Figures 1 and 5)	3 5 9	160 80 50	180 95 60	ns
t_W	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V (Figures 2 and 4)	3 5 9	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}	Maximum Output Transition Time, MC (Figures 3 and 4)	3 5 9	115 60 40	115 75 60	ns
t_{THL}	Maximum Output Transition Time, MC (Figures 3 and 4)	3 5 9	60 34 30	70 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, LD (Figures 3 and 4)	3 5 9	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs (Figures 3 and 4)	3 5 9	160 80 60	175 100 65	ns

SWITCHING WAVEFORMS

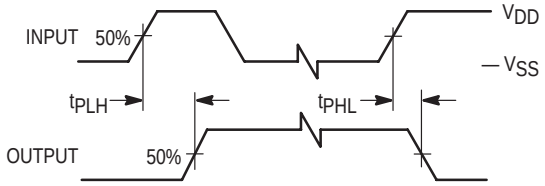
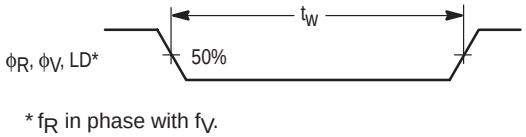


Figure 1.



* f_R in phase with f_V.

Figure 2.

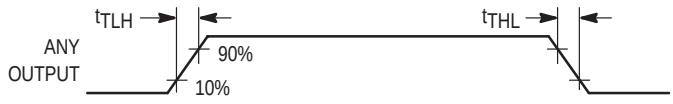
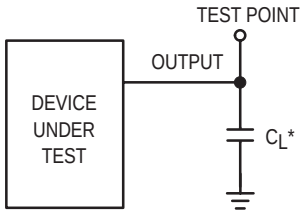
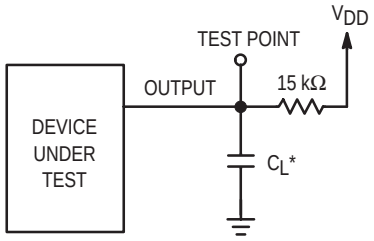


Figure 3.



* Includes all probe and fixture capacitance.

Figure 4. Test Circuit



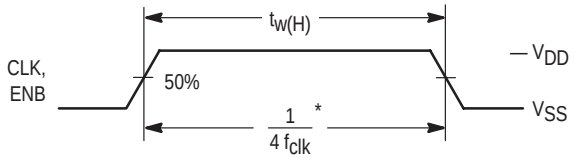
* Includes all probe and fixture capacitance.

Figure 5. Test Circuit

TIMING REQUIREMENTS (Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit – 40 to 85°C	Unit
f_{clk}	Serial Data Clock Frequency, Assuming 25% Duty Cycle NOTE: Refer to CLK $t_{w(H)}$ below (Figure 6)	3 5 9	dc to 5.0 dc to 7.1 dc to 10	dc to 3.5 dc to 7.1 dc to 10	MHz
t_{su}	Minimum Setup Time, Data to CLK (Figure 7)	3 5 9	30 20 18	30 20 18	ns
t_h	Minimum Hold Time, CLK to Data (Figure 7)	3 5 9	40 20 15	40 20 15	ns
t_{su}	Minimum Setup Time, CLK to ENB (Figure 7)	3 5 9	70 32 25	70 32 25	ns
t_{rec}	Minimum Recovery Time, ENB to CLK (Figure 7)	3 5 9	5 10 20	5 10 20	ns
$t_{w(H)}$	Minimum Pulse Width, CLK and ENB (Figure 6)	3 5 9	50 35 25	70 35 25	ns
t_r, t_f	Maximum Input Rise and Fall Times — Any Input (Figure 8)	3 5 9	5 4 2	5 4 2	µs

SWITCHING WAVEFORMS



*Assumes 25% Duty Cycle.

Figure 6.

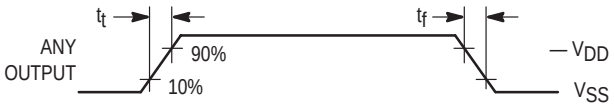


Figure 8.

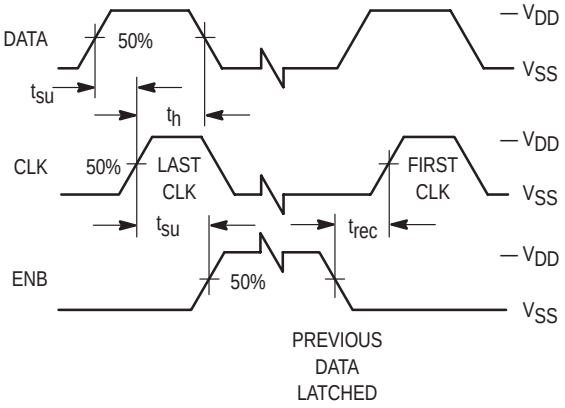
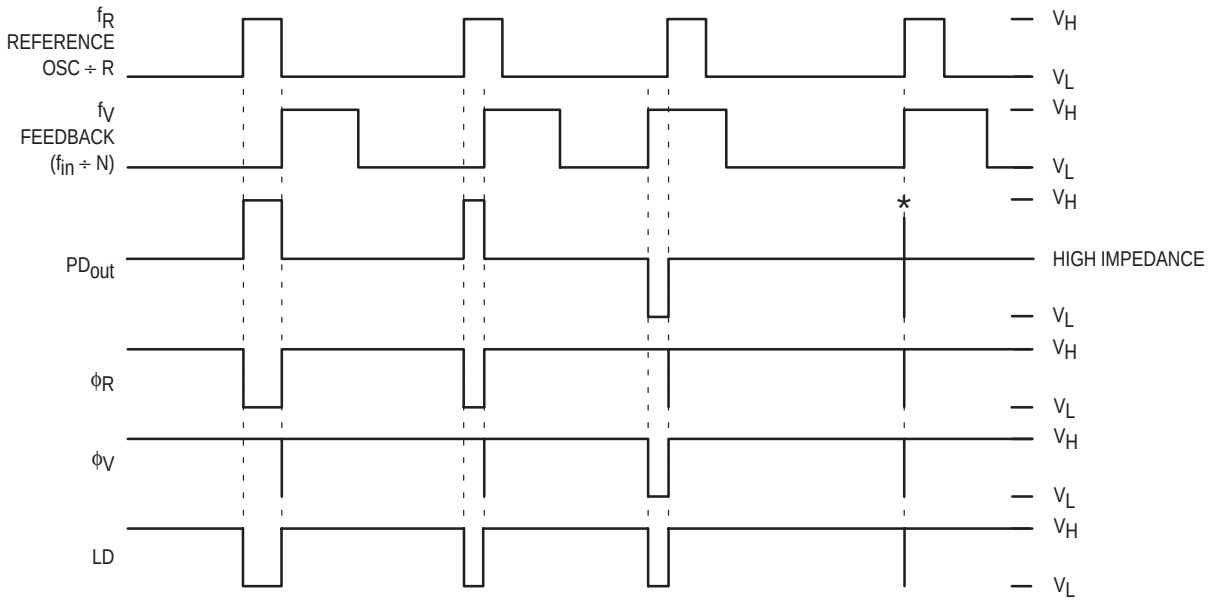


Figure 7.

FREQUENCY CHARACTERISTICS (Voltages References to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ =10 ns unless otherwise indicated)

Symbol	Parameter	Test Condition	V_{DD} V	– 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 500 mV p–p ac coupled sine wave	3 5 9	— — —	6 15 15	— — —	6 15 15	— — —	6 15 15	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 1 V p–p ac coupled sine wave	3 5 9	— — —	12 22 25	— — —	12 20 22	— — —	7 20 22	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 $V_{in} = V_{DD}$ to V_{SS} dc coupled square wave	3 5 9	— — —	13 25 25	— — —	12 22 25	— — —	8 22 25	MHz

NOTE: Usually, the PLL's propagation delay from f_{in} to MC plus the setup time of the prescaler determines the upper frequency limit of the system. The upper frequency limit is found with the following formula: $f = P / (t_P + t_{set})$ where f is the upper frequency in Hz, P is the lower of the dual modulus prescaler ratios, t_P is the f_{in} to MC propagation delay in seconds, and t_{set} is the prescaler setup time in seconds. For example, with a 5 V supply, the f_{in} to MC delay is 70 ns. If the MC12028A prescaler is used, the setup time is 16 ns. Thus, if the 64/65 ratio is utilized, the upper frequency limit is $f = P / (t_P + t_{set}) = 64/(70 + 16) = 744$ MHz.



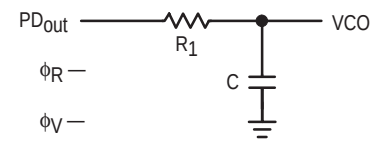
V_H = High Voltage Level.
V_L = Low Voltage Level.
* At this point, when both f_R and f_V are in phase, the output is forced to near mid–supply.
NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency the output is high and the voltage at this pin is determined by the low–pass filter capacitor.

Figure 9. Phase Detector/Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

A)

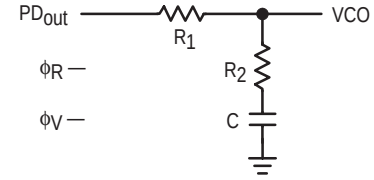


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

B)

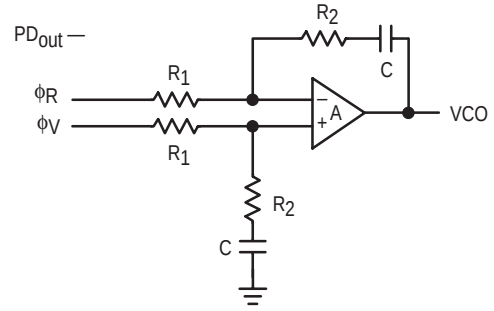


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE: Sometimes R_1 is split into two series resistors, each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:

N = Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) $\approx \frac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \cong 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct–coupled square wave having a rail–to–rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

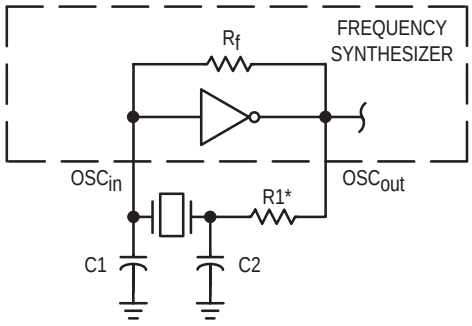
For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct–coupled square wave having rail–to–rail voltage swing.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 10.



* May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_o + \frac{C1 \cdot C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 11)
C_{out} = 6 pF (see Figure 11)
C_a = 1 pF (see Figure 11)
C_O = the crystal's holder capacitance (see Figure 12)
C1 and C2 = external capacitors (see Figure 10)

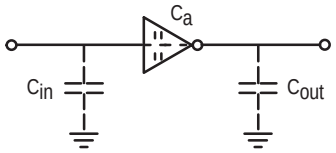
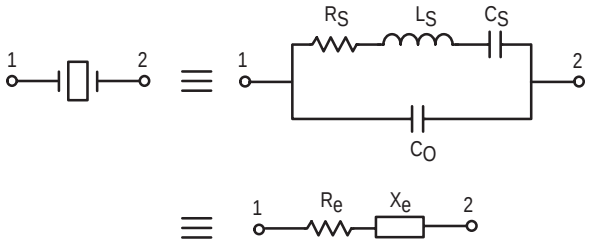


Figure 11. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure 10 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1 = 0 Ω).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 1).

Table 1. Partial List of Crystal Manufacturers

Motorola — Internet Address *http://motorola.com* (Search for resonators)
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

DUAL–MODULUS PRESCALING

OVERVIEW

The technique of dual–modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low–frequency programmable counters to be used as high–frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single–modulus) divider is used for the prescaler.

In dual–modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). Motorola's dual–modulus frequency synthesizers contain this feature and can be used with a variety of dual–modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷ 3/÷ 4 to ÷ 128/÷ 129 can be controlled by most Motorola frequency synthesizers.

Several dual–modulus prescaler approaches suitable for use with the MC145152–2, MC145156–2, or MC145158–2 are:

MC12009	÷ 5/÷ 6	440 MHz
MC12011	÷ 8/÷ 9	500 MHz
MC12013	÷ 10/÷ 11	500 MHz
MC12015	÷ 32/÷ 33	225 MHz
MC12016	÷ 40/÷ 41	225 MHz
MC12017	÷ 64/÷ 65	225 MHz
MC12018	÷ 128/÷ 129	520 MHz
MC12028A	÷ 32/33 or ÷ 64/65	1.1 GHz
MC12052A	÷ 64/65 or ÷ 128/129	1.1 GHz
MC12054A	÷ 64/65 or ÷ 128/129	2.0 GHz

DESIGN GUIDELINES

The system total divide value, N_{total} (N_T) will be dictated by the application:

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷ N counter, A is the number programmed into the ÷ A counter, P and P + 1 are the two selectable divide ratios available in the dual–modulus prescalers. To have a range of N_T values in sequence, the ÷ A counter is programmed from zero through P – 1 for a particular value N in the ÷ N counter. N is then incremented to N + 1 and the ÷ A is sequenced from 0 through P – 1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the ÷ N and ÷ A counters.

The constraint $N \geq A$ always applies. If $A_{max} = P - 1$, then $N_{min} \geq P - 1$. Then $N_{Tmin} = (P - 1)\ P + A$ or $(P - 1)\ P$ since A is free to assume the value of 0.

$$N_{Tmax} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual–modulus prescaler output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its MC is low.

For the maximum frequency into the prescaler (f_{VCOmax}), the value used for P must be large enough such that:

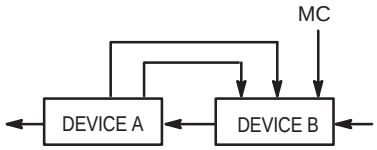
1. f_{VCOmax} divided by P may not exceed the frequency capability of f_{in} (input to the ÷ N and ÷ A counters).
2. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual–modulus prescaler.
   b. Prescaler setup or release time relative to its MC signal.
   c. Propagation time from f_{in} to the MC output for the frequency synthesizer device.

A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of N_T results when N_T in binary is used as the program code to the ÷ N and ÷ A counters treated in the following manner:

1. Assume the ÷ A counter contains "a" bits where $2^a \geq P$.
2. Always program all higher order ÷ A counter bits above "a" to 0.

3. Assume the ÷ N counter and the ÷ A counter (with all the higher order bits above “a” ignored) combined into a single binary counter of n + a bits in length (n = number of divider stages in the ÷ N counter). The MSB of this “hypothetical” counter is to correspond to the MSB of ÷ N and the LSB is to correspond to the LSB of ÷ A. The system divide value, N_T, now results when the value of N_T in binary is used to program the “new” n + a bit counter.

By using the two devices, several dual–modulus values are achievable (shown in Figure 13).



DEVICE A \ DEVICE B	MC12009	MC12011	MC12013
MC10131	÷ 20/÷ 21	÷ 32/÷ 33	÷ 40/÷ 41
MC10138	÷ 50/÷ 51	÷ 80/÷ 81	÷ 100/÷ 101

NOTE: MC12009, MC12011, and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

Figure 13. Dual–Modulus Values

MC145162
MC145162-1

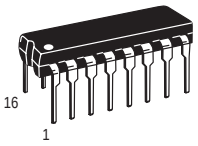
60 MHz and 85 MHz Universal Programmable Dual PLL Frequency Synthesizers
CMOS

The MC145162 is a dual phase–locked loop (PLL) frequency synthesizer especially designed for CT–1 cordless phone applications worldwide. This frequency synthesizer is also for any product with a frequency operation at 60 MHz or below.

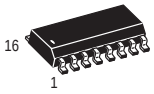
The MC145162–1 is a high frequency derivative of the MC145162, for products with operating frequencies of 85 MHz or below.

The device features fully programmable receive, transmit, reference, and auxiliary reference counters accessed through an MCU serial interface. This feature allows this device to operate in any CT–1 cordless phone application. The device consists of two independent phase detectors for transmit and receive loops. A common reference oscillator, driving two independent reference frequency counters, provides independent reference frequencies for transmit and receive loops. The auxiliary reference counter allows the user to select an additional reference frequency for receive and transmit loops if required.

- Operating Voltage Range: 2.5 to 5.5 V
- Operating Temperature Range: – 40 to + 75°C
- Operating Power Consumption: 3.0 mA @ 2.5 V
- Maximum Operating Frequency:
  MC145162 — 60 MHz @ 200 mV p–p, V_{DD} = 2.5 V
  MC145162–1 — 85 MHz @ 250 mV p–p, V_{DD} = 2.5 V
- Three or Four Pins Used for Serial MCU Interface
- Built–In MCU Clock Output with Frequency of Reference Oscillator ÷3/÷4
- Power Saving Mode Controlled by MCU
- Lock Detect Signal
- On–Chip Reference Oscillator Supports External Crystals to 16.0 MHz
- Reference Frequency Counter Division Range: 16 to 4095
- Auxiliary Reference Frequency Counter Division Range: 16 to 16,383
- Transmit Counter Division Range: 16 to 65,535
- Receive Counter Division Range: 16 to 65,535



P SUFFIX
PLASTIC DIP
CASE 648

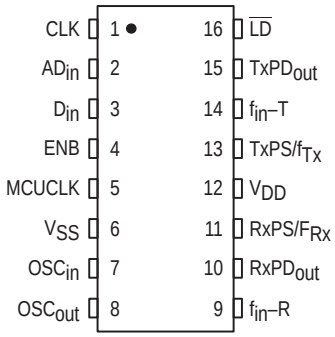


D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

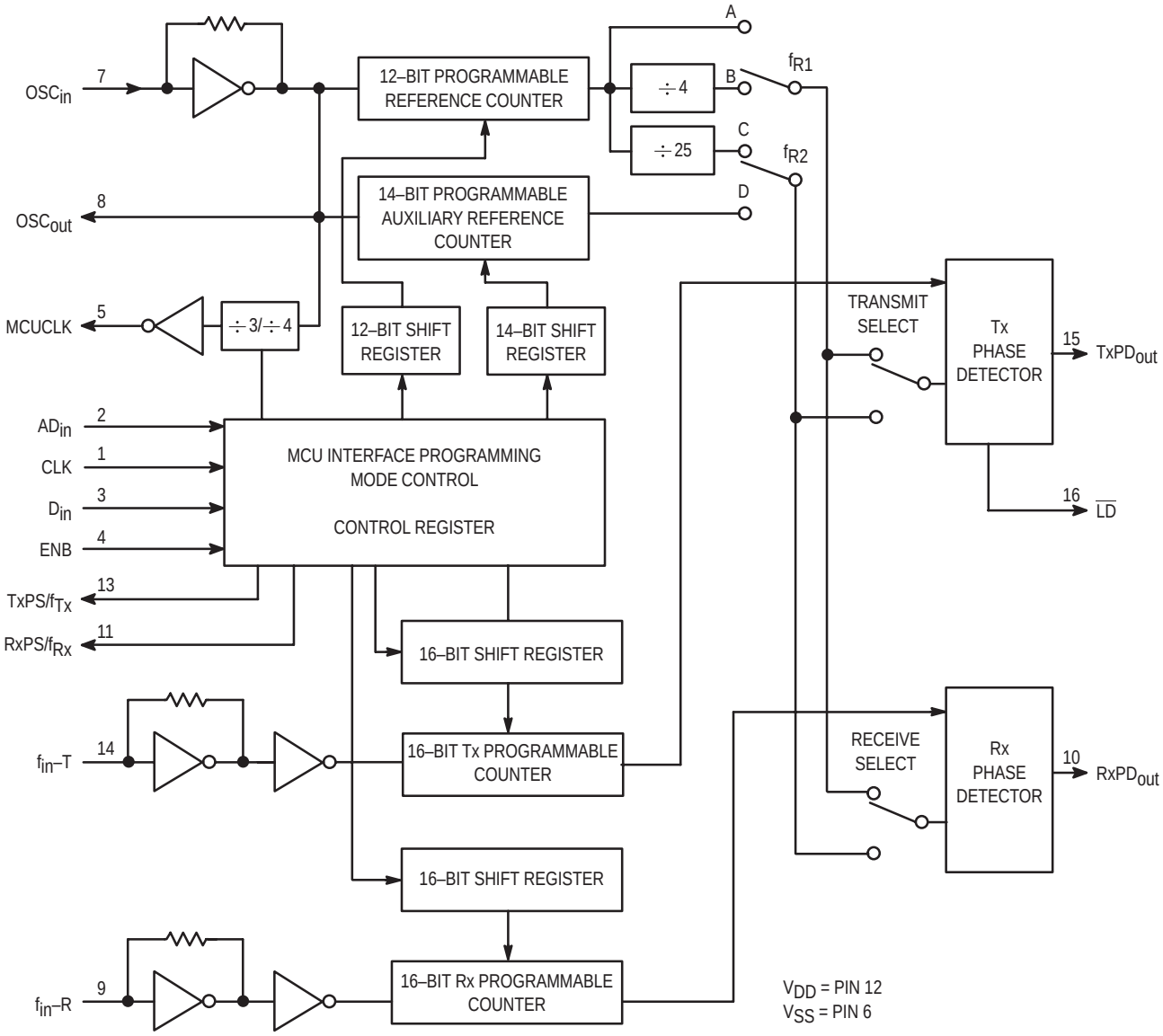
MC145162P	Plastic DIP
MC145162D	SOG Package
MC145162P1	Plastic DIP
MC145162D1	SOG Package

PIN ASSIGNMENT



REV 3.1
2/98

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 6.0	V
V_{in}	Input Voltage, All Inputs	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	DC Current Drain Per Pin	10	mA
I_{DD}, I_{SS}	DC Current Drain V_{DD} or V_{SS} Pins	30	mA
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused pins must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 25°C)

Symbol	Characteristic	V_{DD}	Guaranteed Limit		Unit
			Min	Max	
V_{DD}	Power Supply Voltage Range	—	2.5	5.5	V
V_{OL}	Output Voltage (I_{out} = 0) 0 Level	2.5 5.5	— —	0.1 0.1	V
V_{OH}	(V_{in} = V_{DD} or 0) 1 Level	2.5 5.5	2.45 5.45	— —	
V_{IL}	Input Voltage (V_{out} = 0.5 V or V_{DD} – 0.5 V) 0 Level	2.5 5.5	— —	0.75 1.65	V
V_{IH}	1 Level	2.5 5.5	1.75 3.85	— —	
I_{OH}	Output Current (V_{out} = 2.2 V) (V_{out} = 5.0 V) Source	2.5 5.5	– 0.18 – 0.55	— —	mA
I_{OL}	(V_{out} = 0.3 V) (V_{out} = 0.5 V) Sink	2.5 5.5	0.18 0.55	— —	
I_{IL}	Input Current (V_{in} = 0) OSC_{in}, f_{in}–T, f_{in}–R	2.5 5.5	— —	– 30 – 66	μA
	AD_{in}, CLK, D_{in}, ENB	2.5 5.5	— —	– 1.0 – 1.0	
I_{IH}	(V_{in} = V_{DD} – 0.5) OSC_{in}, f_{in}–T, f_{in}–R	2.5 5.5	— —	30 66	
	AD_{in}, CLK, D_{in}, ENB	2.5 5.5	— —	5.0 5.0	
I_{OZ}	Three–State Leakage Current (V_{out} = 0 V or 5.5 V)	5.5	—	± 100	nA
C_{in}	Input Capacitance	—	—	8.0	pF
C_{out}	Output Capacitance	—	—	8.0	pF
$I_{DD(stdby)}$	Standby Current (All Counters are in Power–Down Mode with Oscillator On)	2.5 5.5	— —	0.3 1.5	mA
I_{DD}	Operating Current MC145162: 200 mV p–p input at f_{in}–T and f_{in}–R = 60 MHz MC145162–1: 250 mV p–p input at f_{in}–T and f_{in}–R = 85 MHz with OSC = 10.24 MHz	2.5 5.5	— —	3.0 10	mA

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Symbol	Characteristic		Figure No.	V_{DD}	Guaranteed Limit		Unit
					Min	Max	
t_{TLH}	Output Rise Time		1	2.5 5.5	— —	200 100	ns
t_{THL}	Output Fall Time		1	2.5 5.5	— —	200 100	ns
t_r, t_f	Input Rise and Fall Time	OSC_{in}	2	2.5 5.5	— —	5.0 4.0	µs
t_w	Input Pulse Width	CLK and ENB	3	2.5 5.5	80 60	— —	ns
f_{max}	Input Frequency Input = Sine Wave @ ≥ 200 mV p–p for MC145162 Input = Sine Wave @ ≥ 250 mV p–p for MC145162–1	OSC_{in} f_{in}–R, f_{in}–T f_{in}–R, f_{in}–T		2.5 – 5.5 2.5 – 5.5 2.5 – 5.5	— — —	16 60 85	MHz
t_{st}	Minimum Start–Up Time					10	ms
t_{su}	Setup Time	DATA to CLK ENB to CLK	5	2.5 5.5	100 200	— —	ns
t_h	Hold Time	CLK to DATA	5	3.0 5.0	80 40	— —	ns
t_{rec}	Recovery Time	ENB to CLK	5	3.0 5.0	80 40	— —	ns
t_{su1}	Setup Time	ENB to CLK	4	2.5 – 5.5	80	—	ns
t_{h1}	Hold Time	CLK to ENB	4	2.5 – 5.5	600	—	ns
f	Phase Detector Frequency				dc	12.5	kHz
f_{MCUCLK}	Output Clock Frequency (OSC_{in} ÷ 3)	MCUCLK			dc	5.33	MHz

SWITCHING WAVEFORMS

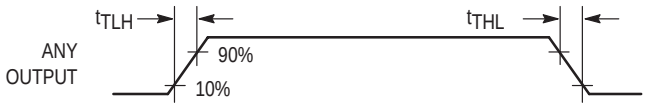


Figure 1.

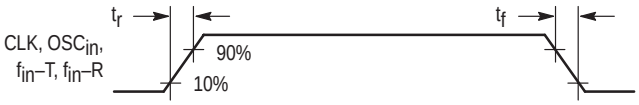


Figure 2.

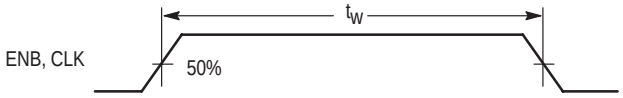


Figure 3.

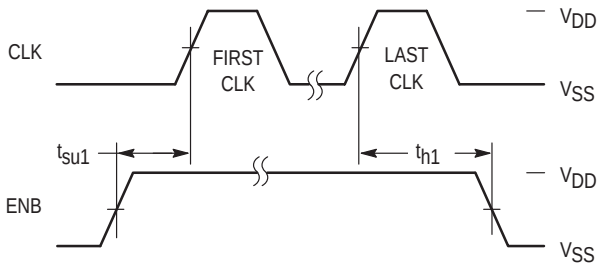


Figure 4. ENB High During Serial Transfer

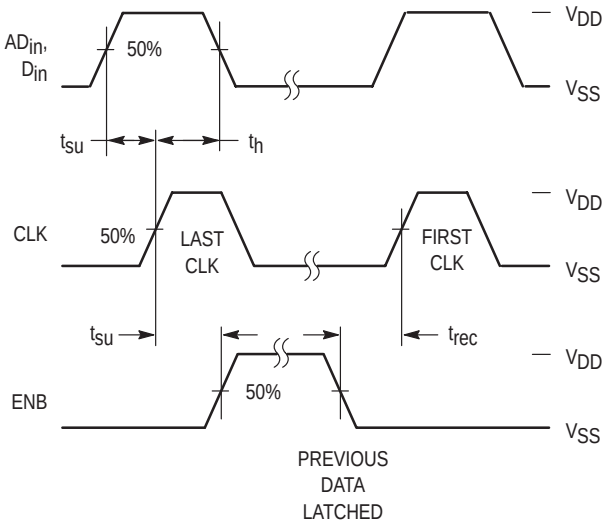


Figure 5. ENB Low During Serial Transfer

PIN DESCRIPTIONS

INPUT PINS

OSC_{in} /OSC_{out}
Reference Oscillator Input/Output (Pins 7, 8)

These pins form a reference oscillator when connected to an external parallel–resonant crystal. Figure 6 shows the relationship of different crystal frequencies and reference frequencies for cordless phone applications in various countries. OSC_{in} may also serve as input for an externally generated reference signal which is typically ac coupled.

MCUCLK
System Clock (Pin 5)

This output pin provides a signal of the crystal frequency (OSC_{out}) divided by 3 or 4 that is controlled by a bit in the control register.

This signal can be a clock source for the MCU or other system clocks.

AD_{in}, D_{in}, CLK, ENB
Auxiliary Data In, Data In, Clock, Enable (Pins 2, 3, 1, 4)

These four pins provide an MCU serial interface for programming the reference counter, the transmit–channel counter, and the receive–channel counter. They also provide various controls of the PLL including the power saving mode and the programming format.

TxPS/f_{Tx}, RxPS/f_{Rx}
Transmit Power Save, Receive Power Save (Pins 13, 11)

For a normal application, these output pins provide the status of the internal power saving mode operation. If the transmit–channels counter circuitry is in power down mode, TxPS/f_{Tx} outputs a high state. If the receive–channels counter circuitry is in power down mode, RxPS/f_{Rx} is set high. These outputs can be applied for controlling the external power switch for the transmitter and the receiver to save MCU control pins.

In the Tx/Rx channel counter test mode, the TxPS/f_{Tx} and RxPS/f_{Rx} pins output the divided value of the transmit channel counter (f_{Tx}) and the receive channel counter (f_{Rx}), respectively. This test mode operation is controlled by the control register. Details of the counter test mode are in the **Tx/Rx Channel Counter Test** section of this data sheet.

f_{in}–T/f_{in}–R
Transmit/Receive Counter Inputs (Pins 14, 9)

f_{in}–T and f_{in}–R are inputs to the transmit and the receive counters, respectively. These signals are typically driven from the loop VCO and ac coupled. The minimum input signal level is 200 mV p–p @ 60.0 MHz.

OUTPUT PINS

$TxPD_{out}$/$RxPD_{out}$
Transmit/Receive Phase Detector Outputs (Pins 15, 10)

These are three–state outputs of the transmit and receive phase detectors for use as loop error signals (see Figure 7 for phase detector output waveforms). Phase detector gain is $V_{DD}/4\ \pi$ volts per radian.

Frequency $f_V > f_R$ or f_V leading: output = negative pulse.
Frequency $f_V < f_R$ or f_V lagging: output = positive pulse.
Frequency $f_V = f_R$ and phase coincidence: output = high–impedance state.
NOTE: f_R is the divided–down reference frequency at the phase detector input and f_V is the divided–down VCO frequency at the phase detector input.

$\overline{LD}$
Lock Detect (Pin 16)

The lock detect signal is associated with the transmit loop. The output at a high level indicates an out–of–lock condition (see Figure 7 for the $\overline{LD}$ output waveform).

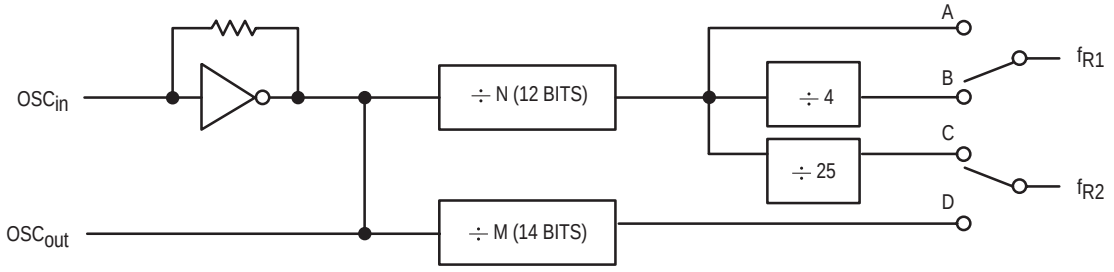
POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 12)

V_{DD} is the most positive power supply potential ranging from 2.5 to 5.5 V with respect to V_{SS}.

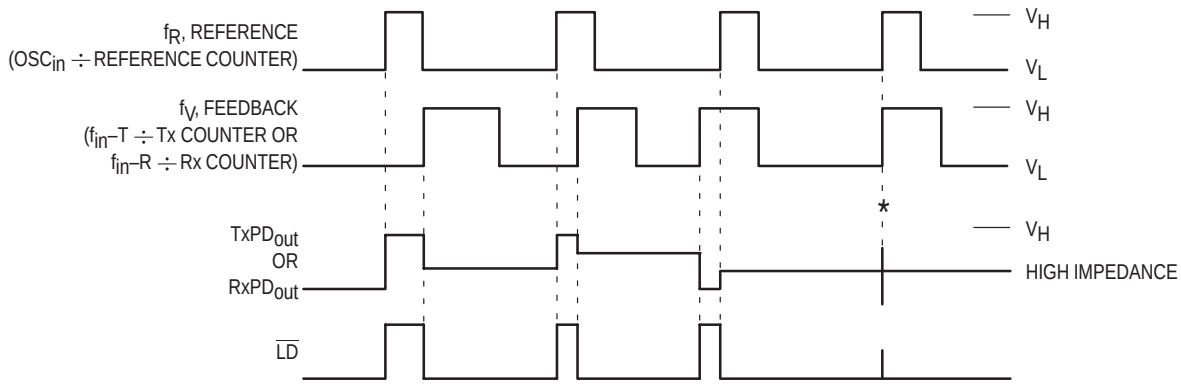
V_{SS}
Negative Power Supply (Pin 6)

V_{SS} is the most negative supply potential and is usually connected to ground.



Crystal	÷ N Value	f_{R1} B	f_{R2} C
11.150 MHz	446	6.25 kHz	1.0 kHz
11.150 MHz	223	12.5 kHz	
10.240 MHz	512	5.0 kHz	
12.000 MHz	600	5.0 kHz	

Figure 6. Reference Frequencies for Cordless Phone Applications of Various Countries



V_H = High voltage level.
V_L = Low voltage level.
*At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.

NOTE: The $TxPD_{out}$ and $RxPD_{out}$ generate error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.

Figure 7. Phase Detector/Lock Detector Output Waveforms

MCU PROGRAMMING SCHEME

The MCU programming scheme is defined in two formats controlled by the ENB input. If the enable signal is high during the serial data transfer, control register/reference frequency programming is selected. If the ENB is low, programming of the transmit and receive counters is selected. During programming of the transmit and receive counters, both AD_{in} and D_{in} pins can input the data to the transmit and receive counters. Both counters' data is clocked into the PLL internal shift register at the leading edge of the CLK signal. It is not necessary to reprogram the reference frequency counter/control register when using the enable signal to program the transmit/receive channels.

In programming the control register/reference frequency scheme, the most significant bit (MSB) of the programming word identifies whether the input data is the control word or the reference frequency data word. If the MSB is 1, the input data is the control word (Figure 8). Also see Figure 8 and Table 1 for control register and bit function. If the MSB is 0, the input data is the reference frequency (Figure 9).

The reference frequency data word is a 32–bit word containing the 12–bit reference frequency data, the 14–bit auxiliary reference frequency counter information, the reference frequency selection plus, the auxiliary reference frequency counter enable bit (Figure 9).

If the AUX REF ENB bit is high, the 14–bit auxiliary reference frequency counter provides an additional phase reference frequency output for the loops. If AUX REF ENB bit is low, the auxiliary reference frequency counter is forced into power–down mode for current saving. (Other power down modes are also provided through the control register per Table 2 and Figure 8.) At the falling edge of the ENB signal, the data is stored in the registers.

There are two interfacing schemes for the universal channel mode: the three–pin and the four–pin interfacing schemes. The three–pin interfacing scheme is suited for use with the MCU SPI (serial peripheral interface) (Figure 10), while the four–pin interfacing scheme is commonly used for general I/O port connection (Figure 11).

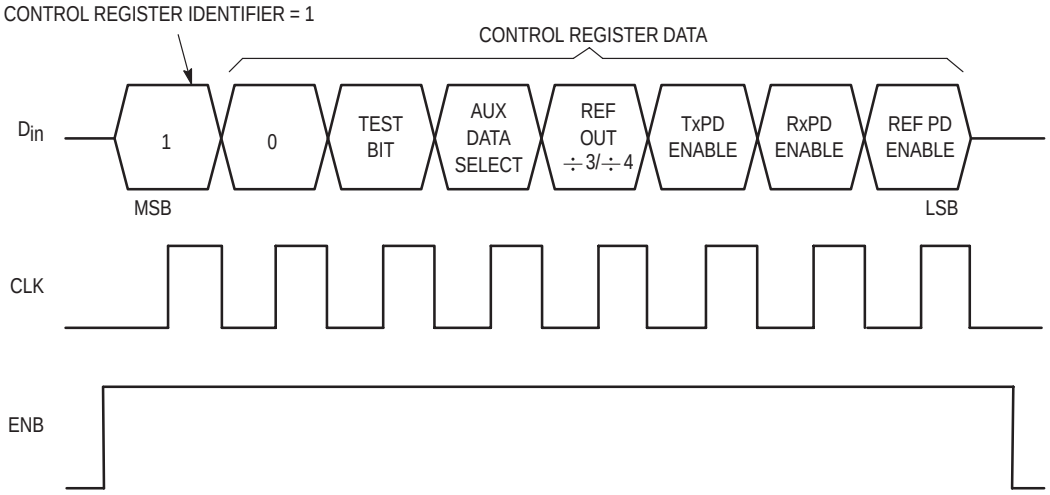
For the three–pin interfacing scheme, the auxiliary data select bit is set to 0. All 32 bits of data, which define both the 16–bit transmit counter and the 16–bit receive counter, latch into the PLL internal register through the data in pins at the leading edge of CLK. See Figures 12 and 13.

For the four–pin interfacing scheme, the auxiliary data select bit is set to 1. In this scheme, the 16–bit transmit counter's data enters into the AD_{in} pin at the same time as the 16–bit receive counter's data enters into the D_{in} pin. This simultaneous entry of the transmit and receive counters causes the programming period of the four–pin scheme to be half that of the three–pin scheme (see Figures 14 and 15).

While programming Tx/Rx Channel Counter, the ENB pin must be pulsed to provide falling edge to latch the shifted data after the rising edge of the last clock. Maximum data transfer rate is 500 kbps.

NOTE

10 ms should be allowed for initial start–up time for the oscillator to allow all registers to clear and enable programming of new register values.



NOTE: ENB must be high during the serial transfer.

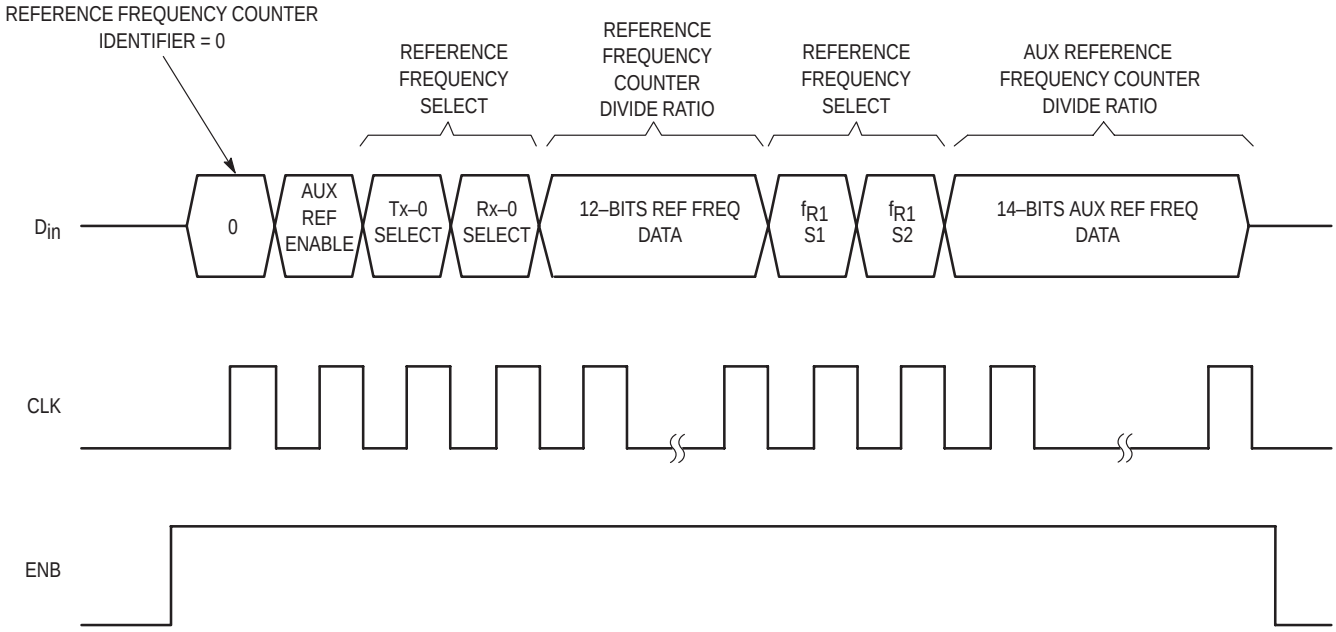
Figure 8. Programming Format of the Control Register

Table 1. Control Register Function Bits Description

Test Bit	Set to 1 for Tx/Rx channel counter test mode Set to 0 for normal application
Aux Data Select	Set to 1 for both AD_{in} and D_{in} pins inputting the transmit 16–bits data and receive 16–bits data respectively. Set to 0 for normal application interfacing with MCU serial peripheral interface. Does not use AD_{in} pin; tie AD_{in} to V_{SS}.
REF_{out} ÷ 3/÷ 4	If set to 1, REF_{out} output frequency is equal to OSC_{out} ÷3. If set to 0, REF_{out} output is OSC_{out} ÷4.
TxPD Enable	If set to 1, the transmit counter, transmit phase detector, and the associated circuitry is in power–down mode. Tx PS/f_{Tx} is set “High”.
RxPD Enable	If set to 1, the receive counter, receive phase detector, and the associated circuitry is in power–down mode. Rx PS/f_{RX} is set “High”.
Ref PD Enable	If set to 1, both 12–bit and 14–bit reference frequency counters are in power–down mode.

Table 2. Control Register Power Down Bits Function

TxPD Enable	RxPD Enable	REF PD Enable	Tx–Channel Counter	Rx–Channel Counter	Reference Frequency Counter
0	0	0	—	—	—
0	0	1	—	—	Power Down
0	1	0	—	Power Down	—
0	1	1	—	Power Down	Power Down
1	0	0	Power Down	—	—
1	0	1	Power Down	—	Power Down
1	1	0	Power Down	Power Down	—
1	1	1	Power Down	Power Down	Power Down



NOTE: ENB must be high during the serial transfer.

Figure 9. Programming Format of the Auxiliary/Reference Frequency Counters

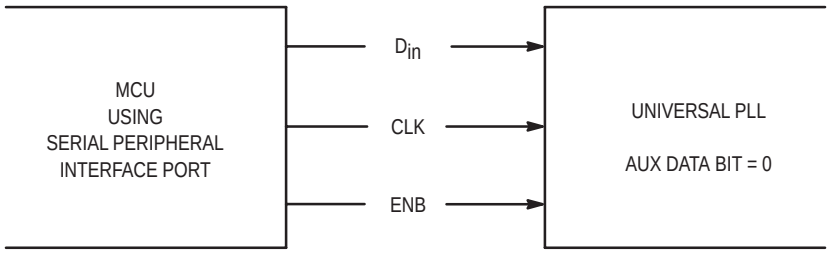


Figure 10. MCU Interface Using SPI

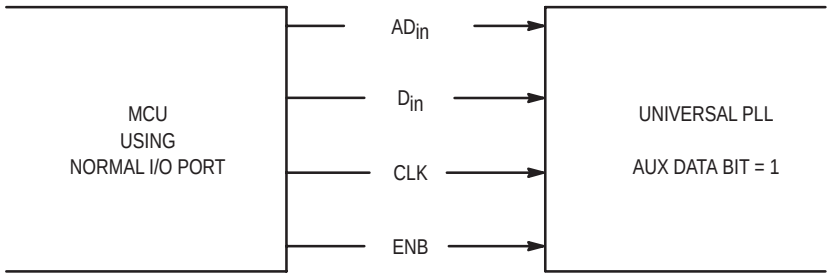
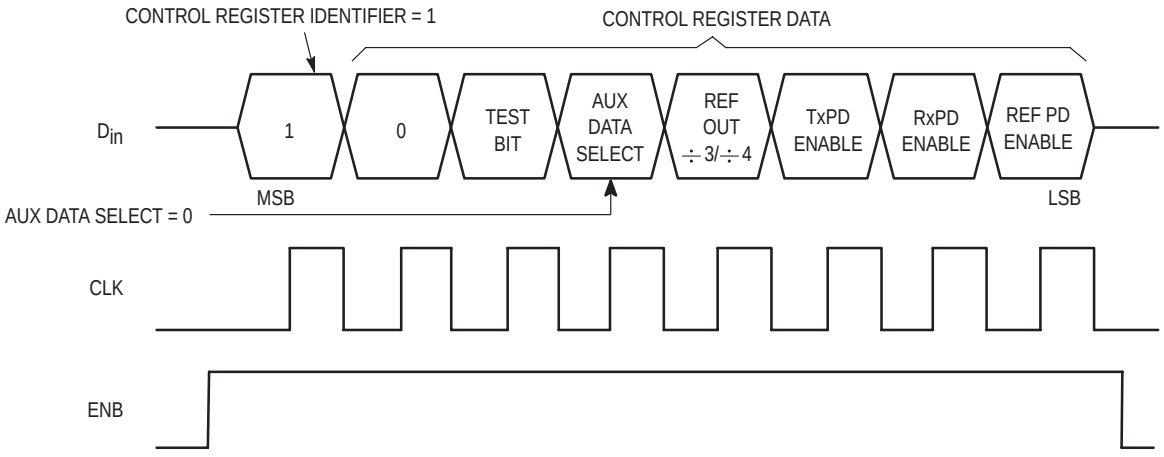
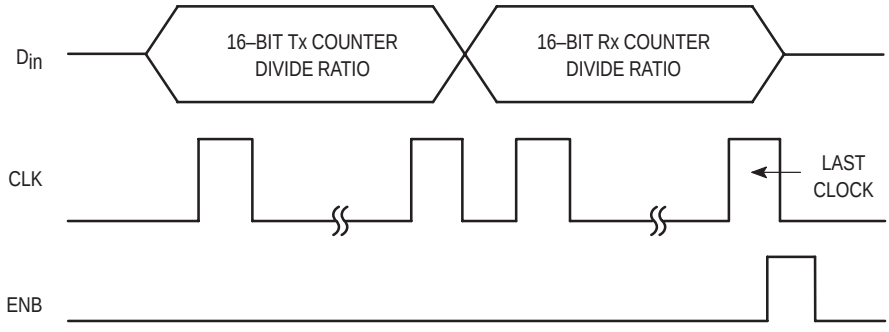


Figure 11. MCU Interface Using Normal I/O Ports with Both D_{in} and AD_{in} for Faster Programming Time



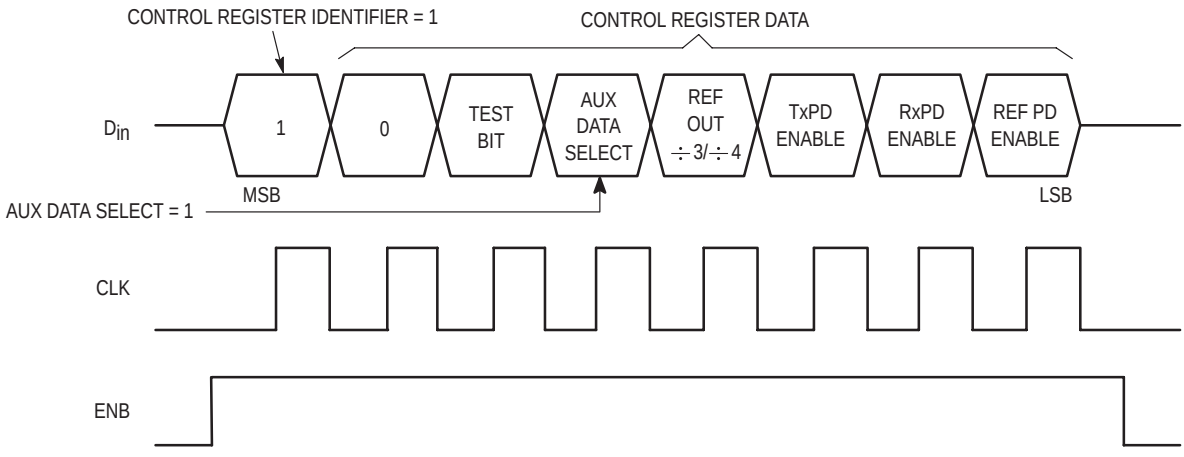
NOTE: ENB must be high during the serial transfer.

Figure 12. Programming Format for Control Register (3–Pin Interfacing Scheme)



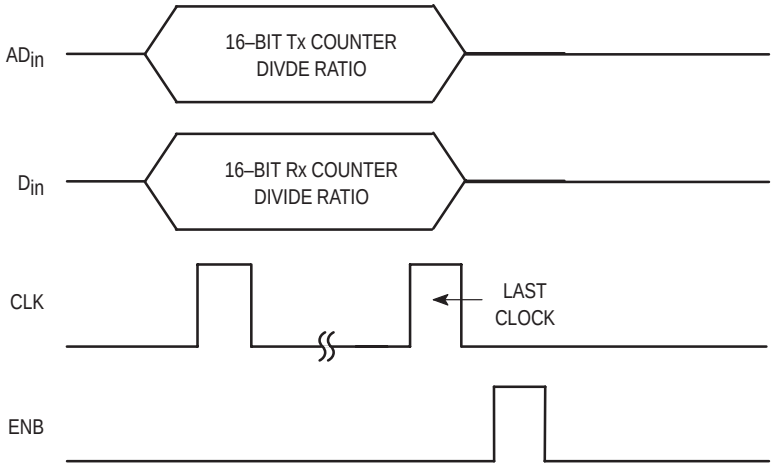
NOTE: ENB must be low during the serial transfer.

Figure 13. Programming Format for Transmit and Receive Counters (3–Pin Interfacing Scheme)



NOTE: ENB must be high during the serial transfer.

Figure 14. Programming Format for Control Register (4–Pin Interfacing Scheme)



NOTE: ENB must be low during the serial transfer.

Figure 15. Programming Format for Transmit and Receive Counters (4–Pin Interfacing Scheme)

Table 3. Global CT–1 Reference Frequency Setting vs Channel Frequencies

Country	Channels Frequency	f_{R1}	f_{R2}
U.S.A.	46/49 MHz (10, 15, 25 Channels)	5.0 kHz	—
France	26/41 MHz	6.25 kHz/12.5 kHz	—
Spain	31/41 MHz	5.0 kHz	—
Australia	30/39 MHz	5.0 kHz	—
U.K.	1.7/47 MHz	6.25 kHz	1.0 kHz
New Zealand	1.7/34/40 MHz	6.25 kHz	1.0 kHz

REFERENCE FREQUENCY SELECTION AND PROGRAMMING

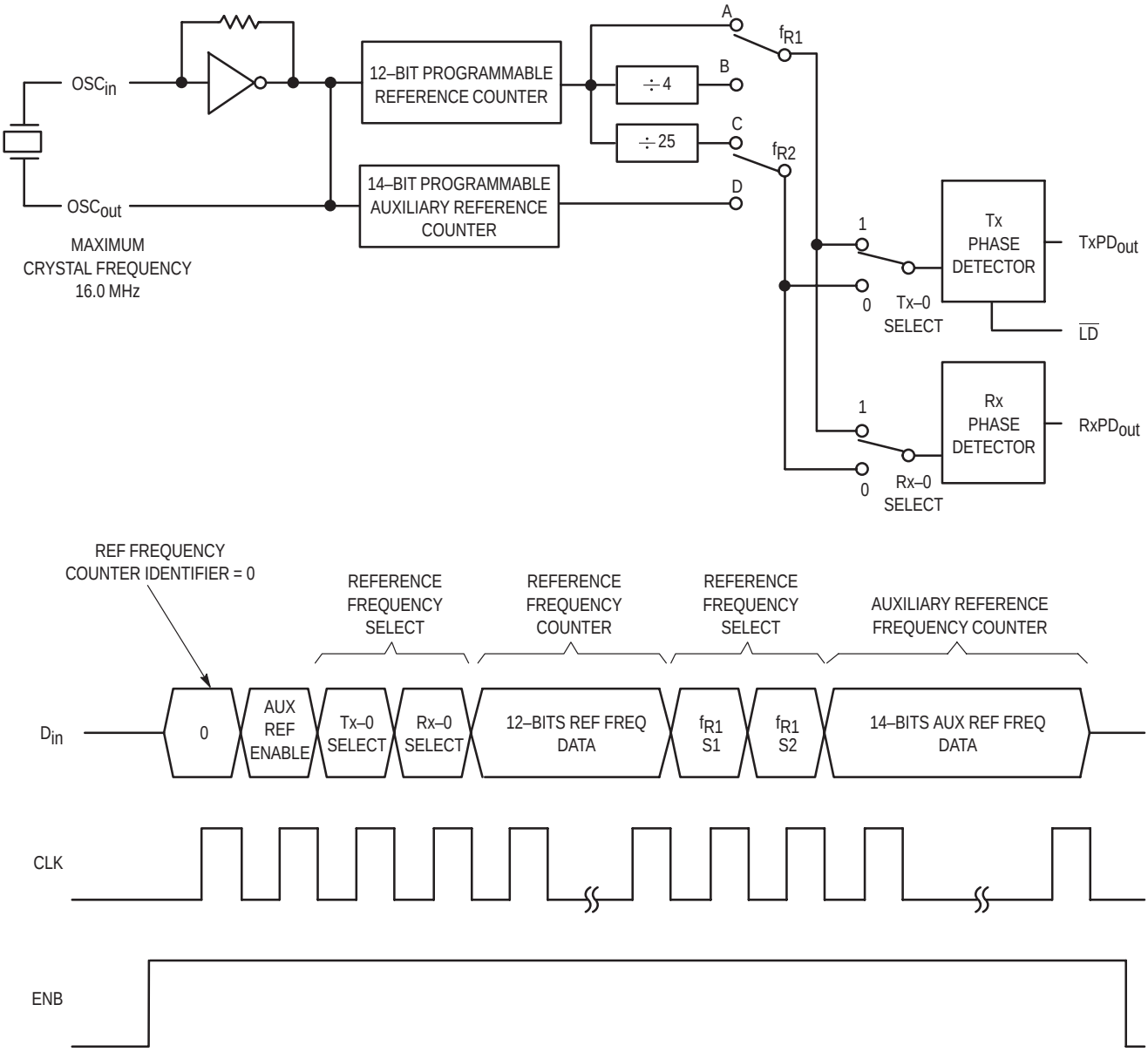
Figure 16 shows the bit function of the reference frequency programming word. The user can either select the “fixed” reference frequency for all channels accordingly or provide a specific reference frequency for a particular channel by using two reference frequency counters (e.g., for an application in France, the base set transmit channel common fixed reference frequency is 6.25 kHz or 12.5 kHz). (See Table 3 and Figure 6 for reference frequencies for various countries.) However, transmit channels 6, 8, and 14 can be set to 25 kHz, and channel 8 reference frequency can be set to 50 kHz. But this reference frequency may not be applied to the receiving side; therefore, the receiving side reference frequency must be generated by another reference frequency counter. The higher the reference frequency, the better the phase noise performance and faster the lock time, but the PLL consumes more current if both reference frequency counters are in operation.

In general, the 12–bit reference frequency counter plus the ÷ 4 and ÷ 25 module can offer all the reference frequencies for global CT–1 transmit and receive channel requirements. Users can select their own reference frequency by introducing the additional 14–bit auxiliary reference frequency counter.

Again, the 14–bit auxiliary reference frequency counter can be shut down by the auxiliary reference enable bit in the reference counter programming word by setting the bit to 0. At this state, the f_{R2} is automatically connected to point C (the ÷25 block output), and f_{R1} can be connected to point A or B by setting the f_{R1}–S1 and f_{R1}–S2 bits in the reference counter program word. The 14–bit auxiliary reference frequency counter data will be in “Don’t Care” state.

If the 14–bit auxiliary reference frequency counter is enabled (auxiliary reference enable = 1), then f_{R2} is automatically connected to point D (14–bit counter output), and f_{R1} can be selected to connect to point A, B, or C, depending on the bit setting of f_{R1}–S1 and f_{R1}–S2.

Table 4 and Figure 16 describe the functions of the auxiliary reference enable bit and the f_{R1}–S1 and f_{R1}–S2 bits selection.



NOTE: ENB must be high during the serial transfer.

Figure 16. Reference Frequency Counter/Selection Programming Mode

Table 4. Bit Function and the Reference Frequency Selection Bit Setting of the Reference Frequency Counter Programming Word

AUX REF Enable	Auxiliary Reference Frequency Counter Mode	Module Select	f_{R1} S1	f_{R1} S2	f_{R1} Routing
0	14–Bit Auxiliary Reference Frequency Counter Disable	f_{R2} C	0	0	N/A
			0	1	f_{R1} A
			1	0	f_{R1} B
			1	1	N/A
1	14–Bit Auxiliary Reference Frequency Counter Enable	f_{R2} D	0	0	N/A
			0	1	f_{R1} A
			1	0	f_{R1} B
			1	1	f_{R1} C

N/A = Not Applicable

POWER SAVING OPERATION

This PLL has a programmable power–saving scheme. The transmit and receive counters and the reference frequency counter can be powered down individually by setting the TxPD enable, RxPD enable, and Ref PD enable bits of the control register. The functions of the power down control bits are explained in Table 2 and the programming format is in Figure 8.

The output pins TxPS/f_{TX} and RxPS/f_{RX} output the status of the internal power saving setting. If the bit TxPD enable is set “high” (transmit counter is set to power–down mode), then the TxPS/f_{TX} pin will also output a “high” state. This TxPS/f_{TX} output can control an external power switch to switch off the transmitter, as shown in Figure 17. This scheme can be applied to the RxPS/f_{RX} output to control the receiver power saving operation as required.

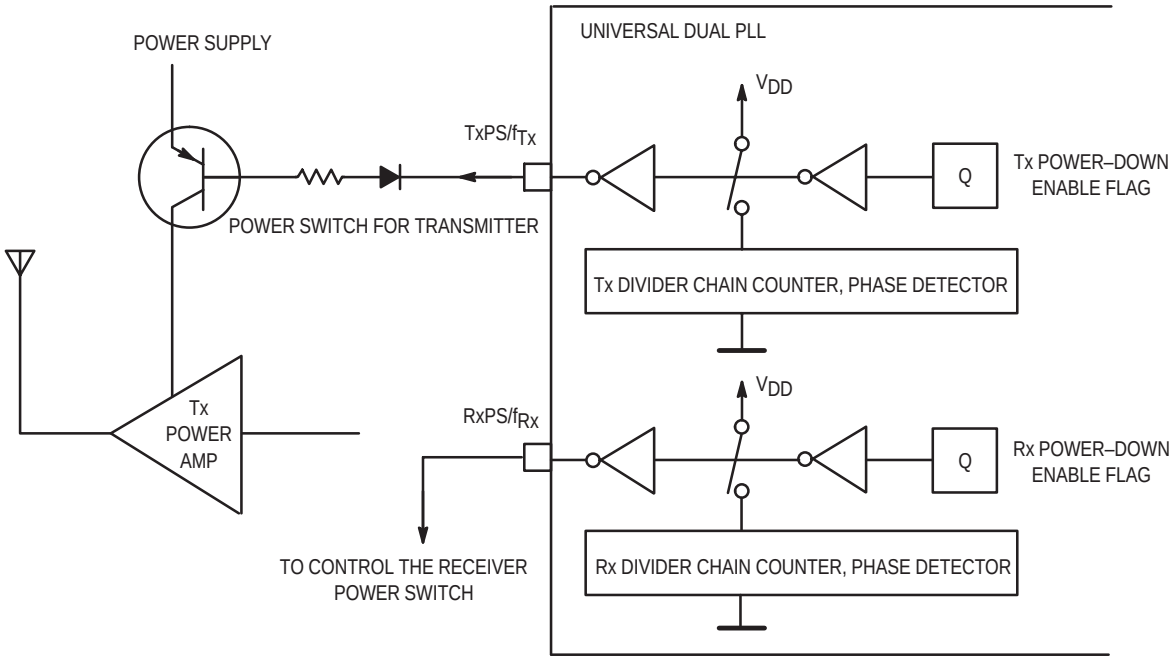


Figure 17. TxPS/f_{TX} and RxPS/f_{RX} Outputs to Control Power Switches of the Transmitter and the Receiver

Tx/Rx CHANNEL COUNTER TEST

In normal applications, the TxPS/f_{Tx} and the RxPS/f_{Rx} output pins indicate the power saving mode status. However, the user can examine the Tx and Rx channel counter outputs by setting the Test bit in the control register to 1. The final value of the transmit–channel counter and the receive–channel counter multiplex out to TxPS/f_{Tx} and RxPS/f_{Rx} respectively. The user can verify the divided–down output waveform associated with the RF input level in the PLL circuitry implementation (Figure 18).

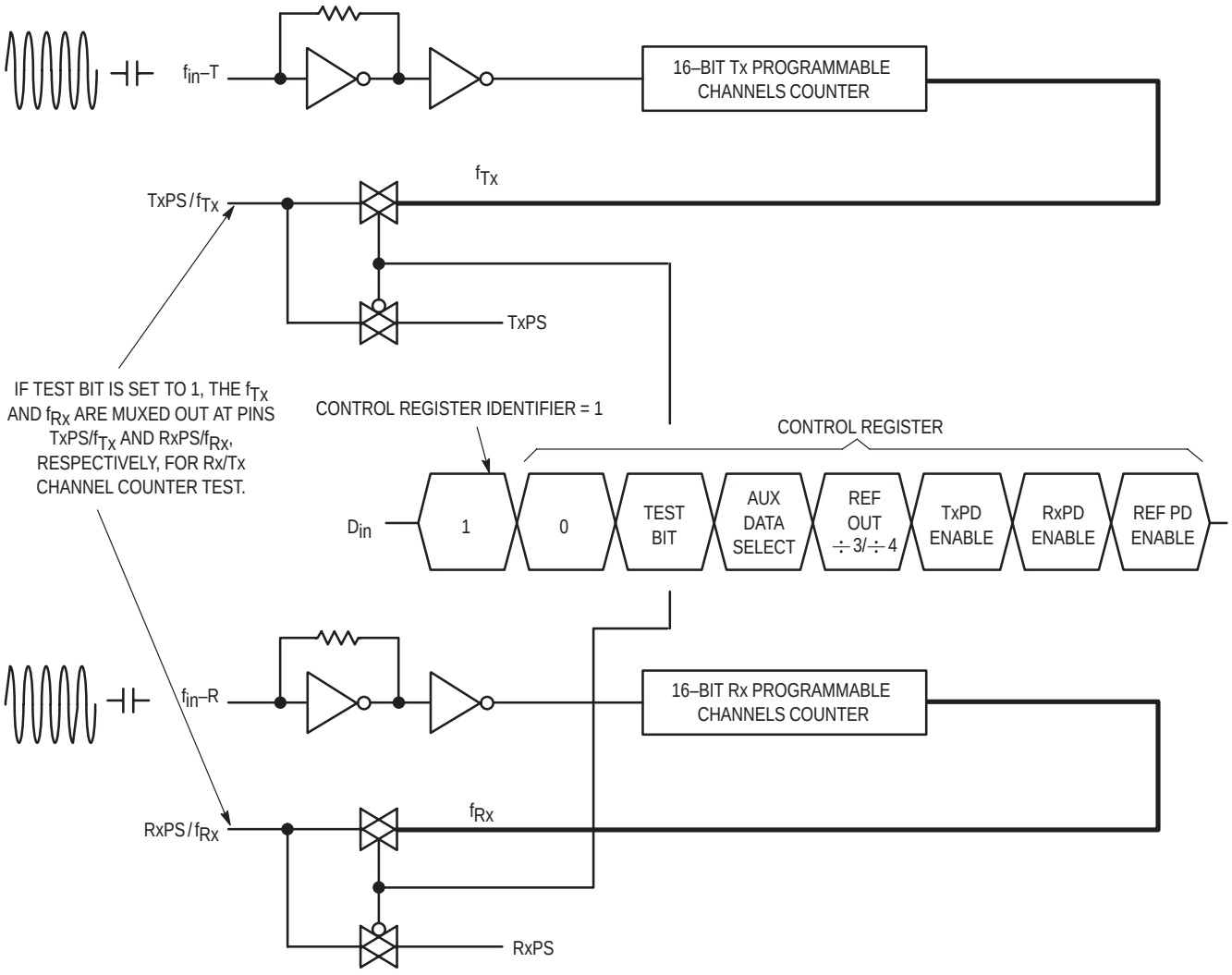


Figure 18. RF Buffer Sensitivity

Table 5. France CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	26.4875	4238	30.7875	4926
2	26.4750	4236	30.7750	4924
3	26.4625	4234	30.7625	4922
4	26.4500	4232	30.7500	4920
5	26.4375	4230	30.7375	4918
6	26.4250	4228	30.7250	4916
7	26.4125	4226	30.7125	4914
8	26.4000	4224	30.7000	4912
9	26.3875	4222	30.6875	4910
10	26.3750	4220	30.6750	4908
11	26.3625	4218	30.6625	4906
12	26.3500	4216	30.6500	4904
13	26.3375	4214	30.6375	4902
14	26.3250	4212	30.6250	4900
15	26.3125	4210	30.6125	4898

Table 6. France CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	41.4875	6638	37.1875	5950
2	41.4750	6636	37.1750	5948
3	41.4625	6634	37.1625	5946
4	41.4500	6632	37.1500	5944
5	41.4375	6630	37.1375	5942
6	41.4250	6628	37.1250	5940
7	41.4125	6626	37.1125	5938
8	41.4000	6624	37.1000	5936
9	41.3875	6622	37.0875	5934
10	41.3750	6620	37.0750	5932
11	41.3625	6618	37.0625	5930
12	41.3500	6616	37.0500	5928
13	41.3375	6614	37.0375	5926
14	41.3250	6612	37.0250	5924
15	41.3125	6610	37.0125	5922

Table 7. Spain CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	31.0250	6205	29.2300	5846
2	31.0500	6210	29.2550	5851
3	31.0750	6215	29.2800	5856
4	31.1000	6220	29.3050	5861
5	31.1250	6225	29.3300	5866
6	31.1500	6230	29.3550	5871
7	31.1750	6235	29.3800	5876
8	31.2000	6240	29.4050	5881
9	31.2500	6250	29.4550	5891
10	31.2750	6255	29.4800	5896
11	31.3000	6260	29.5050	5901
12	31.3250	6265	29.5300	5906

Table 8. Spain CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	39.9250	7985	20.3300	4066
2	39.9500	7990	20.3550	4071
3	39.9750	7995	20.3800	4076
4	40.0000	8000	20.4050	4081
5	40.0250	8005	20.4300	4086
6	40.0500	8010	20.4550	4091
7	40.0750	8015	20.4800	4096
8	40.1000	8020	20.5050	4101
9	40.1500	8030	20.5550	4111
10	40.1750	8035	20.5800	4116
11	40.2000	8040	20.6050	4121
12	40.2250	8045	20.6300	4126

Table 9. New Zealand CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	1.7820	1782	29.7625	4762
2	1.7620	1762	29.7500	4760
3	1.7420	1742	29.7375	4758
4	1.7220	1722	29.7250	4756
5	1.7020	1702	29.7125	4754
6	34.3500	5496	29.7000	4752
7	34.3625	5498	29.6875	4750
8	34.3750	5500	29.6750	4748
9	34.3875	5502	29.6625	4746
10	34.4000	5504	29.6500	4744

Ref Freq = 1.0 kHz

Ref Freq = 6.25 kHz

Table 10. New Zealand CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz)	Rx Counter Value
1	40.4625	6474	2.2370	2237
2	40.4500	6472	2.2170	2217
3	40.4375	6470	2.1970	2197
4	40.4250	6468	2.1770	2177
5	40.4125	6466	2.1570	2157
6	40.4000	6464	23.6500	3784
7	40.3875	6462	23.6625	3786
8	40.3750	6460	23.6750	3788
9	40.3625	6458	23.6875	3790
10	40.3500	6456	23.7000	3792

Ref Freq = 455 kHz

Ref Freq = 1.0 kHz

Ref Freq = 10.7 kHz

Ref Freq = 6.25 kHz

Table 11. Australia CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	30.0750	6015	29.0800	5816
2	30.1250	6025	29.1300	5826
3	30.1750	6035	29.1800	5836
4	30.2250	6045	29.2300	5846
5	30.2750	6055	29.2800	5856
6	30.1000	6020	29.1050	5821
7	30.1500	6030	29.1550	5831
8	30.2000	6040	29.2050	5841
9	30.2500	6050	29.2550	5851
10	30.3000	6060	29.3050	5861

Table 12. Australia CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	39.7750	7955	19.3800	3876
2	39.8250	7965	19.4300	3886
3	39.8750	7975	19.4800	3896
4	39.9250	7985	19.5300	3906
5	39.9750	7995	19.5800	3916
6	39.8000	7960	19.4050	3881
7	39.8500	7970	19.4550	3891
8	39.9000	7980	19.5050	3901
9	39.9500	7990	19.5550	3911
10	40.0000	8000	19.6050	3921

Table 13. U.K. CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 1.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	1.6420	1642	36.75625	5881
2	1.6620	1662	36.76875	5883
3	1.6820	1682	36.78125	5885
4	1.7020	1702	36.79375	5887
5	1.7220	1722	36.80625	5889
6	1.7420	1742	36.81875	5891
7	1.7620	1762	36.83125	5893
8	1.7820	1782	36.84375	5895

Table 14. U.K. CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 455 kHz]	Rx Counter Value (Ref. Freq. = 1.00 kHz)
1	47.45625	7593	2.097	2097
2	47.46875	7595	2.117	2117
3	47.48125	7597	2.137	2137
4	47.49375	7599	2.157	2157
5	47.50625	7601	2.177	2177
6	47.51875	7603	2.197	2197
7	47.53125	7605	2.217	2217
8	47.54375	7607	2.237	2237

Table 15. U.S.A. (10 Channels) CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	46.610	9322	38.975	7795
2	46.630	9326	38.150	7830
3	46.670	9334	38.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.180	7836
6	46.770	9354	39.135	7827
7	46.830	9366	39.195	7839
8	46.870	9374	39.235	7847
9	46.930	9386	39.295	7859
10	46.970	9394	39.275	7855

Table 16. U.S.A. (10 Channels) CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255

Table 17. U.S.A. (25 Channels) CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	43.72	8744	38.06	7612
2	43.74	8748	38.14	7628
3	43.82	8764	38.16	7632
4	43.84	8768	38.22	7644
5	43.92	8784	38.32	7664
6	43.96	8788	38.38	7676
7	44.12	8824	38.40	7680
8	44.16	8832	38.46	7692
9	44.18	8836	38.50	7700
10	44.20	8840	38.54	7708
11	44.32	8864	38.58	7716
12	44.36	8872	38.66	7732
13	44.40	8880	38.70	7740
14	44.46	8892	38.76	7752
15	44.48	8896	38.80	7760
16	46.61	9322	38.97	7794
17	46.63	9326	39.145	7829
18	46.67	9334	39.16	7832
19	46.71	9342	39.07	7814
20	46.73	9346	39.175	7835
21	46.77	9354	39.13	7826
22	46.83	9366	39.19	7838
23	46.87	9374	39.23	7846
24	46.93	9386	39.29	7858
25	46.97	9394	39.27	7854

Table 18. U.S.A. (25 Channels) CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	48.76	9752	33.02	6604
2	48.84	9768	33.04	6608
3	48.86	9772	33.12	6624
4	48.92	9748	33.14	6628
5	49.02	9804	33.22	6644
6	49.08	9816	33.26	6652
7	49.10	9820	33.42	6684
8	49.16	9832	33.46	6692
9	49.20	9840	33.48	6696
10	49.24	9848	33.50	6700
11	49.28	9856	33.62	6724
12	49.36	9872	33.66	6732
13	49.40	9880	33.70	6740
14	49.46	9892	33.76	6752
15	49.50	9900	33.78	6756
16	49.67	9934	33.91	7182
17	49.845	9969	33.93	7186
18	49.86	9972	33.97	7194
19	49.77	9954	36.01	7202
20	49.875	9975	36.03	7206
21	49.83	9966	36.07	7214
22	49.89	9978	36.13	7226
23	49.93	9986	36.17	7234
24	49.99	9998	36.23	7246
25	49.97	9994	36.27	7254

Table 19. Korea CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	46.610	9322	38.975	7795
2	46.630	9326	38.150	7830
3	46.670	9334	38.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.180	7836
6	46.770	9354	39.135	7827
7	46.830	9366	39.195	7839
8	46.870	9374	39.235	7847
9	46.930	9386	39.295	7859
10	46.970	9394	39.275	7855
11	46.510	9302	39.000	7800
12	46.530	9306	39.015	7803
13	46.550	9310	39.030	7806
14	46.570	9314	39.045	7809
15	46.590	9318	39.060	7812

Table 20. Korea CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255
11	49.695	9939	35.815	7163
12	49.710	9942	35.835	7167
13	49.725	9945	35.855	7171
14	49.740	9948	35.875	7175
15	49.755	9951	35.895	7179

Table 21. China CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	45.250	9050	37.550	7510
2	45.275	9055	37.575	7515
3	45.300	9060	37.600	7520
4	45.325	9065	37.625	7525
5	45.350	9070	37.650	7530
6	45.375	9075	37.675	7535
7	45.400	9080	37.700	7540
8	45.425	9085	37.725	7545
9	45.450	9090	37.750	7550
10	45.475	9095	37.775	7555

Table 22. China CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	48.250	9650	34.550	6910
2	48.275	9655	34.575	6915
3	48.300	9660	34.600	6920
4	48.325	9665	34.625	6925
5	48.350	9670	34.650	6930
6	48.375	9675	34.675	6935
7	48.400	9680	34.700	6940
8	48.425	9685	34.725	6945
9	48.450	9690	34.750	6950
10	48.475	9695	34.775	6955

MOTOROLA

MC145170-2

PLL Frequency Synthesizer with Serial Interface

The new MC145170–2 is pin–for–pin compatible with the MC145170–1. A comparison of the two parts is shown in the table below. The MC145170–2 is recommended for new designs and has a more robust power–on reset (POR) circuit that is more responsive to momentary power supply interruptions. The two devices are actually the same chip with mask options for the POR circuit. The more robust POR circuit draws approximately 20 μA additional supply current. Note that the maximum specification of 100 μA quiescent supply current has not changed.

The MC145170–2 is a single–chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL easy to program. Either a bit– or byte–oriented format may be used. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 2–byte serial transfer to the 16–bit N register.

The device features fully programmable R and N counters, an amplifier at the f_{in} pin, on–chip support of an external crystal, a programmable reference output, and both single– and double–ended phase detectors with linear transfer functions (no dead zones). A configuration (C) register allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing noise and interference.

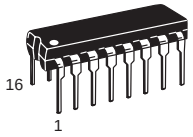
In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam–load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam–loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

- Operating Voltage Range: 2.7 to 5.5 V
- Maximum Operating Frequency:
  185 MHz @ V_{in} = 500 mVpp, 4.5 V Minimum Supply
  100 MHz @ V_{in} = 500 mVpp, 3.0 V Minimum Supply
- Operating Supply Current:
  0.6 mA @ 3.0 V, 30 MHz
  1.5 mA @ 3.0 V, 100 MHz
  3.0 mA @ 5.0 V, 50 MHz
  5.8 mA @ 5.0 V, 185 MHz
- Operating Temperature Range: –40 to 85°C
- R Counter Division Range: 1 and 5 to 32,767
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola SPI Serial Data Port
- See Application Notes AN1207/D and AN1671/D
- See web site *mot–sps.com* for MC145170 control software. Select in order, Products, Wireless Semiconductor, Download, then PLL Demo Software. Choose PLLGEN.EXE.

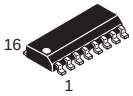
BitGrabber is a trademark of Motorola Inc.

CMOS PLL FREQUENCY SYNTHESIZER WITH SERIAL INTERFACE

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 648

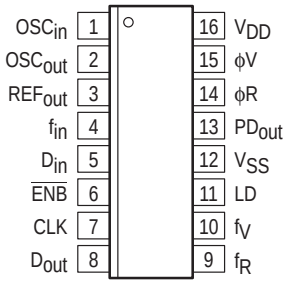


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SOG–16)



DT SUFFIX
PLASTIC PACKAGE
CASE 948C
(TSSOP–16)

PIN CONNECTIONS



(Top View)

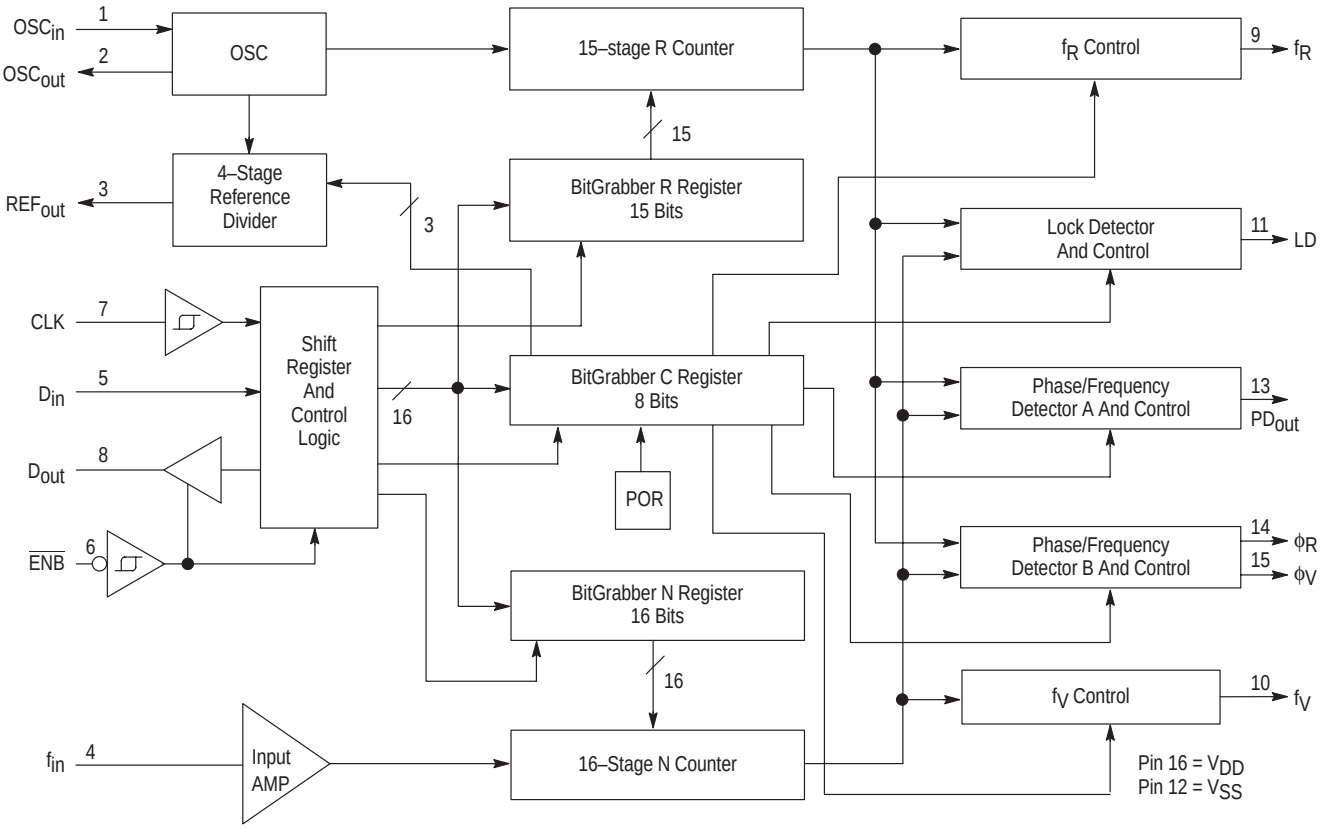
COMPARISION OF THE PLL FREQUENCY SYNTHESIZERS

Parameter	MC145170–2	MC145170–1
Minimum Supply Voltage	2.7 V	2.5 V
Maximum Input Current, f_{in}	150 μA	120 μA
Dynamic Characteristics, f_{in} (Figure 23)	Unchanged	–
Power–On Reset Circuit	Improved	–

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC145170P2	T_A = –40 to 85°C	Plastic DIP
MC145170D2		SOG–16
MC145170DT2		TSSOP–16

BLOCK DIAGRAM



This device contains 4,800 active transistors.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 5.5	V
DC Input Voltage	V_{in}	–0.5 to V_{DD} + 0.5	V
DC Output Voltage	V_{out}	–0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
DC Output Current, per Pin	I_{out}	±20	mA
DC Supply Current, V_{DD} and V_{SS} Pins	I_{DD}	±30	mA
Power Dissipation, per Package	P_D	300	mW
Storage Temperature	T_{stg}	–65 to 150	°C
Lead Temperature, 1 mm from Case for 10 seconds	T_L	260	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.
2. ESD data available upon request.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = –40 to 85°C)

Parameter	Test Condition	Symbol	V_{DD} V	Guaranteed Limit	Unit
Power Supply Voltage Range		V_{DD}	–	2.7 to 5.5	V
Maximum Low–Level Input Voltage [Note 1] (D_{in}, CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	V_{IL}	2.7 4.5 5.5	0.54 1.35 1.65	V
Minimum High–Level Input Voltage [Note 1] (D_{in}, CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	V_{IH}	2.7 4.5 5.5	2.16 3.15 3.85	V
Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		V_{Hys}	2.7 5.5	0.15 0.20	V
Maximum Low–Level Output Voltage (Any Output)	I_{out} = 20 μA	V_{OL}	2.7 5.5	0.1 0.1	V
Minimum High–Level Output Voltage (Any Output)	I_{out} = – 20 μA	V_{OH}	2.7 5.5	2.6 5.4	V
Minimum Low–Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	I_{OL}	2.7 4.5 5.5	0.12 0.36 0.36	mA
Minimum High–Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 2.4 V V_{out} = 4.1 V V_{out} = 5.0 V	I_{OH}	2.7 4.5 5.5	–0.12 –0.36 –0.36	mA
Minimum Low–Level Output Current (D_{out})	V_{out} = 0.4 V	I_{OL}	4.5	1.6	mA
Minimum High–Level Output Current (D_{out})	V_{out} = 4.1 V	I_{OH}	4.5	–1.6	mA
Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, OSC_{in})	V_{in} = V_{DD} or V_{SS}	I_{in}	5.5	±1.0	μA
Maximum Input Current (f_{in})	V_{in} = V_{DD} or V_{SS}	I_{in}	5.5	±150	μA
Maximum Output Leakage Current (PD_{out})	V_{in} = V_{DD} or V_{SS}, Output in High–Impedance State	I_{OZ}	5.5	±100	nA
(D_{out})			5.5	±5.0	μA
Maximum Quiescent Supply Current	V_{in} = V_{DD} or V_{SS}; Outputs Open; Excluding f_{in} Amp Input Current Component	I_{DD}	5.5	100	μA
Maximum Operating Supply Current	f_{in} = 500 mVpp; OSC_{in} = 1.0 MHz @ 1.0 Vpp; LD, f_R, f_V, REF_{out} = Inactive and No Connect; OSC_{out}, ϕ_V, ϕ_R, PD_{out} = No Connect; D_{in}, ENB, CLK = V_{DD} or V_{SS}	I_{dd}	–	[Note 2]	mA

NOTES: 1. When dc coupling to the OSC_{in} pin is used, the pin must be driven rail–to–rail. In this case, OSC_{out} should be floated.
2. The nominal values at 3.0 V are 0.6 mA @ 30 MHz, and 1.5 mA @ 100 MHz. The nominal values at 5.0 V are 3.0 mA @ 50 MHz, and 5.8 mA @ 185 MHz. These are not guaranteed limits.

AC INTERFACE CHARACTERISTICS (T_A = –40 to 85°C, C_L = 50 pF, Input $t_r = t_f$ = 10 ns, unless otherwise noted.)

Parameter	Symbol	Figure No.	V_{DD} V	Guaranteed Limit	Unit
Serial Data Clock Frequency (Note: Refer to Clock t_w Below)	f_{clk}	1	2.7 4.5 5.5	dc to 3.0 dc to 4.0 dc to 4.0	MHz
Maximum Propagation Delay, CLK to D_{out}	t_{PLH}, t_{PHL}	1, 5	2.7 4.5 5.5	150 85 85	ns
Maximum Disable Time, D_{out} Active to High Impedance	t_{PLZ}, t_{PHZ}	2, 6	2.7 4.5 5.5	300 200 200	ns
Access Time, D_{out} High Impedance to Active	t_{PZL}, t_{PZH}	2, 6	2.7 4.5 5.5	0 to 200 0 to 100 0 to 100	ns
Maximum Output Transition Time, D_{out} CL = 50 pF	t_{TLH}, t_{THL}	1, 5	2.7 4.5 5.5	150 50 50	ns
CL = 200 pF		1, 5	2.7 4.5 5.5	900 150 150	ns
Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK	C_{in}		–	10	pF
Maximum Output Capacitance – D_{out}	C_{out}		–	10	pF

TIMING REQUIREMENTS (T_A = –40 to 85°C, Input $t_r = t_f$ = 10 ns, unless otherwise noted.)

Parameter	Symbol	Figure No.	V_{DD} V	Guaranteed Limit	Unit
Minimum Setup and Hold Times, D_{in} vs CLK	t_{su}, t_h	3	2.7 4.5 5.5	55 40 40	ns
Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ vs CLK	t_{su}, t_h, t_{rec}	4	2.7 4.5 5.5	135 100 100	ns
Minimum Inactive–High Pulse Width, $\overline{ENB}$	$t_{w(H)}$	4	2.7 4.5 5.5	400 300 300	ns
Minimum Pulse Width, CLK	t_w	1	2.7 4.5 5.5	166 125 125	ns
Maximum Input Rise and Fall Times, CLK	t_r, t_f	1	2.7 4.5 5.5	100 100 100	µs

SWITCHING WAVEFORMS

Figure 1.

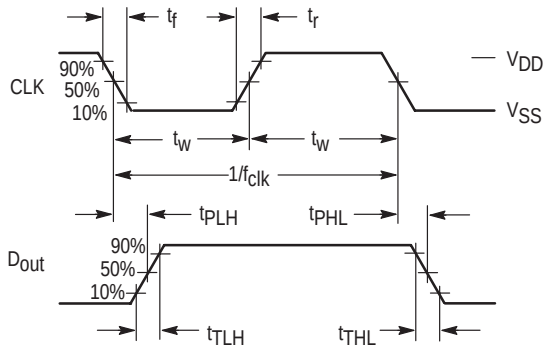


Figure 2.

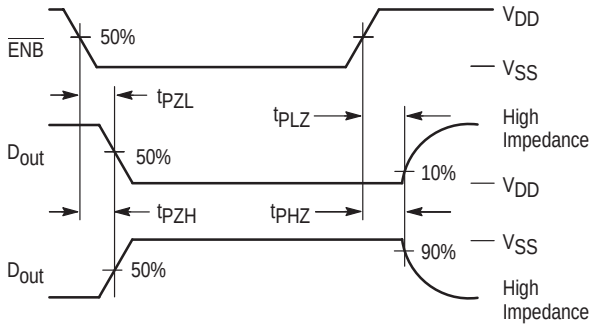


Figure 3.

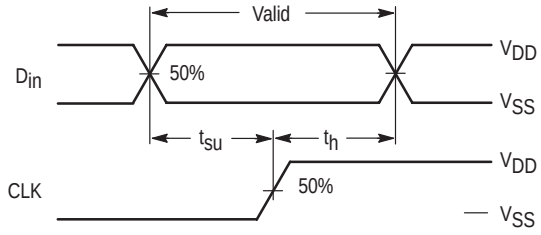


Figure 4.

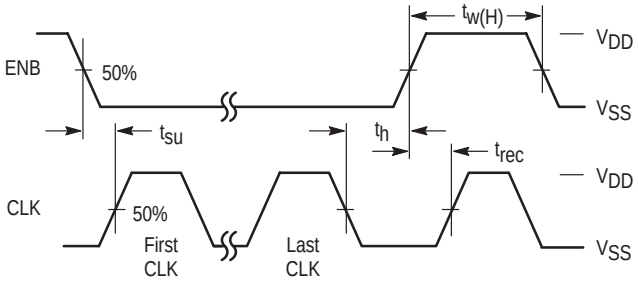
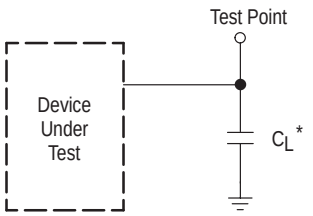
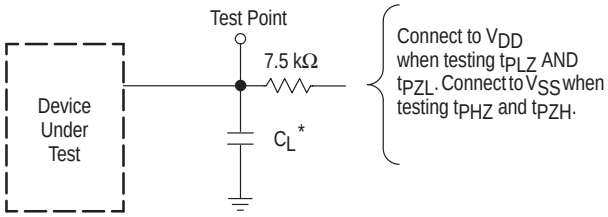


Figure 5. Test Circuit



* Includes all probe and fixture capacitance.

Figure 6. Test Circuit



* Includes all probe and fixture capacitance.

LOOP SPECIFICATIONS (T_A = –40 to 85°C)

Parameter	Test Condition	Symbol	Figure No.	V_{DD} V	Guaranteed Range		Unit
					Min	Max	
Input Frequency, f_{in} [Note}	V_{in} ≥ 500 mVpp Sine Wave, N Counter Set to Divide Ratio Such that f_V ≤ 2.0 MHz	f	7	2.7 3.0 4.5 5.5	5.0 5.0 25 45	80 100 185 185	MHz
Input Frequency, OSC_{in} Externally Driven with ac–coupled Signal	V_{in} ≥ 1.0 V_{pp} Sine Wave, OSC_{out} = No Connect, R Counter Set to Divide Ratio Such that f_R ≤ 2 MHz	f	8a	2.7 3.0 4.5 5.5	1.0* 1.0* 1.0* 1.0*	22 25 30 35	MHz
Crystal Frequency, OSC_{in} and OSC_{out}	C1 ≤ 30 pF C2 ≤ 30 pF Includes Stray Capacitance	f_{XTAL}	9	2.7 3.0 4.5 5.5	2.0 2.0 2.0 2.0	12 12 15 15	MHz
Output Frequency, REF_{out}	C_L = 30 pF	f_{out}	10, 12	2.7 4.5 5.5	dc dc dc	– 10 10	MHz
Operating Frequency of the Phase Detectors		f		2.7 4.5 5.5	dc dc dc	– 2.0 2.0	MHz
Output Pulse Width, ϕ_R, ϕ_V, and LD	f_R in Phase with f_V C_L = 50 pF	t_w	11, 12	2.7 4.5 5.5	– 20 16	– 100 90	ns
Output Transition Times, ϕ_R, ϕ_V, LD, f_R, and f_V	C_L = 50 pF	t_{TLH}, t_{THL}	11, 12	2.7 4.5 5.5	– – –	– 65 60	ns
Input Capacitance f_{in} OSC_{in}		C_{in}	– –	– –	– –	7.0 7.0	pF

* IF lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal in ac–coupled case. Also, see Figure 22 for dc coupling.

Figure 7. Test Circuit, f_{in}

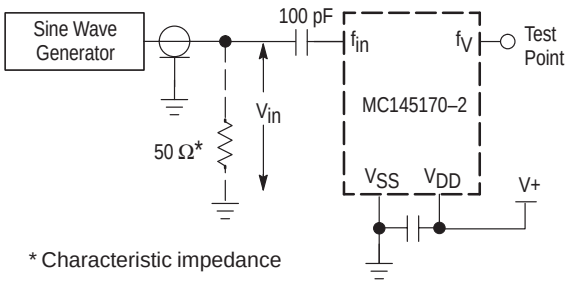


Figure 8.

Figure 8a. Test Circuit, OSC Circuit Externally Driven [Note]

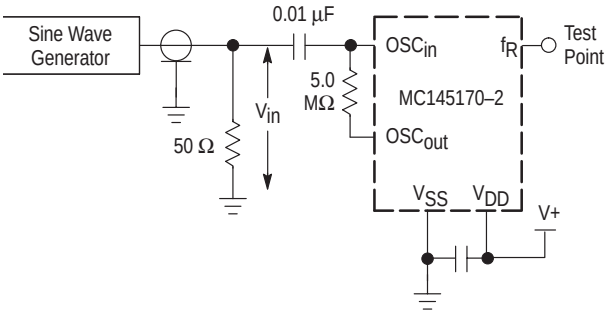


Figure 8b. Circuit to Eliminate Self–Oscillation, OSC Circuit Externally Driven [Note]

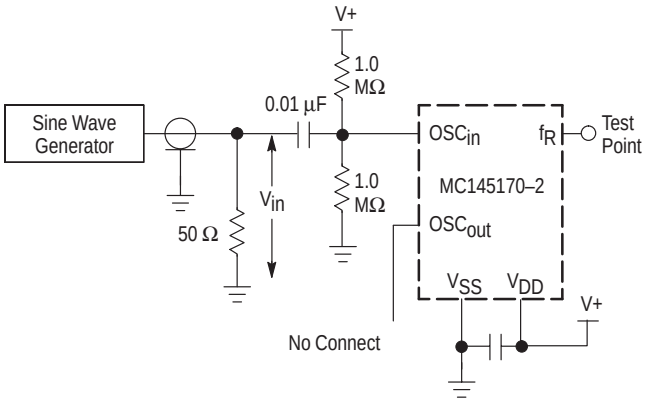


Figure 9. Test Circuit, OSC Circuit with Crystal

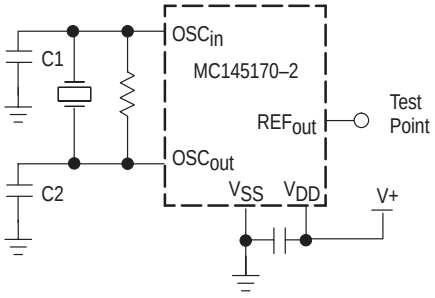


Figure 10. Switching Waveform

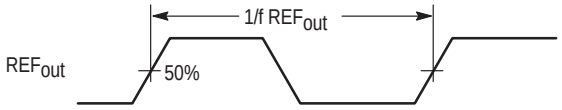


Figure 11. Switching Waveform

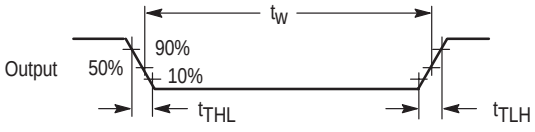
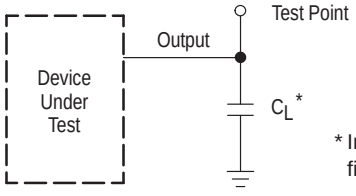


Figure 12. Test Load Circuit



NOTE: Use the circuit of Figure 8b to eliminate self–oscillation of the OSC_{in} pin when the MC145170–2 has power applied with no external signal applied at V_{in}. (Self–oscillation is not harmful to the MC145170–2 and does not damage the IC.)

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}

Serial Data Input (Pin 5)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. Additionally, the R register can be accessed with a 15–bit transfer (see Table 1). An optional pattern which resets the device is shown in Figure 13. The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 13, 14, 15, and 16.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
9 to 13	See Figure 13	(Reset)
8	C Register	C7, C6, C5, . . ., C0
16	N Register	N15, N14, N13, . . ., N0
15 or 24	R Register	R14, R13, R12, . . ., R0
Other Values ≤ 32	None	
Values > 32	See Figures 24 — 31	

CLK

Serial Data Clock Input (Pin 7)

Low–to–high transitions on Clock shift bits available at D_{in}, while high–to–low transitions shift bits from D_{out}. The chip's 16–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Four to eight clock cycles followed by five clock cycles are needed to reset the device; this is optional. Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 cycles can be used to access the R register (see Table 1 and Figures 13, 14, 15, and 16). For cascaded devices, see Figures 24 to 31.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at the potential of either the V_{SS} or V_{DD} pin during power up. That is, the CLK input should not be floated or toggled while the V_{DD} pin is ramping from 0 to at least 2.7 V. If control of the CLK pin is not practical during power up, the initialization sequence shown in Figure 13 must be used.

$\overline{ENB}$

Active–Low Enable Input (Pin 6)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited, D_{out} is forced to the high–impedance state, and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C, N, or R register depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

D_{out}

Three–State Serial Data Output (Pin 8)

Data is transferred out of the 16–1/2–stage shift register through D_{out} on the high–to–low transition of CLK. This output is a No Connect, unless used in one of the manners discussed below.

D_{out} could be fed back to an MCU/MPU to perform a wrap–around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in–line QA test during board manufacturing.

Finally, D_{out} facilitates troubleshooting a system and permits cascading devices.

REFERENCE PINS

OSC_{in}/OSC_{out}

Reference Oscillator Input/Output (Pins 1, 2)

These pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1.0 to 5.0 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the components are shown in Figure 9.

If desired, an external clock source can be ac coupled to OSC_{in}. A 0.01 µF coupling capacitor is used for measurement purposes and is the minimum size

recommended for applications. An external feedback resistor of approximately 5 MΩ is required across the OSC_{in} and OSC_{out} pins in the ac–coupled case (see Figure 8a or alternate circuit 8b). *OSC_{out} is an internal node on the device and should not be used to drive any loads* (i.e., OSC_{out} is unbuffered). However, the buffered REF_{out} is available to drive external loads.

The external signal level must be at least 1 V p–p; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz.)

If an external source is available which swings virtually rail–to–rail (V_{DD} to V_{SS}), then dc coupling can be used. In the dc–coupled case, no external feedback resistor is needed. OSC_{out} must be a No Connect to avoid loading an internal node on the device, as noted above. *For frequencies below 1 MHz, dc coupling must be used.* The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the OSC_{in} pin. See Figure 22.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one.

REF_{out}
Reference Frequency Output (Pin 3)

This output is the buffered output of the crystal–generated reference frequency or externally provided reference source. This output may be enabled, disabled, or scaled via bits in the C register (see Figure 14).

REF_{out} can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on–chip power–on–initialize circuit forces REF_{out} to the OSC_{in} divided–by–8 mode.

REF_{out} is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for OSC_{in} frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

COUNTER OUTPUT PINS

f_R
R Counter Output (Pin 9)

This signal is the buffered output of the 15–stage R counter. f_R can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_R signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the OSC_{in} pin is allowed by choosing a divide value of 1 (see Figure 15). The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R must not exceed 2 MHz.

When activated, the f_R signal appears as normally low and pulses high. The pulse width is 4.5 cycles of the OSC_{in} pin signal, except when a divide ratio of 1 is selected. When 1 is selected, the OSC_{in} signal is buffered and appears at the f_R pin.

f_V
N Counter Output (Pin 10)

This signal is the buffered output of the 16–stage N counter. f_V can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_V signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V must not exceed 2 MHz.

When activated, the f_V signal appears as normally low and pulses high.

LOOP PINS

f_{in}
Frequency Input (Pin 4)

This pin is a frequency input from the VCO. This pin feeds the on–chip amplifier which drives the N counter. This signal is normally sourced from an external voltage–controlled oscillator (VCO), and is ac–coupled into f_{in}. A 100 pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications (see Figure 7). The frequency capability of this input is dependent on the supply voltage as listed in the **Loop Specifications** table. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz.)

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, dc coupling may be used. Also, for low frequency signals (less than the minimum frequencies shown in the **Loop Specifications** table), dc coupling is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the f_{in} pin. See Figure 22.

Each rising edge on the f_{in} pin causes the N counter to decrement by 1.

PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 13)

This is a three–state output for use as a loop error signal when combined with an external low–pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: negative pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: positive pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: positive pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: negative pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high–impedance state by utilization of the disable feature in the C register (patented).

ϕ_R and ϕ_V
Double–Ended Phase/Frequency Detector Outputs (Pins 14, 15)

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register (patented).

LD
Lock Detector Output (Pin 11)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies (see Figure 17).

This output can be enabled and disabled via the C register (patented). Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

POWER SUPPLY

V_{DD}
Most Positive Supply Potential (Pin 16)

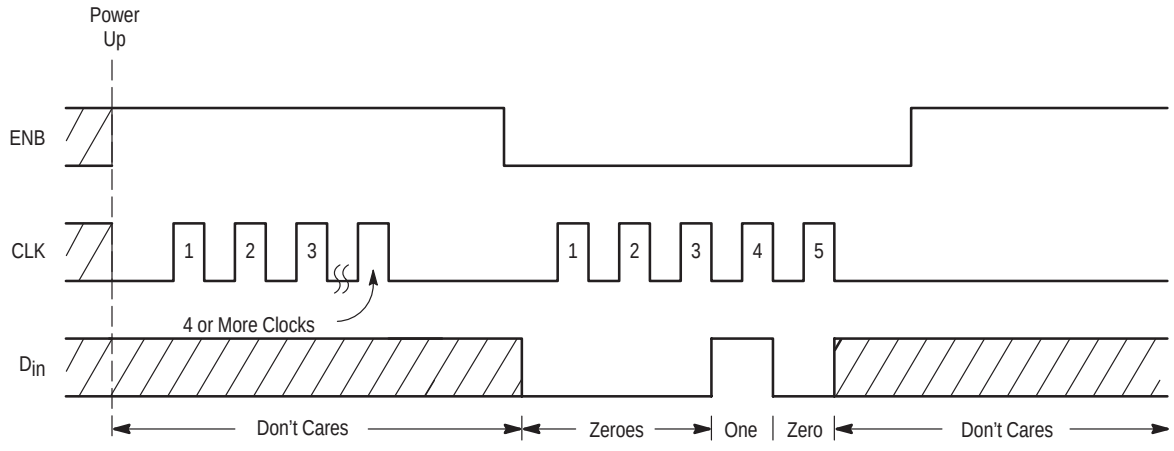
This pin may range from 2.7 to 5.5 V with respect to V_{SS}.

For optimum performance, V_{DD} should be bypassed to V_{SS} using low–inductance capacitor(s) mounted very close to the device. Lead lengths on the capacitor(s) should be minimized. (The very fast switching speed of the device causes current spikes on the power leads.)

V_{SS}
Most Negative Supply Potential (Pin 12)

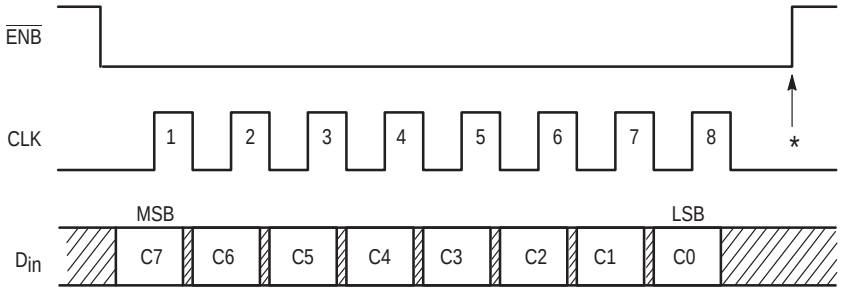
This pin is usually ground. For measurement purposes, the V_{SS} pin is tied to a ground plane.

Figure 13. Reset Sequence



NOTE: This initialization sequence is usually not necessary because the on–chip power–on reset circuit performs the initialization function. However, this initialization sequence must be used immediately after power up if control of the CLK pin is not possible. That is, if CLK (Pin 7) toggles or floats upon power up, use the above sequence to reset the device.
Also, use this sequence if power is momentarily interrupted such that the supply voltage to the device is reduced to below 2.7 V, but not down to at least 1 V (for example, the supply drops down to 2 V). This is necessary because the on–chip power–on reset is only activated when the supply ramps up from a voltage below approximately 1.0 V.

Figure 14. C Register Access and Format (8 Clock Cycles are Used)



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 17. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

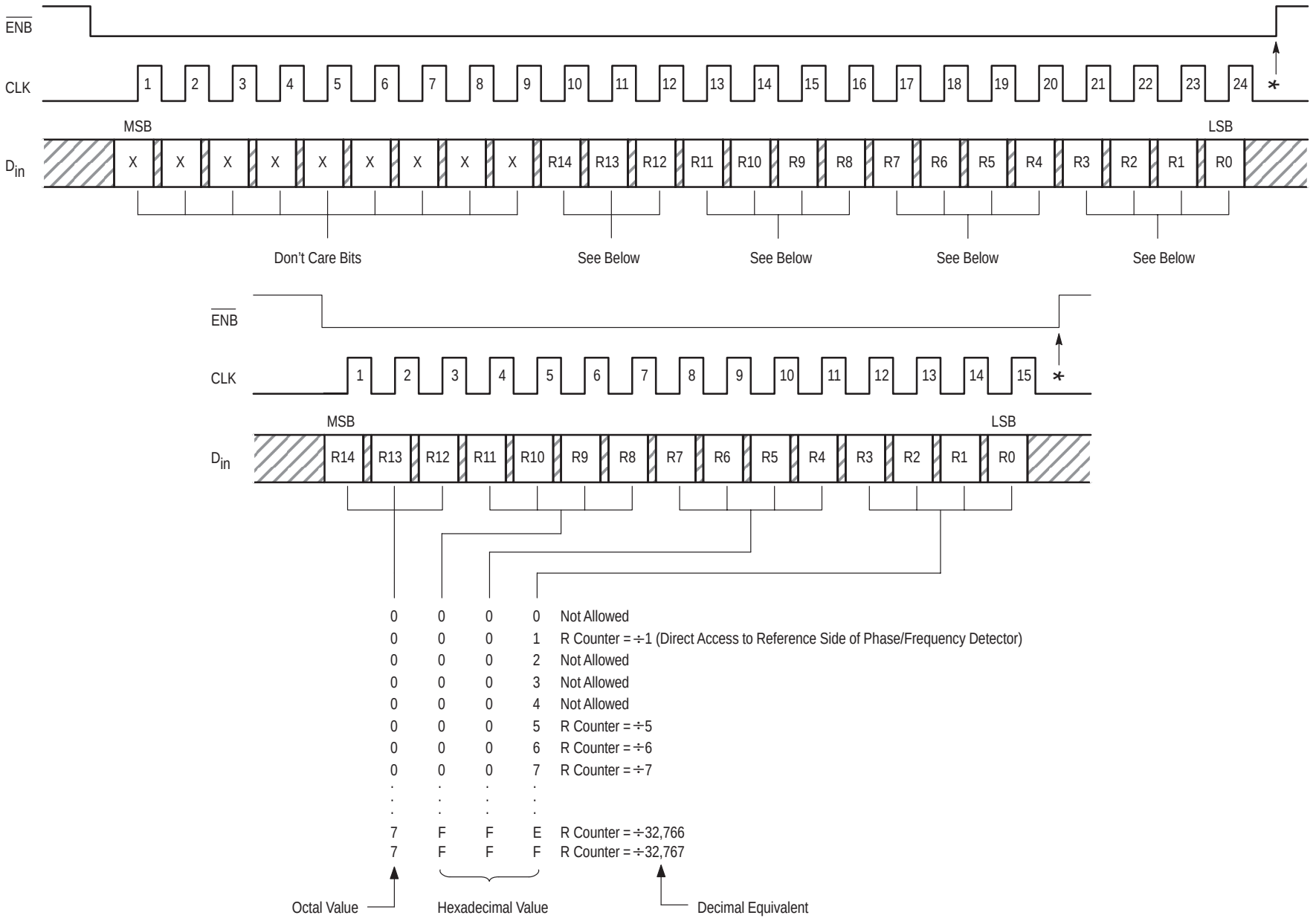
C4 – C2, OSC2 – OSC0: Reference output controls which determine the REF_{out} characteristics as shown below. Upon power up, the bits are initialized such that $OSC_{in}/8$ is selected.

C4	C3	C2	REF_{out} Frequency
0	0	0	dc (Static Low)
0	0	1	OSC_{in}
0	1	0	$OSC_{in}/2$
0	1	1	$OSC_{in}/4$
1	0	0	$OSC_{in}/8$ (POR Default)
1	0	1	$OSC_{in}/16$
1	1	0	$OSC_{in}/8$
1	1	1	$OSC_{in}/16$

C1 — f_VE: Enables the f_V output when set high. When cleared low, the f_V output is forced to a static low level. The bit is cleared low upon power up.

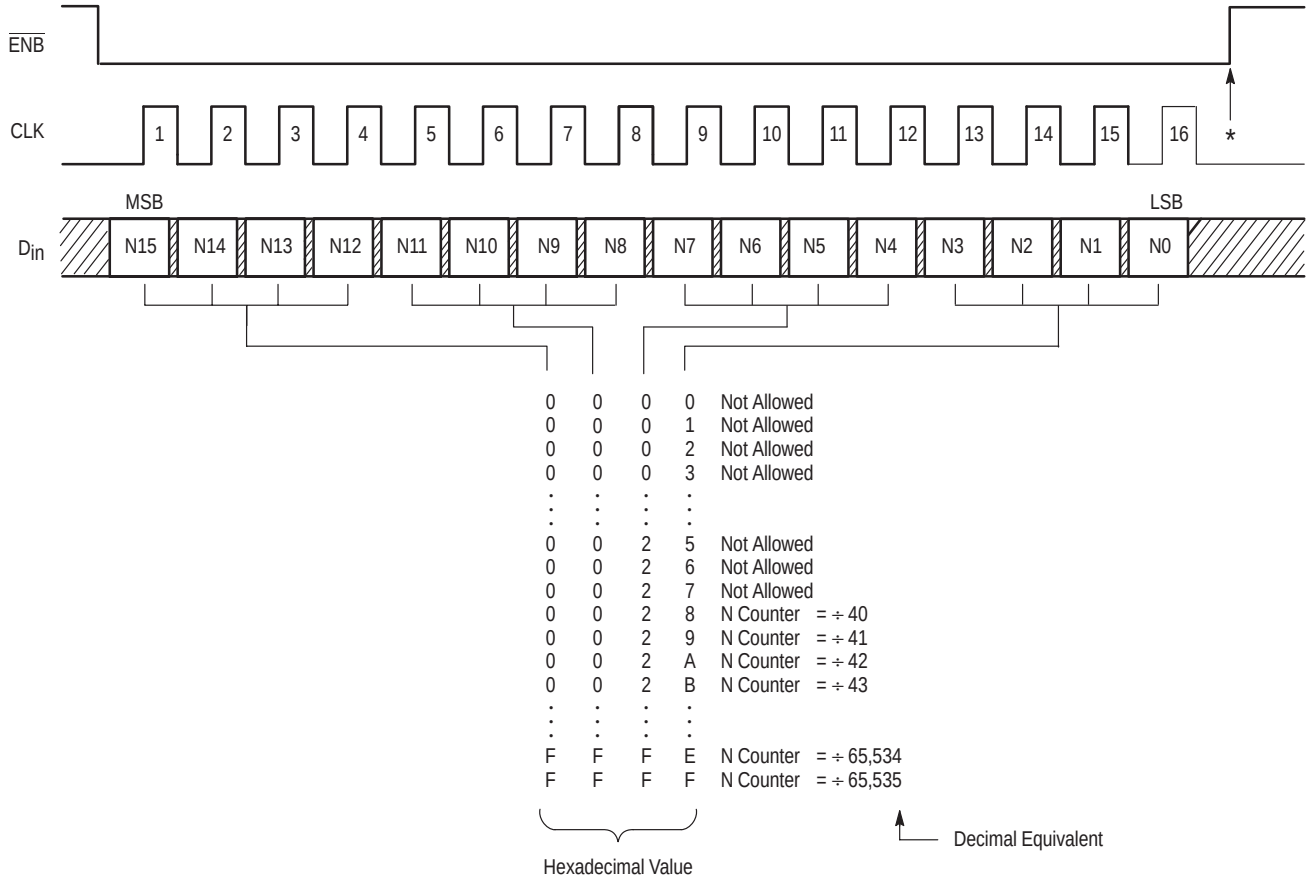
C0 — f_RE: Enables the f_R output when set high. When cleared low, the f_R output is forced to a static low level. The bit is cleared low upon power up.

Figure 15. R Register Access and Formats (Either 24 or 15 Clock Cycles Can Be Used)



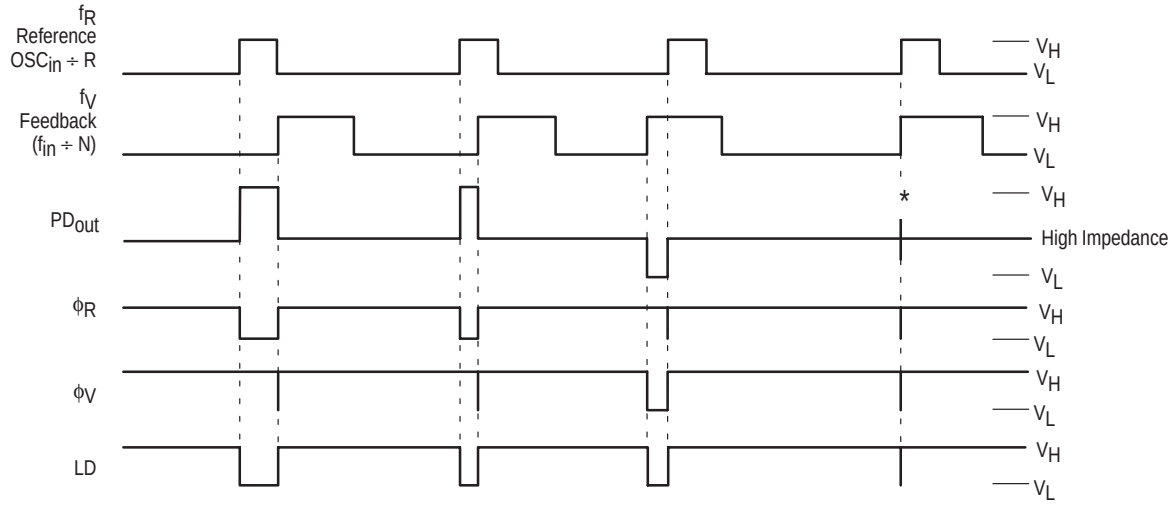
* At this point, the new data is transferred to the R register and stored. No other registers are affected.

Figure 16. N Register Access and Format (16 Clock Cycles Are Used)



* At this point, the two new bytes are transferred to the N register and stored. No other registers are affected. In addition, the N and R counters are jam–loaded and begin counting down together.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, both the sinking and sourcing output FETs are turned on for a very short interval.

NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used (see Figures 8a and 8b).

For additional information about TCXOs, visit *motorola.com* on the world wide web.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance (C_L) which does not exceed 20 pF when used at the highest operating frequencies listed in the **Loop Specifications** table. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \times C2}{C1 + C2}$$

where

C_{in} = 5.0 pF (see Figure 19)
C_{out} = 6.0 pF (see Figure 19)
C_a = 1.0 pF (see Figure 19)
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

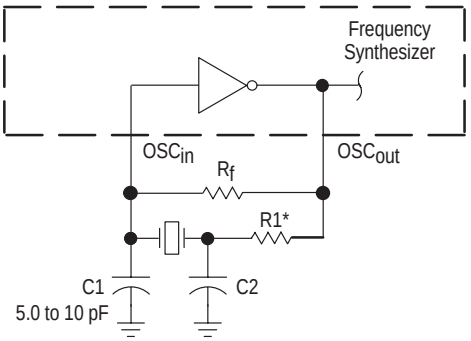
A good design practice is to pick a small value for C1, such as 5 to 10 pF. Next, C2 is calculated. C1 < C2 results in a more robust circuit for start–up and is more tolerant of crystal parameter variations.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the REF_{out} pin (OSC_{out} is not used because loading impacts the oscillator). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 2).

Figure 18. Pierce Crystal Oscillator Circuit



* May be needed in certain cases. See text.

Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}

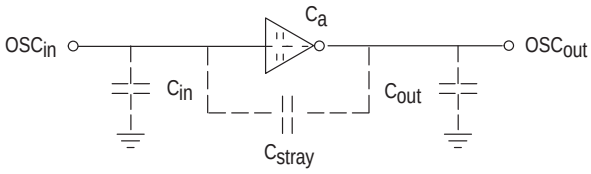
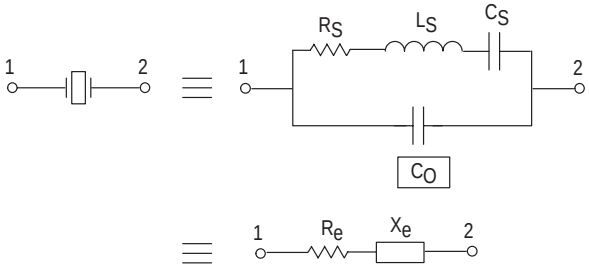


Figure 20. Equivalent Crystal Networks



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, “The Piezoelectric Crystal Unit–Definitions and Method of Measurement”, *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, “Quartz Crystals for Frequency Control”, *Electro–Technology*, June 1969.

P. J. Ottowitz, “A Guide to Crystal Selection”, *Electronic Design*, May 1966.

D. Babin, “Designing Crystal Oscillators”, *Machine Design*, March 7, 1985.

D. Babin, “Guidelines for Crystal Oscillator Design”, *Machine Design*, April 25, 1985.

See web site *mot–sps.com* for MC145170–2 control software. Select in order, Products, Wireless Semiconductor, Download, then PLL Demo Software. Choose PLLGEN.EXE.

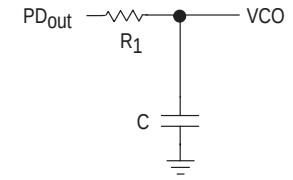
Table 2. Partial List of Crystal Manufacturers

CTS Corp.
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW PASS FILTER DESIGN

(A)

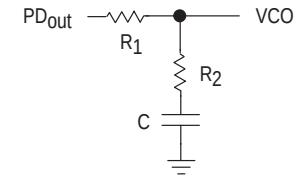


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

(B)

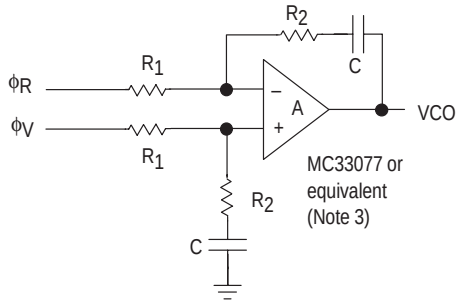


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

(C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

Assuming Gain A Is Very Large, Then:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTES:

8 For (C), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

9 The ϕR and ϕV outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp.

10 For the latest information on MC33077 or equivalent, see the Motorola Analog IC web site at *http://www.mot–sps.com/analog*.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ volts per radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ volts per radian for ϕ_V and ϕ_R

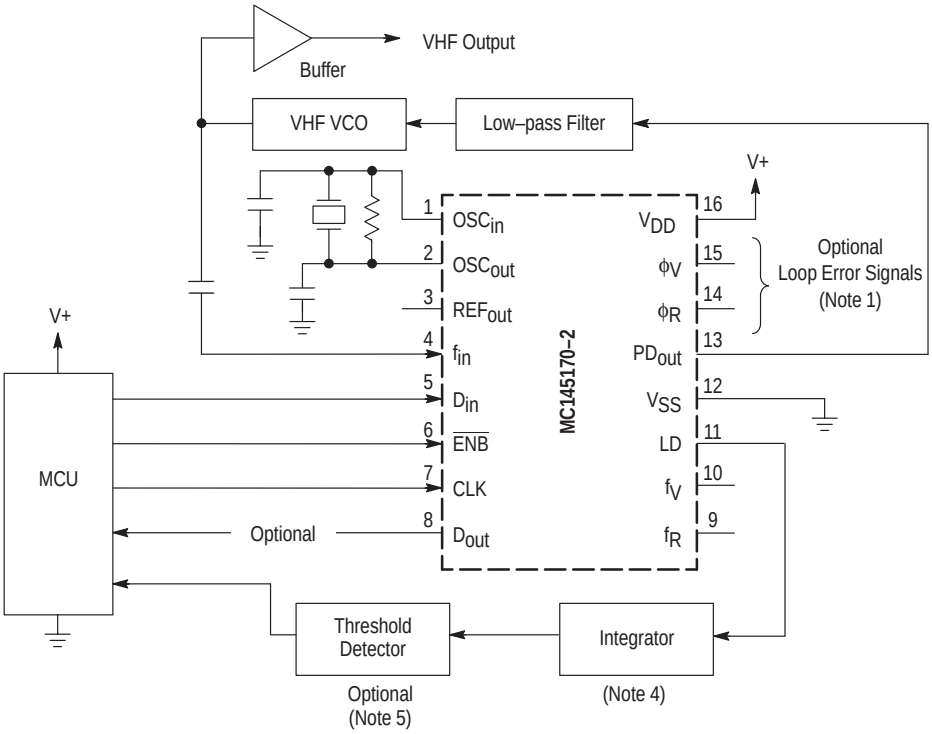
$$K_{VCO}\ (\text{VCO Gain}) = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.
AN1207, The MC145170 in Basic HF and VHF Oscillators, Motorola Semiconductor Products, Inc., 1992.
AN1671, MC145170 PSpice Modeling Kit, Motorola Semiconductor Products, Inc., 1998.

Figure 21. Example Application



NOTES:

1 The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

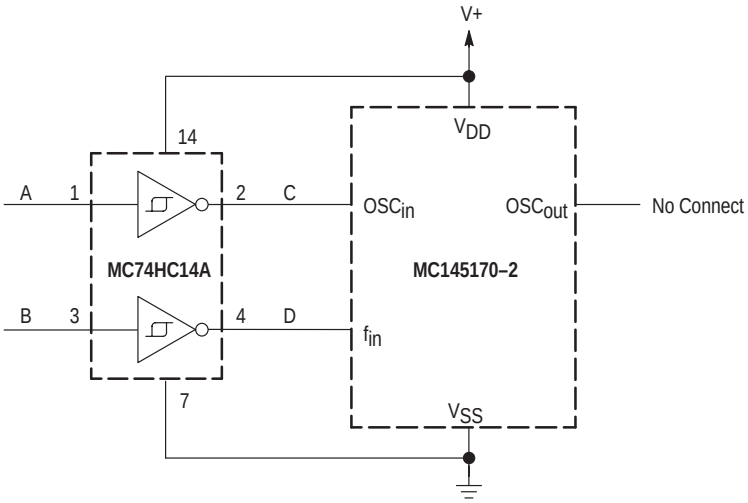
2 For optimum performance, bypass the V_{DD} pin to V_{SS} (GND) with one or more low–inductance capacitors.

3 The R counter is programmed for a divide value = OSC_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by f_R = N, where N is the divide value of the N counter.

4 May be an R–C low–pass filter.

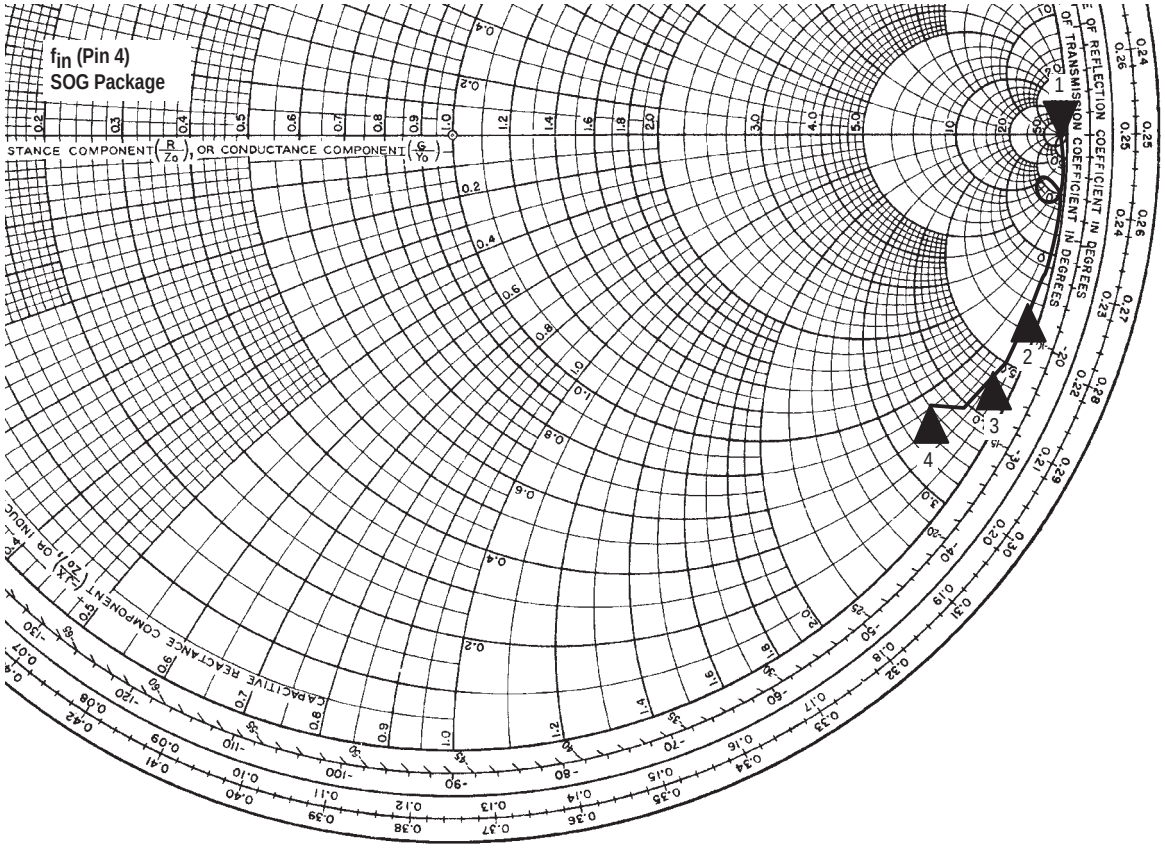
5 May be a bipolar transistor.

Figure 22. Low Frequency Operation Using dc Coupling



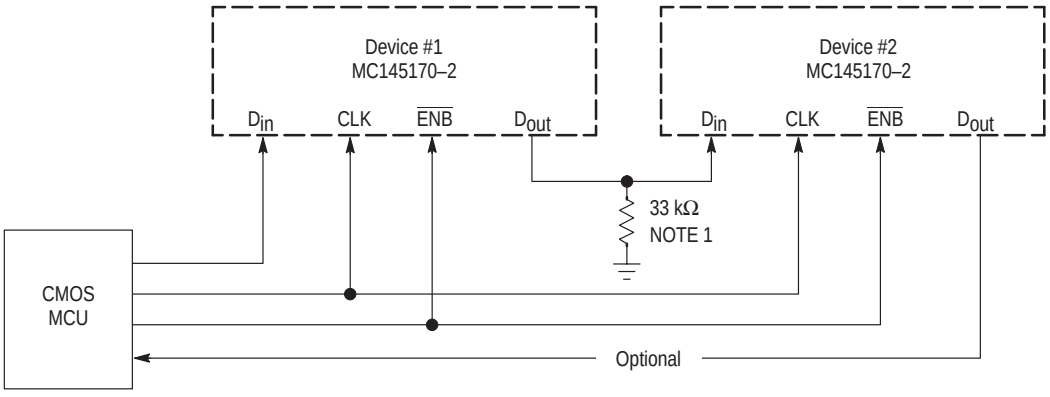
NOTE: The signals at Points A and B may be low–frequency sinusoidal or square waves with slow edge rates or noisy signal edges. At Points C and D, the signals are cleaned up, have sharp edge rates, and rail–to–rail signal swings. With signals as described at Points C and D, the MC145170–2 is guaranteed to operate down to a frequency as low as dc.
Refer to the MC74HC14A data sheet for input switching levels and hysteresis voltage range.

Figure 23. Input Impedance at f_{in} — Series Format (R + jX) (5.0 MHz to 185 MHz)



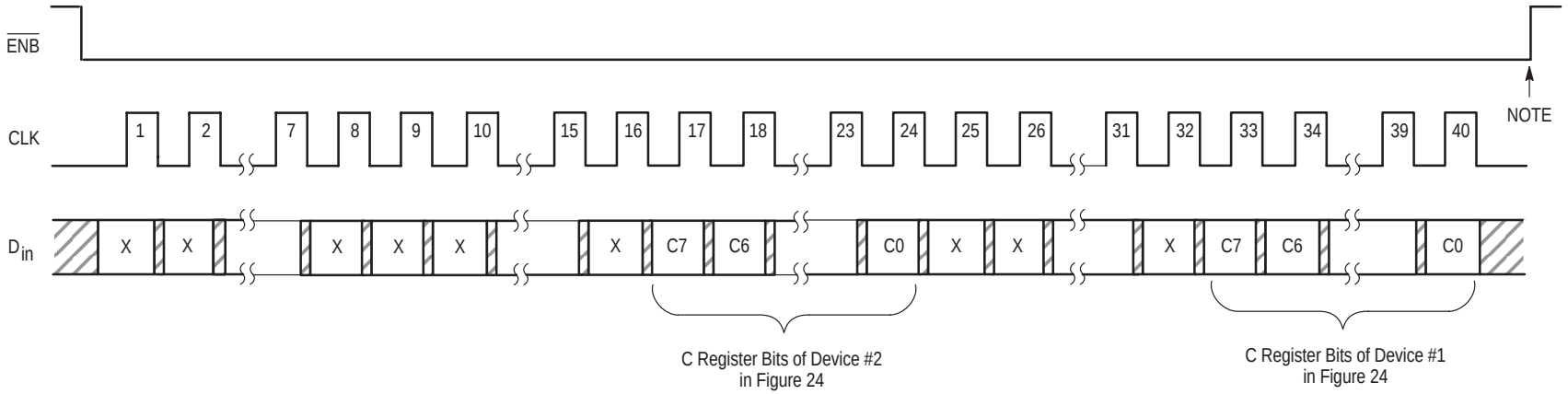
Marker	Frequency (MHz)	Resistance (Ω)	Reactance (Ω)	Capacitance (pF)
1	5	2390	– 5900	5.39
2	100	39.2	– 347	4.58
3	150	25.8	– 237	4.48
4	185	42.6	– 180	4.79

Figure 24. Cascading Two MC145170–2 Devices



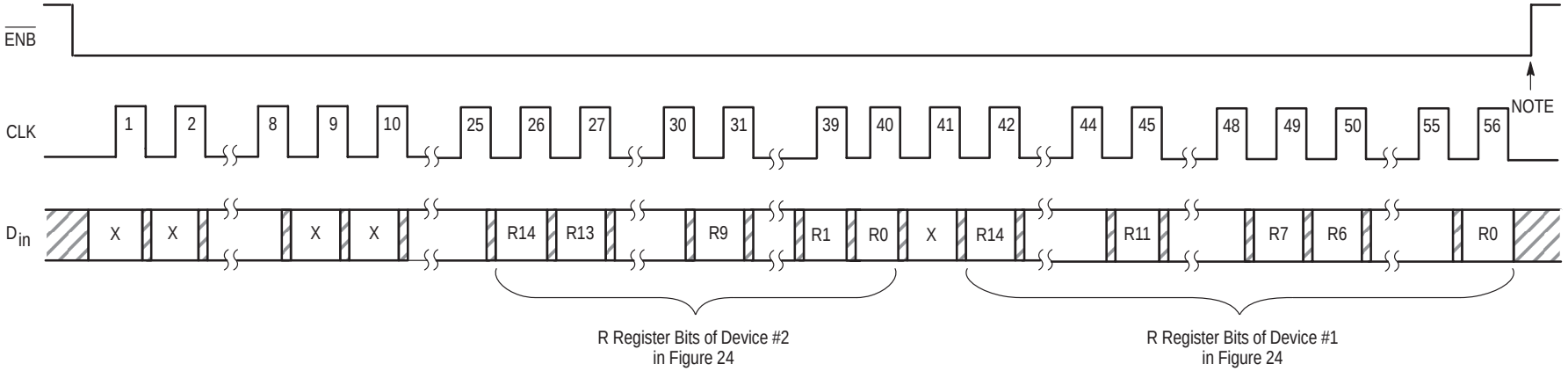
NOTES:
1 The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three–state output.)
2 See related Figures 25, 26, and 27.

Figure 25. Accessing the C Registers of Two Cascaded MC145170–2 Devices



NOTE: At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

Figure 26. Accessing the R Registers of Two Cascaded MC145170–2 Devices



NOTE: At this point, the new data is transferred to the R registers of both devices and stored. No other registers are affected.

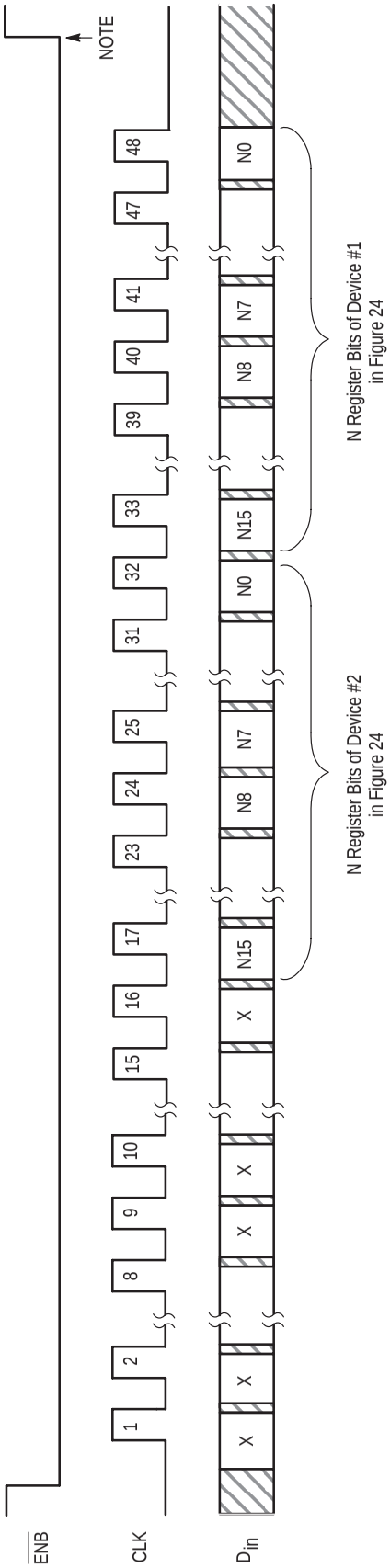
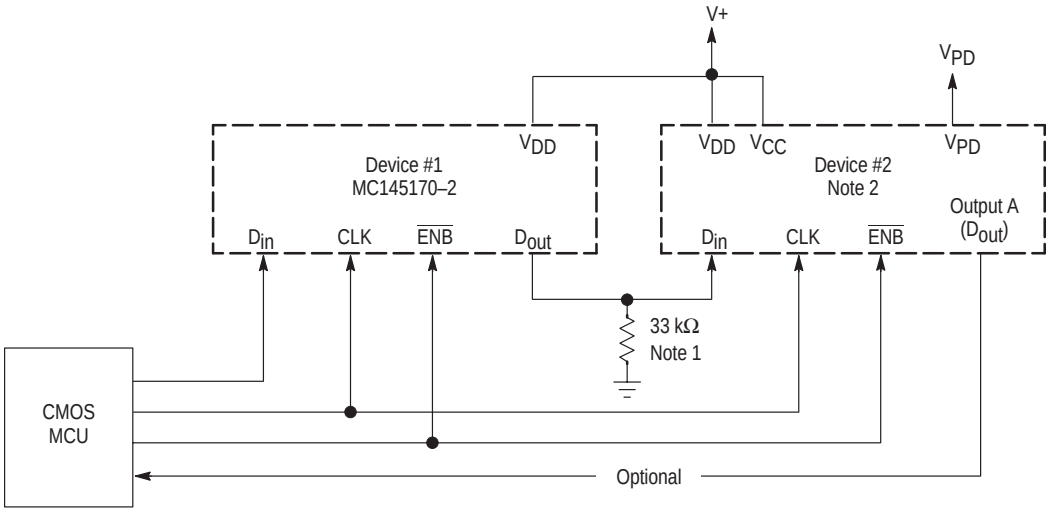


Figure 27. Accessing the N Registers of Two Cascaded MC145170–2 Devices

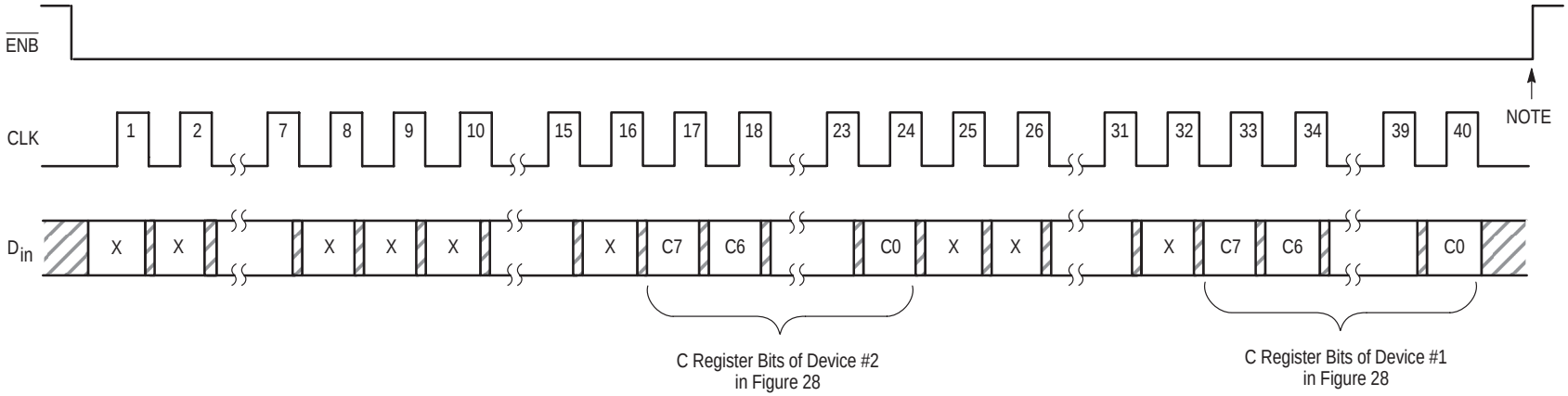
NOTE: At this point, the new data is transferred to the N registers of both devices and stored. No other registers are affected.

Figure 28. Cascading Two Different Device Types



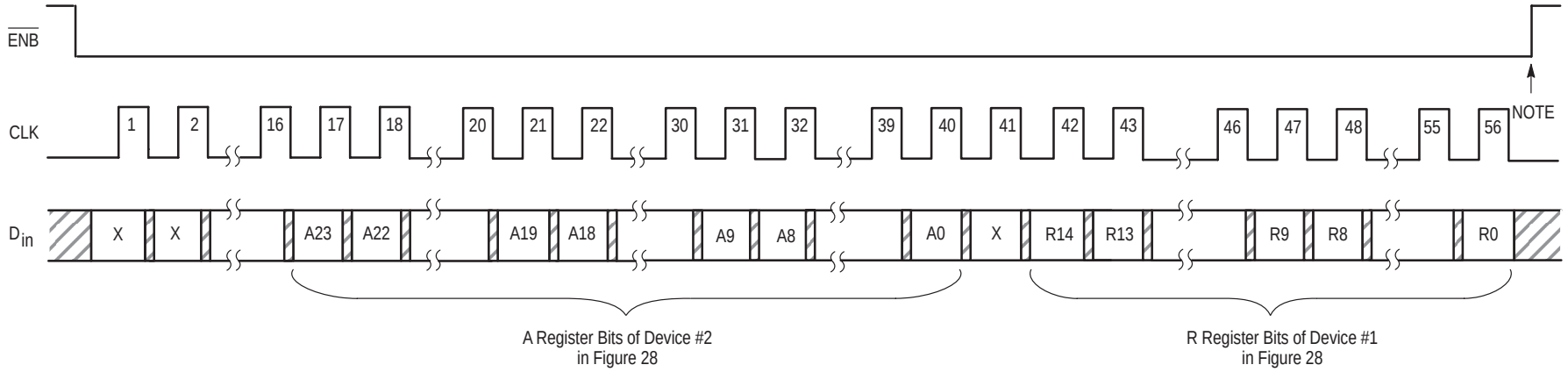
NOTES:
1 The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three–state output.)
2 This PLL Frequency Synthesizer may be a MC145190, MC145191, MC145192, MC145200, or MC145201.
3 See related Figures 29, 30, and 31.

Figure 29. Accessing the C Registers of Two Different Device Types



NOTE: At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

Figure 30. Accessing the A and R Registers of Two Different Device Types



NOTE: At this point, the new data is transferred to the A register of Device #2 and R register of Device #1 and stored. No other registers are affected.

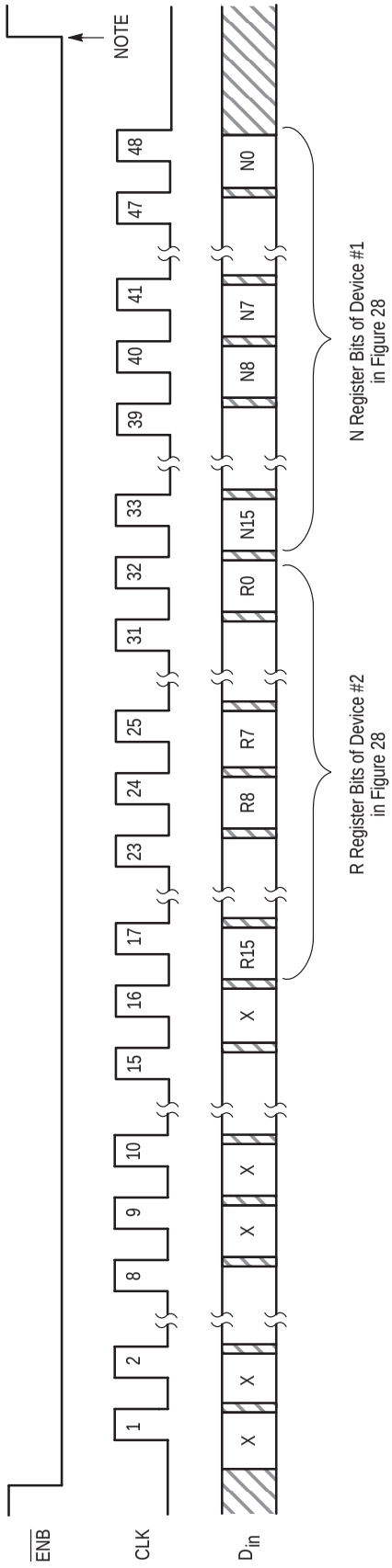


Figure 31. Accessing the R and N Registers of Two Different Device Types

NOTE: At this point, the new data is transferred to the R register of Device #2 and N register of Device #1 and stored. No other registers are affected.

MOTOROLA

Advance Information

Dual 550/60 MHz PLL Frequency Synthesizer with DACs and Voltage Multiplier

MC145181

BiCMOS COMPONENT FOR 2 OR 3 VOLT SYSTEMS

SEMICONDUCTOR TECHNICAL DATA

The MC145181 is a dual frequency synthesizer containing very–low supply voltage circuitry. The device supports two independent loops with a single input reference and operates down to 1.8 V. Phase noise reduction circuitry is incorporated into the device.

The MC145181 operates up to 550 MHz on the main loop and up to 60 MHz on the secondary loop. The device has a 32/33 prescaler for the main loop. Lock detection circuitry for both loops is multiplexed to a single output.

Two 8–bit DACs are powered through a dedicated pin. The DAC supply range is 1.8 to 3.6 V; this voltage may differ from the main supply.

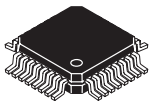
An on–chip voltage multiplier supplies power to the phase/frequency detectors. Thus, in a 2 V application, the detectors are supplied with 4 V power. In 2.6 to 3.6 V applications, the multiplied voltage is regulated at approximately 5 V. The current source/sink phase/frequency detector for the main loop is designed to achieve faster lock times than a conventional detector. Both high and low current outputs are available along with a timer, double buffers, and a MOSFET switch to adjust the external low–pass filter response.

There are several levels of standby which are controllable with a 1–byte transfer through the serial port. Either of the PLLs and/or the reference oscillator may be independently placed in the low–power standby state. In addition, any of the phase/frequency detector outputs may be placed in the floating state to facilitate modulation of the external VCOs. Either DAC may be placed in standby via a 4–byte transfer.

The MC145181 facilitates designing the receiver's first and second local oscillators for ReFLEX™ two–way paging applications. Also, the device accommodates generation of the transmit carrier.

- Operating Frequency
  Main Loop: 100 to 550 MHz
  Secondary Loop: 10 to 60 MHz
- Operating Supply Voltage: 1.8 to 3.6 V
- Nominal Supply Current, Both Loops Active: 3 mA
- Maximum Standby Current, All Systems Shut Down: 10 μA
- Phase Detector Output Current:
  1.8 V Supply — PD_{out}–Hi: 2.8 mA, PD_{out}–Lo: 0.7 mA
  ≥2.5 V Supply — PD_{out}–Hi: 4.4 mA, PD_{out}–Lo: 1.1 mA
- Two Independent 8–Bit DACs with Separate Supply Pin (Up to 3.6 V)
- Lock Detect Output with Adjustable Lock Indication Window
- Independent R Counters Allow Independent Step Sizes for Each Loop
- Main Loop Divider Range: 992 to 262,143
- Secondary Loop Divider Range: 7 to 8,191
- Fractional Reference Counters Divider Range: 20 to 32,767.5
- Auxiliary Reference Divider with Small–Signal Differential Output — Ratios: 8, 10, 12.5
- Three General–Purpose Outputs
- Direct Interface to Motorola SPI Data Port Up to 10 Mbps

ReFLEX and BitGrabber are trademarks of Motorola, Inc.



(Scale 2:1)

PLASTIC PACKAGE
CASE 873C
(LQFP–32, Tape & Reel Only)
VERY–SMALL 5 x 5 mm BODY

DEVELOPMENT SYSTEM

The MC145230EVK, which contains hardware and software, is strongly recommended for system development. (The user must provide the VCOs for evaluating the MC145181.) The software supports all features and modes of operation of the device. Up to four boards or devices can be controlled and the user is alerted to error conditions. The control program may be used with any board based on the MC145181, MC145225, or MC145230.

ORDERING INFORMATION

Device	Main/Secondary Loop Maximum Frequency	Package
MC145181FTAR2	550/60 MHz	LQFP–32

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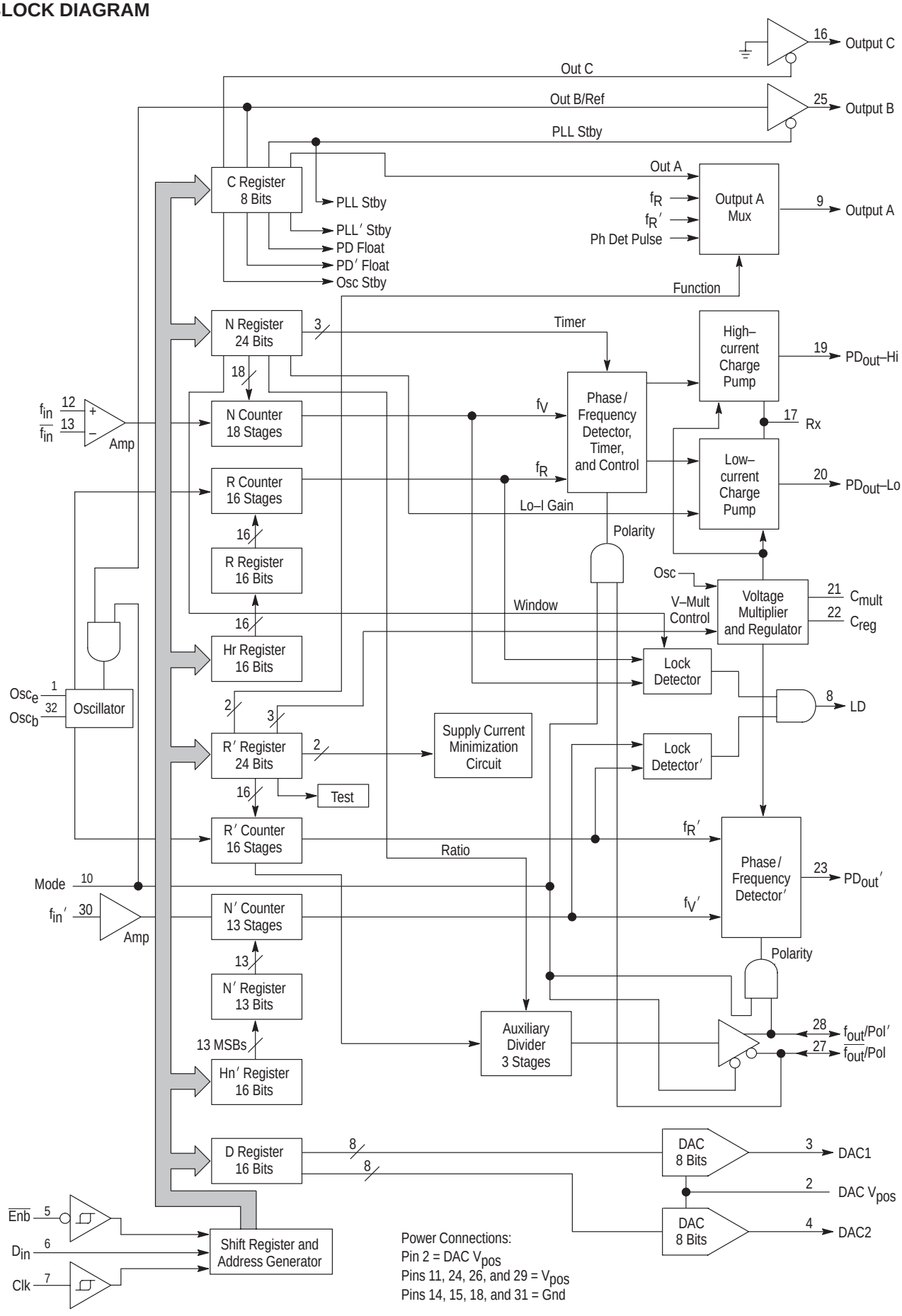
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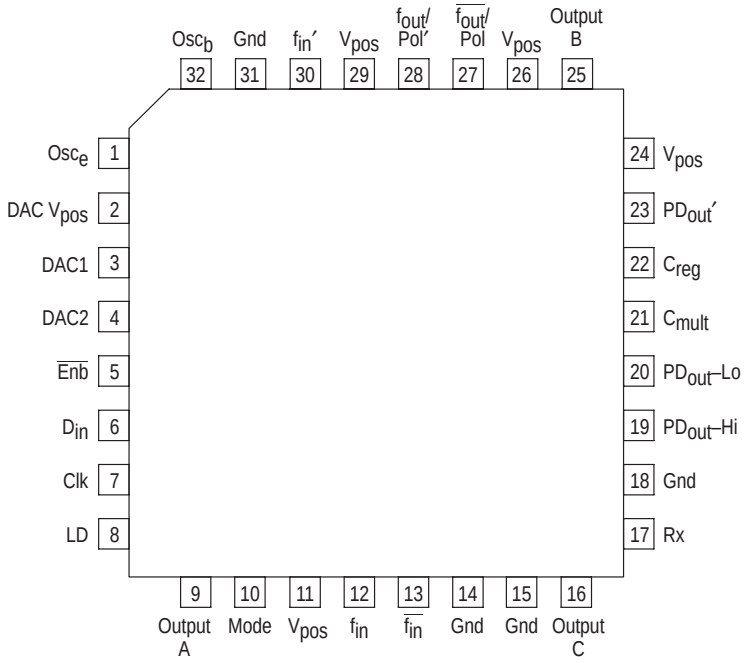
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1. BLOCK DIAGRAM



2. PIN CONNECTIONS



This device contains 15,260 active transistors.

3. PARAMETER TABLES

3A. MAXIMUM RATINGS (Voltages Referenced to Gnd, unless otherwise stated)

Parameter	Symbol	Value	Unit
DC Supply Voltages	V_{pos}, DAC V_{pos}	–0.5 to 3.6	V
DC Input Voltage — Osc_e, f_{in}, f_{in}', Mode, D_{in}, Clk, $\overline{Enb}$, f_{out}/Pol', $\overline{f_{out}}/Pol$	V_{in}	–0.5 to V_{pos} + 0.5	V
DC Output Voltage	V_{out}	–0.5 to V_{pos} + 0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
DC Output Current, per Pin	I_{out}	±20	mA
DC Supply Current, V_{pos} and Gnd Pins	I	25	mA
Power Dissipation, per Package	P_D	100	mW
Storage Temperature	T_{stg}	–65 to 150	°C
Lead Temperature, 1 mm from Case for 10 Seconds	T_L	260	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.
2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) up to 2000 V. Additional ESD data available upon request.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

3B. DC ELECTRICAL CHARACTERISTICS

V_{pos} = 1.8 to 3.6 V, Voltages Referenced to Gnd, T_A = –40 to 85°C, unless otherwise statedtt

Parameter	Condition	Symbol	Guaranteed Limit	Unit
Maximum Low–Level Input Voltage (D_{in}, Clk, $\overline{Enb}$, Mode, f_{out}/Pol', $\overline{f_{out}}/Pol$)	f_{out}/Pol' and $\overline{f_{out}}/Pol$ Configured as Inputs	V_{IL}	0.3 x V_{pos}	V
Minimum High–Level Input Voltage (D_{in}, Clk, $\overline{Enb}$, Mode, f_{out}/Pol', $\overline{f_{out}}/Pol$)	f_{out}/Pol' and $\overline{f_{out}}/Pol$ Configured as Inputs	V_{IH}	0.7 x V_{pos}	V
Minimum Hysteresis Voltage (Clk)		V_{Hys}	100	mV
Maximum Low–Level Output Voltage (LD, Output A, Output B)	I_{out} = 20 μA	V_{OL}	0.1	V
Minimum High–Level Output Voltage (LD, Output A, Output B)	I_{out} = –20 μA	V_{OH}	V_{pos} – 0.1	V
Minimum Low–Level Output Current (LD, Output A, Output B)	V_{out} = 0.3 V	I_{OL}	0.7	mA
Minimum High–Level Output Current (LD, Output A, Output B)	V_{out} = V_{pos} – 0.3 V	I_{OH}	–0.7	mA
Minimum Low–Level Output Current (Output C)	V_{out} = 0.2 V	I_{OL}	2.8	mA
Maximum Input Leakage Current (D_{in}, Clk, $\overline{Enb}$, Mode, f_{out}/Pol', $\overline{f_{out}}/Pol$)	V_{in} = V_{pos} or Gnd; f_{out}/Pol' and $\overline{f_{out}}/Pol$ Configured as Inputs	I_{in}	±1.0	μA
Maximum Output Leakage Current (Output B, Output C)	V_{out} = V_{pos} or Gnd; Output in High–Impedance State	I_{OZ}	±1	μA
Maximum ON Resistance (Output C)	1.8 V ≤ V_{pos} < 2.5 V Supply 2.5 V ≤ V_{pos} ≤ 3.6 V Supply (Note 1)	R_{on}	75 50	Ω
Maximum Standby Supply Current (V_{pos} and DAC V_{pos} Tied Together)	V_{in} = V_{pos} or Gnd; Outputs Open; Both PLLs in Standby Mode; Oscillator in Standby Mode; DAC1 and DAC2 Output = Zero; Keep–alive Oscillator Off (Notes 2, 3, and 4)	I_{STBY}	10	μA

NOTES: 1. For supply voltages restricted to 2.5 to 2.9 V and an ambient temperature range of –10 to 60°C, Output C has a guaranteed ON resistance range of 23 to 44 Ω.
2. The total supply current drain for the keep–alive oscillator, voltage multiplier, and regulator is approximately 250 μA.
3. When the Mode pin is tied high, bit C6 must be programmed to a 0 for minimum supply current drain. Otherwise, if C6 = 1, the current drain is approximately 8 μA for a 1.8 V supply and approximately 40 μA for a 3.6 V supply. This restriction on bit C6 does not apply when the Mode pin is tied low.
4. To ensure minimum standby supply current drain, the voltage potential at the C_{mult} pin must not be allowed to fall below the potential at the V_{pos} pins. See discussion in Section 5E under **C_{mult}**.

3C. PD_{out}–Hi AND PD_{out}–Lo PHASE/FREQUENCY DETECTOR CHARACTERISTICS

Nominal Output Current, V_{pos} = 1.8 V: PD_{out}–Hi = 2.8 mA, PD_{out}–Lo = 0.7 or 0.35 mA
Nominal Output Current, V_{pos} ≥ 2.5 V: PD_{out}–Hi = 4.4 mA, PD_{out}–Lo = 1.1 or 0.55 mA
Rx = 2.0 kΩ, Voltages Referenced to Gnd, Voltage Multiplier ON, T_A = –40 to 85°C

Parameter	Condition	Guaranteed Limit	Unit
Maximum Source Current Variation Part–to–Part (See Note)	V_{out} = 0.5 x V_{Cmult}	±14	%
Maximum Sink–versus–Source Mismatch (See Note)	V_{out} = 0.5 x V_{Cmult}	20	%
Output Voltage Range (See Note)	I_{out} Variation ≤ 27%	0.6 to V_{Cmult} – 0.6 V	V
Maximum Three–State Leakage Current	V_{out} = 0 or V_{Cmult}	±50	nA

NOTE: Percentages calculated using the following formula: (Maximum Value – Minimum Value) / Maximum Value.

3D. PD_{out}' PHASE/FREQUENCY DETECTOR CHARACTERISTICS

V_{pos} = 1.8 to 3.6 V, Voltages Referenced to Gnd, Voltage Multiplier ON, T_A = –40 to 85°C

Parameter	Condition	Guaranteed Limit	Unit
Minimum Low–Level Output Current	V_{out} = 0.3 V	0.3	mA
Minimum High–Level Output Current	V_{out} = V_{Cmult} – 0.3 V	–0.3	mA
Maximum Three–State Leakage Current	V_{out} = 0 or V_{Cmult}	±50	nA

3E. DAC CHARACTERISTICS

V_{pos} = 1.8 to 3.6 V, DAC V_{pos} = 1.8 to 3.6 V; T_A = –40 to 85°C

Parameter	Condition	Guaranteed Limit	Unit
Resolution		8	Bits
Maximum Integral Nonlinearity		±1	LSB
Maximum Offset Voltage from Gnd	No External Load	1	LSB
Maximum Offset Voltage from DAC V_{pos}	No External Load	2	LSB
Maximum Output Impedance	Over Entire Output Range, Including Zero Output (which is Low–power Standby)	130	kΩ
Maximum Standby Current	Zero Output, No External Load	(See I_{STBY} in Section 3B)	
Maximum Supply Current per DAC @ DAC V_{pos} pin	Except with Zero Output, No External Load	(DAC V_{pos}) / 36	mA

3F. VOLTAGE MULTIPLIER AND KEEP–ALIVE OSCILLATOR CHARACTERISTICS

Voltages Referenced to Gnd, T_A = –40 to 85°C

Parameter	Condition	Guaranteed Limit	Unit
Voltage Multiplier Output Voltage	5 MHz Refresh Rate, 100 μA Continuous Sourcing, Measured at C_{mult} pin V_{pos} = 1.8 V V_{pos} = 3.6 V	 3.32 to 3.78 4.75 to 5.35	V
Keep–alive Refresh Frequency	V_{pos} = 1.8 to 3.6 V	300 to 700	kHz

3G. DYNAMIC CHARACTERISTICS OF DIGITAL PINS

V_{pos} = 1.8 to 3.6 V, T_A = –40 to 85°C, Input $t_r = t_f$ = 10 ns, C_L = 25 pF

Parameter	Figure No.	Symbol	Guaranteed Limit	Unit
Serial Data Clk Frequency NOTE: Refer to Clk t_w Below	1	f_{clk}	dc to 10	MHz
Maximum Propagation Delay, $\overline{Enb}$ to Output A (Selected as General–Purpose Output)	2, 7	t_{PLH}, t_{PHL}	200	ns
Maximum Propagation Delay, $\overline{Enb}$ to Output B	2, 3, 7, 8	t_{PLH}, t_{PHL}, t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}	200	ns
Maximum Propagation Delay, $\overline{Enb}$ to Output C	4, 8	t_{PZL}, t_{PLZ}	200	ns
Maximum Output Transition Time, Output A; Output B with Active Pullup and Pulldown	2, 7	t_{TLH}, t_{THL}	75	ns
Minimum Setup and Hold Times, D_{in} versus Clk	5	t_{su}, t_h	30	ns
Minimum Setup, Hold, and Recovery Times, $\overline{Enb}$ versus Clk	6	t_{su}, t_h, t_{rec}	100	ns
Minimum Pulse Width, Inactive (High) Time, $\overline{Enb}$	6	t_w	*	cycles
Minimum Pulse Width, Clk	1	t_w	50	ns
Maximum Input Capacitance — D_{in}, CLK, $\overline{Enb}$		C_{in}	10	pF

*For Hr register access, the minimum limit is 20 Osc_e cycles.
For Hn′ register access, the minimum limit is 27 f_{in}′ cycles.
For N register access, the minimum limit is 20 Osc_e cycles + 99 f_{in} cycles.
When the timer is used for adapt, the minimum limit after the second N register access and before the next register access is the time–out interval + 99 f_{in} cycles.

Figure 1.

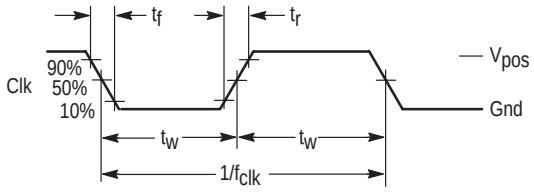


Figure 2.

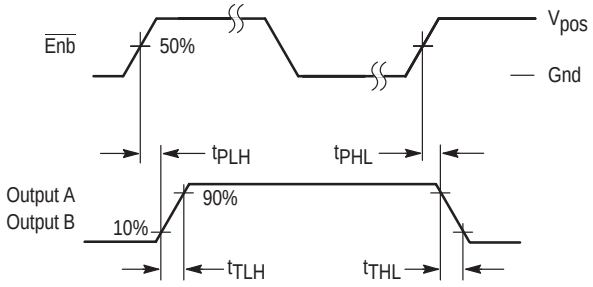


Figure 3.

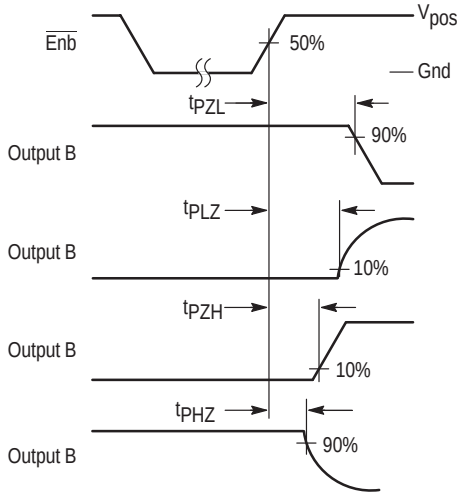


Figure 4.

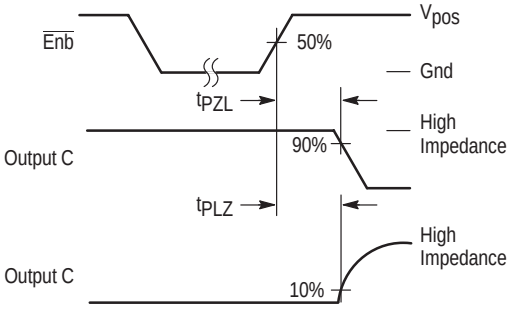


Figure 5.

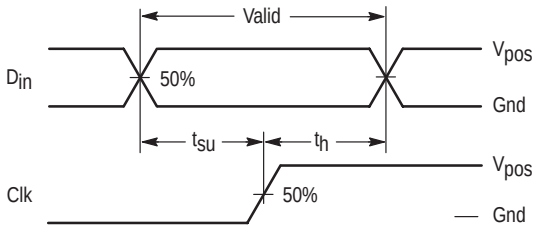


Figure 6.

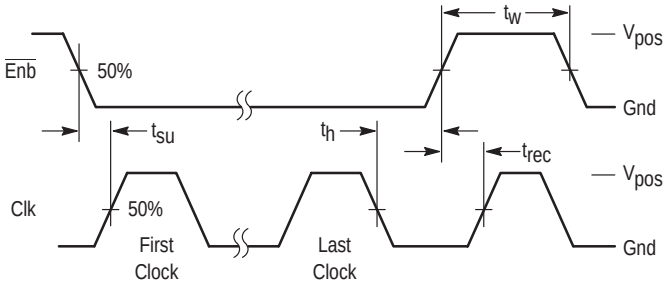
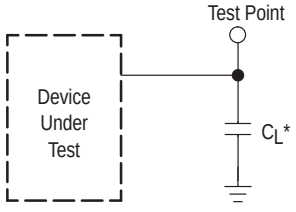
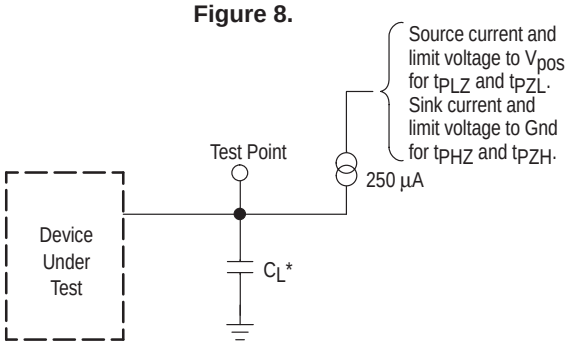


Figure 7.



* Includes all probe and fixture capacitance.

Figure 8.



* Includes all probe and fixture capacitance.

3H. DYNAMIC CHARACTERISTICS OF LOOP AND f_{out} PINS

V_{pos} = 1.8 to 3.6 V, T_A = –40 to 85°C

Symbol	Parameter	Condition	Figure No.	Min	Max	Unit
v_{in}	Input Voltage Range, f_{in}	100 MHz ≤ f_{in} < 550 MHz	9	100	300	mVpp
v_{in}'	Input Voltage Range, f_{in}'	10 MHz ≤ f_{in} < 60 MHz	10	100	400	mVpp
f_{Osce}	Input Frequency Range, Osc_e	v_{in} = 350 to 600 mVpp, Device in External Reference Mode	11	9	80	MHz
f_{Xtal}	Crystal Frequency, Osc_b and Osc_e	Device in Crystal Mode	*	9	80	MHz
C_{in}	Input Capacitance of Pins Osc_b and Osc_e			—	—	pF
f_{out}	Output Frequency Range, f_{out} and $\overline{f_{out}}$	Output Signal Swing > 300 mVpp per pin (600 mVpp differential)	12	1	6.2	MHz
f_ϕ	Operating Frequency Range of the Phase/Frequency Detectors, PD_{out}–Hi, PD_{out}–Lo, PD_{out}'			dc	600	kHz

*Refer to the **Crystal Oscillator Considerations** section.

Figure 9.

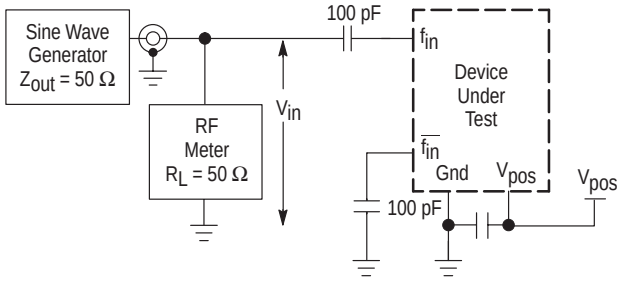


Figure 10.

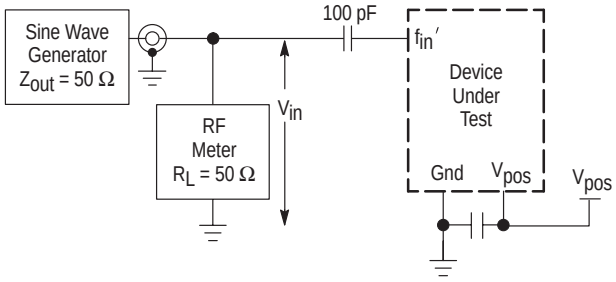


Figure 11.

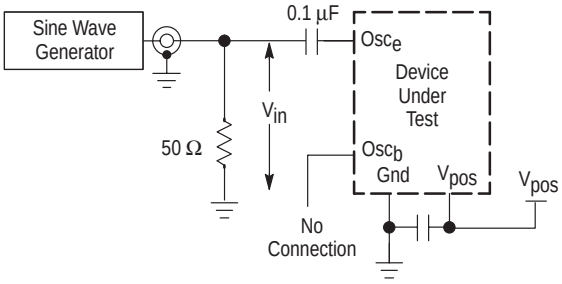
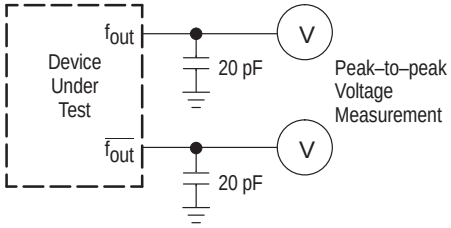


Figure 12.



4. DEVICE OVERVIEW

Refer to the Block Diagram in Section 1.

4A. SERIAL INTERFACE AND REGISTERS

The serial interface is comprised of a Clock pin (Clk), a Data In pin (D_{in}), and an Enable pin ($\overline{Enb}$). Information on the data input pin is shifted into a shift register on the low–to–high transition of the serial clock. The data format is most significant bit (MSB) first. Both Clk and $\overline{Enb}$ are Schmitt–triggered inputs.

The R and N registers contain counter divide ratios for the main loop, PLL. The R′ and N′ registers contain counter divide ratios for the secondary loop, PLL′. Additional contol bits are located in the R′, N, and C registers. The D register controls the digital–to–analog converters (DACs). Random access is allowed to the N, R′, Hr, Hn′, D, and C registers.

Two 16–bit holding registers, Hr and Hn′, feed registers R and N′, respectively. [The three least significant bits (LSBs) of the Hn′ register are not used.] The R and N′ registers determine the divide ratios of the R and N′ counters, respectively. Thus, the information presented to the R and N′ counters is double–buffered. Using the proper programming sequence, new divide ratios may be presented to the N, R, and N′ counters; simultaneously.

$\overline{Enb}$ is used to activate the data port and allow transfer of data. To ensure that data is accepted by the device, the $\overline{Enb}$ signal line must initially be a high voltage (not asserted), then make a transition to a low voltage (asserted) prior to the occurrence of a serial clock, and must remain asserted until after the last serial clock of the burst. Serial data may be transferred in an SPI format (while $\overline{Enb}$ remains asserted). Data is transferred to the appropriate register on the rising edge of $\overline{Enb}$ (see Table 1). “Short shifting”, depicted as BitGrabber™ in the table, allows access to certain registers without requiring address bits. When $\overline{Enb}$ is inactive (high), Clk is inhibited from shifting the shift register.

The serial input pins may NOT be driven above the supply voltage applied to the V_{pos} pins.

4B. REFERENCE INPUT AND COUNTERS CIRCUITS

Reference (Oscillator) Circuit

For the Colpitts reference oscillator, one pin ties to the base (Osc_b, pin 32) and the other ties to the emitter (Osc_e, pin 1), of an on–chip NPN transistor. In addition, the reference circuit may be operated in the external reference (XRef) mode as selectable via bit C6 when the Mode pin is high.

The Osc_b and Osc_e pins support an external fundamental or overtone crystal. The output of the oscillator is routed to both the reference counter for the main loop (R counter) and the reference counter for the secondary loop (R′ counter).

In a second mode, determined by bit C6 being 1 and the Mode pin being high, Osc_e is an input which accepts an ac–coupled signal from a TCXO or other source. Osc_b must be floated. If the Mode pin is low, this “XRef mode” is not allowed.

Reference Counter for Main Loop

Main reference counter R divides down the frequency at Osc_e and feeds the phase/frequency detector for the main loop. The detector feeds the two charge pumps with outputs PD_{out}–Hi and PD_{out}–Lo. The division ratio of the R counter is determined by bits in the R register.

Reference Counter for Secondary Loop

Secondary reference counter R′ divides down the frequency at Osc_e and feeds the phase/frequency detector for the secondary loop. The detector output is PD_{out}′. The division ratio of the R′ counter is determined by the 16 LSBs of the R′ register.

The R′ counter has a special mode to provide a frequency output at pins f_{out} and $\overline{f_{out}}$ (differential outputs). These are low–jitter ECL–type outputs. With the Mode pin low, software control allows the Osc_e frequency to be divided–by–8, –10, or –12.5 and routed to the f_{out} pins. This output is derived by tapping off of a front–end stage of the R′ counter and feeding the auxiliary counter which provides the divided–down frequency. The chip must have the Mode pin low, which activates the f_{out} pins. The actual R′ divide ratio must be divisible by 2 or 2.5 when the f_{out} pins are activated. There is no such restriction when the Mode pin is high. See Section 6D, **R′ Register.**

4C. LOOP DIVIDER INPUTS AND COUNTER CIRCUITS

f_{in} Inputs and Counter Circuit

f_{in} and $\overline{f_{in}}$ are high–frequency inputs to the amplifier which feeds the N counter. A small signal can feed these inputs either differentially or single–ended.

The N counter divides down the external VCO frequency for the main loop. (The divide ratio of the N counter is also known as the loop multiplying factor.) The divide ratio of this counter is determined by the 18 LSBs of the N register. The output of the N counter feeds the phase/frequency detector for the main loop.

f_{in}′ Input and Counter Circuit

f_{in}′ is the high–frequency input to the amplifier which feeds the N′ counter. A small signal can feed this input single–ended.

The N′ counter divides down the external VCO frequency for the secondary loop. (The divide ratio of the N′ counter is also known as the loop multiplying factor.) The divide ratio of this counter is determined by bits in the N′ register. The output of the N′ counter feeds the phase/frequency detector for the secondary loop.

4D. VOLTAGE MULTIPLIER AND KEEP–ALIVE CIRCUITS

The voltage multiplier produces approximately two times the voltage present at the V_{pos} pins over a supply range of 1.8 V to about 2.5 V. With a supply range of approximately 2.5 V to 3.6 V, the elevated voltage is regulated/limited to approximately 5 V. The elevated voltage, present at the C_{mult}

pin, is applied to both phase detectors. An external capacitor to Gnd is required on the C_{mult} pin. The other capacitors required for the multiplier are on–chip.

A capacitor to Gnd is also required on the C_{reg} pin. The voltage on this pin is equal to the voltage on the V_{pos} pins over a supply range of 1.8 V to about 2.5 V. The voltage on C_{reg} is limited to approximately 2.5 V maximum when the V_{pos} pins exceed 2.5 V.

The refresh rate determines the repetition rate that the capacitors for the voltage multiplier are charged. Refresh is normally derived off of the signal present at the Osc_e pin, through a divider which is part of the voltage multiplier and regulator circuitry. The refresh rate is controlled via bits in the R′ register.

When the reference oscillator circuit is placed in standby, an on–chip keep–alive oscillator assists in maintaining the elevated voltage on the phase detectors. The keep–alive refresh rate is per the spec table in Section 3F.

If desired, the keep–alive oscillator can be inhibited from turning on, by placing the multiplier in the inactive state via R′ register bits. This causes the phase/frequency detector voltage to bleed off while in standby, but has the advantage of achieving the lowest supply current if all other sections of the chip are shut down.

4E. PHASE/FREQUENCY DETECTORS

Detector for Main Loop

The detector for the main loop senses the phase and frequency difference between the outputs of the R and N counters. The detector feeds both a high–current charge pump with output PD_{out}–Hi and a low–current charge pump with output PD_{out}–Lo.

The charge pumps can be operated in three conventional manners as controlled by bits in the N register. PD_{out}–Lo can be enabled with PD_{out}–Hi inhibited. Conversely, PD_{out}–Hi can be enabled with PD_{out}–Lo inhibited. Both outputs can be enabled and tied together externally for maximum charge pump current. Finally, both outputs can be inhibited. In this last case, they float. The outputs can also be forced to the floating state by a bit in the C register. This facilitates introduction of modulation into the VCO input.

The charge pumps can be operated in an adapt mode as controlled by bits in the N register. The bits essentially program a timer which determines how long PD_{out}–Hi is active. After the time–out, PD_{out}–Hi floats and PD_{out}–Lo becomes active. In addition, a second set of R and N counter values can be engaged after the time–out. For more information, see Table 16 and Section 8, **Programmer's Guide**.

Detector for Secondary Loop

The detector for the secondary loop senses the phase and frequency difference between the outputs of the R′ and N′ counters. Detector output PD_{out}′ is a voltage–type output with a three–state push–pull driver.

The output can be forced to the floating state by a bit in the C register. This facilitates introduction of modulation into the VCO input.

4F. LOCK DETECTORS

Window counters in each of the lock detector circuits determine the lock detector phase threshold for PLL and PLL′. The window counter divide ratio for the main loop's lock detector is controlled via a bit in the N register. The window counter divide ratio for the secondary loop is not controllable by the user.

The lock detector window determines a minimum phase difference which must occur before the Lock Detect pin goes high. Note that the lock detect signals for each loop drive an AND gate, which then feeds the LD pin. The LD pin indicates the condition of both loops, or the one active loop if the other is in standby. If both loops are in standby, LD is low indicating unlocked.

4G. DACs

The two independent 8–bit DACs facilitate crystal oscillator trimming and PA output power control. They are also suitable for any general–purpose use.

Each DAC utilizes an R–2R ladder architecture. The output pins, DAC1 and DAC2, are directly connected to the ladder; that is, there is no on–chip buffer.

The DAC outputs are determined by the contents of the D register. When a DAC output is zero scale, it is also in a low–power mode. The power–on reset (POR) circuit initializes the DACs in the low–power mode upon power up.

4H. GENERAL–PURPOSE OUTPUTS

There are three outputs which may be used as port expanders for a microcontroller unit (MCU).

Output A is actually a multi–purpose output with a push–pull output driver. See Table 2 for details.

Output B is a three–state output. The state of Output B depends on two bits; one of these bits also controls whether the main PLL is in standby or not. See Table 5 for details.

Output C is an open–drain output. The state of this output is controlled by one bit per Table 4. Output C is specified with a guaranteed ON resistance, and thus, may be used in an analog fashion.

5. PIN DESCRIPTIONS

5A. DIGITAL PINS

$\overline{Enb}$, D_{in}, and Clk
Pins 5, 6, and 7 — Serial Data Port Inputs

The $\overline{Enb}$ input is used to activate the serial interface to allow the transfer of data to the device. To transfer data to the device, the $\overline{Enb}$ pin must be low during the interval that the data is being clocked in. When $\overline{Enb}$ is taken back high (inactive), data is transferred to the appropriate register depending either on the data stream length or address bits. The C, Hr, and N registers can be accessed using either a unique data stream length (BitGrabber) or by using address bits (Conventional). The D, Hn′, and R′ registers can only be accessed using address bits. See Table 1.

The bit stream begins with the MSB and is shifted in on the low–to–high transition of Clk. The bit pattern is 1 byte (8 bits) long to access the C register, 2 bytes (16 bits) to access the Hr register, or 3 bytes (24 bits) to access the N register. A bit pattern of 4 bytes (32 bits) is used to access the registers when using address bits. The device has double buffers for storage of the N′ and R counter divide ratios. One double buffer is composed of the Hr register which feeds the R register. An Hr to R register transfer occurs whenever the N register is written. The other double buffer is the Hn′ register which feeds the N′ register. An Hn′ to N′ register transfer occurs whenever the N register is written. Thus, new divide ratios may be presented to the R, N′, and N counters simultaneously.

Transitions on $\overline{Enb}$ must not be attempted while Clk is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs whenever $\overline{Enb}$ is high (inactive) and Clk is low.

Data is retained in the registers over a supply range of 1.8 to 3.6 V. The bit–stream formats are shown in Figures 13 through 18.

LD
Pin 8 — Lock Detectors Output

This signal is the logical AND of the lock detect signals from both PLL and PLL′. For the main PLL, the phase window that defines “lock” is programmable via bit N22. The phase window for the secondary PLL′ is not programmable.

If either PLL or PLL′ is in standby, LD indicates the lock condition of the active loop only. If both loops are in standby, the LD output is a static low level.

Each PLL’s lock detector is in the high state when the respective loop is locked (the inputs to the phase detector being the same phase and frequency). The lock detect signal is in the low state when a loop is out of lock. See Figure 19.

Upon power up, the LD pin indicates a *not locked* condition. The LD pin is a push–pull CMOS output. If unused, LD should be left open.

Output A
Pin 9 — Multiple–Purpose Digital Output

Depending on control bits R′21 and R′20, Output A is selectable by the user as a general–purpose output (either high or low level), f_R (output of main reference counter), $f_{R'}$ (output of secondary reference counter), or a phase detector pulse indicator for both loops. When selected as general–purpose output, bit C7 determines whether the output is a high or low level per Table 2. When configured as f_R, $f_{R'}$, or phase detector pulse, Output A appears as a normally low signal and pulses high.

Output A is a slew–rate limited CMOS totem–pole output. If unused, Output A should be left open.

Table 1. Register Access
(LSBs are C0, R0, N0, D0, R′0, and N′0)

Access Type	Accessed Register	Address Nibble	Number of Clocks	Register Bit Nomenclature	Figure No.
BitGrabber	C	—	8	C7, C6, C5, ..., C0	13
BitGrabber	Hr	—	16	R15, R14, R13, ..., R0	14
BitGrabber	N	—	24	N23, N22, N21, ..., N0	15
Conventional	C	$0	32	C7, C6, C5, ..., C0	13
Conventional	Hr	$1	32	R15, R14, R13, ..., R0	14
Conventional	N	$2	32	N23, N22, N21, ..., N0	15
Conventional	D	$3	32	D15, D14, D13, ..., D0	18
Conventional	R′	$5	32	R′23, R′22, R′21, ..., R′0	16
Conventional	Hn′	$4	32	N′15, N′14, N′13, ..., N′0	17

NOTE: $0 denotes hexadecimal zero, $1 denotes hexadecimal one, etc.

Table 2. Output A Configuration

Bit R′21	Bit R′20	Bit C7	Function of Output A
0	0	0	General–Purpose Output, Low Level
0	0	1	General–Purpose Output, High Level
0	1	x	f_R
1	0	x	$f_{R'}$
1	1	x	Phase Detector Pulse Indicator

Mode
Pin 10 — Mode Input

When the Mode pin is tied low (approximately Gnd), the pair of pins named f_{out}/Pol′ and $\overline{f_{out}}$/Pol become outputs f_{out} and $\overline{f_{out}}$. As such, these pins are the divided down reference frequency. The division ratio is controlled by bits per Table 6. In addition, when Mode is low, the R′ counter is preceded by a fixed–divide prescaler. Also, only a crystal may be used at pins Osc_b and Osc_e; an external reference, such as a TCXO, should not be used to drive either pin. The default on the phase detector polarity is positive. See the summary in Table 3.

When the Mode pin is tied high (approximately V_{pos}), the pair of pins named f_{out}/Pol′ and $\overline{f_{out}}$/Pol become inputs Pol′ and Pol. As such, these pins control the polarity of the phase/frequency detectors for PLL′ and PLL, respectively. In addition, when Mode is high, the R′ counter is preceded by a dual–modulus prescaler. Therefore, the R′ counter is completely programmable per Figure 16. Also, either a crystal or TCXO may be used with the device. See the summary in Table 3.

Table 3. Mode Pin Summary

Attribute	Mode Pin = Low Level	Mode Pin = High Level
f_{out}/Pol′ pin	Pin is f_{out} output; polarity of phase detector′ is positive	Pin is Pol′ input and controls polarity of phase detector′
$\overline{f_{out}}$/Pol pin	Pin is $\overline{f_{out}}$ output; polarity of phase detector is positive	Pin is Pol input and controls polarity of phase detector
Oscillator circuit	Supports a crystal only	Supports crystal or accommodates TCXO
R′ counter	Programmable in increments of 2 or 2.5	Programmable in increments of 0.5
Output B pin	State of pin controlled by Bit C6	Pin not used, Bit C6 controls whether crystal or TCXO is accommodated

Output C
Pin 16 — General–Purpose Digital Output

This pin is controllable by bit C5 as either low level or high impedance per Table 4.

The output driver is an open–drain N–channel MOSFET connected to Gnd. The ESD (electrostatic discharge) protection circuit for this pin is tied to Gnd and V_{pos}. Thus, voltages above V_{pos} are clipped at approximately 0.7 V above V_{pos}. If unused, Output C should be left open.

Table 4. Output C Programming

Bit C5	State of Output C Pin
0	Low level (ON resistance per Electrical Table)
1	High impedance (leakage per Electrical Table)

Output B
Pin 25 — General–Purpose Digital Output

This pin is controllable by bits C6 and C1 as either low level, high level, or high impedance per Table 5. Note that whenever the main PLL is placed in standby by bit C1, Output B is forced to high impedance. The three–state MOSFET output is slew–rate limited. If unused, Output B should be left open.

Table 5. Output B Programming

Bit C6	Bit C1	State of Output B Pin	Condition of Main PLL
0	0	Low level	Active
0	1	High impedance*	Standby*
1	0	High level	Active
1	1	High impedance	Standby

*Power–up default.

f_{out}/Pol′ and $\overline{f_{out}}$/Pol
Pins 28 and 27 — Dual–purpose Outputs/Inputs

These pins are outputs when the Mode pin is low and inputs when the Mode pin is high.

When the Mode pin is low, these pins are small–signal differential outputs f_{out} and $\overline{f_{out}}$ with a frequency derived from the signal present at the Osc_e pin. The frequency of the output signal is per Table 6. If this function is not needed, the Mode pin should be tied high, which minimizes supply current. In this case, these inputs must be tied high or low per Tables 7 and 8.

Table 6. f_{out} and $\overline{f_{out}}$ Frequency
(Mode Pin = Low)

Bit N23	Bit R′1	Bit R′0	Output Frequency
0	0	0	Osc_e divided by 10
0	0	1	Osc_e divided by 12.5
0	1	0	Osc_e divided by 12.5
0	1	1	Osc_e divided by 12.5
1	0	0	Osc_e divided by 8
1	0	1	Osc_e divided by 10
1	1	0	Osc_e divided by 10
1	1	1	Osc_e divided by 10

When the Mode pin is high, these pins are digital inputs Pol′ and Pol which control the polarity of the phase/frequency detectors. See Tables 7 and 8. Positive polarity is used when an increase in an external VCO control voltage input causes an increase in VCO output frequency. Negative polarity is used when a decrease in an external VCO control voltage input causes an increase in VCO output frequency.

Table 7. Main Phase/Frequency Detector Polarity
(Mode Pin = High)

Mode Pin	Pol Pin	Main Detector Polarity (PD_{out}–Lo and PD_{out}–Hi)
High	Low	Positive
High	High	Negative
Low	*	Positive

*Pin configured as an output; should not be driven.

Table 8. Secondary Phase/Frequency Detector Polarity
(Mode Pin = High)

Mode Pin	Pol′ Pin	Secondary Detector Polarity (PD_{out}′)
High	Low	Positive
High	High	Negative
Low	*	Positive

*Pin configured as an output; should not be driven.

5B. REFERENCE PINS

Osc_e and Osc_b
Pins 1 and 32 — Reference Oscillator Transistor Emitter and Base

These pins can be configured to support an external crystal in a Colpitts oscillator configuration. The required connections for the crystal circuit are shown in the **Crystal Oscillator Considerations** section.

Additionally, the pins can be configured to accept an external reference frequency source, such as a TCXO. In this case, the reference signal is ac coupled into Osc_e and the Osc_b pin is left floating. See Figure 11.

Bit C6 and the Mode input pin control the configuration of these pins per Table 9.

Table 9. Reference Configuration

Mode Input Pin	Bit C6	Reference Configuration	Comment
Low	X	Supports Crystal (default)	C6 used to control Output B*
High	0	Supports Crystal	Output B not useful
High	1	Requires External Reference	Output B not useful

*See Table 5.

5C. LOOP PINS

f_{in} and $\overline{f_{in}}$
Pins 12 and 13 — Frequency Input for Main Loop (PLL)

These pins feed the on–chip RF amplifier which drives the high–speed N counter. This input may be fed differentially. However, it is usually used in a single–ended configuration with f_{in} driven while $\overline{f_{in}}$ is tied to a good RF ground (via a capacitor). The signal source driving this input must be ac coupled and originates from an external VCO.

The sensitivity of the RF amplifier is dependent on frequency as shown in the Loop Specifications table. Sensitivity of the f_{in} input is specified as a level across a 50 Ω load driven by a 50 Ω source. A VCO that can drive a load within the data sheet limits can also drive f_{in}. Usually, to avoid load pull and resultant frequency modulation of the VCO, f_{in} is lightly coupled by a small value capacitor and/or a resistor. See the applications circuit of Figure 65.

f_{in}′
Pin 30 — Frequency Input for Secondary Loop (PLL′)

This pin feeds the on–chip RF amplifier which drives the high–speed N′ counter. This input is used in a single–ended configuration. The signal source driving this input must be ac coupled and originates from an external VCO.

The sensitivity of the RF amplifier is dependent on frequency as shown in the Loop Specifications table. Sensitivity of the f_{in}′ input is specified as a level across a 50 Ω load driven by a 50 Ω source. A VCO that can drive a load within the data sheet limits can also drive f_{in}′. Usually, to avoid load pull and resultant frequency modulation of the VCO, f_{in}′ is lightly coupled by a small value capacitor and/or a resistor. See the applications circuit of Figure 65.

If the secondary loop is not used, PLL′ should be placed in standby and f_{in}′ should be left open.

PD_{out}–Hi and PD_{out}–Lo
Pins 19 and 20 — Phase/Frequency Detector Outputs for Main Loop (PLL)

Each pin is a three–state current source/sink/float output for use as a loop error signal when combined with an external low–pass loop filter. Under bit control, PD_{out}–Lo has either one–quarter or one–eighth the output current of PD_{out}–Hi per Table 10. The detector is characterized by a linear transfer function (no dead zone). The polarity of the detector is controllable. The operation of the detector is described below and shown in Figure 20.

Table 10. Current Ratio of PD_{out}–Hi and PD_{out}–Lo

Bit N18	Output Current Ratio PD_{out}–Hi:PD_{out}–Lo (Gain Ratio)
0	4 : 1
1	8 : 1

When the Mode pin is high, positive polarity occurs when the Pol pin is low. Also, when the Mode pin is low, polarity

defaults to positive. Positive polarity is described below. f_V is the output of the main loop's VCO divider (N counter). f_R is the output of the main loop's reference divider (R counter).

(a) Frequency of $f_V > f_R$ or phase of f_V leading f_R: current–sinking pulses from a floating state.
(b) Frequency of $f_V < f_R$ or phase of f_V lagging f_R: current–sourcing pulses from a floating state.
(c) Frequency and phase of $f_V = f_R$: essentially a floating state, voltage at pin determined by loop filter.

When the Mode pin is high, negative polarity occurs when the Pol pin is high. Negative polarity is described below. f_V is the output of the main loop's VCO divider (N counter). f_R is the output of the main loop's reference divider (R counter).

(a) Frequency of $f_V > f_R$ or phase of f_V leading f_R: current–sourcing pulses from a floating state.
(b) Frequency of $f_V < f_R$ or phase of f_V lagging f_R: current–sinking pulses from a floating state.
(c) Frequency and phase of $f_V = f_R$: essentially a floating state, voltage at pin determined by loop filter.

These outputs can be enabled and disabled by bits in the C and N registers. Placing the main PLL in standby (bit C1 = 1) forces the detector outputs to a floating state. In addition, setting the PD Float bit (bit C4 = 1) forces the detector outputs to a floating state while allowing the counters to run for the main PLL. For selection of the outputs, see Table 11.

The phase detector gain (in amps per radian) = PD_{out} current (in amps) divided by 2π.

If a detector output is not used, that pin should be left open.

Table 11. Selection of Main Detector Outputs

Bit N21	Bit N20	Bit N19	Result
0	0	0	Both outputs not enabled
0	0	1	PD_{out}–Lo enabled
0	1	0	PD_{out}–Hi enabled
0	1	1	Both PD_{out}–Lo and PD_{out}–Hi enabled
1	0	0	PD_{out}–Hi enabled for 16 f_R cycles only, then PD_{out}–Lo enabled
1	0	1	PD_{out}–Hi enabled for 32 f_R cycles only, then PD_{out}–Lo enabled
1	1	0	PD_{out}–Hi enabled for 64 f_R cycles only, then PD_{out}–Lo enabled
1	1	1	PD_{out}–Hi enabled for 128 f_R cycles only, then PD_{out}–Lo enabled

NOTES: 1. When a detector output is not enabled, it is floating.
2. Setting bit N21 = 1 places the IC in an adapt mode and engages a timer.

PD_{out}'
Pin 23 — Phase/Frequency Detector Output for Secondary Loop (PLL′)

This pin is a three–state voltage output for use as a loop error signal when combined with an external low–pass loop filter. The detector is characterized by a linear transfer function (no dead zone). The polarity of the detector is controllable. The operation of the detector is described below and shown in Figure 21.

When the Mode pin is high, positive polarity occurs when the Pol′ pin is low. Also, when the Mode pin is low, polarity defaults to positive. Positive polarity is described below. f_V' is the output of the secondary loop's VCO divider (N′ counter). f_R' is the output of the secondary loop's reference divider (R′ counter.)

(a) Frequency of $f_V' > f_R'$ or phase of f_V' leading f_R': negative pulses from high impedance.
(b) Frequency of $f_V' < f_R'$ or phase of f_V' lagging f_R': positive pulses from high impedance.
(c) Frequency and phase of $f_V' = f_R'$: essentially a high–impedance state, voltage at pin determined by loop filter.

When the Mode pin is high, negative polarity occurs when the Pol′ pin is high. Negative polarity is described below. f_V' is the output of the secondary loop's VCO divider (N′ counter). f_R' is the output of the secondary loop's reference counter (R′ counter.)

(a) Frequency of $f_V' > f_R'$ or phase of f_V' leading f_R': positive pulses from high impedance.
(b) Frequency of $f_V' < f_R'$ or phase of f_V' lagging f_R': negative pulses from high impedance.
(c) Frequency and phase of $f_V' = f_R'$: essentially a high–impedance state, voltage at pin determined by loop filter.

This output can be enabled and disabled by bits in the C register. Placing the secondary PLL′ in standby (bit C0 = 1) forces the detector output to a high–impedance state. In addition, setting the PD′ Float bit (bit C3 = 1) forces the detector output to a high–impedance state while allowing the counters to run for PLL′.

The phase detector gain (in volts per radian) = C_{mult} voltage (in volts) divided by 4π.

If the secondary loop is not used, PLL′ should be placed in standby and PD_{out}' should be left open.

5D. ANALOG OUTPUTS

DAC1 and DAC2
Pins 3 and 4 — Digital–to–Analog Converter Outputs

These are independent outputs of the two 8–bit D/A converters. The output voltage is determined by bits in the D register. Each output is a static level with an output impedance of approximately 100 kΩ.

The DACs may be used for crystal oscillator trimming, PA (power amplifier) output power control, or other general–purpose use.

If a DAC output is not used, the pin should be left open.

5E. EXTERNAL COMPONENTS

Rx
Pin 17 — Current–Setting Resistor

An external resistor to Gnd at this pin sets a reference current that is used to determine the current at the phase/frequency detector outputs PD_{out}–Hi and PD_{out}–Lo. A value of 2 kΩ is required.

C_{mult}
Pin 21 — Voltage–Multiplier Capacitor

An external capacitor to Gnd at this pin is used for the on–chip voltage multiplier circuit. The value of this capacitor must be greater than 20 times the value of the largest loop filter capacitor. For example, if the largest loop filter capacitor on either the main loop or the secondary loop is 0.01 μF, then a 0.22 μF capacitor could be used on the C_{mult} pin.

To ensure minimum standby supply current drain, the voltage potential at the C_{mult} pin must not be allowed to fall below the potential at the V_{pos} pins. Therefore, if the keep–alive oscillator is shut off, the user should tie a large value resistor (> 10 MΩ) between the C_{mult} pin and V_{pos}. This resistor should be sized to overcome leakage from C_{mult} to Gnd due to the printed circuit board and the external capacitor. The consequence of not using the resistor is higher supply current drain in standby. If standby is not used, the resistor is not necessary. Also, if the keep–alive oscillator is used, the resistor can be omitted.

C_{reg}
Pin 22 — Regulator Capacitor

An external capacitor to Gnd at this pin is required for the on–chip voltage regulator. A value of 1 μF is recommended.

5F. SUPPLY PINS

DAC V_{pos}
Pin 2 — Positive Supply Potential for DACs

This pin supplies power to both DACs and determines the full–scale output of the DACs. The full–scale output is approximately equal to the voltage at DAC V_{pos}. The voltage applied to this pin may be more, less, or equal to the potential applied to the V_{pos} pins. The voltage range for DAC V_{pos} is 1.8 to 3.6 V with respect to the Gnd pins.

If both DACs are not used, DAC V_{pos} should be tied to the same potential as V_{pos}.

V_{pos}
Pins 11, 24, 26, and 29 — Principal Positive Supply Potential

These pins supply power to the main portion of the chip. All V_{pos} pins must be at the same voltage potential. The voltage range for V_{pos} is 1.8 to 3.6 V with respect to the Gnd pins.

For optimum performance, all V_{pos} pins should be tied together and bypassed to a ground plane using a low–inductance capacitor mounted very close to the device. Lead lengths and printed circuit board traces between the capacitor and the IC package should be minimized. (The very–fast switching speed of the device can cause excessive current spikes on the power leads if they are improperly bypassed.)

Gnd
Pins 14, 15, 18, and 31 — Ground

Common ground for the device. All Gnd pins must be at the same potential and should be tied to a ground plane.

6. DETAILED REGISTER DESCRIPTIONS

6A. C REGISTER

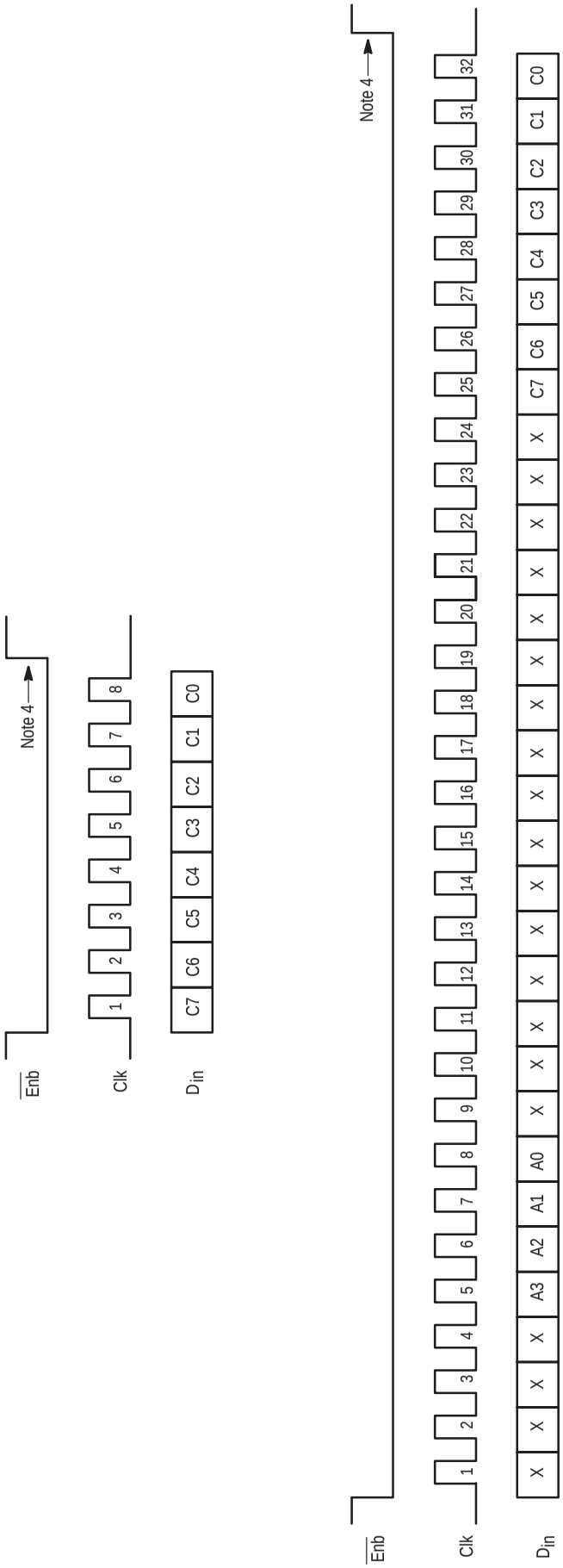


Figure 13. C Register Access and Formats

NOTES:

1. To access the C register, either 8 or 32 clock cycles can be used.
2. For the 8–bit stream, no address bits are needed.
3. For the 32–bit stream, address bits A3 through A0 are required.
4. At this point, the new byte is transferred to the C register. No other register is affected.
5. X signifies a don't care bit.

C REGISTER BITS

See Figure 13 for C register access and serial data formats.

Out A (C7)

When the Output A pin is selected as a General–Purpose Output (via bits R′21 = R′20 = 0), bit C7 determines the state of the pin. When C7 is 1, Output A is forced to a high level. When C0 is 0 Output A is forced low.

When Output A is not selected as a General–Purpose Output, bit C7 has no function; i.e., C7 is a “don’t care” bit.

Out B/XRef (C6)

Bit C6 is a dual–purpose bit.

When the Mode pin is tied low, C6 and C1 (PLL Stby), can be used to control Output B. See Table 12. (The reference circuit defaults to crystal configuration.)

When the Mode pin is tied high, additional control of the reference circuit is allowed. See Table 13.

Table 12. Out B/XRef Bit with Mode Pin = Low

Bit C6	Bit C1	State of Output B Pin	Condition of Main PLL
0	0	Low level	Active
0*	1*	High impedance*	Standby*
1	0	High level	Active
1	1	High impedance	Standby

*Power up default.

Table 13. Out B/XRef Bit with Mode Pin = High

Bit C6	Reference Configuration
0*	Supports Crystal*
1	Accommodates External Reference

*Power up default.

Out C (C5)

This bit determines the state of the Output C pin. When C5 is 1, Output C is forced to a high–impedance state. When C5 is 0, Output C is forced low.

PD Float (C4)

This bit controls the phase detector for the main loop, outputs PD_{out}–Hi and PD_{out}–Lo. When this bit is 0, the main phase detector operates normally. When the bit is 1, the outputs are forced to the floating state which opens the loop and allows modulation to be introduced into the external VCO input. During this time, the counters are still active. This bit is inhibited from affecting the phase detector during a PD_{out}–Hi or PD_{out}–Lo pulse.

If the loop is locked prior to C4 being set to 1, the lock detect signal from the main loop continues to indicate “lock” immediately after PD Float is set to 1. If the phase of the loop drifts outside the lock detect window, then the lock detect signal indicates “not locked”. If the loop is not locked, and PD Float is set to 1, then the lock detect signal from the main loop continues to indicate “not locked”.

PD′ Float (C3)

This bit controls the phase/frequency detector for the secondary loop, output PD_{out}'. When this bit is 0, the secondary phase detector operates normally. When the bit is 1, the output is forced to the floating state which opens the loop and allows modulation to be introduced into the external VCO input. During this time, the counters are still active. This bit is inhibited from affecting the phase detector during a PD_{out}' pulse.

If the loop is locked prior to C3 being set to 1, the lock detect signal from the secondary loop continues to indicate “lock” immediately after PD′ Float is set to 1. If the phase of the loop drifts outside the lock detect window, then the lock detect signal indicates “not locked”. If the loop is not locked, and PD′ Float is set to 1, then the lock detect signal from the secondary loop continues to indicate “not locked”.

Osc Stby (C2)

This bit controls the crystal oscillator and external reference input circuit. When this bit is 0, the circuit is active. When the bit is 1, the circuit is shut down and is in the low–power standby mode. When this circuit is shut down, a keep–alive oscillator for the voltage doubler is activated, unless the doubler is shut off via bits in the R′ register. In the crystal oscillator mode, when C2 transitions from a 1 to a 0 state, a kick–start circuit is engaged for a few milliseconds. The kick–start circuit ensures self–starting for a properly–designed crystal oscillator

NOTE

Whenever C2 is 1, both bits C1 and C0 must be 1, also.

To minimize standby supply current, the voltage multiplier may be shut down (by bits R′19, R′18, and R′17 being all zeroes). If this is the case and the voltage multiplier feature is being used, the user must allow sufficient time for the phase/frequency detector supply voltage to pump up when the multiplier is brought out of standby. This “pump up” time is dependent on the C_{mult} capacitor size. Pump current is approximately 100 μA. During the pump up time, either the PLL standby bits C1 and C2 must be 1 or the phase/frequency detector float bits C3 and C4 must be 1.

PLL Stby (C1)

When set to 1, this bit places the main PLL in the standby mode for reduced power consumption. PD_{out}–Hi and PD_{out}–Lo are forced to the floating state, the N and R counters are inhibited from counting, the main loop’s input amp is shut off, the Rx current is inhibited, and the main phase/frequency detector is shut off. The reference oscillator circuit is still active and independently controlled by bit C2.

When this bit is programmed to 0, the main PLL is taken out of standby in two steps. First, the input amplifier is activated, all counters are enabled, and the Rx current is no longer inhibited. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector at this time. Second, when the f_R pulse occurs, the N counter is loaded, and the phase/frequency and lock detectors are initialized via both flip–flops being reset. Immediately after the load, the N and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase

and lock detectors, and the phase/frequency detector output is enabled to issue an error correction pulse on the next f_R and f_V pulses. (Patent issued on this method.)

During standby, data is retained in all registers and any register may be accessed. When setting or clearing the PLL Stby bit, other bits in the C register may be changed simultaneously.

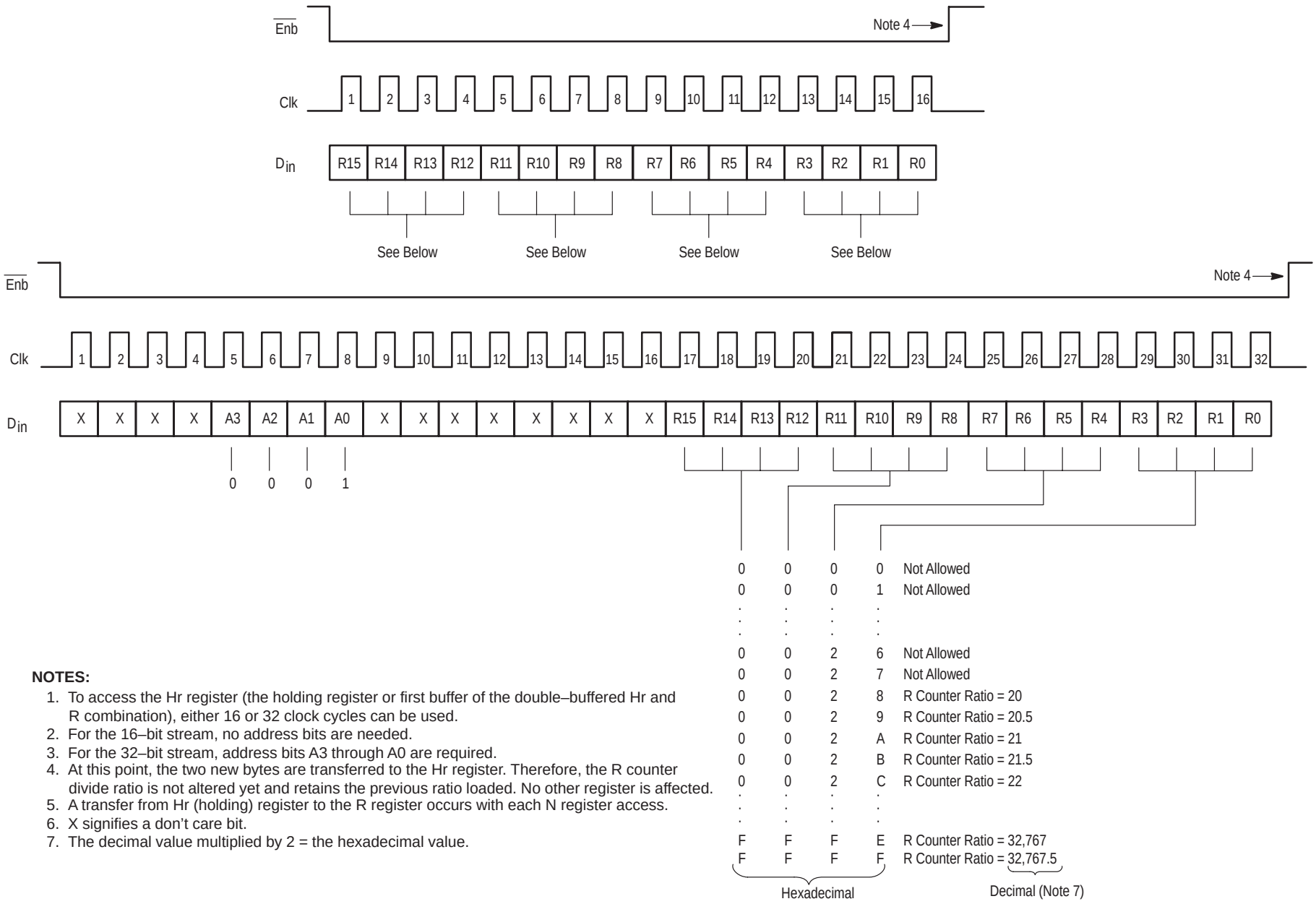
PLL′ Stby (C0)

When set to 1, this bit places the PLL′ section of the chip, which includes the on–chip f_{in}′ input amp, in the standby mode for reduced power consumption. PD_{out}′ is forced to the floating state. The R′ and N′ counters are inhibited from counting and placed in the low–current mode. The exception is the R′ counter's prescaler when the Mode pin is low. The R′ counter's prescaler remains active along with the f_{out} and $\overline{f_{out}}$ pins when PLL′ is placed in standby (Mode pin = low). When the Mode pin is low, the f_{out} pin, $\overline{f_{out}}$ pin, and R′ counter's prescaler are shut down only when Osc Stby bit C2 is set to 1.

When C0 is reset to 0, PLL′ is taken out of standby in two steps. All PLL′ counters and the input amp are enabled. Any f_R′ and f_V′ signals are inhibited from toggling the associated phase/frequency detector at this time. Second, when the f_R′ pulse occurs, the N′ counter is loaded and the phase/frequency detector is initialized via both flip–flops being reset. Immediately after the load, the N′ and R′ counters begin counting down together. At this point, the f_R′ and f_V′ pulses are enabled to the phase and lock detectors, and the phase/frequency detector output is enabled to issue an error correction pulse on the next f_R′ and f_V′ pulses. (Patent issued on this method.)

During standby, data is retained in all registers, and any register may be accessed. When setting or clearing the PLL′ Stby bit, other bits in the C register may be changed simultaneously.

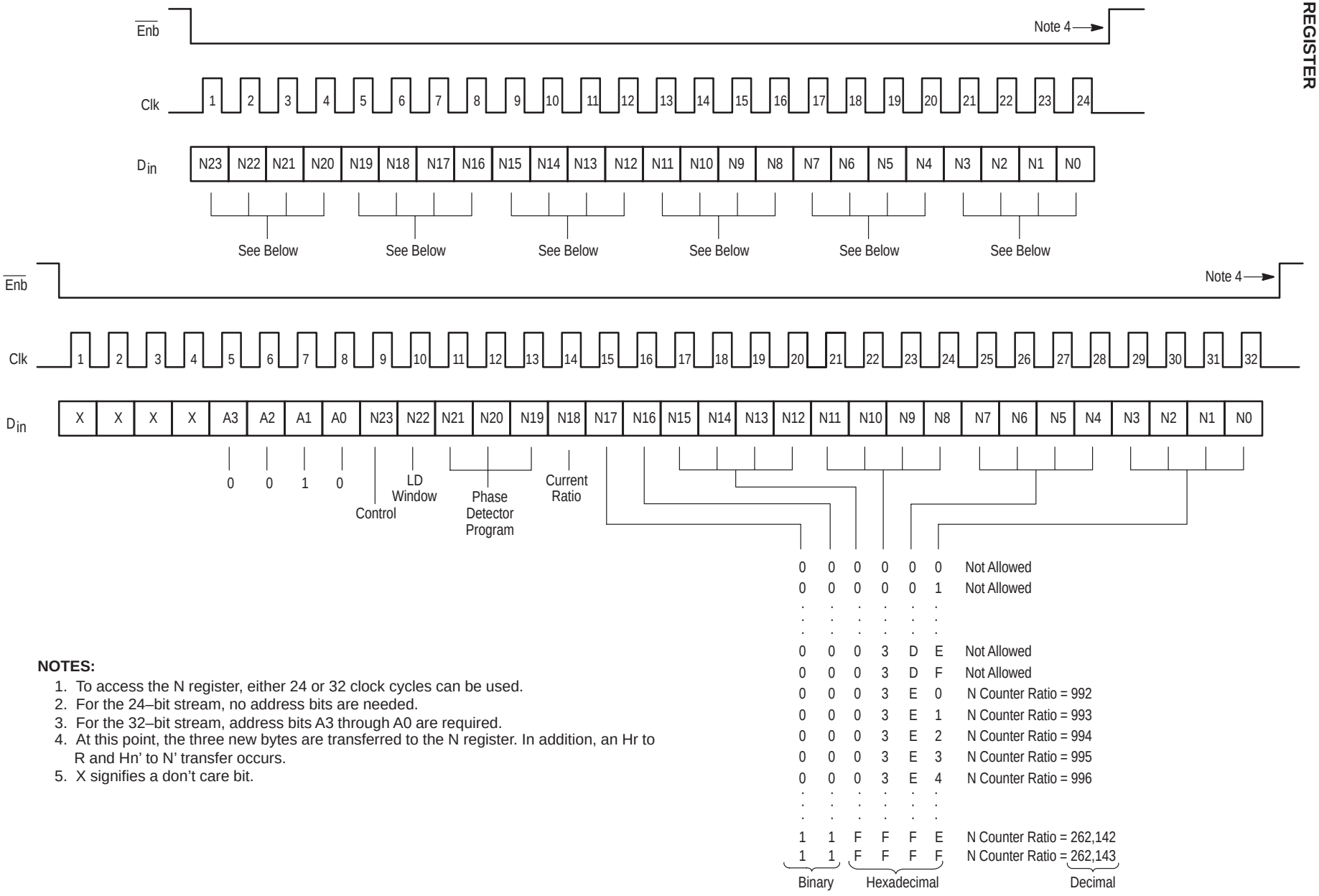
Figure 14. Hr Register Access and Formats



NOTES:

1. To access the Hr register (the holding register or first buffer of the double–buffered Hr and R combination), either 16 or 32 clock cycles can be used.
2. For the 16–bit stream, no address bits are needed.
3. For the 32–bit stream, address bits A3 through A0 are required.
4. At this point, the two new bytes are transferred to the Hr register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. No other register is affected.
5. A transfer from Hr (holding) register to the R register occurs with each N register access.
6. X signifies a don't care bit.
7. The decimal value multiplied by 2 = the hexadecimal value.

Figure 15. N Register Access and Formats



NOTES:

1. To access the N register, either 24 or 32 clock cycles can be used.
2. For the 24–bit stream, no address bits are needed.
3. For the 32–bit stream, address bits A3 through A0 are required.
4. At this point, the three new bytes are transferred to the N register. In addition, an Hr to R and Hn' to N' transfer occurs.
5. X signifies a don't care bit.

N REGISTER BITS

See Figure 15 for N register access and serial data formats.

Control (N23)

When the Mode pin is low, Control bit N23 determines the divide ratio of the auxiliary divider which feeds the buffers for the f_{out} and $\overline{f_{out}}$ pins. See Table 14 for the overall ratio between Osc_e and $f_{out}/\overline{f_{out}}$.

When the Mode pin is high, N23 must be programmed to 1.

Table 14. Osc_e to f_{out} Frequency Ratio, Mode = Low

N23	R′1	R′0	Osc_e to f_{out} Frequency Ratio
0	0	0	10:1
0	0	1	12.5:1
0	1	0	12.5:1
0	1	1	12.5:1
1	0	0	8:1
1	0	1	10:1
1	1	0	10:1
1	1	1	10:1

LD Window (N22)

Bit N22 determines the lock detect window for the main loop. Refer to Table 15 and Figure 19.

Table 15. Lock Detect Window

N22	LD Window (Approximated)
0	32 Osc_e periods
1	128 Osc_e periods

Phase Detector Program (N21, N20, N19)

These bits control which phase detector outputs are active for the main loop. These bits also control the timer interval when adapt is utilized for the main loop. See Table 16.

Table 16. Main Phase Detector Control

N21	N20	N19	Result
0	0	0	Both PD_{out}–Hi and PD_{out}–Lo floating
0	0	1	PD_{out}–Hi floating, PD_{out}–Lo enabled
0	1	0	PD_{out}–Hi enabled, PD_{out}–Lo floating
0	1	1	Both PD_{out}–Hi and PD_{out}–Lo enabled
1	0	0	PD_{out}–Hi enabled and PD_{out}–Lo floating for 16 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled
1	0	1	PD_{out}–Hi enabled and PD_{out}–Lo floating for 32 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled
1	1	0	PD_{out}–Hi enabled and PD_{out}–Lo floating for 64 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled
1	1	1	PD_{out}–Hi enabled and PD_{out}–Lo floating for 128 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled

Current Ratio (N18)

This bit allows for MCU control of the PD_{out}–Hi to PD_{out}–Lo current (or gain) ratio on the main loop phase/frequency detector outputs. See Table 17.

Table 17. PD_{out}–Hi to PD_{out}–Lo Current Ratio

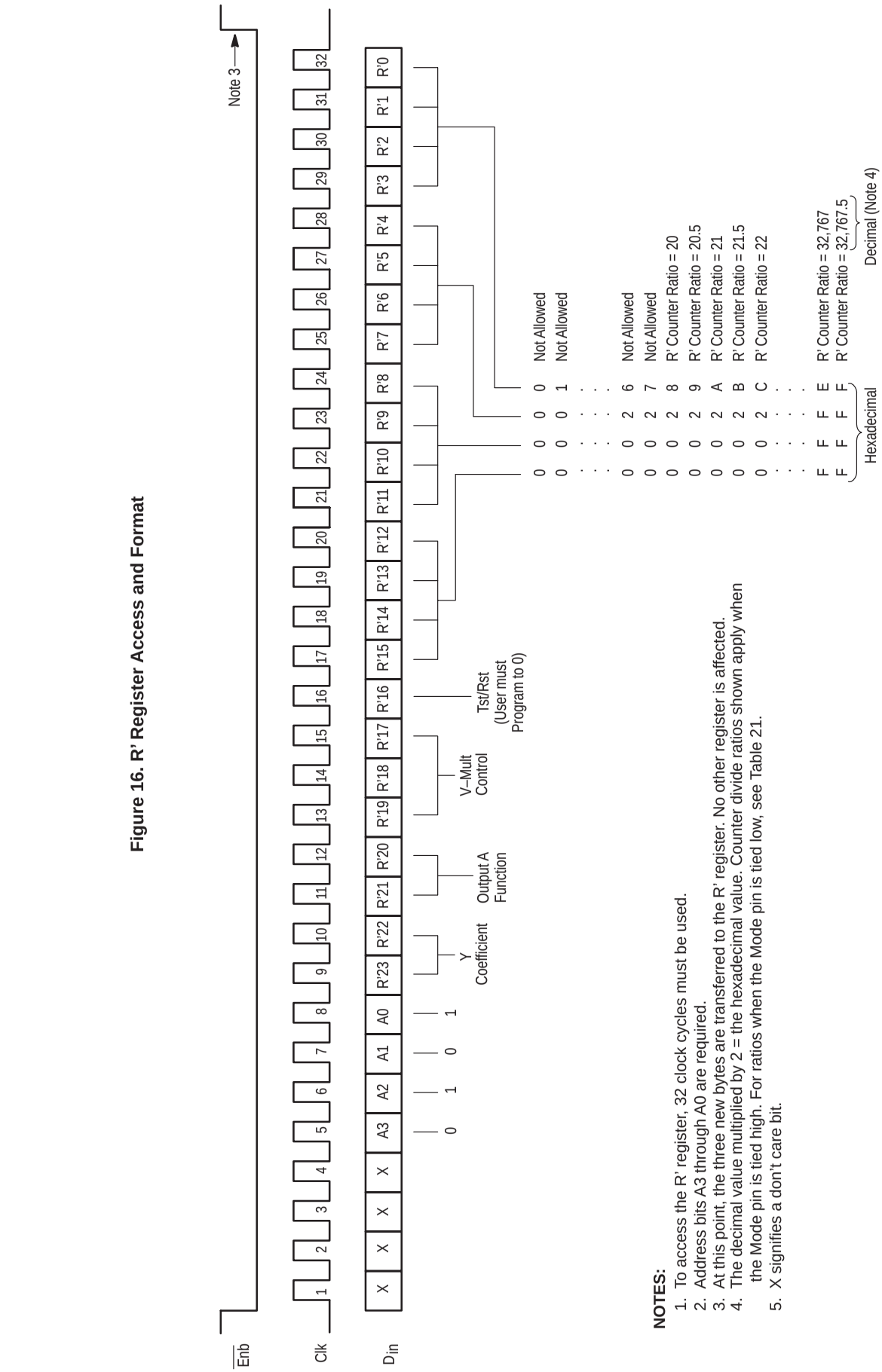
N18	PD_{out}–Hi to PD_{out}–Lo Current Ratio	PD_{out}–Hi Current C_{mult} Pin = 5 V (Nominal)	PD_{out}–Lo Current C_{mult} Pin = 5 V (Nominal)
0	4:1	4.4 mA	1.1 mA
1	8:1	4.4 mA	0.55 mA

N Counter Divide Ratio (N17 to N0)

These bits control the N Counter divide ratio or loop multiplying factor. The minimum allowed value is 992. The maximum value is 262,143. For ease of programming, binary representation is used. For example, if a divide ratio of 1000 is needed, the 1000 in decimal is converted to binary 00 0000 0011 1110 1000 and is loaded into the device for N17 to N0. See Figure 15.

6D. R′ REGISTER

Figure 16. R' Register Access and Format



NOTES:

1. To access the R' register, 32 clock cycles must be used.
2. Address bits A3 through A0 are required.
3. At this point, the three new bytes are transferred to the R' register. No other register is affected.
4. The decimal value multiplied by 2 = the hexadecimal value. Counter divide ratios shown apply when the Mode pin is tied high. For ratios when the Mode pin is tied low, see Table 21.
5. X signifies a don't care bit.

R′ REGISTER BITS

See Figure 16 for R′ register access and serial data format.

Y Coefficient (R′23 and R′22)

These bits are programmed per Table 18. Note that for the MC145181, the bits are always programmed as 00. For compatibility, the other combinations are reserved for use with the MC145225 and MC145230.

Table 18. Y Coefficient

R′23	R′22	Maximum Allowed Frequency at f_{in} Pin
0	0	550 MHz
0	1	(not used)
1	0	(not used)
1	1	(not used)

Output A Function (R′21 and R′20)

These bits control the function of the Output A pin per Table 19. When selected as a general–purpose output, bit C7 controls the state of the pin. The signals f_R and $f_{R'}$ are the outputs of the R and R′ counters, respectively. The selection as a detector pulse is a test feature.

Table 19. Output A Function Selection

R′21	R′20	Function Selected for Output A
0	0	General–Purpose Output
0	1	f_R
1	0	$f_{R'}$
1	1	Phase/Frequency Detector Pulse from either loop

V–Mult Control (R′19, R′18, R′17)

These bits control the voltage multiplier per Table 20. When the multiplier is in the active state, the bits determine the voltage multiplier's refresh rate of the capacitor tied to the C_{mult} pin.

When active, the bits should be programmed for the lowest possible maximum frequency shown in the table. This ensures that the voltage multiplier is operating at optimum efficiency. For example, for a system utilizing a 16.8 MHz reference, bits R′19, R′18, and R′17 should be programmed as 001 if the user desires to use the voltage multiplier. If the user does not want to use the multiplier, the bits should be programmed as 000. In the latter case, only a 0.1 μF bypass capacitor is needed at the C_{mult} pin and an external phase/frequency detector supply voltage of 3.6 to 5.25 V must be provided to the C_{mult} pin.

Table 20. Voltage Multiplier Control

R′19	R′18	R′17	Multiplier State	Maximum Allowed Frequency at Osc_e Pin
0	0	0	Inactive	80 MHz
0	0	1	Active	20 MHz
0	1	0	Active	40 MHz
0	1	1	Active	80 MHz
1	X	X	—	(for factory evaluation)

Test/Rst (R′16)

This bit must be programmed to 0 by the user.

R′ Counter Divide Ratio (R′15 to R′0)

These bits control the R′ counter divide ratio. Thus, these bits determine the secondary loop's minimum step size. This step size is the same as the phase/frequency detector's operating frequency which must not exceed 600 kHz.

With the Mode pin tied high, the minimum allowed value is 20. The maximum value is 32,767.5. For ease of programming, binary representation is used. However, the binary value must be multiplied by 2. For example, if a divide ratio of 1000 is needed, the 1000 in decimal is converted to binary 0000 0011 1110 1000. This value is multiplied by 2 and becomes 0000 0111 1101 0000 and is loaded into the device for R′15 to R′0. See Figure 16.

With the Mode pin tied low, Table 21 shows the divide ratios available. There are two formulas for the divide ratio when Mode is low.

If R′1 R′0 are 00: R′ Ratio = (Value of R′15 to R′2) x 2.

If R′1 R′0 are 01, 10, 11: R′ Ratio = (Value of R′15 to R′2) x 2.5.

Table 21. R′ Counter Divide Ratios with Mode Pin Tied Low*

R′15	R′14	R′13	R′12	R′11	R′10	R′9	R′8	R′7	R′6	R′5	R′4	R′3	R′2	R′1	R′0	R′ Counter Divide Ratio
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Not Allowed
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	Not Allowed
⋮																
0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	Not Allowed
0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	20
0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	25
0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	X	25
0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	22
0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	27.5
0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	X	27.5
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	24
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	30
0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	X	30
0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	26
0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	32.5
0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	X	32.5
⋮																
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	32,766
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	40,957.5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	40,957.5

* Divide ratios with the Mode pin tied high are shown in Figure 16.

Figure 17. Hn' Register Access and Format

NOTES:

1. To access the Hn' register (the holding register or first buffer of the double–buffered Hn' and N' combination), 32 clock cycles must be used.
2. Address bits A3 through A0 are required.
3. At this point, the two new bytes are transferred to the Hn' register. Therefore, the N' counter divide ratio is not altered yet and retains the previous ratio loaded. No other register is affected.
4. A transfer from the Hn' (holding) register to the N' register occurs with each N register access.
5. X signifies a don't care bit.
6. The decimal value multiplied by 8 = the hexadecimal value.

6F. D REGISTER

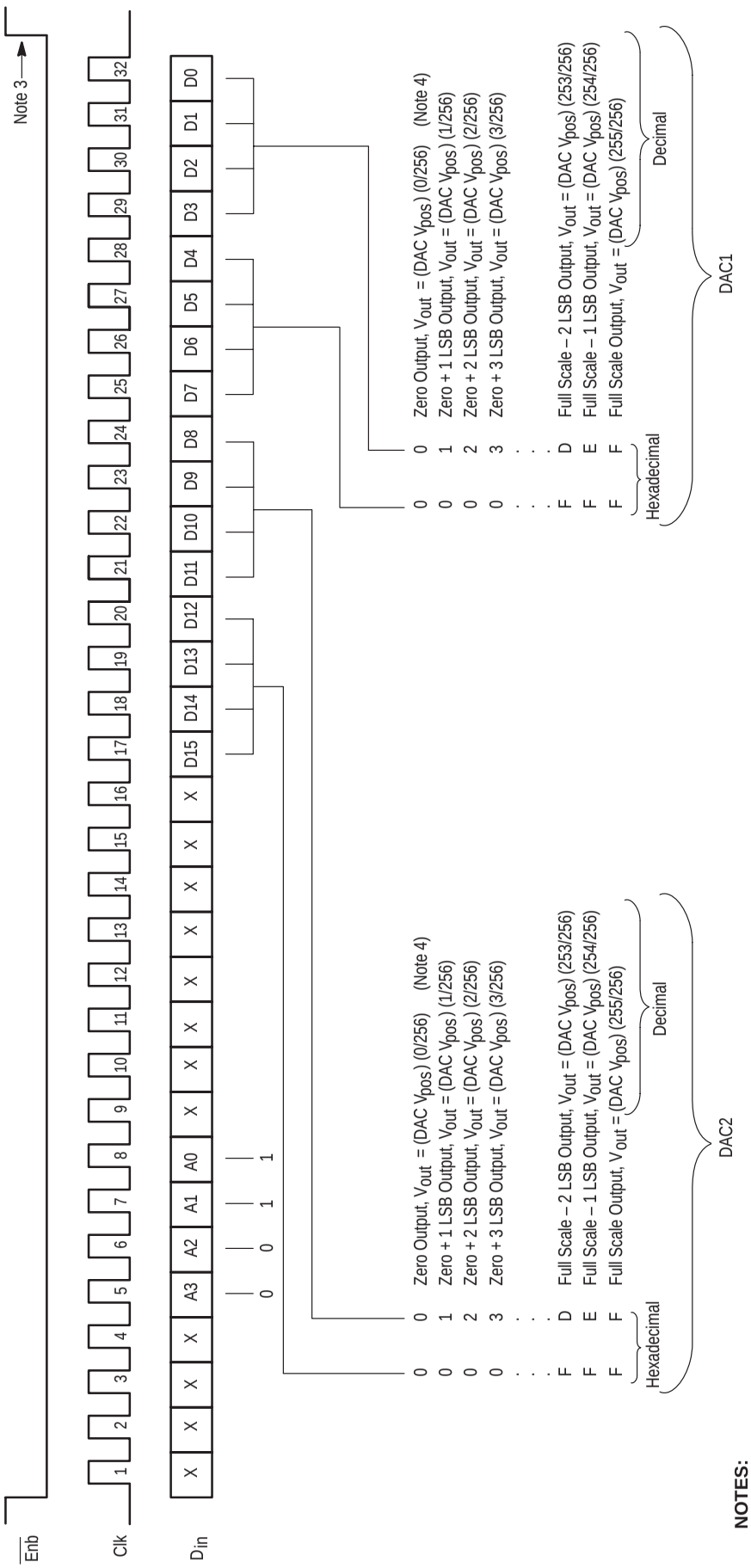
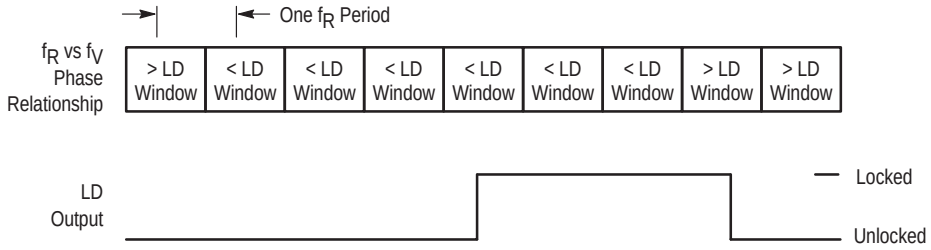


Figure 18. D Register Access and Format

NOTES:
1. To access the D Register, 32 clock cycles are used.
2. Address bits A3 through A0 are required.
3. At this point, the two new bytes are transferred to the D register. No other register is affected.
4. Low–power standby state.
5. X signifies a don't care bit.

Figure 19. Lock Detector Operation



NOTES:

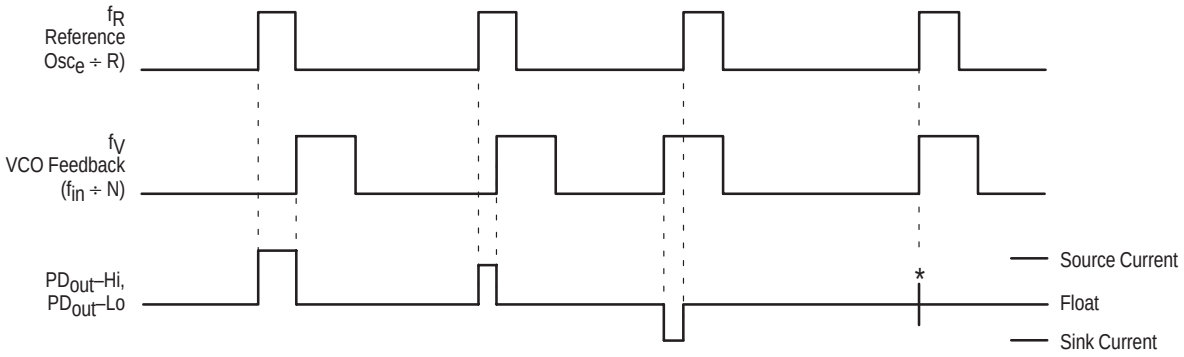
1. Illustration shown is for the main loop and applies when the secondary loop is either phase locked or in standby. The actual detector outputs for each loop are ANDed together at the LD pin.
2. The secondary loop is similar to the above illustration.
3. The approximate lock detect window for the main loop is either 64 or 256 Osc_e cycles and is programmable via bit N22. The approximate window for the secondary loop is 64 Osc_e cycles and is not programmable.
4. The LD output is low whenever the phase difference is more than the lock detect window.
5. The LD output is high whenever the phase difference is less than the lock detect window and continues to be less than the window for 3 f_R periods or more.

LOCK DETECTOR OUTPUT CONDITIONS

f_R versus f_V Relation	Lock Detector Output	Microcontroller Action
Frequency is the same with phase inside the LD window	Static high level output	Senses high level and no edges, therefore loop is locked
Frequency is the same with phase outside the LD window	Static low level output	Senses low level, therefore loop is unlocked
Frequency is slightly different, thus phase is changing	Dynamic “chattering” output, output has transitions	Senses edges, therefore loop is unlocked
Frequency is grossly different	Static low level output	Senses low level, therefore loop is unlocked

NOTE: For simplicity, this table applies to the main loop. The secondary loop is similar. The detector outputs feed an AND gate whose output is the LD pin.

Figure 20. PD_{out}–Hi and PD_{out}–Lo Detector Output Characteristics

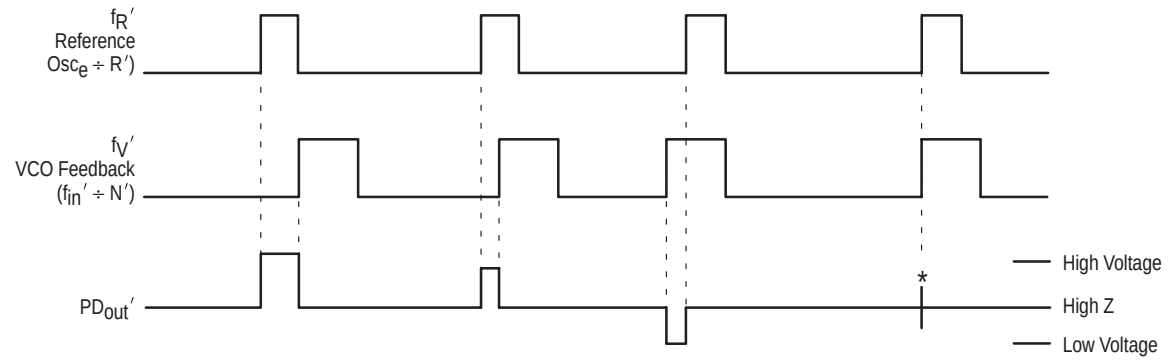


*At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.

NOTES:

1. The detector generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.
2. Waveform shown applies when the $\overline{f_{out}}$/Pol pin is low and the Mode pin is high.
3. When the $\overline{f_{out}}$/Pol pin is high and Mode is high, the PD_{out}–Hi and PD_{out}–Lo waveform is inverted.
4. The waveform shown is also the default when the Mode pin is low.

Figure 21. PD_{out}' Detector Output Characteristics



*At this point, when both f_R' and f_V' are in phase, the output source and sink circuits are turned on for a short interval.

NOTES:

1. The detector generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.
2. Waveform shown applies when the f_{out}/Pol′ pin is low and the Mode pin is high.
3. When the f_{out}/Pol′ pin is high and Mode is high, the PD_{out}' waveform is inverted.
4. The waveform shown is also the default when the Mode pin is low.

7. APPLICATIONS INFORMATION

7A. CRYSTAL OSCILLATOR CONSIDERATIONS

The oscillator/reference circuit may be connected to operate in either of two configurations. With the Mode pin placed “high” and bit C6 programmed to 1, the oscillator/reference circuit of the MC145181 will accept an external reference input. The external reference signal should be capacitive, connected to Osc_e with Osc_b left floating. Commercially available temperature compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide a very stable reference frequency. For additional information about TCXOs and data clock oscillators, please consult the Electronic Engineers Master Catalog, internet web page, or similar publication/service.

The on–chip Colpitts reference oscillator can be selected by either tying the Mode pin low or by programming the C6 bit to zero when Mode is high. The oscillator may be operated in either the fundamental mode, as show by Figure 22, or as an overtone oscillator. The “kick start” feature ensures reduced “stalling” of hard–starting crystals.

Crystal Resonators

The equivalent circuit of a crystal resonator most commonly used is shown in Figure 23. The crystal itself is a specially cut (usually AT for overtone operation) block of quartz. The dimensions, (shape, thickness, length, and width) determine the operating characteristics of the crystal. When deformed and allowed to return naturally to its resting shape, it is observed to oscillate. This oscillation has the typical characteristics of a damped oscillation and an equivalent electrical signal can be found on the surface of the crystal. In addition, if an equivalent electrical signal is applied to the crystal, it will be observed to oscillate. The equivalent values for R_S, L_S, C_S, and C_O can be used to predict the operation of the crystal when used as an electronic oscillator.

Due to the series/parallel arrangement of the equivalent components, the crystal exhibits two resonances. The first, sometimes just called resonance, is the series resonance of the R_S, C_S, L_S branch. The other, sometimes called the anti–resonance, is the parallel resonance including C_O. For the series resonance the formula is

$$f_S = \frac{1}{2\pi \sqrt{L_S C_S}} .$$

For parallel resonance, the formula is

$$f_p = \frac{1}{2\pi \sqrt{\frac{L_S C_S C_O}{C_O + C_S}}} .$$

As can be seen from this equation, the anti–resonant frequency is higher than the series resonant frequency. The ratio between the resonant and anti–resonant frequency can be found using the formula

$$\frac{\Delta f}{f} = \frac{C_S}{2 (C_O + C_S)}$$

where

$$\Delta f = |f_S - f_p|$$

and

$$f = \frac{f_S + f_p}{2} .$$

By exploiting this characteristic, the crystal oscillator frequency can be tuned slightly. If a capacitor is connected in series with the crystal operating in the resonance mode, the frequency will shift upward. If a capacitance is added in parallel with a crystal operating in an anti–resonant mode, the frequency will be shifted down.

Figure 22. Fundamental Mode Oscillator Circuit

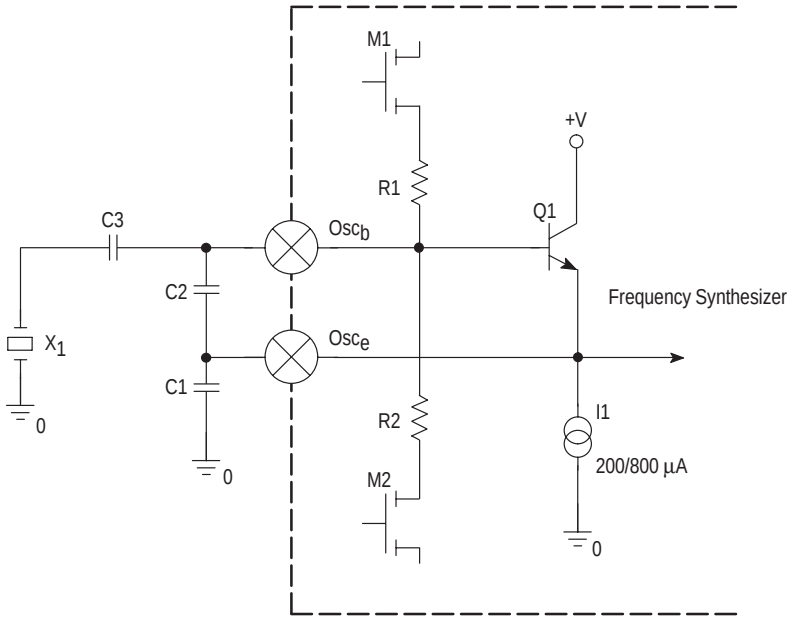
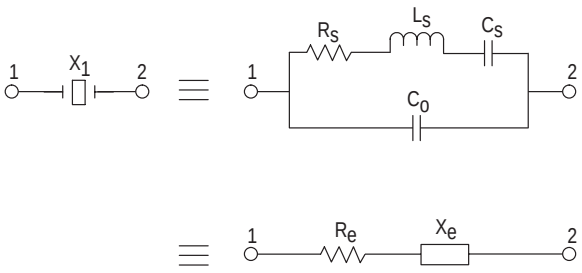
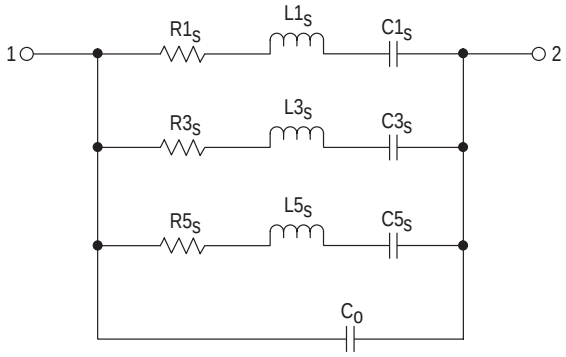


Figure 23. Crystal Resonator Equivalent Circuit



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 24. Overtone Crystal Equivalent Circuit



Because of the acoustic properties of the crystal resonator, the crystal “tank” responds to energy not only at its fundamental frequency, but also at specific multiples of the fundamental frequency. In the same manner that a shorted or open transmission line responds to multiples of the fundamental frequency, the crystal “tank” responds similarly. A shorted half–wave transmission line (or closed acoustic chamber) will not only resonate at its fundamental frequency, but also at odd multiples of the fundamental. These are called the overtones of the crystal and represent frequencies at which the crystal can be made to oscillate. The equivalent circuit of an overtone crystal is shown is Figure 24.

The components for the appropriate overtone are represented by 1, 3, and 5. The fundamental components are represented by 1, and those of importance for the third and fifth overtones, by 3 and 5.

Fundamental Mode

The equivalent circuit for the Colpitts oscillator operating in the fundamental mode is shown in Figure 25.

C3 is selected to provide a small reduction in the inductive property of the crystal. In this manner, the frequency of the oscillator can be “pulled” slightly. The biasing combination of M1R1 and M2R2 provide the ability to start operation with a higher than normal operating current to stimulate crystal activity. This “kick start” current is nominally four times the normal current. An internal counter times the application of the “kick start” and returns the current to normal after the time out period.

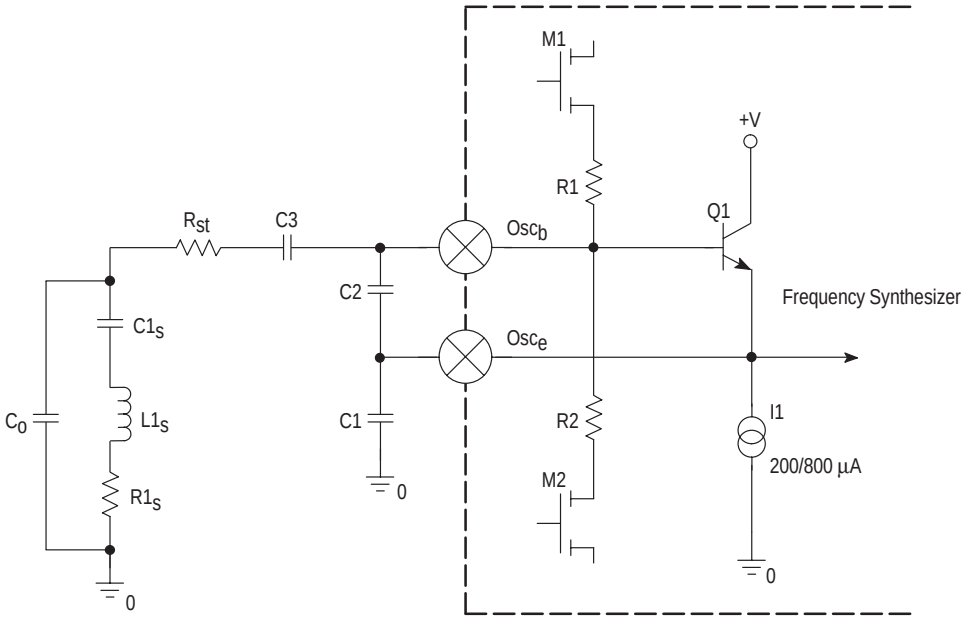
The mutual conductance (transconductance) of the transistor Q1 is useful in determining the conditions necessary for oscillation. The nominal value for the transconductance is found from the formula

$$gm = \frac{I_e}{26}$$

where Ie is the emitter current in mA.

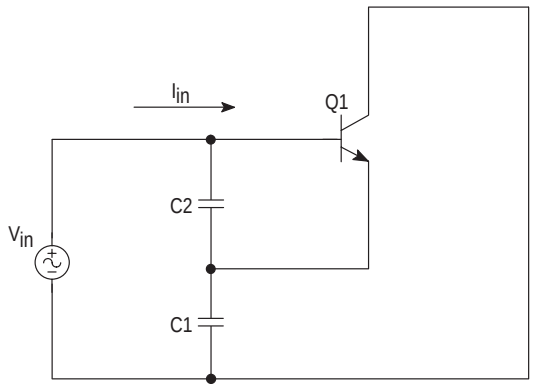
The operation of the oscillator can be described using the concept of “negative resistance”. In a normal tuned circuit, any excitation tends to be dissipated by the resistance of the circuit and oscillation dies out. The resistive part of the crystal along with the resistance of the wiring and the internal resistance of C1, C2, and C3, make up this “damping” resistance. Some form of energy must be fed back into the circuit to sustain oscillation. This is the purpose of the amplifier.

Figure 25. Fundamental Mode Colpitts Oscillator Equivalent Circuit



If we define the damping as resistive, we can define the opposite or regenerative property as negative resistance. Figure 26 shows the basic circuit of the Colpitts oscillator. C3 has been combined with the crystal elements for simplicity. For the circuit to oscillate, there must be at least as much “negative resistance” (regeneration) as there is resistance (damping). We can define this by deriving the input impedance for the amplifier.

Figure 26. Colpitts Oscillator Basic Circuit



If a driving signal is defined as V_{in}, the resultant current that flows can be identified as I_{in}. The relationship of V_{in} to I_{in} is

$$V_{in} = I_{in}\,(Z_{c1} + Z_{c2}) - I_b\,(Z_{c2} - \beta Z_{c1})$$

and

$$0 = I_{in}\,(Z_{c2}) + I_b\,(Z_{c2} + r_b)$$

where I_b is the base current of transistor Q1. Solving the two equations and assuming $Z_{c2} << r_b$, the input impedance can be expressed as

$$Z_{in} \sim \frac{-gm}{\omega^2\,C1\,C2} + \frac{1}{j\omega\left(\frac{C1\,C2}{C1 + C2}\right)}$$

where $\omega = 2\pi f$. This is equivalent to the series combination of a real part whose value is

$$REAL = \frac{-gm}{\omega^2\,C1\,C2}$$

and the imaginary part whose value is

$$IMAG = \frac{1}{j\omega\left(\frac{C1\,C2}{C1 + C2}\right)}$$

To sustain oscillation, the amplifier must generate a “negative resistance” equal or greater than the REAL part of the above equation and opposite in polarity.

$$R_{neg} = \frac{-gm}{\omega^2\,C1\,C2}$$

As long as the relation

$$-R_{neg} = -SUM\,(R_S + R_{st} + R_{c1} + R_{c2} + R_{c3}) \ ,$$

the circuit will oscillate and the frequency of oscillation will be defined as

$$f_o = \frac{1}{2\pi\sqrt{L_S\,(C1||C2||C3)}}$$

where C3 is the series frequency adjusting capacitor.

In determining values for C1, C2, and C3, two limits are considered. At one end is the relationship of C3 to C2 and C1. If C3 is made 0 or the reactance of C3 is small compared to the reactance of C1 and C2, no adjustment of the crystal frequency is possible. The other limit is the relationship

$$gm\,Z_{c1}\,Z_{c2} > R_{sum}$$

where R_{sum} is the sum of resistances in the resonant loop. Since this equation must be true for the circuit to oscillate, it is obvious that as the values of C1 and C2 are increased, the series resistances must be reduced and/or gm increased. Since gm is a function of device current and there is a physical limit on how small R_{sum} can be made, at some point oscillation can no longer be sustained.

Normally, it is desirable to choose the “negative resistance” to be several times greater than the “damping” resistance to ensure stable operation. A factor of four or five is a good “rule of thumb” choice.

To determine crystal power, the equivalent circuit shown in Figure 27 can be used. In this case, we are addressing a condition where the transistor amplifier is operating at the limit of class A; that is, the device is just at cutoff during the peak negative excursions. At this point,

$$R_e = gm\,X_{c1}\,X_{c2}$$

if the amplitude is constant and the oscillator is stable. For this to occur, the sum of all resistances in the resonant loop will be equal to R_e, where R_e represents the effective resistance of I1. This can be written as

$$R_{sum} = R_S + R_{st} = R_e$$

where R_S is the crystal resistance and R_{st} is the additional distributed resistances within the resonant loop. At the point where the transistor enters cutoff we have the equation

$$-I_{in} = \frac{v1 + v2}{X_{ls} + R_e} = \frac{(I_{in} - I_b)\,Z_{c2} + (I_{in} + \beta i_b)\,Z_{c1}}{X_{ls} + R_e} \ .$$

β = current gain of the transistor. Rewriting:

$$I_{in} = \frac{I_b\,(Z_{c2} - \beta Z_{c1})}{Z_{c1} + Z_{c2} + X_{ls} + R_e} \ .$$

For oscillation to occur, we must have

$$Z_{c1} + Z_{c2} + X_{ls} \sim 0 \ .$$

If we assume βZ_{c1} is normally much greater than Z_{c2} then

$$I_{in} \sim \frac{-I_e\,Z_{c1}}{R_e} \ .$$

For the condition we have specified,

$$I_e(bias) + I_e(instantaneous\ ac) = 0$$

the transistor is just cutting off and the peak current, I_{in} is equal to the bias current. The peak input current is represented as

$$I_{in}(peak) = \frac{I_e|Z_{c1}|}{R_e} \ .$$

The power dissipation of the series resistances in the resonant loop can be written as

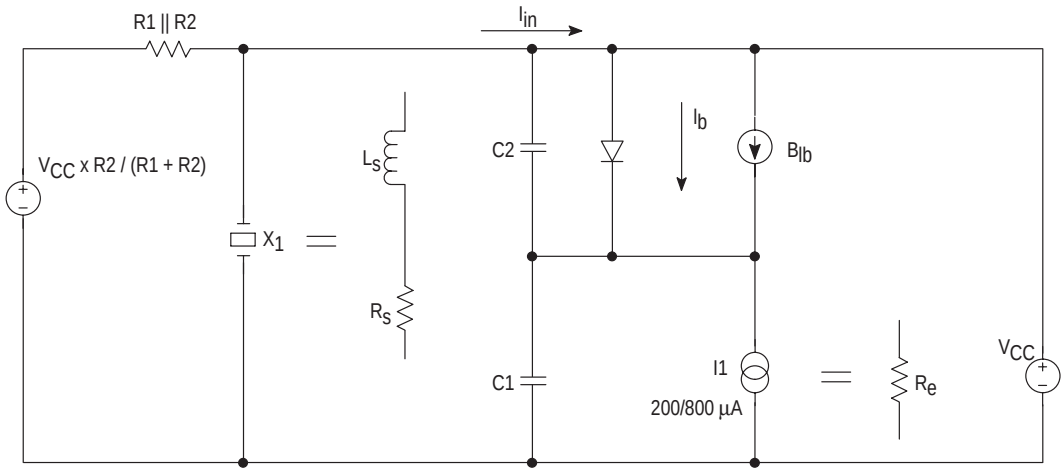
$$P = \frac{I_{in}(peak)^2\,R}{2} = \frac{(I_e|Z_{c1}|)^2}{2\,R_{sum}}$$

where $R_{sum} = R_e$.

The power dissipation for the crystal itself becomes

$$P_{crystal} = \frac{(I_e|Z_{c1}|)^2}{2\,R_S} \ .$$

Figure 27. Equivalent Circuit for Crystal Power Estimation



Overtone Operation

For overtone operation, the circuit is modified by the addition of an inductor, L1; and a series capacitor, C4. C4 is inserted as a dc blocking capacitor whose capacitance is chosen sufficiently large so that its reactance can be ignored. This circuit is shown in Figure 28.

For oscillation to occur at the overtone frequency, the condition

$$gm\ Z_{c1}\ Z_{c2} > R_S$$

must exist.

Z_{c1} represents the impedance across C1 and can be defined as

$$Z_{c1} = jX_{c1} \,||\, (R_{l1} + jX_{l1})$$

where R_{l1} is the dc resistance of the inductor L1.

For overtone operation, this must occur at the desired harmonic. For example, if the crystal is chosen to oscillate at the third overtone, C1 and C2 must be chosen so that the above condition exists for Z_{c1} and Z_{c2} at the third harmonic of the fundamental frequency for the crystal. In addition, care must be taken that the "negative resistance" of the amplifier is not sufficient at the fundamental frequency to induce oscillation at the fundamental frequency. It may be necessary to add additional filtering to reduce the gain of the amplifier at the fundamental frequency. The key to achieving stable overtone oscillator operation is ensuring the existence of the above condition at the desired overtone while ensuring its failure at all other frequencies.

L1 and C1 are chosen so that

$$\frac{1}{2\pi\sqrt{L_1\,C_1}} > F_f$$

where F_f is the fundamental frequency of the crystal resonator. If L1 and C1 are chosen to be net capacitive at the desired overtone frequency and if the condition

$$gm\ Z_{c1}\ Z_{c2} > R_S$$

is true only at the desired overtone frequency, the oscillator will oscillate at the frequency of the overtone. Normally, L1 and C1 are not chosen to be resonant at the overtone frequency but at a lower frequency to ensure that the parallel combination of L1 and C1 is capacitive at the overtone frequency and inductive at the fundamental frequency.

$$F_f < \frac{1}{2\pi\sqrt{L_1\,C_1}} < F_o$$

The net inductance of the rest of the resonant loop then balances this capacitance at the overtone frequency.

$$\frac{1}{\frac{1}{X_{ls} - X_{cs}} - \frac{1}{X_{c0}}} + X_{l2} + X_{l(stray)} - X_{c3}$$

$$+ \frac{1}{\frac{1}{X_{l1}} - \frac{1}{X_{c1}}} = 0$$

L2 and C3 are chosen to provide the desired adjustment to the resonant overtone frequency. This is normally computed by calculating the expected ppm change at the resonant frequency and using this to define the value of the reactance necessary to produce this change.

$$\Delta F_f\ (ppm) = \frac{X\ (of\ L2\ and\ C3)}{Z\ (crystal\ at\ resonance)}$$

$$\Delta F_f\ (ppm) = X(of\ L2\ and\ C3)/Z(crystal\ at\ resonance)$$

The values needed for this calculation can be derived from the value of the fundamental frequency and C_o. If C_o is known or can be measured, C_s is defined as

$$C_s = \frac{C_o}{200}$$

for an AT cut crystal.

The fundamental frequency can be used to calculate the value for L_s using either the series resonant or parallel resonant formulas given earlier. Since the Q of the crystal,

$$Q = \frac{X}{R}$$

is usually sufficiently large at the resonant frequency so that

$$R_S << Z(crystal)$$

R_S can be ignored. The value for C3 and L2 are chosen so that

$$X_{C3} = X_{L2}$$

when C3 is adjusted to approximately half its maximum capacitance. At this setting, the combination produces a zero change in the overtone frequency. If C3 is then chosen so that X_{C3} at minimum capacitance is

$$[X_{C3}(max)] - X_{L2} >= \Delta F_f \text{ (ppm) } Z(crystal)$$

and L2 is approximately

$$X_{L2} = \frac{X_{C3}(max)}{2}$$

then

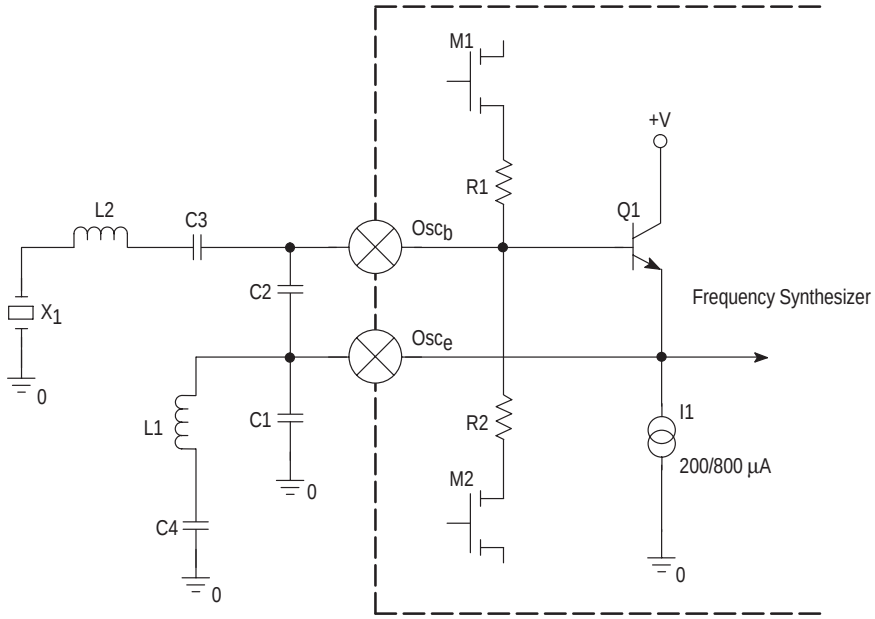
$$X_{C3}(max) >= 2[\Delta F_f \text{ (ppm)}] \, Z(crystal)$$

and

$$X_C(min) = \frac{X_C(max)}{4}$$

This results in an adjustable change in the operating frequency of $+[\Delta F_f \text{ (ppm)}]$ and $-[\Delta F_f \text{ (ppm)}]/2$. If ratios nearer to 1:1 are used for $X_{C3}(max)$ and X_{L2}, the tuning range will be skewed with a wider $-[\Delta F_f \text{ (ppm)}]$ but at the expense of less adjustability over the $+[\Delta F_f \text{ (ppm)}]$ range.

Figure 28. Colpitts Oscillator Configured for Overtone Operation



7B. MAIN LOOP FILTER DESIGN — CONVENTIONAL

The current output of the charge pump allows the loop filter to be realized without the need of any active components. The preferred topology for the filter is illustrated in Figure 29.

The R_o/C_o components realize the primary loop filter. C_a is added to the loop filter to provide for reference sideband suppression. If additional suppression is needed, the R_x/C_x realizes an additional filter. In most applications, this will not be necessary. If all components are used, this results in a fourth order PLL, which makes analysis difficult. To simplify this, the loop design will be treated as a second order loop (R_o/C_o), and additional guidelines are provided to minimize the influence of the other components. If more rigorous analysis is needed, mathematical/system simulation tools should be used.

Component	Guideline
C_a	$<0.1 \times C_o$
R_x	$>10 \times R_o$
C_x	$<0.1 \times C_o$

The focus of the design effort is to determine what the loop's natural frequency, ω_o, should be. This is determined by R_o, C_o, K_p, K_v, and N_t. Because K_p, K_v, and N_t are given, it is only necessary to calculate values for R_o and C_o. There are three considerations in selecting the loop bandwidth:

1. Maximum loop bandwidth for minimum tuning speed.
2. Optimum loop bandwidth for best phase noise performance.
3. Minimum loop bandwidth for greatest reference sideband suppression.

Usually a compromise is struck between these three cases, however, for a fixed frequency application, minimizing the tuning speed is not a critical parameter.

To specify the loop bandwidth for optimal phase noise performance, an understanding of the sources of phase noise in the system and the effect of the loop filter on them is required. There are three major sources of phase noise in the phase–locked loop — the crystal reference, the VCO, and the loop contribution. The loop filter acts as a low–pass filter to the crystal reference and the loop contribution. The loop filter acts as a high–pass filter to the VCO with an in–band gain equal to unity. The loop contribution includes the PLL IC, as well as noise in the system; supply noise, switching noise, etc. For this example, a loop contribution of 15 dB has been selected.

The crystal reference and the VCO are characterized as high–order 1/f noise sources. Graphical analysis is used to determine the optimum loop bandwidth. It is necessary to have noise plots from the manufacturers of both devices. This method provides a straightforward approximation suitable for quickly estimating the optimal bandwidth. The loop contribution is characterized as white–noise or low–order 1/f noise, given in the form of a noise factor which combines all the noise effects into a single value. The phase noise of the crystal reference is increased by the noise factor of the PLL IC and related circuitry. It is further increased by the total divide–by–N ratio of the loop. This is illustrated in Figure 30. The point at which the VCO phase noise crosses the amplified phase noise of the crystal reference is the point of the optimum loop bandwidth. In the example of Figure 30, the optimum bandwidth is approximately 15 kHz.

To simplify analysis further, a damping factor of 1 will be selected. The normalized closed loop response is illustrated in Figure 31 where the loop bandwidth is 2.5 times the loop natural frequency (the loop natural frequency is the frequency at which the loop would oscillate if it were unstable). Therefore, the optimum loop bandwidth is 15 kHz/2.5 or 6.0 kHz (37.7 krads) with a damping coefficient, $\zeta \sim 1$. T(s) is the transfer function of the loop filter.

where

N_t = Total PLL Divide Ratio — 8 x N
where (N = 25 ... 40),
K_v = VCO Gain – 2π Hz/V,
K_p = Phase Detector/Charge Pump Gain – A
= $(|I_{OH}| + |I_{OL}|) / 4\pi$.

Technically, K_v and K_p should be expressed in radian units [K_v (rad/V), K_p (A/rad)]. Since the component design equation contains the $K_v \times K_p$ term, the 2π cancels and the value can be expressed as AHz/V (amp hertz per volt).

Figure 29. Loop Filter

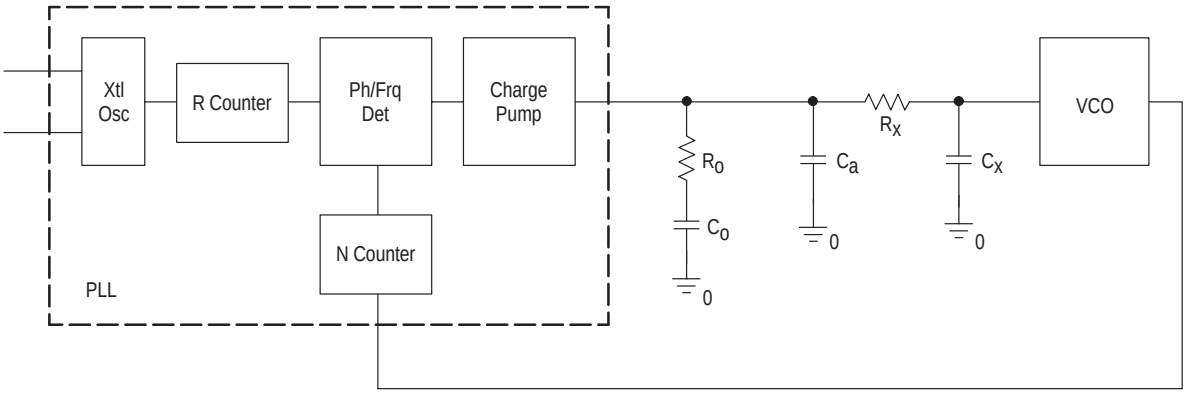


Figure 30. Graphical Analysis of Optimum Bandwidth

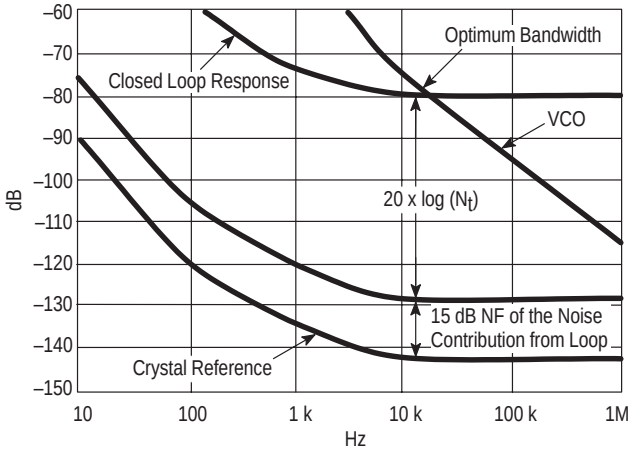
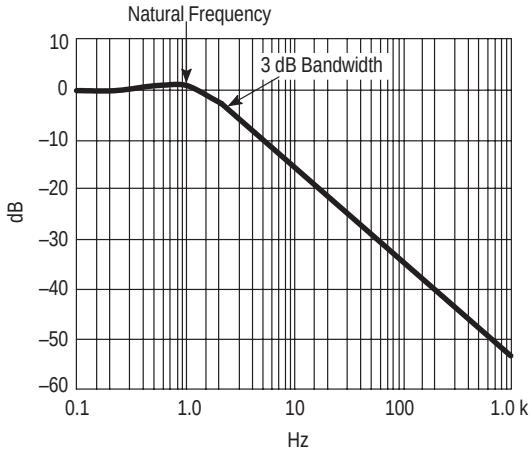


Figure 31. Closed Loop Frequency Response for ζ = 1



In summary, follow the steps given below:

Step 1: Plot the phase noise of crystal reference and the VCO on the same graph.

Step 2: Increase the phase noise of the crystal reference by the noise contribution of the loop.

Step 3: Convert the divide–by–N to dB (20log 8 x N) and increase the phase noise of the crystal reference by that amount.

Step 4: The point at which the VCO phase noise crosses the amplified phase noise of the crystal reference is the point of the optimum loop bandwidth. This is approximately 15 kHz in Figure 30.

Step 5: Correlate this loop bandwidth to the loop natural frequency per Figure 31. In this case the 3.0 dB bandwidth for a damping coefficient of 1 is 2.5 times the loop's natural frequency. The relationship between the 3.0 dB loop bandwidth and the loop's "natural" frequency will vary for different values of ζ. Making use of the equations defined in Figure 32, a math tool or spread sheet is useful to select the values for R_O and C_O.

Appendix: Derivation of Loop Filter Transfer Function

The purpose of the loop filter is to convert the current from the phase detector to a tuning voltage for the VCO. The total transfer function is derived in two steps.

Step 1 is to find the voltage generated by the impedance of the loop filter.

Step 2 is to find the transfer function from the input of the loop filter to its output. The "voltage" times the "transfer function" is the overall transfer function of the loop filter. To use these equations in determining the overall transfer function of a PLL, multiply the filter's impedance by the gain constant of the phase detector, then multiply that by the filter's transfer function. Figure 33 contains the transfer function equations for the second, third, and fourth order PLL filters.

PSpice Simulation

The use of PSpice or similar circuit simulation programs can significantly reduce laboratory time when refining a PLL design. The following describes the use of behavioral modeling to develop useful models for studying loop filter performance. In many applications the levels of sideband spurs can also be studied.

Behavioral modeling is chosen, as opposed to discrete device modeling, to improve performance and reduce simulation time. PLL devices can contain several thousand individual transistors. To simulate at this level can result in generation of an enormous amount of data when compared to a simpler behavioral model. For example, a logic NAND gate can contain several transistors. Each of these requires a data set for each of the transistor terminals. If a half dozen transistors are used in the gate design, both current and voltage measurements for each terminal of each device for every node in the circuit is calculated. The gate can be expressed as a behavioral model, which is treated and simulated as a single device. Since PSpice sees this as a single rather than multiple devices, the amount of accumulated data is much less, resulting in a faster simulation.

For applications using integrated circuits such as PLLs, it is desirable to investigate the performance of the circuitry added externally to the integrated circuit. By using behavioral modeling rather than discrete device modeling to represent the integrated circuit, the engineer is able to study the performance of the design without the overhead contributed by simulating the integrated circuit.

Phase Frequency Detector Model

The model for the phase frequency detector is derived using the waveforms shown in Figure 20. Two signals are present at the input of the phase frequency detector. These are the reference input and the feedback from the VCO and/or prescaler. The two signals are compared to determine the lag/lead relationship between the two signals and pulses generated to represent the leading edge of each signal. A pulse whose width equals the lead of one input signal over the other is generated by an RS flip–flop (RSFF). One RSFF generates a pulse whose width equals the lead of the reference signal over the feedback signal, and a second RSFF generates a signal whose width is the lead of the feedback signal over the reference signal. The logical model for the phase frequency detector is shown in Figure 34.

Figure 32. Design Equations for the Second Order System

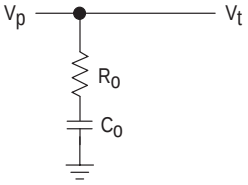
$$T(s) = \frac{R_0C_0s + 1}{\left(\frac{NC_0}{K_pK_v}\right)s^2 + R_0C_0s + 1} = \frac{\left(\frac{2\zeta}{\omega_0}\right)s + 1}{\left(\frac{1}{\omega_0^2}\right)s^2 + \left(\frac{2\zeta}{\omega_0}\right)s + 1}$$

$$\left(\frac{NC_0}{K_pK_v}\right) = \left(\frac{1}{\omega_0^2}\right) \rightarrow \omega_0 = \sqrt{\frac{K_pK_v}{NC_0}} \rightarrow \boxed{C_0 = \left(\frac{K_pK_v}{N\omega_0^2}\right)}$$

$$R_0C_0 = \left(\frac{2\zeta}{\omega_0}\right) \rightarrow \zeta = \left(\frac{\omega_0R_0C_0}{2}\right) \rightarrow \boxed{R_0 = \left(\frac{2\zeta}{\omega_0C_0}\right)}$$

Figure 33. Overall Transfer Function of the PLL

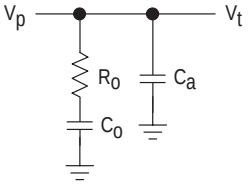
For the Second Order PLL:



$$Z_{LF}(s) = \frac{R_0C_0s + 1}{C_0s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1 \quad , \quad V_p(s) = K_p(s)Z_{LF}(s)$$

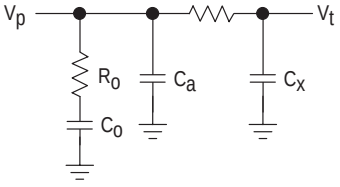
For the Third Order PLL:



$$Z_{LF}(s) = \frac{R_0C_0s + 1}{C_0R_0C_as^2 + (C_0 + C_a)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1 \quad , \quad V_p(s) = K_p(s)Z_{LF}(s)$$

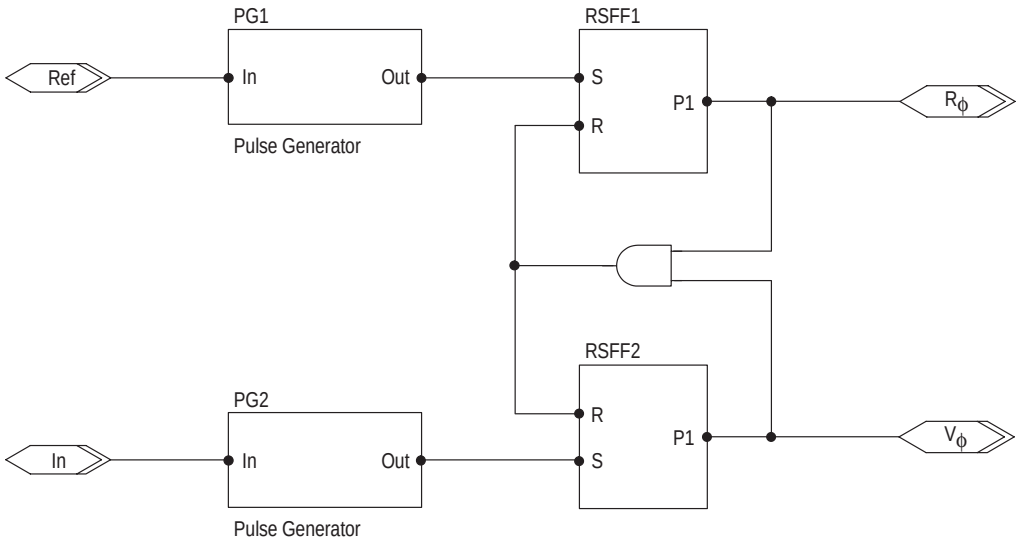
For the Fourth Order PLL:



$$Z_{LF}(s) = \frac{(R_0C_0s + 1)(R_xC_xs + 1)}{C_0R_0C_aR_xC_xs^3 + [(C_0 + C_a)R_xC_x + C_0R_0(C_x + C_a)]s^2 + (C_0 + C_a + C_x)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = \frac{1}{(R_xC_xs + 1)} \quad , \quad V_p(s) = K_p(s)Z_{LF}(s)$$

Figure 34. Phase Frequency Detector Logic Diagram



The behavioral model of the phase frequency detector shown in Figure 35 is derived using the phase frequency detector logic diagram. Behavioral models for the pulse generator, AND gate (Figure 36), and RS flip–flops (Figure 37) are created using analog behavioral blocks. The pulse generator is created using a delay block and a “gate” defined by the behavioral expression:

$$\text{If } [V(v1) \geq 1 \ \& \ V(v2) \ , 1, 5, 0]$$

v1 and v2 represent the two inputs to the block.

This is the behavioral expression for an AND gate with one input inverted. The addition of the delay element produces a pulse whose width equals the delay element.

The pulses appearing at the output of HB1 and HB2 (Figure 35) are used to set the flip–flops, RSFF1, and RSFF2. The leading pulse will set the appropriate flip–flop resulting in a high at the output of that flip–flop. The output of this flip–flop will remain high until the arrival of the second (or lagging) pulse sets the second RS flip–flop. The presence of a high on both RS flip–flop outputs results in the generation of the reset pulse. The reset pulse is generated by the analog behavioral block (configured as an AND gate) and the delay element. The delay element is necessary to eliminate the zero delay paradox of input to output to input.

The output of the phase frequency detector is two pulse trains appearing at R_ϕ and V_ϕ. When the PLL is locked, the pulses in both pulse trains will be of minimum width. When the phase frequency detector is out of lock, one pulse train will consist of pulses of minimum width while the width of the pulses in the second train will be equal to the lead/lag relationship of the input signals. If the Ref input leads ‘In’, the pulse train at R_ϕ will consist of pulses whose width equals the lead of Ref. If Ref lags ‘In’, the width of the pulses appearing at V_ϕ will equal this lag.

The terms lead and lag used in this explanation represent an occurrence in time rather than a phase relationship. At any condition other than locked, one input (either In or Ref), will be of a higher frequency. This results in the arrival of the pulse at that input ahead of the pulse at the other input, or leading. The second then is lagging.

To simulate the operation of the phase frequency detector in an actual circuit, a charge pump needs to be added. The behavioral model for this is shown in Figure 38. Two voltage–to–current behavioral models are used to produce the charge pump output. Two voltage–controlled switches with additional behavioral models, monitor the voltage of the output of the charge pump and clamp to 0 or V_{CC} to simulate a real circuit.

To ensure the model conforms to the PLL, the delay blocks in the phase frequency detector should be set to the expected value as specified by the MC145181 data sheet. In addition, the charge pump sink and source current behavioral model should also be set to deliver the desired current and V_{CC} specified to ensure correct clamping.

Modeling the VCO

The VCO (Figure 39) is also modeled using Analog Behavioral Modeling (ABM). The model used in the following examples assumes a linear response; however, the control voltage equation can be modified as desired. The circuit is modeled as a sine generator controlled by the control voltage. The sine generator can be modeled using the EVALUE function or the ABM function. In Figure 39, the EVALUE function is used to generate the divided output and the ABM function is used for the undivided output. Either the GVALUE or the ABM/I function can be used for the control voltage.

Figure 35. Behavioral Model of the Phase Frequency Detector

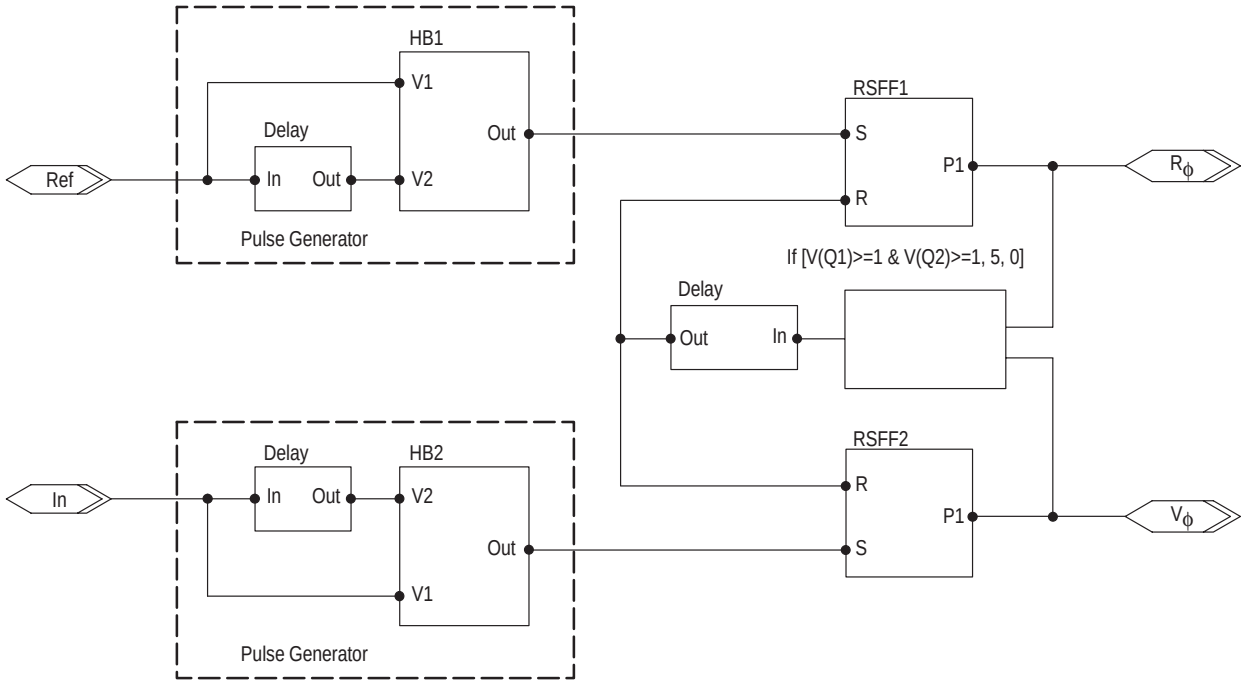


Figure 36. Behavioral Block Used for the Pulse Generator

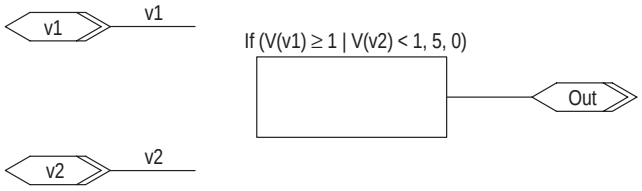


Figure 37. Behavioral Block Used as an RS Flip–flop

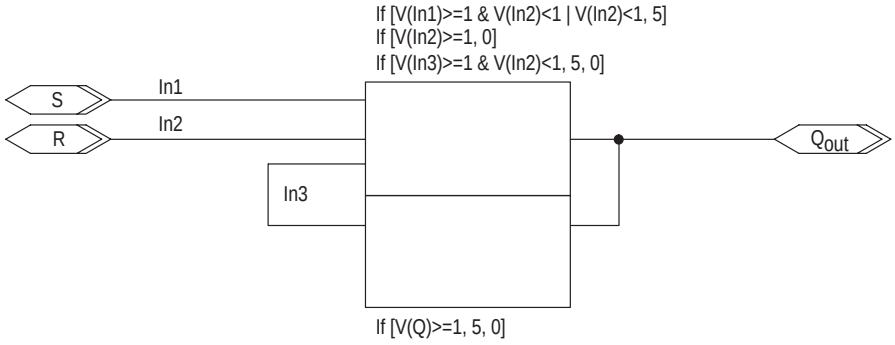


Figure 38. Charge Pump Model

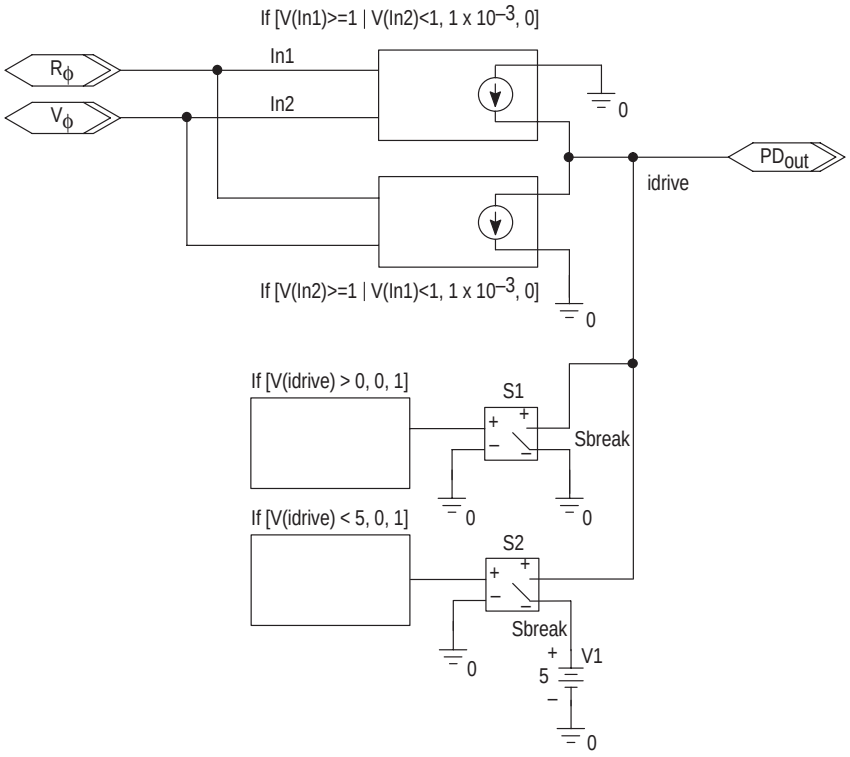
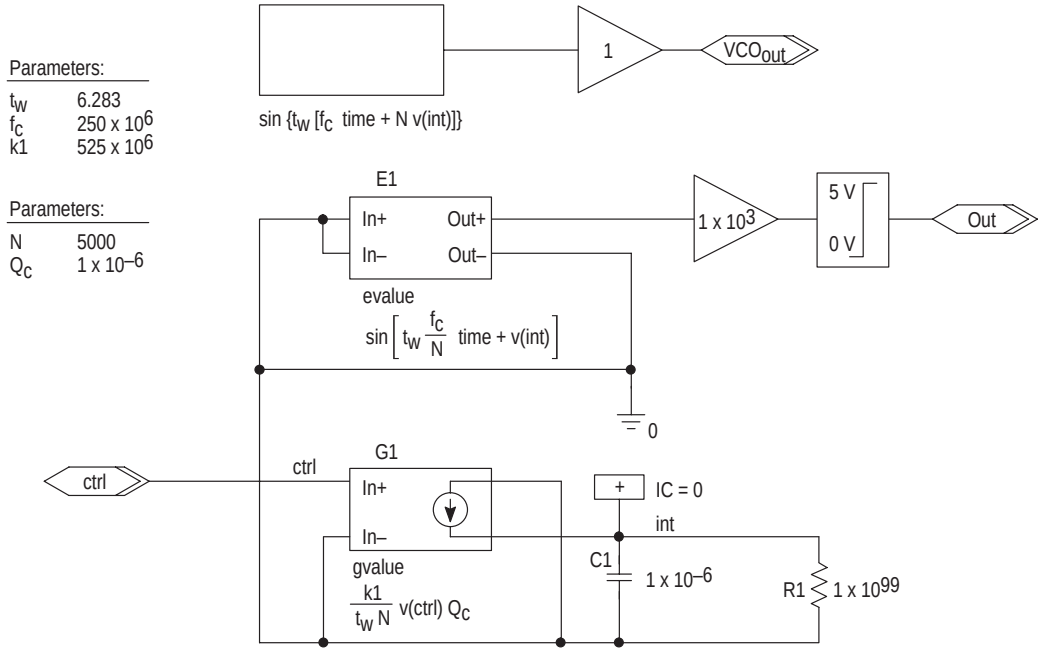


Figure 39. VCO Behavioral Model



The equation for the sine generator is:

$$e = \sin\left[t_W \frac{f_C}{N} \text{ time} + v(\text{int})\right] \quad .$$

f_C is defined as the output frequency when the control voltage is 0. This is the expected VCO frequency before frequency division. For the purpose of simulation, the counter value, N, has been written into the equation to ensure the correlation between the modeled circuit and the mathematical loop filter calculations. t_W is 2π; additional decimal places can be added as needed. v(int) is the control voltage effect and is defined in these examples as:

$$v(\text{int}) = \frac{k1}{t_W N} v(\text{cntl}) \; 1 \times 10^{-6} \quad .$$

where k1 is the VCO gain in rad/V.

The value C1 in the schematic of the VCO can be arbitrarily changed; however, the value must match that of Q_C. Q_C determines the value of the current to be integrated by the capacitor C1. R1 is arbitrarily set to 1×10^{99} and is not an active part of the circuit; however, it must be included to prevent open pin errors from the PSpice software. The GVALUE function is used to perform the generation of v(int). There is some interaction between the integrator, (GVALUE output and C1) and R1. V(int) is a continuous ramp that is loaded by the resistance of R1. Unless the GVALUE output current is sufficiently large for the value chosen for R1, the VCO control voltage required to maintain lock will increase throughout the simulation producing nonlinear operation. Modifications to the circuit can be performed either by changing the values in the parameter list or for major changes to the VCO characteristics, the equations for the sine generator, or control voltage can be altered.

The output of the sine generator is amplified by 1000 to produce a sharp rise/fall time and the output limited to swing between the values of 0 V and 5 V to convert it to a digital output. The resultant circuit/symbol accepts a voltage input from the loop filter and produces a square wave output at the desired frequency. This frequency should be chosen to represent the frequency present at the output of the N counter of the PLL frequency synthesizer.

The second output represented by the ABM function is a sine wave output of the frequency expected from the actual VCO. The primary purpose of this output is to allow full frequency simulation for spectrum analysis. By running a transient analysis of sufficient time, it is possible to determine spur content and level. If sufficient resolution is used in the simulation, the PSpice probe FFT transform can be used to provide the typical spectrum analyzer display.

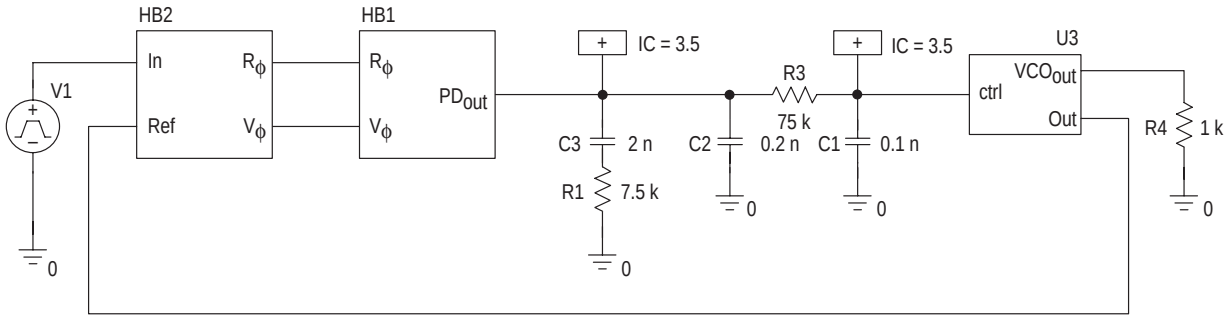
Loop Filter Simulation

The circuit shown in Figure 40 is used to simulate the closed loop operation for a single charge pump output. Component values for the loop filter should be computed using information from the previous section. Initial conditions can be set using the “IC1” symbol with starting values specifying the initial condition.

By adjusting component values for the loop filter, performance of the closed loop operation can be monitored. The control voltage to the input of the VCO can be monitored for a variety of conditions including settling time, lock time, and ripple present at the VCO input. In addition, the output of the VCO can be monitored for spur sidebands caused by ripple on the loop filter output; however, expected operation at high frequencies may be difficult due to the excessive data that can be generated.

As the divider ratio, N, increases for a fixed step frequency, the number of data points required to obtain sufficient information to overcome aliasing problems may become excessively large. In addition, the number of samples required should be three or more per cycle. For VCO frequencies in the range of 500 MHz, this means the step ceiling needs to be in the range of 100 to 500 ps. If a simulation time of 1 ms is needed, the actual computer time can be several hours with data accumulation in the 1– to 2–Gbyte range.

Figure 40. PLL Closed Loop Model



7C. MAIN LOOP FILTER DESIGN — ADAPT

Introduction

For PSpice simulation, the schematic model shown in Figure 41 was chosen. The classical PLL model employing a phase–frequency detector, a VCO, and an adaptive loop filter is used to simplify visualization of circuit operation. The parameter tables allow for modification of circuit performance by providing an easy method for altering critical values without necessitating changes to sub–level schematics. The definition for the terms are:

t_W = 2π,

f_r = reference frequency,

t_d = time delay; allows delay of the start of the high current mode (used to perform reference spur measurements),

CPL = charge pump low current,

CPH = charge pump high current,

N = N counter value,

S_Z = amount the N counter is being increased (or decreased) by,

S_t = number of f_r cycles that CPH is active; this value is either 16, 32, 64, or 128,

VCPHH = charge pump voltage – high,

VCPHL = charge pump voltage – low,

K1 = VCO gain (Hz/volt),

f_C = VCO frequency at 0 V control voltage,

H = reference spur scaling factor.

Modeling the Phase–frequency Detector

Figure 42 is a schematic of the phase–frequency detector. It includes the reference oscillator model, phase–frequency detector model, and charge pump models. V1 is the control element used to generate the step time for switching between CPL and CPH. The signal source VPULSE, is used to simulate the timer that controls when CPL and CPH are turned on. PW calculates the pulse width that simulates the counter from the values for S_t and f_r that are entered in the parameter tables on the top level schematic.

Figure 41. Top Level PLL Model

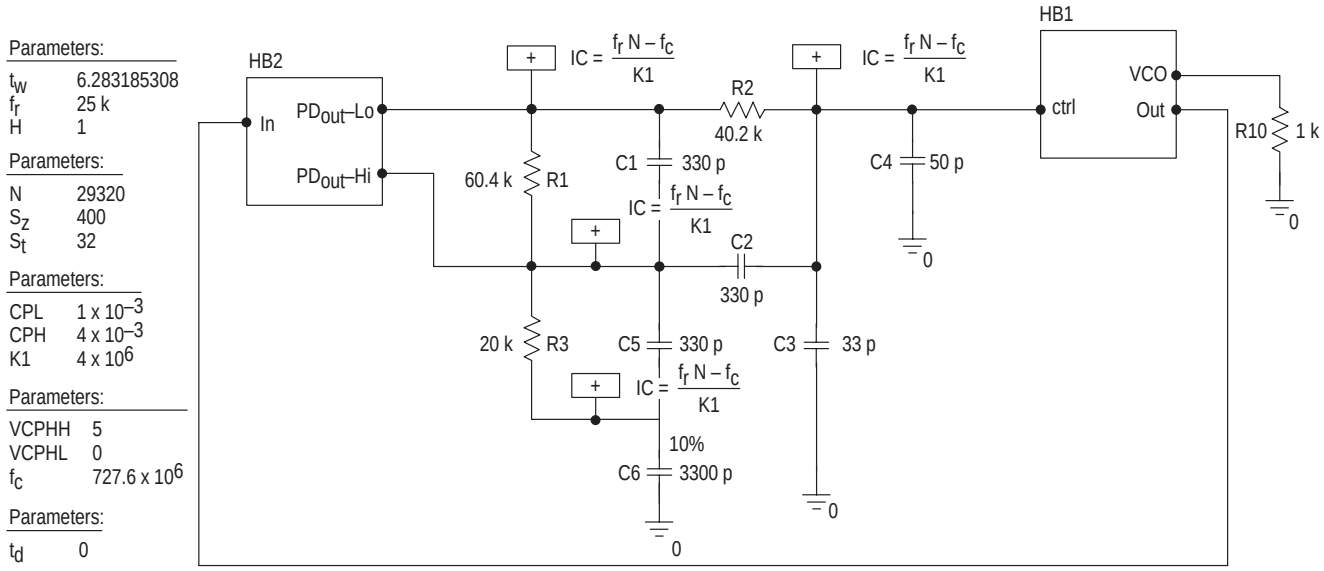
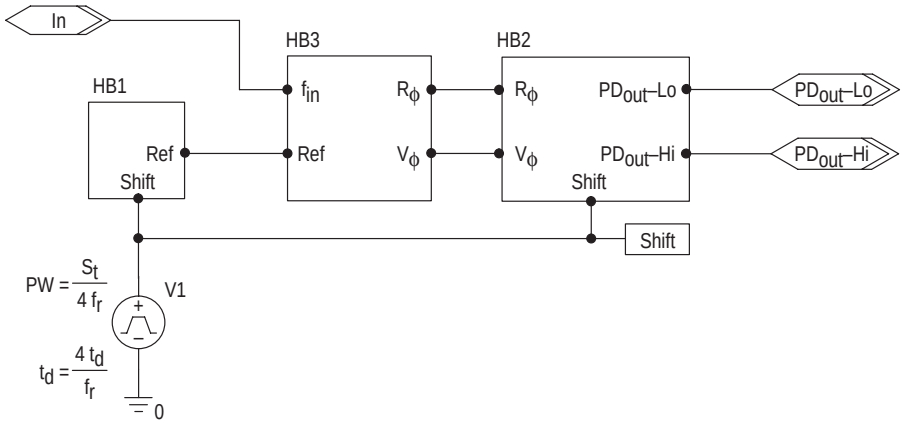


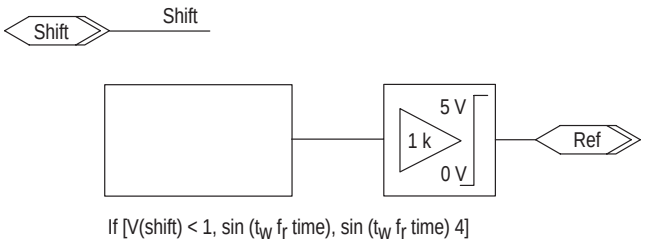
Figure 42. Phase–frequency Detector with Dual Charge Pumps



Reference Oscillator

The reference oscillator is shown in Figure 43. The oscillator is modeled using an analog behavioral block. The function for the block is written as an “If” condition. If the signal shift is low, the reference frequency f_r will be generated if shift is high, a signal of four times f_r will be generated. The limiter/gain block converts the low level sine wave output of the analog behavioral block into a square wave. The values of 0 for the low value and 5 for the high value are used throughout. These values are chosen out of habit and are not critical in an analog behavioral environment, providing the conformity is universal throughout the design.

Figure 43. Reference Oscillator



Phase–frequency Detector

The actual phase–frequency detector model minus reference oscillator and charge pumps is shown in Figure 44. The detector is composed of three delay modules: a behavioral AND gate, and two RS flip–flops. The STP function resets the phase/frequency detector logic on initiation of the simulator. The circuit for the behavioral RS flip–flop is shown in Figure 45.

The RS flip–flop equation illustrates the benefit of using the behavioral block instead of using a primitive logic element. A delay block and the behavioral gate equation generate a pulse whose width is equal to the value of the delay block. To generate the output using a primitive logic element such as a NAND gate, an inverter would be necessary to invert one of the NAND inputs. This approach requires three elements to be used instead of the two of the behavioral approach just for the pulse generator. In the behavioral approach, the equation for the behavioral AND gate is folded into the RS flip–flop, eliminating a separate gate altogether. Constructing the model with classic logic elements would require two NOR gates for the flip–flop, a delay element, an inverter, and an AND gate; five elements as compared with three for the behavioral approach. Since the RS flip–flop is used in two places in the model, four less components are needed for simulation. Since the speed of the simulation is directly impacted by the number of components being simulated, any reduction in the total number of components is a savings in simulation time and computer memory.

The RS flip–flops generate the lead or lag outputs that are used to “steer” the VCO. The pulse generator equation produces narrow pulses coincident with the leading edge of each of the input signals. These pulses set the appropriate RS flip–flop. Once set, the leading flip–flop must wait until the lagging flip–flop is also set. The behavioral AND gate provides the necessary output pulse to reset the flip–flops. The delay element placed at the output of the behavioral AND gate prevents an undefined state for the detector. The value 5 ns is chosen to correspond with the data sheet. The logic functions as a three state phase/frequency detector with an operating range of $\pm 2\pi$. R_ϕ and V_ϕ deliver positive pulses, whose width represents the amount of the lead of each input over the other input.

Figure 44. Phase–frequency Detector Logic

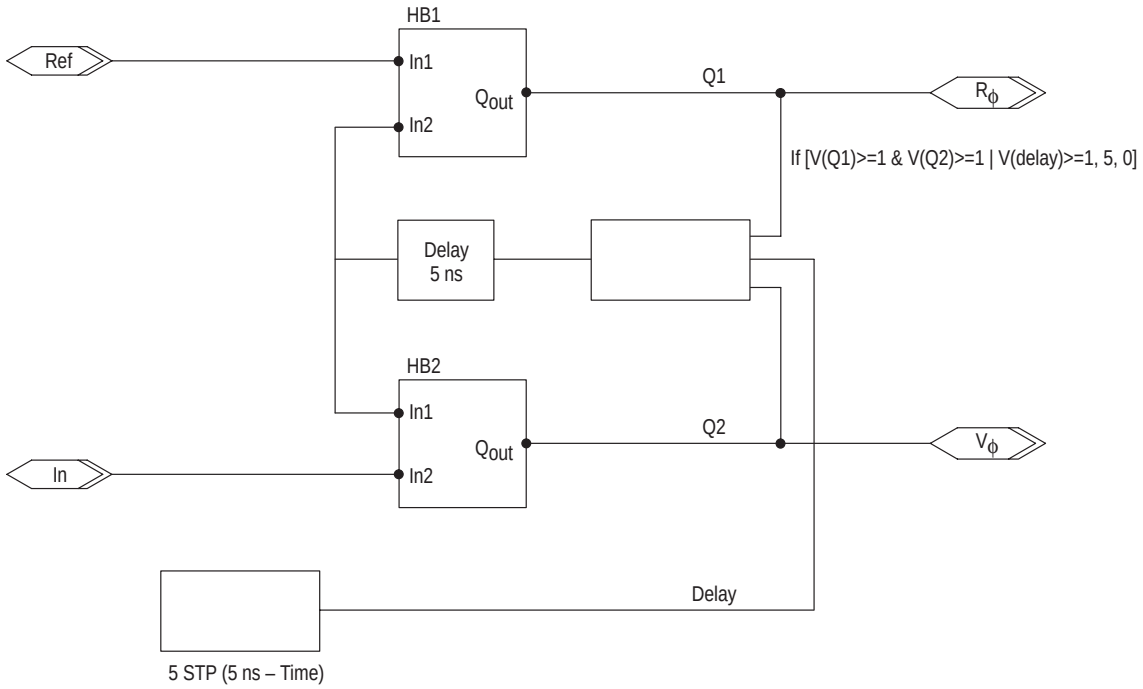
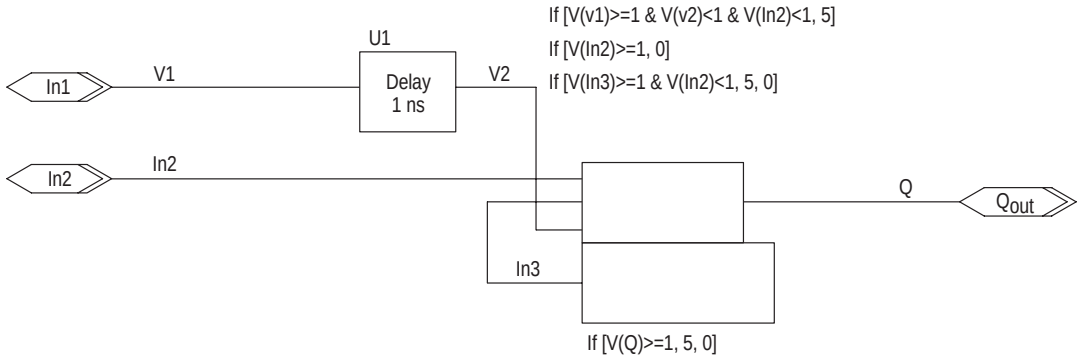


Figure 45. Behavioral RS Flip–flop



Charge Pump Model

The schematic used for the charge pump in the phase–frequency detector model is shown in Figure 46. Each charge pump is made from two analog behavioral blocks. The blocks chosen are three input behavioral blocks with current outputs. The two blocks are connected in push–pull to generate the appropriate source and sink output. The output of each block is defined using an “If” statement to monitor the input signals and generate the correct output at the appropriate time.

One note about this type of design. SPICE does not limit the output voltage swing necessary to generate the programmed current. It is possible to implement values for the loop filter, which will cause the charge pump to exceed the rail voltage. To limit the output voltage to prevent exceeding the value of the rails, the two behavioral blocks, voltage–controlled switches S1 and S2, and constants VCPHH and VCPHL are added. S1 and S2 on/off resistance is set to 1 Ω and 1 x 10^{12} Ω, and the off/on voltage is set to 0 V and 1 V to correspond to the behavioral blocks. The values defined by the constants are accessible from the parameter tables on the top level schematic.

VCO Model

The model used for simulating the VCO is shown in Figure 47. The VCO is composed of a sine wave generator and a control element. An analog behavioral block is used as a sine wave generator and a GVALUE element is used as a control element. The GVALUE is operated as an integrator. The output of the integrator is defined as

$$v(int) = k1\ v(ctrl)\ Q_C \quad .$$

The block designated to provide the feedback to the phase–frequency detector uses a single input analog behavioral block. The signal shift generated by V1 in the phase–frequency detector block is used to define the output frequency of the behavioral block. In this manner, the switching of the N and R values for the programmable counters can be simulated. In the implementation shown, the two frequencies will be either 25 kHz or 100 kHz when locked to the reference oscillator.

The other behavioral block is used to generate a VCO output dependent on the loop, but not contributing to the operation of the loop. This is used to emulate the actual VCO output with one modification. “H” has been added to the equation generating the sine wave. If H is defined as 1, the sine wave generated will be the same as the expected VCO output. If H is chosen as some value greater than 1, the frequency of the output will be reduced accordingly. This is useful when running simulations designed to show reference spur levels.

In cases where it is desirable to view reference spur levels, simulation can become difficult or impossible. For example, consider the circuit that is being discussed. This circuit represents the evaluation kit (MC145230EVK) using a VCO tunable between 733 MHz to 742 MHz, with a step frequency of 25 kHz.

NOTE

This example is for reference only. The maximum operating frequency of the MC145181 is 550 MHz. Operation of the VCO at frequencies greater than 550 MHz requires the inclusion of additional external division such as a prescaler.

To obtain useful information from the simulation, a sampling rate greater than the Nyquist limit must be used (three to five samples per cycle). This dictates a step size less than 1/2 nanosecond. Additionally, the reference frequency is only 25 kHz. To accurately represent the conditions for spur generation, the simulation time must be long enough to include a sufficient number of f_r periods. Otherwise, no spurs are generated. In addition, the data file system is limited to 2 Gbyte, either in the NT 4.0 operating system or in PSpice itself. If the file exceeds 2 Gbyte, the data is discarded. To simulate reference spur generation at 730 MHz, a 1 ms simulation time was chosen. The simulation ran for several hours and generated a data file just under 2 Gbyte. The result is shown in Figure 48. The plot obtained from the EVK is shown in Figure 49 for comparison.

Figure 46. CPL and CPH Charge Pumps

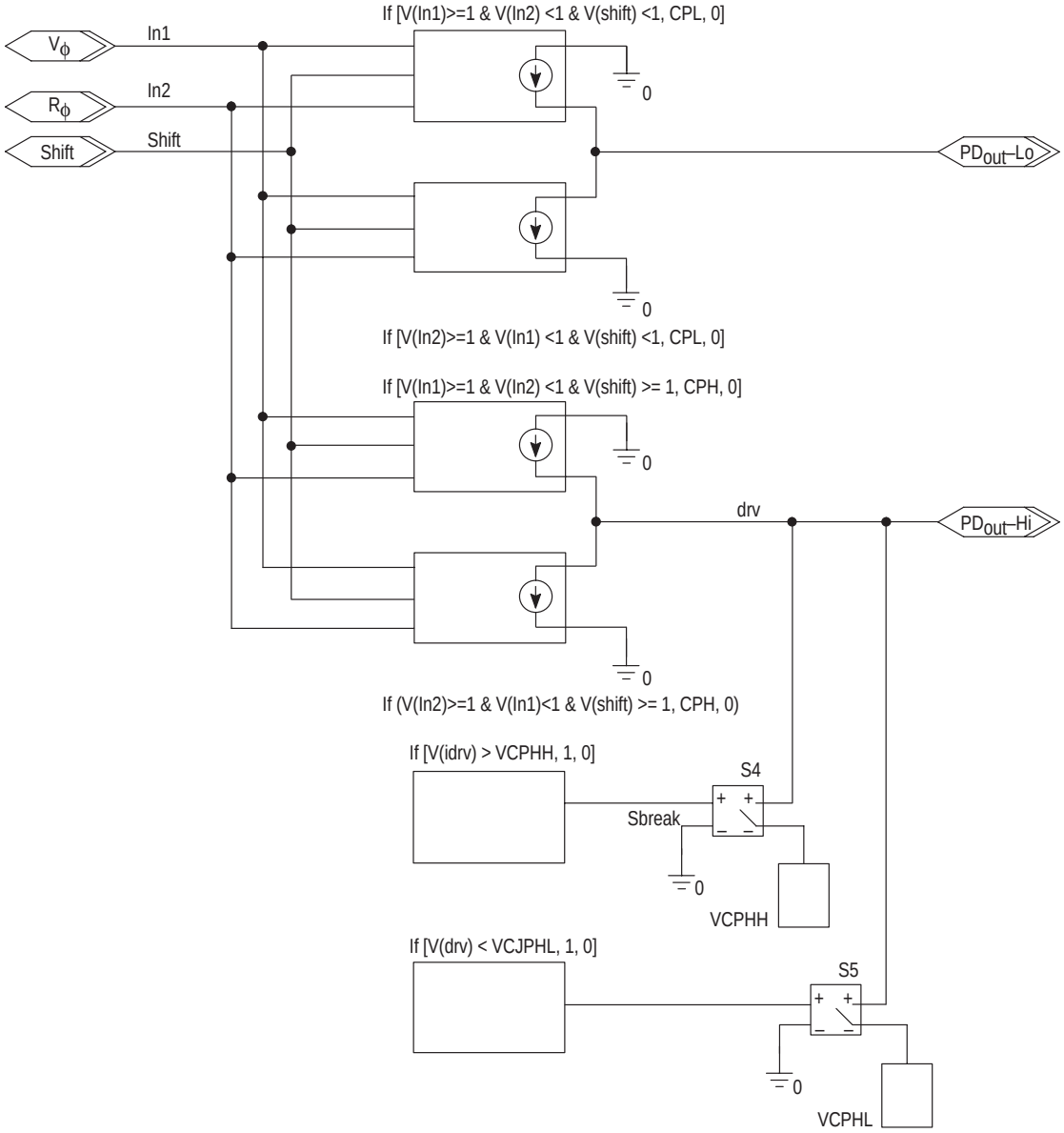


Figure 47. VCO Model

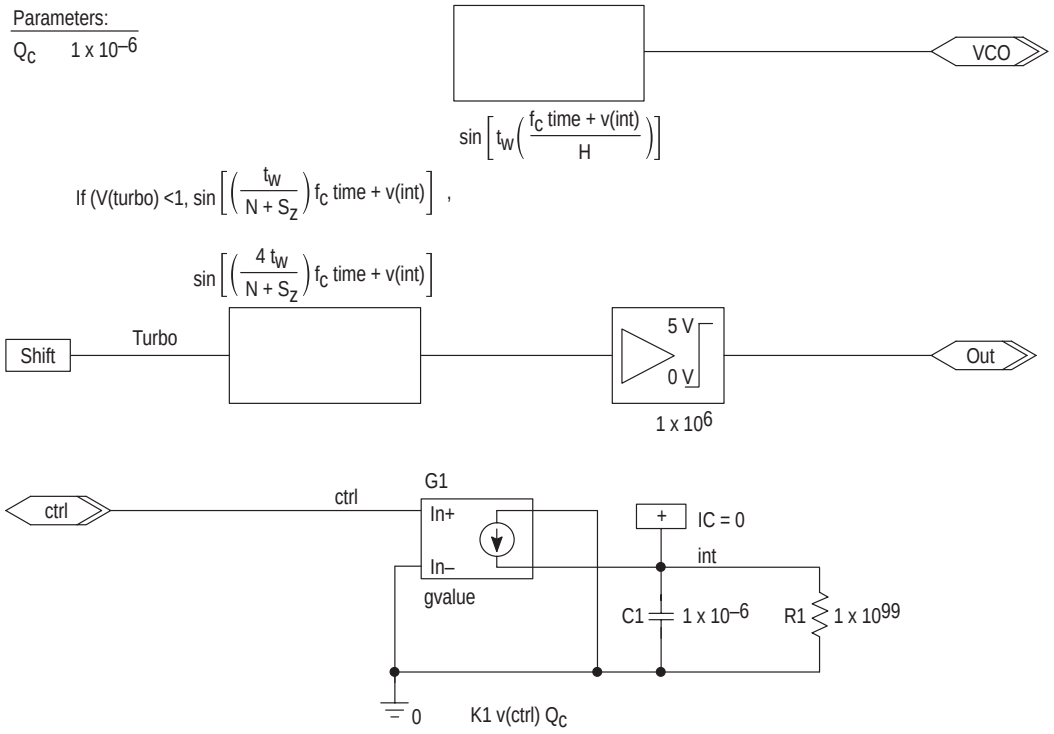


Figure 48. Reference Spur Simulation at 730 MHz

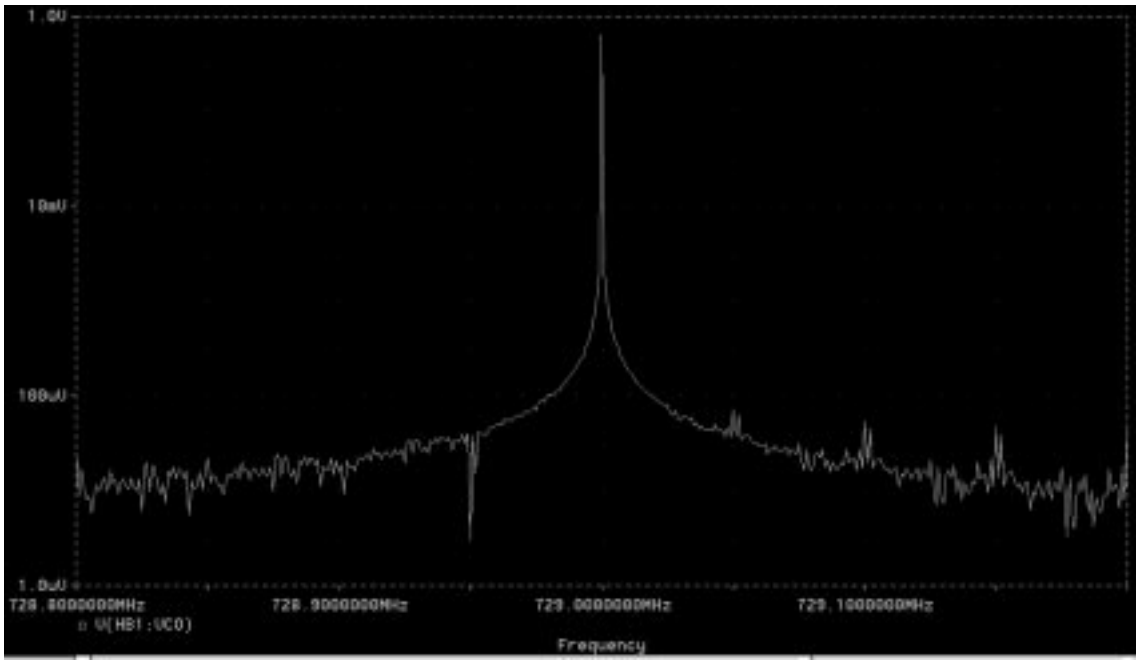
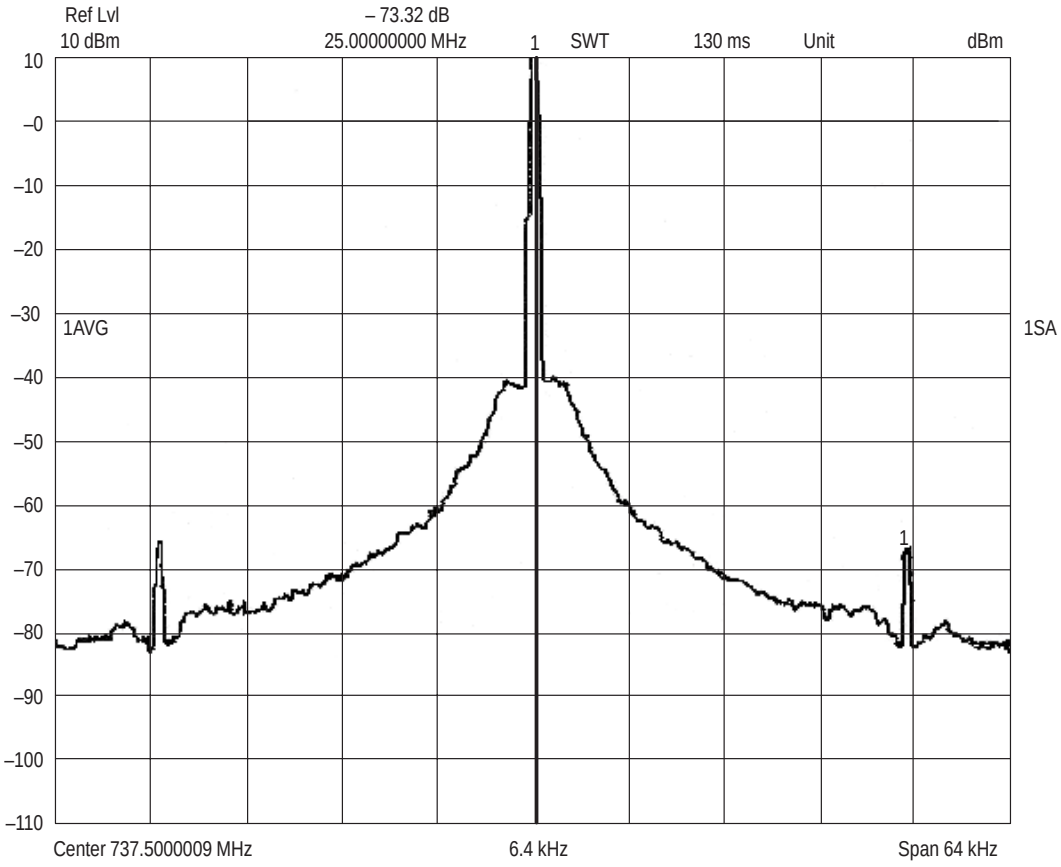


Figure 49. Sybil EVK Reference Spur Measurements



It should be noted that the reference spur values obtained from the simulation are lower than the values obtained from the actual EVK. This is because the simulation model is an “ideal” modeling of the PLL. To obtain results closer to the actual implementation, the models should be “massaged” to be more representative of the actual circuit. For example, spur levels more consistent with actual circuitry can be obtained by adding a resistance to ground at the input of the VCO to represent leakage. The value chosen should be consistent with VCO and circuit component performance.

To reduce simulation time, the H value may be used. By reducing the frequency of the VCO output, the number of samples required for simulation can also be reduced. The output shown in Figure 50 shows the result of dividing the VCO output of 730 MHz by 7.3 to produce a 100 MHz output. The reference spurs are better represented since adequate simulation time is possible.

To generate these outputs, the parameter values used were those shown on the top level schematic. The simulator was set to run a transient sweep, with t_d set for a delay that would prevent the 4X frequency from being started. The initial conditions were set to 1 V and the simulation run for 1 ms. VCO was monitored and the probe display button FFT was initiated. The X and Y axis were adjusted to those shown.

Note: These simulations are presented as the result of “ideal” models and may not accurately display real hardware. It would be best to load the VCO input with additional leakage devices such as a large resistance, to accurately display real conditions. These models are starting points for more accurate implementations.

Loop filter analysis is more accurate, since the predominate factors are in the loop filter itself. To simulate the performance of the loop filter, t_d is set for 0, N is set to the desired divider value, and S_Z is set to the desired step. For this example, 733 MHz was chosen.

NOTE

These values are for reference only. The maximum operating frequency of the MC145181 is 550 MHz. For VCO frequencies greater than 550 MHz, an added external divider such as a prescaler is necessary.

With the VCO model shown, V(ctrl) = 0 produces an output of 727.6 MHz and at V(ctrl) = 1.35 V, the VCO frequency would be 733 MHz; the minimum MC145230EVK default operating frequency. To show the response of the loop filter to a 10 MHz step at this operating frequency, S_Z = 10 MHz/ 25 kHz = 400. The simulation is run for 1 ms with a step ceiling of 100 ns. The result is shown in Figure 51.

If the simulation is examined over a longer period of time, the long term settling can be compared to the performance of the actual circuitry. The plot shown in Figure 52 shows the VCO control voltage with the display resolution set to 1 mV. This compares to the plot of frequency variation measurements made on the actual EVK. This plot is shown in Figure 53.

Figure 50. H Set to Generate a 100 MHz Output

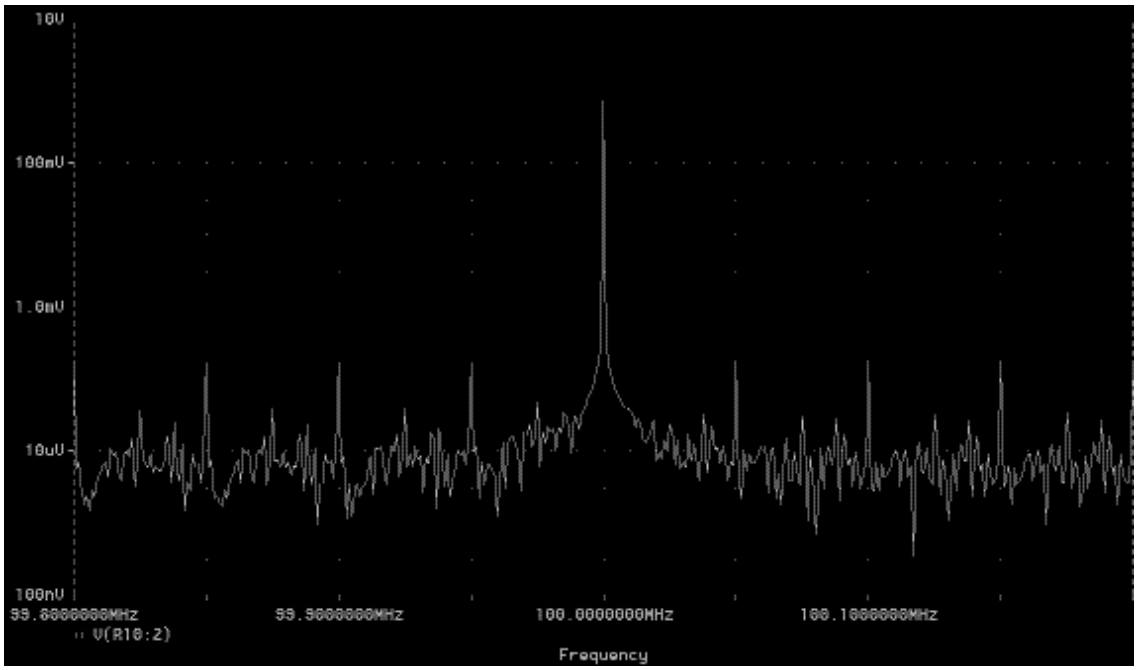


Figure 51. 10 MHz Step for an Operating Frequency of 729 MHz

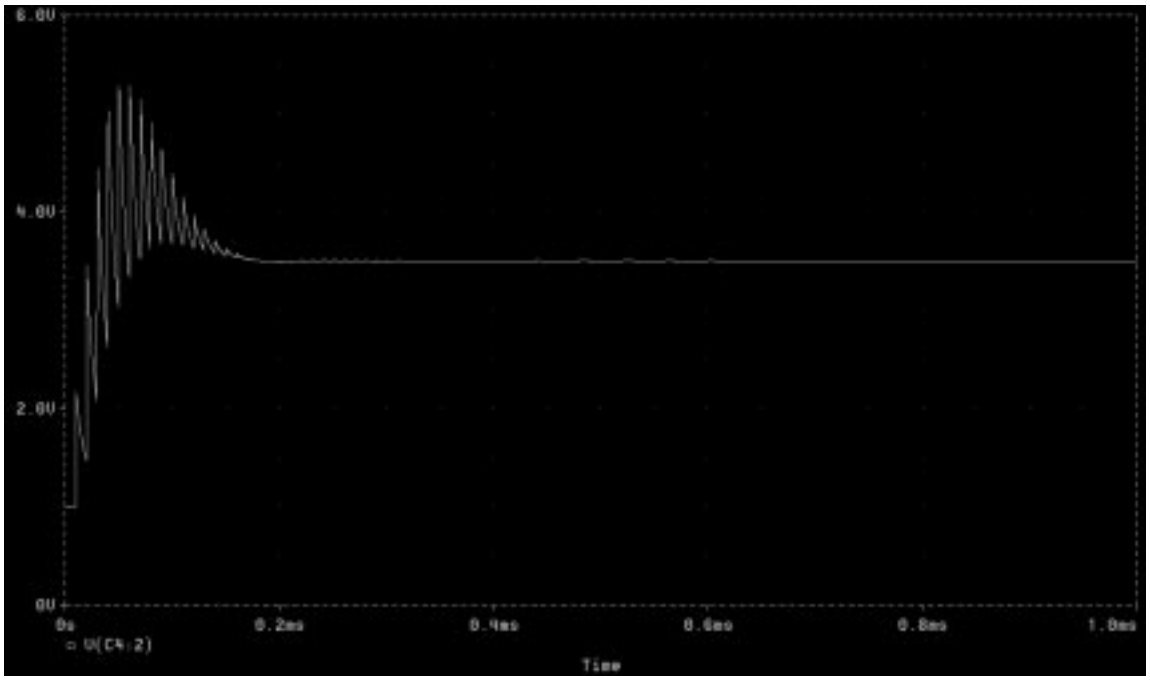


Figure 52. VCO Settling

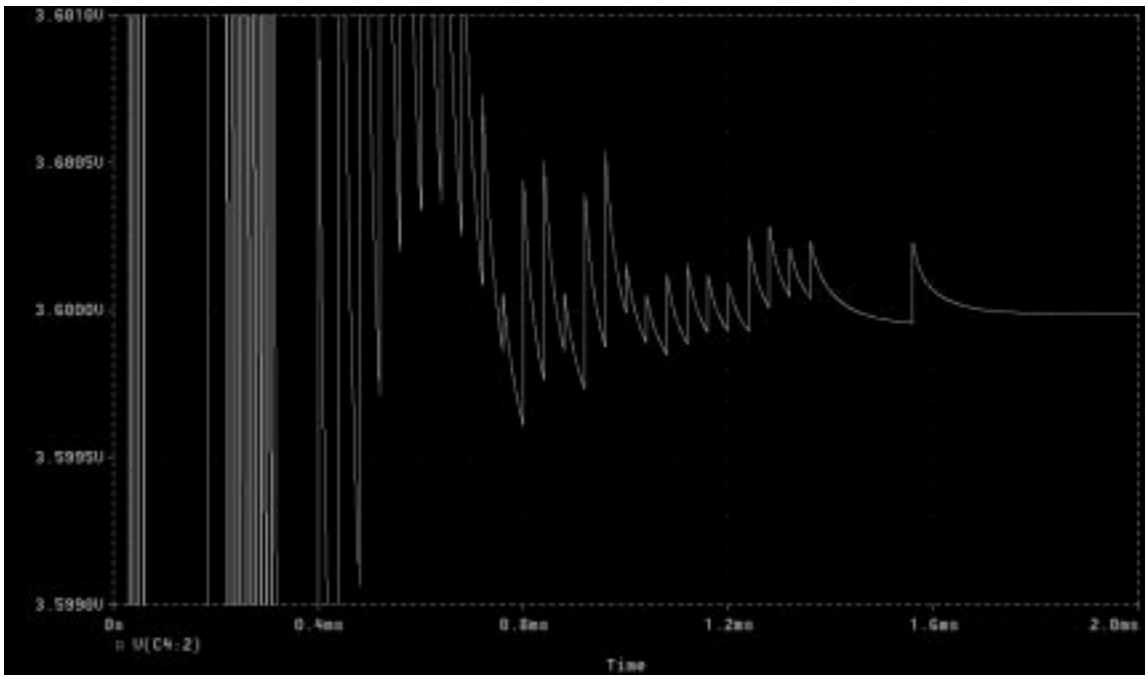
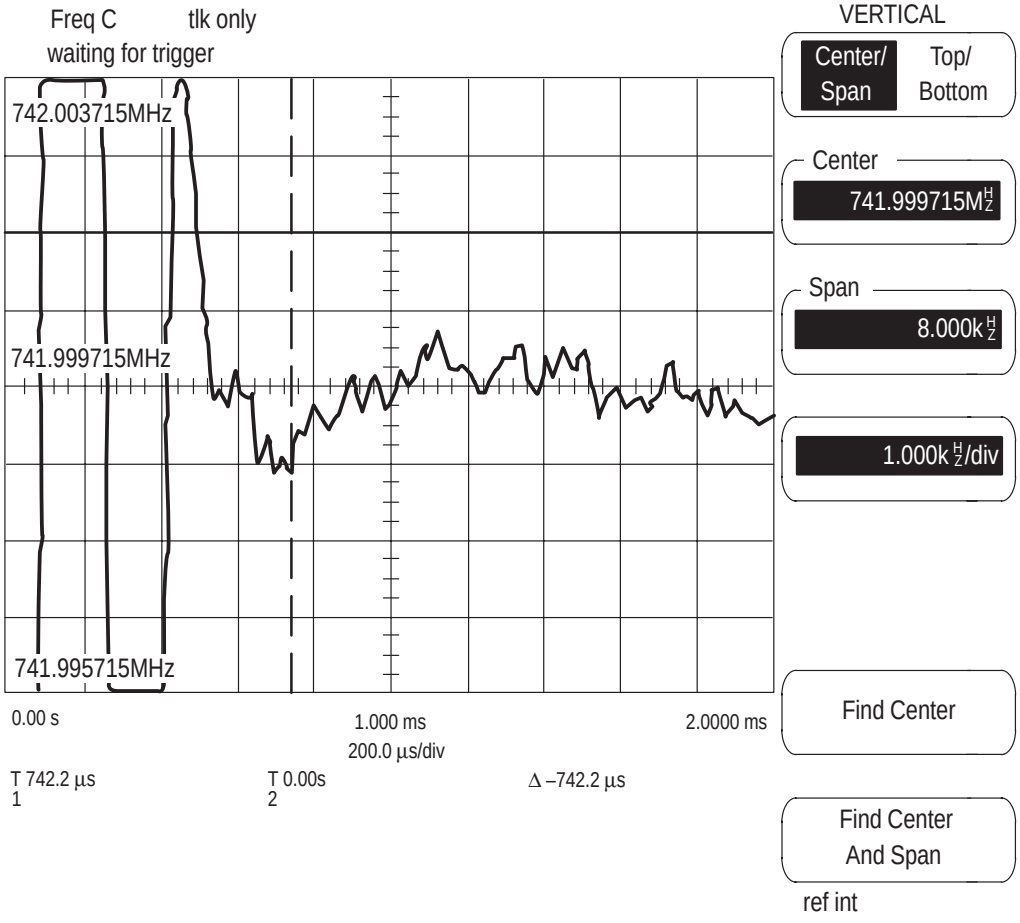


Figure 53. Frequency Settling of the EVK



It is noted that the results obtained from the simulation compare favorably to those obtained from the measurements of the EVK. The simulation display resolution is adjusted to represent the same ±4 kHz deviation as shown in Figure 53. Since variation in VCO control voltage is equal to the VCO frequency divided by the VCO gain, this axis may be redefined to show change in frequency rather than change in control voltage.

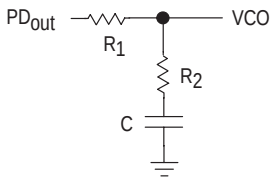
The models shown represent a “skeleton” that may be used to develop extensive and reliable simulations that can greatly reduce actual breadboarding and testing. In addition to the basic simulations shown, PSpice provides a method by which worst case and Monte Carlo evaluation can be performed on all, or selected components. By limiting the circuit to minimum necessary components, simulation can be performed using only the PSpice evaluation copy. In addition, the optional PSpice program Optimizer should allow refining the loop filter more easily.

While PSpice is a powerful tool, it is not without limits. Since it was designed to run on large mainframe computers, the PC is just now becoming powerful enough to make use of the capability of the simulator. A fast Pentium class processor with a large RAM and a hard drive of the Gbyte size is a necessity. Even with the most judicious planning, some simulations will “bump” the limits of the system.

7D. SECONDARY LOOP FILTER DESIGN

Low Pass Filter Design for PD_{out}'

The design of low pass filtering for PD_{out}' for the device can be accomplished using the following design information. In addition to the example included here, Motorola Application Note AN1207, also includes examples of active filtering which may be used to supplement this information.



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n\left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

Definitions:
N = Total Division Ratio in Feedback Loop
K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ V/radian for PD_{out}'
K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ V/radian for ϕ_V and ϕ_R

$$K_{VCO}\ (\text{VCO Gain}) = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$, where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Recommended Reading:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.

Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN*. March 5, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

AN1207, The MC145170 in Basic HF and VHF Oscillators, Motorola Semiconductor Products, Inc., 1992.

AN1671, MC145170 PSpice Modeling Kit, Motorola Semiconductor Products, Inc., 1998.

Example:

Given the following information:

VCO frequency = 45.555 MHz,

Frequency step size = 5 kHz,

VCO gain = 3.4 MHz/V.

Design a loop filter with a damping factor of 0.707.

The VCO is assumed to have a linear response throughout the range used in this example. The gain for the VCO has been given as 3.4 MHz/V and is multiplied by 2π rad/s/Hz for calculating loop filter values.

$K_{VCO} = 2\pi$ rad/s/Hz x 3.4 MHz/V = 2.136 x 10^7 rad/s/V .

The gain for the phase detector is defined as

$$K_\phi = \frac{V_{DD}}{4\pi}\ \text{V/rad for } PD_{out}' \ .$$

Using a value for V_{DD} (phase detector supply voltage) of 3.6 V with the output voltage multiplier turned off, the value is

$$K_\phi = \frac{3.6}{4\pi} = 0.2865\ \text{V/rad} \ .$$

Let

$$\omega_n = \frac{2\pi\, f_r}{50} = 628.3\ \text{rad/s}$$

and

$$N = \frac{F_{VCO}}{F_{\text{step size}}} = \frac{45.555\ \text{MHz}}{5\ \text{kHz}} = 9111 \ .$$

Choosing C = 0.05 μF and calculating R1 + R2,

$$R1 + R2 = \frac{K_\phi\, K_{VCO}}{N\, C\, \omega_n^2} = 34\ \text{k}\Omega \ .$$

With a damping factor of 0.707,

$$R2 = \frac{\dfrac{0.707}{0.5\,\omega_n} - \dfrac{N}{K_\phi\, K_{VCO}}}{C} = 15\ \text{k}\Omega \ ,$$

$R1 = (R2 + R1) - R2 = 34\ \text{k} - 15\ \text{k} = 19\ \text{k}\Omega \sim 20\ \text{k}\Omega$.

The choice for C is somewhat arbitrary, however, its value does impact the performance of the loop filter. If possible, a range of choices for C should be used to calculate potential loop filters and the resultant filters simulated, as will be shown below, to determine the best balance.

If additional filtering is desired, R1 may be split into two equal resistors and a capacitor to ground inserted. Since the closest resistance to one–half of 9 k is 4.7 kΩ, this value is chosen for $R1_a$ and $R1_b$. The maximum value for the added capacitance is based on the bandwidth of the original loop filter.

The general form for the transfer function for the passive filter shown in Figure 54, can be shown to have the form:

$$F(s) = K_h \left[\frac{s + \omega_2}{(s + \omega_1)(s + \omega_3)} \right]$$

where

$$\omega_1 = \frac{1}{(R1_a + R1_b + R2)\, C} \quad ,$$

$$\omega_2 = \frac{1}{R2C} \quad ,$$

$$\omega_3 = \frac{1}{\left[\frac{R1_a\, R1_b + R1_a\, R2}{(R1 + R2)} \right] C_c} \quad ,$$

where

$$R1 = R1_a + R1_b$$

and

$$\omega_3 > \omega_2 \quad .$$

Since splitting R1 into two equal values, $R1_a$ and $R1_b$, and inserting the capacitance between the junction of $R1_a$ and $R1_b$ does not change the position of the pole located at ω_1, the value of ω_1 remains

$$\omega_1 = \frac{1}{(R1_a + R1_b + R2)\, C} = \frac{1}{(R1 + R2)\, C} \quad .$$

The 0 identified at $\omega_2 = 1/R2\ C$ is also unaffected by the addition of C_c if $\omega_3 > \omega_2$.

Since

$$R1_a = R1_b = \frac{R1}{2} \quad .$$

the value of C_c can be determined by specifying the value for ω_3 and using the values already determined for R1 and R2. The rule of thumb is to choose ω_3 to be 10 x ω_B so as not to impact the original filter. ω_B can be found as

$$\omega_B = \omega_n \sqrt{[1 + 2\zeta^2 + \sqrt{(2 + 4\zeta^2 + 4\zeta^4)}]}$$

$$\omega_B = 628.3 \text{ rad/s} \sqrt{[1 + 2\,(0.707)^2 + \sqrt{(2 + 4\,(0.707)^2 + 4\,(0.707)^4)}]}$$

$$= 1.293 \times 10^3 \text{ rad/s} \quad .$$

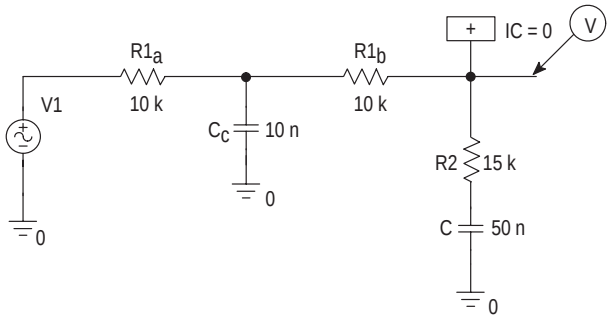
$$10\ \omega_B = 12.93 \times 10^3 \text{ rad/s} \quad .$$

The circuit for the passive loop filter is shown in Figure 54. R1 is split into two equal values and C_c inserted at the junction of $R1_a$ and $R1_b$. Using the values defined above, C_c is determined to be

$$C_c = \frac{1}{\left[\frac{R1_a\, R1_b + R1_a\, R2}{(R1 + R2)\ \omega_3} \right]}$$

$$= \frac{1}{\left[\frac{R1_a\, R1_b + R1_a\, R2}{(R1 + R2)\ 10} \right] \omega_B} = 10.83 \text{ nfd} \sim 10 \text{ nfd} \quad .$$

Figure 54. Passive Loop Filter for PD_{out}'



Open Loop AC Analysis of the Loop Filter

AC analysis is chosen for the mode of simulation for PSpice and VSIN is chosen for V1 and is set to produce a 1 V peak output signal. The simulation is then run and the result shown in Figure 55.

A Bode plot of the loop filter is obtained which describes the open loop characteristics of the loop filter. The corner frequencies of the filter can be modified and the simulation rerun until the desired wave shape is obtained. Since AC analysis runs much faster than transient analysis, the AC open loop analysis of the loop filter is much quicker and requires less resources than the closed loop transient analysis.

Closed Loop Filter Simulations Using PSpice

The top level schematic for simulating a simple loop filter for PD_{out}' operating closed loop, is shown in Figure 56. This filter uses the values calculated above.

The schematic represents the PLL function using the internal phase detector, PD_{out}', the loop filter calculated above, and a VCO. The parameter table allows altering the divider value of N, the maximum current obtained from PD_{out}', and PD_{out} charge pump voltage from the top level schematic.

The schematic for the VCO is shown in Figure 57. Analog behavioral modeling is used rather than discrete transistor modeling to reduce component count and improve simulation efficiency.

The behavioral VCO is composed of an integrator that transforms the input ctrl into the voltage control V(int) and a sine wave generator function whose frequency is controlled by V(int). EVALUE and GVALUE functions are used to perform the transforms. The analog behavioral models, ABM and ABMI, can also be used.

Figure 55. Bode Plot of the Passive Loop Filter

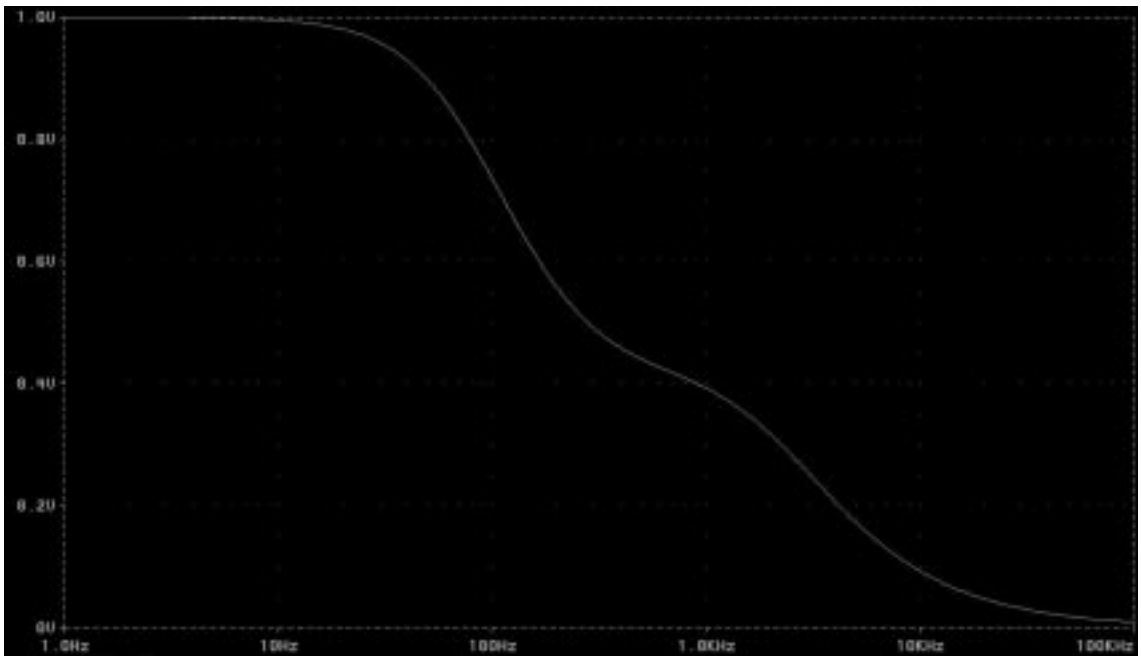


Figure 56. Passive Loop Filter

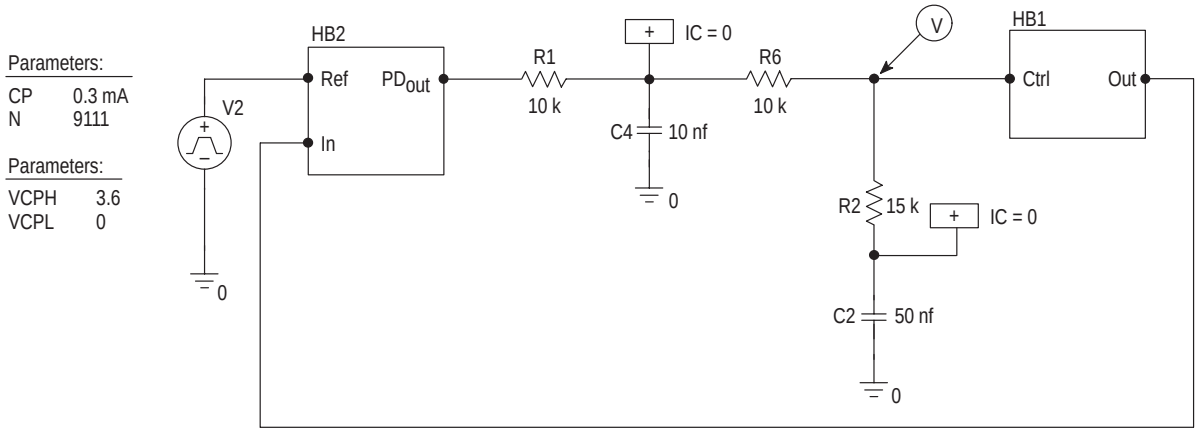
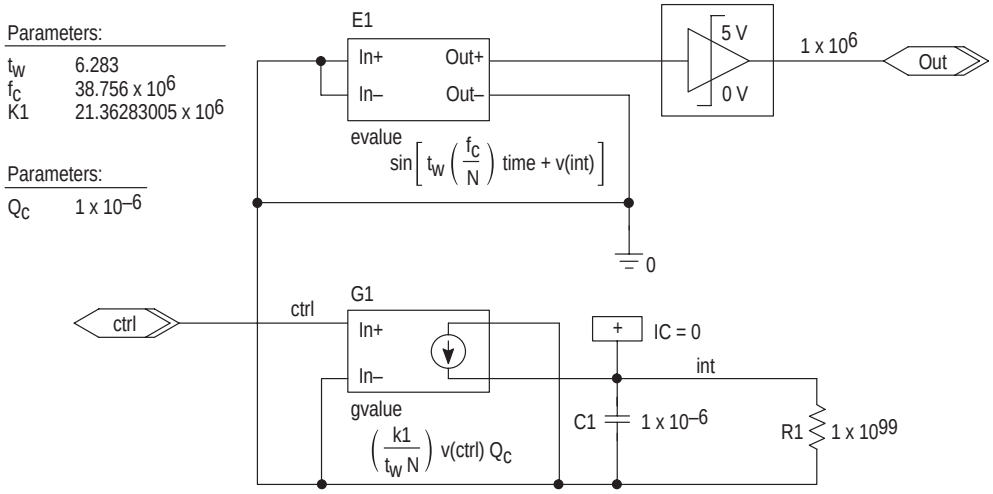


Figure 57. VCO Behavioral Model



G1 performs the operation [k1/(t_W N)] v(ctrl) Q_C. This integrates the input ctrl to produce a voltage ramp used by E1 to produce the desired output. This input is integrated by C1 whose value should equal Q_C for most applications. R1 is required by SPICE to prevent a floating node error.

E1 performs the calculations necessary to generate a sine wave of the desired frequency based on the values listed in the parameter tables and the value of ctrl. The output of E1 is multiplied by 1 x 10^6 and limited to 0 and 5 to obtain a square wave with a fast rise/fall time. Since I/O_STM is a standard model whose values are 0 and 5, these are used here and in the phase detector rather than modifying the component libraries.

The parameter tables provide a convenient method for setting VCO parameters. t_W is 2π, f_C is the zero control voltage VCO frequency, and K1 is the VCO gain in rad/s/V.

The sub–schematic for the phase/frequency detector section of the drawing is shown in Figure 58. This is composed of two blocks, HB3 and HB4. HB3 performs the PD_{out}' function with HB4 performing the actual phase detector operation.

The circuit for the phase/frequency detector is shown in Figure 59. The model is made up of two pulse generators, two RS flip–flops, and appropriate behavioral gates.

HB1 and HB2 are RS flip–flops. These are constructed from behavioral blocks as shown in Figure 60. A behavioral AND gate with a 5 ns delay completes the three state (±2π) phase/frequency detector. The STP function ensures the RS flip–flops are reset at initiation.

To perform the phase detector function, the Ref and f_{in} inputs of the behavioral RS flip–flops are configured to simulate edge triggered operation. This is achieved by placing a 1 ns delay in the Ref and f_{in} signal paths. The input and output of the delay are compared by the input behavioral block and interpreted as a 1 ns pulse. These pulses are used to set HB1 and HB2. If f_{in} leads Ref, the In flip–flop, HB2, will be set first. When Ref leads f_{in}, the Ref flip–flop, HB1, will be set first. The lagging edge drives the second flip–flop output high and the behavioral AND gate then resets both flip–flops. The delay line at the output of the behavioral AND gate prevents PSpice from being confused and also completes the simulation of the phase detector. The outputs of the two RS flip=flops are labeled R_ϕ and V_ϕ. The time between the leading and lagging edges is reflected in the pulse width of the leading edge flip–flop. The lagging edge flip–flop will display a narrow pulse equal in width to the value chosen for the delay at the output of the behavioral AND gate. This should be programmed to the minimum value as specified by the data sheet and is usually 5 ns or less.

Since the outputs R_ϕ and V_ϕ are pure logic signals, additional circuitry is necessary to produce the output PD_{out}'. This output should be high impedance when not driving, and pull either high or low depending on which function (R_ϕ or V_ϕ) is active. The circuitry shown in Figure 61 performs this function.

To eliminate the need for discrete modeling of PD_{out}', analog behavioral modeling is used. Analog behavioral blocks ABMI/2, generate a current source/sink output whenever the appropriate input is high.

A second set of behavioral blocks monitor the output idrive, and switch on the appropriate voltage controlled switch whenever the output rises to the value of V_{DD} (phase detector supply voltage) or drops to 0.

To model PD_{out}', either a model of the transistors used for PD_{out}' must be used or this behavioral arrangement can be used. Since the output is specified by a specific output level and current capability, this arrangement suffices. The output swing becomes VCPH in the schematic and the current capability is CP. If a non–zero value is desired for V_{lo}, the value VCPL is adjusted from the parameter table on the top level schematic.

This arrangement allows setting the output voltage swing of PD_{out}' by specifying VCPH, the current drive of PD_{out}' by specifying the desired value for CP, and leakage values can be simulated by setting the appropriate attributes for S1 and S4 or by adding additional resistance.

Simulation

Figures 62 and 63 are the simulation results of running a transient analysis on the example shown above. The time to lock from power on is simulated by setting the initial condition (IC1) to 0 and running the simulation. Figure 62 is the time versus value of the VCO control voltage. Figure 63 shows the output at the input of the loop filter and can be used to determine lock time.

Figure 58. Phase/Frequency Detector

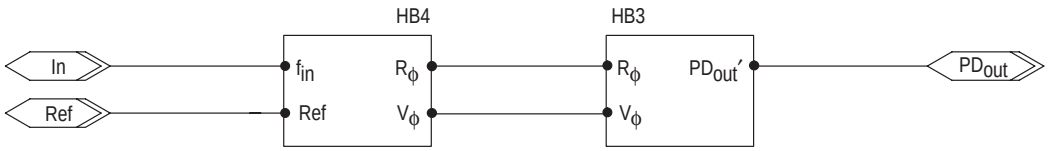


Figure 59. Phase Detector Logic

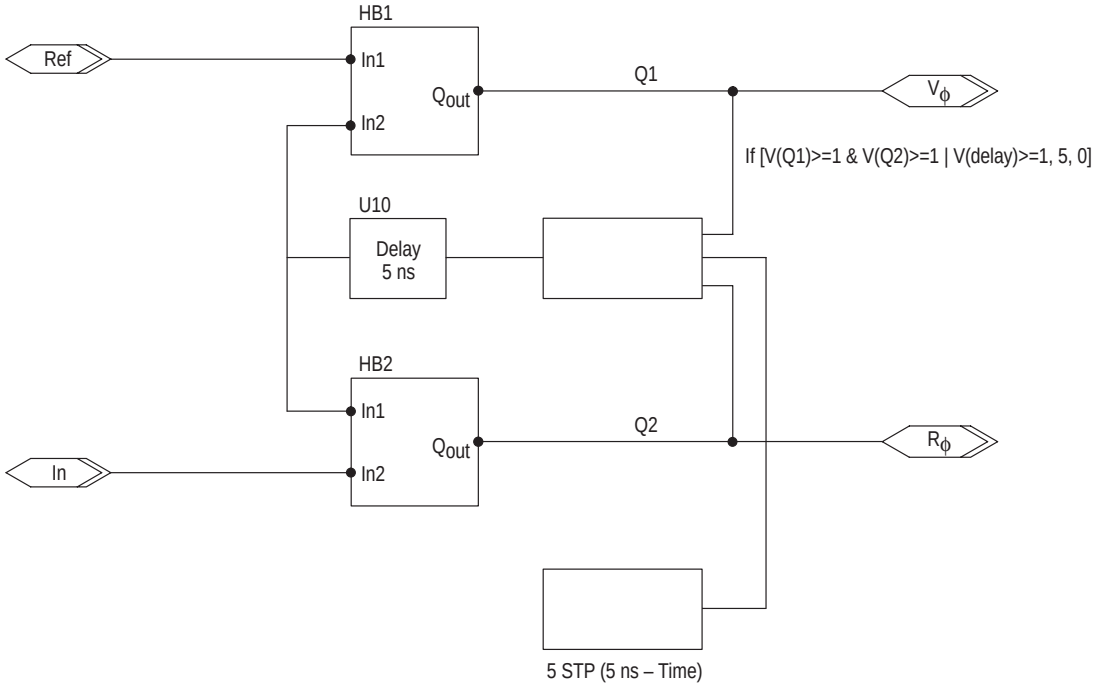


Figure 60. Behavioral RS Flip–flop

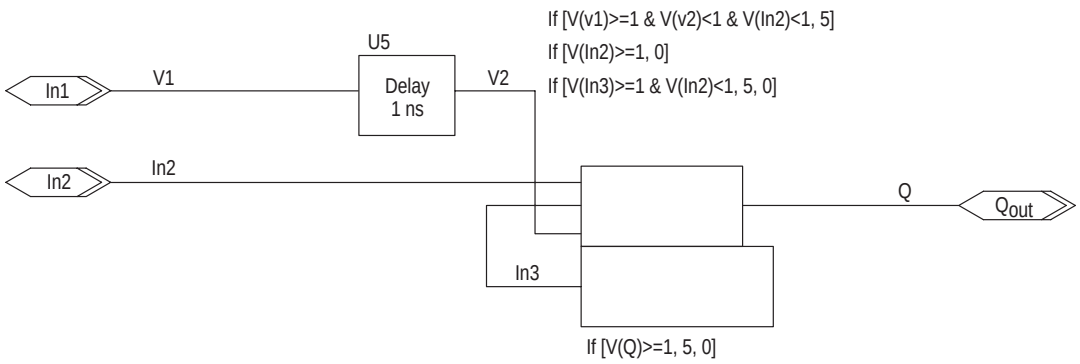


Figure 61. R_ϕ / V_ϕ to PD_{out}' Conversion

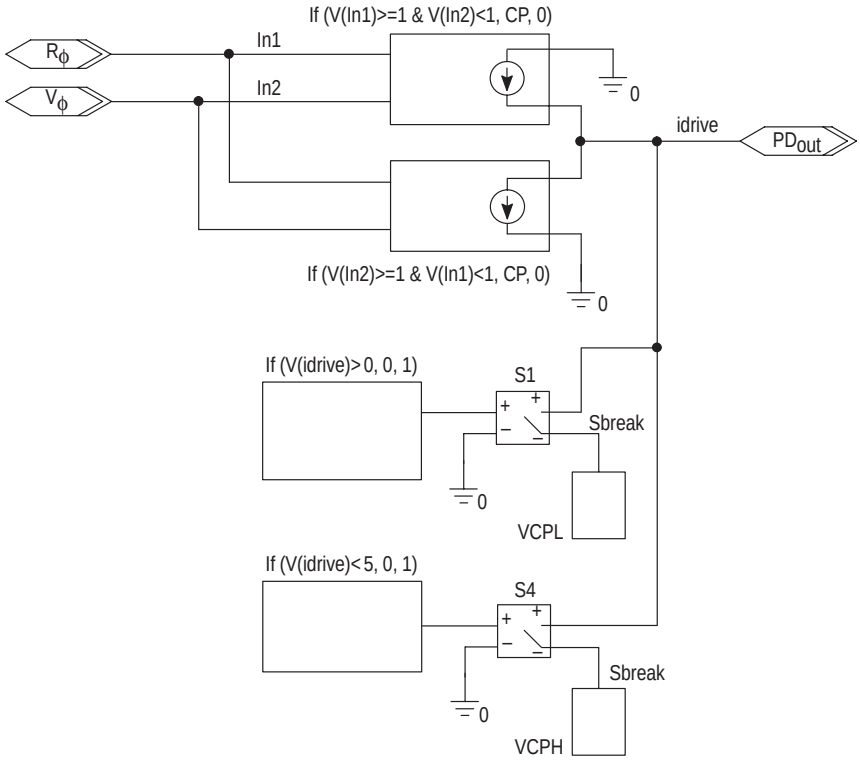


Figure 62. VCO Control Voltage versus Time

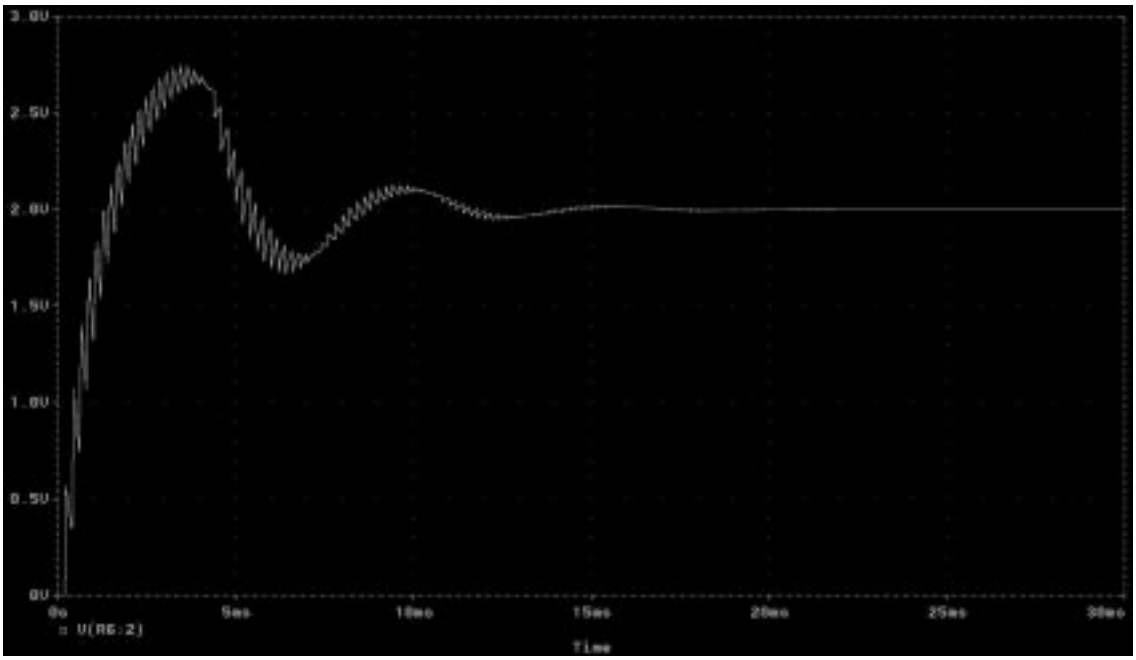
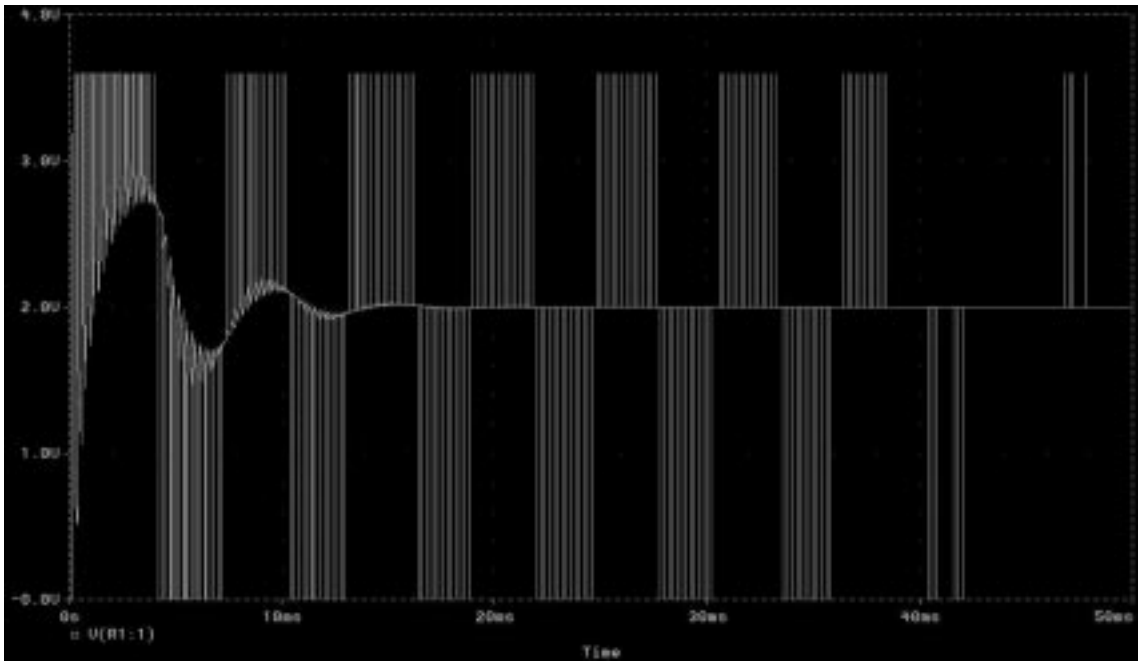


Figure 63. PD_{out}' at Input to Loop Filter



Summary

PSpice provides a method by which the performance of PLL circuitry can be simulated prior to, or in addition to, laboratory testing. The use of behavioral modeling allows the creation of simulation circuits that can provide valuable information for loop filter design and adjustment. By judicious attention to VCO modeling, expected output characteristics can be verified prior to laboratory testing. While simulation does not replace laboratory testing, it can be used to find solutions to “what if” questions without the need for extensive empirical data gathering.

7E. VOLTAGE MULTIPLIER STALL AVOIDANCE

There are three important criteria to note, highlighted in the following sections: **Allowing for Voltage Build, Ensuring Valid Counter Programming,** and **Allowing for Overshoot.** Violation of any of these may cause the voltage multiplier to collapse. Once the voltage collapses, the loop goes out of lock and can not recover until the voltage is allowed to build up again. For an active loop, the voltage multiplier is designed to *maintain* the multiplied voltage on the phase/frequency detector supply pin (C_{mult}). If the main loop is active, the multiplier cannot build the voltage.

Allowing for Voltage Build

After power up, a sufficient time interval must be provided for the on–chip voltage multiplier to build up the voltage on the C_{mult} pin. During this interval, the phase/frequency detector outputs for the main loop (PD_{out}–Hi and PD_{out}–Lo) must be inactive (floating outputs). The POR (power–on reset) circuit forces this "float" condition, thus allowing the voltage to build on the C_{mult} pin.

The duration of the interval to build the voltage is determined by the external capacitor size tied to the C_{mult} pin and the charging current which is 100 μA minimum. The following formula may be used:

$$T = CV/I$$

where

T is the interval in seconds,

C is the C_{mult} capacitor size in farads,

V is the desired voltage on C_{mult} in volts, and

I is the charging current, 1×10^{-4} amps.

The desired voltage on C_{mult} is 4 V for a nominal 2 V supply and 5 V for any supply above 2.6 V.

After this interval, the chip can maintain the voltage on the C_{mult} pin and the phase detectors may be safely placed in the active state.

The interval above also applies when the voltage multiplier is turned off (with power applied) via bits R′19 R′18 R′17 being 000. After the multiplier is turned back on, sufficient time must be allowed for the voltage to build on C_{mult}. In this case, typically an external resistor does not allow the C_{mult} voltage to discharge below approximately V_{pos} (see Section 5E, under **C_{mult}**). Note that if the voltage multiplier is NOT turned off (that is, the above bits are unequal to 000), the keep–alive circuit maintains the multiplied voltage on C_{mult}.

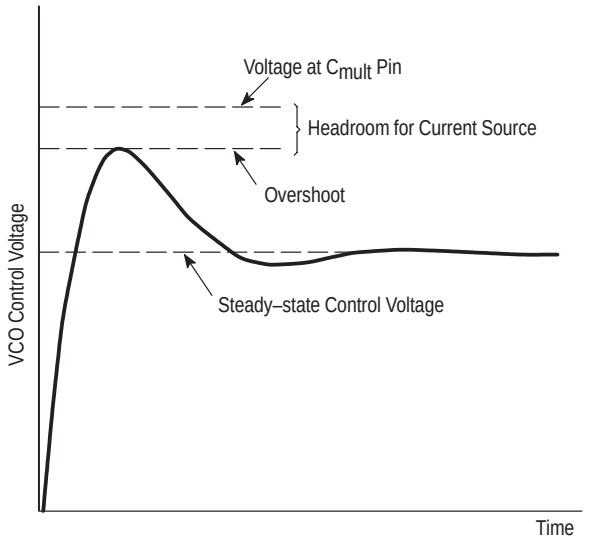
Ensuring Valid Counter Programming

Before the PLLs and/or phase detectors are taken out of standby, legitimate divide ratios (pertinent to the application) must be loaded in the registers. For example, proper divide ratios must be loaded for the R, N, R′, and N′ counters. Also, proper values for all other bits must be loaded. For example: selection of crystal or external reference mode must be made prior to activation of the loops.

After the IC is initialized with the proper bits loaded, the main loop may then be safely activated via the phase detector float bit and/or the PLL standby bit being programmed to 0.

Allowing for Overshoot

The VCO control voltage overshoot for the main loop must not be allowed to exceed the capability of the phase/frequency detectors' maximum output voltage. The detectors' maximum output voltage is determined by the minimum voltage at C_{mult} and the headroom required for the current source. See the following figure.



For example, if the main supply voltage (V_{pos}) is 3 V and the voltage multiplier is utilized, the minimum voltage at C_{mult} is 4.75 V. Then, to allow for current source headroom, the maximum output voltage from the parameter table in Section 3C is approximately C_{mult} – 0.6 V or 4.2 V approximately. Thus, the maximum output overshoot voltage at the phase/frequency detector outputs should be no more than 4.2 V.

Continuing the above example, if the loop is designed with 20% overshoot in the VCO control voltage, then the overshoot must be subtracted off of the 4.2 V shown above. Therefore, the upper end of the control voltage to the VCO must be no more than approximately 3.64 V.

The equations below can be used to determine constraints:

$$\Delta V \leq \frac{V_\phi - 1.2}{2\alpha + 1}$$

$$SSV_{max} = V_\phi - \alpha\,(\Delta V) - 0.6$$

where

ΔV is the VCO control voltage range, the maximum minus the minimum voltage,

V_ϕ is the minimum phase detector supply voltage (at the C_{mult} pin) per the following table,

α is the control voltage overshoot in decimal; for example, 20% overshoot is 0.2, and

SSV_{max} is the maximum allowed steady–state VCO control voltage.

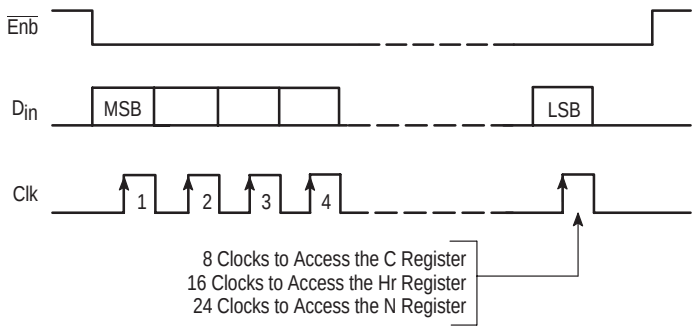
MINIMUM PHASE DETECTOR VOLTAGE FROM VOLTAGE MULTIPLIER

Supply Voltage, V_{pos}	Minimum Phase Detector Voltage, V_ϕ
1.8 V	3.32 V
2.0 V	3.72 V
2.5 V	4.75 V
3.6 V	4.75 V

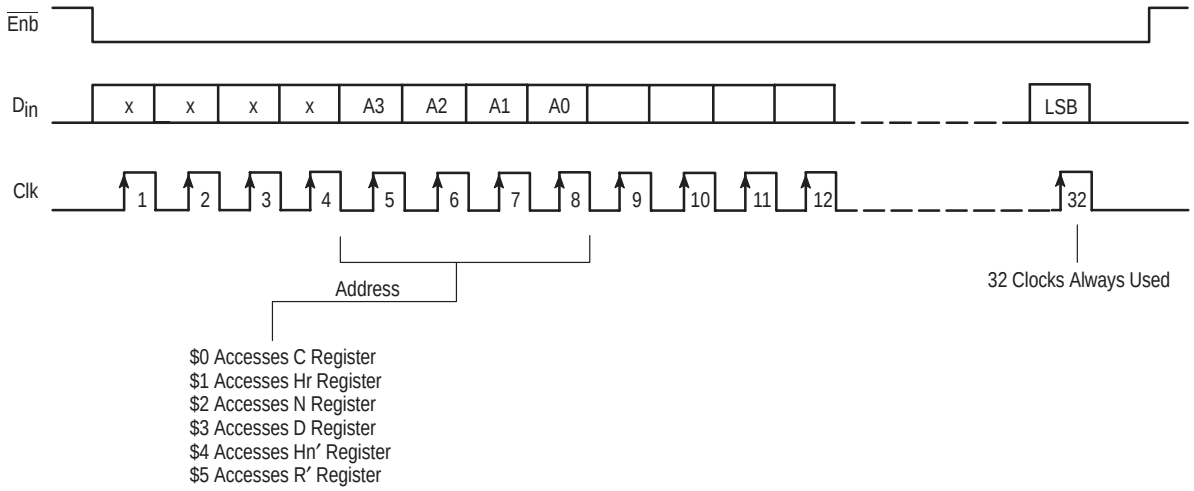
8. PROGRAMMER'S GUIDE

8A. QUICK REFERENCE

BitGrabber ACCESS OF THE REGISTERS



CONVENTIONAL ACCESS OF THE REGISTERS

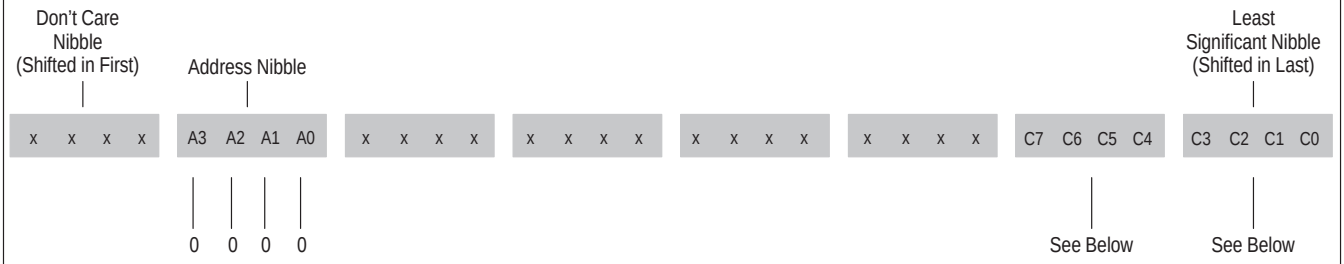


↑ = when the PLL device loads the data bit.

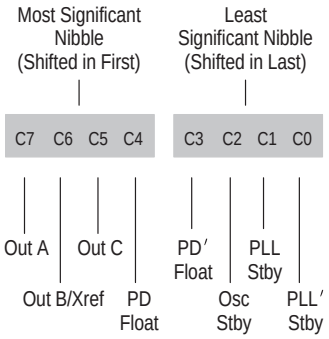
8A. QUICK REFERENCE (continued)

C REGISTER

Conventional Access



BitGrabber Access



Out A = Output A Pin Logic State
0 = Pin is forced to 0 (power up default)
1 = Pin is forced to 1
See Note 1

Out B/XRef = Output B Pin Logic State/
External Reference Selection
See table below

Out C = Output C Pin Logic State
0 = Pin is forced to 0 (power up default)
1 = Pin is forced to high impedance

PD Float = Phase Detector Float
0 = Active, normal operation (power up default)
1 = PD_{out}–Hi/PD_{out}–Lo are forced to high impedance

PD′ Float = Phase Detector′ Float
0 = Active, normal operation (power up default)
1 = PD_{out}′ is forced to high impedance

Osc Stby = Oscillator Standby
0 = Active, normal operation (power up default)
1 = Oscillator/reference circuit in standby
See Note 2

PLL Stby = PLL Standby
0 = Active, normal operation
1 = Main PLL in standby (power up default)
See table below

PLL′ Stby = PLL′ Standby
0 = Active, normal operation
1 = Secondary PLL in standby (power up default)

NOTES: 1. For the Out A bit to control the Output A pin as a port expander, bits R′21 R′20 must be 0 0, which selects Output A as a general–purpose output. If R′21 R′20 are not equal to 0 0, then the Out A bit is a don't care.
2. Whenever Osc Stby = 1, both PLL Stby and PLL′ Stby must be 1, also.

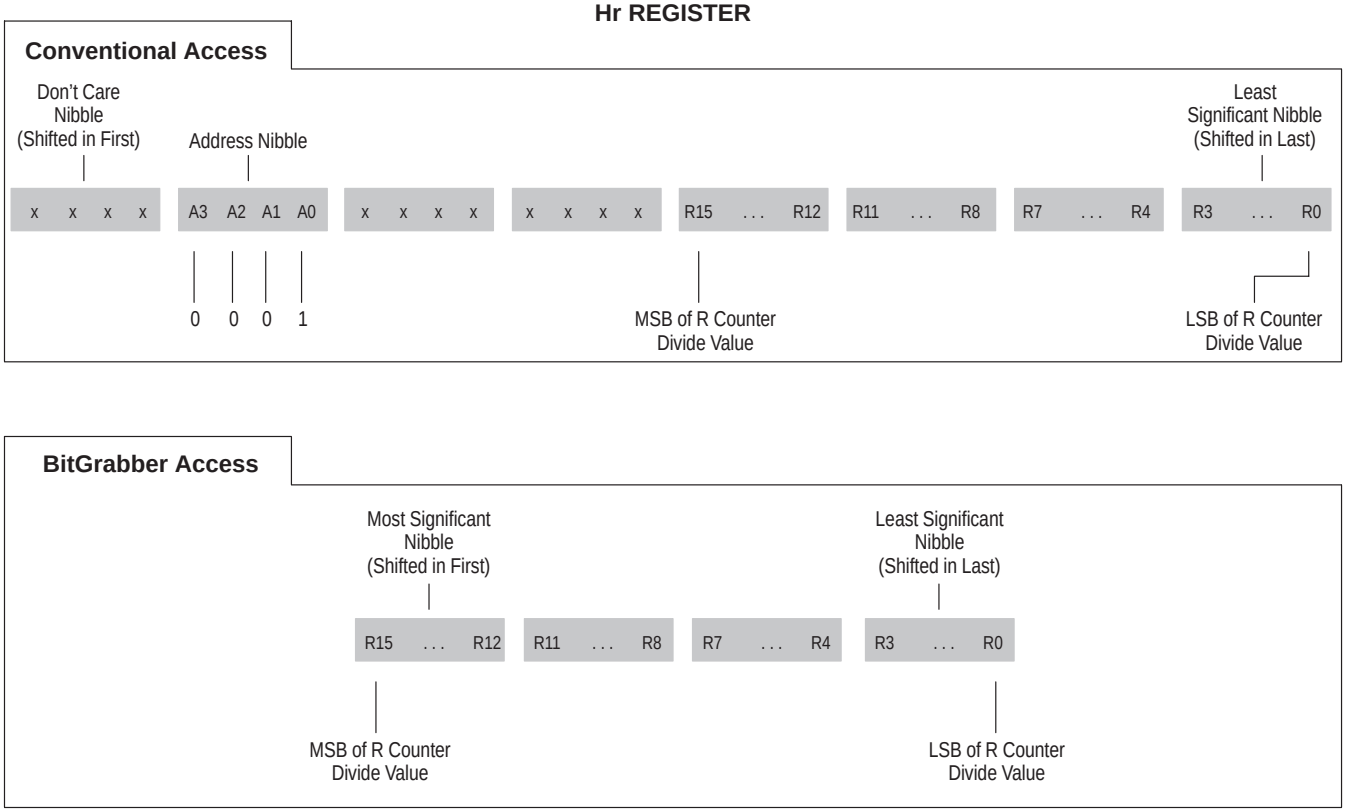
Mode Pin and Bit Summary

Mode Pin	Out B/XRef Bit	PLL Stby Bit	Reference Circuit	Output B Pin	Main PLL
0	0	0	Xtal Osc mode	0	Active
0	0	1	Xtal Osc mode	Z	Standby
0	1	0	Xtal Osc mode	1	Active
0	1	1	Xtal Osc mode	Z	Standby
1	0	0	Xtal Osc mode	0	Active
1	0	1	Xtal Osc mode	Z	Standby
1	1	0	External Reference mode	1	Active
1	1	1	External Reference mode	Z	Standby

NOTES: Xtal osc = crystal oscillator. Z = high impedance.

8A. QUICK REFERENCE (continued)

Hr REGISTER



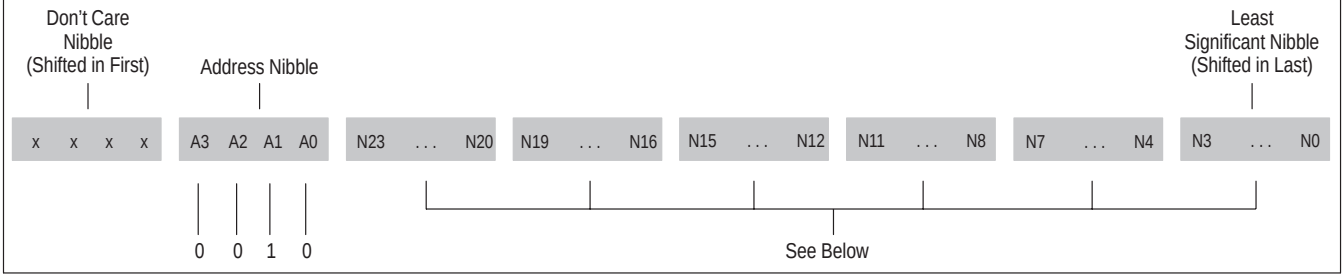
EXAMPLE: To program the R counter to divide by 1000 in decimal, first multiply 1000 by 2 which is 2000. Convert 2000 to hexadecimal: $7D0. Then, add leading 0s to form 2 bytes (4 nibbles): $07D0. Finally, load the Hr register bits R15 to R0 with $07D0. When the N register is subsequently loaded, data passes from the first Hr register (buffer) to the second R register (buffer). (Data is still retained in the Hr register.)
With BitGrabber, no address bits are needed. With a conventional load, address bits A3 to A0 must be included.

NOTE: Hexadecimal numbers are preceded with a dollar sign. For example: hexadecimal 1234 is shown as $1234.

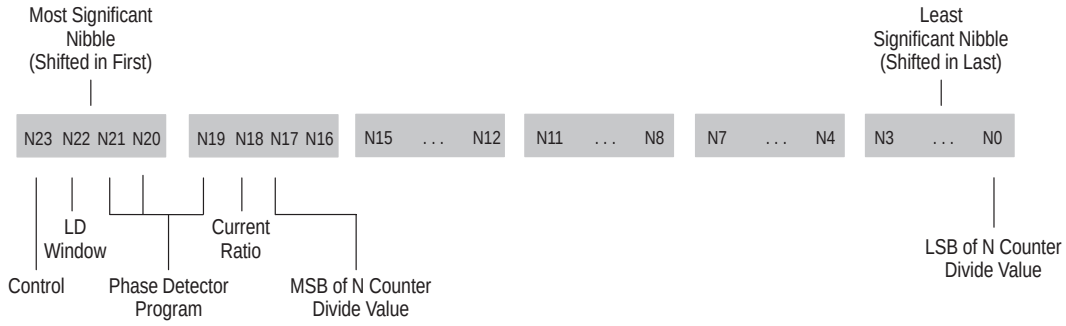
8A. QUICK REFERENCE (continued)

N REGISTER

Conventional Access



BitGrabber Access



Control = Control for Auxiliary Divider
See Table A

LD Window = Lock Detector Window for Main Loop
0 = 32 Osc_e periods
1 = 128 Osc_e periods

Phase Detector Program = Detector Program for Main Loop
See Table B

Current Ratio = PD_{out}–Hi to PD_{out}–Lo Current Ratio
0 = 4:1
1 = 8:1

EXAMPLE: To program the N counter to divide by 1000 in decimal, first convert to hexadecimal: $3E8. Then, add leading 0s to form 2 leading bits plus 2 bytes (2 bits plus 4 nibbles); this is N17 to N0. Bits N23 to N18 should be appropriate to control the above functions. Finally, load the N register. Loading the N register also causes data to pass from the Hr register to the R register and data from the Hn′ register to pass to the N′ register.
With BitGrabber, no address bits are needed. With a conventional load, address bits A3 to A0 must be included.

Table A. Osc_e to f_{out} Frequency Ratio, Mode = Low

N23	R′1	R′0	Osc_e to f_{out} Frequency Ratio
0	0	0	10:1
0	0	1	12.5:1
0	1	0	12.5:1
0	1	1	12.5:1
1	0	0	8:1
1	0	1	10:1
1	1	0	10:1
1	1	1	10:1

NOTE: When the Mode pin is high, the f_{out} pins are configured as polarity inputs and N23 must be programmed to 1.

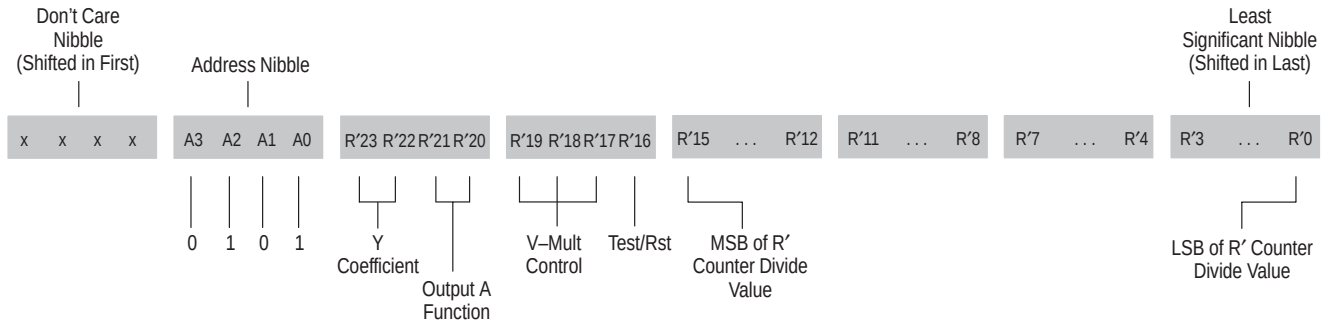
Table B. Main Phase Detector Control

N21	N20	N19	Result
0	0	0	Both PD_{out}–Hi and PD_{out}–Lo floating
0	0	1	PD_{out}–Hi floating, PD_{out}–Lo enabled
0	1	0	PD_{out}–Hi enabled, PD_{out}–Lo floating
0	1	1	Both PD_{out}–Hi and PD_{out}–Lo enabled
1	0	0	PD_{out}–Hi enabled and PD_{out}–Lo floating for 16 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled
1	0	1	PD_{out}–Hi enabled and PD_{out}–Lo floating for 32 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled
1	1	0	PD_{out}–Hi enabled and PD_{out}–Lo floating for 64 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled
1	1	1	PD_{out}–Hi enabled and PD_{out}–Lo floating for 128 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled

8A. QUICK REFERENCE (continued)

R′ REGISTER

Conventional Access only



Y Coefficient
0 0 = only programming values allowed

Output A Function = Controls Output A Mux
0 0 = General–Purpose Output
0 1 = f_R
1 0 = $f_{R'}$
1 1 = Phase Detector pulse

V–Mult Control = Voltage Multiplier Control
0 0 0 = Multiplier OFF, 9 MHz ≤ Osc_e ≤ 80 MHz
0 0 1 = Multiplier ON, 9 MHz ≤ Osc_e ≤ 20 MHz
0 1 0 = Multiplier ON, 20 MHz < Osc_e ≤ 40 MHz
0 1 1 = Multiplier ON, 40 MHz < Osc_e ≤ 80 MHz

Test/Rst = Test/Reset
0 = only programming value allowed

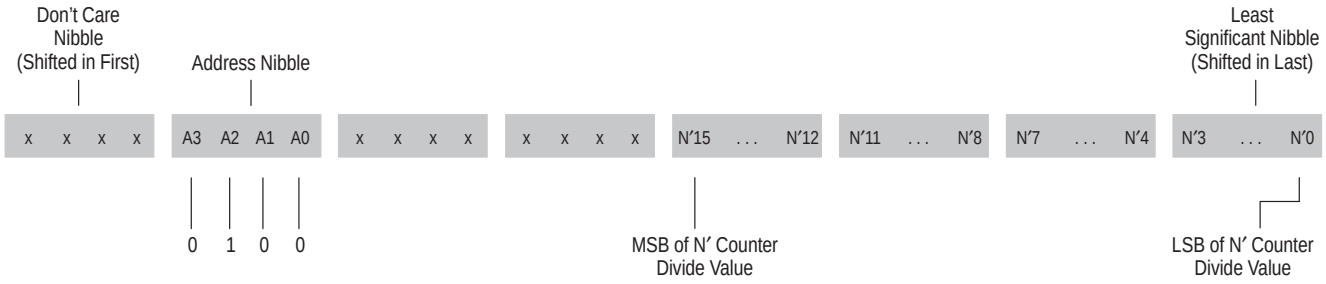
EXAMPLE: When the Mode pin is tied low, see Table 21 for R′ counter programming. When the Mode pin is tied high, to program the R′ counter to divide by 1000 in decimal, first multiply 1000 by 2, which is 2000. Convert 2000 to hexadecimal: $7D0. Then, add leading 0s to form 2 bytes (4 nibbles); this becomes bits R′15 to R′0. Bits R′23 to R′16 should be appropriate to control the above functions. Finally, load the R′ register.
With a conventional load, address bits A3 to A0 must be included.

NOTE: Hexadecimal numbers are preceded with a dollar sign. For example: hexadecimal 1234 is shown as $1234.

8A. QUICK REFERENCE (continued)

Hn′ REGISTER

Conventional Access only

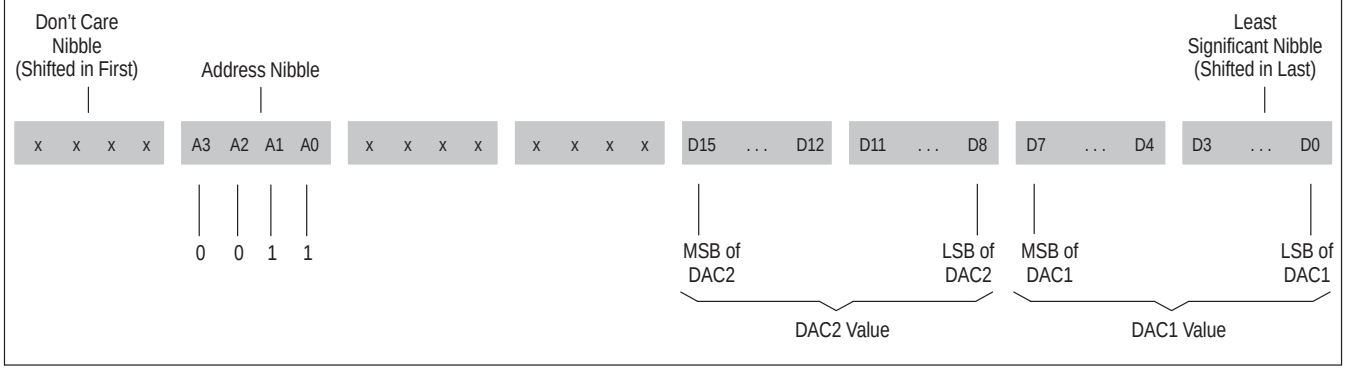


EXAMPLE: To program the N′ counter to divide by 1000 in decimal, first multiply 1000 by 8, which is 8000. Convert 8000 to hexadecimal: $1F40. Then, add leading 0s (if necessary) to form 2 bytes (4 nibbles). Finally, configure address bits A3 to A0 and load the Hn′ register. When the N register is subsequently loaded, data passes from the first Hn′ register (buffer) to the second N′ register (buffer). (Data is still retained in the Hn′ register.)

8A. QUICK REFERENCE (continued)

D REGISTER

Conventional Access only



DAC2 Value = Analog Output Level of DAC2
- $00 = zero output
- $01 = zero + 1 LSB output
- $02 = zero + 2 LSBs output
- $03 = zero + 3 LSBs output
- •
- •
- •
- $FD = full scale – 2 LSBs output
- $FE = full scale – 1 LSB output
- $FF = full scale output

DAC1 Value = Analog Output Level of DAC1
- $00 = zero output
- $01 = zero + 1 LSB output
- $02 = zero + 2 LSBs output
- $03 = zero + 3 LSBs output
- •
- •
- •
- $FD = full scale – 2 LSBs output
- $FE = full scale – 1 LSB output
- $FF = full scale output

8B. INITIALIZING THE DEVICE

Introduction

The registers retain data as long as power is applied to the device. The R and N registers contain counter divide ratios for the main loop, PLL. The R′ and N′ registers contain counter divide ratios for the secondary loop, PLL′. Additional control bits are located in the R′, N, and C registers. The D register controls the DACs. Section 8A is a handy reference for register access and bit definitions.

The C, D, R′, and N registers can be directly written, and have an immediate impact on chip operation. The Hr and Hn′ registers can be directly written, but have no immediate impact on chip operation. This is because the Hr and Hn′ registers are the front–ends of double buffers. The Hr register feeds the R register. The Hn′ register feeds the N′ register. Changing data in the R and/or N′ registers is done with a write to the Hr and/or Hn′ register, respectively, followed by a write to the N register. The transfer of data from the Hr to R and Hn′ to N′ registers is triggered with a write to the N register.

Typically, the Hr and Hn′ registers are written once, during initialization after power up. The Hr and Hn′ registers only need to be accessed if their data is changing.

An Example

Following is an initialization example for a system with a main loop that covers 450 to 500 MHz in 5 kHz steps. An external reference of 19.44 MHz is utilized. The secondary loop is selected to run at 50 MHz. Both VCOs are positive polarity meaning that when the input control voltage increases, the output frequency increases. A divided–down reference is not needed (f_{out} and $\overline{f_{out}}$). Therefore, the Mode pin is tied to V_{pos} and the Pol and Pol′ pins are tied to ground.

The following initialization gives serial data examples for BitGrabber access of the C, Hr, and N registers.

Initialization

Below is the six–step initialization sequence used after power up for the example given above.

Programming the C register first is recommended if the voltage multiplier is utilized. There are three important criteria to note. Violation of any criterion may cause the voltage multiplier to collapse. The first criterion is that after power up, a sufficient time interval must be provided (after the C and R′ registers are initialized) for the on–chip voltage multiplier to build up the voltage on the C_{mult} pin. This interval is determined by the external capacitor size tied to the C_{mult} pin and the charging current which is about 100 μA. After this interval, the chip can maintain the voltage on the C_{mult} pin and the phase/frequency detectors for the main loop may be safely activated. The second criterion is that before the phase/frequency detectors are activated, legitimate divide ratios (pertinent to the application) must be loaded in the registers. The third criterion is a hardware issue. The three criteria are discussed with more detail in Section 7E.

If the voltage multiplier is not used, Step 1 is eliminated and the initialization sequence starts with Step 2.

Step 1: Load the C Register

The C register is programmed such that the main loop's phase/frequency detector outputs are floating (PD Float bit C4 = 1), the reference circuit is active (Osc Stby bit C2 = 0), and an external reference is accommodated (Out B/Xref bit C6 = 1, with the Mode pin high). When the voltage multiplier is enabled by programming the R′ register, the voltage is allowed to build on the C_{mult} pin such that a voltage higher than the main supply voltage is providing power to the phase/frequency detectors. Both loops are active (PLL Stby bits C1 = C0 = 0). Also, for this example, Output A and Output C are programmed low (Out bits C7 = C5 = 0).

In summary, hexadecimal 58 or $58 is serially transferred (BitGrabber access with no address bits).

Step 2: Load the R′ Register

For the secondary loop, the 19.44 MHz reference must be divided down to 80 kHz by the R′ counter; the divide ratio is 243. Per Section 8A, the value is doubled to 486. The 16 LSBs of the R′ register determine the R′ counter divide ratio. Therefore, 486 is converted to $01E6 and becomes the 16 LSBs (R′15 to R′0) in the R′ register. Test/Rst bit R′16 must be a 0. Bits R′19 to R′17 determine the refresh rate of the voltage multiplier. The frequency at Osc_e is <20 MHz. Therefore, per Section 8A, bits R′19 to R′17 must be 001. If Output A is needed as a MCU port expander, bits R′21 = R′20 = 0. Per Section 8A, Y Coefficient bits R′23 = R′22 = 0.

In summary, $050201E6 is serially transferred (conventional access with an address of 0101).

Step 3: Load the Hr Register

For the main loop, the 19.44 MHz reference must be divided down to 5 kHz by the R counter; the divide ratio is 3888. Per Section 8A, the ratio 3888 is doubled to 7776 and then converted to $1E60. The Hr register value is programmed as $1E60. When the Hr register contents are transferred to the R register, the R counter divide ratio is determined.

In summary, $1E60 is serially transferred (BitGrabber access). This value is transferred from the Hr to the R register when the N register is accessed in Step 5.

Step 4: Load the Hn′ Register

For the secondary loop, the phase detector is chosen to run at 80 kHz. Therefore, 80 kHz must be multiplied up to 50 MHz which is a factor of 625. Per Section 8A, the factor is first multiplied by 8 which equals 5000 and then converted to $1388. The Hn′ register is programmed as $1388. When the Hn′ register contents are transferred to the N′ register, the N′ counter divide ratio is determined.

In summary, $04001388 is serially transferred (conventional access with an address of 0100). The value $1388 is transferred to the N′ register when the N register is accessed in Step 5.

Step 5: Load the N Register

For this example, the IC is initialized to tune the lowest end of the main loop. The lowest end of the main loop's frequency range is 450 MHz. Therefore, the 5 kHz must be multiplied up to 450 MHz which is a factor of 90,000 or $15F90 to be loaded into bits N17 to N0 of the N register. Bit N18 is programmed to 0 for a PD_{out}–Hi to PD_{out}–Lo current ratio of 4:1. If PD_{out}–Lo is used for the main loop, bits N21 to N19 must be 001. (PD_{out}–Lo must be used to initialize the device when *adapt* is used, see Section 8D.) Bit N22 = 0 to select a lock detect window of approximately $32 / Osc_e$ = 32/19.44 MHz or 1.6 μs. Bit N23 must be programmed to 1

by the user. (When the Mode pin is high, programming N23 to a 0 is for Motorola use only.)

In summary, $895F90 is serially transferred (BitGrabber access). The N register access also causes double–buffer transfers of Hr to R and Hn′ to N′.

Step 6: Load the C Register

Now that legitimate divide ratios are programmed for the counters, the main loop may be activated. Thus, the PD float bit C4 is now programmed to 0. The standby bits are unchanged: C2 = C1 = C0 = 0. Bit C5 could be used to control Output C to either a low level or high impedance; for a low level, C5 = 0. Whenever an external reference is utilized, bit C6 must be 1. Bit C7 may be used to control Output A to a low or high level because it is selected as “port expander” by bit R′21 and R′20; for a low level, C7 = 0.

In summary, $40 is serially transferred (BitGrabber access). This causes the main loop to tune to 450 MHz, the secondary loop to tune to 50 MHz, and both the Output A and Output C pins to be forced low.

The device is now initialized.

8C. PROGRAMMING WITHOUT ADAPT

Tuning the Top of the Band

After initializing the device via steps 1 through 6 in Section 8B, the only register that needs to be loaded to tune the main loop is the N register.

For this example, tuning the upper end of the band (500 MHz) requires that the 5 kHz at the phase/frequency detector be multiplied up to 500 MHz. This is a loop multiplying factor of 100,000. This value is converted to $186A0 and is loaded for bits N17 to N0. Bits N23 to N18 are not changed and are programmed as indicated in Section 8B, step 5.

In summary, $8986A0 is transferred to tune the main loop. No other registers are loaded.

Tuning Other Channels

Tuning other channels for the main loop, while keeping the secondary loop at a constant frequency, only requires programming the N register. See Table 22 for example frequencies.

Table 22. Main Loop Tuning Examples

Frequency Desired (MHz)	Multiplying Factor (Decimal)	Multiplying Factor (Hexadecimal)	N Register Data (Hexadecimal)
450.000	90,000	$15F90	$895F90
450.005	90,001	$15F91	$895F91
450.010	90,002	$15F92	$895F92
450.015	90,003	$15F93	$895F93
455.000	91,000	$16378	$896378
458.015	91,603	$165D3	$8965D3
471.040	94,208	$17000	$897000
500.000	100,000	$186A0	$8986A0

8D. PROGRAMMING UTILIZING HORSESHOE WITH ADAPT

Introduction

A unique adapt feature can be used with the MC145181 when conventional tuning can not meet the lock–time requirements of a system and the annoying spurs or noise can not be tolerated from a fractional–N scheme. The adapt feature is available on the main loop only.

For adapt, a timer is engaged which causes an internal data update of the R and N registers to be delayed. The IC supports the *Horseshoe* scheme for adapt by allowing a fairly–close quickly–tuned *approximate* frequency to be tuned, followed by the tuning of the *exact* frequency. Two sets of R and N data are sent to the device. The first set {R1, N1} is for tuning the approximate frequency. The second set {R2, N2} is for tuning the exact frequency. Use of the timer delays the transfer of {R2, N2} until a programmed interval has elapsed. In addition, after the interval has elapsed, the main loop control switches from PD_{out}–Hi to PD_{out}–Lo.

Tuning Near the Top of the Band

Continuing the example, after initializing the device via steps 1 through 6 in Section 8B, Horseshoe with adapt can be used to tune the main loop to obtain fast frequency jumps. Use of the BitGrabber access is recommended to minimize the number of serial data clocks required for sending the four “words”.

In this example, the first phase of adapt utilizes approximate tuning with the phase/frequency detector running at 4x the step size. Therefore, the approximate tuning runs the detector at about 20 kHz. The second phase, with exact tuning, runs the detector at 5 kHz. Horseshoe with adapt requires that two data sets be serially sent to the device for every frequency tuned. The first set is for approximate tuning {R1, N1}; the second set is for exact tuning {R2, N2}.

Approximate tuning with Horseshoe is unique. This method involves two key elements: (1) increasing the phase detector frequency and (2) varying *both* the R and N divide values such that the approximate frequency is within a certain predetermined range. The Horseshoe algorithm contained in the development system software also allows placing a constraint on the loop–gain variation that the user can tolerate.

For example, to tune 459.97 MHz, the first {R1, N1} data set could contain divide ratios for the R and N counters of 973.5 and 23,034, respectively. With this data set, the phase detector is running at about 19.97 kHz and the approximate frequency is about 170 Hz from the exact frequency. The second data set contains R and N divide values of 3,888 and 91,994, respectively. This achieves the exact (target) frequency of 459.97 MHz.

The timer must be programmed to determine the interval that the device is in the approximate–tune mode. For this example, assume this is 32 f_R cycles; thus, bits N21 N20 N19 = 1 0 1 in the first data set. Note that this time interval is 32 cycles of f_R, with the phase detector running at about 20 kHz (approximate tune) or about 1.6 ms plus the MCU shift time shown in Figure 64. Included in the first data set are N23 = 1 which is required when the Mode pin is high, N22 = 0

for the lock detect window of 1.6 μs, and N18 = 0 for a current ratio of 4:1 (because the phase detector is running at approximately 4x the step size). Note that bits N23, N22, and N18 are unchanged from the initialization values.

For the second data set, bits N23, N22, and N18 are unchanged. Bits N21, N20, and N19 must be programmed as 001. This enables PD_{out}–Lo for the exact tune after time out.

In summary, two data sets need to be sent to the device: {R1, N1} and {R2, N2}. They are sent in succession as R1, N1, R2, N2; where R1 is the R register value for the first data set, N1 is the N register value for the first set, etc. For the example, these values are {R1, N1} = {$079B, $A859FA} and {R2, N2} = {$1E60, $89675A}. See Figure 64.

Tuning Other Channels

Tuning other channels for the main loop, while keeping the secondary loop at a constant frequency, requires sending two data sets to the part {R1, N1} and {R2, N2}. See Table 23.

8E. CONTROLLING THE DACs

Introduction

The two 8–bit DACs are independent circuit blocks on the chip. They have no interaction with other circuits on the chip. A single 16–bit register, called the D register, holds the binary value which controls both DACs.

Programming the DACs

A DAC programmed for 0 scale is in the low–power mode. The 0 scale is programmed as $00 for each 8–bit DAC.

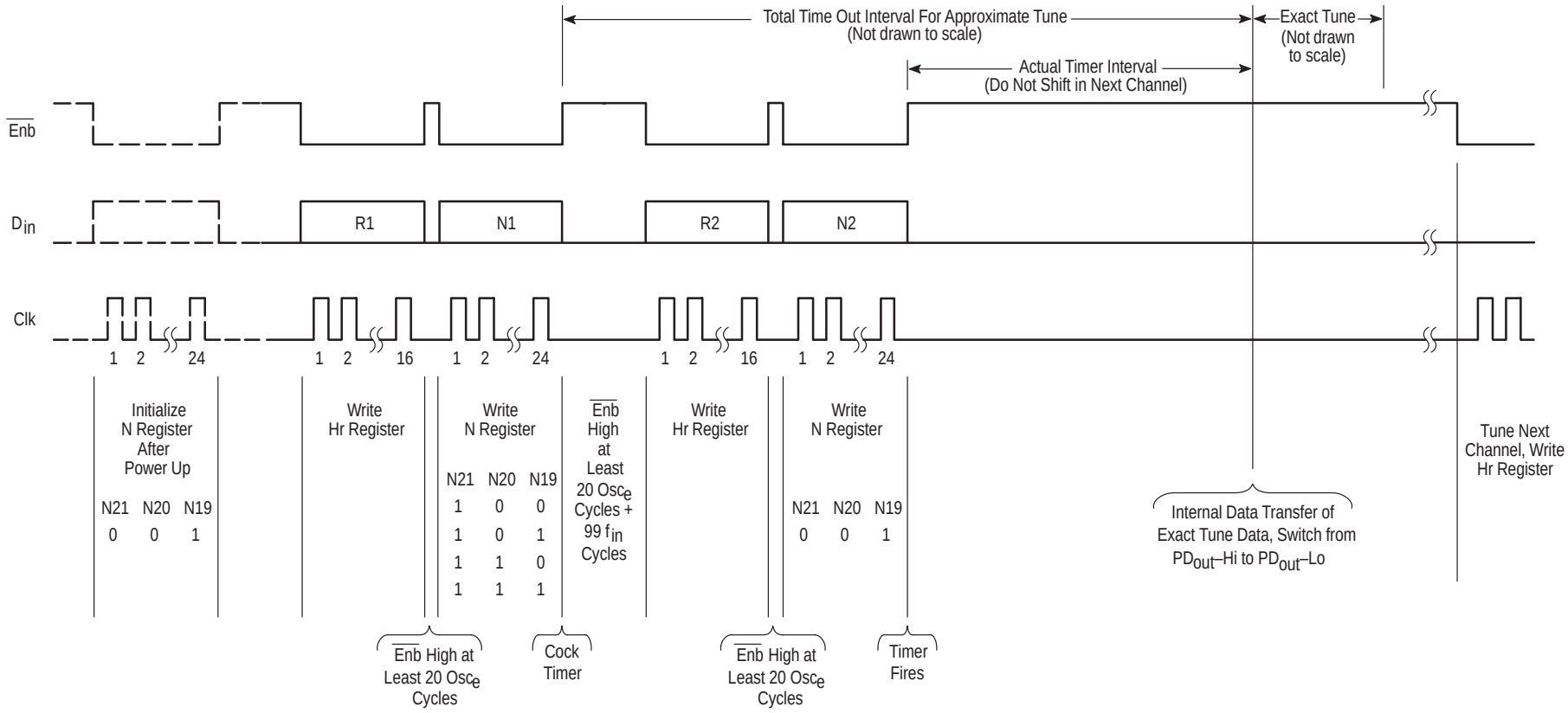
As an example, consider a system that uses just one of the DACs (DAC 1). The other DAC output is unused and is programmed for 0 output. If a condition for a system requires that the DAC have a half–scale output, then DAC 1 is programmed as $80.

In summary, $03000080 is serially transferred (conventional access with an address of 0011).

Table 23. Main Loop Tuning Using Horseshoe With Adapt

Desired Target Frequency (MHz)	Approximate Tuning			Exact Tuning	
	R1	N1	Frequency Error (Hz)	R2	N2
450.000	$0798	$A857E4	0	$1E60	$895F90
450.005	$079B	$A85807	548	$1E60	$895F91
450.020	$0798	$A857E5	0	$1E60	$895F94
450.255	$0795	$A857CE	162	$1E60	$895FC3
459.970	$079B	$A859FA	170	$1E60	$89675A
500.000	$0798	$A861A8	0	$1E60	$8986A0

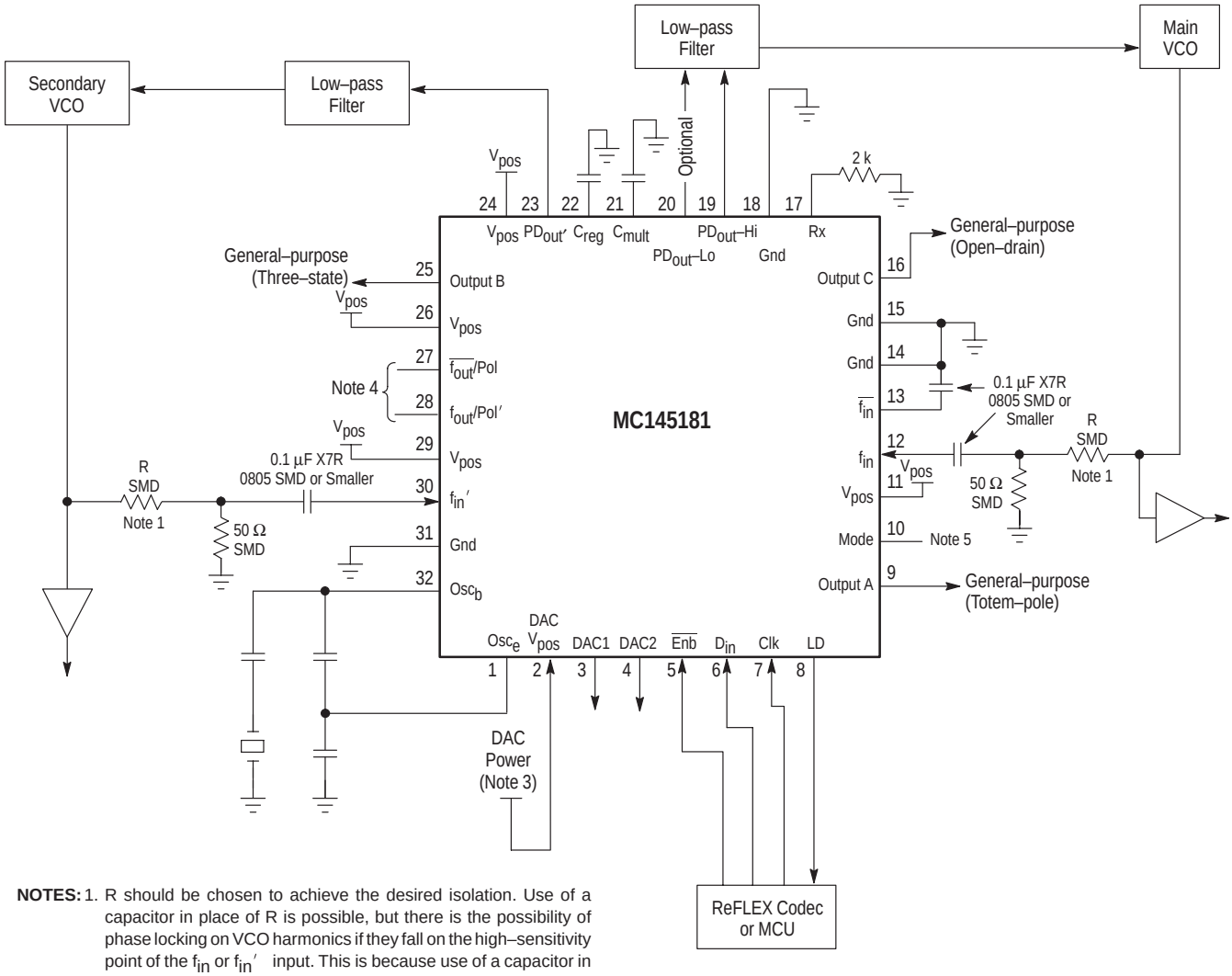
Figure 64. Serial Data Format for Horseshoe with Adapt



NOTE: The interval for shifting in Exact Tune {R2, N2} data adds to the actual Approximate Tuning time. However, this is usually insignificant. For example, at a data rate of 2 Mbps (2 megabits per second), approximately 20 μs is added to the Approximate Tuning time.

9. APPLICATION CIRCUIT

Figure 65. Application Circuit

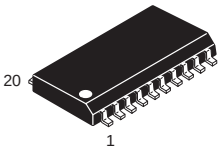


NOTES: 1. R should be chosen to achieve the desired isolation. Use of a capacitor in place of R is possible, but there is the possibility of phase locking on VCO harmonics if they fall on the high–sensitivity point of the f_{in} or f_{in}' input. This is because use of a capacitor in place of R forms a high–pass filter.
2. V_{pos} may range from 1.8 to 3.6 V.
3. DAC power may be any potential between 1.8 V and 3.6 V.
4. Configurable pins. See Pin Descriptions.
5. Tie mode to Gnd or V_{pos}.

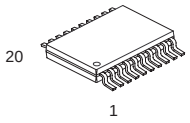
1.1 GHz PLL Frequency Synthesizer

Includes On–Board 64/65 Prescaler

MC145191



F SUFFIX
SOG PACKAGE
CASE 751J



DT SUFFIX
TSSOP
CASE 948D

ORDERING INFORMATION

MC145191F	SOG Package
MC145191DT	TSSOP

The MC145191 is a single–package synthesizer with serial interface capable of direct usage up to 1.1 GHz. A special architecture makes this PLL very easy to program because a byte–oriented format is utilized. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 3–byte serial transfer to the 24–bit A register. The interface is both SPI and MICROWIRE™ compatible.

The device features a single–ended current source/sink phase detector output and a double–ended phase detector output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single–ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

The MC145191 has phase/frequency detectors optimized for single–supply systems of 5 V ±10%.

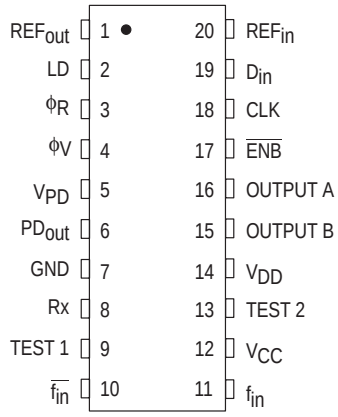
The part includes a differential RF input which may be operated in a single–ended mode. Also featured are on–board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on–board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double–buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

- Maximum Operating Frequency: 1100 MHz @ V_{in} = 200 mV p–p
- Operating Supply Current: 7 mA Nominal
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 4.5 to 5.5 V
- Operating Supply Voltage Range of Phase Detectors (V_{PD} Pin): 4.5 to 5.5 V
- Current Source/Sink Phase Detector OUTPUT Capability: 2 mA Maximum
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: – 40 to + 85°C
- R Counter Division Range: (1 and) 5 to 8191
- Dual–Modulus Capability Provides Total Division up to 262,143
- High–Speed Serial Interface: 4 Mbps
- OUTPUT A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General–Purpose Digital Outputs — OUTPUT A: Totem–Pole (Push–Pull)
  OUTPUT B: Open–Drain
- Patented Power–Saving Standby Feature with Orderly Recovery for Minimizing Lock Times, Standby Current: 30 μA
- Evaluation Kit Available (Part Number MC145191EVK)
- See Application Note AN1253/D for Low–Pass Filter Design, and AN1277/D for Offset Reference PLLs for Fine Resolution or Fast Hopping

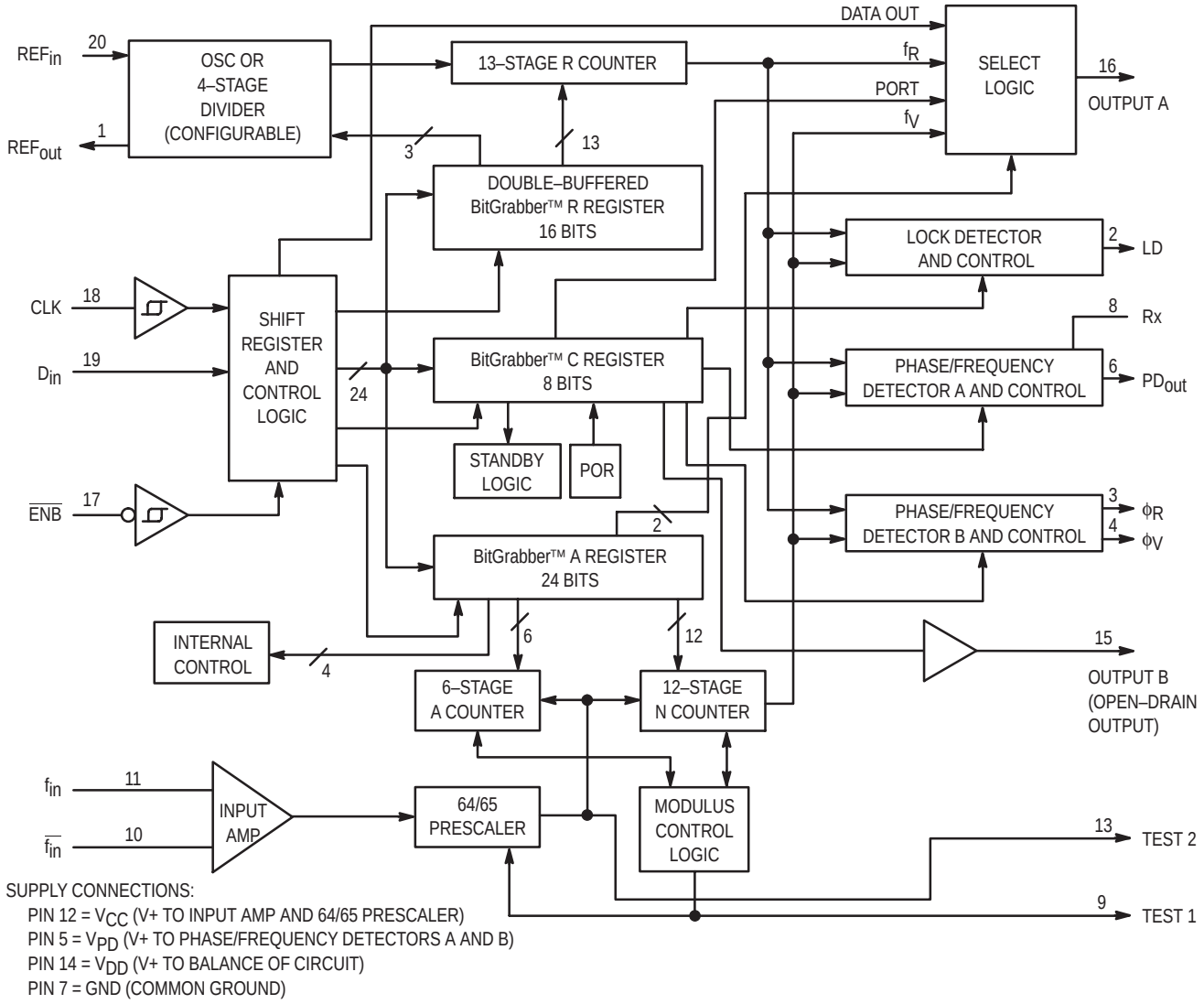
PIN ASSIGNMENT



NOT RECOMMENDED FOR NEW DESIGN
DEVICES TO BE PHASED OUT.
Consider MC145193 for New Designs.

REV 1
12/99

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)	– 0.5 to + 6.0	V
V_{PD}	DC Supply Voltage (Pin 5)	V_{DD} – 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage (except OUTPUT B, PD_{out}, ϕ_R, ϕ_V)	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage (OUTPUT B, PD_{out}, ϕ_R, ϕ_V)	– 0.5 to V_{PD} + 0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = 4.5 to 5.5 V, Voltages Referenced to GND, T_A = –40 to +85°C, unless otherwise stated; V_{PD} = 4.5 to 5.5 V with $V_{DD} \le V_{PD}$.)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, dc Coupled	$0.3 \times V_{DD}$	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, dc Coupled	$0.7 \times V_{DD}$	V
V_{hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		300	mV
V_{OL}	Maximum Low–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = 20 μA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = –20 μA, Device in Reference Mode	V_{DD} – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = 0.4 V	0.36	mA
I_{OH}	Minimum High–Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = V_{DD} – 0.4 V for REF_{out}, LD V_{out} = V_{PD} – 0.4 V for ϕ_R, ϕ_V	– 0.36	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT A, OUTPUT B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High–Level Output Current (OUTPUT A, Only)	V_{out} = V_{DD} – 0.4 V	– 0.6	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	V_{in} = V_{DD} or GND, Device in XTAL Mode	± 1.0	μA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V_{DD} or GND, Device in Reference Mode	± 150	μA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{out} = V_{PD} – 0.5 V or 0.5 V, Output in High–Impedance State	± 200	nA
I_{OZ}	Maximum Output Leakage Current (OUTPUT B)	V_{out} = V_{PD} or GND, Output in High–Impedance State	± 10	μA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	V_{in} = V_{DD} or GND; Outputs Open; Device in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode; OUTPUT B Controlling V_{CC} per Figure 22	30	μA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static Low or High, Bit C4 = Low Which is ***not*** Standby, I_{Rx} = 113 μA	600	μA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is ***not*** Standby	30	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 1.1 GHz; REF_{in} = 13 MHz @ 1 V p–p; OUTPUT A = Inactive and No Connect; $REF_{out} \div 8$; ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, $\overline{ENB}$, CLK = V_{DD} or GND, Phase Detector B Selected (Bit C6 = Low)	*	mA

* The nominal value = 7 mA. This is not a guaranteed limit.

ANALOG CHARACTERISTICS—CURRENT SOURCE/SINK OUTPUT—PD_{out}

($I_{out} \leq 2$ mA, $V_{DD} = V_{CC} = 4.5$ to 5.5 V, $V_{DD} \leq V_{PD}$. Voltages Referenced to GND)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation (Part–to–Part)	$V_{out} = 0.5 \times V_{PD}$	4.5	± 20	%
		5.5	± 20	
Maximum Sink–vs–Source Mismatch (Note 3)	$V_{out} = 0.5 \times V_{PD}$	4.5	12	%
		5.5	12	
Output Voltage Range (Note 3)	I_{out} Variation ≤ 20%	4.5	0.5 to 4.0	V
		5.5	0.5 to 5.0	

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value) / Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within – 40° to + 85°C.

AC INTERFACE CHARACTERISTICS ($V_{DD} = 4.5$ to 5.5 V, $T_A = -40$ to + 85°C, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns; $V_{PD} = 4.5$ to 5.5 V with $V_{DD} \leq V_{PD}$)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w below)	1	dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to OUTPUT A (Selected as Data Out)	1, 5	105	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT A (Selected as Port)	2, 5	100	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT B	2, 6	120	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, OUTPUT A and OUTPUT B; t_{THL} ONLY, on OUTPUT B	1, 5, 6	100	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK		10	pF

TIMING REQUIREMENTS

($V_{DD} = V_{CC} = 4.5$ to 5.5 V, $T_A = -40$ to + 85°C, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	20	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{ENB}$ vs CLK	4	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$	4	*	cycles
t_w	Minimum Pulse Width, CLK	1	125	ns
t_r, t_f	Maximum Input Rise and Fall Times – CLK	1	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

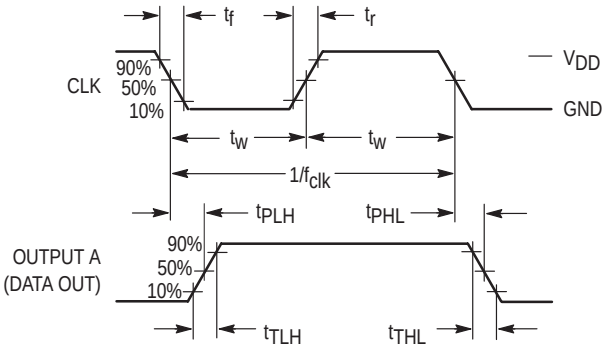


Figure 1.

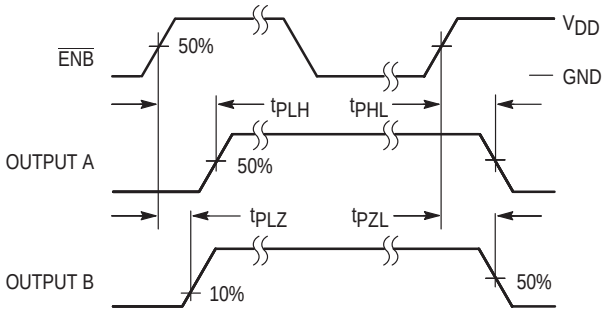


Figure 2.

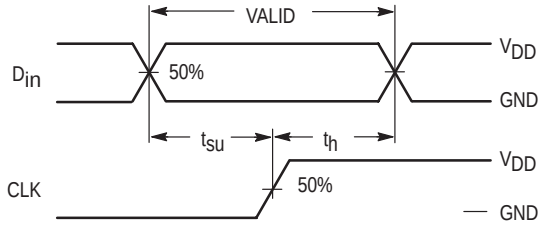


Figure 3.

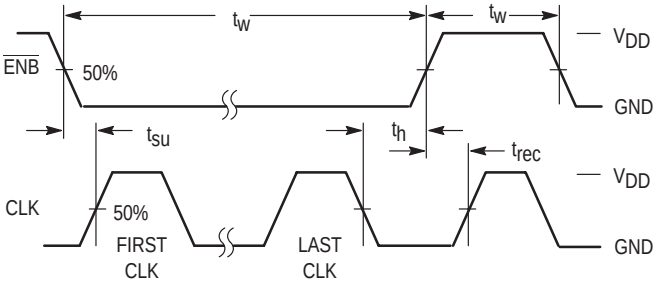
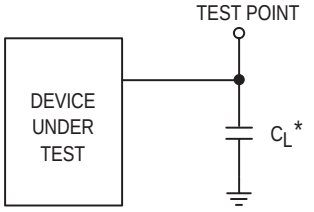
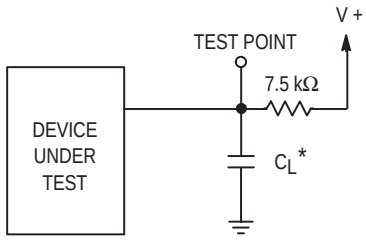


Figure 4.



*Includes all probe and fixture capacitance.

Figure 5. Test Circuit



*Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 4.5 to 5.5 V unless otherwise indicated, T_A = – 40 to + 85°C)

Symbol	Parameter	Test Condition	Figure No.	Guaranteed Operating Range		Unit
				Min	Max	
V_{in}	Input Voltage Range, f_{in}	100 MHz ≤ f_{in} < 250 MHz 250 MHz ≤ f_{in} ≤ 1100 MHz	7	400 200	1500 1500	mV p–p
f_{ref}	Input Frequency Range, REF_{in} Externally Driven in Reference Mode	V_{in} ≥ 400 mV p–p V_{in} ≥ 1 V p–p	8	12 4.5*	27 27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance	9	2	15	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 30 pF	10, 12	dc	10	MHz
f	Operating Frequency of the Phase Detectors			dc	2	MHz
t_w	Output Pulse Width, ϕ_R, ϕ_V, LD	f_R in Phase with f_V, C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	17	85	ns
t_{TLH}, t_{THL}	Output Transition Times, LD, ϕ_V, ϕ_R	C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	—	65	ns
C_{in}	Input Capacitance, REF_{in}			—	5	pF

*If lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal.

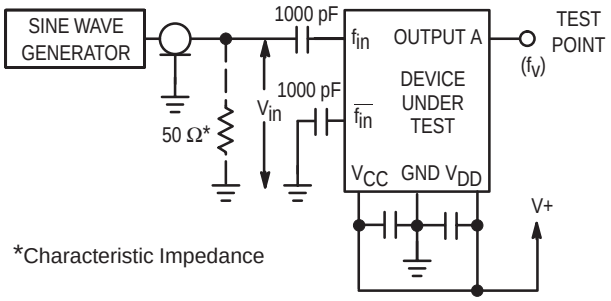


Figure 7. Test Circuit

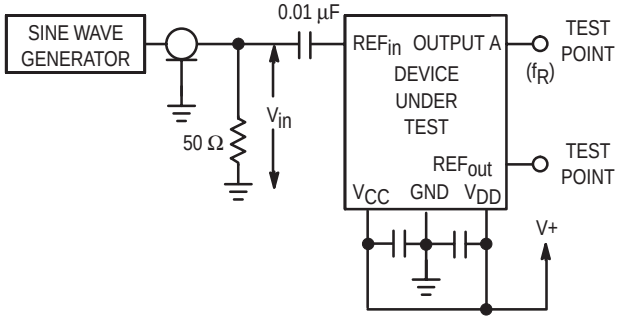


Figure 8. Test Circuit — Reference Mode

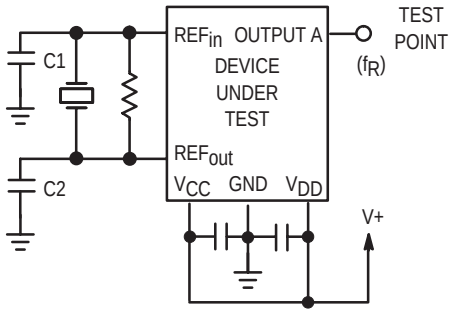


Figure 9. Test Circuit — Crystal Mode

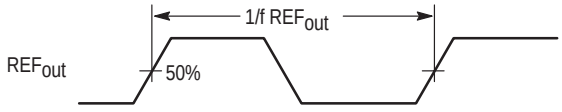


Figure 10. Switching Waveform

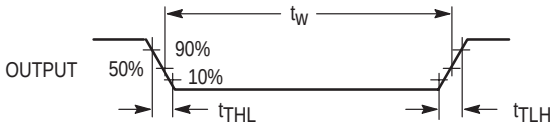


Figure 11. Switching Waveform

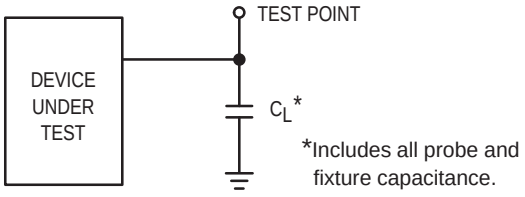
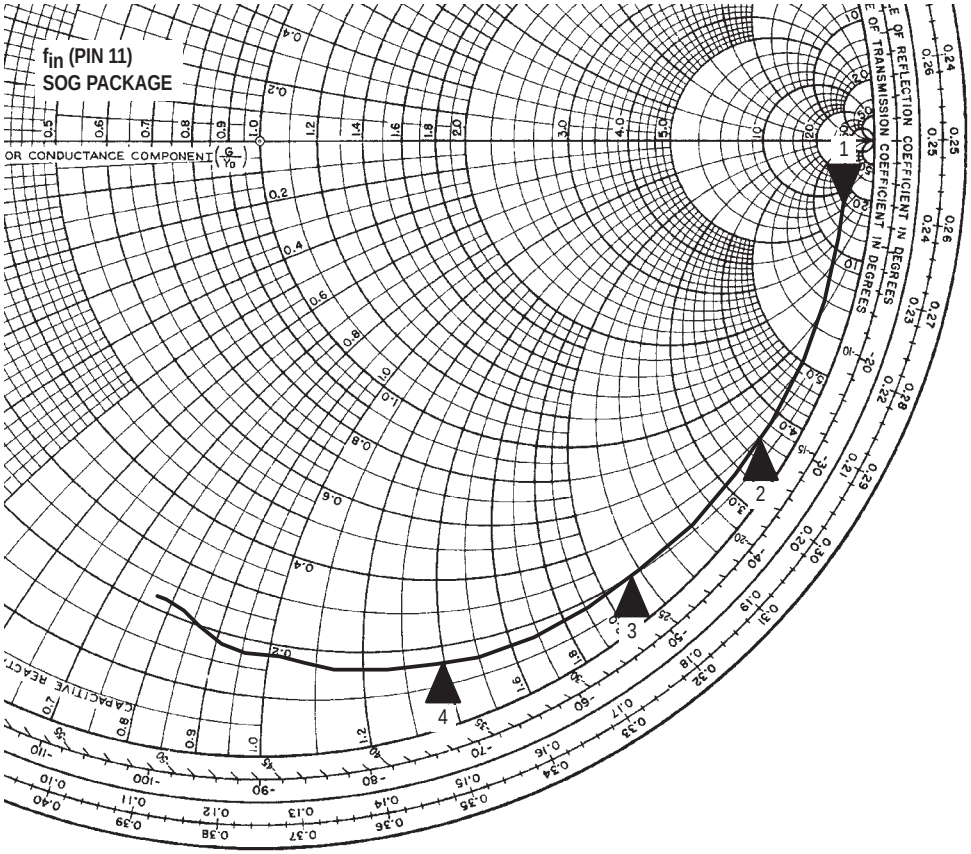


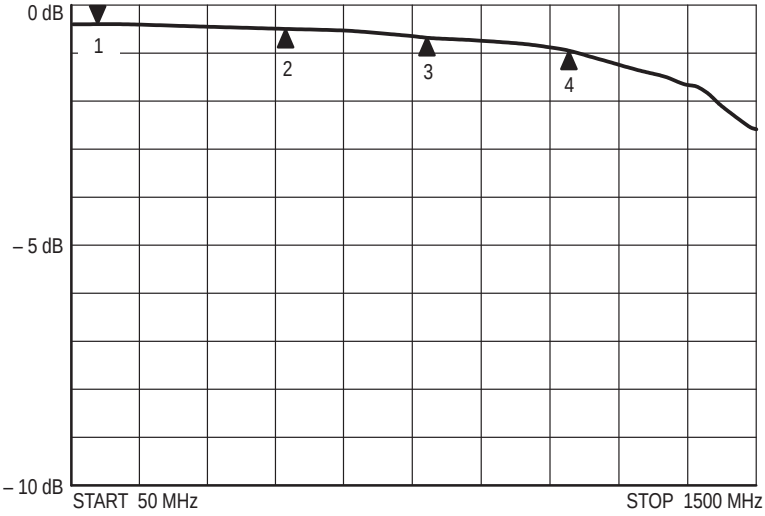
Figure 12. Test Circuit

NORMALIZED INPUT IMPEDANCE AT f_{in} — SERIES FORMAT (R + jX)
(100 MHz to 1.1 GHz)

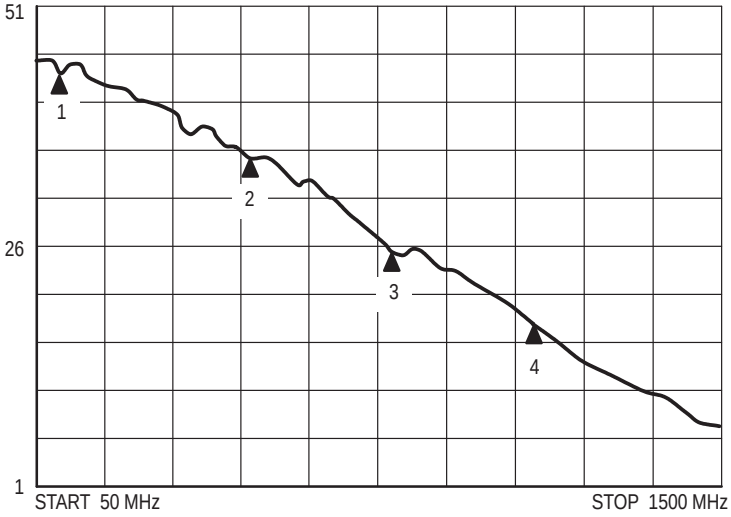


Marker	Frequency (MHz)	Resistance (Ω)	Capacitive Reactance (Ω)	Capacitance (pF)
1	100	338	– 785	2.03
2	500	20.2	– 183	1.74
3	800	11.5	– 109	1.83
4	1100	8.2	– 70.2	2.06

RETURN LOSS AT f_{in}



STANDING WAVE RATIO AT f_{in}



Marker	Frequency (MHz)	SWR	Return Loss (dB)
1	100	43.7	0.40
2	500	34.7	0.48
3	800	25.3	0.68
4	1100	17.9	0.98

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 19)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 1). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

CAUTION

The value programmed for the N–counter must be greater than or equal to the value of the A–counter.

The 13 least significant bits (LSBs) of the R register are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24–bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16–bit transfer may be followed by pulsing $\overline{ENB}$ low with no signal on the CLK pin. This is an alternate method of transferring data to the second buffer of the R register (see Figure 17).

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 4.5 to 5.5 V. The formats are shown in Figures 15, 16, and 17.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	See Figure 13	
Values > 32	See Figures 22 – 25	

CLK
Serial Data Clock Input (Pin 18)

Low–to–high transitions on CLK shift bits available at the D_{in} pin, while high–to–low transitions shift bits from OUTPUT A (when configured as Data Out, see Pin 16). The 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A register. See Table 1 and Figures 15, 16, and 17. The number of clocks required for cascaded devices is shown in Figures 24 through 26.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at GND (with $\overline{ENB}$ being a don't care) or $\overline{ENB}$ must be held at the potential of the V+ pin (with CLK being a don't care) during power–up. As an alternative, the bit sequence of Figure 13 may be used.

$\overline{ENB}$
Active Low Enable Input (Pin 17)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs whenever $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

For POR information, see the note for the **CLK pin**.

OUTPUT A
Configurable Digital Output (Pin 16)

OUTPUT A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 16.

If A23 = A22 = high, OUTPUT A is configured as f_R. This signal is the buffered output of the 13–stage R counter. The f_R signal appears as normally low and pulses high, and can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0–R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of 1 (see Figure 17). The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R should not exceed 2 MHz.

If A23 = high and A22 = low, OUTPUT A is configured as f_V. This signal is the buffered output of the 12–stage N counter. The f_V signal appears as normally low and pulses high, and can be used to verify the operation of the prescaler,

A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is $N \times 64 + A$. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 16. The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V should not exceed 2 MHz.

If A23 = low and A22 = high, OUTPUT A is configured as Data Out. This signal is the serial output of the 24–1/2–stage shift register. The bit stream is shifted out on the high–to–low transition of the CLK input. Upon power up, OUTPUT A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, OUTPUT A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

OUTPUT B
Open–Drain Digital Output (Pin 15)

This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, OUTPUT B assumes the high–impedance state. OUTPUT B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. **Note**: the maximum voltage allowed on the V_{PD} pin is 5.5 V for the MC145191.

Upon power–up, power–on reset circuitry forces OUTPUT B to a low level.

REFERENCE PINS

REF_{in} and REF_{out}
Reference Input and Reference Output (Pins 20 and 1)

Configurable pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 17.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The device is designed to operate with crystals up to 15 MHz; the required connections are shown in Figure 9. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary, respectively). This is the active–crystal mode shown in Figure 17. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode (shown in Figure 17) and can be engaged whether in standby or not.

In the reference mode, REF_{in} (Pin 20) accepts a signal up to 27 MHz from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 17 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 10 MHz. Therefore, for REF_{in} frequencies above 10 MHz, the one–to–one ratio may not be used. Likewise, for REF_{in} frequencies above 20 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in} and $\overline{f_{in}}$
Frequency Inputs (Pins 11 and 10)

These pins are frequency inputs from the VCO. These pins feed the on–board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they usually are used in a single–ended configuration (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 6)

This is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function (no dead zone). The operation of the phase/frequency detector is described below and is shown in Figure 18.

POL bit (C7) in the C register = low (see Figure 15)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the floating state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the

floating state when the device is put into standby (STBY bit C4 = high).

The PD_{out} circuit is powered by V_{PD}. The phase detector gain is controllable by bits C3, C2, and C1: gain (in amps per radian) = PD_{out} current divided by 2π.

ϕ_R and ϕ_V (Pins 3 and 4)
Double–Ended Phase/Frequency Detector Outputs

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 18.

POL bit (C7) in the C register = low (see Figure 15)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD
Lock Detector Output (Pin 2)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V (see Figure 18).

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx
External Resistor (Pin 8)

A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Tables 2 and 3 for other values of current. To achieve a maximum current of 2 mA, the resistor should be about 18 kΩ when V_{PD} is 5.0 V. See Figure 14 if lower maximum current values are desired.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

TEST POINT PINS

TEST 1
Modulus Control Signal (Pin 9)

This pin may be used in conjunction with the Test 2 pin for access to the on–board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace.

TEST 2
Prescaler Output (Pin 13)

This pin may be used to access to the on–board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply (Pin 14)

This pin supplies power to the main CMOS digital portion of the device. The voltage range is + 4.5 to + 5.5 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC}
Positive Power Supply (Pin 12)

This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is + 4.5 to + 5.5 V with respect to the GND pin. In the standby mode, the VCC pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 22.

For optimum performance, VCC should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

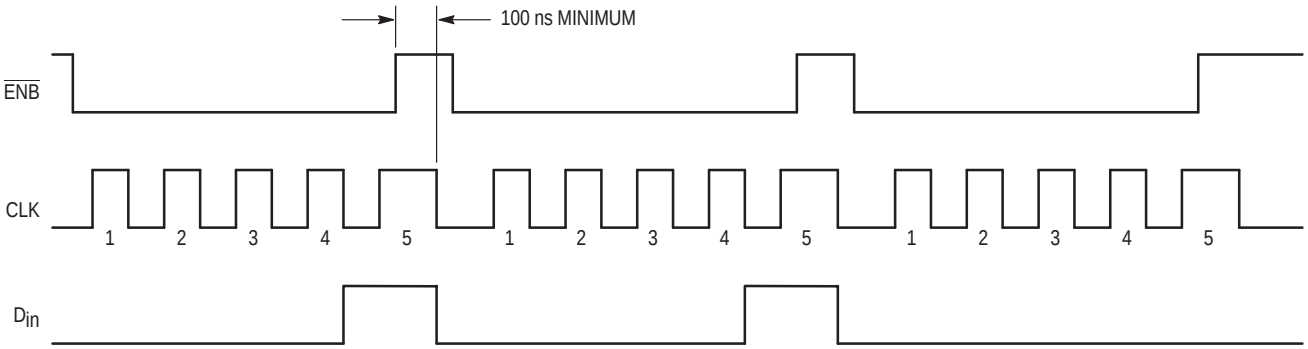
V_{PD}
Positive Power Supply (Pin 5)

This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin must be no less than the potential applied to the V_{DD} pin. The maximum voltage can be + 5.5 V with respect to the GND pin.

For optimum performance, V_{PD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND
Ground (Pin 7)

Common ground.



NOTE: It may not be convenient to control the $\overline{ENB}$ or CLK pins during power up per the Pin Descriptions. If this is the case, the part may be initialized through the serial port as shown in the figure above. The sequence is similar to accessing the registers except that the CLK must remain high at least 100 ns after $\overline{ENB}$ is brought high. Note that 3 groups of 5 bits are needed.

Figure 13. Initializing the PLL through the Serial Port

Nominal PD_{out} Spurious Current vs f_R Frequency ($1\ V < PD_{out} < V_{PD} - 1\ V$)

f_R (kHz)	Current (RMS nA)
10	3.6
20	4.6
50	17
100	75
200	244

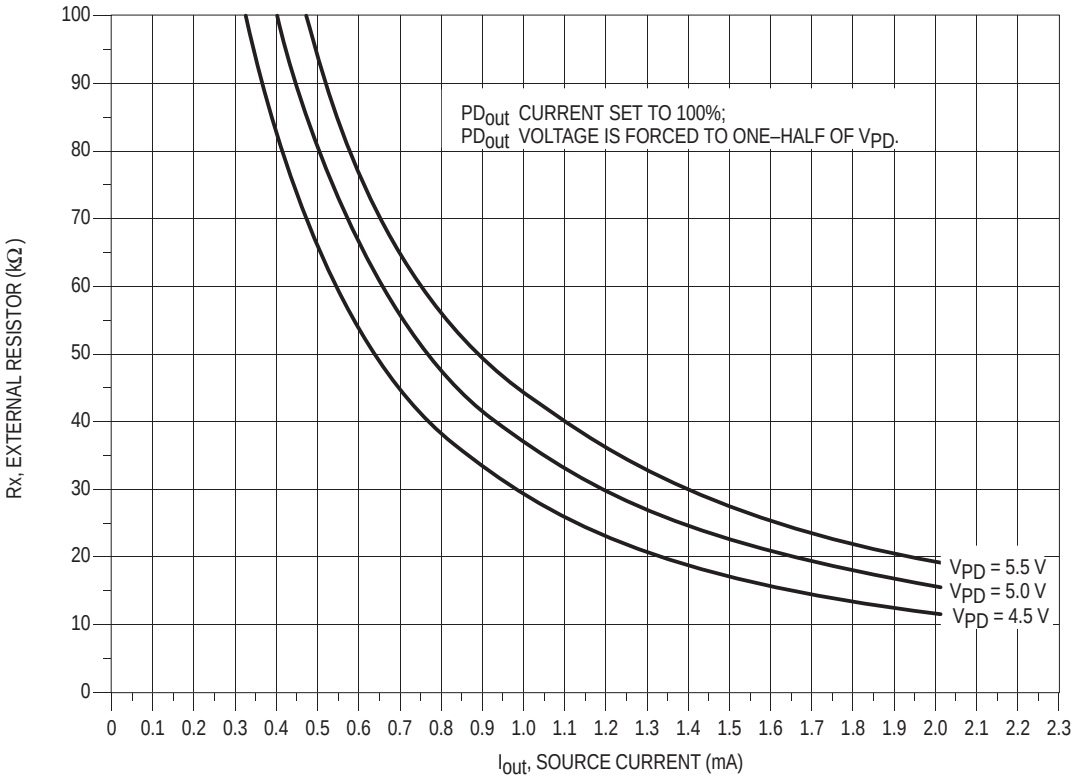
NOTE: For information on spurious current measurement see AN1253/D, "An Improved PLL Design Method Without ω_n and ζ".

Table 2. PD_{out} Current, C1 = Low with OUTPUT A *NOT* Selected as "Port"; Also, Default Mode When OUTPUT A Selected as "Port"

C3	C2	PD_{out} Current
0	0	70%
0	1	80%
1	0	90%
1	1	100%

Table 3. PD_{out} Current, C1 = High with OUTPUT A *NOT* Selected as "Port"

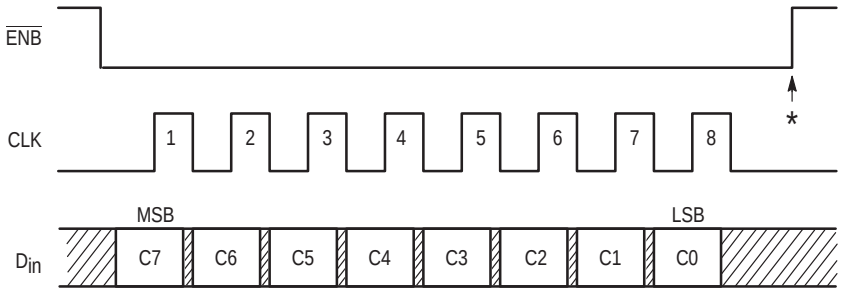
C3	C2	PD_{out} Current
0	0	25%
0	1	50%
1	0	75%
1	1	100%



Nominal MC145191 PD_{out} Source Current vs Rx Resistance

NOTE: The MC145191 is optimized for Rx values in the 18 kΩ to 40 kΩ range. For example, to achieve 0.3 mA of output current, it is preferable to use a 30–kΩ resistor for Rx and bit settings for 25% (as shown in Table 3).

Figure 14.



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts the polarity of PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 18. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output (LD) when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 — STBY: When set high, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high–impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.

When C4 is reset low, the part is taken out of standby in 2 steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C3, C2 — I2, I1: Controls the PD_{out} source/sink current per Tables 2 and 3. With both bits high, the maximum current (as set by Rx per Figure 14) is available. Also, see C1 bit description.

C1 — Port: When the OUTPUT A pin is selected as “Port” via bits A22 and A23, C1 determines the state of OUTPUT A. When C1 is set high, OUTPUT A is forced high; C1 low forces OUTPUT A low. When OUTPUT A is NOT selected as “Port,” C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 2 and 3.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when OUTPUT A is selected as “Port.” The Port bit is not affected by the standby mode.

C0 — Out B: Determines the state of OUTPUT B. When C0 is set high, OUTPUT B is high–impedance; C0 low forces OUTPUT B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 15. C Register Access and Format (8 Clock Cycles are Used)

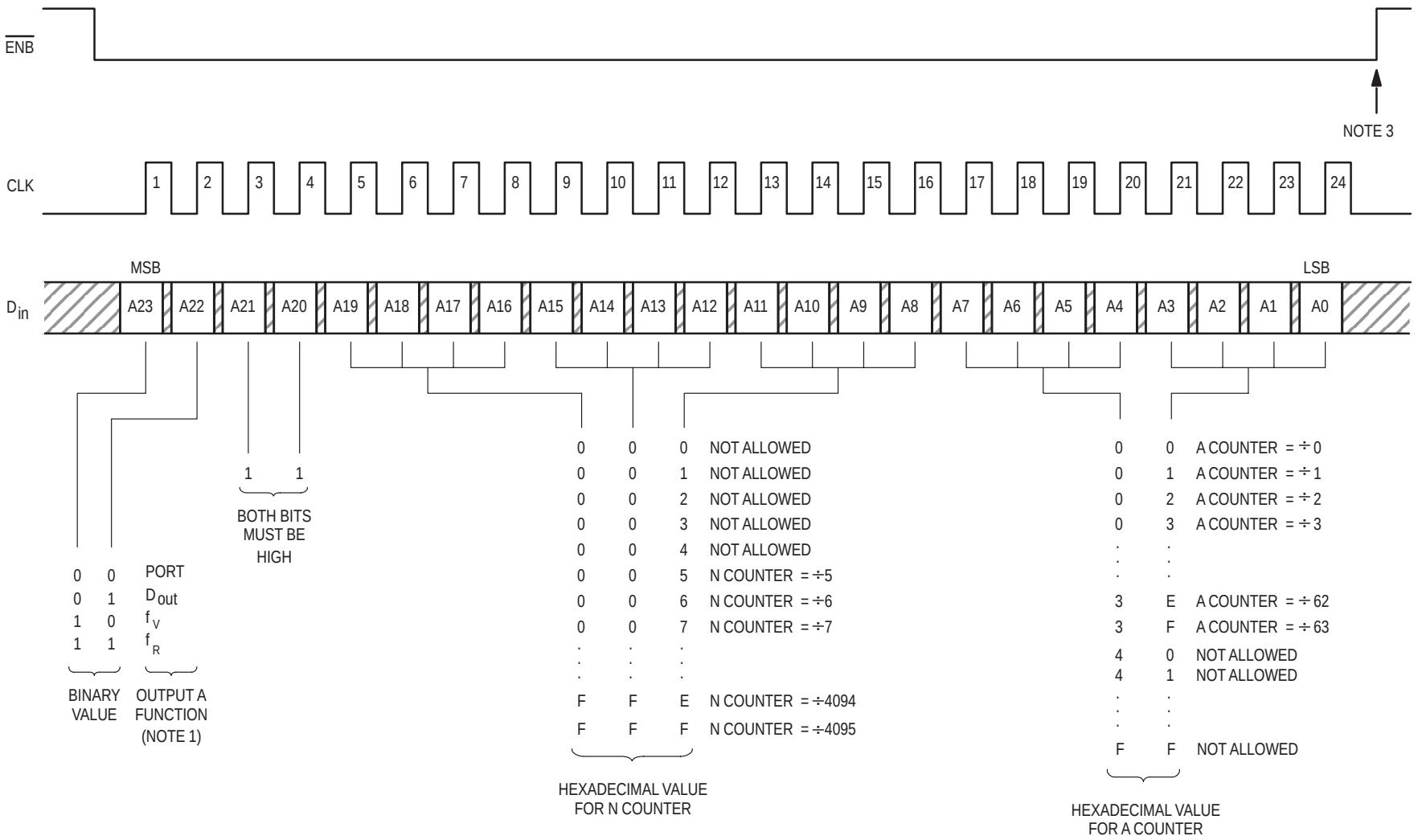
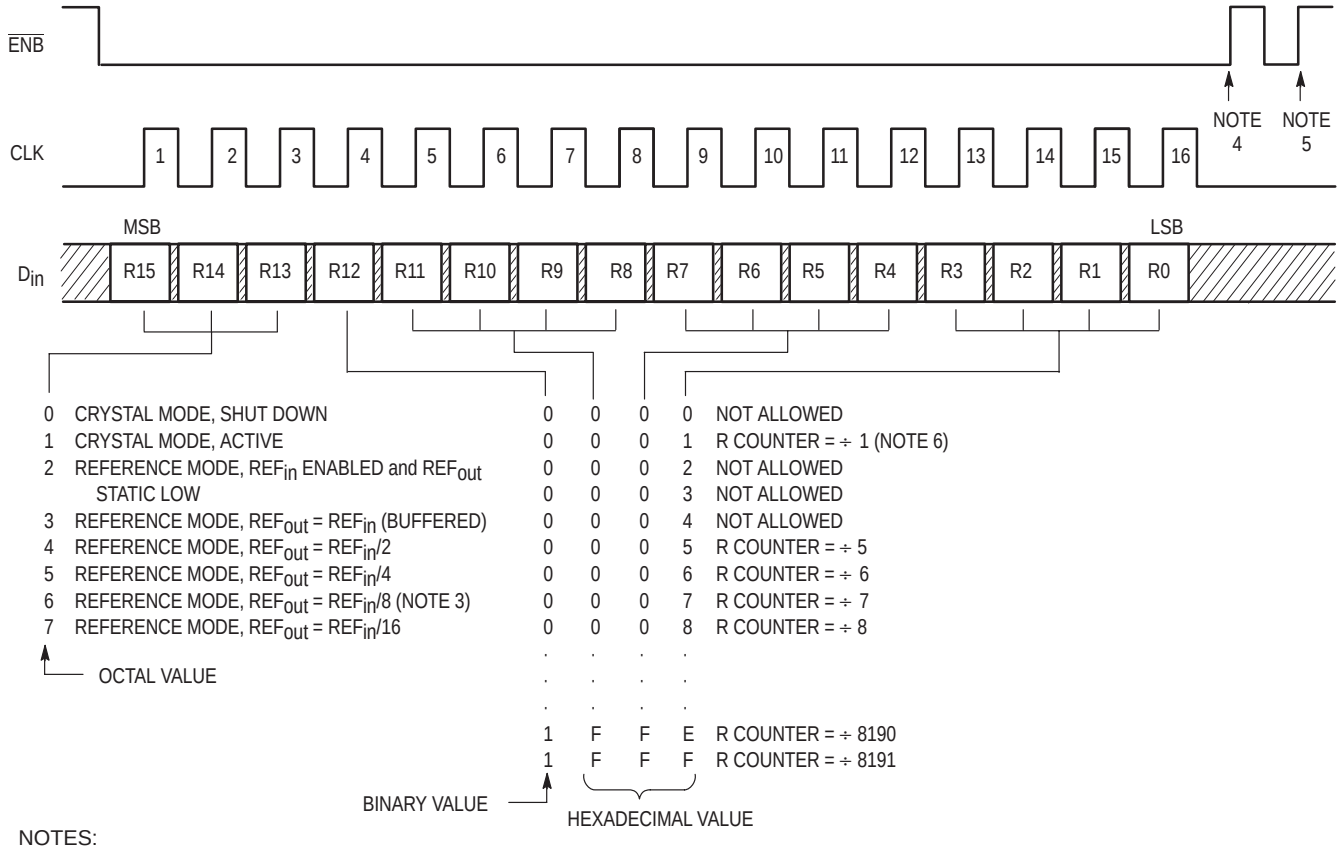


Figure 16. A Register Access and Format (24 Clock Cycles are Used)

NOTES:

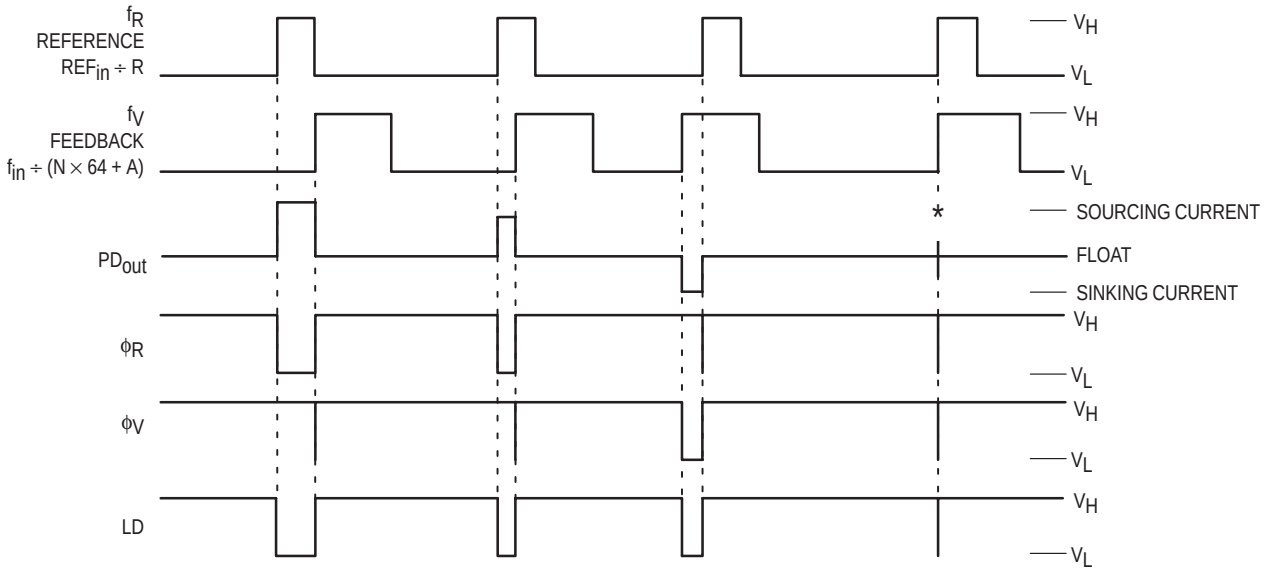
1. A power–on initialize circuit forces the OUTPUT A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.



NOTES:

1. Bits R15 through R13 control the configurable “OSC or 4–stage divider” block (see Block Diagram).
2. Bits R12 through R0 control the “13–stage R counter” block (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the “OSC or 4–Stage Divider” block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. At this point, bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. Also, see note 3 of Figure 16 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 17. R Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.
NOTE: The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.

Figure 18. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in} (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 19.

The crystal should be specified for a loading capacitance (C_L) which does not exceed approximately 20 pF when used at the highest operating frequency of 15 MHz. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_{stray} + \frac{C1 \bullet C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 20)
C_{out} = 6 pF (see Figure 20)
C_a = 1 pF (see Figure 20)
C1 and C2 = external capacitors (see Figure 19)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 21. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 19 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output

frequency (f_R) at OUTPUT A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 4).

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

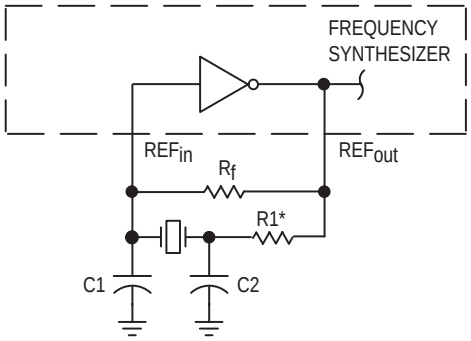
E. Hafner, “The Piezoelectric Crystal Unit–Definitions and Method of Measurement”, *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, “Quartz Crystals for Frequency Control”, *Electro–Technology*, June 1969.

P. J. Ottowitz, “A Guide to Crystal Selection”, *Electronic Design*, May 1966.

D. Babin, “Designing Crystal Oscillators”, *Machine Design*, March 7, 1985.

D. Babin, “Guidelines for Crystal Oscillator Design”, *Machine Design*, April 25, 1985.



* May be needed in certain cases. See text.

Figure 19. Pierce Crystal Oscillator Circuit

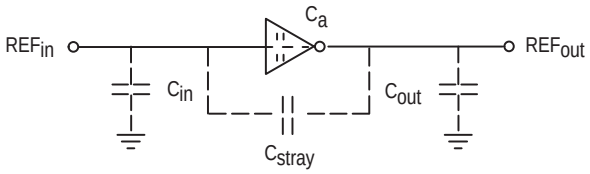
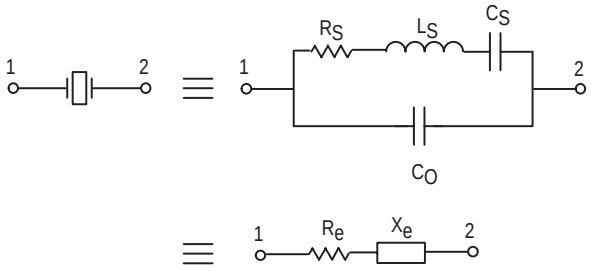


Figure 20. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 21. Equivalent Crystal Networks

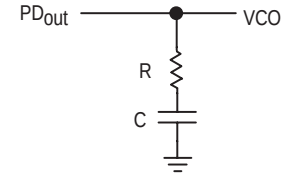
Table 4. Partial List of Crystal Manufacturers

United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP—LOW PASS FILTER DESIGN

(A)



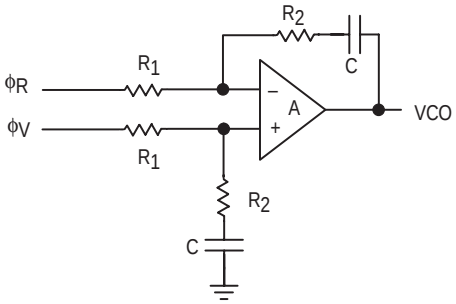
$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:
For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:
For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

* The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:
N = Total Division Ratio in Feedback Loop
K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}
K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

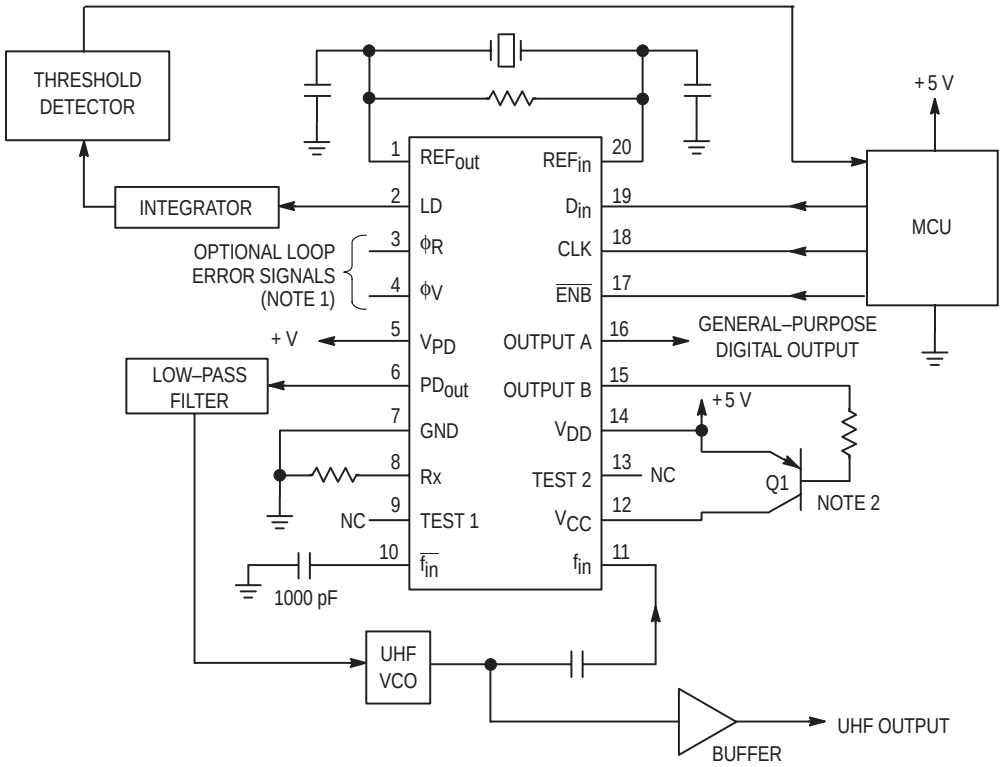
K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

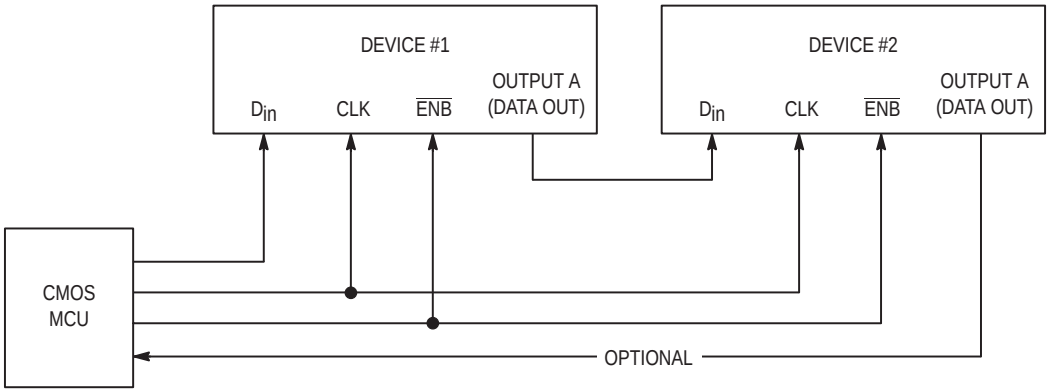
Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.
AN1253/D, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general–purpose digital pin, OUTPUT B. If the standby feature is not needed, tie Pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low–inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

Figure 22. Example Application



NOTE: See related Figures 24 through 26; these bit streams apply to the MC145191 and MC145201.

Figure 23. Cascading Two Devices

Figure 24. Accessing the C Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the C registers of both devices and stored. No other registers are affected.

Figure 25. Accessing the A Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

Figure 26. Accessing the R Registers of Two Cascaded Devices

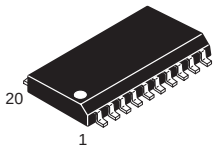
NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14, and R15 are stored and sent to the “OSC or 4-Stage Divider” block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double-buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. At this point, the bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{\text{ENB}}$ pulse, as shown. Also, see note of Figure 25 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

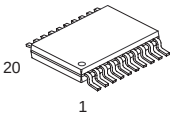
Low-Voltage 1.1 GHz PLL Frequency Synthesizer

Includes On–Board 64/65 Prescaler

MC145192



F SUFFIX
SOG PACKAGE
CASE 751J



DT SUFFIX
TSSOP
CASE 948D

ORDERING INFORMATION

MC145192F	SOG Package
MC145192DT	TSSOP

The MC145192 is a low–voltage single–package synthesizer with serial interface capable of direct usage up to 1.1 GHz. A special architecture makes this PLL very easy to program because a byte–oriented format is utilized. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 3–byte serial transfer to the 24–bit A register. The interface is both SPI and MICROWIRE™ compatible.

The device features a single–ended current source/sink phase detector A output and a double–ended phase detector B output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single–ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

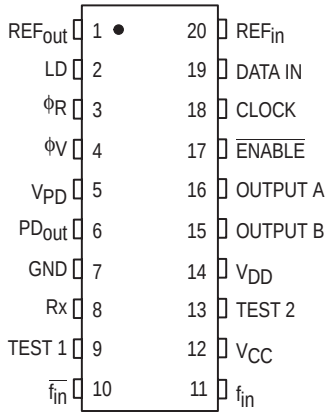
The MC145192 phase/frequency detector B ϕ_R and ϕ_V outputs can be powered from 2.7 to 5.5 V. This is optimized for 3.0 V systems. The phase/frequency detector A PD_{out} output must be powered from 4.5 to 5.5 V, and is optimized for a 5 volt supply.

This part includes a differential RF input which may be operated in a single–ended mode. Also featured are on–board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on–board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double–buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

PIN ASSIGNMENT

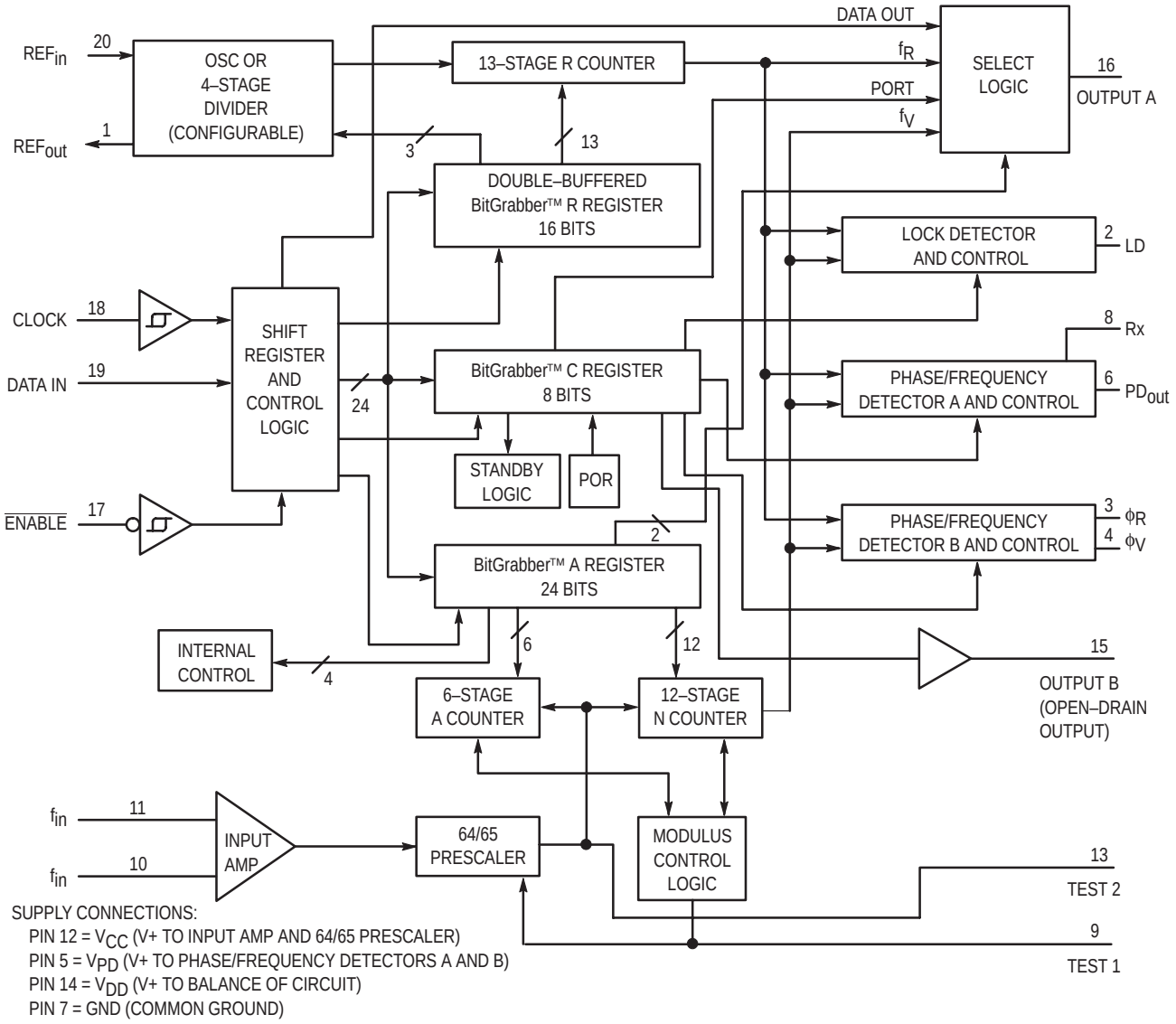


- Maximum Operating Frequency: 1100 MHz @ V_{in} = 200 mV p–p
- Operating Supply Current: 6 mA Nominal at 2.7 V
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 2.7 to 5.0 V
- Operating Supply Voltage Range of Phase Frequency Detector A (V_{PD} Pin) = 4.5 to 5.5 V
- Operating Supply Voltage Range of Phase Detector B (V_{PD} Pin) = 2.7 to 5.5 V
- Current Source/Sink Phase Detector Output Capability: 2 mA Maximum
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: – 40° to 85°C
- R Counter Division Range: (1 and) 5 to 8191
- N Counter Division Range: 5 to 4095
- A Counter Division Range: 0 to 63
- Dual–Modulus Capability Provides Total Division up to 262,143
- High–Speed Serial Interface: 2 Megabits per Second
- Output A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General–Purpose Digital Outputs — Output A: Totem–Pole (Push–Pull) with Four Output Modes
  Output B: Open–Drain
- Power–Saving Standby Feature with Patented Orderly Recovery for Minimizing Lock Times, Standby Current: 30 μA

NOT RECOMMENDED FOR NEW DESIGN
DEVICES TO BE PHASED OUT.
Consider MC145193 for New Designs.

REV 4
12/99

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)	– 0.5 to + 6.0	V
V_{PD}	DC Supply Voltage (Pin 5)	V_{DD} – 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage, except Output B, PD_{out}, ϕ_R, ϕ_V Output B, PD_{out}, ϕ_R, ϕ_V	 – 0.5 to V_{DD} + 0.5 – 0.5 to V_{PD} + 0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

ELECTRICAL CHARACTERISTICS (V_{DD} = V_{CC} = 2.7 to 5.0 V, Voltages Referenced to GND, T_A = – 40° to 85°C, unless otherwise stated; Phase/Frequency Detector A V_{PD} = 4.5 to 5.5 V with $V_{DD} \leq V_{PD}$; Phase/Frequency Detector B V_{PD} = 2.7 to 5.5 V with $V_{DD} \leq V_{PD}$)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (Data In, Clock, $\overline{\text{Enable}}$, REF_{in})	Device in Reference Mode, DC Coupled	0.2 x V_{DD}	V
V_{IH}	Minimum High–Level Input Voltage (Data In, Clock, $\overline{\text{Enable}}$, REF_{in})	Device in Reference Mode, DC Coupled	0.8 x V_{DD}	V
V_{Hys}	Minimum Hysteresis Voltage (Clock, $\overline{\text{Enable}}$)	V_{DD} = 2.7 V V_{DD} = 5.0 V	100 300	mV
V_{OL}	Maximum Low–Level Output Voltage (REF_{out}, Output A)	I_{out} = 20 μA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, Output A)	I_{out} = – 20 μA, Device in Reference Mode	V_{DD} – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out}, LD)	V_{out} = 0.4 V	0.25	mA
I_{OL}	Minimum Low–Level Output Current (ϕ_R, ϕ_V)	V_{out} = 0.4 V V_{DD}, V_{PD} = 2.7 V	0.36	mA
I_{OL}	Minimum Low–Level Output Current (Output A)	V_{out} = 0.4 V	0.6	mA
I_{OL}	Minimum Low–Level Output Current (Output B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High–Level Output Current (REF_{out}, LD)	V_{out} = V_{DD} – 0.4 V	– 0.25	mA
I_{OH}	Minimum High–Level Output Current (ϕ_R, ϕ_V)	V_{out} = V_{PD} – 0.4 V V_{DD}, V_{PD} = 2.7 V	– 0.36	mA
I_{OH}	Minimum High–Level Output Current (Output A Only)	V_{out} = V_{DD} – 0.4 V	– 0.35	mA
I_{in}	Maximum Input Leakage Current (Data In, Clock, $\overline{\text{Enable}}$, REF_{in})	V_{in} = V_{DD} or GND, Device in XTAL Mode	± 1.0	μA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V_{DD} or GND, Device in Reference Mode	± 150	μA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{out} = V_{PD} – 0.5 V or 0.5 V, Output in High–Impedance State	± 200	nA
	(Output B)	Output in High–Impedance State	± 10	μA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	V_{in} = V_{DD} or GND; Outputs Open; Device in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode; Output B Controlling V_{CC} per Figure 22	30	μA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static Low or High, Bit C4 = Low Which is NOT Standby, I_{RX} = 113 μA, V_{PD} = 5.5 V	600	μA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is NOT Standby	30	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 1.1 GHz; REF_{in} = 13 MHz @ 1 V p–p; Output A = Inactive and No Connect; V_{DD} = V_{CC}, REF_{out}, $\overline{\phi V}$, $\overline{\phi R}$, PD_{out}, LD = No Connect; Data In, $\overline{\text{Enable}}$, Clock = V_{DD} or GND, Phase Detector A Off	*	mA

* The nominal values are:
6 mA at V_{DD} = 2.7 V and V_{PD} = 2.7 V
9 mA at V_{DD} = 5.0 V and V_{PD} = 5.5 V
These are not guaranteed limits.

ANALOG CHARACTERISTICS — CURRENT SOURCE/SINK OUTPUT — PD_{out}

($I_{out} \leq 2$ mA, $V_{DD} = V_{CC} = 2.7$ to 5.0 V, Voltages Referenced to GND, $V_{DD} = V_{CC} \leq V_{PD}$)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation Part–to–Part	$V_{out} = 0.5 \times V_{PD}$	4.5	± 20	%
		5.5	± 20	
Maximum Sink–versus–Source Mismatch	$V_{out} = 0.5 \times V_{PD}$	4.5	12	%
(Note 3)		5.5	12	
Output Voltage Range	I_{out} variation ≤ 20%	4.5	0.5 to 4.0	V
(Note 3)		5.5	0.5 to 5.0	

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value) / Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within – 40° to 85°C.

AC INTERFACE CHARACTERISTICS

($V_{DD} = V_{CC} = 2.7$ to 5.0 V, $T_A = -40°$ to 85°C, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns, $V_{PD} = 2.7$ to 5.5 V with $V_{DD} \leq V_{PD}$)

Symbol	Parameter	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Figure 1) NOTE: Refer to Clock t_W below	dc to 2.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Output A (Selected as Data Out) (Figures 1 and 5)	200	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{\text{Enable}}$ to Output A (Selected as Port) (Figures 2 and 5)	200	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{\text{Enable}}$ to Output B (Figures 2 and 6)	200	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Output A and Output B; t_{THL} only, on Output B (Figures 1, 5, and 6)	200	ns
C_{in}	Maximum Input Capacitance — Data In, Clock, $\overline{\text{Enable}}$	10	pF

TIMING REQUIREMENTS ($V_{DD} = V_{CC} = 2.7$ to 5.0 V, $T_A = -40°$ to 85°C, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, Data In versus Clock (Figure 3)	50	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{\text{Enable}}$ versus Clock (Figure 4)	100	ns
t_W	Minimum Pulse Width, $\overline{\text{Enable}}$ (Figure 4)	*	cycles
t_W	Minimum Pulse Width, Clock (Figure 1)	250	ns
t_r, t_f	Maximum Input Rise and Fall Times, Clock (Figure 1)	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

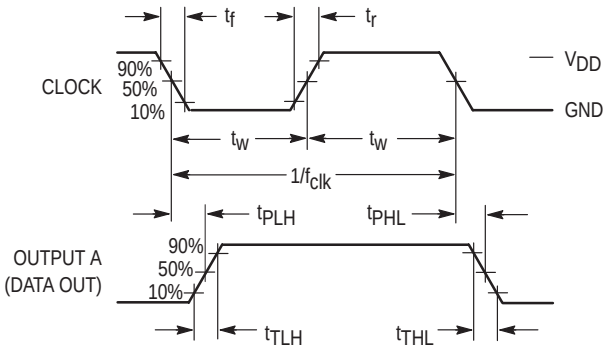


Figure 1.

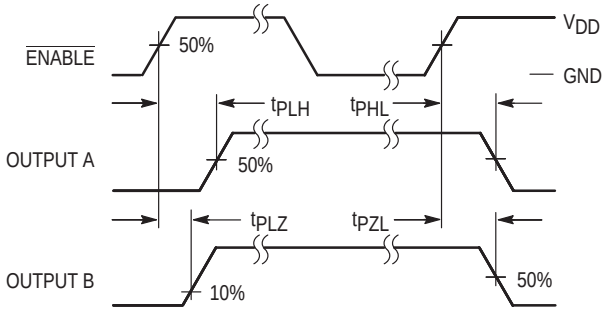


Figure 2.

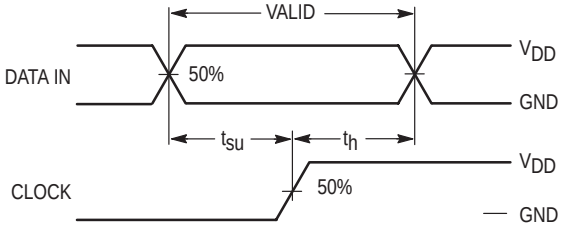


Figure 3.

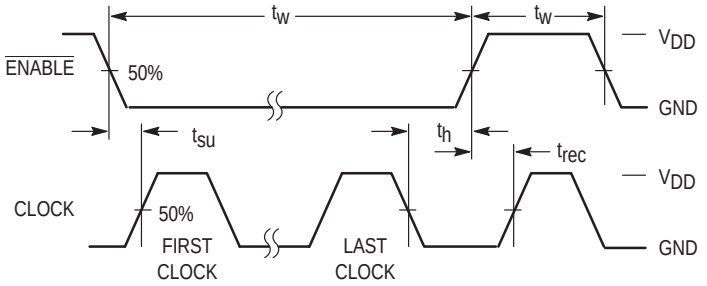
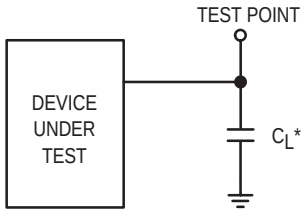
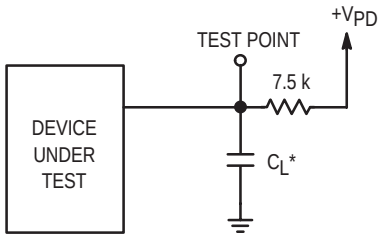


Figure 4.



* Includes all probe and fixture capacitance.

Figure 5. Test Circuit



* Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 2.7 to 5.0 V unless otherwise indicated, T_A = – 40° to 85°C)

Symbol	Parameter	Test Condition	Guaranteed Operating Range		Unit
			Min	Max	
V_{in}	Input Voltage Range, f_{in} (Figure 7)	100 MHz ≤ f_{in} < 250 MHz 250 MHz ≤ f_{in} ≤ 1100 MHz	400 200	1500 1500	mV p–p
f_{ref}	Input Frequency, REF_{in} Externally Driven in Reference Mode (Figure 8)	V_{in} ≥ 400 mV p–p V_{DD} = 2.7 V V_{DD} = 3.0 V V_{DD} = 3.5 V V_{DD} = 4.5 to 5 V	 1 4.5 5.5 12	 20 20 20 27	MHz
		V_{in} ≥ 1 V p–p V_{DD} = 2.7 V V_{DD} = 3.0 V V_{DD} = 3.5 V V_{DD} = 4.5 to 5 V	 1 1.5 2 4.5	 20 20 20 27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode (Figure 9)	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance	2	10	MHz
f_{out}	Output Frequency, REF_{out} (Figures 10 and 12)	C_L = 30 pF	dc	5	MHz
f	Operating Frequency of the Phase Detectors		dc	1	MHz
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD (Figures 11 and 12)	f_R in Phase with f_V, C_L = 50 pF, V_{PD} = 2.7 V, V_{DD} = V_{CC} = 2.7 V	20	140	ns
t_{TLH}, t_{THL}	Output Transition Times, LD, ϕ_V, and ϕ_R (Figures 11 and 12)	C_L = 50 pF, V_{PD} = 2.7 V, V_{DD} = V_{CC} = 2.7 V	—	80	ns
C_{in}	Input Capacitance, REF_{in}		—	5	pF

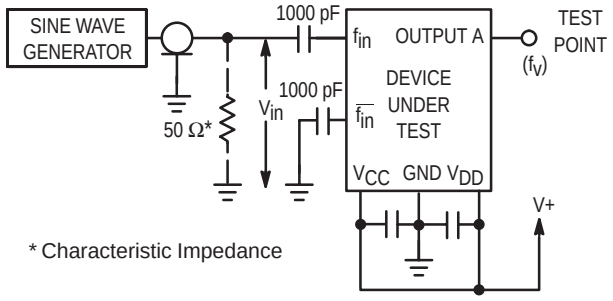


Figure 7. Test Circuit

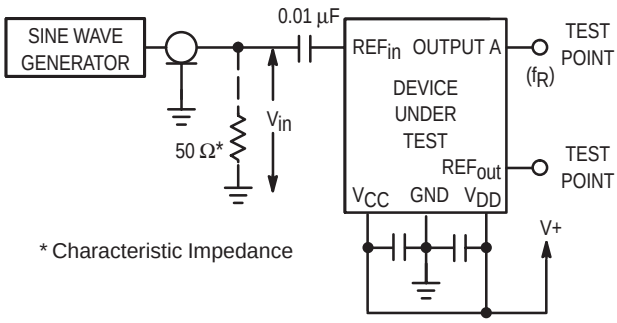


Figure 8. Test Circuit–Reference Mode

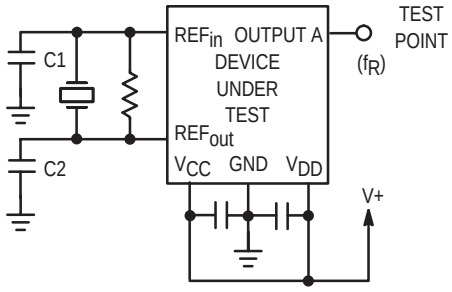


Figure 9. Test Circuit–Crystal Mode

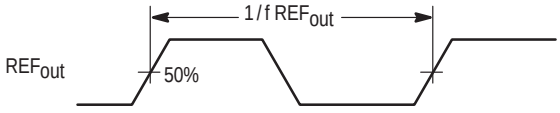


Figure 10. Switching Waveform

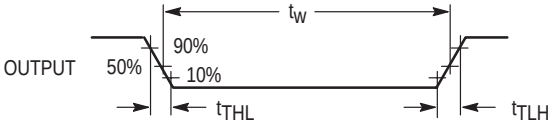


Figure 11. Switching Waveform

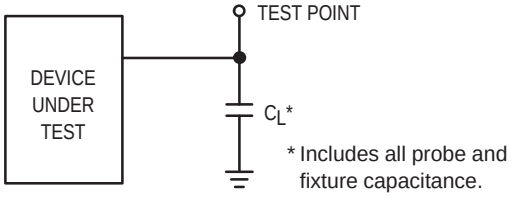
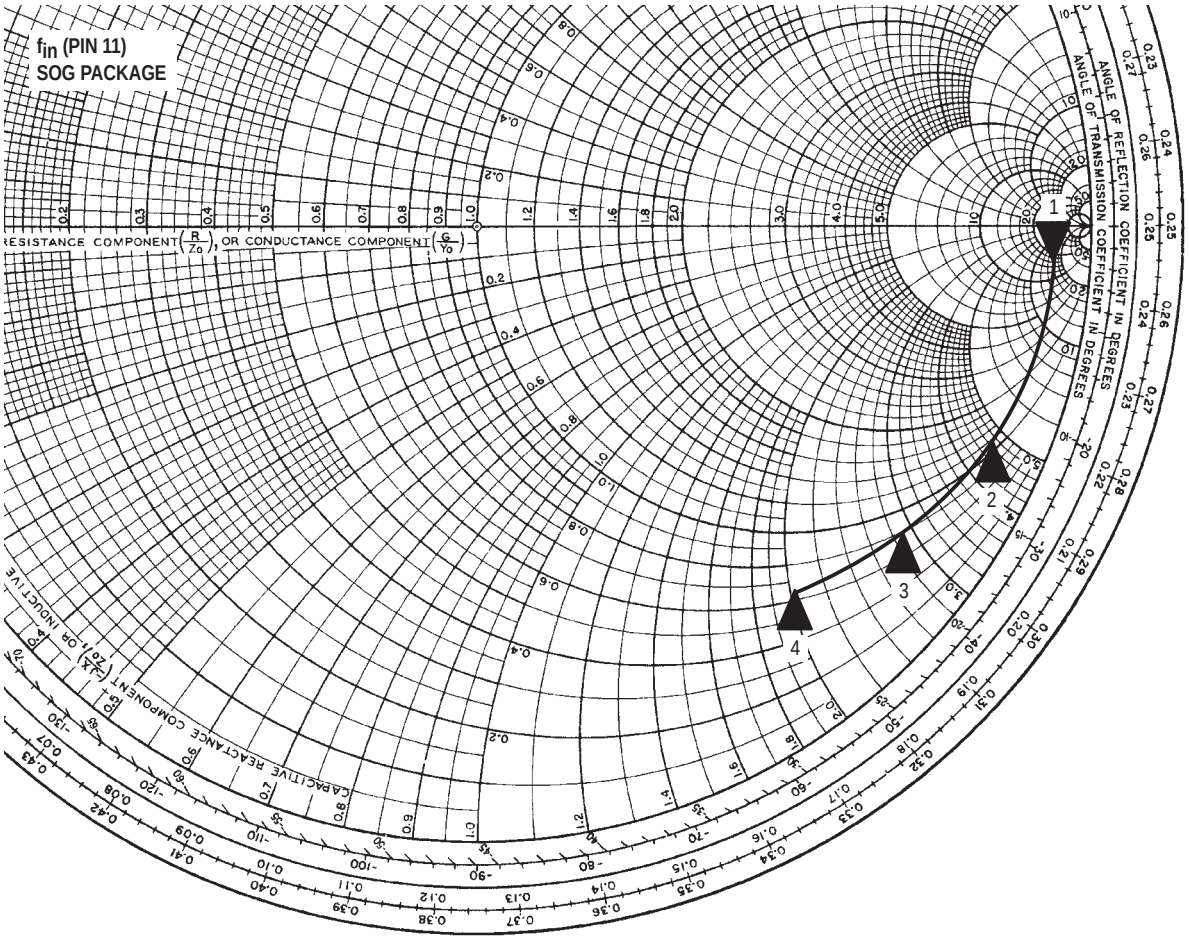


Figure 12. Test Circuit



Marker	Frequency (MHz)	Resistance (Ω)	Capacitive Reactance (Ω)	Capacitance (pF)
1	100	574	– 881	1.81
2	500	57.9	– 242	1.31
3	800	38.3	– 148	1.34
4	1100	31.6	– 103	1.40

Figure 13. Normalized Input Impedance at f_{in} — Series Format (R + jX) (100 MHz to 1100 MHz)

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

Data In (Pin 19)

Serial Data Input. The bit stream begins with the MSB and is shifted in on the low–to–high transition of Clock. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 1). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{\text{Enable}}$.

CAUTION

The value programmed for the N–counter must be greater than or equal to the value of the A–counter.

The 13 LSBs of the R register are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24–bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16–bit transfer may be followed by pulsing $\overline{\text{Enable}}$ low with no signal on the Clock pin. This is an alternate method of transferring data to the second buffer of the R register. See Figure 17.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 2.7 to 5.0 V. The formats are shown in Figures 15, 16, and 17.

Data In typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first, C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	Not Allowed	
Values > 32	See Figures 24 to 27	

Clock (Pin 18)

Serial Data Clock Input. Low–to–high transitions on Clock shift bits available at the Data pin, while high–to–low transitions shift bits from Output A (when configured as Data Out, see Pin 16). The 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A register. See Table 1 and Figures 15, 16, and 17. The number of clocks required for cascaded devices is shown in Figures 25 through 27.

Clock typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow Clock rise and fall times are allowed. See the last paragraph of **Data In** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the Clock pin must be held at GND (with $\overline{\text{Enable}}$ being a don't care) or $\overline{\text{Enable}}$ must be held at the potential of the V+ pin (with Clock being a don't care) during power–up. As an alternative, the bit sequence of Figure 18 may be used.

$\overline{\text{Enable}}$ (Pin 17)

Active–Low Enable Input. This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{\text{Enable}}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{\text{Enable}}$ (which must start inactive high) is taken low, a serial transfer is made via Data In and Clock, and $\overline{\text{Enable}}$ is taken back high. The low–to–high transition on $\overline{\text{Enable}}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{\text{Enable}}$ must not be attempted while Clock is high. This will put the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{\text{Enable}}$ is high and Clock is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **Data In** for more information.

For POR information, see the note for the **Clock pin**.

Output A (Pin 16)

Configurable Digital Output. Output A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 16.

If A23 = A22 = high, Output A is configured as f_R. This signal is the buffered output of the 13–stage R counter. The f_R signal appears as normally low and pulses high. The f_R signal can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0 through R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of one. See Figure 17. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_R should not exceed 1 MHz.

If A23 = high and A22 = low, Output A is configured as f_V. This signal is the buffered output of the 12–stage N counter.

The f_V signal appears as normally low and pulses high. The f_V signal can be used to verify the operation of the prescaler, A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is $N \times 64 + A$. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 16. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_V should not exceed 1 MHz.

If A23 = low and A22 = high, Output A is configured as Data Out. This signal is the serial output of the 24–1/2–stage shift register. The bit stream is shifted out on the high–to–low transition of the Clock input. Upon power up, Output A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, Output A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

Output B (Pin 15)

Open–Drain Digital Output. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, Output B assumes the high–impedance state. Output B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. Note: the maximum voltage allowed on the V_{PD} pin is 5.5 V for the MC145192.

Upon power–up, power–on reset circuitry forces Output B to a low level.

REFERENCE PINS

REF_{in} and REF_{out} (Pins 20 and 1)

Configurable Pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 17.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The device is designed to operate with crystals up to 10 MHz; the required connections are shown in Figure 9. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary). This is the active–crystal mode shown in Figure 17. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode shown in Figure 17, and can be engaged whether in standby or not.

In the reference mode, REF_{in} (Pin 20) accepts a signal up to 20 MHz from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. The ac–coupled signal must be at least 400 mV p–p. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 17 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 5 MHz for V_{DD} to V_{SS} swing. Therefore, for REF_{in} frequencies above 5 MHz, the one–to–one ratio may not be used for large signal swing requirements. Likewise, for REF_{in} frequencies above 10 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in} and $\overline{f_{in}}$ (Pins 11 and 10)

Frequency Input from the VCO. These pins feed the on–board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they are usually used in a single–ended configuration as shown in Figure 7. Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out} (Pin 6)

Single–Ended Phase/Frequency Detector Output. This is a 3–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 19.

POL bit (C7) in the C register = low (see Figure 15)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state

Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state
Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the floating state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the floating state when the device is put into standby (STBY bit C4 = high).

The PD_{out} circuit is powered by V_{PD}. The phase detector gain is controllable by bits C3, C2, and C1: gain (in amps per radian) = PD_{out} current divided by 2π.

ϕ_R and ϕ_V (Pins 3 and 4)

Double–Ended Phase/Frequency Detector Outputs. These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 19.

POL bit (C7) in the C register = low (see Figure 15)
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD (Pin 2)

Lock Detector Output. This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V. See Figure 19.

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false lock signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx (Pin 8)

External Resistor. A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Figure 15 for other values of current. To achieve a maximum current of 2 mA, the resistor should be about 22 kΩ when V_{PD} is 5 V.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

TEST POINT PINS

Test 1 (Pin 9)

Modulus Control Signal. This pin may be used in conjunction with the Test 2 pin for access to the on–board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and must be floated in an actual application. This pin may be attached to an isolated pad with no trace.

Test 2 (Pin 13)

Prescaler Output. This pin may be used to access to the on–board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and must be floated in an actual application. This pin may be attached to an isolated pad with no trace.

POWER SUPPLY PINS

V_{DD} (Pin 14)

Positive Supply Potential. This pin supplies power to the main CMOS digital portion of the device. The voltage range is + 2.7 to + 5.0 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC} (Pin 12)

Positive Supply Potential. This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is + 2.7 to + 5.0 V with respect to the GND pin. In the standby mode, the V_{CC} pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 23.

For optimum performance, V_{CC} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

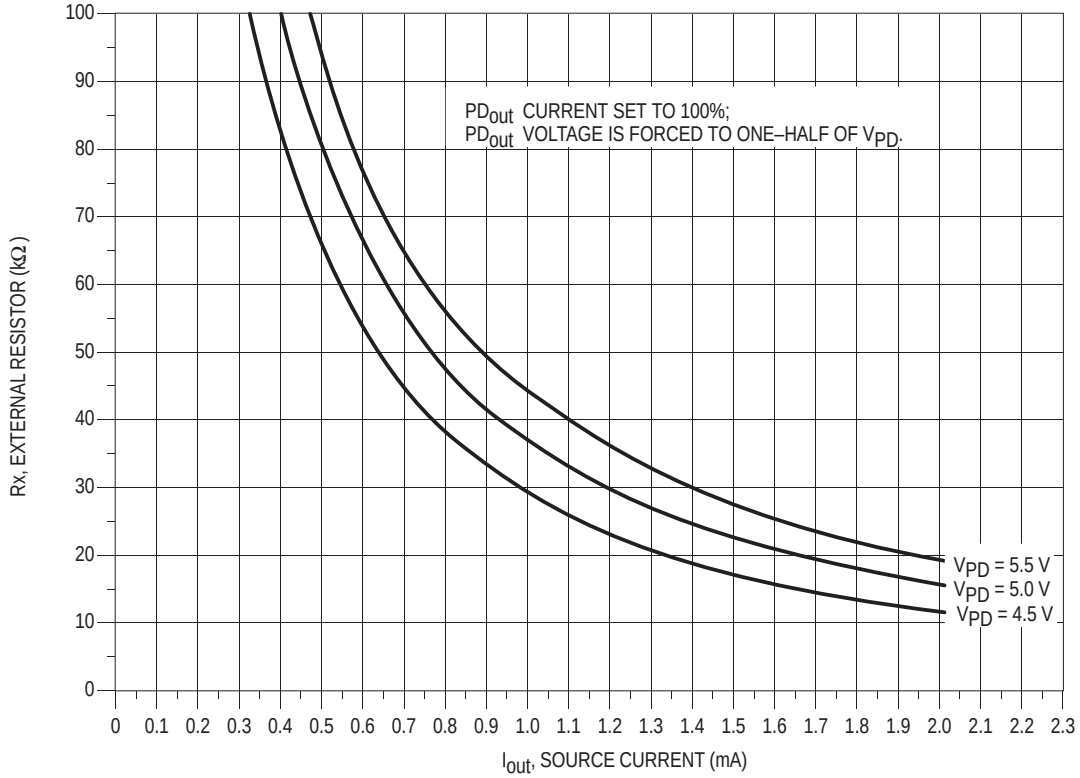
V_{PD} (Pin 5)

Positive Supply Potential. This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin must be ≥ V_{DD} but not more than 5.5 V. The voltage range for V_{PD} is 4.5 to 5.5 V with respect to the GND pin when using PD_{OUT} and 2.7 to 5.5 V when using ϕ_R, ϕ_V outputs.

For optimum performance, V_{PD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND (Pin 7)

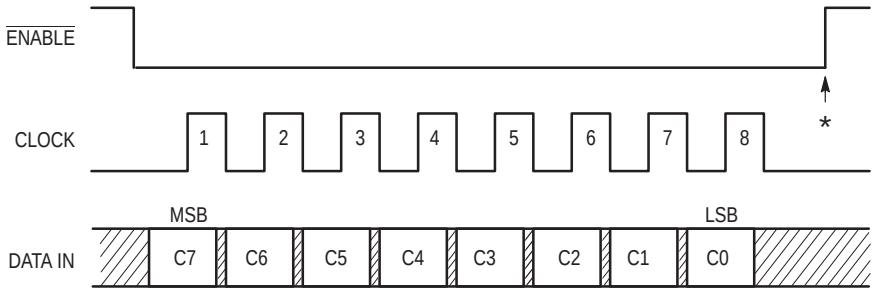
Common ground.



Nominal MC145192 PD_{out} Source Current vs Rx Resistance

NOTE: The MC145192 is optimized for Rx values in the 18 kΩ to 40 kΩ range. For example, to achieve 0.3 mA of output current, it is preferable to use a 30–kΩ resistor for Rx and bit settings for 25% (as shown in Table 3).

Figure 14.



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 – POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 19. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 – PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 – LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 – STBY: When set high, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high–impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.
When C4 is reset low, the part is taken out of standby in 2 steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. This is a patented feature.

C3, C2 – I2, I1: Controls the PD_{out} source/sink current per Tables 2 and 3. With both bits high, the maximum current (as set by Rx) is available. Also, see C1 bit description.

C1 – Port: When the Output A pin is selected as “Port” via bits A22 and A23, C1 determines the state of Output A. When C1 is set high, Output A is forced high; C1 low forces Output A low. When Output A is not selected as “Port,” C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 2 and 3.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when Output A is selected as “Port.” The Port bit is not affected by the standby mode.

C0 – Out B: Determines the state of Output B. When C0 is set high, Output B is high–impedance; C0 low forces Output B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 15. C Register Access and Format (8 Clock Cycles Are Used)

Table 2. PD_{out} Current, C1 = Low with Output A NOT Selected as “Port”; Also, Default Mode When Output A Selected as “Port”

C3	C2	PD_{out} Current
0	0	70%
0	1	80%
1	0	90%
1	1	100%

Table 3. PD_{out} Current, C1 = High with Output A NOT Selected as “Port”

C3	C2	PD_{out} Current
0	0	25%
0	1	50%
1	0	75%
1	1	100%

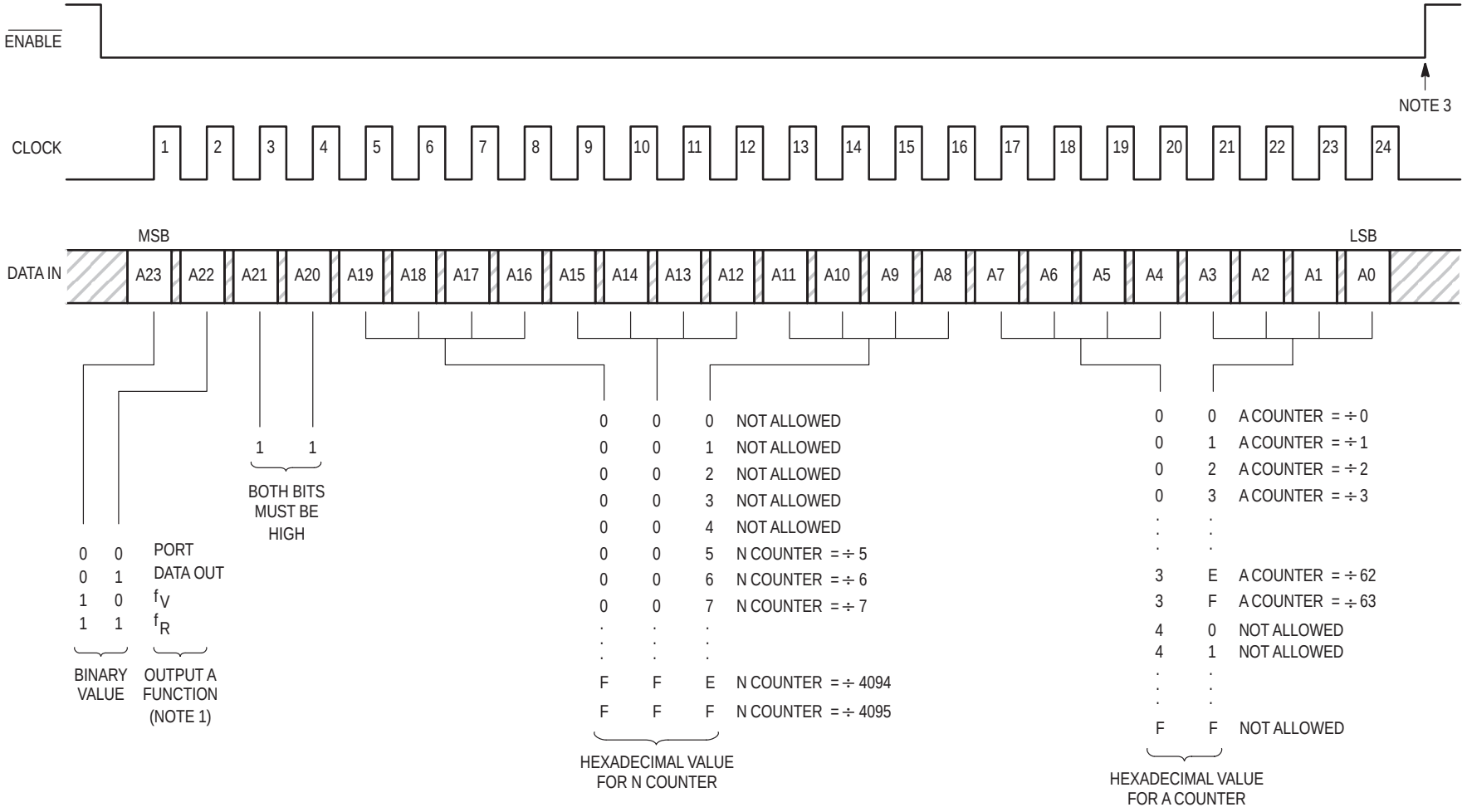
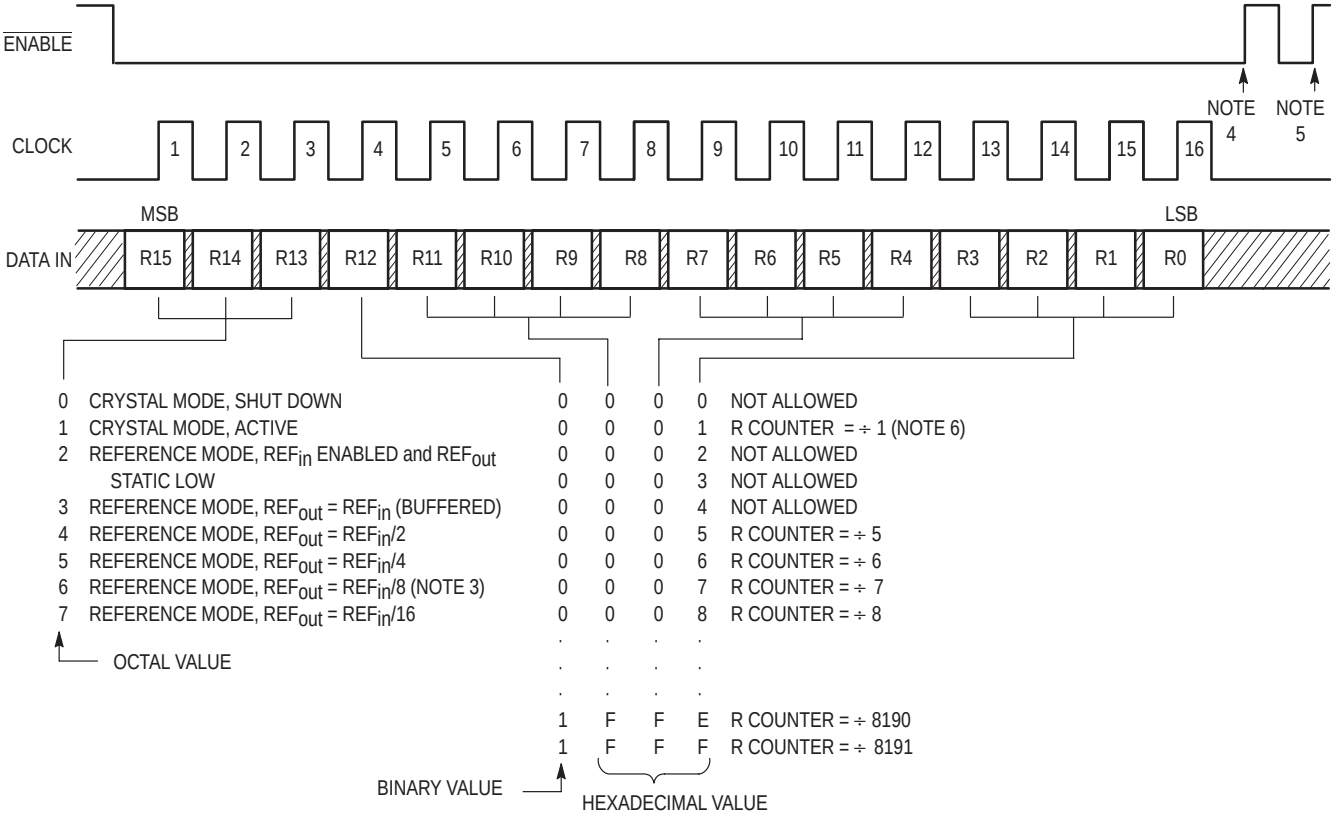


Figure 16. A Register Access and Format (24 Clock Cycles are Used)

NOTES:

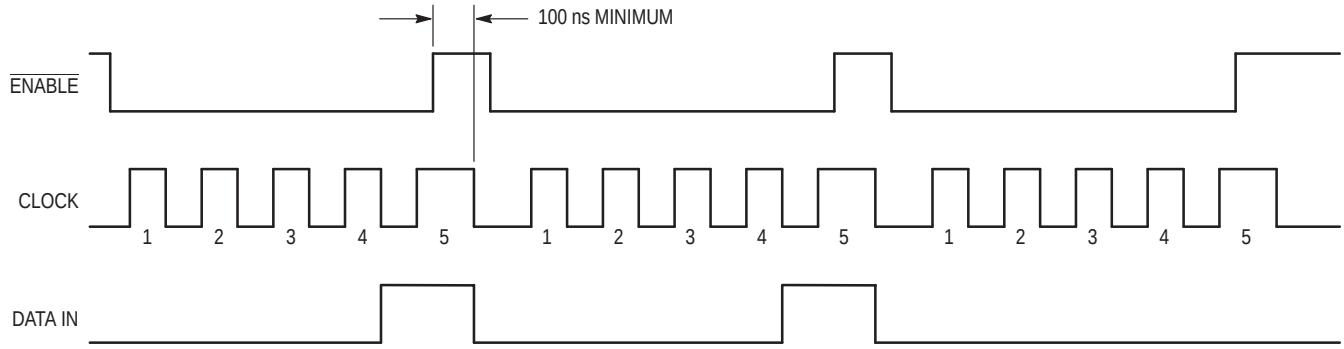
1. A power–on initialize circuit forces the Output A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.



NOTES:

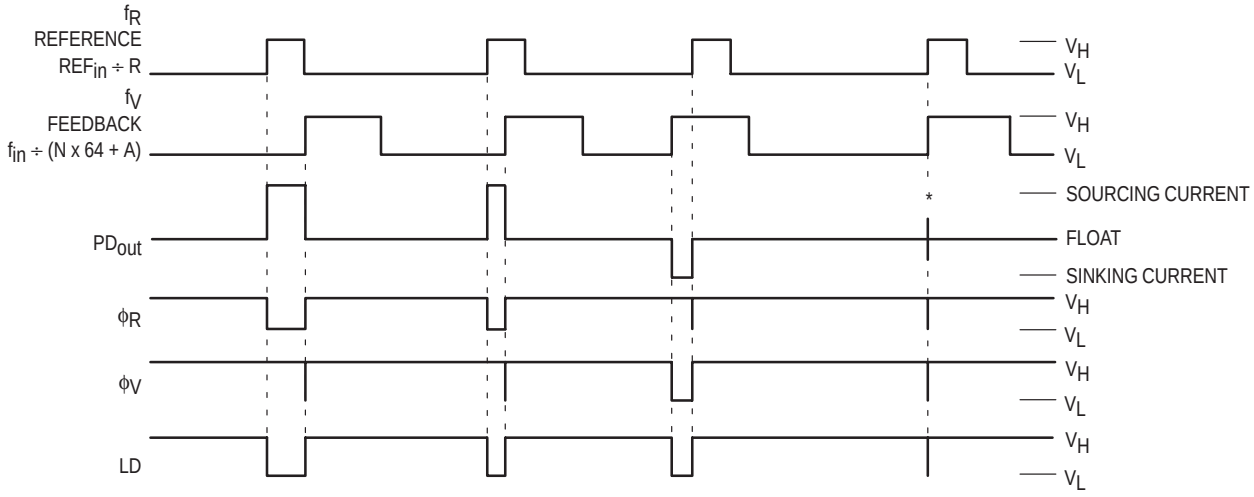
1. Bits R15 through R13 control the configurable “OSC or 4–stage divider” block (see Block Diagram).
2. Bits R12 through R0 control the “13–stage R counter” block (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the “OSC or 4–Stage Divider” block in the Block Diagram. Bits R0 – R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. At this point, bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. Clock must be low during the $\overline{\text{Enable}}$ pulse, as shown. Also, see note 3 of Figure 16 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 17. R Register Access and Format (16 Clock Cycles Are Used)



NOTE: It may not be convenient to control the Enable or Clock pins high during power up per the Pin Descriptions. If this is the case, the part may be initialized through the serial port as shown in the figure above. The sequence is similar to accessing the registers except that the Clock must remain high at least 100 ns after Enable is brought high. Note that 3 groups of 5 bits are needed.

Figure 18. Initializing the PLL through the Serial Port



V_H = High voltage level
V_L = Low voltage level
* At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.
NOTE: The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 15 for POL.

Figure 19. Phase/Frequency Detectors and Lock Detector Output Waveforms

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used. See Figure 8.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

DESIGN AN OFF–CHIP REFERENCE

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in}. (See Figure 8.) For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

USE OF THE ON–CHIP OSCILLATOR CIRCUITRY

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 20.

The crystal should be specified for a loading capacitance, C_L, which does not exceed approximately 20 pF when used at the highest operating frequency of 10 MHz. Assuming R1 = 0 Ω, the shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \bullet C2}{C1 + C2}$$

where

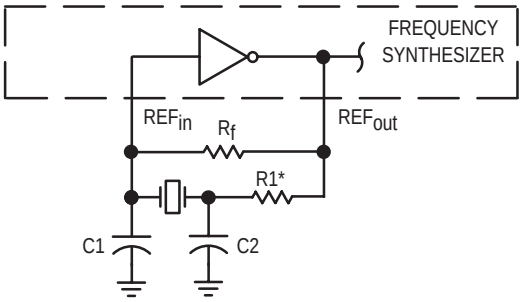
C_{in} = 5 pF (see Figure 21)
C_{out} = 6 pF (see Figure 21)
C_a = 1 pF (see Figure 21)
C1 and C2 = external capacitors (see Figure 20)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making either a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes zero in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 22. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 20 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven; monitor the output frequency (f_R) at Output A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. Note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 4.



* May be needed in certain cases. See text.

Figure 20. Pierce Crystal Oscillator Circuit

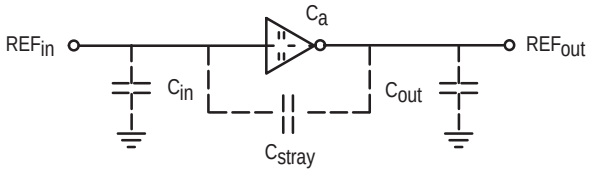
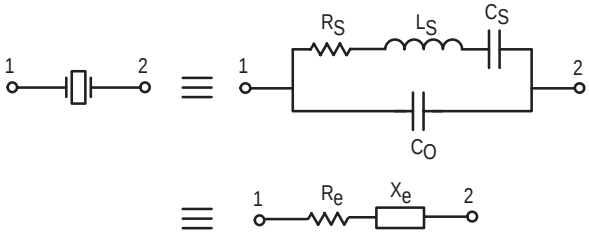


Figure 21. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 22. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, “The Piezoelectric Crystal Unit–Definitions and Method of Measurement”, *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, “Quartz Crystals for Frequency Control”, *Electro–Technology*, June 1969.

P. J. Ottowitz, “A Guide to Crystal Selection”, *Electronic Design*, May 1966.

D. Babin, “Designing Crystal Oscillators”, *Machine Design*, March 7, 1985.

D. Babin, “Guidelines for Crystal Oscillator Design”, *Machine Design*, April 25, 1985.

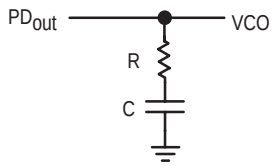
Table 4. Partial List of Crystal Manufacturers

Motorola — Internet Address *http://motorola.com* (Search for resonators)
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

(A)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

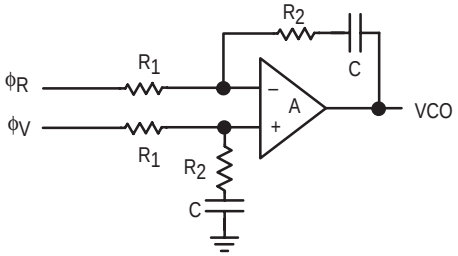
$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:

For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:

For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

* The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

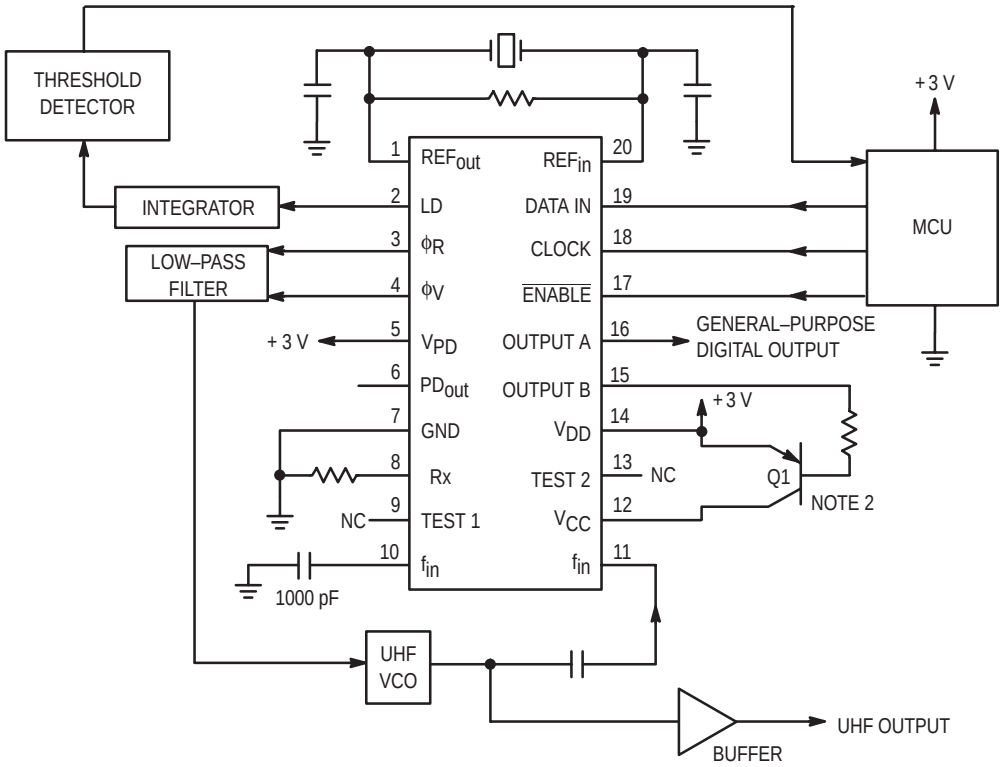
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.

Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

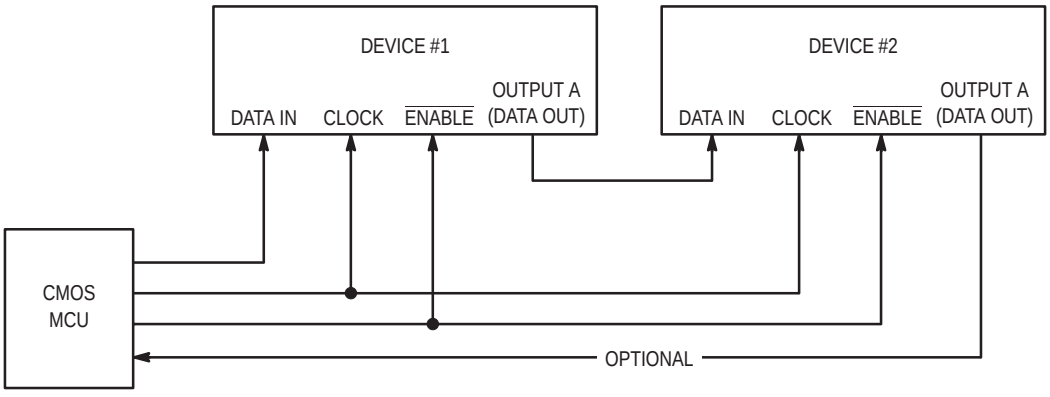
AN1253/D, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general–purpose digital pin, Output B. If the standby feature is not needed, tie Pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low–inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in} / f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

Figure 23. Example Application



NOTE: See related Figures 25, 26, and 27.

Figure 24. Cascading Two Devices

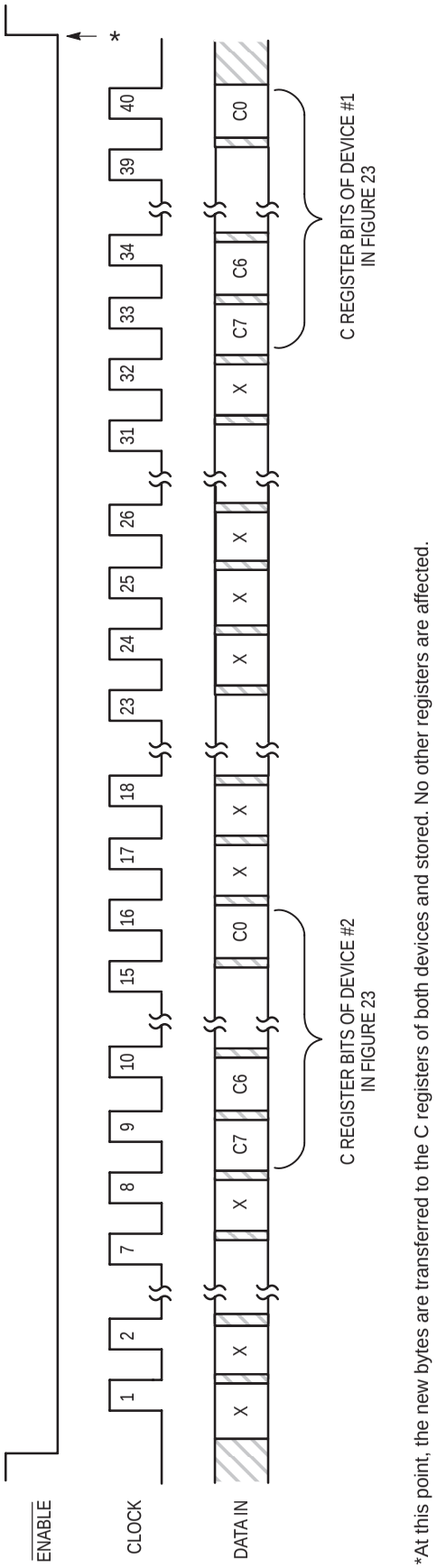


Figure 25. Accessing the C Registers of Two Cascaded Devices

Figure 26. Accessing the A Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

Figure 27. Accessing the R Registers of Two Cascaded Devices

NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14, and R15 are stored and sent to the “OSC or 4–Stage Divider” block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. At this point, the bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. Clock must be low during the $\overline{\text{Enable}}$ pulse, as shown. Also, see note of Figure 25 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

MOTOROLA

MC145193

Product Preview

1.1 GHz PLL Frequency Synthesizer

PLL FREQUENCY SYNTHESIZER

SEMICONDUCTOR TECHNICAL DATA

The MC145193 is pin–for–pin compatible with the previous generation MC145190, MC145191 and MC145192 devices. Table 1 highlights the different features in these four devices. The MC145193 is recommended for new designs, and also offers reduced power consumption.

The counters are programmed via a synchronous serial port which is SPI compatible. The serial port is byte-oriented to facilitate control via an MCU. Due to the innovative BitGrabber Plus™ registers, the MC145193 may be cascaded with other peripherals featuring BitGrabber Plus without requiring leading dummy bits or address bits in the serial data stream. In addition, BitGrabber Plus peripherals may be cascaded with existing BitGrabber™ peripherals.

The device features a single–ended current source/sink phase detector A output and a double–ended phase detector B output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single–ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

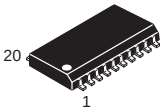
Slew–rate control is provided by a special driver designed for the REF_{out} pin. This minimizes interference caused by REF_{out}.

This part includes a differential RF input that may be operated in a single–ended mode. Also featured are on–board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

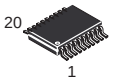
In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on–board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double–buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

- Maximum Operating Frequency: 1100 MHz @ –10 dBm
- Operating Supply Current: 3 mA Nominal at 3.0 V
- Operating Supply Voltage Range (V_{DD}, V_{CC}, V_{PD} Pins): 2.7 to 5.5 V
- Current Source/Sink Phase Detector Output:
  1.7 mA @ 5.0 V or 1.0 mA @ 3.0 V
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- R Counter Division Range: 1 and 5 to 8191
- Dual–Modulus Capability Provides Total Division up to 262,143
- High–Speed Serial Interface: 4 Mbps
- Output A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General–Purpose Digital Outputs:
  Output A: Totem–Pole (Push–Pull) with Four Output Modes
  Output B: Open–Drain
- Patented Power–Saving Standby Feature with Orderly Recovery for Minimizing Lock Times, Standby Current: 30 μA
- See App Note AN1253/D for Low–Pass Filter Design, and AN1277/D for Offset Reference PLLs for Fine Resolution or Fast Hopping

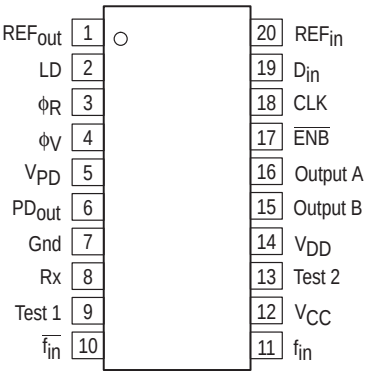


F SUFFIX
PLASTIC PACKAGE
CASE 751J
(SO–20)



DT SUFFIX
PLASTIC PACKAGE
CASE 948D
(TSSOP–20)

PIN CONNECTIONS



(Top View)

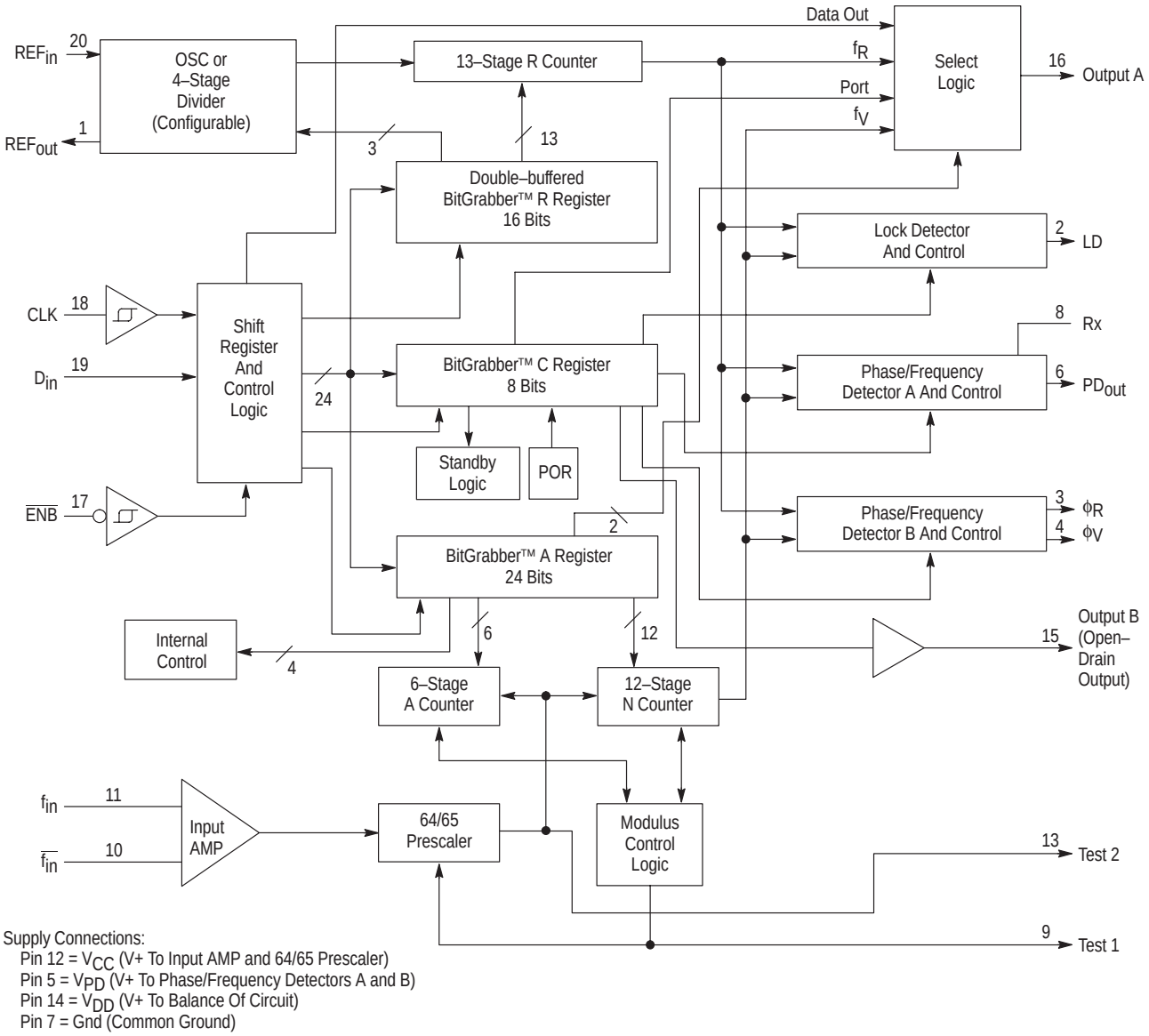
EVALUATION KIT

The MC145193EVK, which contains hardware and software, will be available.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC145193F	T_A = –40 to 85°C	SO–20
MC145193DT		TSSOP–20

BLOCK DIAGRAM



Supply Connections:
Pin 12 = V_{CC} (V+ To Input AMP and 64/65 Prescaler)
Pin 5 = V_{PD} (V+ To Phase/Frequency Detectors A and B)
Pin 14 = V_{DD} (V+ To Balance Of Circuit)
Pin 7 = Gnd (Common Ground)

Table 1. Differences in the PLL Frequency Synthesizers

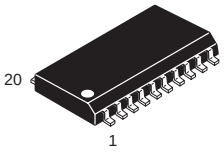
	Preferred	Not Recommended For New Designs		
Parameter	**MC145193**	**MC145192**	**MC145191**	**MC145190**
Supply Voltage, V_{DD} and V_{CC} (main supply)	2.7 to 5.5 V	2.7 to 5.0 V	4.5 to 5.5 V	4.5 to 5.5 V
Supply Voltage, V_{PD} (charge pump supply)	2.7 to 5.5 V	4.5 to 5.5 V	4.5 to 5.5 V	8.0 to 9.5 V
Supply Current	3 mA	6 mA	7 mA	7 mA
Value of External Resistor Rx, typical	3.9 kΩ for 1.7 mA [Note]	22 kΩ for 2.0 mA	18 kΩ for 2.0 mA	47 kΩ for 2.0 mA
Serial Programming with only 1 PLL (not cascaded)	Same, No Change	Same	Same	Same
Serial Prograaming with 2 or more PLLS (cascaded)	No leading dummy bits	Leading dummy bits	Leading dummy bits	Leading dummy bits

NOTE: Preliminary value.

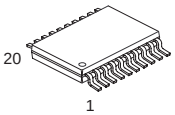
2.0 GHz PLL Frequency Synthesizer

Includes On–Board 64/65 Prescaler

MC145201



F SUFFIX
SOG PACKAGE
CASE 751J



DT SUFFIX
TSSOP
CASE 948D

ORDERING INFORMATION

MC145201F	SOG Package
MC145201DT	TSSOP

The MC145201 is a single–package synthesizer with serial interface capable of direct usage up to 2.0 GHz. A special architecture makes this PLL very easy to program because a byte–oriented format is utilized. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 3–byte serial transfer to the 24–bit A register. The interface is both SPI and MICROWIRE™ compatible.

The device features a single–ended current source/sink phase detector output and a double–ended phase detector output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single–ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

The MC145201 has phase/frequency detectors optimized for single–supply systems of 5 V ±10%.

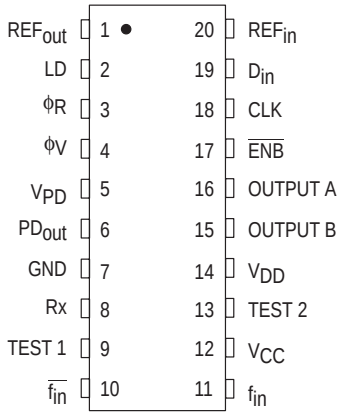
The part includes a differential RF input which may be operated in a single–ended mode. Also featured are on–board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the parts to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on–board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double–buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

- Maximum Operating Frequency: 2000 MHz @ V_{in} = 200 mV p–p
- Operating Supply Current: 12 mA Nominal
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 4.5 to 5.5 V
- Operating Supply Voltage Range of Phase Detectors (V_{PD} Pin): 4.5 to 5.5 V
- Current Source/Sink Phase Detector Output Capability: 2 mA Maximum
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: – 40 to +85°C
- R Counter Division Range: (1 and) 5 to 8191
- Dual–Modulus Capability Provides Total Division up to 262,143
- High–Speed Serial Interface: 4 Mbps
- OUTPUT A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General–Purpose Digital Outputs — OUTPUT A: Totem–Pole (Push–Pull)
  OUTPUT B: Open–Drain
- Power–Saving Standby Feature with Orderly Recovery for Minimizing Lock Times, Standby Current: 30 μA
- Evaluation Kit Available (Part Number MC145201EVK)
- See Application Note AN1253/D for Low–Pass Filter Design, and AN1277/D for Offset Reference PLLs for Fine Resolution or Fast Hopping

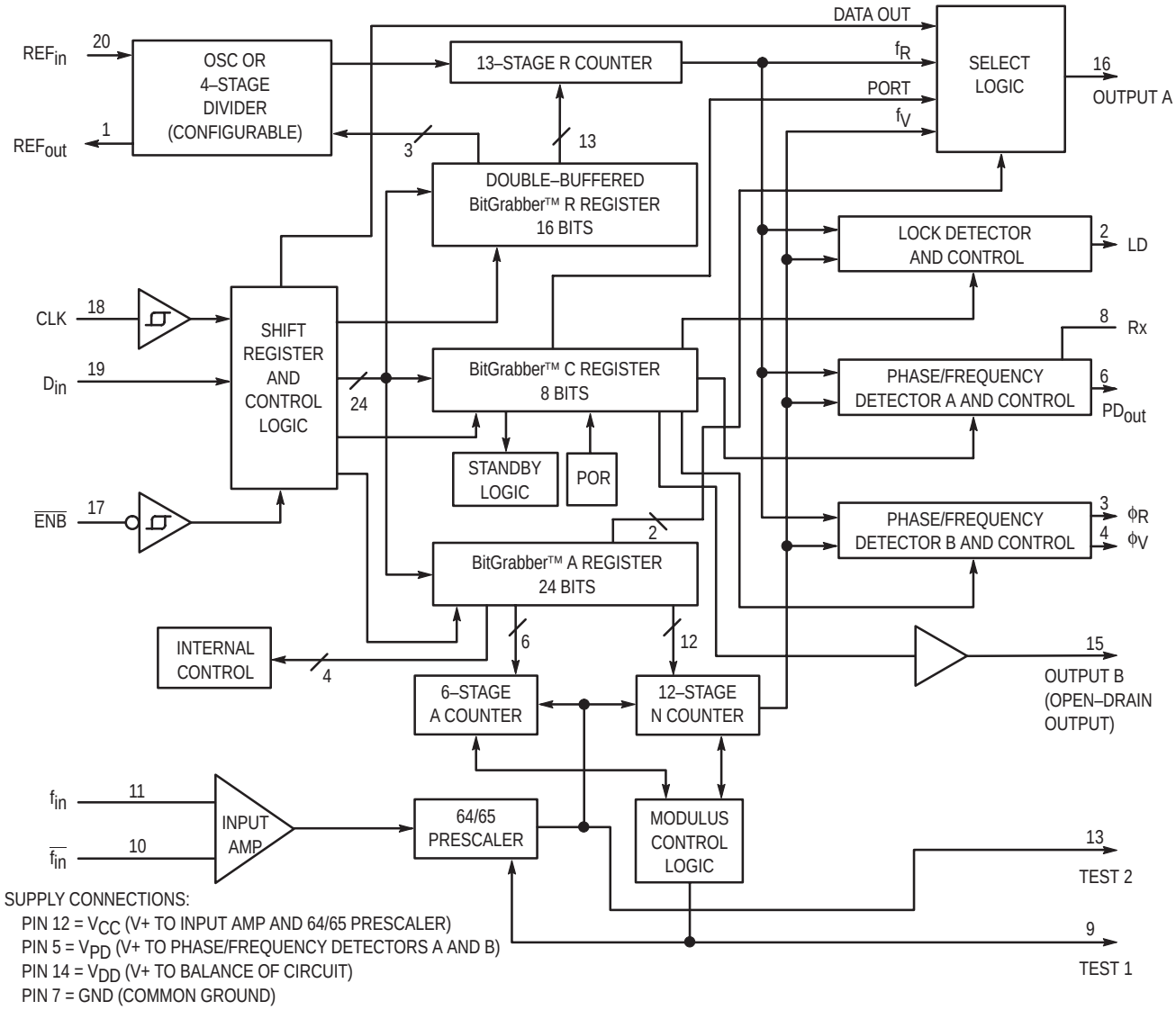
PIN ASSIGNMENT



NOT RECOMMENDED FOR NEW DESIGN
DEVICES TO BE PHASED OUT.
Consider MC145202–1 for New Designs.

REV 1
12/99

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)	–0.5 to +6.0	V
V_{PD}	DC Supply Voltage (Pin 5)	V_{DD} –0.5 to +6.0	V
V_{in}	DC Input Voltage	–0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage (except OUTPUT B, PD_{out}, ϕ_R, ϕ_V)	–0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage (OUTPUT B, PD_{out}, ϕ_R, ϕ_V)	–0.5 to V_{PD} +0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})	±10	mA
I_{out}	DC Output Current, per Pin	±20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins	±30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = 4.5 to 5.5 V, Voltages Referenced to GND, T_A = –40 to +85°C, unless otherwise stated; V_{PD} = 4.5 to 5.5 V with $V_{DD} \leq V_{PD}$.)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, DC Coupled	$0.3 \times V_{DD}$	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, DC Coupled	$0.7 \times V_{DD}$	V
V_{hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		300	mV
V_{OL}	Maximum Low–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = 20 μA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = –20 μA, Device in Reference Mode	V_{DD} – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = 0.4 V	0.36	mA
I_{OH}	Minimum High–Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = V_{DD} – 0.4 V for REF_{out}, LD V_{out} = V_{PD} – 0.4 V for ϕ_R, ϕ_V	–0.36	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT A, OUTPUT B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High–Level Output Current (OUTPUT A Only)	V_{out} = V_{DD} – 0.4 V	– 0.6	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	V_{in} = V_{DD} or GND, Device in XTAL Mode	± 1.0	μA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V_{DD} or GND, Device in Reference Mode	± 150	μA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{out} = V_{PD} – 0.5 or 0.5 V Output in High–Impedance State	± 200	nA
I_{OZ}	Maximum Output Leakage Current (OUTPUT B)	V_{out} = V_{PD} or GND, Output in High–Impedance State	± 10	μA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	V_{in} = V_{DD} or GND; Outputs Open; Device in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode; OUTPUT B Controlling V_{CC} per Figure 22	30	μA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static Low or High, Bit C4 = Low Which is ***not*** Standby, I_{Rx} = 113 μA	600	μA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is ***not*** Standby	30	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 2.0 GHz; REF_{in} = 13 MHz @ 1 V p–p; OUTPUT A = Inactive and No Connect; REF_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, $\overline{ENB}$, CLK = V_{DD} or GND, Phase Detector B Enabled (Bit C6 = Low)	*	mA

* The nominal value = 12 mA. This is not a guaranteed limit.

ANALOG CHARACTERISTICS—CURRENT SOURCE/SINK OUTPUT—PD_{out}

($I_{out} \le 2$ mA, $V_{DD} = V_{CC} = 4.5$ to 5.5 V, $V_{DD} \le V_{PD}$. Voltages Referenced to GND)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation	$V_{out} = 0.5 \times V_{PD}$	4.5	± 20	%
		5.5	± 20	
Maximum Sink–vs–Source Mismatch (Note 3)	$V_{out} = 0.5 \times V_{PD}$	4.5	12	%
		5.5	12	
Output Voltage Range (Note 3)	I_{out} variation ≤ 20%	4.5	0.5 to 4.0	V
		5.5	0.5 to 5.0	

NOTES:

1. Percentages calculated using the following formula: (Maximum Value – Minimum Value) / Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within – 40 to + 85°C.

AC INTERFACE CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, C_L = 50 pF, Input $t_r = t_f$ = 10 ns; V_{PD} = 4.5 to 5.5 V with $V_{DD} \le V_{PD}$)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w below)	1	dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to OUTPUT A (Selected as Data Out)	1, 5	105	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT A (Selected as Port)	2, 5	100	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT B	2, 6	120	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, OUTPUT A and OUTPUT B; t_{THL} only, on OUTPUT B	1, 5, 6	100	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK,		10	pF

TIMING REQUIREMENTS

(V_{DD} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	20	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{ENB}$ vs CLK	4	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$	4	*	cycles
t_w	Minimum Pulse Width, CLK	1	125	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK	1	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

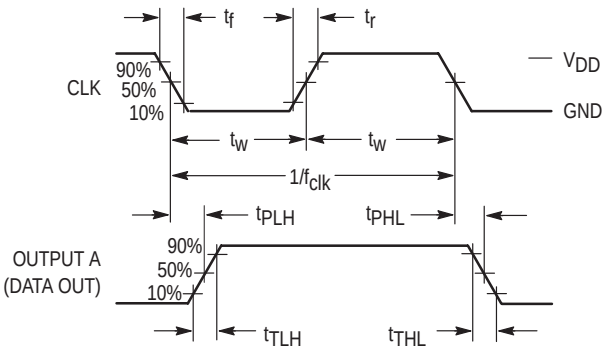


Figure 1.

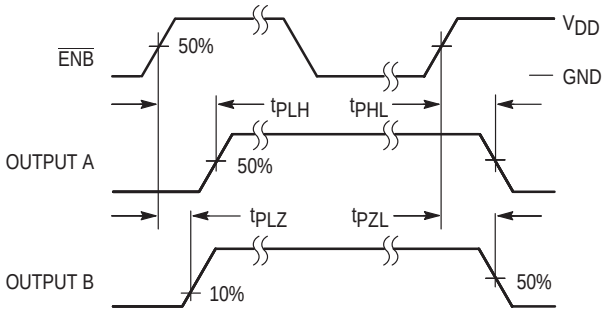


Figure 2.

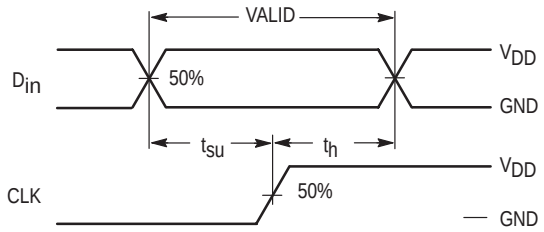


Figure 3.

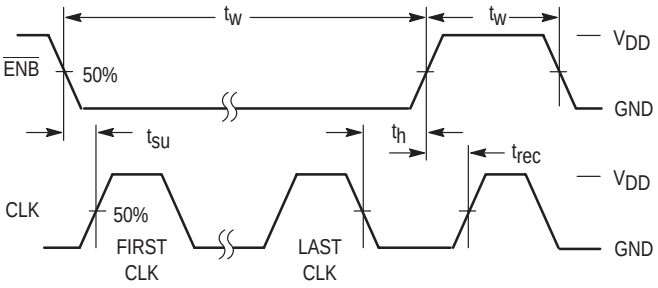
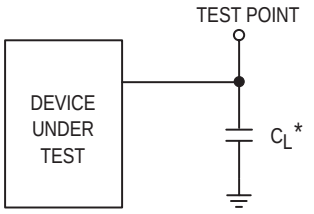
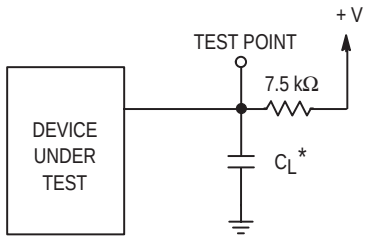


Figure 4.



*Includes all probe and fixture capacitance.

Figure 5. Test Circuit



*Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 4.5 to 5.5 V unless otherwise indicated, T_A = –40 to +85°C)

Symbol	Parameter	Test Condition	Figure No.	Guaranteed Operating Range		Unit
				Min	Max	
V_{in}	Input Voltage Range, f_{in}	500 MHz ≤ f_{in} ≤ 2000 MHz	7	200	1500	mV p–p
f_{ref}	Input Frequency, REF_{in} Externally Driven in Reference Mode	V_{in} ≥ 400 mV p–p V_{in} ≥ 1 V p–p	8	12 4.5*	27 27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance	9	2	15	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 30 pF	10, 12	dc	10	MHz
f	Operating Frequency of the Phase Detectors			dc	2	MHz
t_w	Output Pulse Width, LD, ϕ_R, and ϕ_V,	f_R in Phase with f_V, C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	17	85	ns
t_{TLH}, t_{THL}	Output Transition Times, LD, ϕ_V, and ϕ_R	C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	—	65	ns
C_{in}	Input Capacitance, REF_{in}		—	—	5	pF

*If lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal.

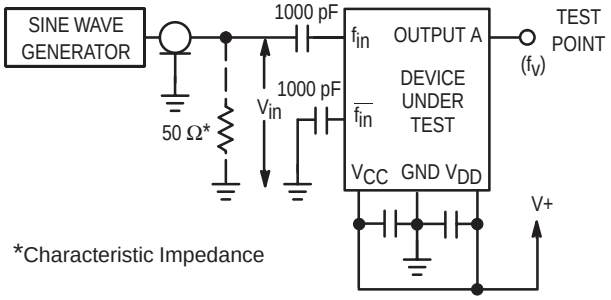


Figure 7. Test Circuit

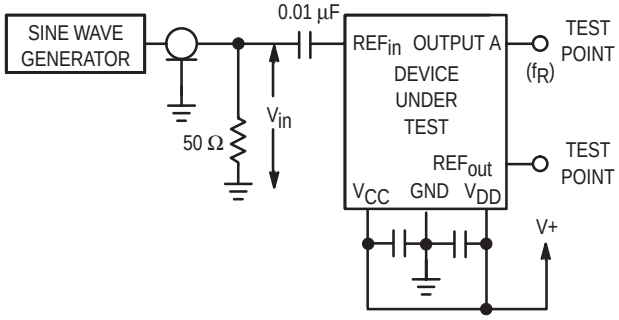


Figure 8. Test Circuit–Reference Mode

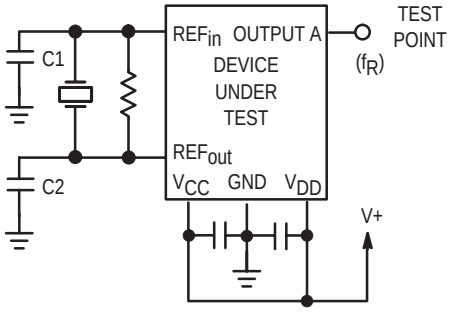


Figure 9. Test Circuit–Crystal Mode

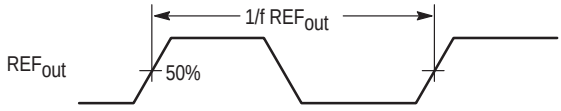


Figure 10. Switching Waveform

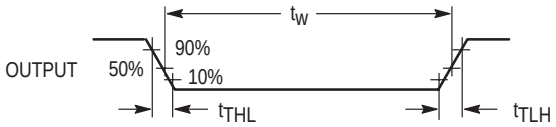


Figure 11. Switching Waveform

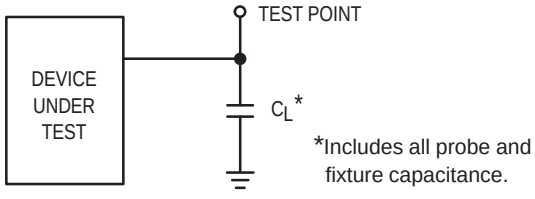
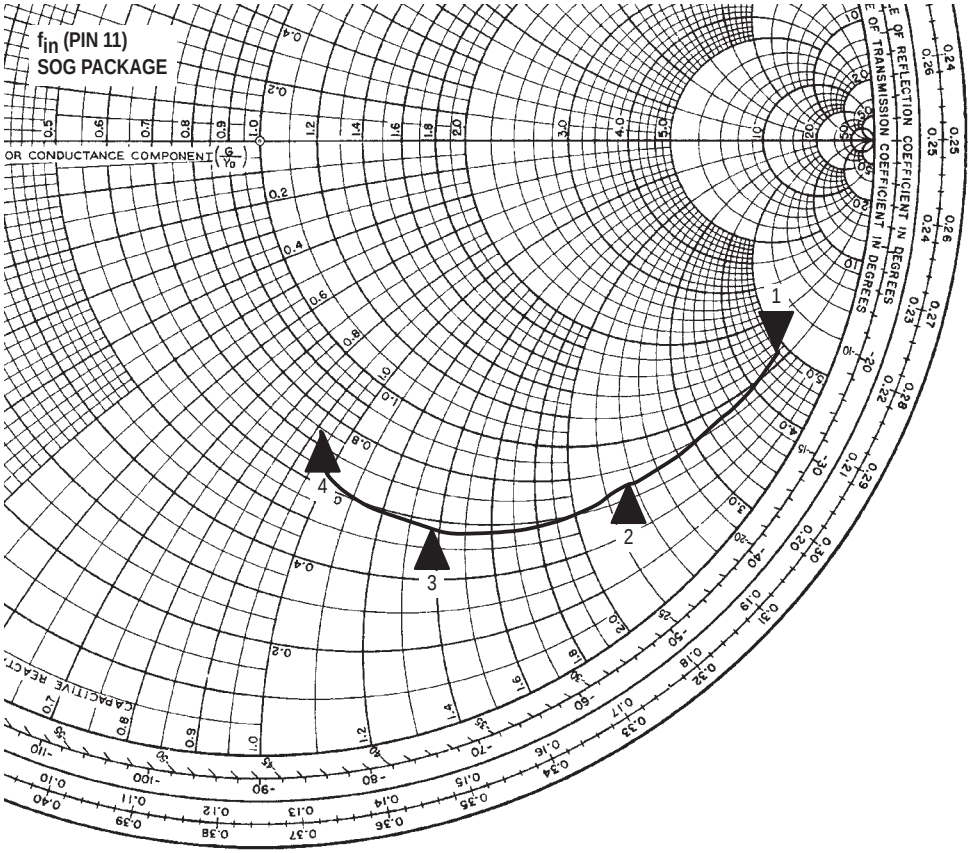


Figure 12. Test Circuit

MC145201
NORMALIZED INPUT IMPEDANCE AT f_{in} — SERIES FORMAT (R + jX)
(500 MHz to 2 GHz)



Marker	Frequency (GHz)	Resistance (Ω)	Capacitive Reactance (Ω)	Capacitance (pF)
1	0.5	59.0	– 240	1.33
2	1	34.7	– 118	1.35
3	1.5	28.3	– 68.7	1.54
4	2	37.4	– 45.7	1.74

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 19)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 1). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

CAUTION

The value programmed for the N–counter must be greater than or equal to the value of the A–counter.

The 13 least significant bits (LSBs) of the R register are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24–bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16–bit transfer may be followed by pulsing $\overline{ENB}$ low with no signal on the CLK pin. This is an alternate method of transferring data to the second buffer of the R register (see Figure 17).

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 4.5 to 5.5 V. The formats are shown in Figures 15, 16, and 17.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	See Figure 13	
Values > 32	See Figures 22–25	

CLK
Serial Data Clock Input (Pin 18)

Low–to–high transitions on CLK shift bits available at the D_{in} pin, while high–to–low transitions shift bits from OUTPUT A (when configured as Data Out, see Pin 16). The 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A register. See Table 1 and Figures 15, 16, and 17. The number of clocks required for cascaded devices is shown in Figures 24 through 26.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at GND (with $\overline{ENB}$ being a don't care) or $\overline{ENB}$ must be held at the potential of the V+ pin (with CLK being a don't care) during power–up. As an alternative, the bit sequence of Figure 13 may be used.

$\overline{ENB}$
Active Low Enable Input (Pin 17)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

For POR information, see the note for the **CLK pin**.

OUTPUT A
Configurable Digital Output (Pin 16)

OUTPUT A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 16.

If A23 = A22 = high, OUTPUT A is configured as f_R. This signal is the buffered output of the 13–stage R counter. The f_R signal appears as normally low and pulses high, and can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0 through R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of 1 (see Figure 17). The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R should not exceed 2 MHz.

If A23 = high and A22 = low, OUTPUT A is configured as f_V. This signal is the buffered output of the 12–stage N counter. The f_V signal appears as normally low and pulses high, and can be used to verify the operation of the prescaler, A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is $N \times 64 + A$. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 16. The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V should not exceed 2 MHz.

If A23 = low and A22 = high, OUTPUT A is configured as Data Out. This signal is the serial output of the 24–1/2–stage shift register. The bit stream is shifted out on the high–to–low transition of the CLK input. Upon power up, OUTPUT A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, OUTPUT A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

OUTPUT B
Open–Drain Digital Output (Pin 15)

This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, OUTPUT B assumes the high–impedance state. OUTPUT B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. **Note**: the maximum voltage allowed on the V_{PD} pin is 5.5 V for the MC145201.

Upon power–up, power–on reset circuitry forces OUTPUT B to a low level.

REFERENCE PINS

REF_{in} and REF_{out}
Reference Input and Reference Output (Pins 20 and 1)

Configurable pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 17.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The device is designed to operate with crystals up to 15 MHz; the required connections are shown in Figure 8. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary, respectively). This is the active–crystal mode shown in Figure 17. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode (shown in Figure 17) and can be engaged whether in standby or not.

In the reference mode, REF_{in} (Pin 20) accepts a signal up to 27 MHz from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 17 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 10 MHz. Therefore, for REF_{in} frequencies above 10 MHz, the one–to–one ratio may not be used. Likewise, for REF_{in} frequencies above 20 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in} and $\overline{f_{in}}$
Frequency Inputs (Pins 11 and 10)

These pins are frequency inputs from the VCO. These pins feed the on–board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they usually are used in a single–ended configuration (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out}
Single–Ended Phase/Freq. Detector Output (Pin 6)

This is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function (no dead zone). The operation of the phase/ frequency detector is described below and is shown in Figure 18.

POL bit (C7) in the C register = low (see Figure 15)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state

Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to a floating state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the floating state when the device is put into standby (STBY bit C4 = high).

The PD_{out} circuit is powered by V_{PD}. The phase detector gain is controllable by bits C3, C2, and C1: gain (in amps per radian) = PD_{out} current divided by 2π.

ϕ_R and ϕ_V (Pins 3 and 4)
Double–Ended Phase/Frequency Detector Outputs

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 18.

POL bit (C7) in the C register = low (see Figure 15)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD
Lock Detector Output (Pin 2)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V (see Figure 18).

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx
External Resistor (Pin 8)

A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Tables 2 and 3 for other values of current. To achieve a maximum current of 2 mA, the resistor should be about 18 kΩ when V_{PD} is 5.0 V. See Figure 14 if lower maximum current values are desired.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

TEST POINT PINS

TEST 1
Modulus Control Signal (Pin 9)

This pin may be used in conjunction with the Test 2 pin for access to the on–board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace.

TEST 2
Prescaler Output (Pin 13)

This pin may be used to access to the on–board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply (Pin 14)

This pin supplies power to the main CMOS digital portion of the device. The voltage range is + 4.5 to + 5.5 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC}
Positive Power Supply (Pin 12)

This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is + 4.5 to + 5.5 V with respect to the GND pin. In the standby mode, the V_{CC} pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 22.

For optimum performance, V_{CC} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

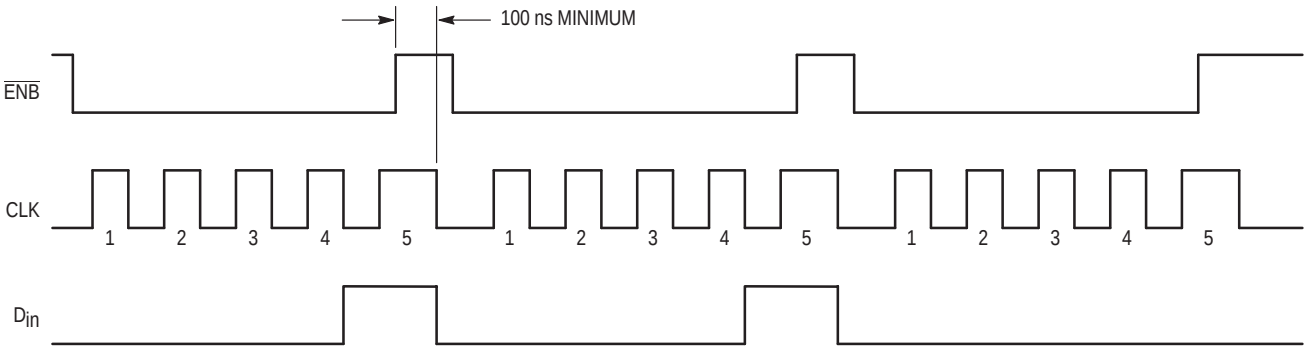
V_{PD}
Positive Power Supply (Pin 5)

This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin must be no less than the potential applied to the V_{DD} pin. The maximum voltage can be +5.5 V with respect to the GND pin.

For optimum performance, V_{PD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND
Ground (Pin 7)

Common ground.



NOTE: It may not be convenient to control the $\overline{ENB}$ or CLK pins during power up per the Pin Descriptions. If this is the case, the part may be initialized through the serial port as shown in the figure above. The sequence is similar to accessing the registers except that the CLK must remain high at least 100 ns after $\overline{ENB}$ is brought high. Note that 3 groups of 5 bits are needed.

Figure 13. Initializing the PLL through the Serial Port

MC145201
Nominal PD_{out} Spurious Current vs f_R Frequency
($1\ V < PD_{out} < V_{PD} - 1V$)

f_R (kHz)	Current (RMS nA)
10	3.6
20	4.6
50	17
100	75
200	244

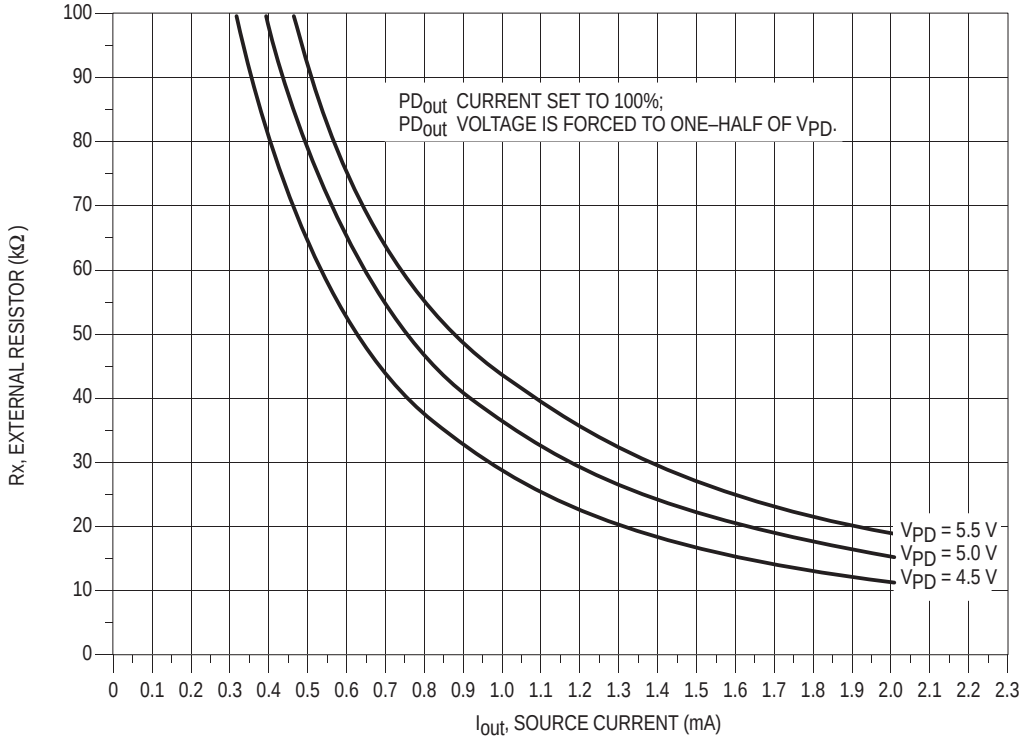
NOTE: For information on spurious current measurement see AN1253/D, "An Improved PLL Design Method Without ω_n and ζ".

Table 2. PD_{out} Current, C1 = Low with OUTPUT A *NOT* Selected as "Port"; Also, Default Mode When OUTPUT A Selected as "Port"

C3	C2	PD_{out} Current
0	0	70%
0	1	80%
1	0	90%
1	1	100%

Table 3. PD_{out} Current, C1 = High with OUTPUT A *NOT* Selected as "Port"

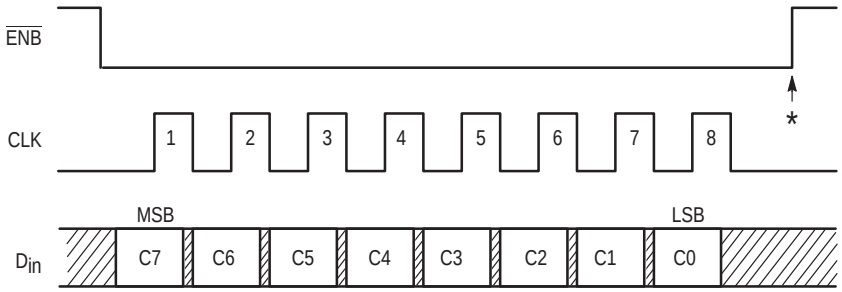
C3	C2	PD_{out} Current
0	0	25%
0	1	50%
1	0	75%
1	1	100%



Nominal MC145201 PD_{out} Source Current vs Rx Resistance

NOTE: The MC145201 is optimized for Rx values in the 18 kΩ to 40 kΩ range. For example, to achieve 0.3 mA of output current, it is preferable to use a 30–kΩ resistor for Rx and bit settings for 25% (as shown in Table 3).

Figure 14.



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts the polarity of PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 18. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output (LD) when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 — STBY: When set high, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high–impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.

When C4 is reset low, the part is taken out of standby in 2 steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C3, C2 — I2, I1: Controls the PD_{out} source/sink current per Tables 2 and 3. With both bits high, the maximum current (as set by Rx per Figure 14) is available. Also, see C1 bit description.

C1 — Port: When the OUTPUT A pin is selected as “Port” via bits A22 and A23, C1 determines the state of OUTPUT A. When C1 is set high, OUTPUT A is forced high; C1 low forces OUTPUT A low. When OUTPUT A is NOT selected as “Port,” C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 2 and 3.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when OUTPUT A is selected as “Port.” The Port bit is not affected by the standby mode.

C0 — Out B: Determines the state of OUTPUT B. When C0 is set high, OUTPUT B is high–impedance; C0 low forces OUTPUT B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 15. C Register Access and Format (8 Clock Cycles are Used)

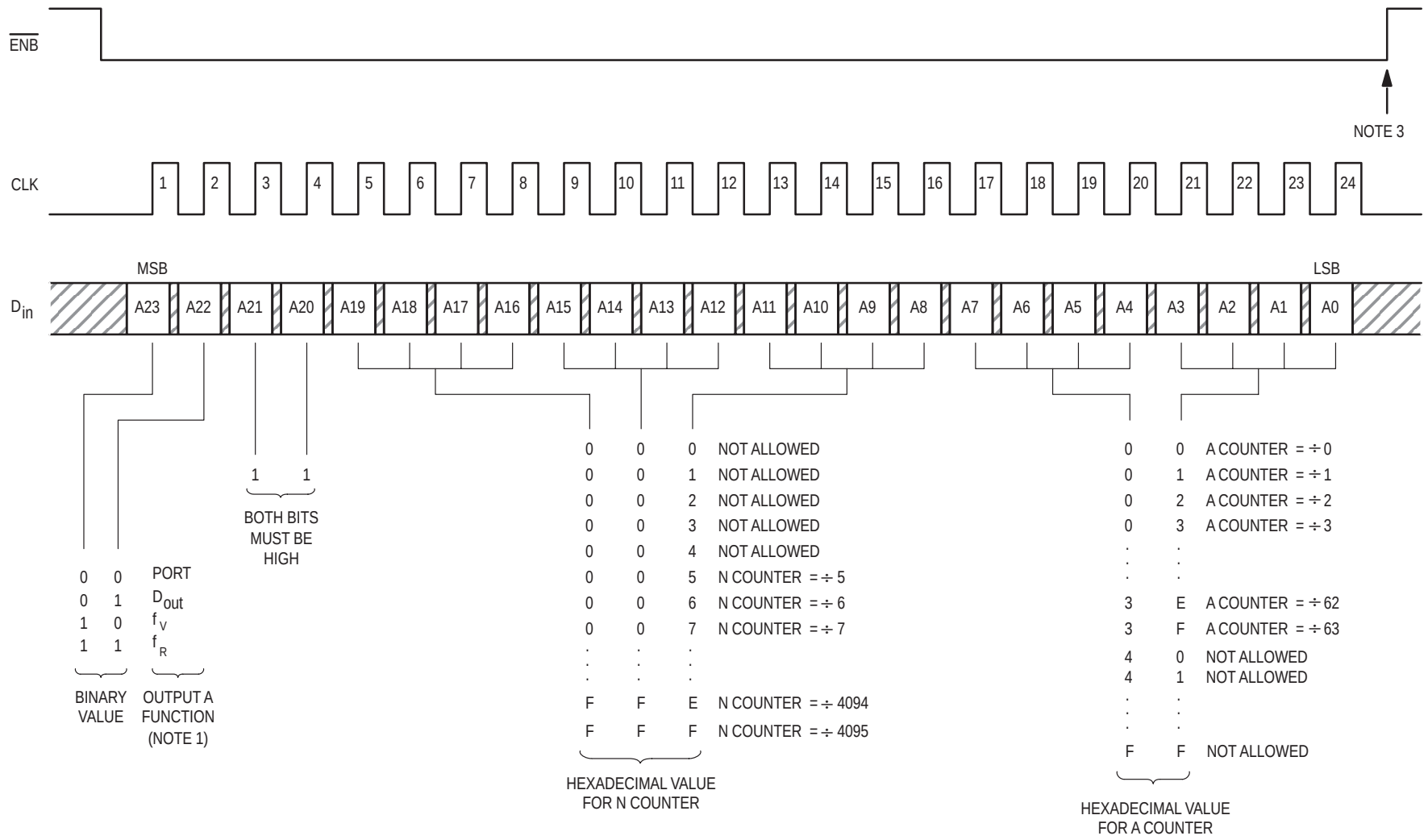
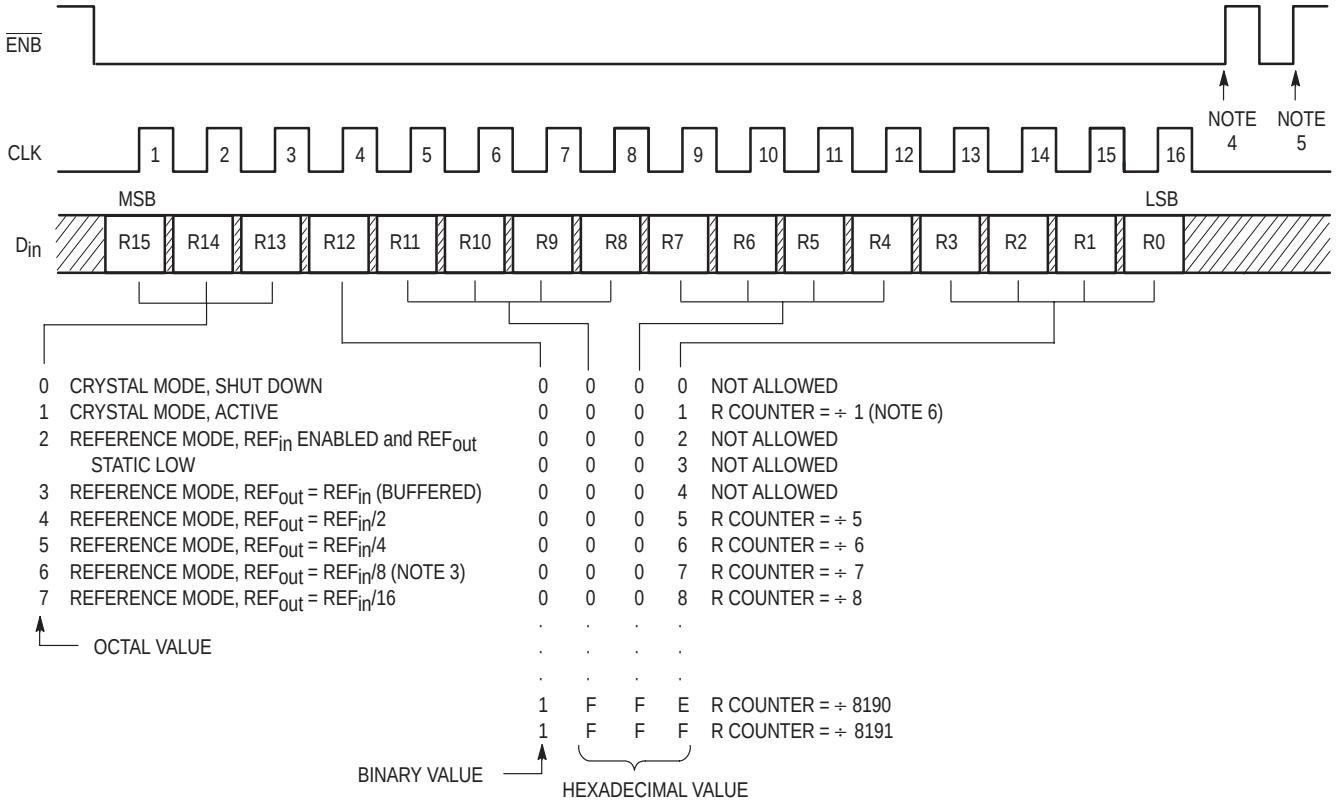


Figure 16. A Register Access and Format (24 Clock Cycles are Used)

NOTES:

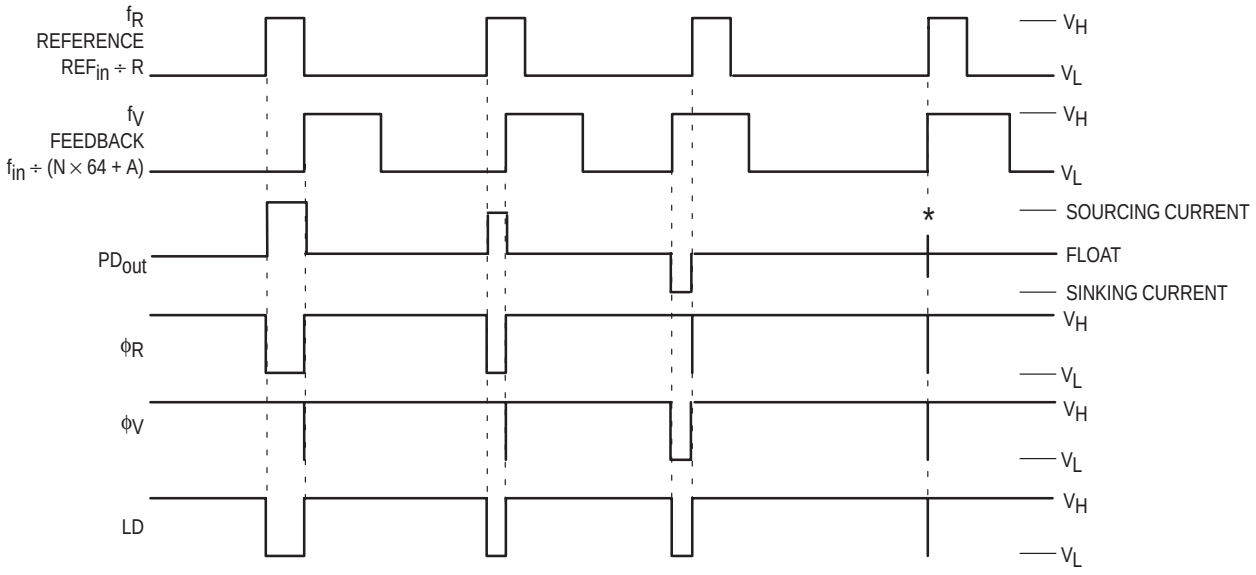
1. A power-on initialize circuit forces the OUTPUT A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.



NOTES:

1. Bits R15 through R13 control the configurable “OSC or 4–stage divider” block (see Block Diagram).
2. Bits R12 through R0 control the “13–stage R counter” block (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the “OSC or 4–Stage Divider” block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. At this point, bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. Also, see note 3 of Figure 16 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 17. R Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.

NOTE: The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.

Figure 18. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in} (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 19.

The crystal should be specified for a loading capacitance (C_L) which does not exceed approximately 20 pF when used at the highest operating frequency of 15 MHz. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 20)
C_{out} = 6 pF (see Figure 20)
C_a = 1 pF (see Figure 20)

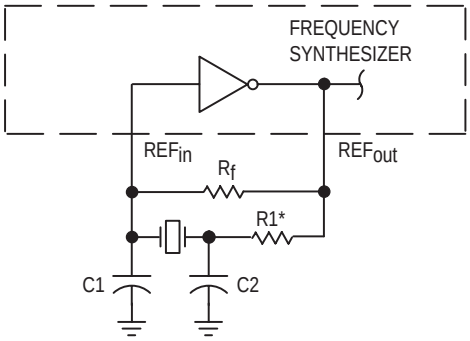
C1 and C2 = external capacitors (see Figure 19)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 21. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 19 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency (f_R) at OUTPUT A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 4).



* May be needed in certain cases. See text.

Figure 19. Pierce Crystal Oscillator Circuit

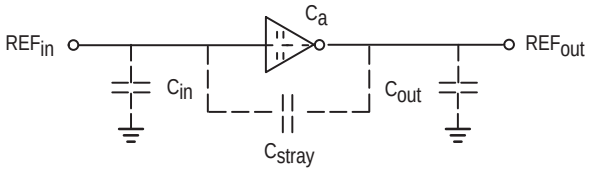
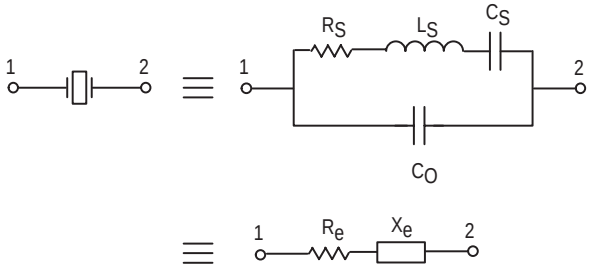


Figure 20. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 21. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, “The Piezoelectric Crystal Unit–Definitions and Method of Measurement”, *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, “Quartz Crystals for Frequency Control”, *Electro–Technology*, June 1969.

P. J. Ottowitz, “A Guide to Crystal Selection”, *Electronic Design*, May 1966.

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D. Babin, “Guidelines for Crystal Oscillator Design”, *Machine Design*, April 25, 1985.

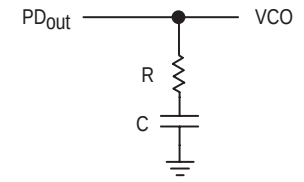
Table 4. Partial List of Crystal Manufacturers

United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

(A)



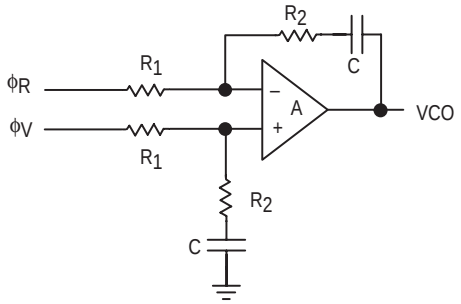
$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:
For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:
For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

* The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:
N = Total Division Ratio in Feedback Loop
K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}
K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

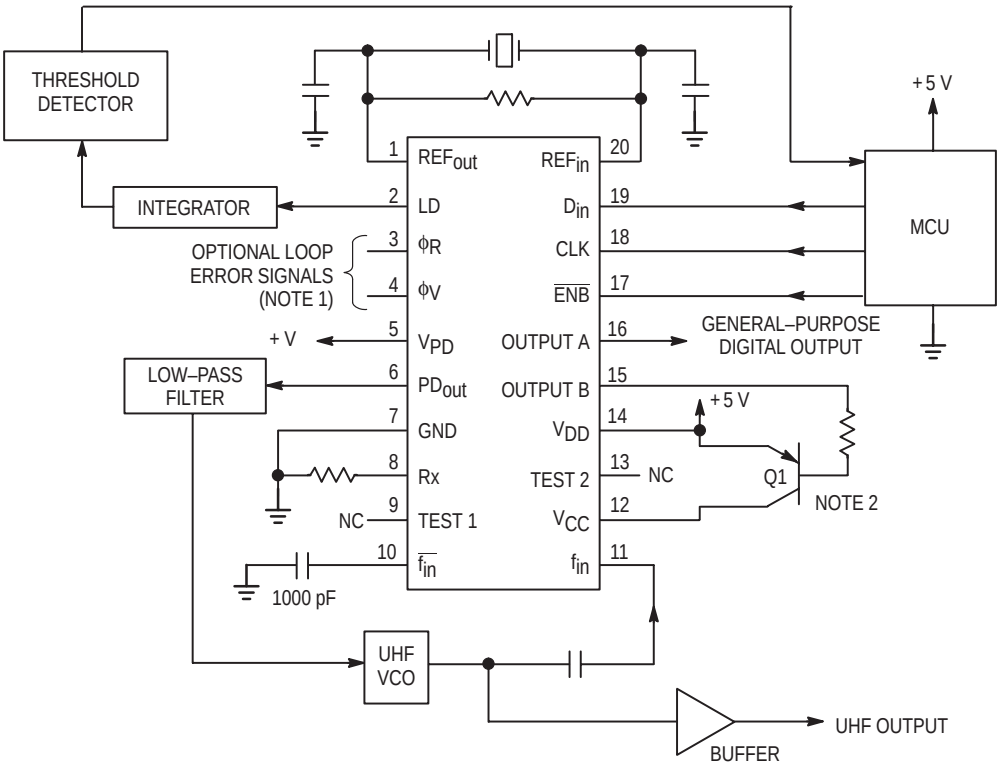
K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

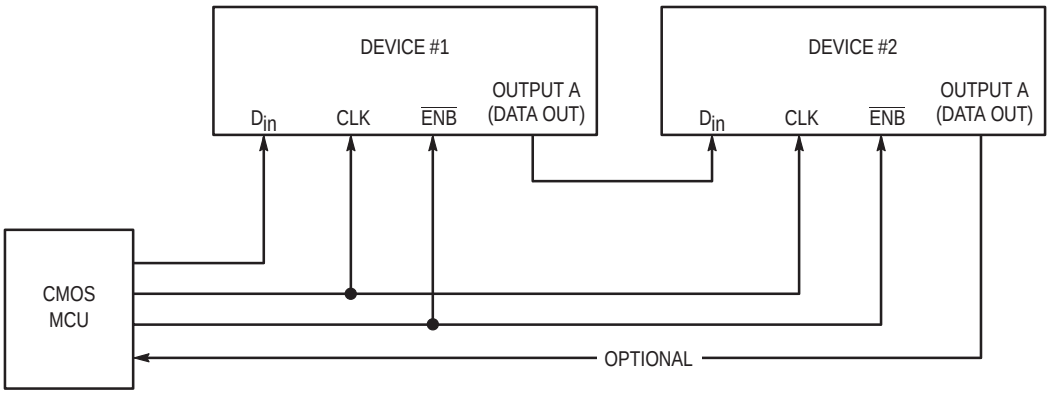
Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.
AN1253/D, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general–purpose digital pin, OUTPUT B. If the standby feature is not needed, tie Pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low–inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

Figure 22. Example Application



NOTE: See related Figures 24 through 26; these bit streams apply to the MC145191 and MC145201.

Figure 23. Cascading Two Devices

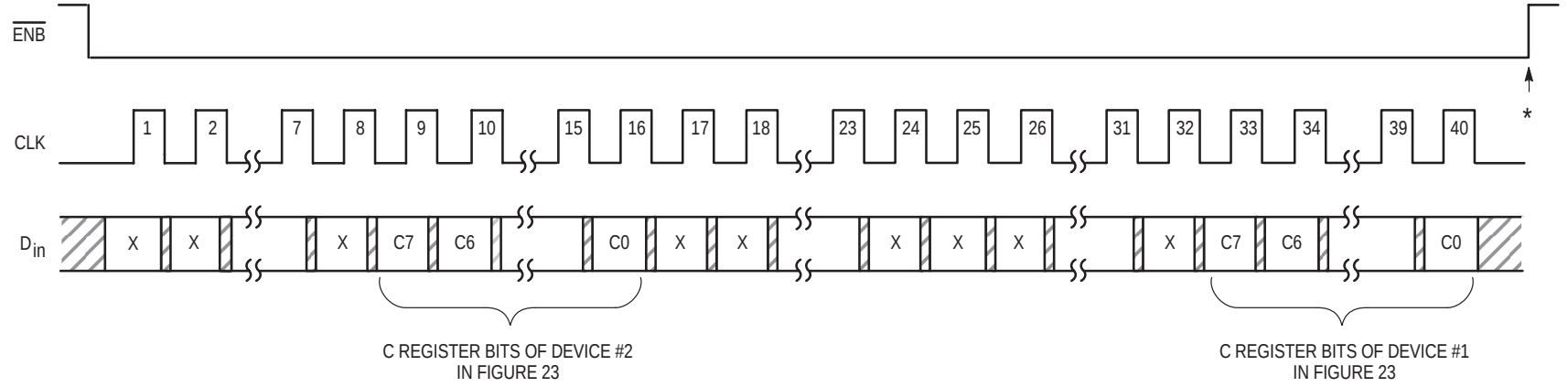


Figure 24. Accessing the C Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the C registers of both devices and stored. No other registers are affected.

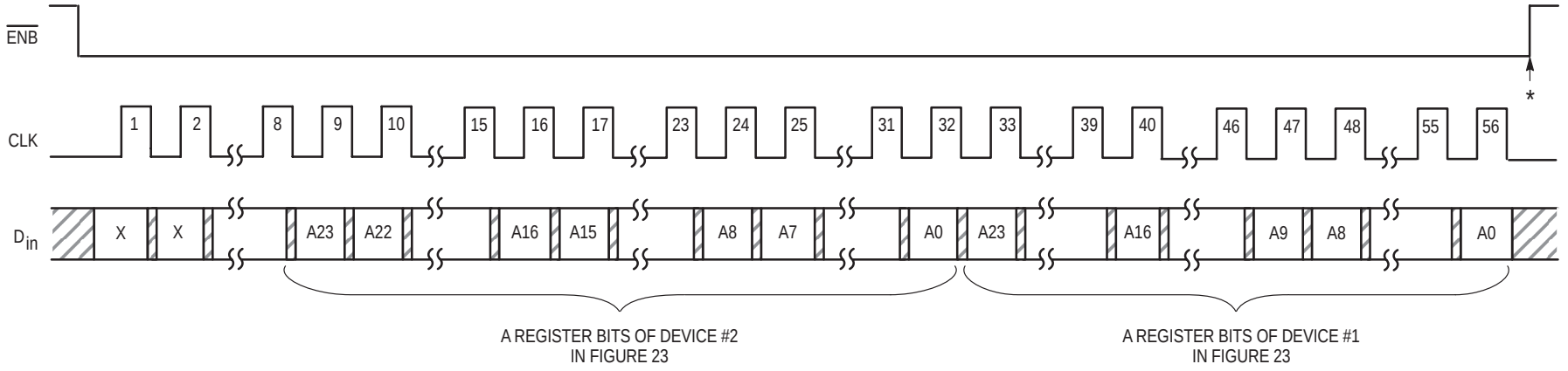


Figure 25. Accessing the A Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

Figure 26. Accessing the R Registers of Two Cascaded Devices

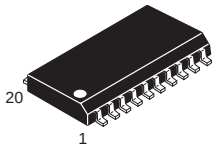
NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14, and R15 are stored and sent to the “OSC or 4-Stage Divider” block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double-buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. At this point, the bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{\text{ENB}}$ pulse, as shown. Also, see note of Figure 25 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

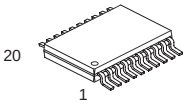
Low-Voltage 2.0 GHz PLL Frequency Synthesizer

Includes On–Board 64/65 Prescaler

MC145202



F SUFFIX
SOG PACKAGE
CASE 751J



DT SUFFIX
TSSOP
CASE 948D

ORDERING INFORMATION

MC145202F	SOG Package
MC145202DT	TSSOP

The MC145202 is a low–voltage single–package synthesizer with serial interface capable of direct usage up to 2.0 GHz.

The counters are programmed via a synchronous serial port which is SPI compatible. The serial port is byte-oriented to facilitate control via an MCU. Due to the innovative BitGrabber Plus™ registers, the MC145202 may be cascaded with other peripherals featuring BitGrabber Plus without requiring leading dummy bits or address bits in the serial data stream. In addition, BitGrabber Plus peripherals may be cascaded with existing BitGrabber™ peripherals.

The device features a single–ended current source/sink phase detector A output and a double–ended phase detector B output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single–ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

Slew–rate control is provided by a special driver designed for the REF_{out} pin. This minimizes interference caused by REF_{out}.

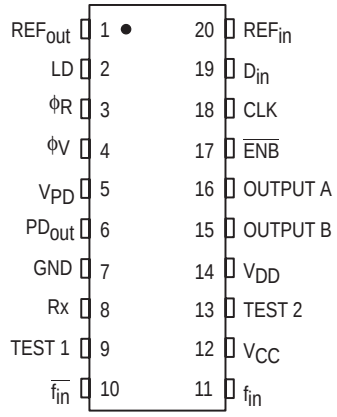
This part includes a differential RF input that may be operated in a single–ended mode. Also featured are on–board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on–board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double–buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

- Maximum Operating Frequency: 2000 MHz @ – 10 dBm
- Operating Supply Current: 4 mA Nominal at 3.0 V
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 2.7 to 5.5 V
- Operating Supply Voltage Range of Phase Detectors (V_{PD} Pin): 2.7 to 5.5 V
- Current Source/Sink Phase Detector Output Capability: 1.7 mA @ 5.0 V
  1.0 mA @ 3.0 V
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: – 40 to + 85°C
- R Counter Division Range: 1 and 5 to 8191
- Dual–Modulus Capability Provides Total Division up to 262,143
- High–Speed Serial Interface: 4 Mbps
- OUTPUT A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General–Purpose Digital Outputs — OUTPUT A: Totem–Pole (Push–Pull) with Four Output Modes
  OUTPUT B: Open–Drain
- Patented Power–Saving Standby Feature with Orderly Recovery for Minimizing Lock Times, Standby Current: 30 μA

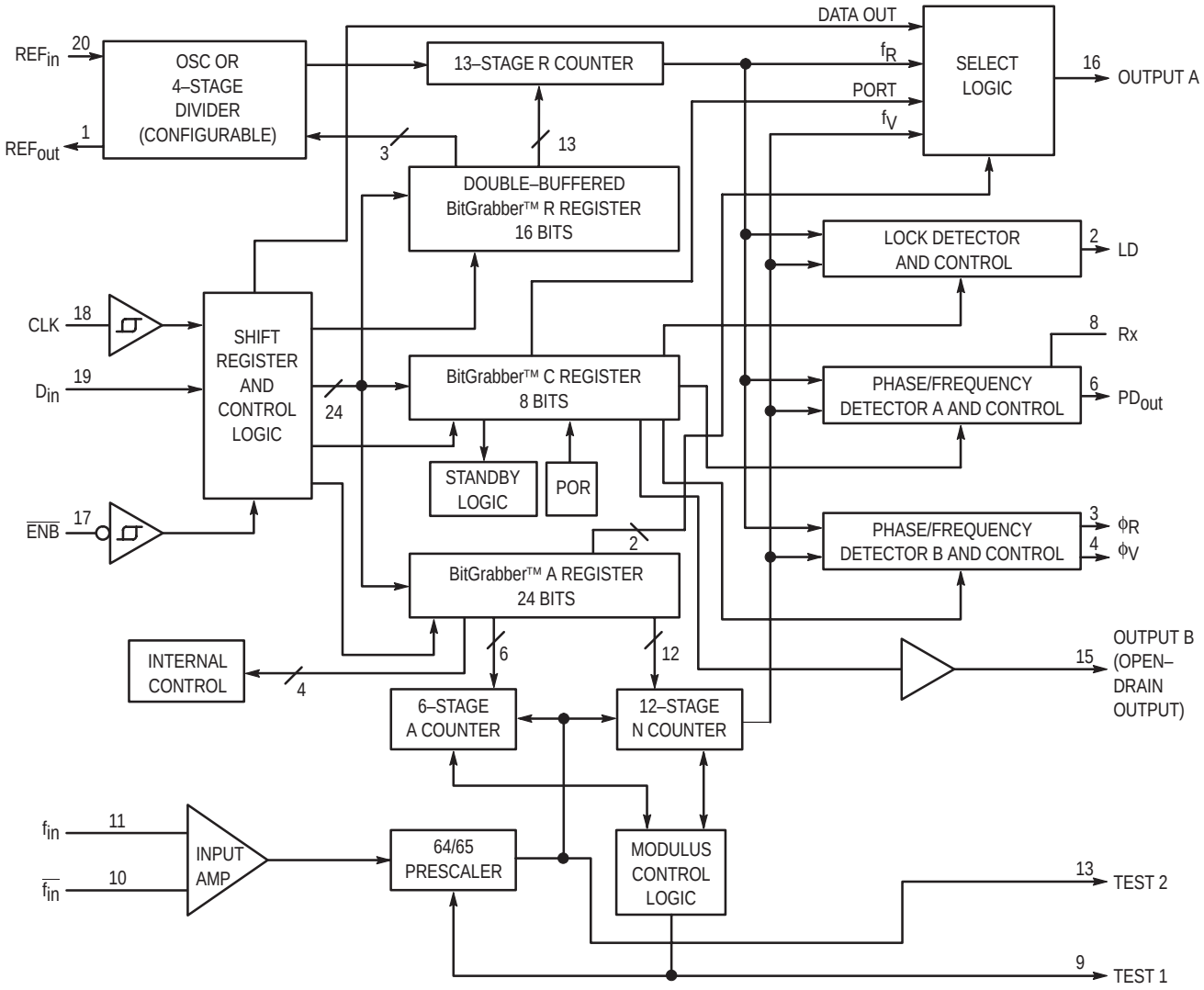
PIN ASSIGNMENT



NOT RECOMMENDED FOR NEW DESIGN
DEVICES TO BE PHASED OUT.
Consider MC145202–1 for New Designs.

REV 4
12/99

BLOCK DIAGRAM



SUPPLY CONNECTIONS:

PIN 12 = V_{CC} (V+ TO INPUT AMP AND 64/65 PRESCALER)

PIN 5 = V_{PD} (V+ TO PHASE/FREQUENCY DETECTORS A AND B)

PIN 14 = V_{DD} (V+ TO BALANCE OF CIRCUIT)

PIN 7 = GND (COMMON GROUND)

MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)	– 0.5 to + 6.0	V
V_{PD}	DC Supply Voltage (Pin 5)	V_{DD} – 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage (except OUTPUT B, PD_{out}, ϕ_R, ϕ_V)	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage (OUTPUT B, PD_{out}, ϕ_R, ϕ_V)	– 0.5 to V_{PD} + 0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = 2.7 to 5.5 V, Voltages Referenced to GND, unless otherwise stated; V_{PD} = 2.7 to 5.5 V, T_A = – 40 to 85°C)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$)		0.3 x V_{DD}	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$)		0.7 x V_{DD}	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)	V_{DD} = 2.7 V V_{DD} = 4.5 V	100 250	mV
V_{OL}	Maximum Low–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = 20 μA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = – 20 μA, Device in Reference Mode	V_{DD} – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out}, LD)	V_{out} = 0.3 V	0.36	mA
I_{OL}	Minimum Low–Level Output Current (ϕ_R, ϕ_V)	V_{out} = 0.3 V	0.36	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT A)	V_{out} = 0.4 V V_{DD} = 4.5 V	1.0	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High–Level Output Current (REF_{out}, LD)	V_{out} = V_{DD} – 0.3 V	– 0.36	mA
I_{OH}	Minimum High–Level Output Current (ϕ_R, ϕ_V)	V_{out} = V_{PD} – 0.3 V	– 0.36	mA
I_{OH}	Minimum High–Level Output Current (OUTPUT A Only)	V_{out} = V_{DD} – 0.4 V V_{DD} = 4.5 V	– 0.6	mA

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	V_{in} = V_{DD} or GND, Device in XTAL Mode	± 1.0	μA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V_{DD} or GND, Device in Reference Mode	± 100	μA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{out} = V_{PD} or GND, Output in Floating State	± 130	nA
	(OUTPUT B)	V_{out} = V_{PD} or GND, Output in High–Impedance State	± 1	μA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	V_{in} = V_{DD} or GND; Outputs Open; Device in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode; OUTPUT B Controlling V_{CC} per Figure 21	30	μA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static State, Bit C4 = Low Which is ***not*** Standby, I_{Rx} = 170 μA, V_{PD} = 5.5 V	750	μA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is ***not*** Standby	30	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 2.0 GHz; REF_{in} = 13 MHz @ 1 Vp–p; OUTPUT A = Inactive and No Connect; V_{DD} = V_{CC}, REF_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, $\overline{ENB}$, CLK = V_{DD} or GND, Phase Detector B Selected (Bit C6 = Low)	*	mA

* The nominal values are:
4 mA at V_{DD} = 3.0 V and V_{PD} = 3.0 V
6 mA at V_{DD} = 5.0 V and V_{PD} = 5.0 V
These are not guaranteed limits.

ANALOG CHARACTERISTICS — CURRENT SOURCE/SINK OUTPUT — PD_{out}

(I_{out} ≤ 1 mA @ V_{DD} = 2.7 V and I_{out} ≤ 1.7mA @ V_{DD} ≥ 4.5 V, V_{DD} = V_{CC} = 2.7 to 5.5 V, Voltages Referenced to GND)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation (Part–to–Part)	V_{out} = 0.5 x V_{PD}	2.7	± 15	%
		4.5	± 15	
		5.5	± 15	
Maximum Sink–vs–Source Mismatch (Note 3)	V_{out} = 0.5 x V_{PD}	2.7	11	%
		4.5	11	
		5.5	11	
Output Voltage Range (Note 3)	I_{out} Variation ≤ 15%	2.7	0.5 to 2.2	V
	I_{out} Variation ≤ 20%	4.5	0.5 to 3.7	
	I_{out} Variation ≤ 22%	5.5	0.5 to 4.7	

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within – 40 to + 85°C.

AC INTERFACE CHARACTERISTICS

(V_{DD} = V_{CC} = 2.7 to 5.5 V, T_A = – 40 to + 85°C, C_L = 25 pF, Input t_r = t_f = 10 ns; V_{PD} = 2.7 to 5.5 V)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w below)	1	dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to OUTPUT A (Selected as Data Out)	1, 5	100	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT A (Selected as Port)	2, 5	150	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT B	2, 6	150	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, OUTPUT A and OUTPUT B; t_{THL}only, on OUTPUT B	1, 5, 6	50	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK		10	pF

TIMING REQUIREMENTS

(V_{DD} = V_{CC} = 2.7 to 5.5 V, T_A = – 40 to + 85°C, Input t_r = t_f = 10 ns, unless otherwise indicated)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	50	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{ENB}$ vs CLK	4	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$	4	*	cycles
t_w	Minimum Pulse Width, CLK	1	125	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK	1	100	μs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

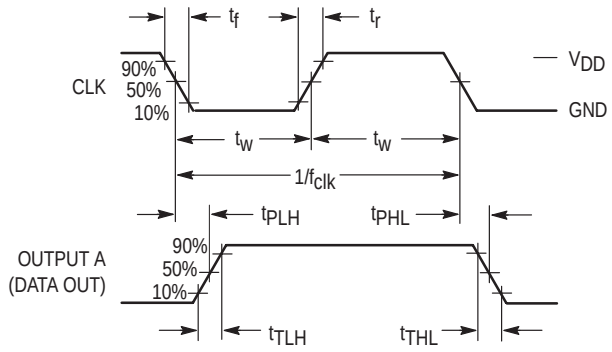


Figure 1.

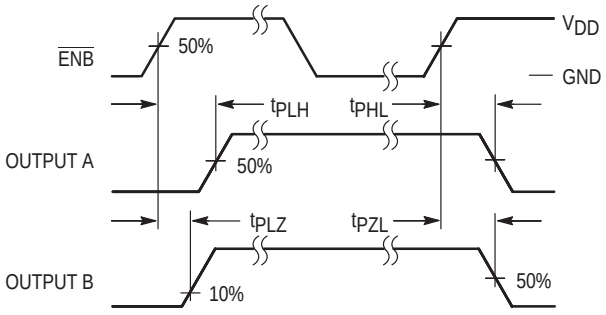


Figure 2.

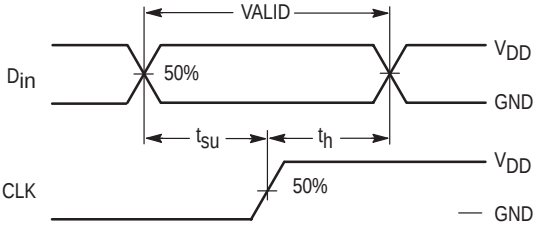


Figure 3.

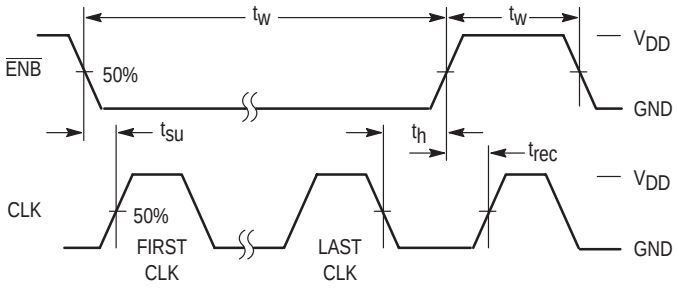
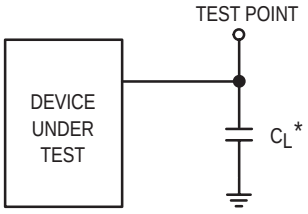
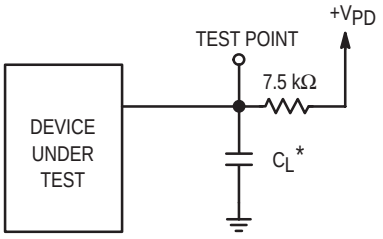


Figure 4.



* Includes all probe and fixture capacitance.

Figure 5.



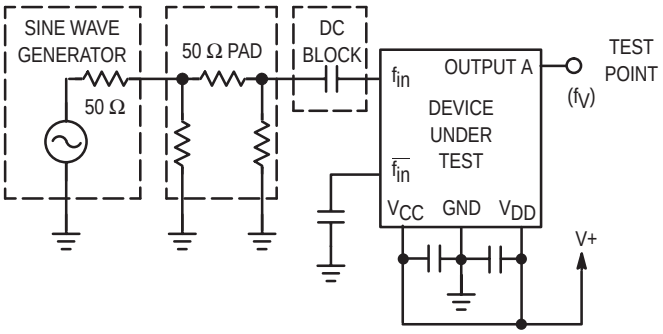
* Includes all probe and fixture capacitance.

Figure 6.

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 2.7 to 5.5 V unless otherwise indicated, T_A = – 40 to + 85°C)

Symbol	Parameter	Test Condition	Fig. No.	Guaranteed Operating Range		Unit
				Min	Max	
P_{in}	Input Sensitivity Range, f_{in}	500 MHz ≤ f_{in} ≤ 2000 MHz	7	– 10	4	dBm*
f_{ref}	Input Frequency, REF_{in} Externally Driven in Reference Mode	V_{in} ≥ 400 mV p–p 2.7 ≤ V_{DD} < 4.5 V 4.5 ≤ V_{DD} ≤ 5.5 V	8	1.5 1.5	20 30	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance	9	2	15	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 20 pF, V_{out} ≥ 1 V p–p	10, 12	dc	10	MHz
f	Operating Frequency of the Phase Detectors			dc	2	MHz
t_w	Output Pulse Width (ϕ_R, ϕ_V, and LD)	f_R in Phase with f_V, C_L = 20 pF, ϕ_R and ϕ_V active for LD measurement, ** V_{PD} = 2.7 to 5.5 V V_{DD} = 2.7 V V_{DD} = 4.5 V V_{DD} = 5.5 V	11, 12	 40 18 14	 120 60 50	ns
t_{TLH}, t_{THL}	Output Transition Times (LD, ϕ_V, and ϕ_R)	C_L = 20 pF, V_{PD} = 2.7 V, V_{DD} = V_{CC} = 2.7 V	11, 12	—	80	ns
C_{in}	Input Capacitance, REF_{in}			—	7	pF

* Power level at the input to the dc block.
** When PD_{out} is active, LD minimum pulse width is approximately 5 ns.



NOTE: Alternately, the 50 Ω pad may be a T network.

Figure 7. Test Circuit

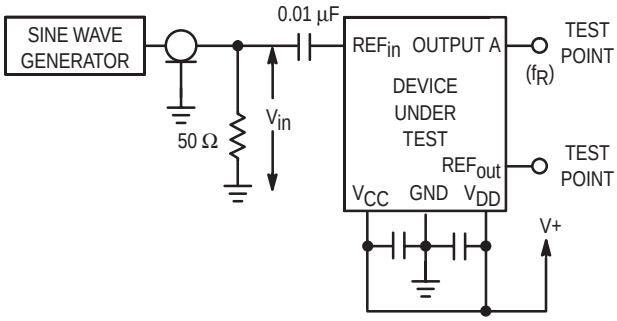


Figure 8. Test Circuit — Reference Mode

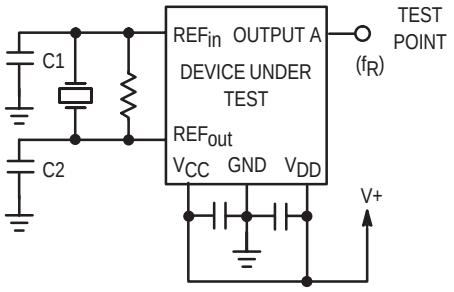


Figure 9. Test Circuit — Crystal Mode

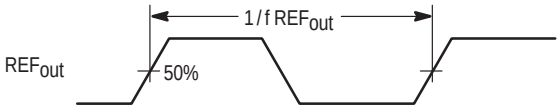


Figure 10. Switching Waveform

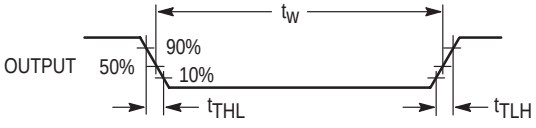


Figure 11. Switching Waveform

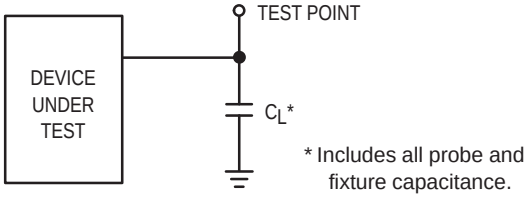


Figure 12. Test Circuit

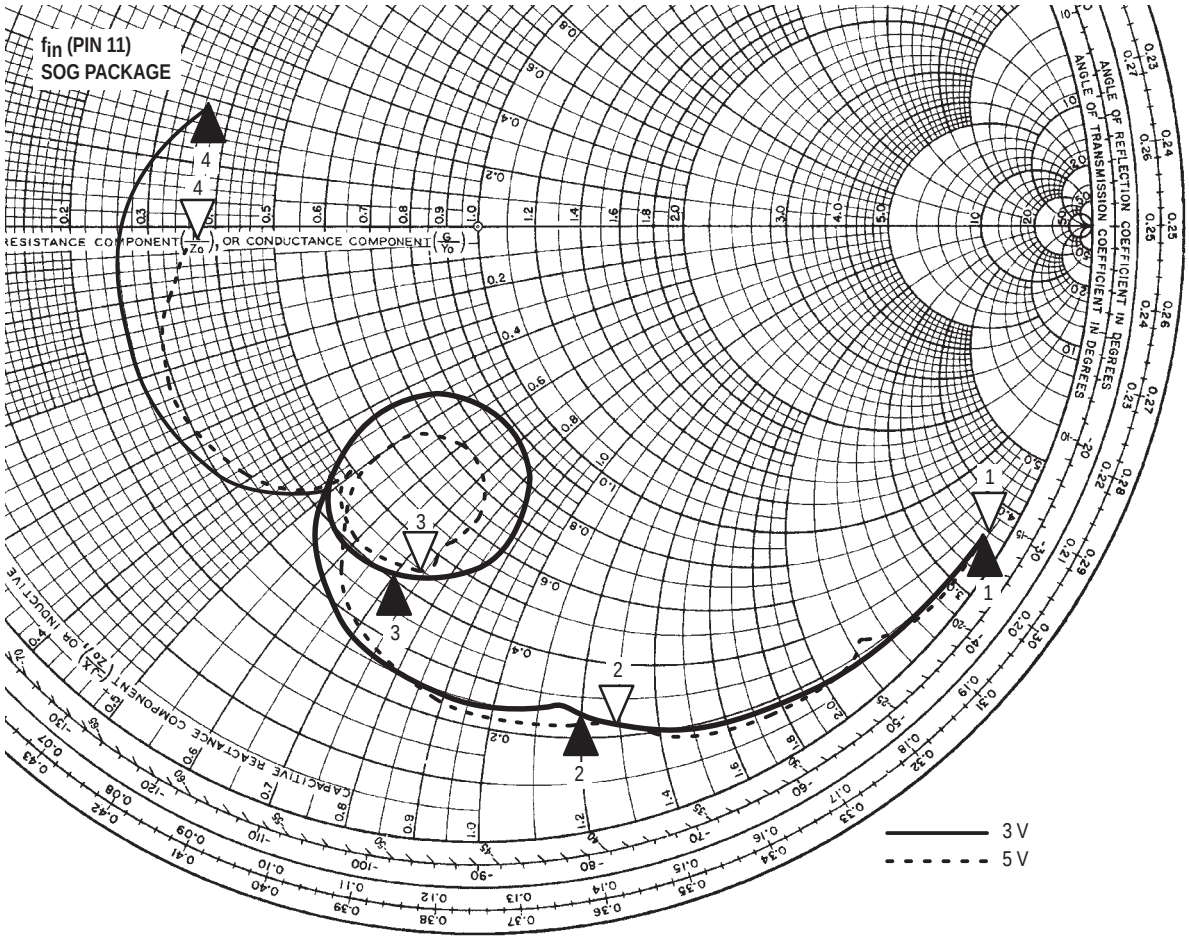


Figure 13. Normalized Input Impedance at f_{in} — Series Format (R + jx)

Table 1. Input Impedence at f_{in} — Series Format (R + jx), V_{CC} = 3 V

Marker	Frequency (GHz)	Resistance (Ω)	Reactance (Ω)	Capacitance/ Inductance
1	0.5	11.4	– 168	1.9 pF
2	1	12.4	– 59.4	2.68 pF
3	1.5	19.8	– 34.9	3.04 pF
4	2	18.1	9.43	751 pH

Table 2. Input Impedence at f_{in} — Series Format (R + jx), V_{CC} = 5 V

Marker	Frequency (GHz)	Resistance (Ω)	Reactance (Ω)	Capacitance/ Inductance
1	0.5	11.8	–175	1.82 pF
2	1	11.5	– 64.4	2.47 pF
3	1.5	22.2	– 36.5	2.91 pF
4	2	18.4	1.14	90.4 pH

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 19)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 3). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

CAUTION

The value programmed for the N counter must be greater than or equal to the value of the A counter.

The 13 least significant bits (LSBs) of the R register are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24–bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16–bit transfer may be followed by pulsing $\overline{ENB}$ low with no signal on the CLK pin. This is an alternate method of transferring data to the second buffer of the R register (see Figure 16).

The bit stream needs neither address nor steering bits due to the innovative BitGrabber Plus registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 14, 15, and 16.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 3. Register Access
(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	Not Allowed	
Values > 32	See Figures 22 – 25	

CLK
Serial Data Clock Input (Pin 18)

Low–to–high transitions on CLK shift bits available at the D_{in} pin, while high–to–low transitions shift bits from OUTPUT A (when configured as Data Out, see Pin 16). The 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A register. See Table 3 and Figures 14, 15, and 16. The number of clocks required for cascaded devices is shown in Figures 23 through 25.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at GND (with $\overline{ENB}$ being a don't care) or $\overline{ENB}$ must be held at the potential of the V+ pin (with CLK being a don't care) during power–up. Floating, toggling, or having these pins in the wrong state during power–up does not harm the chip, but causes two potentially undesirable effects. First, the outputs of the device power up in an unknown state. Second, if two devices are cascaded, the A Registers must be written twice after power up. After these two accesses, the two cascaded chips perform normally.

$\overline{ENB}$
Active Low Enable Input (Pin 17)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 3.

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

For POR information, see the note for the **CLK pin**.

OUTPUT A
Configurable Digital Output (Pin 16)

OUTPUT A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 15.

If A23 = A22 = high, OUTPUT A is configured as f_R. This signal is the buffered output of the 13–stage R counter. The f_R signal appears as normally low and pulses high. The f_R signal can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0–R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of 1 (see Figure 16). The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R should not exceed 2 MHz.

If A23 = high and A22 = low, OUTPUT A is configured as f_V. This signal is the buffered output of the 12–stage N counter. The f_V signal appears as normally low and pulses high. The f_V signal can be used to verify the operation of the prescaler, A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is $N \times 64 + A$. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 15. The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V should not exceed 2 MHz.

If A23 = low and A22 = high, OUTPUT A is configured as Data Out. This signal is the serial output of the 24–1/2–stage shift register. The bit stream is shifted out on the high–to–low transition of the CLK input. Upon power up, OUTPUT A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, OUTPUT A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

OUTPUT B
Open–Drain Digital Output (Pin 15)

This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, OUTPUT B assumes the high–impedance state. OUTPUT B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. **Note**: the maximum voltage allowed on the V_{PD} pin is 5.5 V.

Upon power–up, power–on reset circuitry forces OUTPUT B to a low level.

REFERENCE PINS

REF_{in} and REF_{out}
Reference Input and Reference Output (Pins 20 and 1)

Configurable pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 16.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values, as recommended by the crystal supplier, are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the components are shown in Figure 9.

To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary, respectively). This is the active–crystal mode shown in Figure 16. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode (shown in Figure 16) and can be engaged whether in standby or not.

In the reference mode, REF_{in} (Pin 20) accepts a signal from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 16 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is listed in the Loop Specifications table for an output swing of 1 V p–p and 20 pF loads. Therefore, for higher REF_{in} frequencies, the one–to–one ratio may not be used for this magnitude of signal swing and loading requirements. Likewise, for REF_{in} frequencies above two times the highest rated frequency, the ratio must be more than two.

The output has a special on–board driver that has slew–rate control. This feature minimizes interference in the application.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption.

LOOP PINS

f_{in} and $\overline{f_{in}}$
Frequency Inputs (Pins 11 and 10)

These pins are frequency inputs from the VCO. These pins feed the on–board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they are usually used in a single–ended configuration (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 6)

This is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter
POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state
Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high–impedance state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the high–impedance state when the device is put into standby (STBY bit C4 = high).

The PD_{out} circuit is powered by V_{PD}. The phase detector gain is controllable by bits C3, C2, and C1: gain (in amps per radian) = PD_{out} current divided by 2π.

ϕ_R and ϕ_V (Pins 3 and 4)
Double–Ended Phase/Frequency Detector Outputs

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase
POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD
Lock Detector Output (Pin 2)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V (see Figure 17).

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx
External Resistor (Pin 8)

A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Tables 4 and 5 for other current values. The recommended value for Rx is 3.9 kΩ. A value of 3.9 kΩ provides current at the PD_{out} pin of approximately 1 mA @ V_{DD} = 3 V and approximately 1.7 mA @ V_{DD} = 5 V in the 100% current mode. Note that V_{DD}, not V_{PD}, is a factor in determining the current.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

Table 4. PD_{out} Current*, C1 = Low with OUTPUT A *not* Selected as "Port"; Also, Default Mode When OUTPUT A Selected as "Port"

Bit C3	Bit C2	PD_{out} Current*
0	0	70%
0	1	80%
1	0	90%
1	1	100%

* At the time the data sheet was printed, only the 100% current mode was guaranteed. The reduced current modes were for experimentation only.

Table 5. PD_{out} Current*, C1 = High with OUTPUT A *not* Selected as "Port"

Bit C3	Bit C2	PD_{out} Current*
0	0	25%
0	1	50%
1	0	75%
1	1	100%

* At the time the data sheet was printed, only the 100% current mode was guaranteed. The reduced current modes were for experimentation only.

TEST POINT PINS

TEST 1
Modulus Control Signal (Pin 9)

This pin may be used in conjunction with the Test 2 pin for access to the on–board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and must be floated in an actual application. This pin must be attached to an isolated pad with no trace.

TEST 2
Prescaler Output (Pin 13)

This pin may be used to access the on–board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and must be floated in an actual application. This pin must be attached to an isolated pad with no trace.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply (Pin 14)

This pin supplies power to the main CMOS digital portion of the device. Also, this pin, in conjunction with the Rx resistor, determines the internal reference current for the PD_{out} pin. The voltage range is +2.7 to +5.5 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC}
Positive Power Supply (Pin 12)

This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is +2.7 to +5.5 V with respect to the GND pin. In standby mode, the V_{CC} pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 21.

For optimum performance, V_{CC} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

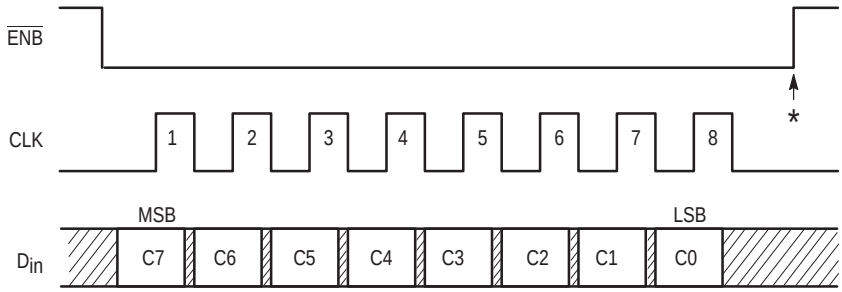
V_{PD}
Positive Power Supply (Pin 5)

This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin may be more or less than the potential applied to the V_{DD} and V_{CC} pins. The voltage range for V_{PD} is 2.7 to 5.5 V with respect to the GND pin.

For optimum performance, V_{PD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND
Ground (Pin 7)

Common ground.



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 – POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 17. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 – PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 – LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 – STBY: When set, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high–impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.

When C4 is reset low, the part is taken out of standby in two steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C3, C2 – I2, I1: Controls the PD_{out} source/sink current per Tables 4 and 5. With both bits high, the maximum current is available. Also, see C1 bit description.

C1 – Port: When the OUTPUT A pin is selected as “Port” via bits A22 and A23, C1 determines the state of OUTPUT A. When C1 is set high, OUTPUT A is forced high; C1 low forces OUTPUT A low. When OUTPUT A is ***not*** selected as “Port,” C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 4 and 5.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when OUTPUT A is selected as “Port.” The Port bit is not affected by the standby mode.

C0 – Out B: Determines the state of OUTPUT B. When C0 is set high, OUTPUT B is high–impedance; C0 low forces OUTPUT B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 14. C Register Access and Format (8 Clock Cycles are Used)

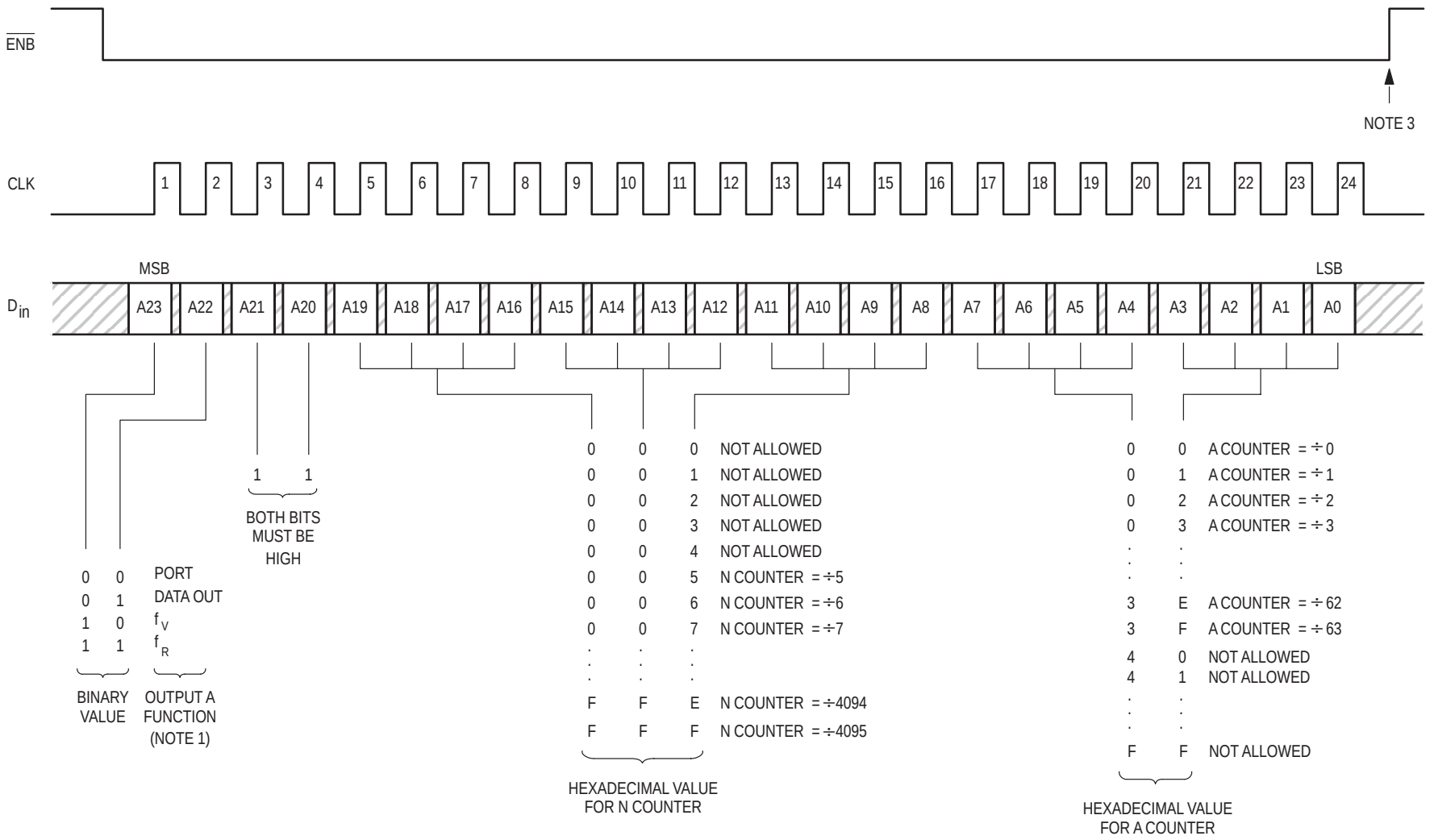
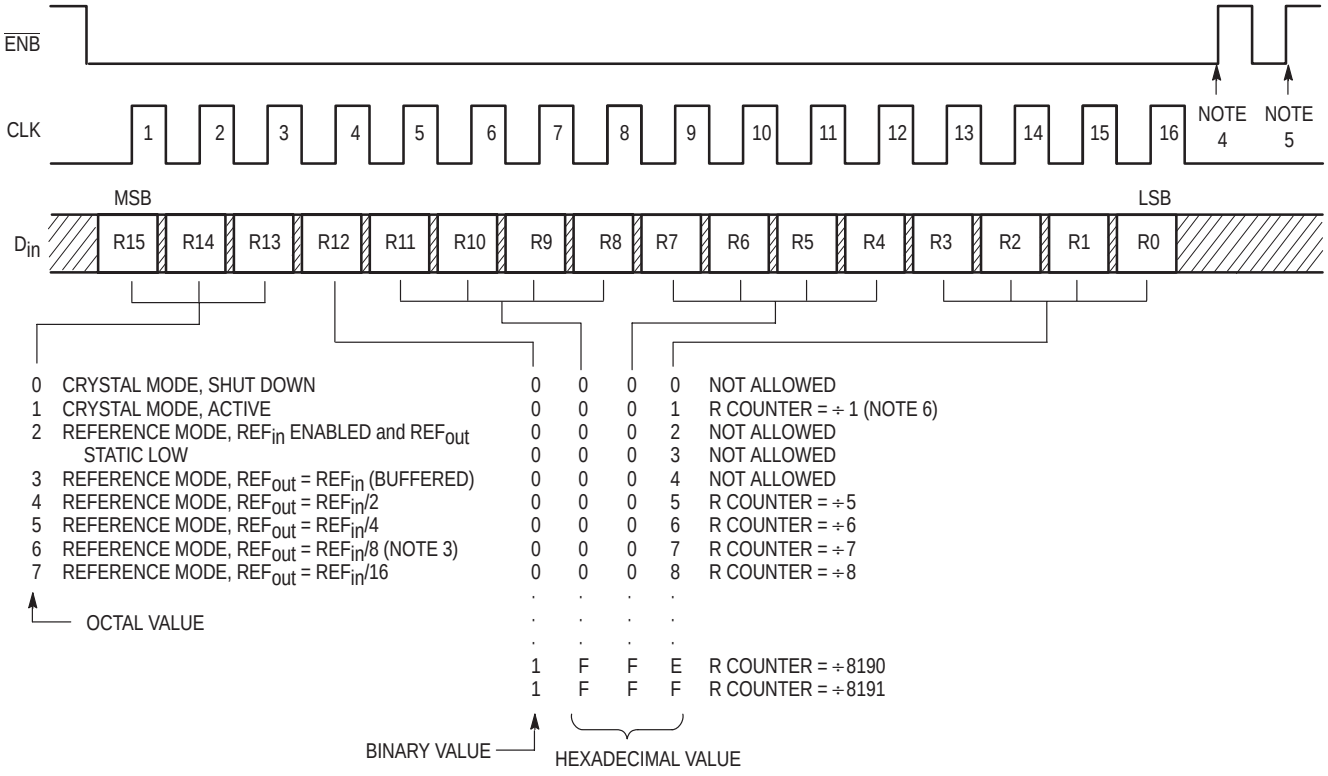


Figure 15. A Register Access and Format (24 Clock Cycles are Used)

NOTES:

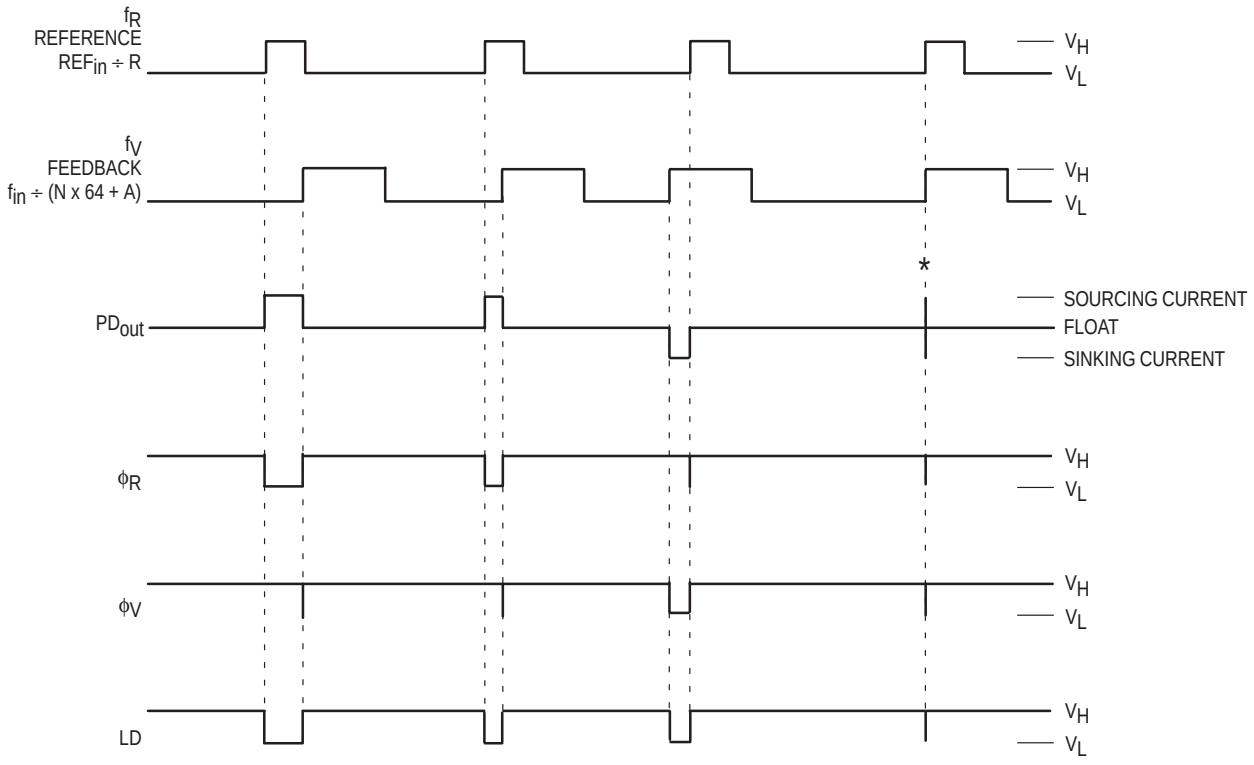
1. A power-on initialize circuit forces the OUTPUT A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.



NOTES:

1. Bits R15 through R13 control the configurable “OSC or 4–stage divider” block (see Block Diagram).
2. Bits R12 through R0 control the “13–stage R counter” block (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the “OSC or 4–Stage Divider” block in the Block Diagram. Bits R0 – R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. Optional load pulse. At this point, bits R0 – R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. The C and A registers are not affected. The first buffer of the R register is not affected. Also, see note 3 of Figure 15 for an alternate method of loading the second buffer in the R register.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 16. R Register Access and Format (16 Clock Cycles are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.

NOTE: The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is in the floating condition and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in} (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance (C_L) which does not exceed approximately 20 pF when used at the highest operating frequencies listed in the Loop Specifications table. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

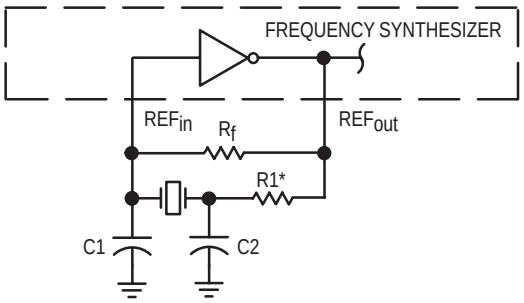
C_{in} = 5 pF (see Figure 19)
C_{out} = 6 pF (see Figure 19)
C_a = 1 pF (see Figure 19)
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency (f_R) at OUTPUT A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table NO TAG).



* May be needed in certain cases. See text.

Figure 18. Pierce Crystal Oscillator Circuit

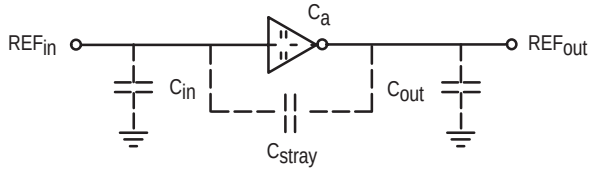
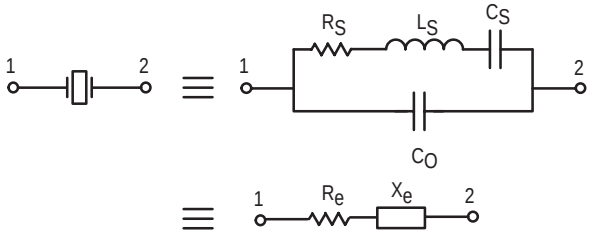


Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 20. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, “The Piezoelectric Crystal Unit–Definitions and Method of Measurement”, *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, “Quartz Crystals for Frequency Control”, *Electro–Technology*, June 1969.

P. J. Ottowitz, “A Guide to Crystal Selection”, *Electronic Design*, May 1966.

D. Babin, “Designing Crystal Oscillators”, *Machine Design*, March 7, 1985.

D. Babin, “Guidelines for Crystal Oscillator Design”, *Machine Design*, April 25, 1985.

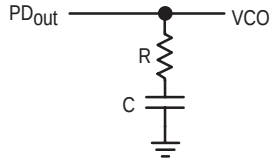
Table 6. Partial List of Crystal Manufacturers

Motorola — Internet Address *http://motorola.com* (Search for resonators)
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

(A)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

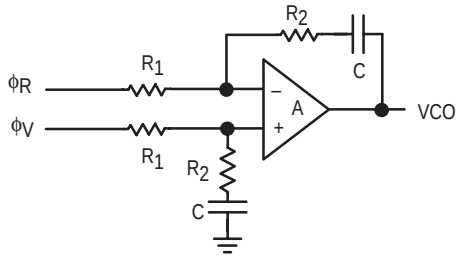
$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:

For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:

For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

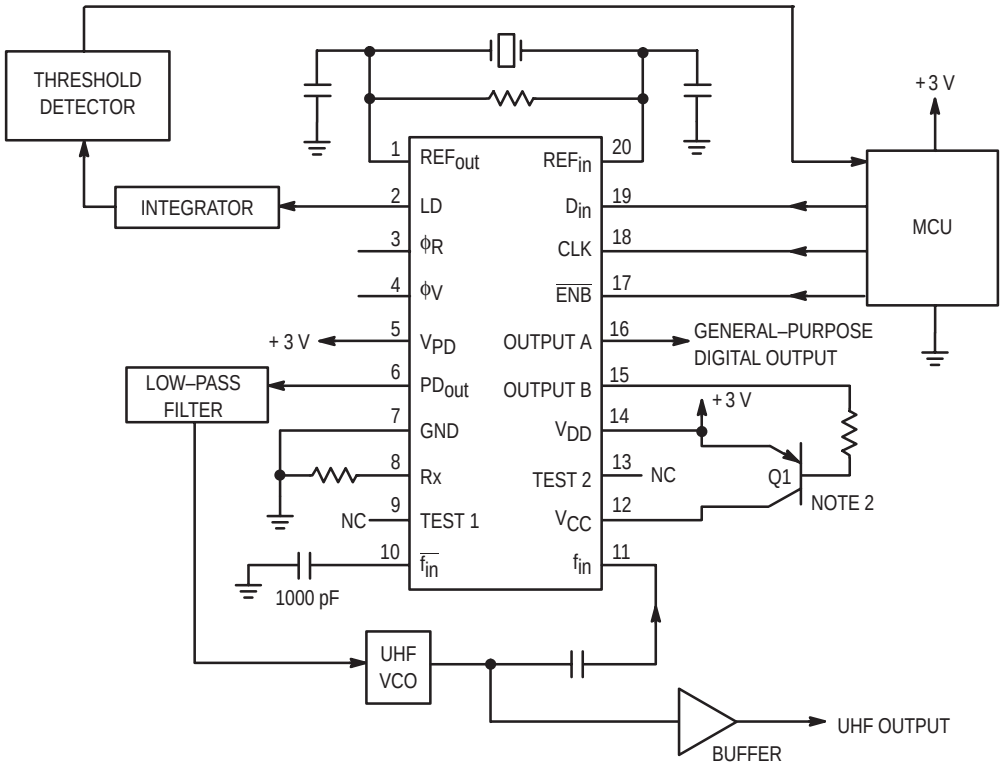
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.

Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

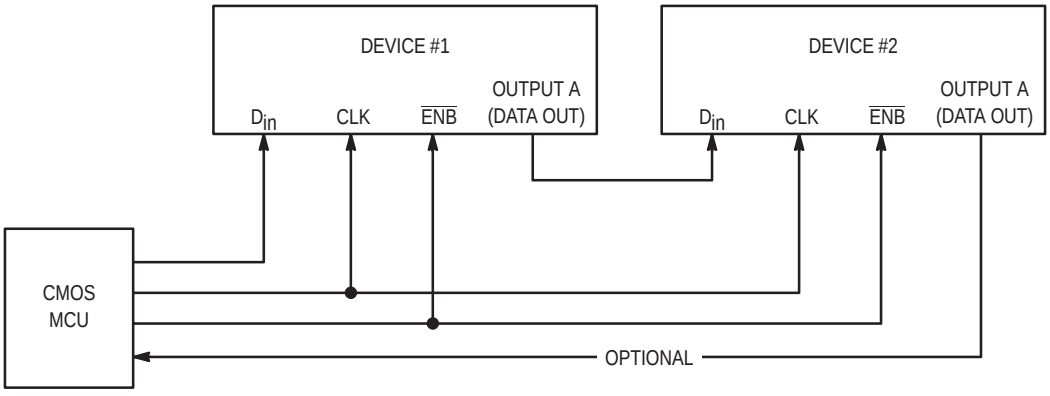
AN1253, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

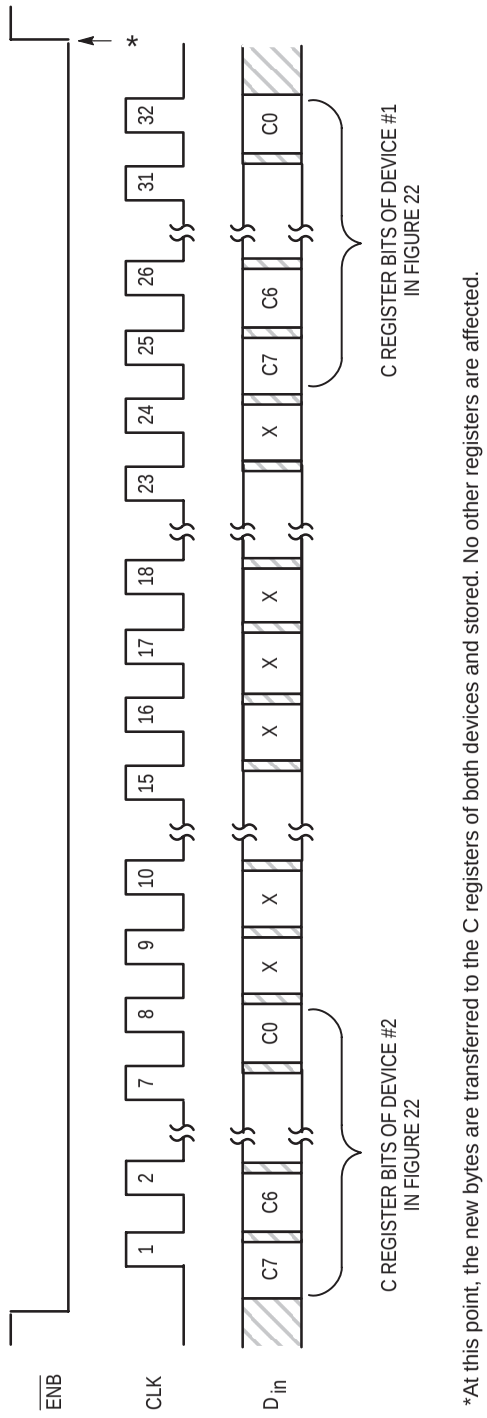
1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general–purpose digital pin, OUTPUT B. If the standby feature is not needed, tie Pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low–inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in} / f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

Figure 21. Example Application



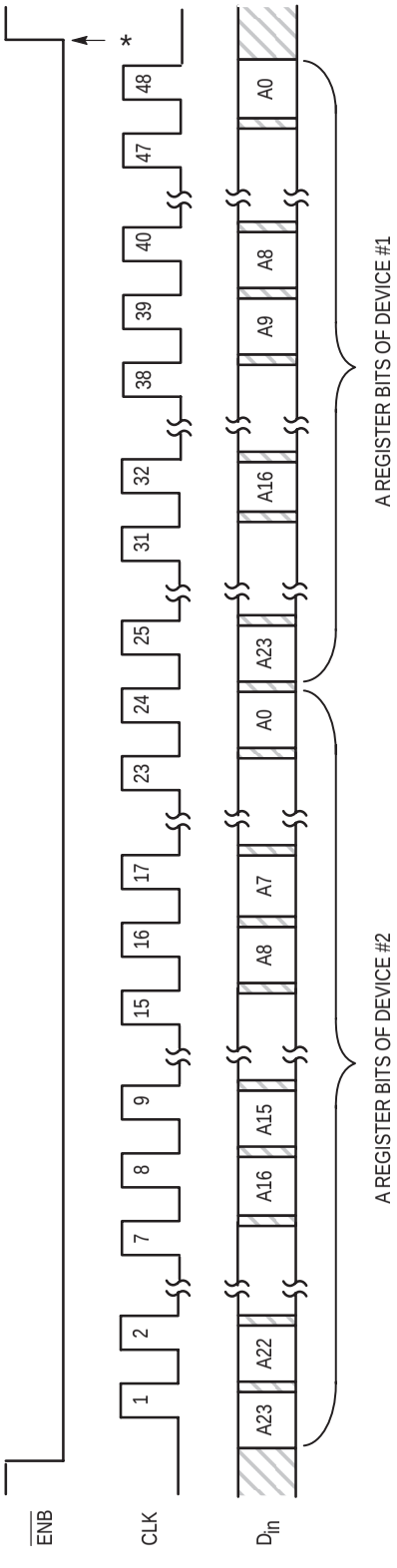
NOTE: See related Figures 23, 24, and 25.

Figure 22. Cascading Two Devices



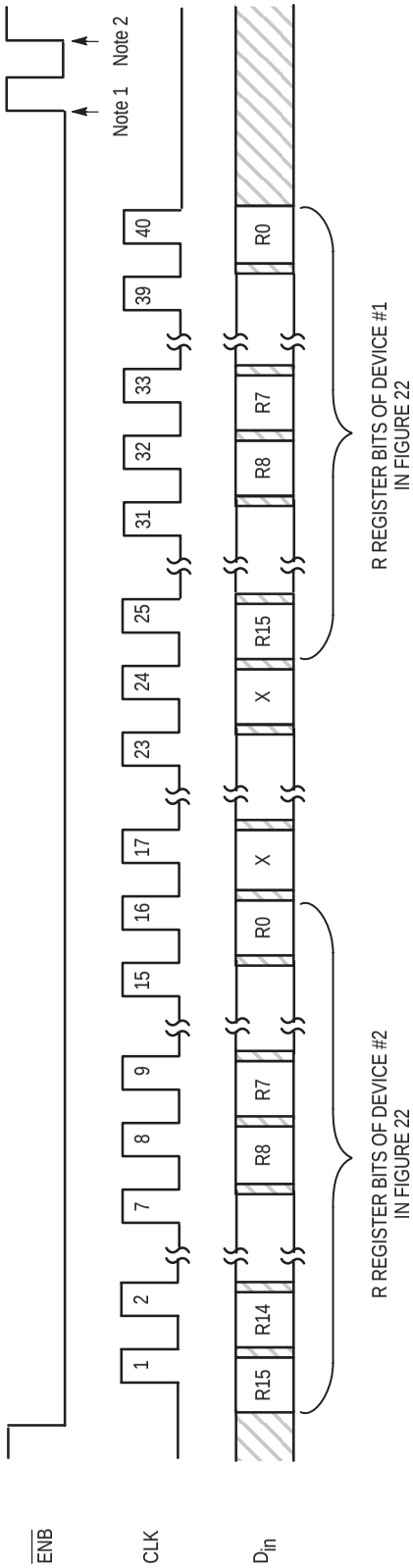
*At this point, the new bytes are transferred to the C registers of both devices and stored. No other registers are affected.

Figure 23. Accessing the C Registers of Two Cascaded MC145202 Devices



* At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counter can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

Figure 24. Accessing the A Registers of Two Cascaded MC145202 Devices



NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14 and R15 are stored and sent to the "OSC or 4–Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therfore, the R counter divide is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. Optional load pulse. At this point, the bits R0 through R12 are transfered to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the ENB pulse, as shown. The C and A registers are not affected. The first buffer of the R register is not affected. Also, see note of Figure 24 for an alternate method of loading the second buffer in the R register.

Figure 25. Accessing the R Registers of Two Cascaded MC145202 Devices

MOTOROLA

Product Preview

2.0 GHz PLL Frequency Synthesizer

MC145202-1

PLL FREQUENCY SYNTHESIZER

SEMICONDUCTOR TECHNICAL DATA

The MC145202–1 is pin–for–pin compatible with the previous generation MC145200, MC145201, and MC145202. Table 1 highlights the different features in these four devices. The MC145202–1 is recommended for new designs, and also offers improved suppression of reference sideband spurs.

The counters are programmed via a synchronous serial port which is SPI compatible. The serial port is byte-oriented to facilitate control via an MCU. Due to the innovative BitGrabber Plus™ registers, the MC145202–1 may be cascaded with other peripherals featuring BitGrabber Plus without requiring leading dummy bits or address bits in the serial data stream. In addition, BitGrabber Plus peripherals may be cascaded with existing BitGrabber™ peripherals.

The device features a single–ended current source/sink phase detector A output and a double–ended phase detector B output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single–ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

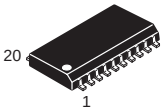
Slew–rate control is provided by a special driver designed for the REF_{out} pin. This minimizes interference caused by REF_{out}.

This part includes a differential RF input that may be operated in a single–ended mode. Also featured are on–board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

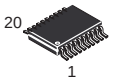
In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on–board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double–buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

- Maximum Operating Frequency: 2000 MHz @ –10 dBm
- Operating Supply Current: 4 mA Nominal at 3.0 V
- Operating Supply Voltage Range (V_{DD}, V_{CC}, V_{PD} Pins): 2.7 to 5.5 V
- Current Source/Sink Phase Detector Output:
  1.7 mA @ 5.0 V or 1.0 mA @ 3.0 V
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- R Counter Division Range: 1 and 5 to 8191
- Dual–Modulus Capability Provides Total Division up to 262,143
- High–Speed Serial Interface: 4 Mbps
- Output A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General–Purpose Digital Outputs:
  Output A: Totem–Pole (Push–Pull) with Four Output Modes
  Output B: Open–Drain
- Patented Power–Saving Standby Feature with Orderly Recovery for Minimizing Lock Times, Standby Current: 30 μA
- See App Note AN1253/D for Low–Pass Filter Design, and AN1277/D for Offset Reference PLLs for Fine Resolution or Fast Hopping

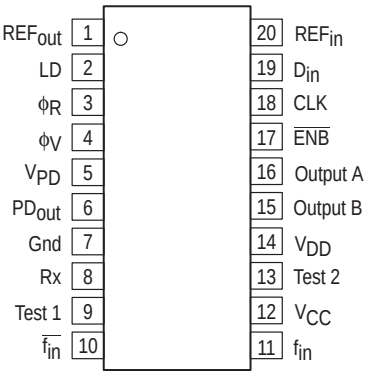


F SUFFIX
PLASTIC PACKAGE
CASE 751J
(SO–20)



DT SUFFIX
PLASTIC PACKAGE
CASE 948D
(TSSOP–20)

PIN CONNECTIONS



(Top View)

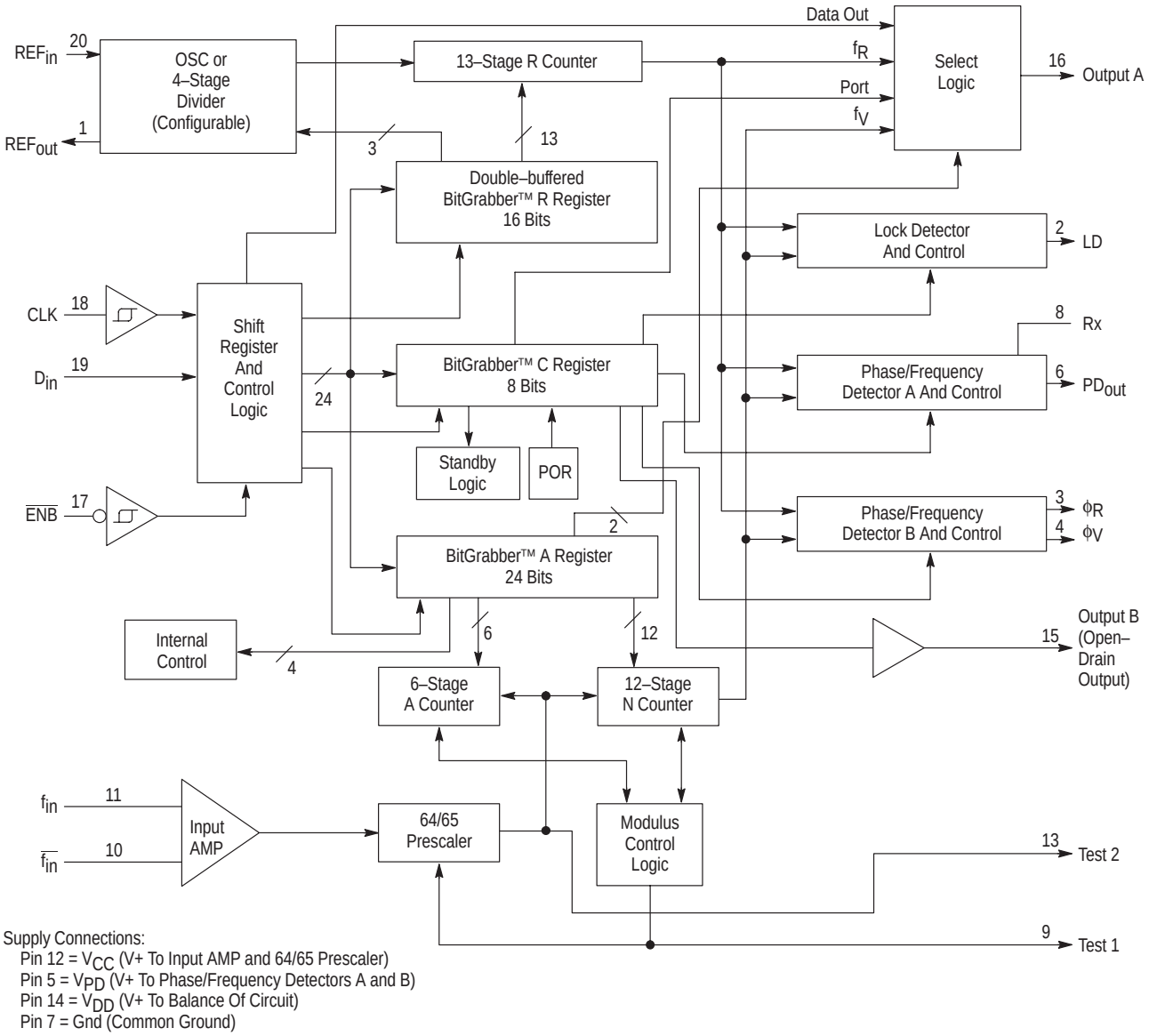
EVALUATION KIT

The P/N TBD, which contains hardware and software, will be available.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC145202F1	T_A = –40 to 85°C	SO–20
MC145202DT1		TSSOP–20

BLOCK DIAGRAM



Supply Connections:
Pin 12 = V_{CC} (V+ To Input AMP and 64/65 Prescaler)
Pin 5 = V_{PD} (V+ To Phase/Frequency Detectors A and B)
Pin 14 = V_{DD} (V+ To Balance Of Circuit)
Pin 7 = Gnd (Common Ground)

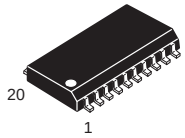
Table 1. Differences in the PLL Frequency Synthesizers

	Preferred	Not Recommended For New Designs		
Parameter	**MC145202–1**	**MC145202**	**MC145201**	**MC145200**
Supply Voltage, V_{DD} and V_{CC} (main supply)	2.7 to 5.5 V	2.7 to 5.5 V	4.5 to 5.5 V	4.5 to 5.5 V
Supply Voltage, V_{PD} (charge pump supply)	2.7 to 5.5 V	2.7 to 5.5 V	4.5 to 5.5 V	8.0 to 9.5 V
Supply Current	4 mA	4 mA	12 mA	12 mA
Value of External Resistor Rx, typical	3.9 kΩ for 1.7 mA [Note]	3.9 kΩ for 1.7 mA	18 kΩ for 2.0 mA	47 kΩ for 2.0 mA
Serial Programming with only 1 PLL (not cascaded)	Same, No Change	Same	Same	Same
Serial Programming with 2 or more PLLS (cascaded)	No leading dummy bits	No leading dummy bits	Leading dummy bits	Leading dummy bits

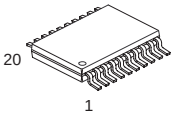
NOTE: Preliminary value.

MC145220

Dual 1.1 GHz PLL Frequency Synthesizer
BiCMOS



F SUFFIX
SOG PACKAGE
CASE 803C

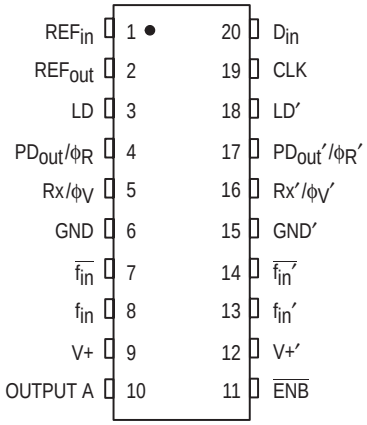


DT SUFFIX
TSSOP
CASE 948D

ORDERING INFORMATION

MC145220F	SOG Package
MC145220DT	TSSOP

PIN ASSIGNMENT



The MC145220 is a low–voltage, single–chip frequency synthesizer with serial interface capable of direct usage up to 1.1 GHz. The device simultaneously supports two loops. The two on–chip dual–modulus prescalers may be independently programmed to divide by either 32/33 or 64/65.

The device consists of two dual–modulus prescalers, two 6–stage A counters, two 12–stage N counters, two fully programmable 13–stage R (reference) counters, and two lock detectors. Four phase/frequency detectors are included: two with current source/sink outputs and two with double–ended outputs.

The counters are programmed via a synchronous serial port which is SPI compatible. The serial port is byte–oriented to facilitate control via an MCU. Due to the innovative BitGrabber Plus™ registers, the MC145220 may be cascaded with other peripherals featuring BitGrabber Plus without requiring leading dummy bits or multiple address bits in the serial data stream. In addition, BitGrabber Plus peripherals may be cascaded with existing BitGrabber™ peripherals. Because this device is a dual synthesizer, a single steering bit is used in the serial data stream to direct the data to either side of the chip.

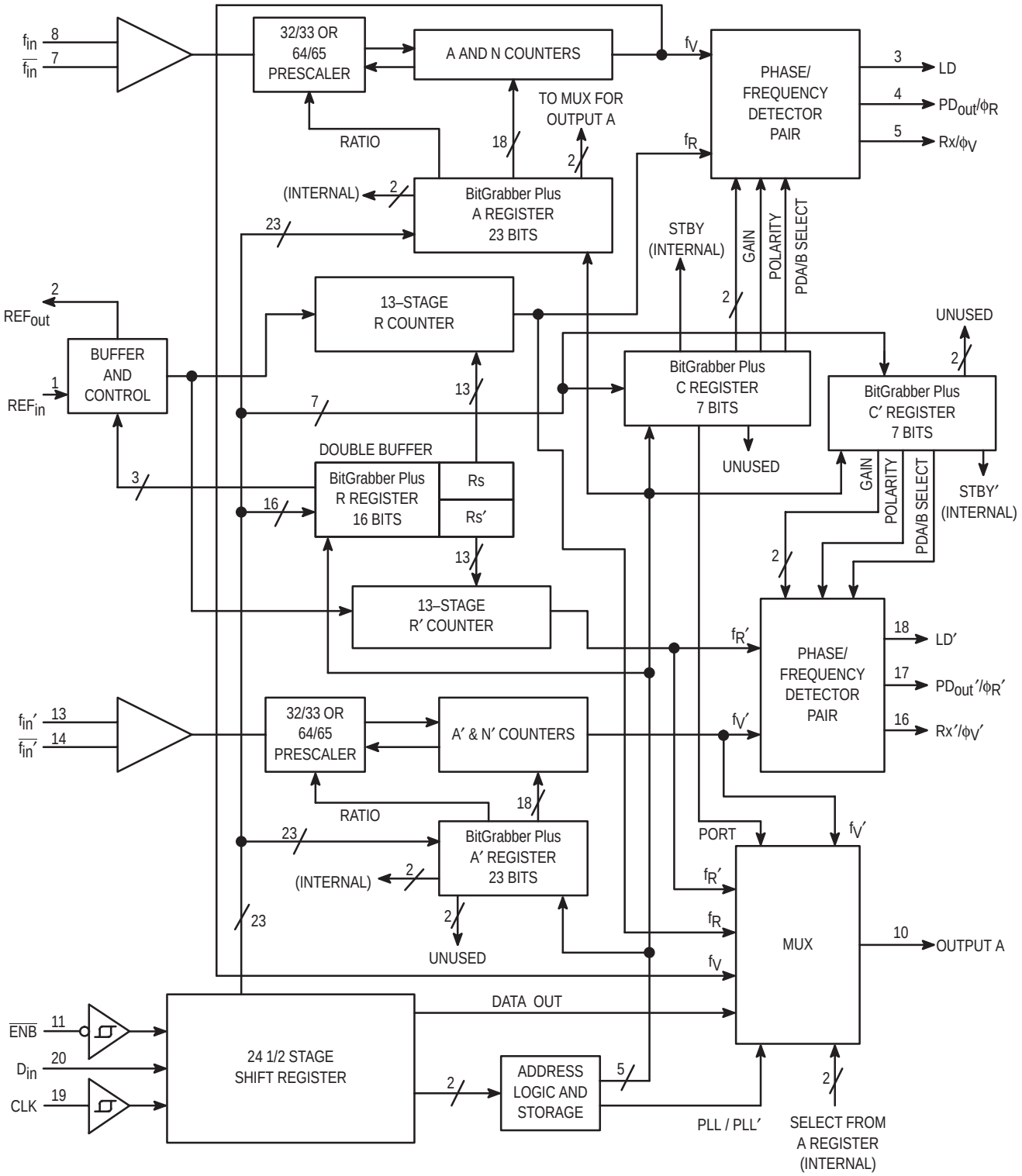
The phase/frequency detectors have linear transfer functions (no dead zones). The current delivered by the current source/sink outputs is controllable via the serial port.

Also featured are low–power standby for either one or both loops and on–board support of an external crystal. In addition, the part may be configured such that the REF_{in} pin accepts an external reference signal. In this configuration, the REF_{out} pin may be programmed to output the REF_{in} frequency divided by 1, 2, 4, 8, or 16.

- Operating Frequency: 40 to 1100 MHz
- Operating Supply Voltage Range: 2.7 to 5.5 V
- Supply Current: Both PLLs Operating — 12 mA Nominal
  One PLL Operating, One on Standby — 6.5 mA Nominal
  Both PLLs on Standby — 30 μA Maximum
- Phase Detector Output Current: Up to 2 mA @ 5 V
  Up to 1 mA @ 3 V
- Operating Temperature Range: – 40 to 85°C
- Independent R Counters Allow Use of Different Step Sizes for Each Loop
- Double–Buffered R Register — Reference and Loop Divide Ratios Updated Simultaneously
- R Counter Division Range: 1 and 10 to 8,191
- Dual–Modulus Capability Provides Total Division of the VCO Frequency up to 262,143
- Direct Interface to Motorola SPI Data Port
- Evaluation Kit Available (Part Number MC145220EVK)
- See Application Note AN1253/D for Low–Pass Filter Design, and AN1277/D for Offset Reference PLLs for Fine Resolution or Fast Hopping

REV 4
1/98 TN98012300

BLOCK DIAGRAM



PIN 9 = V+ (Positive Power to the main PLL, Reference Circuit, and a portion of the Serial Port)
PIN 6 = GND (Ground to the main PLL, Reference Circuit, and a portion of the Serial Port)
PIN 12 = V+′ (Positive Power to PLL′ and a portion of the Serial Port)
PIN 15 = GND′ (Ground to PLL′ and a portion of the Serial Port)

MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V+, V+′	DC Supply Voltage	– 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V+ + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V+ + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I	DC Supply Current, V+, V+′, GND, and GND′ Pins	30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

ELECTRICAL CHARACTERISTICS

(V+ = V+′ = 2.7 to 5.5 V, GND = GND′, Voltages Referenced to GND, T_A = – 40 to 85°C, unless otherwise stated)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, dc Coupled	0.3 x V+	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, dc Coupled	0.7 x V+	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		100	mV
V_{OL}	Maximum Low–Level Output Voltage (LD, LD′, REF_{out}, Output A)	I_{out} = 20 μA, Device in Reference Mode; Output A Not Selected as Port	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, Output A)	I_{out} = – 20 μA, Device in Reference Mode; Output A Not Selected as Port	V+ – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out})	V_{out} = 0.3 V	0.5	mA
I_{OL}	Minimum Low–Level Output Current (PD_{out}/ϕ_R, PD_{out}'/ϕ_R', Rx/ϕ_V, Rx'/ϕ_V')	V_{out} = 0.3 V; Phase/Frequency Detectors Configured with ϕ_R, ϕ_V Outputs	0.5	mA
I_{OL}	Minimum Low–Level Output Current (Output A)	V_{out} = 0.3 V	0.5	mA
I_{OL}	Minimum Low–Level Output Current (LD, LD′)	V_{out} = 0.3 V	0.5	mA
I_{OH}	Minimum High–Level Output Current (REF_{out})	V_{out} = V+ – 0.3 V	– 0.4	mA
I_{OH}	Minimum High–Level Output Current (PD_{out}/ϕ_R, PD_{out}'/ϕ_R', Rx/ϕ_V, Rx'/ϕ_V')	V_{out} = V+ – 0.3 V; Phase/Frequency Detectors Configured with ϕ_R, ϕ_V Outputs	– 0.4	mA
I_{OH}	Minimum High–Level Output Current (Output A)	V_{out} = V+ – 0.3 V; Output A Not Selected as Port	– 0.4	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	V_{in} = V+ or GND; Device in XTAL Mode	± 1.0	μA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V+ or GND; Device in Reference Mode	± 150	μA
I_{OZ}	Maximum Output Leakage Current (PD_{out}/ϕ_R, PD_{out}'/ϕ_R')	V_{out} = V+ or GND; Phase/Frequency Detectors Configured with PD_{out} Output, Output in High–Impedance State	± 150	nA
I_{OZ}	Maximum Output Leakage Current (Output A, LD, LD′)	V_{out} = V+ or GND; Output A Selected as Port; Output in High–Impedance State	± 5	μA
I_{STBY}	Maximum Standby Supply Current	V_{in} = V+ or GND; Outputs Open; Both PLLs in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode	30	μA
I_T	Total Operating Supply Current	$f_{in} = f_{in}'$ = 1.1 GHz; both loops active; REF_{in} = 13 MHz @ 1 V p–p; Output A = Inactive; All Outputs = No Connect; D_{in}, $\overline{ENB}$, CLK = V+ or GND; Phase/Frequency Detectors Configured with ϕ_R, ϕ_V Outputs	*	mA

* The nominal value is 12 mA. This is not a guaranteed limit.

ANALOG CHARACTERISTICS — CURRENT SOURCE/SINK OUTPUTS — PD_{out}/ϕ_R AND PD_{out}'/ϕ_R'

(Phase/Frequency Detectors Configured with PD_{out} Outputs, $I_{out} \leq 2$ mA @V+ = V+′ = 4.5 to 5.5 V, $I_{out} \leq 1$ mA @V+ = V+′ = 2.7 to 4.4 V, GND = GND′, Voltages Referenced to GND)

Parameter	Test Condition	Guaranteed Limit	Unit
Maximum Source Current Variation Part–to–Part (Notes 3 and 4)	V_{out} = 0.5 x V+	± 20	%
Maximum Sink–versus–Source Mismatch (Note 3)	V_{out} = 0.5 x V+	12	%
Output Voltage Range (Note 3)	I_{out} variation ≤ 20%	0.5 to V+ – 0.5 V	V

NOTES:

5. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
6. See Rx Pin Description for external resistor values.
7. This parameter is guaranteed for a given temperature within – 40 to 85°C and given supply voltage within 2.7 to 5.5 V.
8. Applicable for the Rx/ϕ_V or Rx'/ϕ_V' reference pin tied to the GND or GND′ pin through a resistor. See Pin Descriptions for suggested resistor values.

AC INTERFACE CHARACTERISTICS

(V+ = V+′ = 2.7 to 5.5 V, GND = GND′, T_A = – 40 to 85°C, C_L = 25 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	Guaranteed Limit	Unit
f_{clk}	Serial Data CLK Frequency (Figure 1) NOTE: Refer to Clock t_w below	dc to 2.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to Output A (Selected as Data Out) (Figures 1 and 5)	200	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to Output A (Selected as Port) (Figures 2 and 6)	200	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Output A; t_{THL} only, on Output A when Selected as Port (Figures 1, 5, and 6)	200	ns
C_{in}	Maximum Input Capacitance — D_{in}, CLK, $\overline{ENB}$	10	pF

TIMING REQUIREMENTS (V+ = V+′ = 2.7 to 5.5 V, GND = GND′, T_A = – 40 to 85°C, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} versus CLK (Figure 3)	50	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ versus CLK (Figure 4)	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$ (Figure 4)	*	cycles
t_w	Minimum Pulse Width, CLK (Figure 1)	250	ns
t_r, t_f	Maximum Input Rise and Fall Times — CLK (Figure 1)	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} or f_{in}' cycles with selection of a 64/65 prescale ratio or 99 f_{in} or f_{in}' cycles with selection of a 32/33 prescale ratio, whichever is greater.

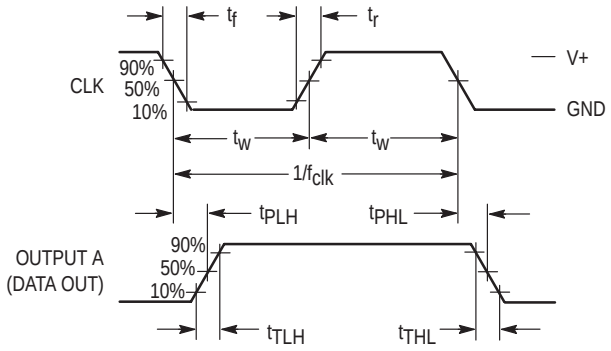


Figure 1.

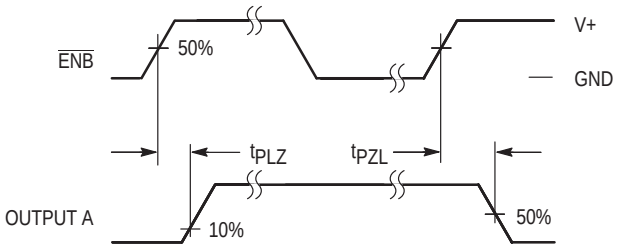


Figure 2.

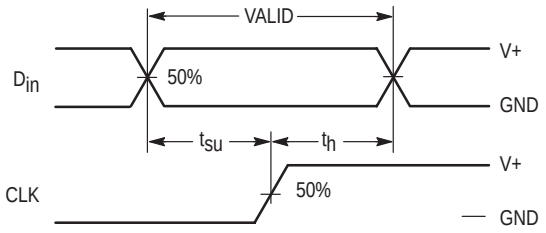


Figure 3.

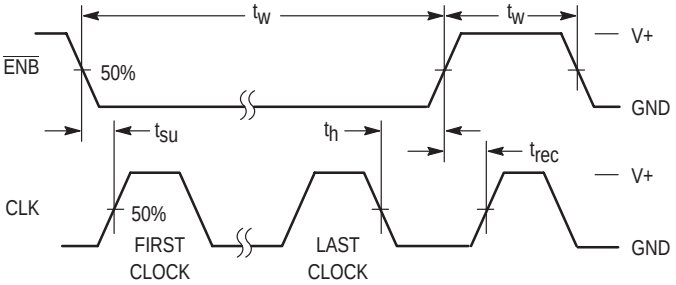
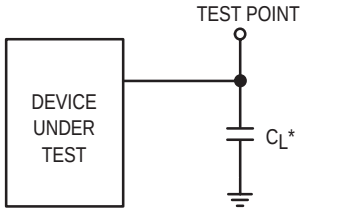
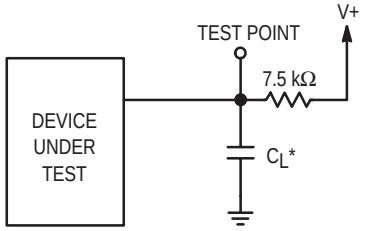


Figure 4.



* Includes all probe and fixture capacitance.

Figure 5.



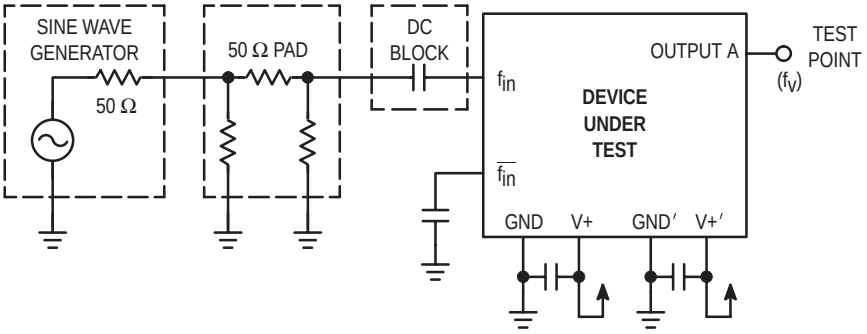
* Includes all probe and fixture capacitance.

Figure 6.

LOOP SPECIFICATIONS (V+ = V+′ = 2.7 to 5.5 V unless otherwise indicated, GND = GND′, T_A = – 40 to 85°C)

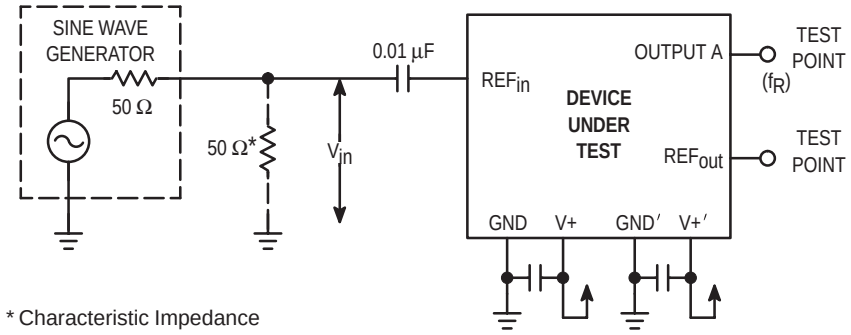
Symbol	Parameter	Test Condition	Guaranteed Operating Range		Unit
			Min	Max	
P_{in}	Input Sensitivity Range, f_{in} or f_{in}' (Figure 7)	40 MHz ≤ frequency < 300 MHz 300 MHz ≤ frequency < 700 MHz 700 MHz ≤ frequency < 1100 MHz	– 2 – 5 – 16	8 6 4	dBm*
ΔP_{in}	Difference Allowed Between f_{in} and f_{in}'			10	dB
—	Isolation Between f_{in} and f_{in}'		15		dB
f_{ref}	Input Frequency, REF_{in} Externally Driven in Reference Mode (Figure 8)	V_{in} ≥ 400 mV p–p, R Counter set to divide ratio such that f_R ≤ 1 MHz, REF Counter set to divide ratio such that REF_{out} ≤ 5 MHz	4	27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode (Figure 9)	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance; R Counter and REF Counter same as above V+ = 2.7 V V+ = 3.5 V V+ = 4.5 V V+ = 5.5 V	 2 2 2 2	 10 13 15 15	MHz
f_{out}	Output Frequency, REF_{out} (Figures 10 and 12)	C_L = 25 pF	dc	5	MHz
f	Operating Frequency of the Phase Detectors		dc	1	MHz
t_w	Output Pulse Width, ϕ_R, ϕ_V, ϕ_R', ϕ_V' (Figures 11 and 12)	f_R in Phase with f_V, C_L = 25 pF	16	125	ns
C_{in}	Input Capacitance, REF_{in}		—	5	pF

* Power level at the input to the dc block.



NOTE: Alternately, the 50 Ω pad may be a T network.

Figure 7. Test Circuit



* Characteristic Impedance

Figure 8. Test Circuit — Reference Mode

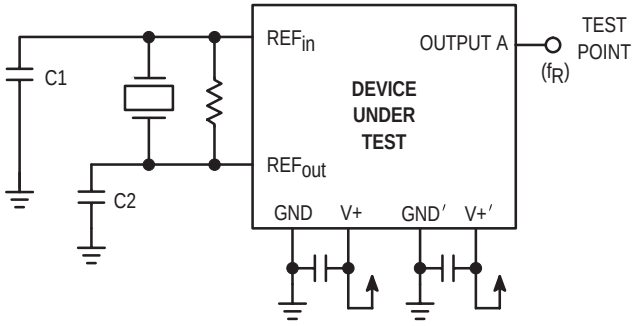


Figure 9. Test Circuit — Crystal Mode

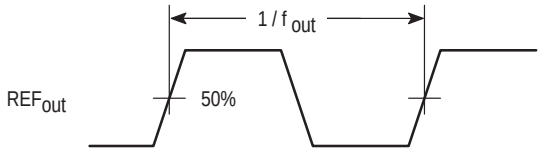


Figure 10. Switching Waveform

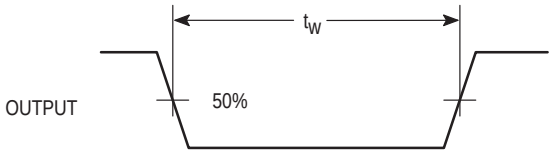
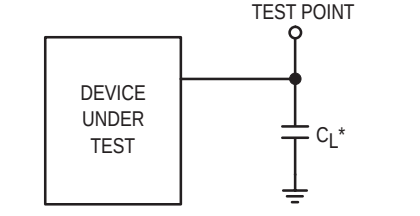
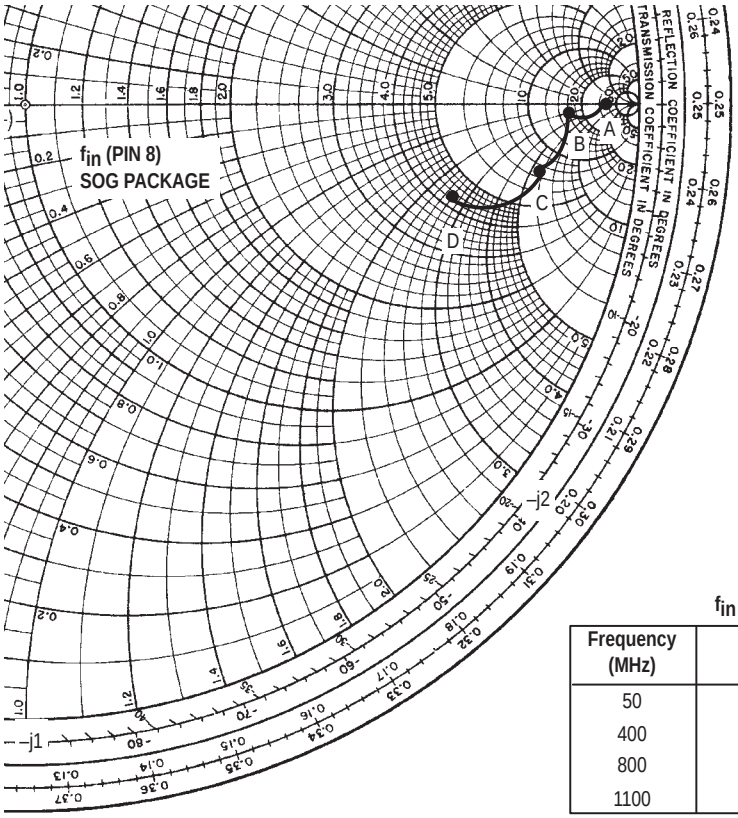


Figure 11. Switching Waveform



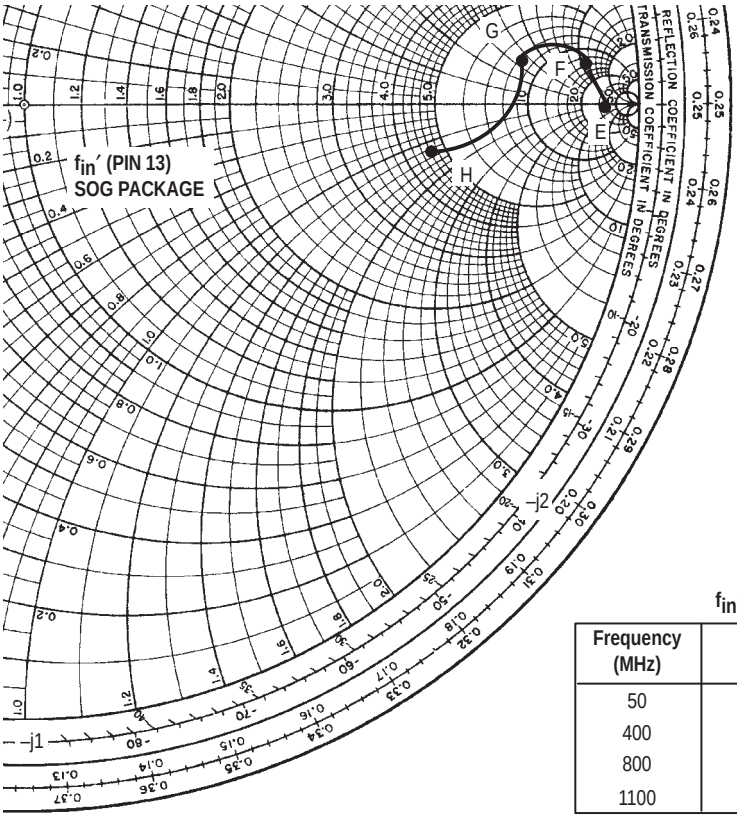
* Includes all probe and fixture capacitance.

Figure 12. Test Circuit



f_{in} (PIN 8) – SOG PACKAGE

Frequency (MHz)	Point	Impedance (Ω)	
		3 V Supply	5 V Supply
50	A	1900 – j 157	1970 – j 102
400	B	1440 – j 228	1510 + j 19
800	C	552 – j 380	671 – j 334
1100	D	196 – j 141	223 – j 147



f_{in}' (PIN 13) – SOG PACKAGE

Frequency (MHz)	Point	Impedance (Ω)	
		3 V Supply	5 V Supply
50	E	1900 + j 149	1930 + j 214
400	F	878 + j 703	746 + j 741
800	G	705 + j 208	626 + j 327
1100	H	215 – j 69.3	243 – j 61.3

Figure 13. Nominal Input Impedance of f_{in} and f_{in}' — Series Format (R + jX) (50 – 1100 MHz)

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 20)

The bit stream begins with the MSB and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration registers, 2 bytes (16 bits) to access the first buffer of the R registers, or 3 bytes (24 bits) to access the A registers (see Table 1). The values in the registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

NOTE

The value programmed for the N counter must be greater than or equal to the value of the A counter.

The 13 LSBs of the R registers are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The two second buffers of the R register contain the two 13–bit divide ratios for the R counters. These second buffers are loaded with the contents of the first buffer as follows. Whenever the A register is loaded, the Rs (second) buffer is loaded from the R (first) buffer. Similarly, whenever the A′ register is loaded, the Rs′ (second) buffer is updated from the R (first) buffer. This allows presenting new values to the R, A, and N counters simultaneously. Note that two different R counter divide ratios may be established: one for the main PLL and another for PLL′.

The bit stream does not need address bits due to the innovative BitGrabber Plus registers. A steering bit is used to direct data to either the main PLL or PLL′ section of the chip. Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 14, 15, and 16.

D_{in} typically switches near 50% of V+ to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Registers	C7, C6, C5, . . ., C0
16	R Register, First Buffer	R15, R14, R13, . . ., R0
24	A Registers	A23, A22, A21, . . ., A0
Other Values ≤ 32	Not Allowed	
Values > 32	See Figures 24 to 27	

CLK
Serial Data Clock Input (Pin 19)

Low–to–high transitions on CLK shift bits available at the D_{in} pin, while high–to–low transitions shift bits from Output A (when configured as Data Out, see Pin 10). The 24–1/2 stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C registers. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A registers. See Table 1 and Figures 14, 15, and 16. The number of clocks required for cascaded devices is shown in Figures 25 through 27.

CLK typically switches near 50% of V+ and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at GND (with $\overline{ENB}$ being a don't care) or $\overline{ENB}$ must be held at the potential of the V+ pin (with CLK being a don't care) during power–up. Floating, toggling, or having these pins in the wrong state during power–up does not harm the chip, but causes two potentially undesirable effects. First, the outputs of the device power up in an unknown state. Second, if two devices are cascaded, the A Registers must be written twice after power up. After these two accesses, the two cascaded chips perform normally.

$\overline{ENB}$
Active–Low Enable Input (Pin 11)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs whenever $\overline{ENB}$ is high and CLK is low.

This input is Schmitt–triggered and switches near 50% of V+, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

For POR information, see the note for the **CLK pin**.

OUTPUT A
Configurable Digital Output (Pin 10)

Output A is selectable as f_R, f_V, f_R', f_V', Data Out, or Port. Bits A21 and A22 and the steering bit (A23) control the selection; see Figure 15. When selected as Port, the pin becomes an open–drain N–channel MOSFET output. As such, a pullup device is needed for pin 10. With all other selections, the pin is a totem–pole (push–pull) output.

If A22 = A21 = high, Output A is configured as f_R when the steering bit is low and f_R' when the bit is high. These signals are the buffered outputs of the 13–stage R counters. The signals appear as normally low and pulse high. The signals can be used to verify the divide ratios of the R counters. These ratios extend from 10 to 8191 and are determined by the binary value loaded into bits R0 – R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of one. See Figure 16. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_R and f_R' should not exceed 1 MHz.

If A22 = high and A21 = low, Output A is configured as f_V when the steering bit is low and f_V' when the bit is high. These signals are the buffered outputs of the 12–stage N counters. The signals appear as normally low and pulse high. The signals can be used to verify the operation of the prescalers, A counters, and N counters. The divide ratio between the f_{in} or f_{in}' input and the f_V or f_V' signal is N x P + A. N is the divide ratio of the N counter, P is 32 with a 32/33 prescale ratio or 64 with a 64/65 prescale ratio, and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A registers. See Figure 15. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_V and f_V' should not exceed 1 MHz.

If A22 = low and A21 = high, Output A is configured as Data Out. This signal is the serial output of the 24–1/2 stage shift register. The bit stream is shifted out on the high–to–low transition of the CLK input. Upon power up, Output A is automatically configured as Data Out to facilitate cascading devices.

If A22 = A21 = low, Output A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high impedance when the Port bit is high. See Figure 14.

REFERENCE PINS

REF_{in} and REF_{out}
Reference Oscillator Input and Output (Pins 1 and 2)

Configurable Pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 16.

In the crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values, as recommended by the crystal supplier, are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the crystal are shown in Figure 9. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary). This is the active–crystal mode shown in Figure 16. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C or C′ register, the oscillator runs, but the R or R′ counter is stopped, respectively. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode shown in Figure 16, and can be engaged whether in standby or not.

In the reference mode, REF_{in} (pin 1) accepts a signal from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. The ac–coupled signal must be at least 400 mV p–p. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 16 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 5 MHz for large output swings (V_{OH} to V_{OL}) and 25 pF loads. Therefore, for REF_{in} frequencies above 5 MHz, the one–to–one ratio may not be used for these large signal swing and large C_L requirements. Likewise, for REF_{in} frequencies above 10 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in}, $\overline{f_{in}}$ and f_{in}', $\overline{f_{in}'}$
Frequency Inputs (Pins 8, 7 and 13, 14)

These pins feed the onboard RF amplifiers which drive the prescalers. These inputs may be fed differentially. However, they usually are used in single–ended configurations (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ac ground (via capacitor). The signal sources driving these pins originate from external VCOs.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the **Loop Specifications** table.

PD_{out}/ϕ_R, PD_{out}'/ϕ_R'
Single–Ended Phase/Frequency Detector Outputs (Pins 4 and 17)

When the C2 bits in the C or C′ registers are low, these pins are independently configured as single–ended outputs PD_{out} or PD_{out}', respectively. As such, each pin is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C0) in the C register = low (see Figure 14)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

POL bit (C0) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

These outputs can be enabled, disabled, and inverted via the C and C′ registers. If desired, these pins can be forced to the floating state by utilization of the standby feature in the C or C′ registers (bit C6). This is a patented feature.

The phase detector gain is controllable by bits C4 and C5: gain (in amps per radian) = PD_{out} current in amps divided by 2π.

PD_{out}/ϕ_R, Rx/ϕ_V and PD_{out}'/ϕ_R', Rx'/ϕ_V'
Double–Ended Phase/Frequency Detector Outputs (Pins 4, 5 and 17, 16)

When the C2 bits in the C or C′ registers are high, these two pairs of pins are independently configured as double–ended outputs ϕ_R, ϕ_V or ϕ_R', ϕ_V', respectively. As such, these outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detectors are described below and are shown in Figure 17.

POL bit (C0) in the C register = low (see Figure 14)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C0) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, or interchanged via C register bits C6 or C0. This is a patented feature. Note that when disabled in standby, these outputs are forced to their rest condition (high state). See Figure 14.

The ϕ_R and ϕ_V output signals swing from approximately GND to V+.

LD and LD′
Lock Detector Outputs (Pins 3 and 18)

Each output is essentially at a high–impedance state with very narrow low–going pulses of a few nanoseconds when the respective loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V, while LD′ is the logical ANDing of ϕ_R' and ϕ_V'. See Figure 17.

Upon power up, on–chip initialization circuitry forces LD and LD′ to the high–impedance state. These pins are low during standby. If unused, LD should be tied to GND and LD′ should be tied to GND′.

These outputs have open–drain N–channel MOSFET drivers. This facilitates a wired–OR function. See Figure 21.

Rx/ϕ_V and Rx'/ϕ_V'
External Current Setting Resistors (Pins 5 and 16)

When the C2 bits in the C or C′ registers are low, these two pins are independently configured as current setting pins Rx or Rx′, respectively. As such, resistors tied between each of these pins and GND and GND′, in conjunction with bits C4 and C5 in the C and C′ registers, determine the amount of current that the PD_{out} pins sink and source. When bits C4 and C5 are both set high, the maximum current is obtained; see Table 2 for other values of current.

Table 2. PD_{out} or PD_{out}' Current

C5	C4	Current
0	0	5%
0	1	50%
1	0	80%
1	1	100%

The formula for determining the value of Rx or Rx′ is as follows.

$$Rx = \frac{V1 - V2}{I}$$

where Rx is the value of external resistor in ohms, V1 is the supply voltage, V2 is 1.5 V for a reference current through Rx of 100 μA or 1.745 V for a reference current of 200 μA, and I is the reference current flowing through Rx or Rx′.

The reference current flowing through Rx or Rx′ is multiplied by a factor of approximately 10 (in the 100% current mode) and delivered by the PD_{out} or PD_{out}' pin, respectively. To achieve a maximum phase detector output current of 1 mA, the resistor should be about 15 kΩ when a 3 V supply is employed. See Table 3.

Table 3. Rx Values

Supply Voltage	Rx	PD_{out} or PD_{out}' Current in 100% Mode
3 V	15 kΩ	1 mA
5 V	16 kΩ	2 mA

Do not use a decoupling capacitor on the Rx or Rx′ pin. Use of a capacitor causes undesirable current spikes to appear on the phase detector output when invoking the standby mode.

POWER SUPPLY PINS

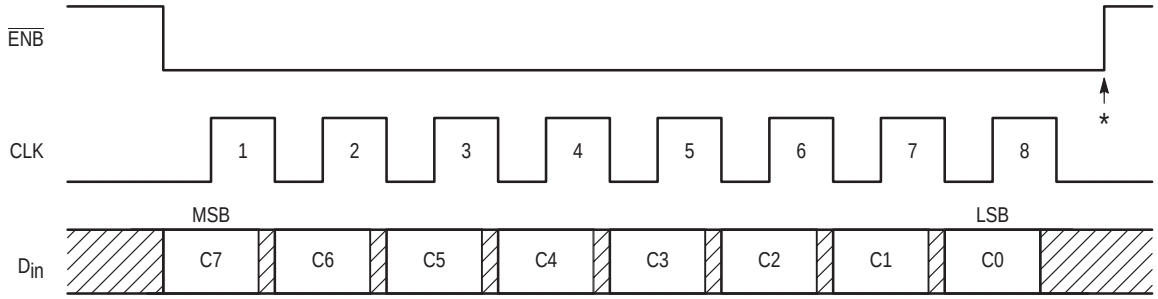
V+ and V+′
Positive Supply Potentials (Pins 9 and 12)

V+ supplies power to the main PLL, reference circuit, and a portion of the serial port. V+′ supplies power to PLL′ and a portion of the serial port. Both V+ and V+′ must be at the same voltage level and may range from 2.7 V to 5.5 V with respect to the GND and GND′ pins.

For optimum performance, V+ should be bypassed to GND and V+′ bypassed to GND′ using separate low–inductance capacitors mounted very close to the MC145220. Lead lengths and printed circuit board traces to the capacitors should be minimized. (The very fast switching speed of the device can cause excessive current spikes on the power leads if they are improperly bypassed.)

GND and GND′
Grounds (Pins 6 and 15)

The GND pin is the ground for the main PLL and GND′ is the ground for PLL′.



* At this point, the new byte is transferred to the C or C′ register and stored. No other registers are affected.

C7 – Steer: Used to direct the data to either the C or C′ register. A low level directs data to the C register; a high level is for the C′ register.

C6 – Standby: When set high, places both the main PLL and PLL′ (when C6 is set in the C register) or PLL′ only (when C6 is set in the C′ register) in the standby mode for reduced power consumption. The associated PD_{out} is forced to the floating state, the associated counters (A, N, and R) are inhibited from counting, the associated Rx current is shut off, and the associated prescaler stops counting and is placed in a low current mode. The associated double–ended phase/frequency detector outputs are forced to a high level. In standby, the associated LD output is placed in the low–state, thus indicating "not locked" (open loop). During standby, data is retained in all registers and any register may be accessed.

In standby, the condition of the REF/OSC circuitry is determined by bits R13, R14, and R15 in the R register per Figure 16. However, if REF_{out} = *static low* is selected, the internal feedback resistor is disconnected and the REF_{in} is inhibited when both PLL and PLL′ are placed in standby via the C register. Thus, the REF_{in} only presents a capacitive load. **Note**: PLL/PLL′ standby does not affect the other modes of the REF/OSC circuitry as determined by bits R13, R14, and R15 in the R register. The PLL′ standby mode (controlled from the C′ register) has no effect on the REF/OSC circuit.

When C6 is reset low, the associated PLL (or PLLs) is (are) taken out of standby in two steps. First, the REF_{in} (only in 1 mode, PLL/PLL′ in standby) resistor is reconnected, REF_{in} (only 1 mode) is gated on, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detectors. Second, when the appropriate f_R pulse occurs, the A and N counters are jam loaded, the prescaler is gated on, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C5, C4 – I2, I1: Independently controls the PD_{out} or PD_{out}' source/sink current per Table 2. With both bits high, the maximum current (as set by Rx or Rx′) is available. POR forces C5 and C4 to high levels.

C3 – Spare: Unused

C2 – PDA/B: Independently selects which phase/frequency detector is to be used. When set high, the double–ended detector is selected with outputs ϕ_R and ϕ_V or ϕ_R' and ϕ_V'. When reset low, the current source/sink detector is selected with outputs PD_{out} or PD_{out}'. In the second case, the appropriate Rx or Rx′ pin is tied to an external resistor. POR forces C2 low.

C1 – Port: When the Output A pin is selected as "Port" via bits A22 and A21, C1 of the C register determines the state of Output A. When C1 is set high, Output A is forced to the high–impedance state; C1 low forces Output A low. The Port bit is not affected by the standby mode. **Note**: C1 of the C′ register is not used in any mode.

C0 – POL: Selects the output polarity of the associated phase/frequency detectors. When set high, this bit inverts the associated current source/sink output and interchanges the associated double–ended output relative to the waveforms in Figure 17. Also, see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

Figure 14. C and C′ Register Accesses and Format (8 Clock Cycles are Used)

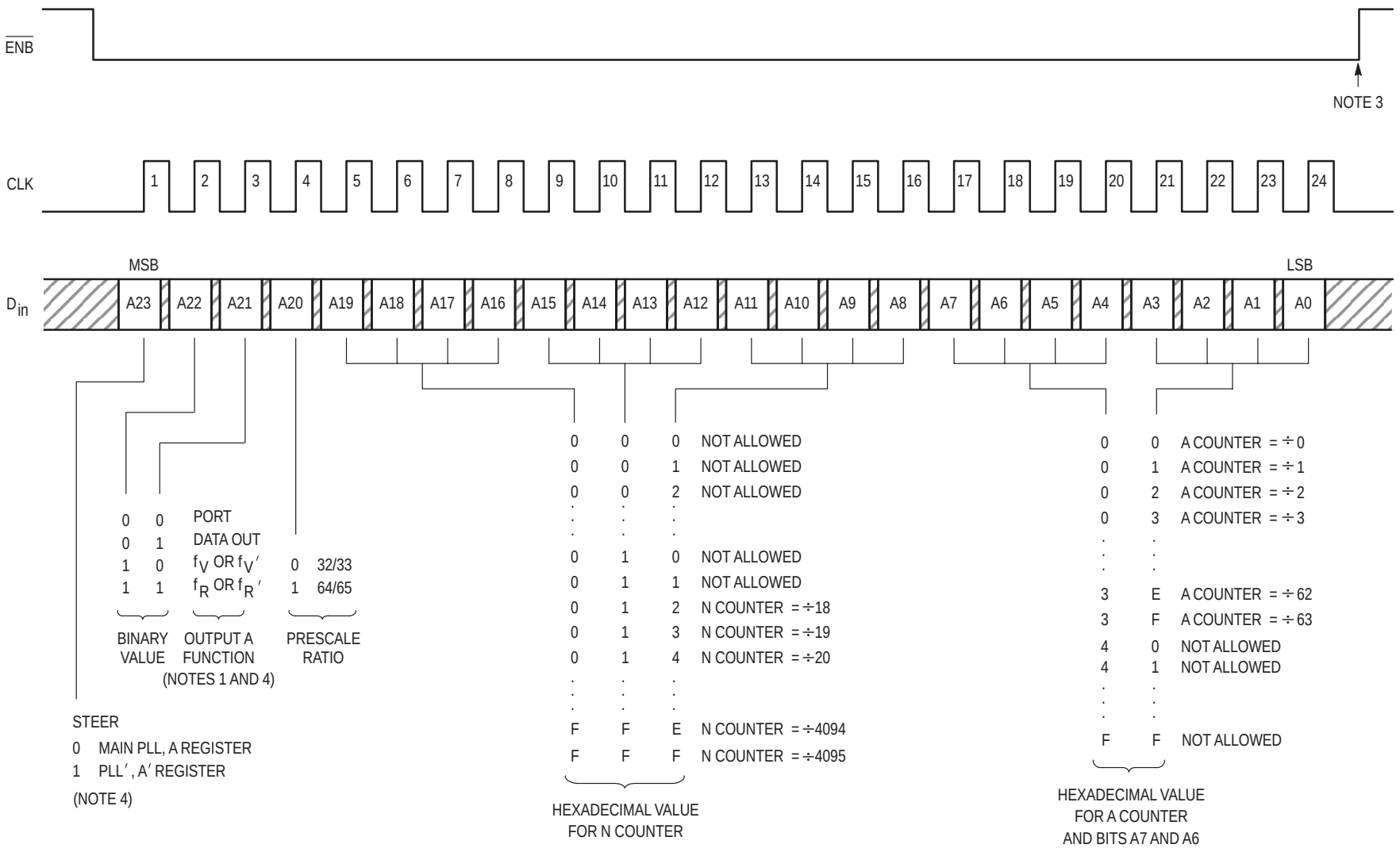
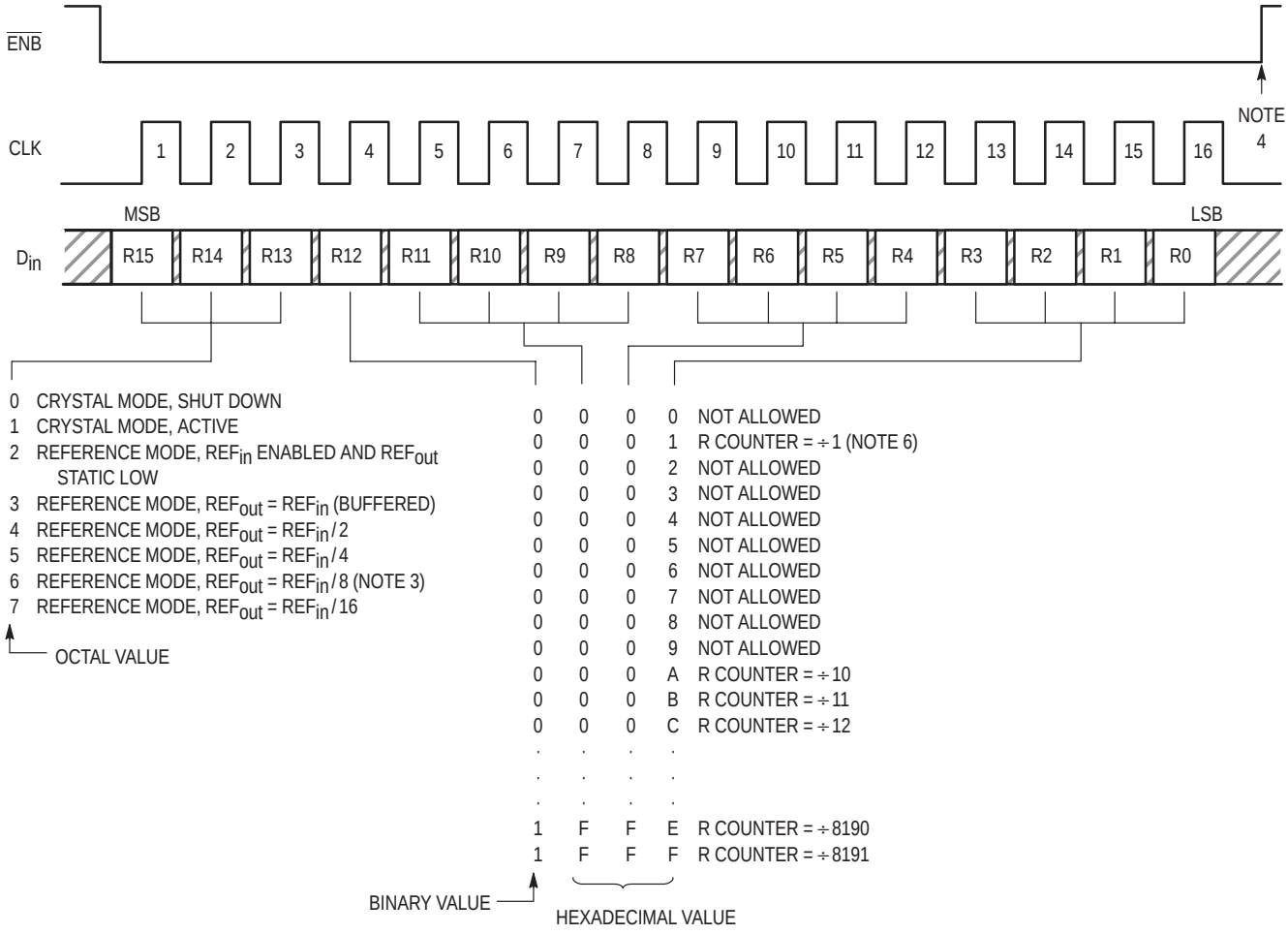


Figure 15. A and A′ Register Accesses and Format (24 Clock Cycles are Used)

NOTES:

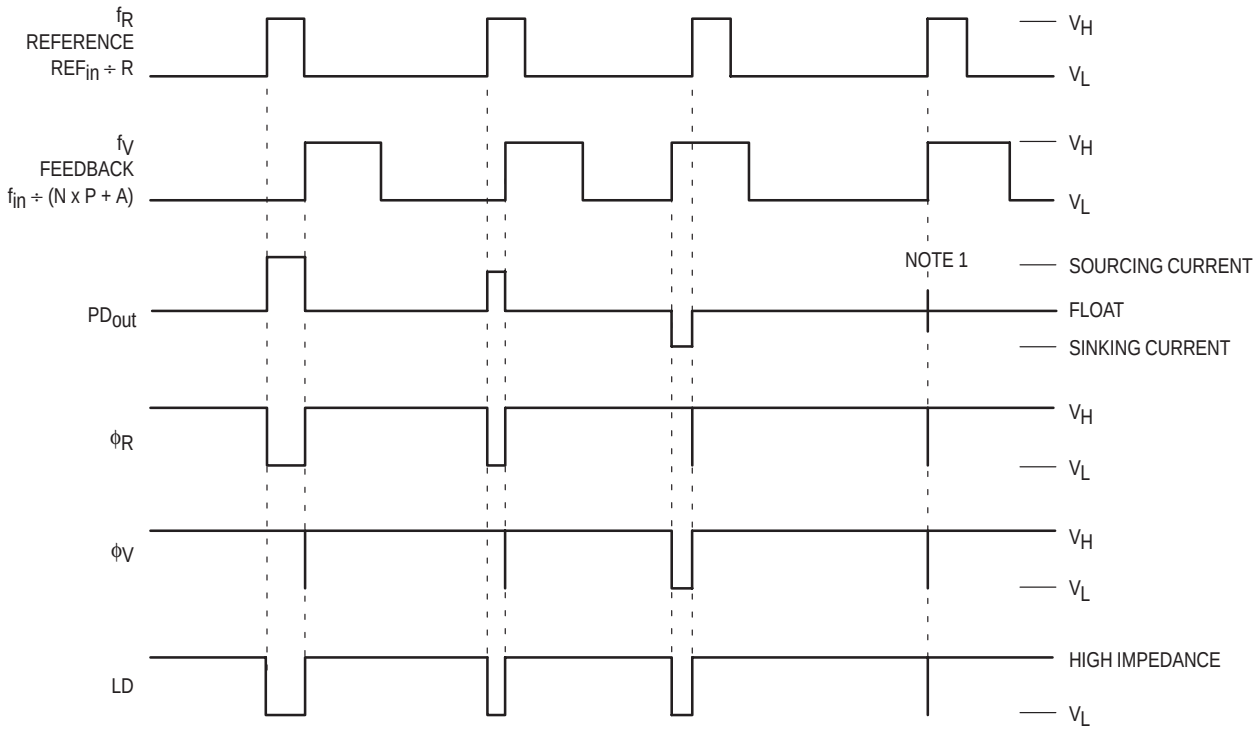
1. A power-on initialize circuit forces the Output A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x P + A where N is the value programmed for the N counter, P is 32 if bit A20 is low or 64 if A20 is high, and A is the value programmed for the A counter.
3. At this point, the three new bytes are transferred to the A register if bit A23 is a “0” or A′ register if A23 is a “1”. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register’s relative second buffer, Rs or Rs′. Thus, the R, N, and A (or R′, N′, and A′) counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C or C′ registers are not affected.
4. A “0” for the Steering bit allows selection of f_R, f_V, Data Out, or Port by bits A21 and A22. A “1” for the Steering bit allows selection of $f_{R'}$, $f_{V'}$, Data Out, or Port.



NOTES:

1. Bits R15 – R13 control the configurable “Buffer and Control” block (see Block Diagram).
2. Bits R12 – R0 control the “13–stage R counter” blocks (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the “Buffer and Control” block in the Block Diagram. Bits R0 – R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R or R′ counter divide ratio is not altered yet and retains the previous ratio loaded. The C, C′, A, and A′ registers are not affected.
5. Bits R0 – R12 are transferred to the second buffer of the R register (Rs in the Block Diagram) on a subsequent 24–bit write to the A register. The bits are transferred to Rs′ on a subsequent 24–bit write to the A′ register. The respective R counter begins dividing by the new ratio after completing the rest of its present count cycle.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 16. R Register Access and Format (16 Clock Cycles are Used)



NOTES:

1. At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.
2. The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is mostly in a floating condition and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.
3. V_H = High voltage level, V_L = Low voltage level.
4. The waveforms are applicable to both the main PLL and PLL′.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} must be used. See Figure 8.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in}. (See Figure 8.) For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance, C_L, which does not exceed approximately 20 pF when used near the highest operating frequency of the MC145220. Assuming R1 = 0 Ω, the shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

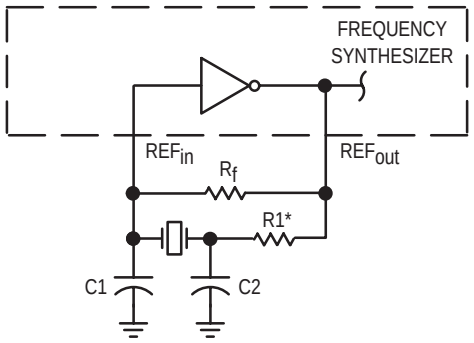
C_{in} = 5 pF (see Figure 19)
C_{out} = 6 pF (see Figure 19)
C_a = 1 pF (see Figure 19)
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making either a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes zero in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

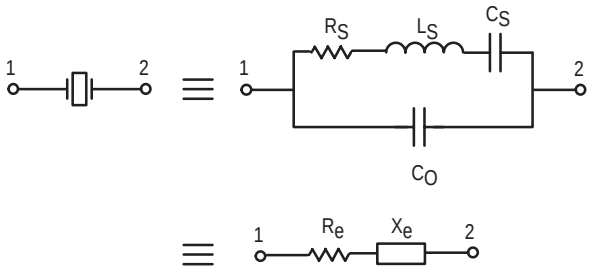
To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency (f_R) at Output A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. Note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 4.



* May be needed in certain cases. See text.

Figure 18. Pierce Crystal Oscillator Circuit



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 20. Equivalent Crystal Networks

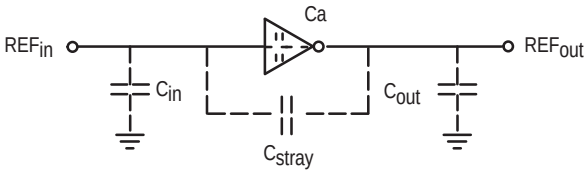


Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, “The Piezoelectric Crystal Unit – Definitions and Method of Measurement”, *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, “Quartz Crystals for Frequency Control”, *Electro–Technology*, June 1969.

P. J. Ottowitz, “A Guide to Crystal Selection”, *Electronic Design*, May 1966.

D. Babin, “Designing Crystal Oscillators”, *Machine Design*, March 7, 1985.

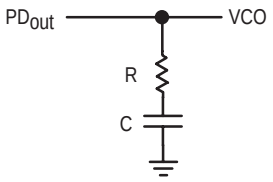
D. Babin, “Guidelines for Crystal Oscillator Design”, *Machine Design*, April 25, 1985.

Table 4. Partial List of Crystal Manufacturers

United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

(A)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

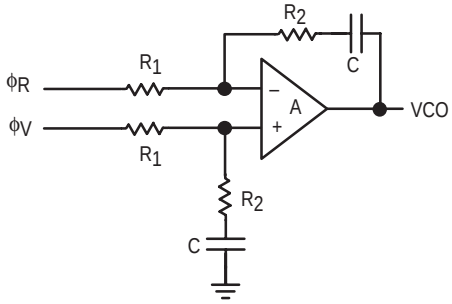
$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:

For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$Z(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:

For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V+/2\pi$ volts per radian for ϕ_V and ϕ_R

K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

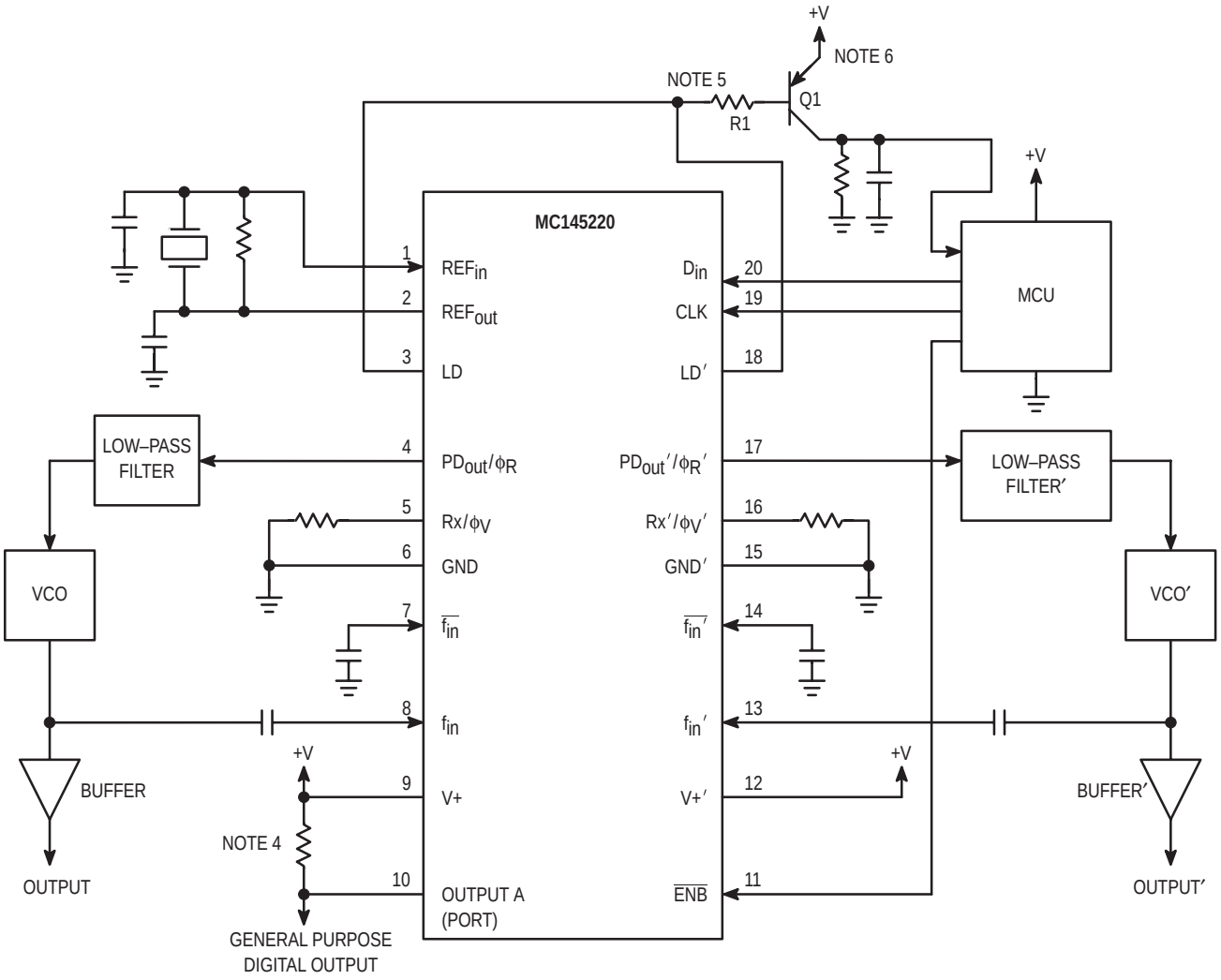
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.

Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

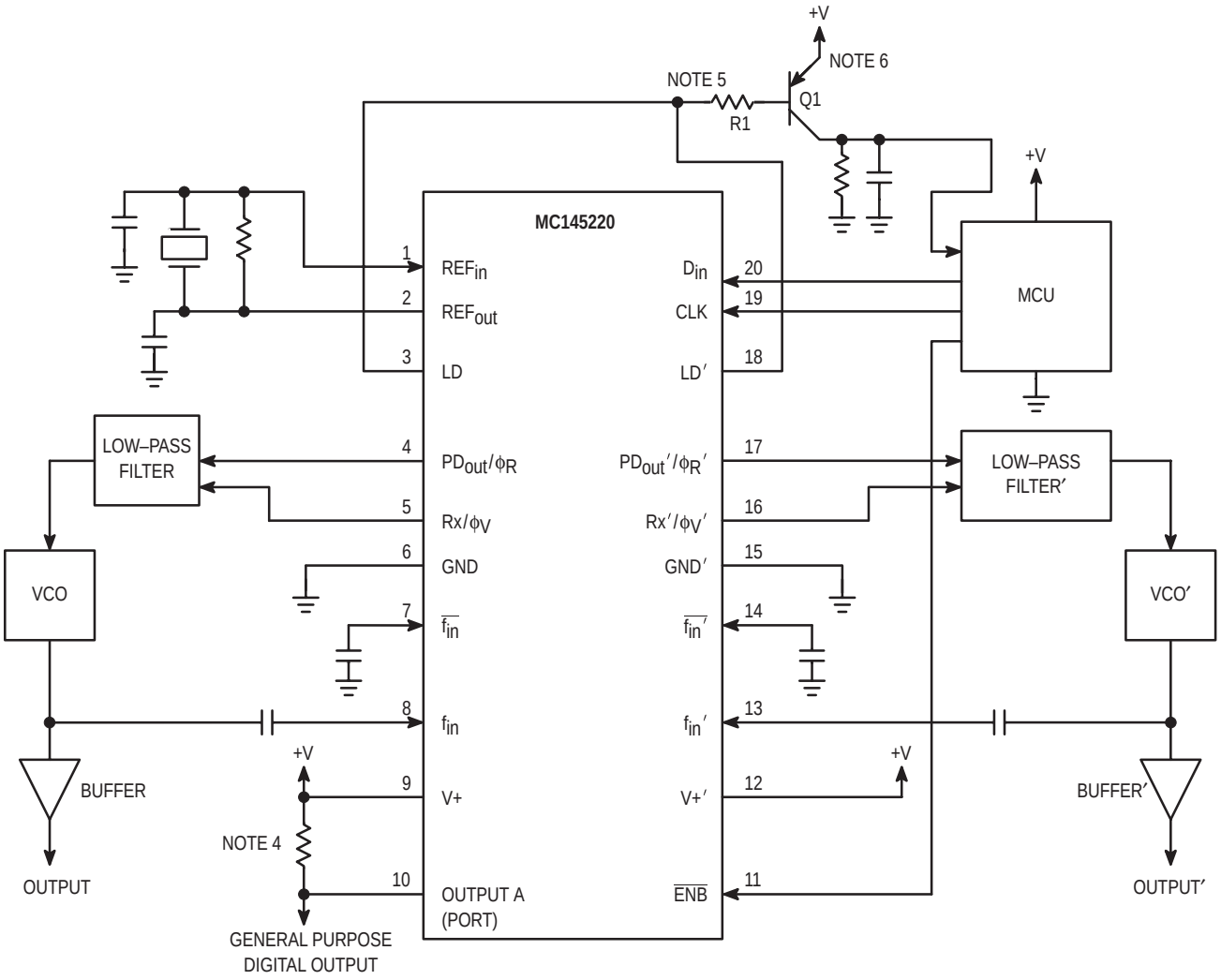
AN1253, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

1. The PD_{out} output is fed to an external loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. For optimum performance, bypass the V+ and V+′ pins to GND and GND′ with low–inductance capacitors.
3. The R counter is programmed for a divide value = REF_{in} /f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \bullet P + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively. P is the lower divide ratio of the dual–modulus prescaler (i.e., 32 or 64).
4. Pull–up voltage must be at the same potential as the V+ pin or less. Pull–up device other than a resistor may be used. (Pull–up device not required when Output A is configured as f_R, $f_R′$, f_V, $f_V′$, DATA OUT.)
5. LD and LD′ are open–drain outputs. This allows the wired–OR configuration shown. Note that R1 and Q1 form the “pull–up device”.
6. Use of Q1 is optional and depends on loading.

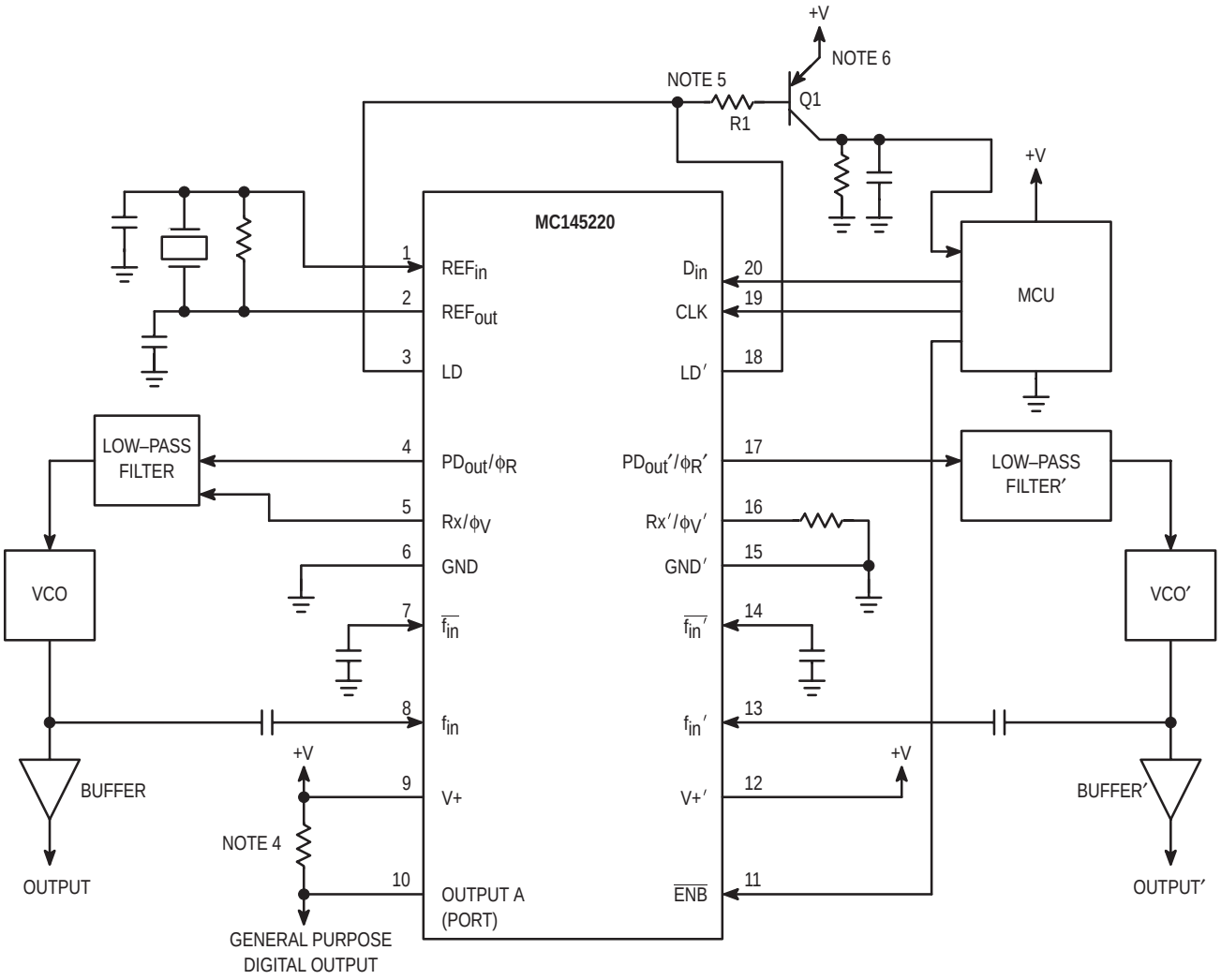
Figure 21. Application Showing Use of the Two Single–Ended Phase/Frequency Detectors



NOTES:

1. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.
2. For optimum performance, bypass the V+ and V+′ pins to GND and GND′ with low–inductance capacitors.
3. The R counter is programmed for a divide value = REF_{in} /f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \bullet P + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively. P is the lower divide ratio of the dual–modulus prescaler (i.e., 32 or 64).
4. Pull–up voltage must be at the same potential as the V+ pin or less. Pull–up device other than a resistor may be used. (Pull–up device not required when Output A is configured as f_R, $f_R′$, f_V, $f_V′$, DATA OUT.)
5. LD and LD′ are open–drain outputs. This allows the wired–OR configuration shown. Note that R1 and Q1 form the “pull–up device”.
6. Use of Q1 is optional and depends on loading.

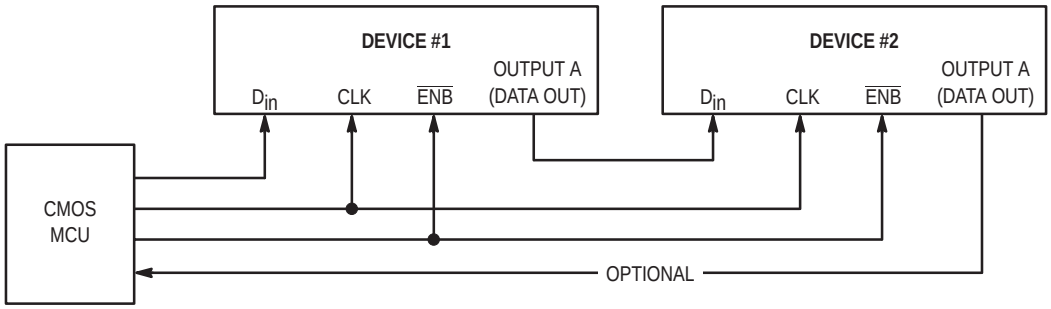
Figure 22. Application Showing Use of the Two Double–Ended Phase/Frequency Detectors



NOTES:

1. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. For optimum performance, bypass the V+ and V+′ pins to GND and GND′ with low–inductance capacitors.
3. The R counter is programmed for a divide value = REF_{in} /f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \bullet P + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively. P is the lower divide ratio of the dual–modulus prescaler (i.e., 32 or 64).
4. Pull–up voltage must be at the same potential as the V+ pin or less. Pull–up device other than a resistor may be used. (Pull–up device not required when Output A is configured as f_R, $f_R′$, f_V, $f_V′$, DATA OUT.)
5. LD and LD′ are open–drain outputs. This allows the wired–OR configuration shown. Note that R1 and Q1 form the “pull–up device”.
6. Use of Q1 is optional and depends on loading.

Figure 23. Application Showing Use of Both the Single– and Double–Ended Phase/Frequency Detectors



NOTE: See related Figures 25, 26, and 27.

Figure 24. Cascading Two Devices

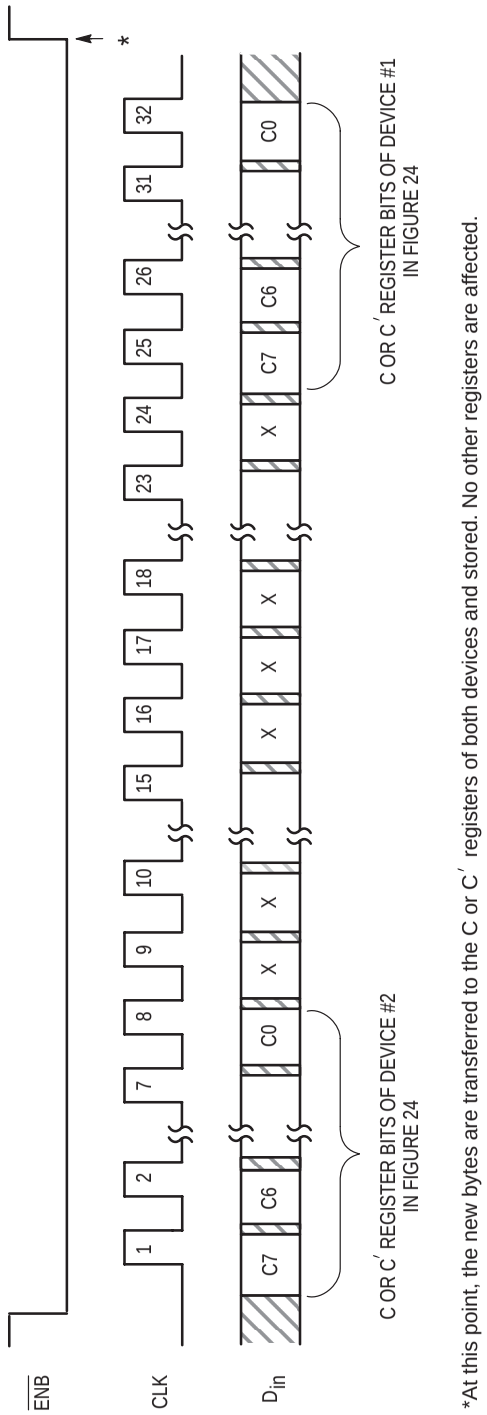
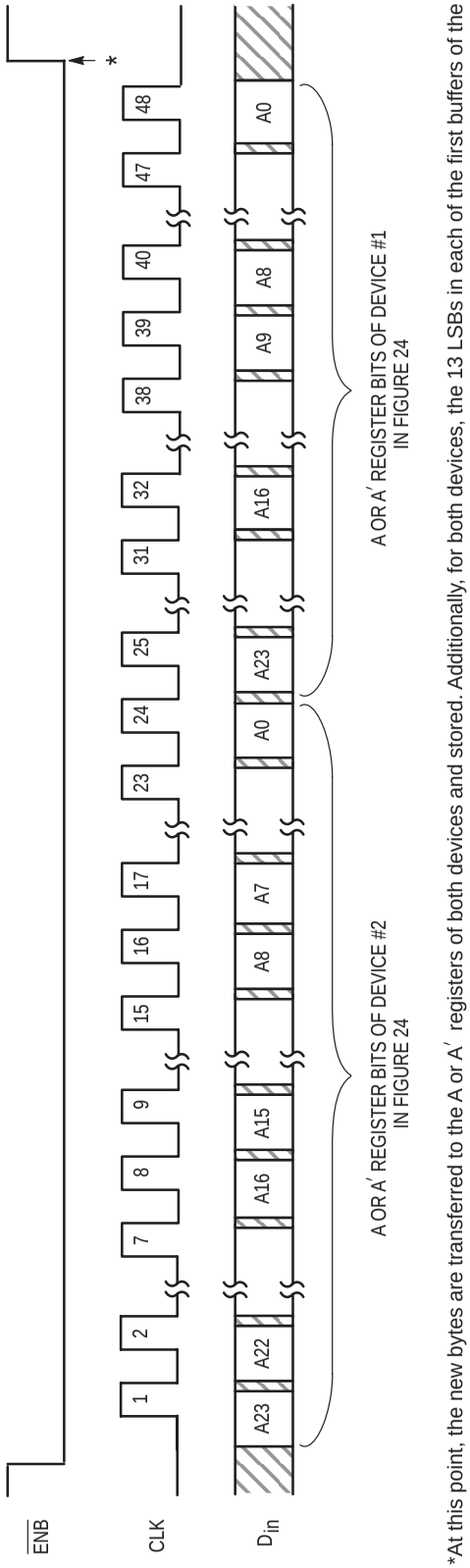
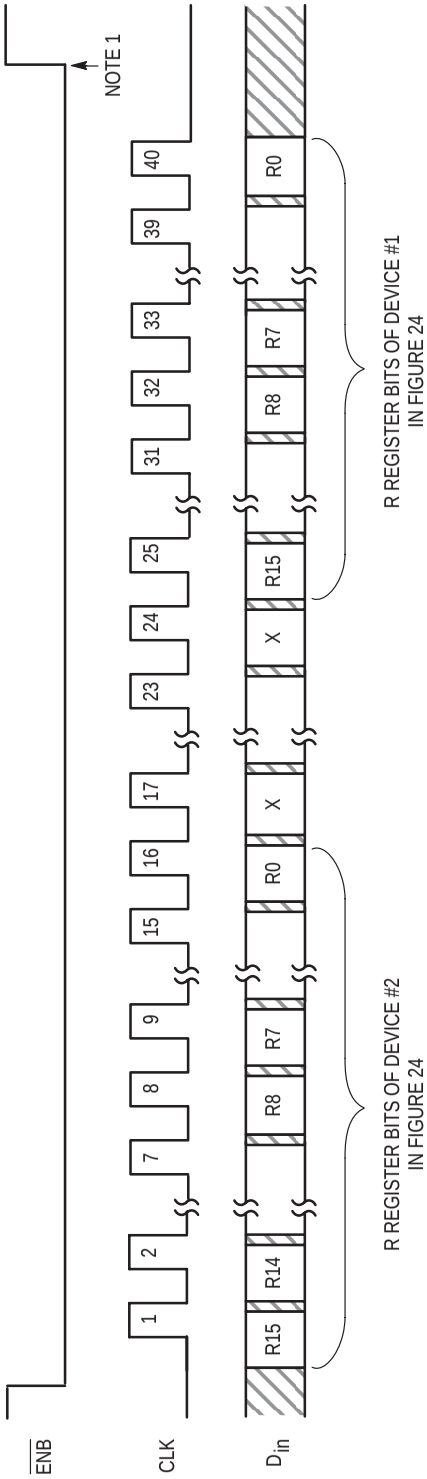


Figure 25. Accessing the C or C′ Registers of Two Cascaded MC145220 Devices (32 Clock Cycles are Used)



*At this point, the new bytes are transferred to the A or A′ registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R Registers are transferred to the respective R register's second buffer. Thus, the R, N, and A (R′, N′, and A′) counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. None of the C or C′ registers are affected.

Figure 26. Accessing the A or A′ Registers of Two Cascaded MC145220 Devices (48 Clock Cycles are Used)



NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14, and R15 are stored and sent to the Buffer and Control block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R and R′ counter divide ratios are not altered yet and retain the previous ratios loaded. The other registers are not affected.
2. See note of Figure 26 for the method of loading the second buffers in the R register to achieve new divide ratios.

Figure 27. Accessing the R Registers of Two Cascaded MC145220 Devices (40 Clock Cycles are Used)

MOTOROLA

Advance Information

Dual PLL Frequency Synthesizers with DACs and Voltage Multiplier

MC145225
MC145230

BiCMOS COMPONENT FOR 2 OR 3 VOLT SYSTEMS

SEMICONDUCTOR TECHNICAL DATA

The MC145225 and MC145230 are dual frequency synthesizers containing very–low supply voltage circuitry. These devices support two independent loops with a single input reference and operate down to 1.8 V. Phase noise reduction circuitry is incorporated into each device.

The MC145225 is capable of direct usage up to 1.2 GHz on the main loop and up to 550 MHz on the secondary loop. The MC145230 is capable of direct usage up to 2.2 GHz on the main loop and up to 550 MHz on the secondary loop. Each device has a 32/33 prescaler for the main loop and an 8/9 prescaler for the secondary loop. Lock detection circuitry for each loop is multiplexed to a single output.

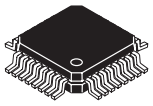
Two 8–bit DACs are powered through a dedicated pin. The DAC supply range is 1.8 to 3.6 V; this voltage may differ from the main supply.

An on–chip voltage multiplier supplies power to the phase/frequency detectors. Thus, in a 2 V application, the detectors are supplied with 4 V power. In 2.6 to 3.6 V applications, the multiplied voltage is regulated at approximately 5 V. The current source/sink phase/frequency detector for the main loop is designed to achieve faster lock times than a conventional detector. Both high and low current outputs are available along with a timer, double buffers, and a MOSFET switch to adjust the external low–pass filter response.

There are several levels of standby which are controllable with a 1–byte transfer through the serial port. Either of the PLLs and/or the reference oscillator may be independently placed in the low–power standby state. In addition, any of the phase/frequency detector outputs may be placed in the floating state to facilitate modulation of the external VCOs. Either DAC may be placed in standby via a 4–byte transfer.

- Operating Frequency
  MC145225 — Main Loop: 100 to 1200 MHz
  Secondary Loop: 50 to 550 MHz
  MC145230 — Main Loop: 500 to 2200 MHz
  Secondary Loop: 50 to 550 MHz
- Operating Supply Voltage: 1.8 to 3.6 V
- Nominal Supply Current, Both Loops Active — MC145225: 4 mA
  MC145230: 5 mA
- Maximum Standby Current, All Systems Shut Down: 10 μA
- Nominal Phase Detector Output Current:
  1.8 V Supply — PD_{out}–Hi: 2.8 mA, PD_{out}–Lo: 0.7 mA
  ≥ 2.5 V Supply — PD_{out}–Hi: 4.4 mA, PD_{out}–Lo: 1.1 mA
- Two Independent 8–Bit DACs with Separate Supply Pin (Up to 3.6 V)
- Lock Detect Output with Adjustable Lock Indication Window
- Independent R Counters Allow Independent Step Sizes for Each Loop
- Main Loop Divider Range: 992 to 262,143
- Secondary Loop Divider Range: 152 to 65,535
- Fractional Reference Counters Divider Range: 20 to 32,767.5
- Auxiliary Reference Divider with Small–Signal Differential Output — Ratios: 8, 10, 12.5
- Three General–Purpose Outputs
- Direct Interface to Motorola SPI Data Port Up to 10 Mbps

BitGrabber is a trademark of Motorola, Inc.



(Scale 2:1)

PLASTIC PACKAGE
CASE 873C
(LQFP–32, Tape & Reel Only)
VERY–SMALL 5 x 5 mm BODY

DEVELOPMENT SYSTEM

The MC145230EVK, which contains hardware and software, is strongly recommended for system development. (The user must provide the VCOs for evaluating the MC145181.) The software supports all features and modes of operation of the device. Up to four boards or devices can be controlled and the user is alerted to error conditions. The control program may be used with any board based on the MC145181, MC145225, or MC145230.

ORDERING INFORMATION

Device	Main/Secondary Loop Maximum Frequency	Package
MC145225FTAR2	1200/550 MHz	LQFP–32
MC145230FTAR2	2200/550 MHz	

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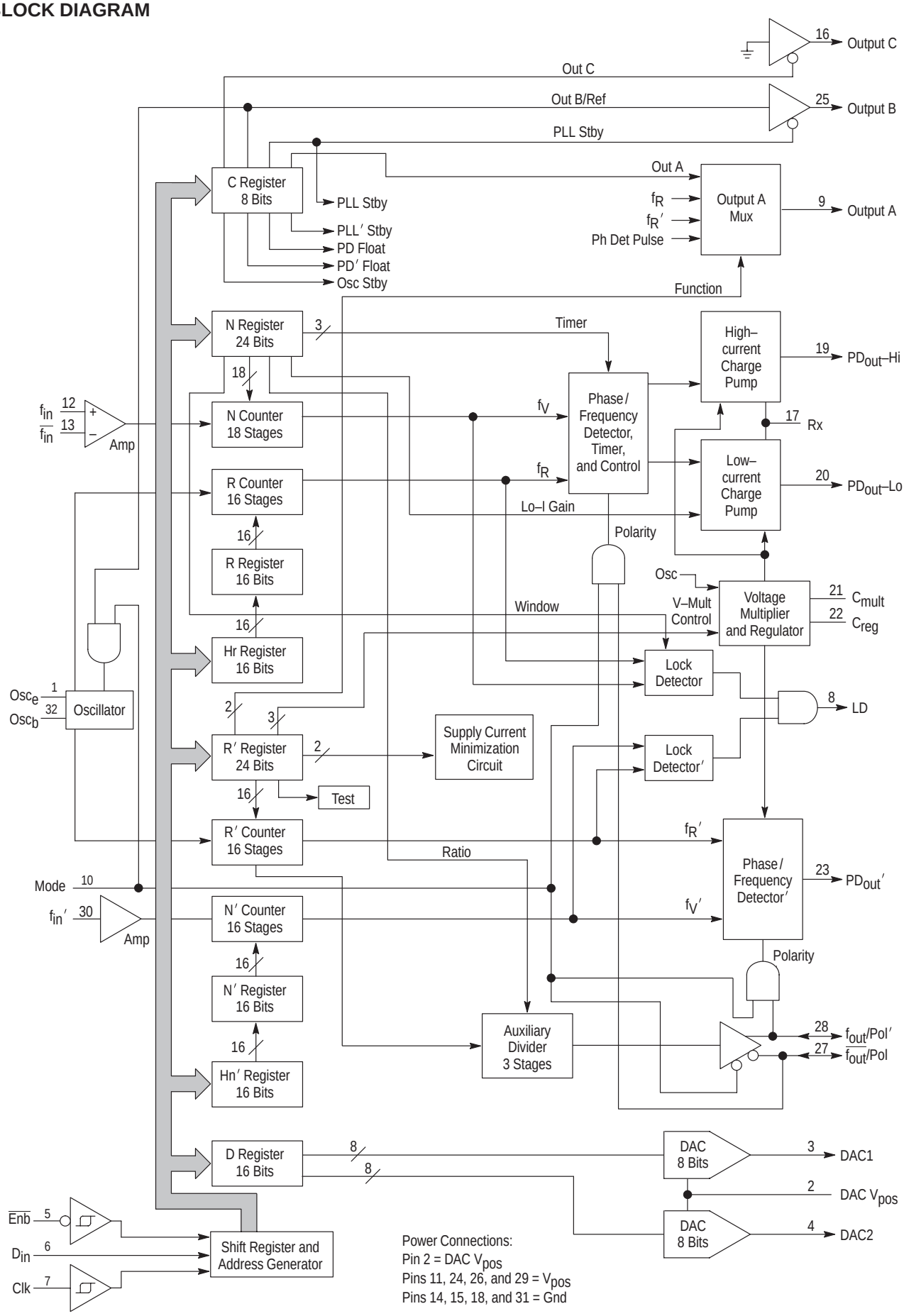
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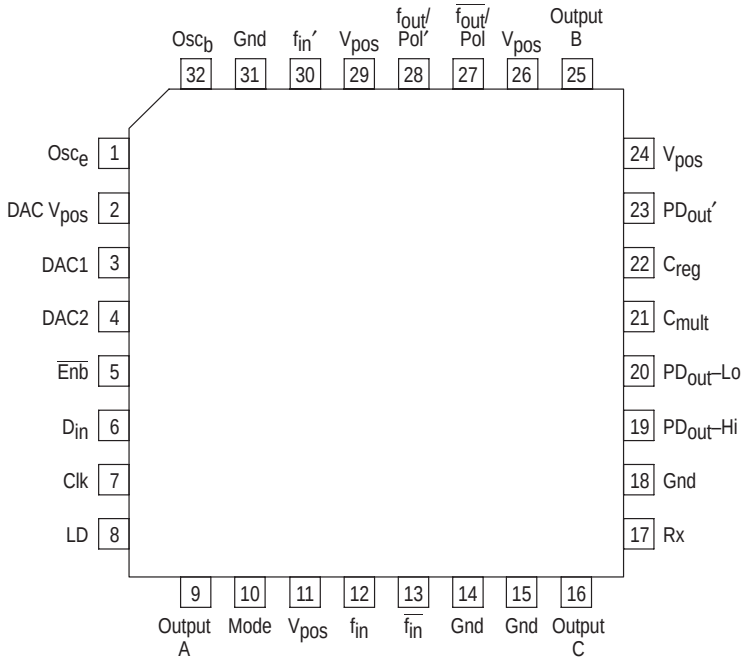
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1. BLOCK DIAGRAM



2. PIN CONNECTIONS



This device contains 15,260 active transistors.

3. PARAMETER TABLES

3A. MAXIMUM RATINGS (Voltages Referenced to Gnd, unless otherwise stated)

Parameter	Symbol	Value	Unit
DC Supply Voltages	V_{pos}, DAC V_{pos}	–0.5 to 3.6	V
DC Input Voltage — Osc_e, f_{in}, f_{in}', Mode, D_{in}, Clk, $\overline{Enb}$, f_{out}/Pol′, $\overline{f_{out}}$/Pol	V_{in}	–0.5 to V_{pos} + 0.5	V
DC Output Voltage	V_{out}	–0.5 to V_{pos} + 0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
DC Output Current, per Pin	I_{out}	±20	mA
DC Supply Current, V_{pos} and Gnd Pins	I	25	mA
Power Dissipation, per Package	P_D	100	mW
Storage Temperature	T_{stg}	–65 to 150	°C
Lead Temperature, 1 mm from Case for 10 Seconds	T_L	260	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.
2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) up to 2000 V. Additional ESD data available upon request.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

3B. DC ELECTRICAL CHARACTERISTICS

V_{pos} = 1.8 to 3.6 V, Voltages Referenced to Gnd, T_A = –40 to 85°C, unless otherwise statedt

Parameter	Condition	Symbol	Guaranteed Limit	Unit
Maximum Low–Level Input Voltage (D_{in}, Clk, $\overline{Enb}$, Mode, f_{out}/Pol', $\overline{f_{out}}/Pol$)	f_{out}/Pol' and $\overline{f_{out}}/Pol$ Configured as Inputs	V_{IL}	0.3 x V_{pos}	V
Minimum High–Level Input Voltage (D_{in}, Clk, $\overline{Enb}$, Mode, f_{out}/Pol', $\overline{f_{out}}/Pol$)	f_{out}/Pol' and $\overline{f_{out}}/Pol$ Configured as Inputs	V_{IH}	0.7 x V_{pos}	V
Minimum Hysteresis Voltage (Clk)		V_{Hys}	100	mV
Maximum Low–Level Output Voltage (LD, Output A, Output B)	I_{out} = 20 µA	V_{OL}	0.1	V
Minimum High–Level Output Voltage (LD, Output A, Output B)	I_{out} = –20 µA	V_{OH}	V_{pos} – 0.1	V
Minimum Low–Level Output Current (LD, Output A, Output B)	V_{out} = 0.3 V	I_{OL}	0.7	mA
Minimum High–Level Output Current (LD, Output A, Output B)	V_{out} = V_{pos} – 0.3 V	I_{OH}	–0.7	mA
Minimum Low–Level Output Current (Output C)	V_{out} = 0.2 V	I_{OL}	2.8	mA
Maximum Input Leakage Current (D_{in}, Clk, $\overline{Enb}$, Mode, f_{out}/Pol', $\overline{f_{out}}/Pol$)	V_{in} = V_{pos} or Gnd; f_{out}/Pol' and $\overline{f_{out}}/Pol$ Configured as Inputs	I_{in}	±1.0	µA
Maximum Output Leakage Current (Output B, Output C)	V_{out} = V_{pos} or Gnd; Output in High–Impedance State	I_{OZ}	±1	µA
Maximum ON Resistance (Output C)	1.8 V ≤ V_{pos} < 2.5 V Supply 2.5 V ≤ V_{pos} ≤ 3.6 V Supply	R_{on}	75 50	Ω
Maximum Standby Supply Current (V_{pos} and DAC V_{pos} Tied Together)	V_{in} = V_{pos} or Gnd; Outputs Open; Both PLLs in Standby Mode; Oscillator in Standby Mode; DAC1 and DAC2 Output = Zero; Keep–alive Oscillator Off (Notes 1, 2, and 3)	I_{STBY}	10	µA

NOTES: 1. The total supply current drain for the keep–alive oscillator, voltage multiplier, and regulator is approximately 250 µA.
2. When the Mode pin is tied high, bit C6 must be programmed to a 0 for minimum supply current drain. Otherwise, if C6 = 1, the current drain is approximately 8 µA for a 1.8 V supply and approximately 40 µA for a 3.6 V supply. This restriction on bit C6 does not apply when the Mode pin is tied low.
3. To ensure minimum standby supply current drain, the voltage potential at the C_{mult} pin must not be allowed to fall below the potential at the V_{pos} pins. See discussion in Section 5E under **C_{mult}**.

3C. PD_{out}–Hi AND PD_{out}–Lo PHASE/FREQUENCY DETECTOR CHARACTERISTICS

Nominal Output Current, V_{pos} = 1.8 V: PD_{out}–Hi = 2.8 mA, PD_{out}–Lo = 0.7 or 0.35 mA
Nominal Output Current, V_{pos} ≥ 2.5 V: PD_{out}–Hi = 4.4 mA, PD_{out}–Lo = 1.1 or 0.55 mA
Rx = 2.0 kΩ, Voltages Referenced to Gnd, Voltage Multiplier ON, T_A = –40 to 85°C

Parameter	Condition	Guaranteed Limit	Unit
Maximum Source Current Variation Part–to–Part (See Note)	V_{out} = 0.5 x V_{Cmult}	±14	%
Maximum Sink–versus–Source Mismatch (See Note)	V_{out} = 0.5 x V_{Cmult}	20	%
Output Voltage Range (See Note)	I_{out} Variation ≤ 27%	0.6 to V_{Cmult} – 0.6 V	V
Maximum Three–State Leakage Current	V_{out} = 0 or V_{Cmult}	±50	nA

NOTE: Percentages calculated using the following formula: (Maximum Value – Minimum Value) / Maximum Value.

3D. PD_{out}' PHASE/FREQUENCY DETECTOR CHARACTERISTICS

V_{pos} = 1.8 to 3.6 V, Voltages Referenced to Gnd, Voltage Multiplier ON, T_A = –40 to 85°C

Parameter	Condition	Guaranteed Limit	Unit
Minimum Low–Level Output Current	V_{out} = 0.3 V	0.3	mA
Minimum High–Level Output Current	V_{out} = V_{Cmult} – 0.3 V	–0.3	mA
Maximum Three–State Leakage Current	V_{out} = 0 or V_{Cmult}	±50	nA

3E. DAC CHARACTERISTICS

V_{pos} = 1.8 to 3.6 V, DAC V_{pos} = 1.8 to 3.6 V; T_A = –40 to 85°C

Parameter	Condition	Guaranteed Limit	Unit
Resolution		8	Bits
Maximum Integral Nonlinearity		±1	LSB
Maximum Offset Voltage from Gnd	No External Load	1	LSB
Maximum Offset Voltage from DAC V_{pos}	No External Load	2	LSB
Maximum Output Impedance	Over Entire Output Range, Including Zero Output (which is Low–power Standby)	130	kΩ
Maximum Standby Current	Zero Output, No External Load	(See I_{STBY} in Section 3B)	
Maximum Supply Current per DAC @ DAC V_{pos} pin	Except with Zero Output, No External Load	(DAC V_{pos}) / 36	mA

3F. VOLTAGE MULTIPLIER AND KEEP–ALIVE OSCILLATOR CHARACTERISTICS

Voltages Referenced to Gnd, T_A = –40 to 85°C

Parameter	Condition	Guaranteed Limit	Unit
Voltage Multiplier Output Voltage	5 MHz Refresh Rate, 100 μA Continuous Sourcing, Measured at C_{mult} pin V_{pos} = 1.8 V V_{pos} = 3.6 V	 3.32 to 3.78 4.75 to 5.35	V
Keep–alive Refresh Frequency	V_{pos} = 1.8 to 3.6 V	300 to 700	kHz

3G. DYNAMIC CHARACTERISTICS OF DIGITAL PINS

V_{pos} = 1.8 to 3.6 V, T_A = –40 to 85°C, Input $t_r = t_f$ = 10 ns, C_L = 25 pF

Parameter	Figure No.	Symbol	Guaranteed Limit	Unit
Serial Data Clk Frequency NOTE: Refer to Clk t_w Below	1	f_{clk}	dc to 10	MHz
Maximum Propagation Delay, $\overline{Enb}$ to Output A (Selected as General–Purpose Output)	2, 7	t_{PLH}, t_{PHL}	200	ns
Maximum Propagation Delay, $\overline{Enb}$ to Output B	2, 3, 7, 8	t_{PLH}, t_{PHL}, t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}	200	ns
Maximum Propagation Delay, $\overline{Enb}$ to Output C	4, 8	t_{PZL}, t_{PLZ}	200	ns
Maximum Output Transition Time, Output A; Output B with Active Pullup and Pulldown	2, 7	t_{TLH}, t_{THL}	75	ns
Minimum Setup and Hold Times, D_{in} versus Clk	5	t_{su}, t_h	30	ns
Minimum Setup, Hold, and Recovery Times, $\overline{Enb}$ versus Clk	6	t_{su}, t_h, t_{rec}	100	ns
Minimum Pulse Width, Inactive (High) Time, $\overline{Enb}$	6	t_w	*	cycles
Minimum Pulse Width, Clk	1	t_w	50	ns
Maximum Input Capacitance — D_{in}, CLK, $\overline{Enb}$		C_{in}	10	pF

*For Hr register access, the minimum limit is 20 Osc_e cycles.
For Hn′ register access, the minimum limit is 27 f_{in}′ cycles.
For N register access, the minimum limit is 20 Osc_e cycles + 99 f_{in} cycles.
When the timer is used for adapt, the minimum limit after the second N register access and before the next register access is the time–out interval + 99 f_{in} cycles.

Figure 1.

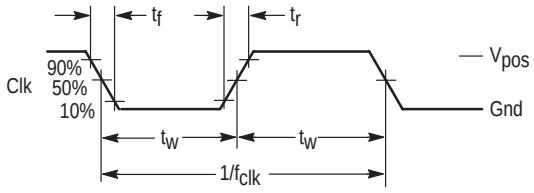


Figure 2.

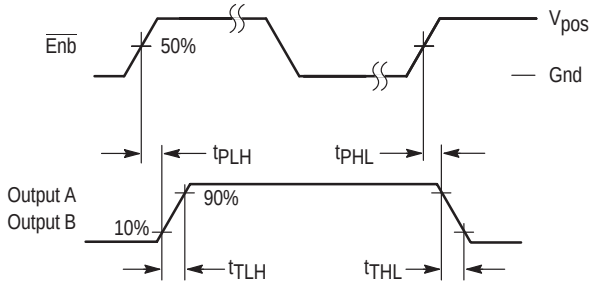


Figure 3.

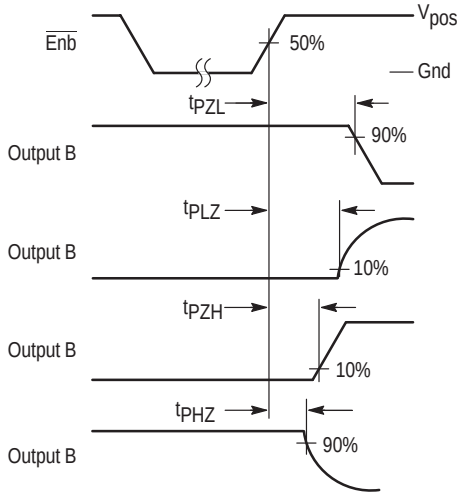


Figure 4.

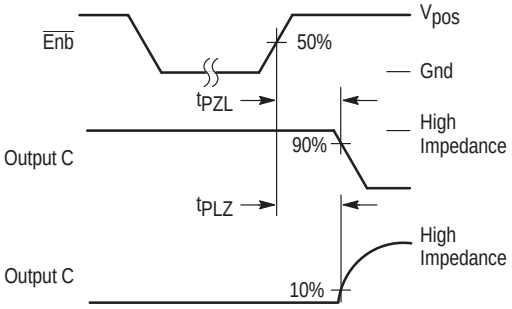


Figure 5.

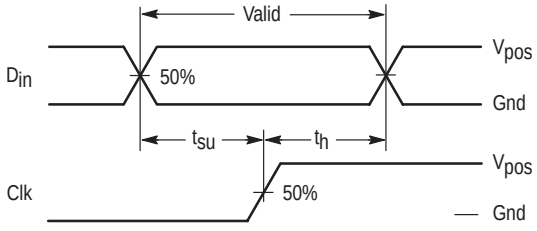


Figure 6.

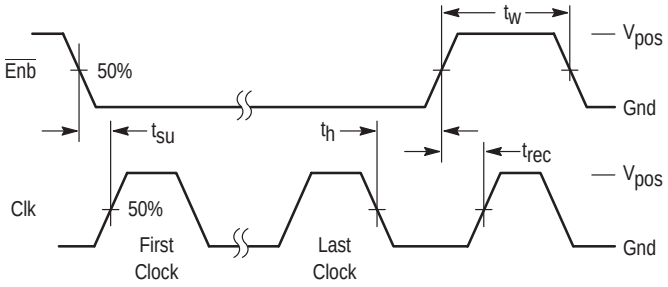
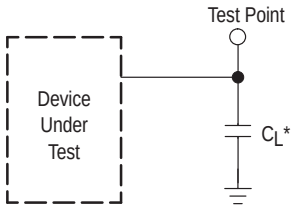
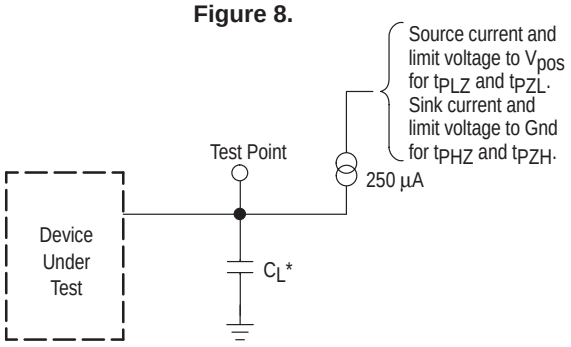


Figure 7.



* Includes all probe and fixture capacitance.

Figure 8.



* Includes all probe and fixture capacitance.

3H. DYNAMIC CHARACTERISTICS OF LOOP AND f_{out} PINS

V_{pos} = 1.8 to 3.6 V, T_A = –40 to 85°C

Symbol	Parameter	Condition	Figure No.	Min	Max	Unit
v_{in}	Input Voltage Range, f_{in}	MC145225: 100 MHz ≤ f_{in} < 400 MHz 400 MHz ≤ f_{in} ≤ 1.2 GHz MC145230: 500 MHz ≤ f_{in} < 800 MHz 800 MHz ≤ f_{in} ≤ 2.2 GHz	9	 300 100 200 100	 600 500 600 500	mVpp
v_{in}'	Input Voltage Range, f_{in}'	50 MHz ≤ f_{in} < 150 MHz 150 MHz ≤ f_{in} ≤ 550 MHz	10	400 175	600 600	mVpp
f_{Osce}	Input Frequency Range, Osc_e	v_{in} = 350 to 600 mVpp, Device in External Reference Mode	11	9	80	MHz
f_{Xtal}	Crystal Frequency, Osc_b and Osc_e	Device in Crystal Mode	*	9	80	MHz
C_{in}	Input Capacitance of Pins Osc_b and Osc_e			—	—	pF
f_{out}	Output Frequency Range, f_{out} and $\overline{f_{out}}$	Output Signal Swing > 300 mVpp per pin (600 mVpp differential)	12	1	6.2	MHz
f_ϕ	Operating Frequency Range of the Phase/Frequency Detectors, PD_{out}–Hi, PD_{out}–Lo, PD_{out}'			dc	600	kHz

* Refer to the **Crystal Oscillator Considerations** section.

Figure 9.

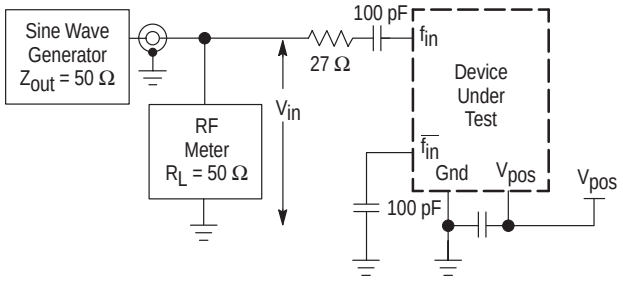


Figure 10.

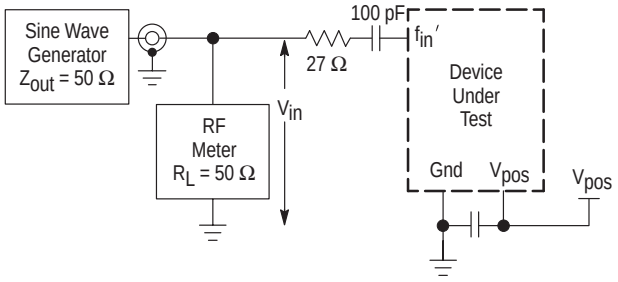


Figure 11.

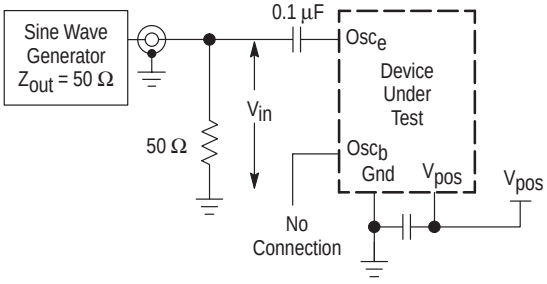
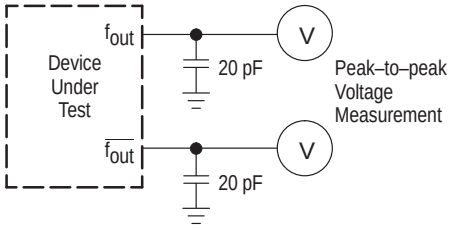


Figure 12.



4. DEVICE OVERVIEW

Refer to the Block Diagram in Section 1.

4A. SERIAL INTERFACE AND REGISTERS

The serial interface is comprised of a Clock pin (Clk), a Data In pin (D_{in}), and an Enable pin ($\overline{Enb}$). Information on the data input pin is shifted into a shift register on the low–to–high transition of the serial clock. The data format is most significant bit (MSB) first. Both Clk and $\overline{Enb}$ are Schmitt–triggered inputs.

The R and N registers contain counter divide ratios for the main loop, PLL. The R′ and N′ registers contain counter divide ratios for the secondary loop, PLL′. Additional contol bits are located in the R′, N, and C registers. The D register controls the digital–to–analog converters (DACs). Random access is allowed to the N, R′, Hr, Hn′, D, and C registers.

Two 16–bit holding registers, Hr and Hn′, feed registers R and N′, respectively. The R and N′ registers determine the divide ratios of the R and N′ counters, respectively. Thus, the information presented to the R and N′ counters is double–buffered. Using the proper programming sequence, new divide ratios may be presented to the N, R, and N′ counters; simultaneously.

$\overline{Enb}$ is used to activate the data port and allow transfer of data. To ensure that data is accepted by the device, the $\overline{Enb}$ signal line must initially be a high voltage (not asserted), then make a transition to a low voltage (asserted) prior to the occurrence of a serial clock, and must remain asserted until after the last serial clock of the burst. Serial data may be transferred in an SPI format (while $\overline{Enb}$ remains asserted). Data is transferred to the appropriate register on the rising edge of $\overline{Enb}$ (see Table 1). “Short shifting”, depicted as BitGrabber™ in the table, allows access to certain registers without requiring address bits. When $\overline{Enb}$ is inactive (high), Clk is inhibited from shifting the shift register.

The serial input pins may NOT be driven above the supply voltage applied to the V_{pos} pins.

4B. REFERENCE INPUT AND COUNTERS CIRCUITS

Reference (Oscillator) Circuit

For the Colpitts reference oscillator, one pin ties to the base (Osc_b, pin 32) and the other ties to the emitter (Osc_e, pin 1), of an on–chip NPN transistor. In addition, the reference circuit may be operated in the external reference (XRef) mode as selectable via bit C6 when the Mode pin is high.

The Osc_b and Osc_e pins support an external fundamental or overtone crystal. The output of the oscillator is routed to both the reference counter for the main loop (R counter) and the reference counter for the secondary loop (R′ counter).

In a second mode, determined by bit C6 being 1 and the Mode pin being high, Osc_e is an input which accepts an ac–coupled signal from a TCXO or other source. Osc_b must be floated. If the Mode pin is low, this “XRef mode” is not allowed.

Reference Counter for Main Loop

Main reference counter R divides down the frequency at Osc_e and feeds the phase/frequency detector for the main loop. The detector feeds the two charge pumps with outputs PD_{out}–Hi and PD_{out}–Lo. The division ratio of the R counter is determined by bits in the R register.

Reference Counter for Secondary Loop

Secondary reference counter R′ divides down the frequency at Osc_e and feeds the phase/frequency detector for the secondary loop. The detector output is PD_{out}′. The division ratio of the R′ counter is determined by the 16 LSBs of the R′ register.

The R′ counter has a special mode to provide a frequency output at pins f_{out} and $\overline{f_{out}}$ (differential outputs). These are low–jitter ECL–type outputs. With the Mode pin low, software control allows the Osc_e frequency to be divided–by–8, –10, or –12.5 and routed to the f_{out} pins. This output is derived by tapping off of a front–end stage of the R′ counter and feeding the auxiliary counter which provides the divided–down frequency. The chip must have the Mode pin low, which activates the f_{out} pins. The actual R′ divide ratio must be divisible by 2 or 2.5 when the f_{out} pins are activated. There is no such restriction when the Mode pin is high. See Section 6D, **R′ Register.**

4C. LOOP DIVIDER INPUTS AND COUNTER CIRCUITS

f_{in} Inputs and Counter Circuit

f_{in} and $\overline{f_{in}}$ are high–frequency inputs to the amplifier which feeds the N counter. A small signal can feed these inputs either differentially or single–ended.

The N counter divides down the external VCO frequency for the main loop. (The divide ratio of the N counter is also known as the loop multiplying factor.) The divide ratio of this counter is determined by the 18 LSBs of the N register. The output of the N counter feeds the phase/frequency detector for the main loop.

f_{in}′ Input and Counter Circuit

f_{in}′ is the high–frequency input to the amplifier which feeds the N′ counter. A small signal can feed this input single–ended.

The N′ counter divides down the external VCO frequency for the secondary loop. (The divide ratio of the N′ counter is also known as the loop multiplying factor.) The divide ratio of this counter is determined by bits in the N′ register. The output of the N′ counter feeds the phase/frequency detector for the secondary loop.

4D. VOLTAGE MULTIPLIER AND KEEP–ALIVE CIRCUITS

The voltage multiplier produces approximately two times the voltage present at the V_{pos} pins over a supply range of 1.8 V to about 2.5 V. With a supply range of approximately 2.5 V to 3.6 V, the elevated voltage is regulated/limited to approximately 5 V. The elevated voltage, present at the C_{mult} pin, is applied to both phase detectors. An external capacitor to Gnd is required on the C_{mult} pin. The other capacitors required for the multiplier are on–chip.

A capacitor to Gnd is also required on the C_{reg} pin. The voltage on this pin is equal to the voltage on the V_{pos} pins over a supply range of 1.8 V to about 2.5 V. The voltage on

C_{reg} is limited to approximately 2.5 V maximum when the V_{pos} pins exceed 2.5 V.

The refresh rate determines the repetition rate that the capacitors for the voltage multiplier are charged. Refresh is normally derived off of the signal present at the Osc_e pin, through a divider which is part of the voltage multiplier and regulator circuitry. The refresh rate is controlled via bits in the R′ register.

When the reference oscillator circuit is placed in standby, an on–chip keep–alive oscillator assists in maintaining the elevated voltage on the phase detectors. The keep–alive refresh rate is per the spec table in Section 3F.

If desired, the keep–alive oscillator can be inhibited from turning on, by placing the multiplier in the inactive state via R′ register bits. This causes the phase/frequency detector voltage to bleed off while in standby, but has the advantage of achieving the lowest supply current if all other sections of the chip are shut down.

4E. PHASE/FREQUENCY DETECTORS

Detector for Main Loop

The detector for the main loop senses the phase and frequency difference between the outputs of the R and N counters. The detector feeds both a high–current charge pump with output PD_{out}–Hi and a low–current charge pump with output PD_{out}–Lo.

The charge pumps can be operated in three conventional manners as controlled by bits in the N register. PD_{out}–Lo can be enabled with PD_{out}–Hi inhibited. Conversely, PD_{out}–Hi can be enabled with PD_{out}–Lo inhibited. Both outputs can be enabled and tied together externally for maximum charge pump current. Finally, both outputs can be inhibited. In this last case, they float. The outputs can also be forced to the floating state by a bit in the C register. This facilitates introduction of modulation into the VCO input.

The charge pumps can be operated in an adapt mode as controlled by bits in the N register. The bits essentially program a timer which determines how long PD_{out}–Hi is active. After the time–out, PD_{out}–Hi floats and PD_{out}–Lo becomes active. In addition, a second set of R and N counter values can be engaged after the time–out. For more information, see Table 16 and Section 8, **Programmer's Guide**.

Detector for Secondary Loop

The detector for the secondary loop senses the phase and frequency difference between the outputs of the R′ and N′ counters. Detector output PD_{out}′ is a voltage–type output with a three–state push–pull driver.

The output can be forced to the floating state by a bit in the C register. This facilitates introduction of modulation into the VCO input.

4F. LOCK DETECTORS

Window counters in each of the lock detector circuits determine the lock detector phase threshold for PLL and PLL′. The window counter divide ratio for the main loop's lock detector is controlled via a bit in the N register. The window counter divide ratio for the secondary loop is not controllable by the user.

The lock detector window determines a minimum phase difference which must occur before the Lock Detect pin goes high. Note that the lock detect signals for each loop drive an AND gate, which then feeds the LD pin. The LD pin indicates the condition of both loops, or the one active loop if the other is in standby. If both loops are in standby, LD is low indicating unlocked.

4G. DACs

The two independent 8–bit DACs facilitate crystal oscillator trimming and PA output power control. They are also suitable for any general–purpose use.

Each DAC utilizes an R–2R ladder architecture. The output pins, DAC1 and DAC2, are directly connected to the ladder; that is, there is no on–chip buffer.

The DAC outputs are determined by the contents of the D register. When a DAC output is zero scale, it is also in a low–power mode. The power–on reset (POR) circuit initializes the DACs in the low–power mode upon power up.

4H. GENERAL–PURPOSE OUTPUTS

There are three outputs which may be used as port expanders for a microcontroller unit (MCU).

Output A is actually a multi–purpose output with a push–pull output driver. See Table 2 for details.

Output B is a three–state output. The state of Output B depends on two bits; one of these bits also controls whether the main PLL is in standby or not. See Table 5 for details.

Output C is an open–drain output. The state of this output is controlled by one bit per Table 4. Output C is specified with a guaranteed ON resistance, and thus, may be used in an analog fashion.

5. PIN DESCRIPTIONS

5A. DIGITAL PINS

$\overline{Enb}$, D_{in}, and Clk
Pins 5, 6, and 7 — Serial Data Port Inputs

The $\overline{Enb}$ input is used to activate the serial interface to allow the transfer of data to the device. To transfer data to the device, the $\overline{Enb}$ pin must be low during the interval that the data is being clocked in. When $\overline{Enb}$ is taken back high (inactive), data is transferred to the appropriate register depending either on the data stream length or address bits. The C, Hr, and N registers can be accessed using either a unique data stream length (BitGrabber) or by using address bits (Conventional). The D, Hn′, and R′ registers can only be accessed using address bits. See Table 1.

The bit stream begins with the MSB and is shifted in on the low–to–high transition of Clk. The bit pattern is 1 byte (8 bits) long to access the C register, 2 bytes (16 bits) to access the Hr register, or 3 bytes (24 bits) to access the N register. A bit pattern of 4 bytes (32 bits) is used to access the registers when using address bits. The device has double buffers for storage of the N′ and R counter divide ratios. One double buffer is composed of the Hr register which feeds the R register. An Hr to R register transfer occurs whenever the N register is written. The other double buffer is the Hn′ register which feeds the N′ register. An Hn′ to N′ register transfer occurs whenever the N register is written. Thus, new divide ratios may be presented to the R, N′, and N counters simultaneously.

Transitions on $\overline{Enb}$ must not be attempted while Clk is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs whenever $\overline{Enb}$ is high (inactive) and Clk is low.

Data is retained in the registers over a supply range of 1.8 to 3.6 V. The bit–stream formats are shown in Figures 13 through 18.

LD
Pin 8 — Lock Detectors Output

This signal is the logical AND of the lock detect signals from both PLL and PLL′. For the main PLL, the phase window that defines “lock” is programmable via bit N22. The phase window for the secondary PLL′ is not programmable.

If either PLL or PLL′ is in standby, LD indicates the lock condition of the active loop only. If both loops are in standby, the LD output is a static low level.

Each PLL’s lock detector is in the high state when the respective loop is locked (the inputs to the phase detector being the same phase and frequency). The lock detect signal is in the low state when a loop is out of lock. See Figure 19.

Upon power up, the LD pin indicates a *not locked* condition. The LD pin is a push–pull CMOS output. If unused, LD should be left open.

Output A
Pin 9 — Multiple–Purpose Digital Output

Depending on control bits R′21 and R′20, Output A is selectable by the user as a general–purpose output (either high or low level), f_R (output of main reference counter), $f_{R'}$ (output of secondary reference counter), or a phase detector pulse indicator for both loops. When selected as general–purpose output, bit C7 determines whether the output is a high or low level per Table 2. When configured as f_R, $f_{R'}$, or phase detector pulse, Output A appears as a normally low signal and pulses high.

Output A is a slew–rate limited CMOS totem–pole output. If unused, Output A should be left open.

Table 1. Register Access
(LSBs are C0, R0, N0, D0, R′0, and N′0)

Access Type	Accessed Register	Address Nibble	Number of Clocks	Register Bit Nomenclature	Figure No.
BitGrabber	C	—	8	C7, C6, C5, ..., C0	13
BitGrabber	Hr	—	16	R15, R14, R13, ..., R0	14
BitGrabber	N	—	24	N23, N22, N21, ..., N0	15
Conventional	C	$0	32	C7, C6, C5, ..., C0	13
Conventional	Hr	$1	32	R15, R14, R13, ..., R0	14
Conventional	N	$2	32	N23, N22, N21, ..., N0	15
Conventional	D	$3	32	D15, D14, D13, ..., D0	18
Conventional	R′	$5	32	R′23, R′22, R′21, ..., R′0	16
Conventional	Hn′	$4	32	N′15, N′14, N′13, ..., N′0	17

NOTE: $0 denotes hexadecimal zero, $1 denotes hexadecimal one, etc.

Table 2. Output A Configuration

Bit R′21	Bit R′20	Bit C7	Function of Output A
0	0	0	General–Purpose Output, Low Level
0	0	1	General–Purpose Output, High Level
0	1	x	f_R
1	0	x	$f_{R'}$
1	1	x	Phase Detector Pulse Indicator

Mode
Pin 10 — Mode Input

When the Mode pin is tied low (approximately Gnd), the pair of pins named f_{out}/Pol′ and $\overline{f_{out}}$/Pol become outputs f_{out} and $\overline{f_{out}}$. As such, these pins are the divided down reference frequency. The division ratio is controlled by bits per Table 6. In addition, when Mode is low, the R′ counter is preceded by a fixed–divide prescaler. Also, only a crystal may be used at pins Osc_b and Osc_e; an external reference, such as a TCXO, should not be used to drive either pin. The default on the phase detector polarity is positive. See the summary in Table 3.

When the Mode pin is tied high (approximately V_{pos}), the pair of pins named f_{out}/Pol′ and $\overline{f_{out}}$/Pol become inputs Pol′ and Pol. As such, these pins control the polarity of the phase/frequency detectors for PLL′ and PLL, respectively. In addition, when Mode is high, the R′ counter is preceded by a dual–modulus prescaler. Therefore, the R′ counter is completely programmable per Figure 16. Also, either a crystal or TCXO may be used with the device. See the summary in Table 3.

Table 3. Mode Pin Summary

Attribute	Mode Pin = Low Level	Mode Pin = High Level
f_{out}/Pol′ pin	Pin is f_{out} output; polarity of phase detector′ is positive	Pin is Pol′ input and controls polarity of phase detector′
$\overline{f_{out}}$/Pol pin	Pin is $\overline{f_{out}}$ output; polarity of phase detector is positive	Pin is Pol input and controls polarity of phase detector
Oscillator circuit	Supports a crystal only	Supports crystal or accommodates TCXO
R′ counter	Programmable in increments of 2 or 2.5	Programmable in increments of 0.5
Output B pin	State of pin controlled by Bit C6	Pin not used, Bit C6 controls whether crystal or TCXO is accommodated

Output C
Pin 16 — General–Purpose Digital Output

This pin is controllable by bit C5 as either low level or high impedance per Table 4.

The output driver is an open–drain N–channel MOSFET connected to Gnd. The ESD (electrostatic discharge) protection circuit for this pin is tied to Gnd and V_{pos}. Thus, voltages above V_{pos} are clipped at approximately 0.7 V above V_{pos}. If unused, Output C should be left open.

Table 4. Output C Programming

Bit C5	State of Output C Pin
0	Low level (ON resistance per Electrical Table)
1	High impedance (leakage per Electrical Table)

Output B
Pin 25 — General–Purpose Digital Output

This pin is controllable by bits C6 and C1 as either low level, high level, or high impedance per Table 5. Note that whenever the main PLL is placed in standby by bit C1, Output B is forced to high impedance. The three–state MOSFET output is slew–rate limited. If unused, Output B should be left open.

Table 5. Output B Programming

Bit C6	Bit C1	State of Output B Pin	Condition of Main PLL
0	0	Low level	Active
0	1	High impedance*	Standby*
1	0	High level	Active
1	1	High impedance	Standby

*Power–up default.

f_{out}/Pol′ and $\overline{f_{out}}$/Pol
Pins 28 and 27 — Dual–purpose Outputs/Inputs

These pins are outputs when the Mode pin is low and inputs when the Mode pin is high.

When the Mode pin is low, these pins are small–signal differential outputs f_{out} and $\overline{f_{out}}$ with a frequency derived from the signal present at the Osc_e pin. The frequency of the output signal is per Table 6. If this function is not needed, the Mode pin should be tied high, which minimizes supply current. In this case, these inputs must be tied high or low per Tables 7 and 8.

Table 6. f_{out} and $\overline{f_{out}}$ Frequency
(Mode Pin = Low)

Bit N23	Bit R′1	Bit R′0	Output Frequency
0	0	0	Osc_e divided by 10
0	0	1	Osc_e divided by 12.5
0	1	0	Osc_e divided by 12.5
0	1	1	Osc_e divided by 12.5
1	0	0	Osc_e divided by 8
1	0	1	Osc_e divided by 10
1	1	0	Osc_e divided by 10
1	1	1	Osc_e divided by 10

When the Mode pin is high, these pins are digital inputs Pol′ and Pol which control the polarity of the phase/frequency detectors. See Tables 7 and 8. Positive polarity is used when an increase in an external VCO control voltage input causes an increase in VCO output frequency. Negative polarity is used when a decrease in an external VCO control voltage input causes an increase in VCO output frequency.

Table 7. Main Phase/Frequency Detector Polarity
(Mode Pin = High)

Mode Pin	Pol Pin	Main Detector Polarity (PD_{out}–Lo and PD_{out}–Hi)
High	Low	Positive
High	High	Negative
Low	*	Positive

*Pin configured as an output; should not be driven.

Table 8. Secondary Phase/Frequency Detector Polarity
(Mode Pin = High)

Mode Pin	Pol′ Pin	Secondary Detector Polarity (PD_{out}′)
High	Low	Positive
High	High	Negative
Low	*	Positive

*Pin configured as an output; should not be driven.

5B. REFERENCE PINS

Osc_e and Osc_b
Pins 1 and 32 — Reference Oscillator Transistor Emitter and Base

These pins can be configured to support an external crystal in a Colpitts oscillator configuration. The required connections for the crystal circuit are shown in the **Crystal Oscillator Considerations** section.

Additionally, the pins can be configured to accept an external reference frequency source, such as a TCXO. In this case, the reference signal is ac coupled into Osc_e and the Osc_b pin is left floating. See Figure 11.

Bit C6 and the Mode input pin control the configuration of these pins per Table 9.

Table 9. Reference Configuration

Mode Input Pin	Bit C6	Reference Configuration	Comment
Low	X	Supports Crystal (default)	C6 used to control Output B*
High	0	Supports Crystal	Output B not useful
High	1	Requires External Reference	Output B not useful

*See Table 5.

5C. LOOP PINS

f_{in} and $\overline{f_{in}}$
Pins 12 and 13 — Frequency Input for Main Loop (PLL)

These pins feed the on–chip RF amplifier which drives the high–speed N counter. This input may be fed differentially. However, it is usually used in a single–ended configuration with f_{in} driven while $\overline{f_{in}}$ is tied to a good RF ground (via a capacitor). The signal source driving this input must be ac coupled and originates from an external VCO.

The sensitivity of the RF amplifier is dependent on frequency as shown in the Loop Specifications table. Sensitivity of the f_{in} input is specified as a level across a 50 Ω load driven by a 50 Ω source. A VCO that can drive a load within the data sheet limits can also drive f_{in}. Usually, to avoid load pull and resultant frequency modulation of the VCO, f_{in} is lightly coupled by a small value capacitor and/or a resistor. See the applications circuit of Figure 65.

f_{in}′
Pin 30 — Frequency Input for Secondary Loop (PLL′)

This pin feeds the on–chip RF amplifier which drives the high–speed N′ counter. This input is used in a single–ended configuration. The signal source driving this input must be ac coupled and originates from an external VCO.

The sensitivity of the RF amplifier is dependent on frequency as shown in the Loop Specifications table. Sensitivity of the f_{in}′ input is specified as a level across a 50 Ω load driven by a 50 Ω source. A VCO that can drive a load within the data sheet limits can also drive f_{in}′. Usually, to avoid load pull and resultant frequency modulation of the VCO, f_{in}′ is lightly coupled by a small value capacitor and/or a resistor. See the applications circuit of Figure 65.

If the secondary loop is not used, PLL′ should be placed in standby and f_{in}′ should be left open.

PD_{out}–Hi and PD_{out}–Lo
Pins 19 and 20 — Phase/Frequency Detector Outputs for Main Loop (PLL)

Each pin is a three–state current source/sink/float output for use as a loop error signal when combined with an external low–pass loop filter. Under bit control, PD_{out}–Lo has either one–quarter or one–eighth the output current of PD_{out}–Hi per Table 10. The detector is characterized by a linear transfer function (no dead zone). The polarity of the detector is controllable. The operation of the detector is described below and shown in Figure 20.

Table 10. Current Ratio of PD_{out}–Hi and PD_{out}–Lo

Bit N18	Output Current Ratio PD_{out}–Hi:PD_{out}–Lo (Gain Ratio)
0	4 : 1
1	8 : 1

When the Mode pin is high, positive polarity occurs when the Pol pin is low. Also, when the Mode pin is low, polarity

defaults to positive. Positive polarity is described below. f_V is the output of the main loop's VCO divider (N counter). f_R is the output of the main loop's reference divider (R counter).

(a) Frequency of $f_V > f_R$ or phase of f_V leading f_R: current–sinking pulses from a floating state.
(b) Frequency of $f_V < f_R$ or phase of f_V lagging f_R: current–sourcing pulses from a floating state.
(c) Frequency and phase of $f_V = f_R$: essentially a floating state, voltage at pin determined by loop filter.

When the Mode pin is high, negative polarity occurs when the Pol pin is high. Negative polarity is described below. f_V is the output of the main loop's VCO divider (N counter). f_R is the output of the main loop's reference divider (R counter).

(a) Frequency of $f_V > f_R$ or phase of f_V leading f_R: current–sourcing pulses from a floating state.
(b) Frequency of $f_V < f_R$ or phase of f_V lagging f_R: current–sinking pulses from a floating state.
(c) Frequency and phase of $f_V = f_R$: essentially a floating state, voltage at pin determined by loop filter.

These outputs can be enabled and disabled by bits in the C and N registers. Placing the main PLL in standby (bit C1 = 1) forces the detector outputs to a floating state. In addition, setting the PD Float bit (bit C4 = 1) forces the detector outputs to a floating state while allowing the counters to run for the main PLL. For selection of the outputs, see Table 11.

The phase detector gain (in amps per radian) = PD_{out} current (in amps) divided by 2π.

If a detector output is not used, that pin should be left open.

Table 11. Selection of Main Detector Outputs

Bit N21	Bit N20	Bit N19	Result
0	0	0	Both outputs not enabled
0	0	1	PD_{out}–Lo enabled
0	1	0	PD_{out}–Hi enabled
0	1	1	Both PD_{out}–Lo and PD_{out}–Hi enabled
1	0	0	PD_{out}–Hi enabled for 16 f_R cycles only, then PD_{out}–Lo enabled
1	0	1	PD_{out}–Hi enabled for 32 f_R cycles only, then PD_{out}–Lo enabled
1	1	0	PD_{out}–Hi enabled for 64 f_R cycles only, then PD_{out}–Lo enabled
1	1	1	PD_{out}–Hi enabled for 128 f_R cycles only, then PD_{out}–Lo enabled

NOTES: 1. When a detector output is not enabled, it is floating.
2. Setting bit N21 = 1 places the IC in an adapt mode and engages a timer.

PD_{out}'
Pin 23 — Phase/Frequency Detector Output for Secondary Loop (PLL′)

This pin is a three–state voltage output for use as a loop error signal when combined with an external low–pass loop filter. The detector is characterized by a linear transfer function (no dead zone). The polarity of the detector is controllable. The operation of the detector is described below and shown in Figure 21.

When the Mode pin is high, positive polarity occurs when the Pol′ pin is low. Also, when the Mode pin is low, polarity defaults to positive. Positive polarity is described below. f_V' is the output of the secondary loop's VCO divider (N′ counter). f_R' is the output of the secondary loop's reference divider (R′ counter.)

(a) Frequency of $f_V' > f_R'$ or phase of f_V' leading f_R': negative pulses from high impedance.
(b) Frequency of $f_V' < f_R'$ or phase of f_V' lagging f_R': positive pulses from high impedance.
(c) Frequency and phase of $f_V' = f_R'$: essentially a high–impedance state, voltage at pin determined by loop filter.

When the Mode pin is high, negative polarity occurs when the Pol′ pin is high. Negative polarity is described below. f_V' is the output of the secondary loop's VCO divider (N′ counter). f_R' is the output of the secondary loop's reference counter (R′ counter.)

(a) Frequency of $f_V' > f_R'$ or phase of f_V' leading f_R': positive pulses from high impedance.
(b) Frequency of $f_V' < f_R'$ or phase of f_V' lagging f_R': negative pulses from high impedance.
(c) Frequency and phase of $f_V' = f_R'$: essentially a high–impedance state, voltage at pin determined by loop filter.

This output can be enabled and disabled by bits in the C register. Placing the secondary PLL′ in standby (bit C0 = 1) forces the detector output to a high–impedance state. In addition, setting the PD′ Float bit (bit C3 = 1) forces the detector output to a high–impedance state while allowing the counters to run for PLL′.

The phase detector gain (in volts per radian) = C_{mult} voltage (in volts) divided by 4π.

If the secondary loop is not used, PLL′ should be placed in standby and PD_{out}' should be left open.

5D. ANALOG OUTPUTS

DAC1 and DAC2
Pins 3 and 4 — Digital–to–Analog Converter Outputs

These are independent outputs of the two 8–bit D/A converters. The output voltage is determined by bits in the D register. Each output is a static level with an output impedance of approximately 100 kΩ.

The DACs may be used for crystal oscillator trimming, PA (power amplifier) output power control, or other general–purpose use.

If a DAC output is not used, the pin should be left open.

5E. EXTERNAL COMPONENTS

Rx
Pin 17 — Current–Setting Resistor

An external resistor to Gnd at this pin sets a reference current that is used to determine the current at the phase/frequency detector outputs PD_{out}–Hi and PD_{out}–Lo. A value of 2 kΩ is required.

C_{mult}
Pin 21 — Voltage–Multiplier Capacitor

An external capacitor to Gnd at this pin is used for the on–chip voltage multiplier circuit. The value of this capacitor must be greater than 20 times the value of the largest loop filter capacitor. For example, if the largest loop filter capacitor on either the main loop or the secondary loop is 0.01 μF, then a 0.22 μF capacitor could be used on the C_{mult} pin.

To ensure minimum standby supply current drain, the voltage potential at the C_{mult} pin must not be allowed to fall below the potential at the V_{pos} pins. Therefore, if the keep–alive oscillator is shut off, the user should tie a large value resistor (> 10 MΩ) between the C_{mult} pin and V_{pos}. This resistor should be sized to overcome leakage from C_{mult} to Gnd due to the printed circuit board and the external capacitor. The consequence of not using the resistor is higher supply current drain in standby. If standby is not used, the resistor is not necessary. Also, if the keep–alive oscillator is used, the resistor can be omitted.

C_{reg}
Pin 22 — Regulator Capacitor

An external capacitor to Gnd at this pin is required for the on–chip voltage regulator. A value of 1 μF is recommended.

5F. SUPPLY PINS

DAC V_{pos}
Pin 2 — Positive Supply Potential for DACs

This pin supplies power to both DACs and determines the full–scale output of the DACs. The full–scale output is approximately equal to the voltage at DAC V_{pos}. The voltage applied to this pin may be more, less, or equal to the potential applied to the V_{pos} pins. The voltage range for DAC V_{pos} is 1.8 to 3.6 V with respect to the Gnd pins.

If both DACs are not used, DAC V_{pos} should be tied to the same potential as V_{pos}.

V_{pos}
Pins 11, 24, 26, and 29 — Principal Positive Supply Potential

These pins supply power to the main portion of the chip. All V_{pos} pins must be at the same voltage potential. The voltage range for V_{pos} is 1.8 to 3.6 V with respect to the Gnd pins.

For optimum performance, all V_{pos} pins should be tied together and bypassed to a ground plane using a low–inductance capacitor mounted very close to the device. Lead lengths and printed circuit board traces between the capacitor and the IC package should be minimized. (The very–fast switching speed of the device can cause excessive current spikes on the power leads if they are improperly bypassed.)

Gnd
Pins 14, 15, 18, and 31 — Ground

Common ground for the device. All Gnd pins must be at the same potential and should be tied to a ground plane.

6. DETAILED REGISTER DESCRIPTIONS

6A. C REGISTER

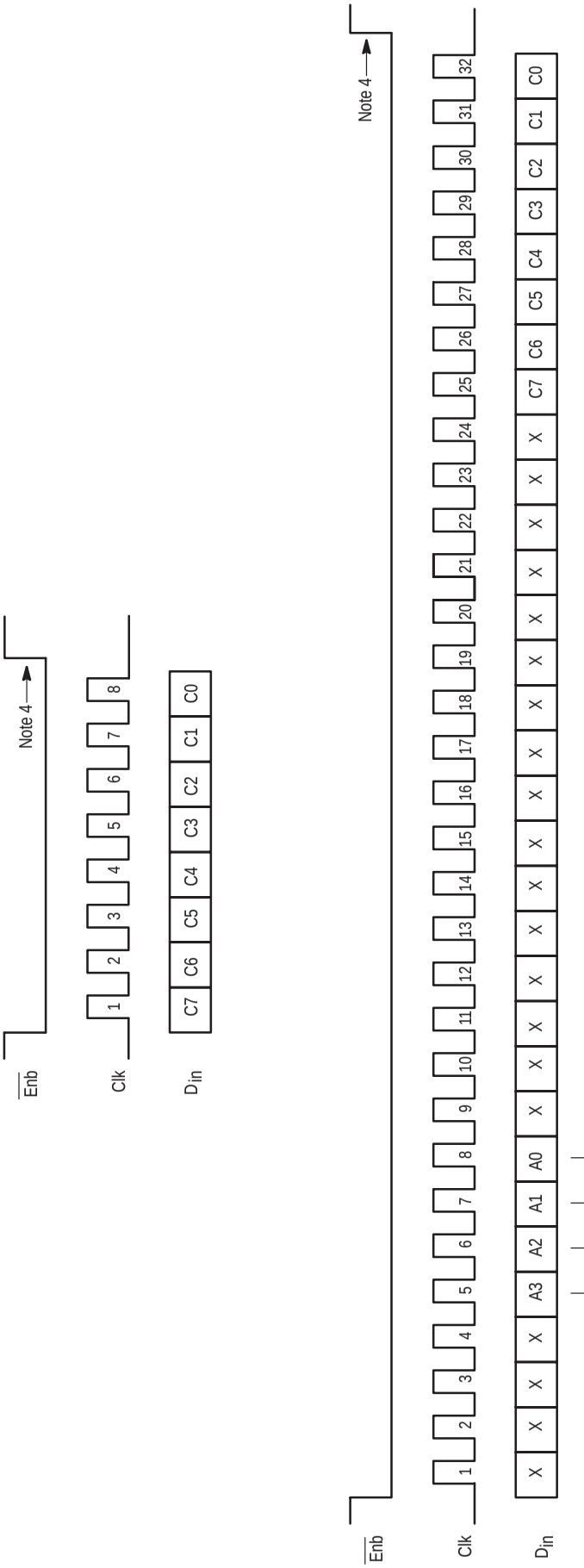


Figure 13. C Register Access and Formats

NOTES:

1. To access the C register, either 8 or 32 clock cycles can be used.
2. For the 8–bit stream, no address bits are needed.
3. For the 32–bit stream, address bits A3 through A0 are required.
4. At this point, the new byte is transferred to the C register. No other register is affected.
5. X signifies a don't care bit.

C REGISTER BITS

See Figure 13 for C register access and serial data formats.

Out A (C7)

When the Output A pin is selected as a General–Purpose Output (via bits R′21 = R′20 = 0), bit C7 determines the state of the pin. When C7 is 1, Output A is forced to a high level. When C0 is 0 Output A is forced low.

When Output A is not selected as a General–Purpose Output, bit C7 has no function; i.e., C7 is a “don’t care” bit.

Out B/XRef (C6)

Bit C6 is a dual–purpose bit.

When the Mode pin is tied low, C6 and C1 (PLL Stby), can be used to control Output B. See Table 12. (The reference circuit defaults to crystal configuration.)

When the Mode pin is tied high, additional control of the reference circuit is allowed. See Table 13.

Table 12. Out B/XRef Bit with Mode Pin = Low

Bit C6	Bit C1	State of Output B Pin	Condition of Main PLL
0	0	Low level	Active
0*	1*	High impedance*	Standby*
1	0	High level	Active
1	1	High impedance	Standby

*Power up default.

Table 13. Out B/XRef Bit with Mode Pin = High

Bit C6	Reference Configuration
0*	Supports Crystal*
1	Accommodates External Reference

*Power up default.

Out C (C5)

This bit determines the state of the Output C pin. When C5 is 1, Output C is forced to a high–impedance state. When C5 is 0, Output C is forced low.

PD Float (C4)

This bit controls the phase detector for the main loop, outputs PD_{out}–Hi and PD_{out}–Lo. When this bit is 0, the main phase detector operates normally. When the bit is 1, the outputs are forced to the floating state which opens the loop and allows modulation to be introduced into the external VCO input. During this time, the counters are still active. This bit is inhibited from affecting the phase detector during a PD_{out}–Hi or PD_{out}–Lo pulse.

If the loop is locked prior to C4 being set to 1, the lock detect signal from the main loop continues to indicate “lock” immediately after PD Float is set to 1. If the phase of the loop drifts outside the lock detect window, then the lock detect signal indicates “not locked”. If the loop is not locked, and PD Float is set to 1, then the lock detect signal from the main loop continues to indicate “not locked”.

PD′ Float (C3)

This bit controls the phase/frequency detector for the secondary loop, output PD_{out}'. When this bit is 0, the secondary phase detector operates normally. When the bit is 1, the output is forced to the floating state which opens the loop and allows modulation to be introduced into the external VCO input. During this time, the counters are still active. This bit is inhibited from affecting the phase detector during a PD_{out}' pulse.

If the loop is locked prior to C3 being set to 1, the lock detect signal from the secondary loop continues to indicate “lock” immediately after PD′ Float is set to 1. If the phase of the loop drifts outside the lock detect window, then the lock detect signal indicates “not locked”. If the loop is not locked, and PD′ Float is set to 1, then the lock detect signal from the secondary loop continues to indicate “not locked”.

Osc Stby (C2)

This bit controls the crystal oscillator and external reference input circuit. When this bit is 0, the circuit is active. When the bit is 1, the circuit is shut down and is in the low–power standby mode. When this circuit is shut down, a keep–alive oscillator for the voltage doubler is activated, unless the doubler is shut off via bits in the R′ register. In the crystal oscillator mode, when C2 transitions from a 1 to a 0 state, a kick–start circuit is engaged for a few milliseconds. The kick–start circuit ensures self–starting for a properly–designed crystal oscillator

NOTE

Whenever C2 is 1, both bits C1 and C0 must be 1, also.

To minimize standby supply current, the voltage multiplier may be shut down (by bits R′19, R′18, and R′17 being all zeroes). If this is the case and the voltage multiplier feature is being used, the user must allow sufficient time for the phase/frequency detector supply voltage to pump up when the multiplier is brought out of standby. This “pump up” time is dependent on the C_{mult} capacitor size. Pump current is approximately 100 μA. During the pump up time, either the PLL standby bits C1 and C2 must be 1 or the phase/frequency detector float bits C3 and C4 must be 1.

PLL Stby (C1)

When set to 1, this bit places the main PLL in the standby mode for reduced power consumption. PD_{out}–Hi and PD_{out}–Lo are forced to the floating state, the N and R counters are inhibited from counting, the main loop’s input amp is shut off, the Rx current is inhibited, and the main phase/frequency detector is shut off. The reference oscillator circuit is still active and independently controlled by bit C2.

When this bit is programmed to 0, the main PLL is taken out of standby in two steps. First, the input amplifier is activated, all counters are enabled, and the Rx current is no longer inhibited. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector at this time. Second, when the f_R pulse occurs, the N counter is loaded, and the phase/frequency and lock detectors are initialized via both flip–flops being reset. Immediately after the load, the N and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase

and lock detectors, and the phase/frequency detector output is enabled to issue an error correction pulse on the next f_R and f_V pulses. (Patent issued on this method.)

During standby, data is retained in all registers and any register may be accessed. When setting or clearing the PLL Stby bit, other bits in the C register may be changed simultaneously.

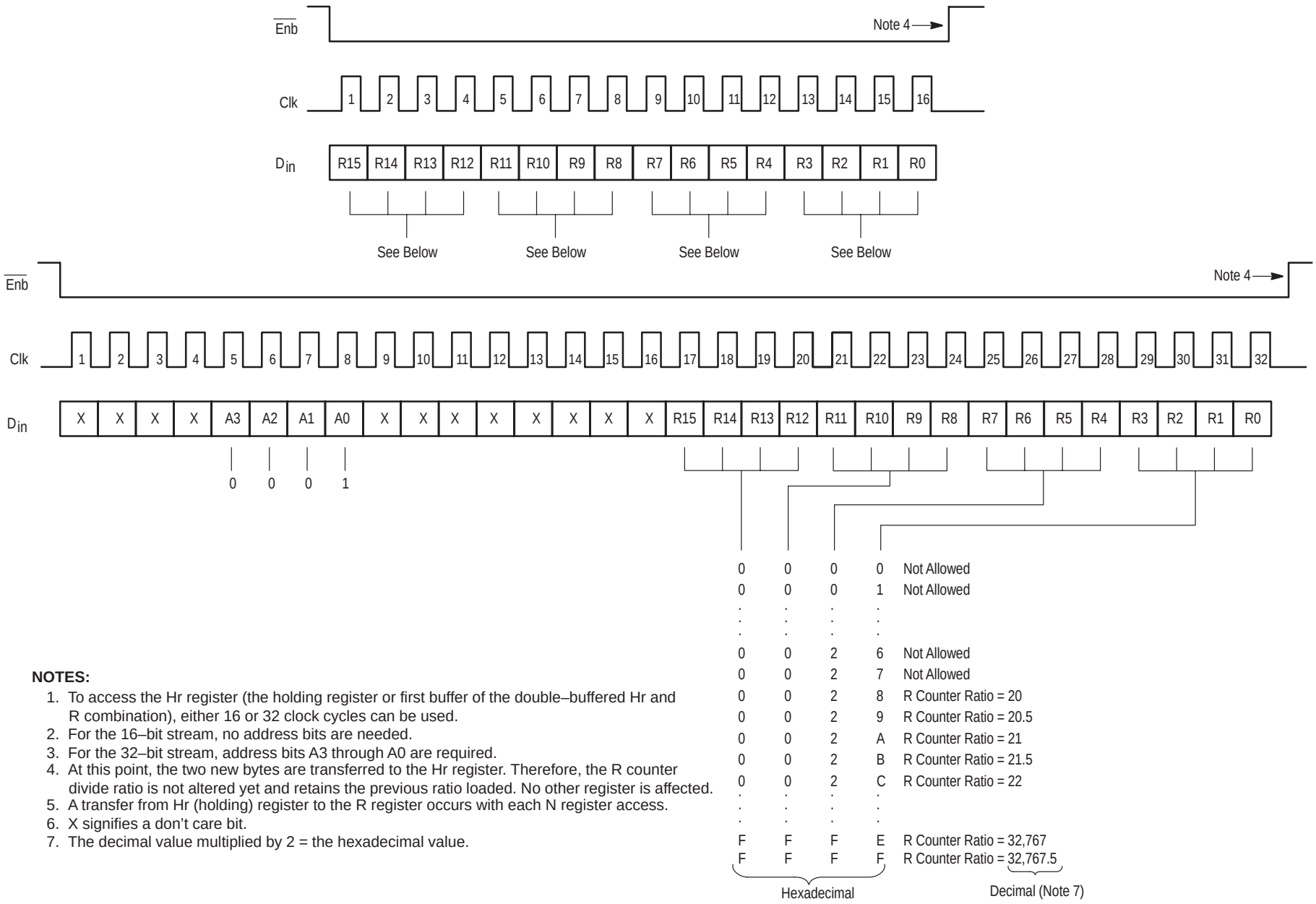
PLL′ Stby (C0)

When set to 1, this bit places the PLL′ section of the chip, which includes the on–chip f_{in}′ input amp, in the standby mode for reduced power consumption. PD_{out}′ is forced to the floating state. The R′ and N′ counters are inhibited from counting and placed in the low–current mode. The exception is the R′ counter's prescaler when the Mode pin is low. The R′ counter's prescaler remains active along with the f_{out} and $\overline{f_{out}}$ pins when PLL′ is placed in standby (Mode pin = low). When the Mode pin is low, the f_{out} pin, $\overline{f_{out}}$ pin, and R′ counter's prescaler are shut down only when Osc Stby bit C2 is set to 1.

When C0 is reset to 0, PLL′ is taken out of standby in two steps. All PLL′ counters and the input amp are enabled. Any f_R′ and f_V′ signals are inhibited from toggling the associated phase/frequency detector at this time. Second, when the f_R′ pulse occurs, the N′ counter is loaded and the phase/frequency detector is initialized via both flip–flops being reset. Immediately after the load, the N′ and R′ counters begin counting down together. At this point, the f_R′ and f_V′ pulses are enabled to the phase and lock detectors, and the phase/frequency detector output is enabled to issue an error correction pulse on the next f_R′ and f_V′ pulses. (Patent issued on this method.)

During standby, data is retained in all registers, and any register may be accessed. When setting or clearing the PLL′ Stby bit, other bits in the C register may be changed simultaneously.

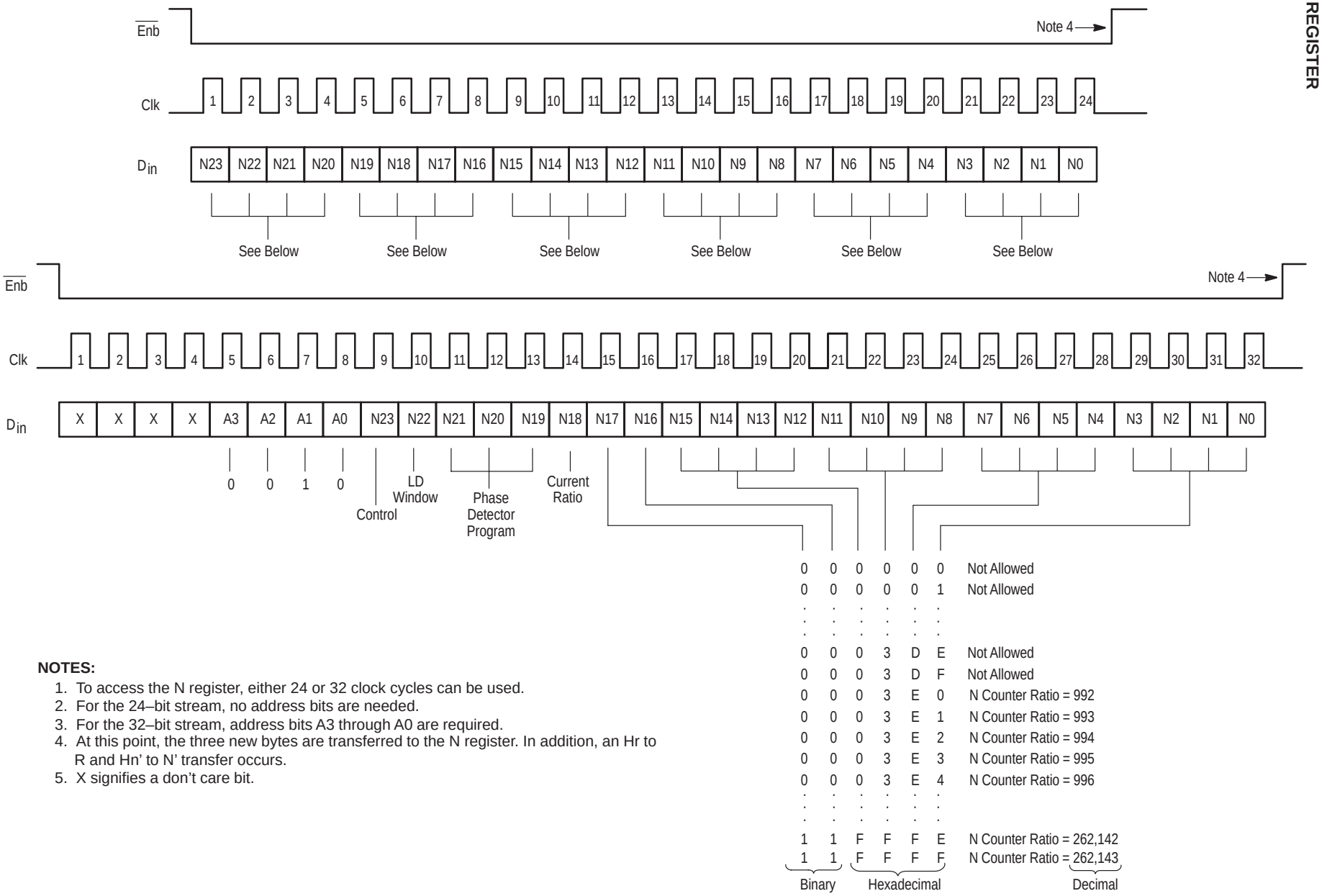
Figure 14. Hr Register Access and Formats



NOTES:

1. To access the Hr register (the holding register or first buffer of the double–buffered Hr and R combination), either 16 or 32 clock cycles can be used.
2. For the 16–bit stream, no address bits are needed.
3. For the 32–bit stream, address bits A3 through A0 are required.
4. At this point, the two new bytes are transferred to the Hr register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. No other register is affected.
5. A transfer from Hr (holding) register to the R register occurs with each N register access.
6. X signifies a don't care bit.
7. The decimal value multiplied by 2 = the hexadecimal value.

Figure 15. N Register Access and Formats



NOTES:

1. To access the N register, either 24 or 32 clock cycles can be used.
2. For the 24–bit stream, no address bits are needed.
3. For the 32–bit stream, address bits A3 through A0 are required.
4. At this point, the three new bytes are transferred to the N register. In addition, an Hr to R and Hn' to N' transfer occurs.
5. X signifies a don't care bit.

N REGISTER BITS

See Figure 15 for N register access and serial data formats.

Control (N23)

When the Mode pin is low, Control bit N23 determines the divide ratio of the auxiliary divider which feeds the buffers for the f_{out} and $\overline{f_{out}}$ pins. See Table 14 for the overall ratio between Osc_e and $f_{out}/\overline{f_{out}}$.

When the Mode pin is high, N23 must be programmed to 1.

Table 14. Osc_e to f_{out} Frequency Ratio, Mode = Low

N23	R′1	R′0	Osc_e to f_{out} Frequency Ratio
0	0	0	10:1
0	0	1	12.5:1
0	1	0	12.5:1
0	1	1	12.5:1
1	0	0	8:1
1	0	1	10:1
1	1	0	10:1
1	1	1	10:1

LD Window (N22)

Bit N22 determines the lock detect window for the main loop. Refer to Table 15 and Figure 19.

Table 15. Lock Detect Window

N22	LD Window (Approximated)
0	32 Osc_e periods
1	128 Osc_e periods

Phase Detector Program (N21, N20, N19)

These bits control which phase detector outputs are active for the main loop. These bits also control the timer interval when adapt is utilized for the main loop. See Table 16.

Table 16. Main Phase Detector Control

N21	N20	N19	Result
0	0	0	Both PD_{out}–Hi and PD_{out}–Lo floating
0	0	1	PD_{out}–Hi floating, PD_{out}–Lo enabled
0	1	0	PD_{out}–Hi enabled, PD_{out}–Lo floating
0	1	1	Both PD_{out}–Hi and PD_{out}–Lo enabled
1	0	0	PD_{out}–Hi enabled and PD_{out}–Lo floating for 16 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled
1	0	1	PD_{out}–Hi enabled and PD_{out}–Lo floating for 32 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled
1	1	0	PD_{out}–Hi enabled and PD_{out}–Lo floating for 64 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled
1	1	1	PD_{out}–Hi enabled and PD_{out}–Lo floating for 128 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled

Current Ratio (N18)

This bit allows for MCU control of the PD_{out}–Hi to PD_{out}–Lo current (or gain) ratio on the main loop phase/frequency detector outputs. See Table 17.

Table 17. PD_{out}–Hi to PD_{out}–Lo Current Ratio

N18	PD_{out}–Hi to PD_{out}–Lo Current Ratio	PD_{out}–Hi Current C_{mult} Pin = 5 V (Nominal)	PD_{out}–Lo Current C_{mult} Pin = 5 V (Nominal)
0	4:1	4.4 mA	1.1 mA
1	8:1	4.4 mA	0.55 mA

N Counter Divide Ratio (N17 to N0)

These bits control the N Counter divide ratio or loop multiplying factor. The minimum allowed value is 992. The maximum value is 262,143. For ease of programming, binary representation is used. For example, if a divide ratio of 1000 is needed, the 1000 in decimal is converted to binary 00 0000 0011 1110 1000 and is loaded into the device for N17 to N0. See Figure 15.

Figure 16. R' Register Access and Format

NOTES:

1. To access the R' register, 32 clock cycles must be used.
2. Address bits A3 through A0 are required.
3. At this point, the three new bytes are transferred to the R' register. No other register is affected.
4. The decimal value multiplied by 2 = the hexadecimal value. Counter divide ratios shown apply when the Mode pin is tied high. For ratios when the Mode pin is tied low, see Table 21.
5. X signifies a don't care bit.

R′ REGISTER BITS

See Figure 16 for R′ register access and serial data format.

Y Coefficient (R′23 and R′22)

These bits are programmed per Table 18. Note that for the MC145181, the bits are always programmed as 00. For compatibility, the other combinations are reserved for use with the MC145225 and MC145230.

Table 18. Y Coefficient

R′23	R′22	Maximum Allowed Frequency at f_{in} Pin
0	0	550 MHz
0	1	1.2 GHz
1	0	2.2 GHz
1	1	(not used)

Output A Function (R′21 and R′20)

These bits control the function of the Output A pin per Table 19. When selected as a general–purpose output, bit C7 controls the state of the pin. The signals f_R and $f_{R'}$ are the outputs of the R and R′ counters, respectively. The selection as a detector pulse is a test feature.

Table 19. Output A Function Selection

R′21	R′20	Function Selected for Output A
0	0	General–Purpose Output
0	1	f_R
1	0	$f_{R'}$
1	1	Phase/Frequency Detector Pulse from both loops

V–Mult Control (R′19, R′18, R′17)

These bits control the voltage multiplier per Table 20. When the multiplier is in the active state, the bits determine the voltage multiplier's refresh rate of the capacitor tied to the C_{mult} pin.

When active, the bits should be programmed for the lowest possible maximum frequency shown in the table. This ensures that the voltage multiplier is operating at optimum efficiency. For example, for a system utilizing a 16.8 MHz reference, bits R′19, R′18, and R′17 should be programmed as 001 if the user desires to use the voltage multiplier. If the user does not want to use the multiplier, the bits should be programmed as 000. In the latter case, only a 0.1 μF bypass capacitor is needed at the C_{mult} pin and an external phase/frequency detector supply voltage of 3.6 to 5.25 V must be provided to the C_{mult} pin.

Table 20. Voltage Multiplier Control

R′19	R′18	R′17	Multiplier State	Maximum Allowed Frequency at Osc_e Pin
0	0	0	Inactive	80 MHz
0	0	1	Active	20 MHz
0	1	0	Active	40 MHz
0	1	1	Active	80 MHz
1	X	X	—	(for factory evaluation)

Test/Rst (R′16)

This bit must be programmed to 0 by the user.

R′ Counter Divide Ratio (R′15 to R′0)

These bits control the R′ counter divide ratio. Thus, these bits determine the secondary loop's minimum step size. This step size is the same as the phase/frequency detector's operating frequency which must not exceed 600 kHz.

With the Mode pin tied high, the minimum allowed value is 20. The maximum value is 32,767.5. For ease of programming, binary representation is used. However, the binary value must be multiplied by 2. For example, if a divide ratio of 1000 is needed, the 1000 in decimal is converted to binary 0000 0011 1110 1000. This value is multiplied by 2 and becomes 0000 0111 1101 0000 and is loaded into the device for R′15 to R′0. See Figure 16.

With the Mode pin tied low, Table 21 shows the divide ratios available. There are two formulas for the divide ratio when Mode is low.

If R′1 R′0 are 00: R′ Ratio = (Value of R′15 to R′2) x 2.

If R′1 R′0 are 01, 10, 11: R′ Ratio = (Value of R′15 to R′2) x 2.5.

Table 21. R′ Counter Divide Ratios with Mode Pin Tied Low*

R′15	R′14	R′13	R′12	R′11	R′10	R′9	R′8	R′7	R′6	R′5	R′4	R′3	R′2	R′1	R′0	R′ Counter Divide Ratio
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Not Allowed
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	Not Allowed
⋮																
0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	Not Allowed
0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	20
0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	25
0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	X	25
0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	22
0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	27.5
0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	X	27.5
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	24
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	30
0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	X	30
0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	26
0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	32.5
0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	X	32.5
⋮																
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	32,766
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	40,957.5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	40,957.5

* Divide ratios with the Mode pin tied high are shown in Figure 16.

6E. Hn′ REGISTER

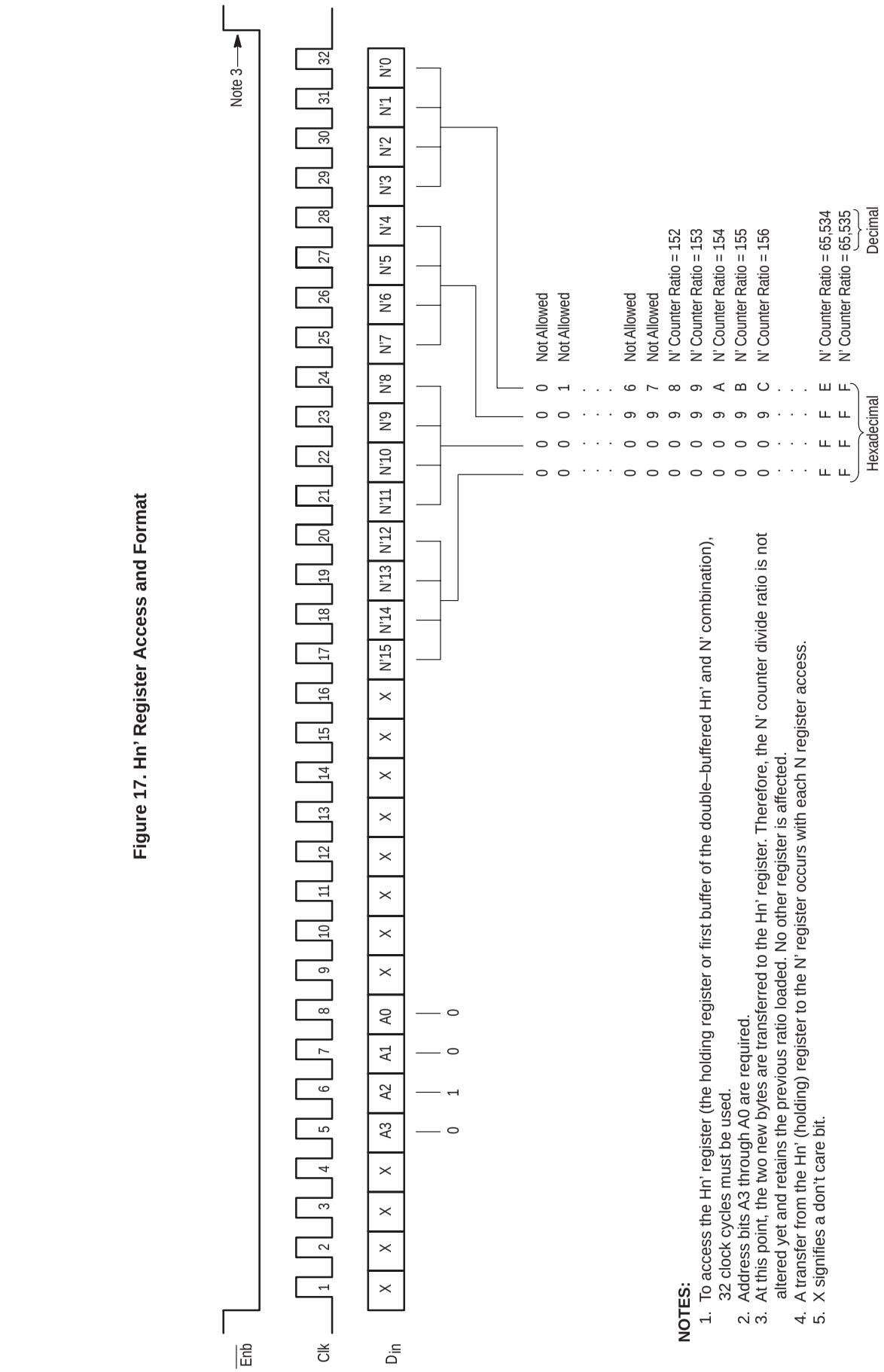


Figure 17. Hn′ Register Access and Format

NOTES:

1. To access the Hn′ register (the holding register or first buffer of the double–buffered Hn′ and N′ combination), 32 clock cycles must be used.
2. Address bits A3 through A0 are required.
3. At this point, the two new bytes are transferred to the Hn′ register. Therefore, the N′ counter divide ratio is not altered yet and retains the previous ratio loaded. No other register is affected.
4. A transfer from the Hn′ (holding) register to the N′ register occurs with each N register access.
5. X signifies a don't care bit.

6F. D REGISTER

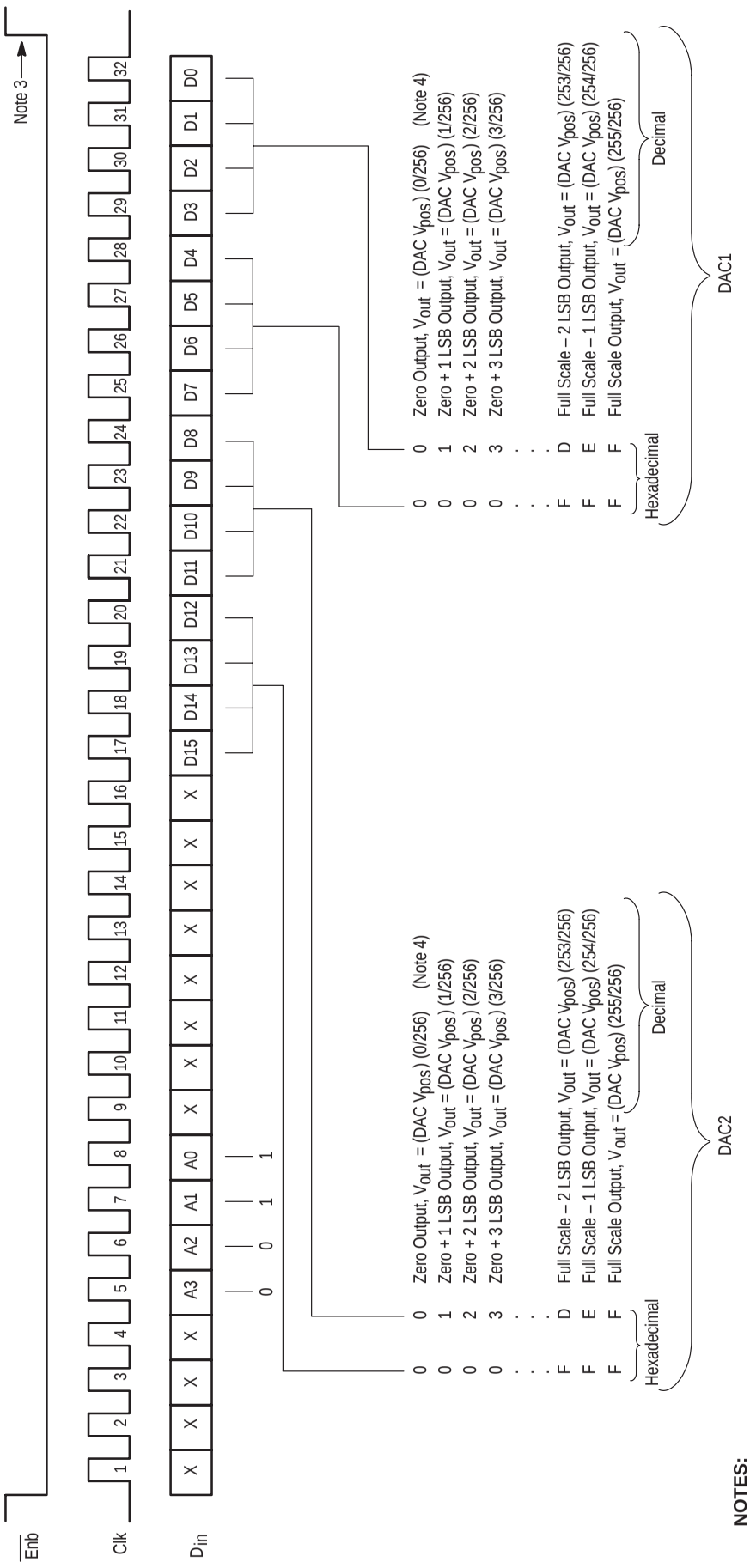
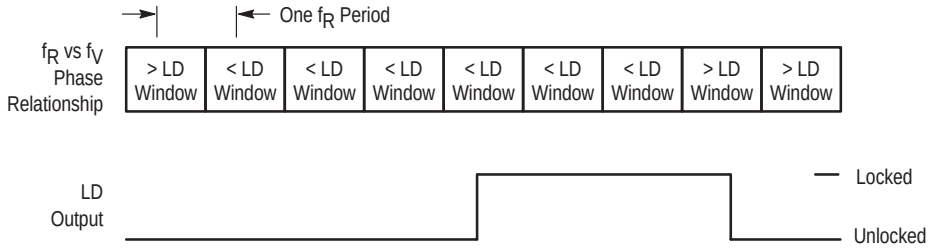


Figure 18. D Register Access and Format

NOTES:

1. To access the D Register, 32 clock cycles are used.
2. Address bits A3 through A0 are required.
3. At this point, the two new bytes are transferred to the D register. No other register is affected.
4. Low–power standby state.
5. X signifies a don't care bit.

Figure 19. Lock Detector Operation



NOTES:

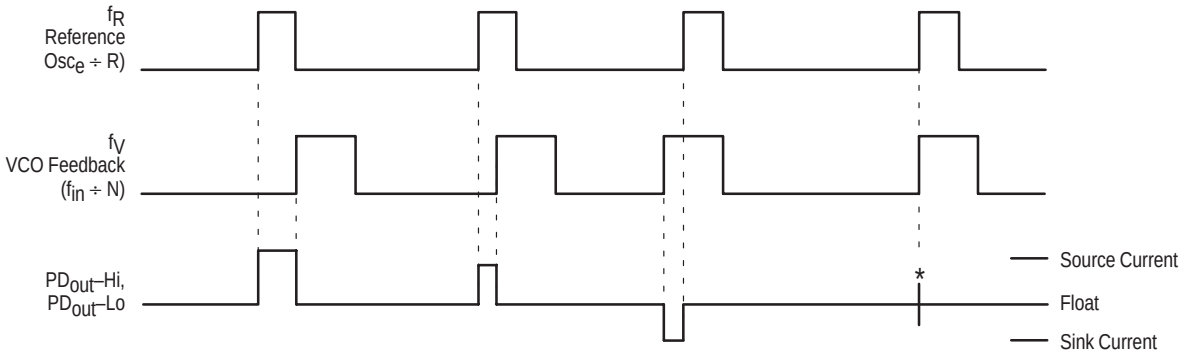
1. Illustration shown is for the main loop and applies when the secondary loop is either phase locked or in standby. The actual detector outputs for each loop are ANDed together at the LD pin.
2. The secondary loop is similar to the above illustration.
3. The approximate lock detect window for the main loop is either 64 or 256 Osc_e cycles and is programmable via bit N22. The approximate window for the secondary loop is 64 Osc_e cycles and is not programmable.
4. The LD output is low whenever the phase difference is more than the lock detect window.
5. The LD output is high whenever the phase difference is less than the lock detect window and continues to be less than the window for 3 f_R periods or more.

LOCK DETECTOR OUTPUT CONDITIONS

f_R versus f_V Relation	Lock Detector Output	Microcontroller Action
Frequency is the same with phase inside the LD window	Static high level output	Senses high level and no edges, therefore loop is locked
Frequency is the same with phase outside the LD window	Static low level output	Senses low level, therefore loop is unlocked
Frequency is slightly different, thus phase is changing	Dynamic “chattering” output, output has transitions	Senses edges, therefore loop is unlocked
Frequency is grossly different	Static low level output	Senses low level, therefore loop is unlocked

NOTE: For simplicity, this table applies to the main loop. The secondary loop is similar. The detector outputs feed an AND gate whose output is the LD pin.

Figure 20. PD_{out}–Hi and PD_{out}–Lo Detector Output Characteristics

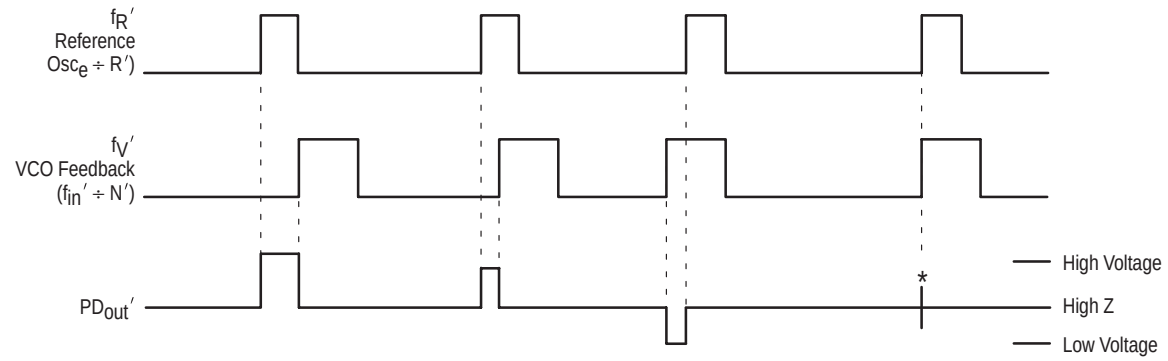


*At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.

NOTES:

1. The detector generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.
2. Waveform shown applies when the $\overline{f_{out}}$/Pol pin is low and the Mode pin is high.
3. When the $\overline{f_{out}}$/Pol pin is high and Mode is high, the PD_{out}–Hi and PD_{out}–Lo waveform is inverted.
4. The waveform shown is also the default when the Mode pin is low.

Figure 21. $PD_{out}{}'$ Detector Output Characteristics



*At this point, when both $f_R{}'$ and $f_V{}'$ are in phase, the output source and sink circuits are turned on for a short interval.

NOTES:

1. The detector generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.
2. Waveform shown applies when the f_{out}/Pol′ pin is low and the Mode pin is high.
3. When the f_{out}/Pol′ pin is high and Mode is high, the $PD_{out}{}'$ waveform is inverted.
4. The waveform shown is also the default when the Mode pin is low.

7. APPLICATIONS INFORMATION

7A. CRYSTAL OSCILLATOR CONSIDERATIONS

The oscillator/reference circuit may be connected to operate in either of two configurations. With the Mode pin placed “high” and bit C6 programmed to 1, the oscillator/reference circuit of the MC145181 will accept an external reference input. The external reference signal should be capacitive, connected to Osc_e with Osc_b left floating. Commercially available temperature compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide a very stable reference frequency. For additional information about TCXOs and data clock oscillators, please consult the Electronic Engineers Master Catalog, internet web page, or similar publication/service.

The on–chip Colpitts reference oscillator can be selected by either tying the Mode pin low or by programming the C6 bit to zero when Mode is high. The oscillator may be operated in either the fundamental mode, as show by Figure 22, or as an overtone oscillator. The “kick start” feature ensures reduced “stalling” of hard–starting crystals.

Crystal Resonators

The equivalent circuit of a crystal resonator most commonly used is shown in Figure 23. The crystal itself is a specially cut (usually AT for overtone operation) block of quartz. The dimensions, (shape, thickness, length, and width) determine the operating characteristics of the crystal. When deformed and allowed to return naturally to its resting shape, it is observed to oscillate. This oscillation has the typical characteristics of a damped oscillation and an equivalent electrical signal can be found on the surface of the crystal. In addition, if an equivalent electrical signal is applied to the crystal, it will be observed to oscillate. The equivalent values for R_S, L_S, C_S, and C_O can be used to predict the operation of the crystal when used as an electronic oscillator.

Due to the series/parallel arrangement of the equivalent components, the crystal exhibits two resonances. The first, sometimes just called resonance, is the series resonance of the R_S, C_S, L_S branch. The other, sometimes called the anti–resonance, is the parallel resonance including C_O. For the series resonance the formula is

$$f_S = \frac{1}{2\pi \sqrt{L_S C_S}} .$$

For parallel resonance, the formula is

$$f_p = \frac{1}{2\pi \sqrt{\frac{L_S C_S C_O}{C_O + C_S}}} .$$

As can be seen from this equation, the anti–resonant frequency is higher than the series resonant frequency. The ratio between the resonant and anti–resonant frequency can be found using the formula

$$\frac{\Delta f}{f} = \frac{C_S}{2 (C_O + C_S)}$$

where

$$\Delta f = |f_S - f_p|$$

and

$$f = \frac{f_S + f_p}{2} .$$

By exploiting this characteristic, the crystal oscillator frequency can be tuned slightly. If a capacitor is connected in series with the crystal operating in the resonance mode, the frequency will shift upward. If a capacitance is added in parallel with a crystal operating in an anti–resonant mode, the frequency will be shifted down.

Figure 22. Fundamental Mode Oscillator Circuit

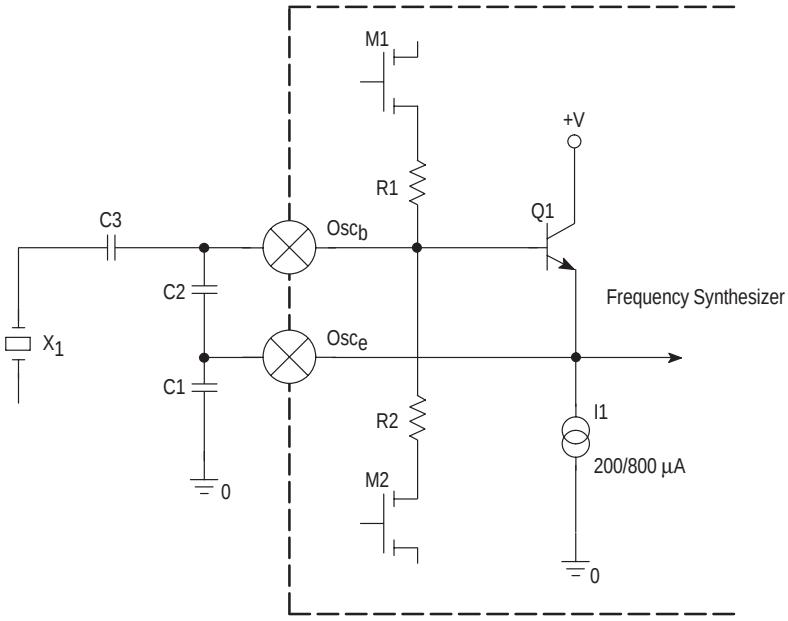
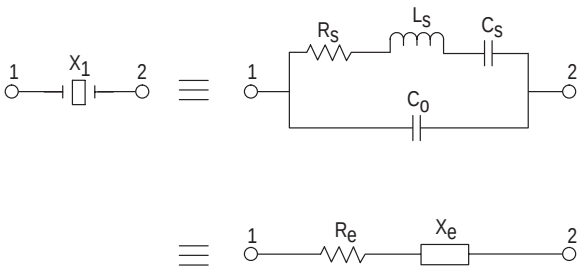
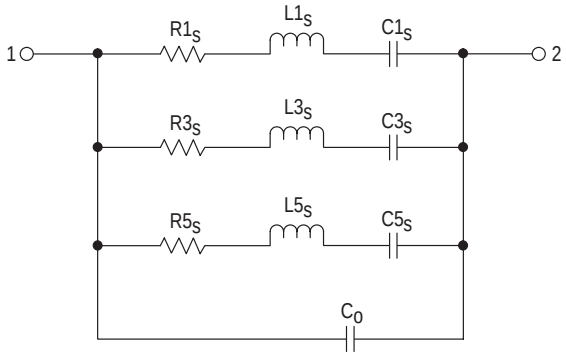


Figure 23. Crystal Resonator Equivalent Circuit



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 24. Overtone Crystal Equivalent Circuit



Because of the acoustic properties of the crystal resonator, the crystal “tank” responds to energy not only at its fundamental frequency, but also at specific multiples of the fundamental frequency. In the same manner that a shorted or open transmission line responds to multiples of the fundamental frequency, the crystal “tank” responds similarly. A shorted half–wave transmission line (or closed acoustic chamber) will not only resonate at its fundamental frequency, but also at odd multiples of the fundamental. These are called the overtones of the crystal and represent frequencies at which the crystal can be made to oscillate. The equivalent circuit of an overtone crystal is shown is Figure 24.

The components for the appropriate overtone are represented by 1, 3, and 5. The fundamental components are represented by 1, and those of importance for the third and fifth overtones, by 3 and 5.

Fundamental Mode

The equivalent circuit for the Colpitts oscillator operating in the fundamental mode is shown in Figure 25.

C3 is selected to provide a small reduction in the inductive property of the crystal. In this manner, the frequency of the oscillator can be “pulled” slightly. The biasing combination of M1R1 and M2R2 provide the ability to start operation with a higher than normal operating current to stimulate crystal activity. This “kick start” current is nominally four times the normal current. An internal counter times the application of the “kick start” and returns the current to normal after the time out period.

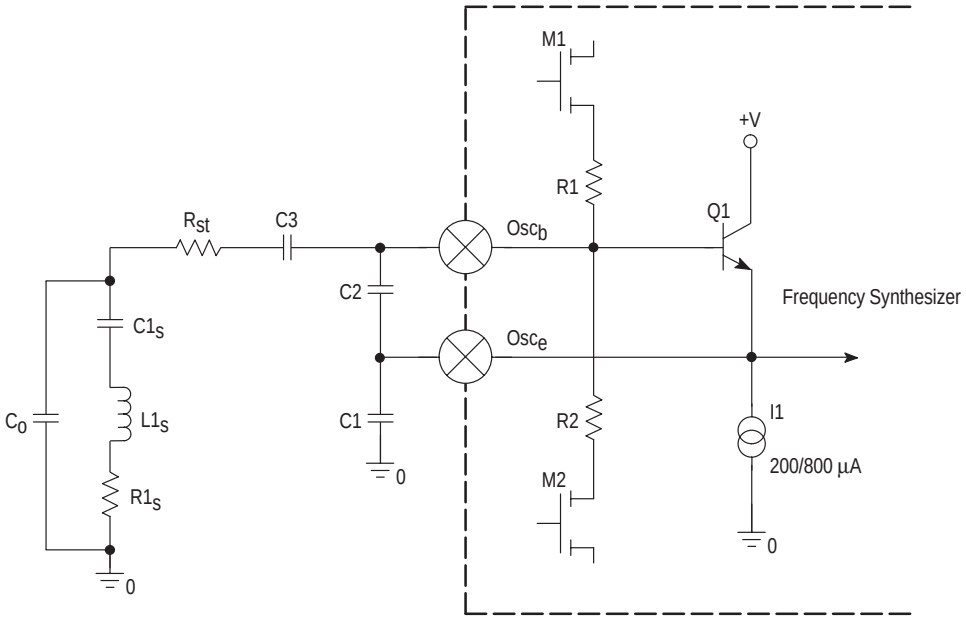
The mutual conductance (transconductance) of the transistor Q1 is useful in determining the conditions necessary for oscillation. The nominal value for the transconductance is found from the formula

$$gm = \frac{I_e}{26}$$

where Ie is the emitter current in mA.

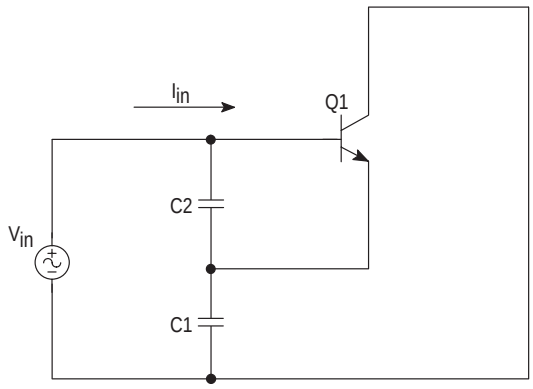
The operation of the oscillator can be described using the concept of “negative resistance”. In a normal tuned circuit, any excitation tends to be dissipated by the resistance of the circuit and oscillation dies out. The resistive part of the crystal along with the resistance of the wiring and the internal resistance of C1, C2, and C3, make up this “damping” resistance. Some form of energy must be fed back into the circuit to sustain oscillation. This is the purpose of the amplifier.

Figure 25. Fundamental Mode Colpitts Oscillator Equivalent Circuit



If we define the damping as resistive, we can define the opposite or regenerative property as negative resistance. Figure 26 shows the basic circuit of the Colpitts oscillator. C3 has been combined with the crystal elements for simplicity. For the circuit to oscillate, there must be at least as much “negative resistance” (regeneration) as there is resistance (damping). We can define this by deriving the input impedance for the amplifier.

Figure 26. Colpitts Oscillator Basic Circuit



If a driving signal is defined as V_{in}, the resultant current that flows can be identified as I_{in}. The relationship of V_{in} to I_{in} is

$$V_{in} = I_{in}\,(Z_{c1} + Z_{c2}) - I_b\,(Z_{c2} - \beta Z_{c1})$$

and

$$0 = I_{in}\,(Z_{c2}) + I_b\,(Z_{c2} + r_b)$$

where I_b is the base current of transistor Q1. Solving the two equations and assuming $Z_{c2} << r_b$, the input impedance can be expressed as

$$Z_{in} \sim \frac{-gm}{\omega^2\,C1\,C2} + \frac{1}{j\omega\left(\frac{C1\,C2}{C1 + C2}\right)}$$

where $\omega = 2\pi f$. This is equivalent to the series combination of a real part whose value is

$$REAL = \frac{-gm}{\omega^2\,C1\,C2}$$

and the imaginary part whose value is

$$IMAG = \frac{1}{j\omega\left(\frac{C1\,C2}{C1 + C2}\right)}$$

To sustain oscillation, the amplifier must generate a “negative resistance” equal or greater than the REAL part of the above equation and opposite in polarity.

$$R_{neg} = \frac{-gm}{\omega^2\,C1\,C2}$$

As long as the relation

$$-R_{neg} = -SUM\,(R_S + R_{st} + R_{c1} + R_{c2} + R_{c3}) \ ,$$

the circuit will oscillate and the frequency of oscillation will be defined as

$$f_o = \frac{1}{2\pi\sqrt{L_S\,(C1||C2||C3)}}$$

where C3 is the series frequency adjusting capacitor.

In determining values for C1, C2, and C3, two limits are considered. At one end is the relationship of C3 to C2 and C1. If C3 is made 0 or the reactance of C3 is small compared to the reactance of C1 and C2, no adjustment of the crystal frequency is possible. The other limit is the relationship

$$gm\,Z_{c1}\,Z_{c2} > R_{sum}$$

where R_{sum} is the sum of resistances in the resonant loop. Since this equation must be true for the circuit to oscillate, it is obvious that as the values of C1 and C2 are increased, the series resistances must be reduced and/or gm increased. Since gm is a function of device current and there is a physical limit on how small R_{sum} can be made, at some point oscillation can no longer be sustained.

Normally, it is desirable to choose the “negative resistance” to be several times greater than the “damping” resistance to ensure stable operation. A factor of four or five is a good “rule of thumb” choice.

To determine crystal power, the equivalent circuit shown in Figure 27 can be used. In this case, we are addressing a condition where the transistor amplifier is operating at the limit of class A; that is, the device is just at cutoff during the peak negative excursions. At this point,

$$R_e = gm\,X_{c1}\,X_{c2}$$

if the amplitude is constant and the oscillator is stable. For this to occur, the sum of all resistances in the resonant loop will be equal to R_e, where R_e represents the effective resistance of I1. This can be written as

$$R_{sum} = R_S + R_{st} = R_e$$

where R_S is the crystal resistance and R_{st} is the additional distributed resistances within the resonant loop. At the point where the transistor enters cutoff we have the equation

$$-I_{in} = \frac{v1 + v2}{X_{ls} + R_e} = \frac{(I_{in} - I_b)\,Z_{c2} + (I_{in} + \beta i_b)\,Z_{c1}}{X_{ls} + R_e} \ .$$

β = current gain of the transistor. Rewriting:

$$I_{in} = \frac{I_b\,(Z_{c2} - \beta Z_{c1})}{Z_{c1} + Z_{c2} + X_{ls} + R_e} \ .$$

For oscillation to occur, we must have

$$Z_{c1} + Z_{c2} + X_{ls} \sim 0 \ .$$

If we assume βZ_{c1} is normally much greater than Z_{c2} then

$$I_{in} \sim \frac{-I_e\,Z_{c1}}{R_e} \ .$$

For the condition we have specified,

$$I_e(bias) + I_e(instantaneous\ ac) = 0$$

the transistor is just cutting off and the peak current, I_{in} is equal to the bias current. The peak input current is represented as

$$I_{in}(peak) = \frac{I_e|Z_{c1}|}{R_e} \ .$$

The power dissipation of the series resistances in the resonant loop can be written as

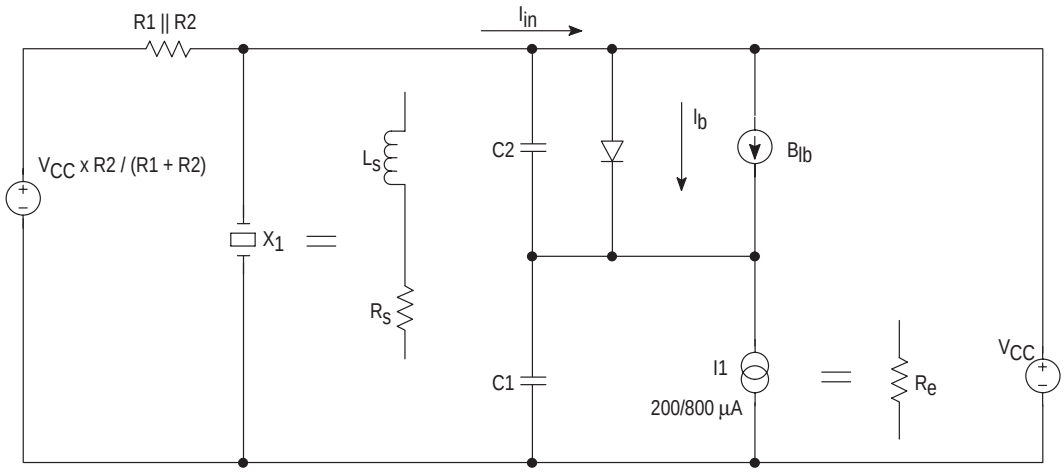
$$P = \frac{I_{in}(peak)^2\,R}{2} = \frac{(I_e|Z_{c1}|)^2}{2\,R_{sum}}$$

where $R_{sum} = R_e$.

The power dissipation for the crystal itself becomes

$$P_{crystal} = \frac{(I_e|Z_{c1}|)^2}{2\,R_S} \ .$$

Figure 27. Equivalent Circuit for Crystal Power Estimation



Overtone Operation

For overtone operation, the circuit is modified by the addition of an inductor, L1; and a series capacitor, C4. C4 is inserted as a dc blocking capacitor whose capacitance is chosen sufficiently large so that its reactance can be ignored. This circuit is shown in Figure 28.

For oscillation to occur at the overtone frequency, the condition

$$gm\ Z_{c1}\ Z_{c2} > R_S$$

must exist.

Z_{c1} represents the impedance across C1 and can be defined as

$$Z_{c1} = jX_{c1} \,||\, (R_{l1} + jX_{l1})$$

where R_{l1} is the dc resistance of the inductor L1.

For overtone operation, this must occur at the desired harmonic. For example, if the crystal is chosen to oscillate at the third overtone, C1 and C2 must be chosen so that the above condition exists for Z_{c1} and Z_{c2} at the third harmonic of the fundamental frequency for the crystal. In addition, care must be taken that the “negative resistance” of the amplifier is not sufficient at the fundamental frequency to induce oscillation at the fundamental frequency. It may be necessary to add additional filtering to reduce the gain of the amplifier at the fundamental frequency. The key to achieving stable overtone oscillator operation is ensuring the existence of the above condition at the desired overtone while ensuring its failure at all other frequencies.

L1 and C1 are chosen so that

$$\frac{1}{2\pi\sqrt{L_1\,C_1}} > F_f$$

where F_f is the fundamental frequency of the crystal resonator. If L1 and C1 are chosen to be net capacitive at the desired overtone frequency and if the condition

$$gm\ Z_{c1}\ Z_{c2} > R_S$$

is true only at the desired overtone frequency, the oscillator will oscillate at the frequency of the overtone. Normally, L1 and C1 are not chosen to be resonant at the overtone frequency but at a lower frequency to ensure that the parallel combination of L1 and C1 is capacitive at the overtone frequency and inductive at the fundamental frequency.

$$F_f < \frac{1}{2\pi\sqrt{L_1\,C_1}} < F_o$$

The net inductance of the rest of the resonant loop then balances this capacitance at the overtone frequency.

$$\frac{1}{\dfrac{1}{X_{ls} - X_{cs}} - \dfrac{1}{X_{c0}}} + X_{l2} + X_{l(stray)} - X_{c3}$$

$$+ \frac{1}{\dfrac{1}{X_{l1}} - \dfrac{1}{X_{c1}}} = 0$$

L2 and C3 are chosen to provide the desired adjustment to the resonant overtone frequency. This is normally computed by calculating the expected ppm change at the resonant frequency and using this to define the value of the reactance necessary to produce this change.

$$\Delta F_f\ (ppm) = \frac{X\ (of\ L2\ and\ C3)}{Z\ (crystal\ at\ resonance)}$$

$$\Delta F_f\ (ppm) = X(of\ L2\ and\ C3)/Z(crystal\ at\ resonance)$$

The values needed for this calculation can be derived from the value of the fundamental frequency and C_o. If C_o is known or can be measured, C_s is defined as

$$C_s = \frac{C_o}{200}$$

for an AT cut crystal.

The fundamental frequency can be used to calculate the value for L_s using either the series resonant or parallel resonant formulas given earlier. Since the Q of the crystal,

$$Q = \frac{X}{R}$$

is usually sufficiently large at the resonant frequency so that

$$R_S << Z(crystal)$$

R_S can be ignored. The value for C3 and L2 are chosen so that

$$X_{C3} = X_{L2}$$

when C3 is adjusted to approximately half its maximum capacitance. At this setting, the combination produces a zero change in the overtone frequency. If C3 is then chosen so that X_{C3} at minimum capacitance is

$$[X_{C3}(max)] - X_{L2} >= \Delta F_f \text{ (ppm) } Z(crystal)$$

and L2 is approximately

$$X_{L2} = \frac{X_{C3}(max)}{2}$$

then

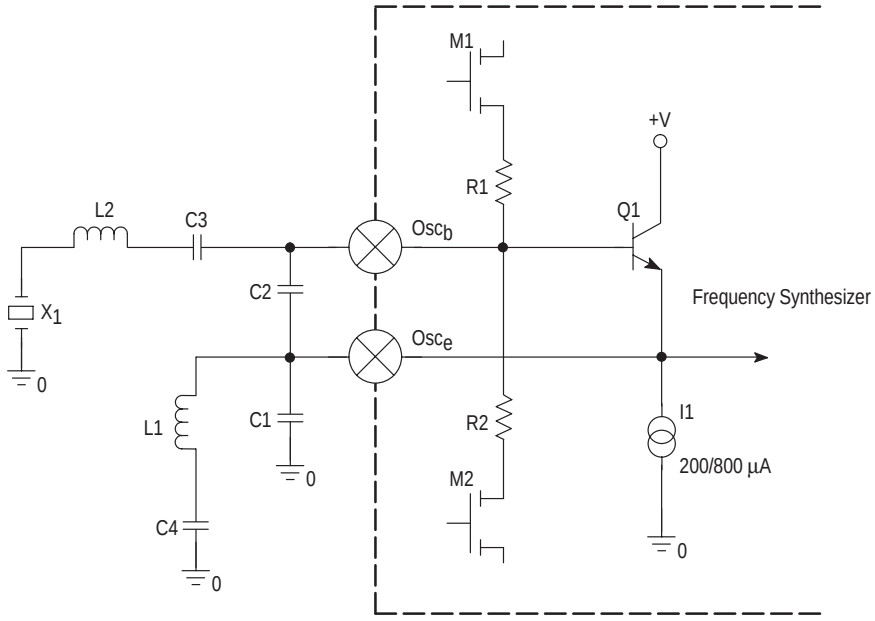
$$X_{C3}(max) >= 2[\Delta F_f \text{ (ppm)}]\ Z(crystal)$$

and

$$X_C(min) = \frac{X_C(max)}{4}$$

This results in an adjustable change in the operating frequency of $+[\Delta F_f \text{ (ppm)}]$ and $-[\Delta F_f \text{ (ppm)}]/2$. If ratios nearer to 1:1 are used for $X_{C3}(max)$ and X_{L2}, the tuning range will be skewed with a wider $-[\Delta F_f \text{ (ppm)}]$ but at the expense of less adjustability over the $+[\Delta F_f \text{ (ppm)}]$ range.

Figure 28. Colpitts Oscillator Configured for Overtone Operation



7B. MAIN LOOP FILTER DESIGN — CONVENTIONAL

The current output of the charge pump allows the loop filter to be realized without the need of any active components. The preferred topology for the filter is illustrated in Figure 29.

The R_o/C_o components realize the primary loop filter. C_a is added to the loop filter to provide for reference sideband suppression. If additional suppression is needed, the R_x/C_x realizes an additional filter. In most applications, this will not be necessary. If all components are used, this results in a fourth order PLL, which makes analysis difficult. To simplify this, the loop design will be treated as a second order loop (R_o/C_o), and additional guidelines are provided to minimize the influence of the other components. If more rigorous analysis is needed, mathematical/system simulation tools should be used.

Component	Guideline
C_a	$<0.1 \times C_o$
R_x	$>10 \times R_o$
C_x	$<0.1 \times C_o$

The focus of the design effort is to determine what the loop's natural frequency, ω_o, should be. This is determined by R_o, C_o, K_p, K_v, and N_t. Because K_p, K_v, and N_t are given, it is only necessary to calculate values for R_o and C_o. There are three considerations in selecting the loop bandwidth:

1. Maximum loop bandwidth for minimum tuning speed.
2. Optimum loop bandwidth for best phase noise performance.
3. Minimum loop bandwidth for greatest reference sideband suppression.

Usually a compromise is struck between these three cases, however, for a fixed frequency application, minimizing the tuning speed is not a critical parameter.

To specify the loop bandwidth for optimal phase noise performance, an understanding of the sources of phase noise in the system and the effect of the loop filter on them is required. There are three major sources of phase noise in the phase–locked loop — the crystal reference, the VCO, and the loop contribution. The loop filter acts as a low–pass filter to the crystal reference and the loop contribution. The loop filter acts as a high–pass filter to the VCO with an in–band gain equal to unity. The loop contribution includes the PLL IC, as well as noise in the system; supply noise, switching noise, etc. For this example, a loop contribution of 15 dB has been selected.

The crystal reference and the VCO are characterized as high–order 1/f noise sources. Graphical analysis is used to determine the optimum loop bandwidth. It is necessary to have noise plots from the manufacturers of both devices. This method provides a straightforward approximation suitable for quickly estimating the optimal bandwidth. The loop contribution is characterized as white–noise or low–order 1/f noise, given in the form of a noise factor which combines all the noise effects into a single value. The phase noise of the crystal reference is increased by the noise factor of the PLL IC and related circuitry. It is further increased by the total divide–by–N ratio of the loop. This is illustrated in Figure 30. The point at which the VCO phase noise crosses the amplified phase noise of the crystal reference is the point of the optimum loop bandwidth. In the example of Figure 30, the optimum bandwidth is approximately 15 kHz.

To simplify analysis further, a damping factor of 1 will be selected. The normalized closed loop response is illustrated in Figure 31 where the loop bandwidth is 2.5 times the loop natural frequency (the loop natural frequency is the frequency at which the loop would oscillate if it were unstable). Therefore, the optimum loop bandwidth is 15 kHz/2.5 or 6.0 kHz (37.7 krads) with a damping coefficient, $\zeta \sim 1$. T(s) is the transfer function of the loop filter.

where

N_t = Total PLL Divide Ratio — 8 x N
where (N = 25 ... 40),
K_v = VCO Gain – 2π Hz/V,
K_p = Phase Detector/Charge Pump Gain – A
$= (|I_{OH}| + |I_{OL}|) / 4\pi$.

Technically, K_v and K_p should be expressed in radian units [K_v (rad/V), K_p (A/rad)]. Since the component design equation contains the $K_v \times K_p$ term, the 2π cancels and the value can be expressed as AHz/V (amp hertz per volt).

Figure 29. Loop Filter

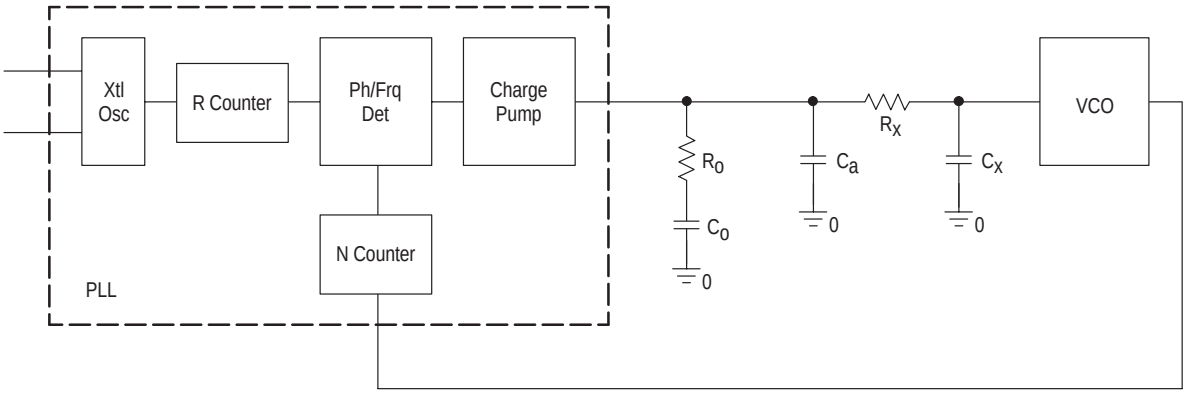


Figure 30. Graphical Analysis of Optimum Bandwidth

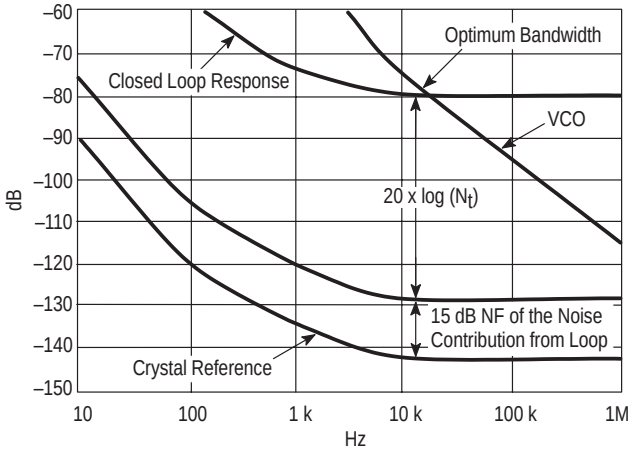
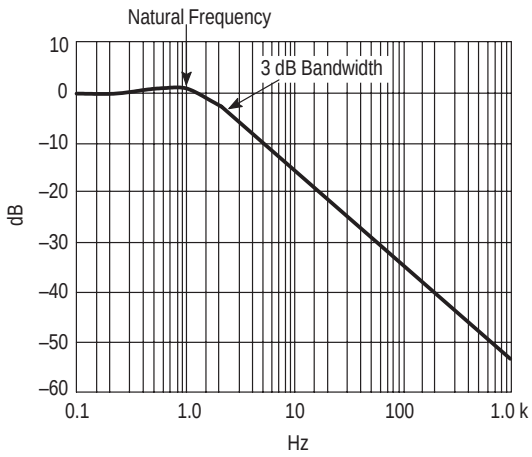


Figure 31. Closed Loop Frequency Response for ζ = 1



In summary, follow the steps given below:

Step 1: Plot the phase noise of crystal reference and the VCO on the same graph.

Step 2: Increase the phase noise of the crystal reference by the noise contribution of the loop.

Step 3: Convert the divide–by–N to dB (20log 8 x N) and increase the phase noise of the crystal reference by that amount.

Step 4: The point at which the VCO phase noise crosses the amplified phase noise of the crystal reference is the point of the optimum loop bandwidth. This is approximately 15 kHz in Figure 30.

Step 5: Correlate this loop bandwidth to the loop natural frequency per Figure 31. In this case the 3.0 dB bandwidth for a damping coefficient of 1 is 2.5 times the loop's natural frequency. The relationship between the 3.0 dB loop bandwidth and the loop's "natural" frequency will vary for different values of ζ. Making use of the equations defined in Figure 32, a math tool or spread sheet is useful to select the values for R_O and C_O.

Appendix: Derivation of Loop Filter Transfer Function

The purpose of the loop filter is to convert the current from the phase detector to a tuning voltage for the VCO. The total transfer function is derived in two steps.

Step 1 is to find the voltage generated by the impedance of the loop filter.

Step 2 is to find the transfer function from the input of the loop filter to its output. The "voltage" times the "transfer function" is the overall transfer function of the loop filter. To use these equations in determining the overall transfer function of a PLL, multiply the filter's impedance by the gain constant of the phase detector, then multiply that by the filter's transfer function. Figure 33 contains the transfer function equations for the second, third, and fourth order PLL filters.

PSpice Simulation

The use of PSpice or similar circuit simulation programs can significantly reduce laboratory time when refining a PLL design. The following describes the use of behavioral modeling to develop useful models for studying loop filter performance. In many applications the levels of sideband spurs can also be studied.

Behavioral modeling is chosen, as opposed to discrete device modeling, to improve performance and reduce simulation time. PLL devices can contain several thousand individual transistors. To simulate at this level can result in generation of an enormous amount of data when compared to a simpler behavioral model. For example, a logic NAND gate can contain several transistors. Each of these requires a data set for each of the transistor terminals. If a half dozen transistors are used in the gate design, both current and voltage measurements for each terminal of each device for every node in the circuit is calculated. The gate can be expressed as a behavioral model, which is treated and simulated as a single device. Since PSpice sees this as a single rather than multiple devices, the amount of accumulated data is much less, resulting in a faster simulation.

For applications using integrated circuits such as PLLs, it is desirable to investigate the performance of the circuitry added externally to the integrated circuit. By using behavioral modeling rather than discrete device modeling to represent the integrated circuit, the engineer is able to study the performance of the design without the overhead contributed by simulating the integrated circuit.

Phase Frequency Detector Model

The model for the phase frequency detector is derived using the waveforms shown in Figure 20. Two signals are present at the input of the phase frequency detector. These are the reference input and the feedback from the VCO and/or prescaler. The two signals are compared to determine the lag/lead relationship between the two signals and pulses generated to represent the leading edge of each signal. A pulse whose width equals the lead of one input signal over the other is generated by an RS flip–flop (RSFF). One RSFF generates a pulse whose width equals the lead of the reference signal over the feedback signal, and a second RSFF generates a signal whose width is the lead of the feedback signal over the reference signal. The logical model for the phase frequency detector is shown in Figure 34.

Figure 32. Design Equations for the Second Order System

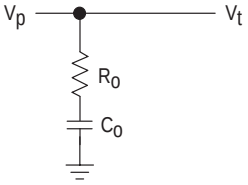
$$T(s) = \frac{R_0C_0s + 1}{\left(\frac{NC_0}{K_pK_v}\right)s^2 + R_0C_0s + 1} = \frac{\left(\frac{2\zeta}{\omega_0}\right)s + 1}{\left(\frac{1}{\omega_0{}^2}\right)s^2 + \left(\frac{2\zeta}{\omega_0}\right)s + 1}$$

$$\left(\frac{NC_0}{K_pK_v}\right) = \left(\frac{1}{\omega_0{}^2}\right) \rightarrow \omega_0 = \sqrt{\frac{K_pK_v}{NC_0}} \rightarrow \boxed{C_0 = \left(\frac{K_pK_v}{N\omega_0{}^2}\right)}$$

$$R_0C_0 = \left(\frac{2\zeta}{\omega_0}\right) \rightarrow \zeta = \left(\frac{\omega_0R_0C_0}{2}\right) \rightarrow \boxed{R_0 = \left(\frac{2\zeta}{\omega_0C_0}\right)}$$

Figure 33. Overall Transfer Function of the PLL

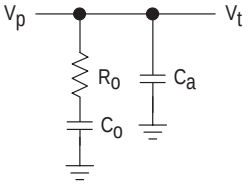
For the Second Order PLL:



$$Z_{LF}(s) = \frac{R_0C_0s + 1}{C_0s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1 \quad , \quad V_p(s) = K_p(s)Z_{LF}(s)$$

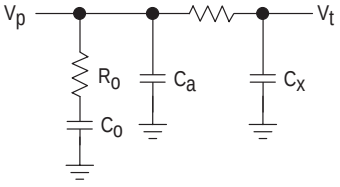
For the Third Order PLL:



$$Z_{LF}(s) = \frac{R_0C_0s + 1}{C_0R_0C_as^2 + (C_0 + C_a)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1 \quad , \quad V_p(s) = K_p(s)Z_{LF}(s)$$

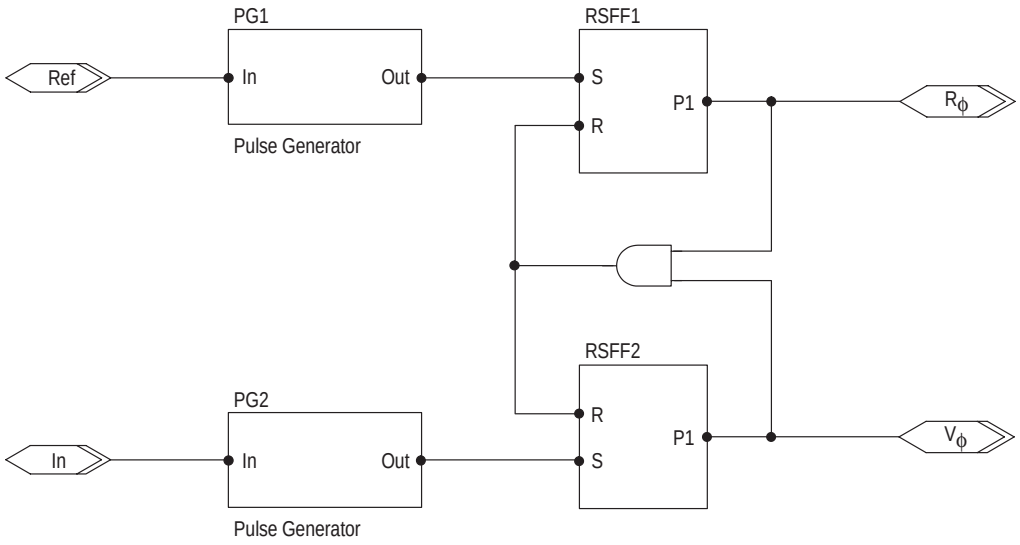
For the Fourth Order PLL:



$$Z_{LF}(s) = \frac{(R_0C_0s + 1)(R_xC_xs + 1)}{C_0R_0C_aR_xC_xs^3 + [(C_0 + C_a)R_xC_x + C_0R_0(C_x + C_a)]s^2 + (C_0 + C_a + C_x)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = \frac{1}{(R_xC_xs + 1)} \quad , \quad V_p(s) = K_p(s)Z_{LF}(s)$$

Figure 34. Phase Frequency Detector Logic Diagram



The behavioral model of the phase frequency detector shown in Figure 35 is derived using the phase frequency detector logic diagram. Behavioral models for the pulse generator, AND gate (Figure 36), and RS flip–flops (Figure 37) are created using analog behavioral blocks. The pulse generator is created using a delay block and a “gate” defined by the behavioral expression:

If [V(v1) ≥ 1 & V(v2) , 1, 5, 0]

v1 and v2 represent the two inputs to the block.

This is the behavioral expression for an AND gate with one input inverted. The addition of the delay element produces a pulse whose width equals the delay element.

The pulses appearing at the output of HB1 and HB2 (Figure 35) are used to set the flip–flops, RSFF1, and RSFF2. The leading pulse will set the appropriate flip–flop resulting in a high at the output of that flip–flop. The output of this flip–flop will remain high until the arrival of the second (or lagging) pulse sets the second RS flip–flop. The presence of a high on both RS flip–flop outputs results in the generation of the reset pulse. The reset pulse is generated by the analog behavioral block (configured as an AND gate) and the delay element. The delay element is necessary to eliminate the zero delay paradox of input to output to input.

The output of the phase frequency detector is two pulse trains appearing at R_ϕ and V_ϕ. When the PLL is locked, the pulses in both pulse trains will be of minimum width. When the phase frequency detector is out of lock, one pulse train will consist of pulses of minimum width while the width of the pulses in the second train will be equal to the lead/lag relationship of the input signals. If the Ref input leads ‘In’, the pulse train at R_ϕ will consist of pulses whose width equals the lead of Ref. If Ref lags ‘In’, the width of the pulses appearing at V_ϕ will equal this lag.

The terms lead and lag used in this explanation represent an occurrence in time rather than a phase relationship. At any condition other than locked, one input (either In or Ref), will be of a higher frequency. This results in the arrival of the pulse at that input ahead of the pulse at the other input, or leading. The second then is lagging.

To simulate the operation of the phase frequency detector in an actual circuit, a charge pump needs to be added. The behavioral model for this is shown in Figure 38. Two voltage–to–current behavioral models are used to produce the charge pump output. Two voltage–controlled switches with additional behavioral models, monitor the voltage of the output of the charge pump and clamp to 0 or V_{CC} to simulate a real circuit.

To ensure the model conforms to the PLL, the delay blocks in the phase frequency detector should be set to the expected value as specified by the MC145181 data sheet. In addition, the charge pump sink and source current behavioral model should also be set to deliver the desired current and V_{CC} specified to ensure correct clamping.

Modeling the VCO

The VCO (Figure 39) is also modeled using Analog Behavioral Modeling (ABM). The model used in the following examples assumes a linear response; however, the control voltage equation can be modified as desired. The circuit is modeled as a sine generator controlled by the control voltage. The sine generator can be modeled using the EVALUE function or the ABM function. In Figure 39, the EVALUE function is used to generate the divided output and the ABM function is used for the undivided output. Either the GVALUE or the ABM/I function can be used for the control voltage.

Figure 35. Behavioral Model of the Phase Frequency Detector

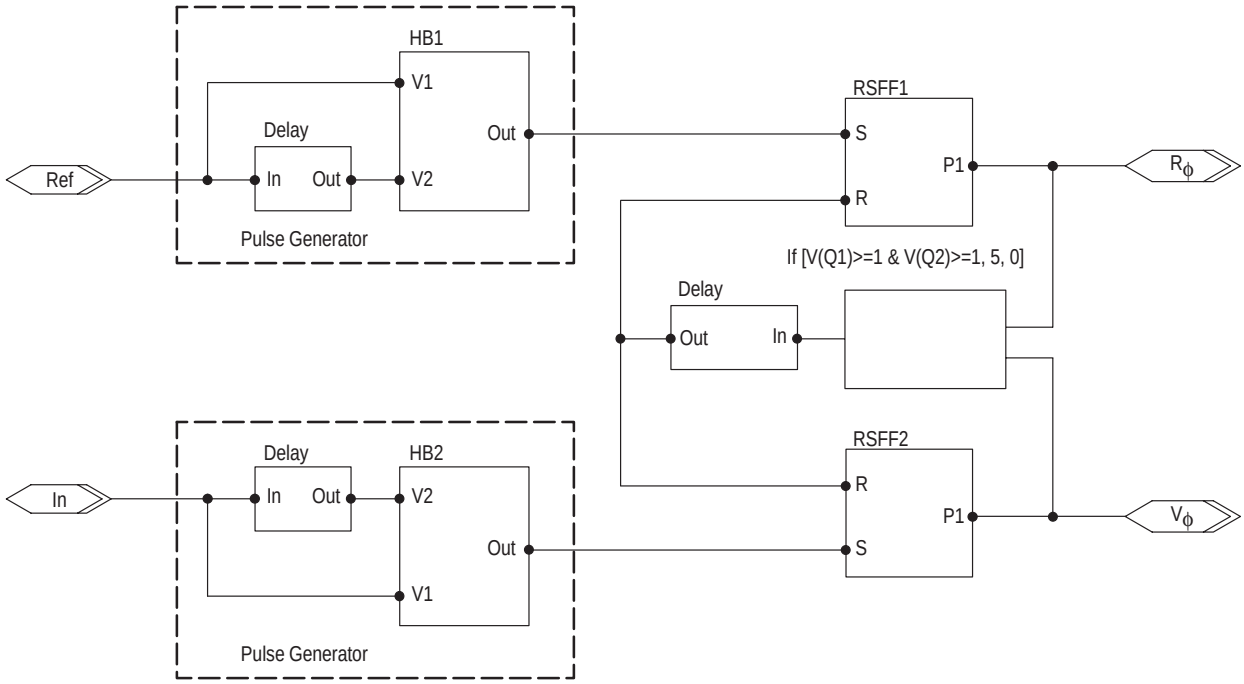


Figure 36. Behavioral Block Used for the Pulse Generator

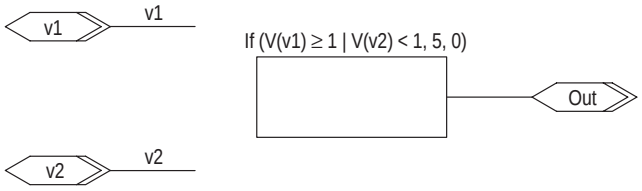


Figure 37. Behavioral Block Used as an RS Flip–flop

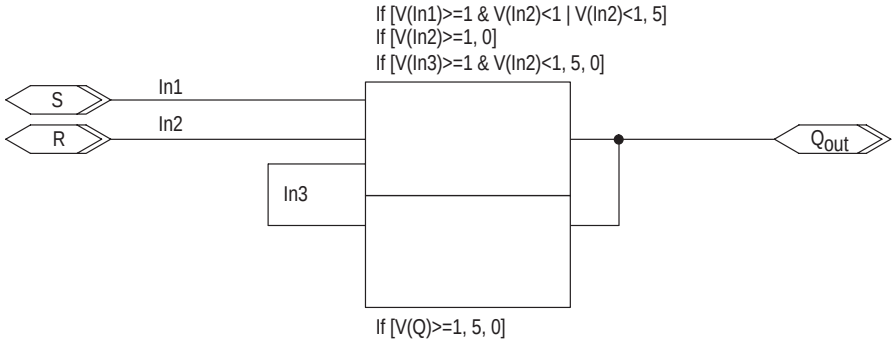


Figure 38. Charge Pump Model

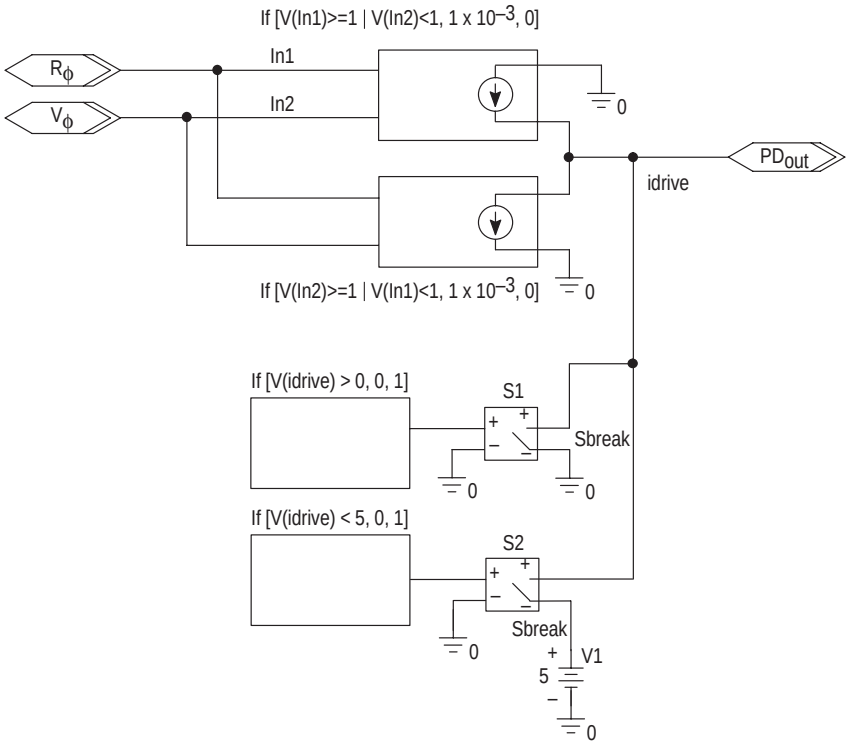
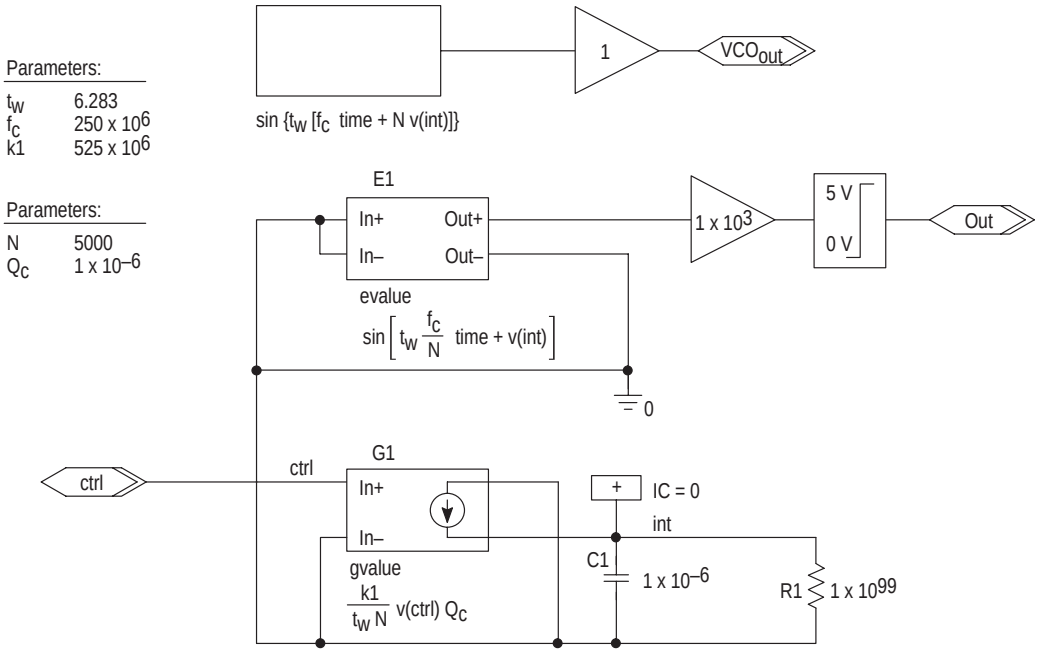


Figure 39. VCO Behavioral Model



The equation for the sine generator is:

$$e = \sin\left[t_W \frac{f_C}{N} \text{ time} + v(\text{int})\right] \quad .$$

f_C is defined as the output frequency when the control voltage is 0. This is the expected VCO frequency before frequency division. For the purpose of simulation, the counter value, N, has been written into the equation to ensure the correlation between the modeled circuit and the mathematical loop filter calculations. t_W is 2π; additional decimal places can be added as needed. v(int) is the control voltage effect and is defined in these examples as:

$$v(\text{int}) = \frac{k1}{t_W N} v(\text{cntl}) \; 1 \times 10^{-6} \quad .$$

where k1 is the VCO gain in rad/V.

The value C1 in the schematic of the VCO can be arbitrarily changed; however, the value must match that of Q_C. Q_C determines the value of the current to be integrated by the capacitor C1. R1 is arbitrarily set to 1×10^{99} and is not an active part of the circuit; however, it must be included to prevent open pin errors from the PSpice software. The GVALUE function is used to perform the generation of v(int). There is some interaction between the integrator, (GVALUE output and C1) and R1. V(int) is a continuous ramp that is loaded by the resistance of R1. Unless the GVALUE output current is sufficiently large for the value chosen for R1, the VCO control voltage required to maintain lock will increase throughout the simulation producing nonlinear operation. Modifications to the circuit can be performed either by changing the values in the parameter list or for major changes to the VCO characteristics, the equations for the sine generator, or control voltage can be altered.

The output of the sine generator is amplified by 1000 to produce a sharp rise/fall time and the output limited to swing between the values of 0 V and 5 V to convert it to a digital output. The resultant circuit/symbol accepts a voltage input from the loop filter and produces a square wave output at the desired frequency. This frequency should be chosen to represent the frequency present at the output of the N counter of the PLL frequency synthesizer.

The second output represented by the ABM function is a sine wave output of the frequency expected from the actual VCO. The primary purpose of this output is to allow full frequency simulation for spectrum analysis. By running a transient analysis of sufficient time, it is possible to determine spur content and level. If sufficient resolution is used in the simulation, the PSpice probe FFT transform can be used to provide the typical spectrum analyzer display.

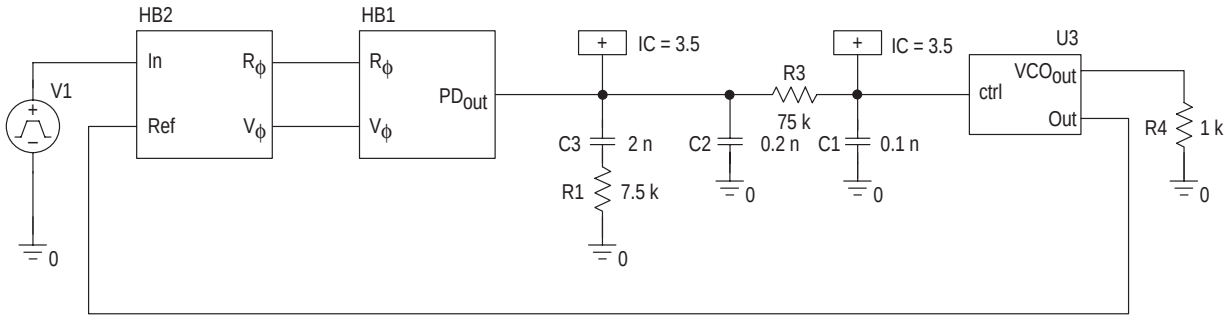
Loop Filter Simulation

The circuit shown in Figure 40 is used to simulate the closed loop operation for a single charge pump output. Component values for the loop filter should be computed using information from the previous section. Initial conditions can be set using the “IC1” symbol with starting values specifying the initial condition.

By adjusting component values for the loop filter, performance of the closed loop operation can be monitored. The control voltage to the input of the VCO can be monitored for a variety of conditions including settling time, lock time, and ripple present at the VCO input. In addition, the output of the VCO can be monitored for spur sidebands caused by ripple on the loop filter output; however, expected operation at high frequencies may be difficult due to the excessive data that can be generated.

As the divider ratio, N, increases for a fixed step frequency, the number of data points required to obtain sufficient information to overcome aliasing problems may become excessively large. In addition, the number of samples required should be three or more per cycle. For VCO frequencies in the range of 500 MHz, this means the step ceiling needs to be in the range of 100 to 500 ps. If a simulation time of 1 ms is needed, the actual computer time can be several hours with data accumulation in the 1– to 2–Gbyte range.

Figure 40. PLL Closed Loop Model



7C. MAIN LOOP FILTER DESIGN — ADAPT

Introduction

For PSpice simulation, the schematic model shown in Figure 41 was chosen. The classical PLL model employing a phase–frequency detector, a VCO, and an adaptive loop filter is used to simplify visualization of circuit operation. The parameter tables allow for modification of circuit performance by providing an easy method for altering critical values without necessitating changes to sub–level schematics. The definition for the terms are:

t_W = 2π,

f_r = reference frequency,

t_d = time delay; allows delay of the start of the high current mode (used to perform reference spur measurements),

CPL = charge pump low current,

CPH = charge pump high current,

N = N counter value,

S_Z = amount the N counter is being increased (or decreased) by,

S_t = number of f_r cycles that CPH is active; this value is either 16, 32, 64, or 128,

VCPHH = charge pump voltage – high,

VCPHL = charge pump voltage – low,

K1 = VCO gain (Hz/volt),

f_C = VCO frequency at 0 V control voltage,

H = reference spur scaling factor.

Modeling the Phase–frequency Detector

Figure 42 is a schematic of the phase–frequency detector. It includes the reference oscillator model, phase–frequency detector model, and charge pump models. V1 is the control element used to generate the step time for switching between CPL and CPH. The signal source VPULSE, is used to simulate the timer that controls when CPL and CPH are turned on. PW calculates the pulse width that simulates the counter from the values for S_t and f_r that are entered in the parameter tables on the top level schematic.

Figure 41. Top Level PLL Model

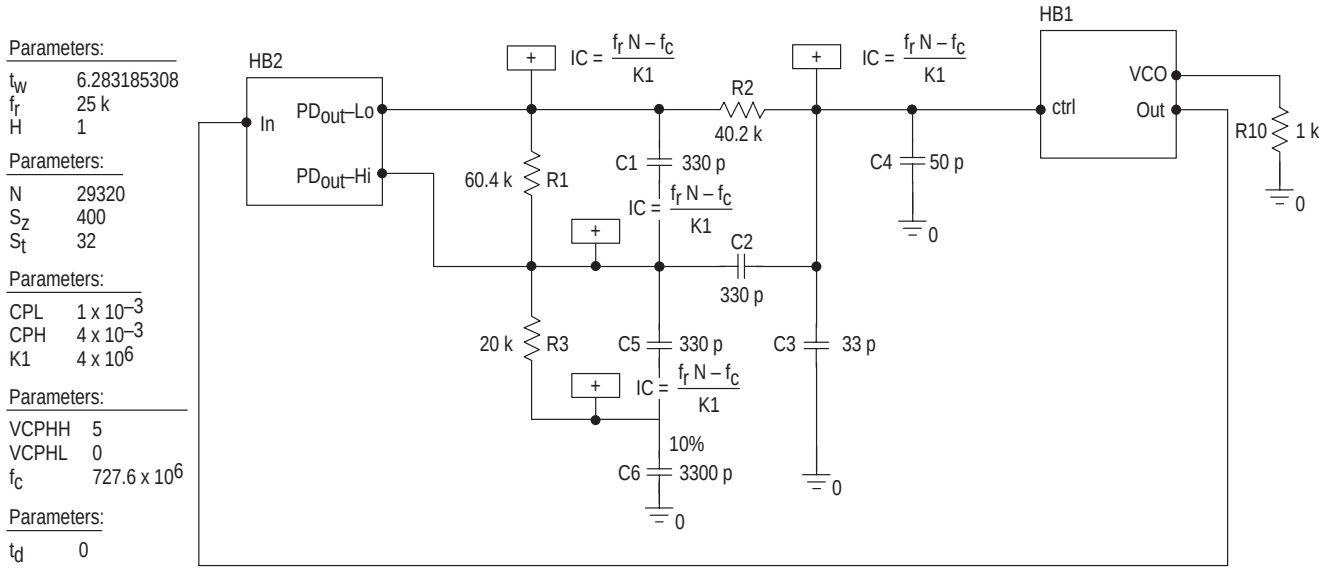
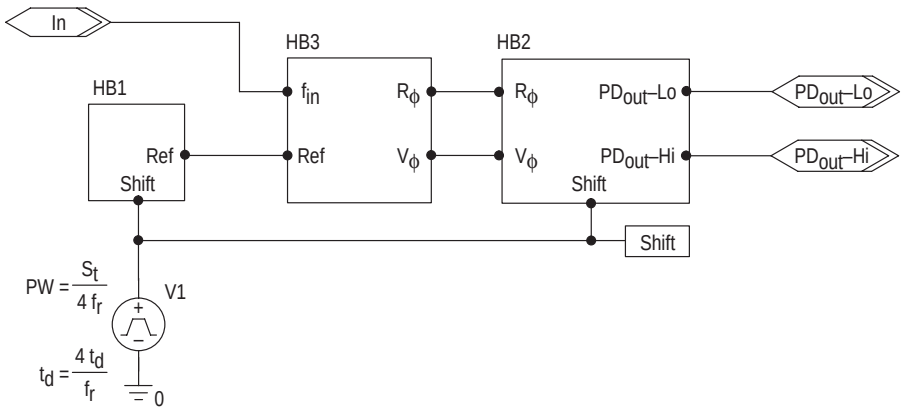


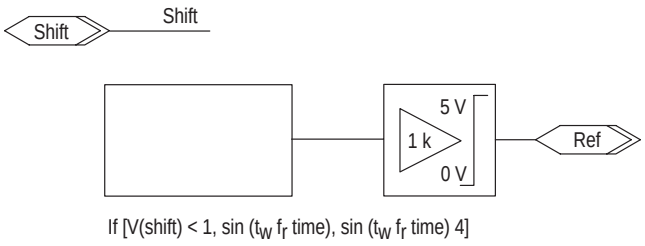
Figure 42. Phase–frequency Detector with Dual Charge Pumps



Reference Oscillator

The reference oscillator is shown in Figure 43. The oscillator is modeled using an analog behavioral block. The function for the block is written as an “If” condition. If the signal shift is low, the reference frequency f_r will be generated if shift is high, a signal of four times f_r will be generated. The limiter/gain block converts the low level sine wave output of the analog behavioral block into a square wave. The values of 0 for the low value and 5 for the high value are used throughout. These values are chosen out of habit and are not critical in an analog behavioral environment, providing the conformity is universal throughout the design.

Figure 43. Reference Oscillator



Phase–frequency Detector

The actual phase–frequency detector model minus reference oscillator and charge pumps is shown in Figure 44. The detector is composed of three delay modules: a behavioral AND gate, and two RS flip–flops. The STP function resets the phase/frequency detector logic on initiation of the simulator. The circuit for the behavioral RS flip–flop is shown in Figure 45.

The RS flip–flop equation illustrates the benefit of using the behavioral block instead of using a primitive logic element. A delay block and the behavioral gate equation generate a pulse whose width is equal to the value of the delay block. To generate the output using a primitive logic element such as a NAND gate, an inverter would be necessary to invert one of the NAND inputs. This approach requires three elements to be used instead of the two of the behavioral approach just for the pulse generator. In the behavioral approach, the equation for the behavioral AND gate is folded into the RS flip–flop, eliminating a separate gate altogether. Constructing the model with classic logic elements would require two NOR gates for the flip–flop, a delay element, an inverter, and an AND gate; five elements as compared with three for the behavioral approach. Since the RS flip–flop is used in two places in the model, four less components are needed for simulation. Since the speed of the simulation is directly impacted by the number of components being simulated, any reduction in the total number of components is a savings in simulation time and computer memory.

The RS flip–flops generate the lead or lag outputs that are used to “steer” the VCO. The pulse generator equation produces narrow pulses coincident with the leading edge of each of the input signals. These pulses set the appropriate RS flip–flop. Once set, the leading flip–flop must wait until the lagging flip–flop is also set. The behavioral AND gate provides the necessary output pulse to reset the flip–flops. The delay element placed at the output of the behavioral AND gate prevents an undefined state for the detector. The value 5 ns is chosen to correspond with the data sheet. The logic functions as a three state phase/frequency detector with an operating range of $\pm 2\pi$. R_ϕ and V_ϕ deliver positive pulses, whose width represents the amount of the lead of each input over the other input.

Figure 44. Phase–frequency Detector Logic

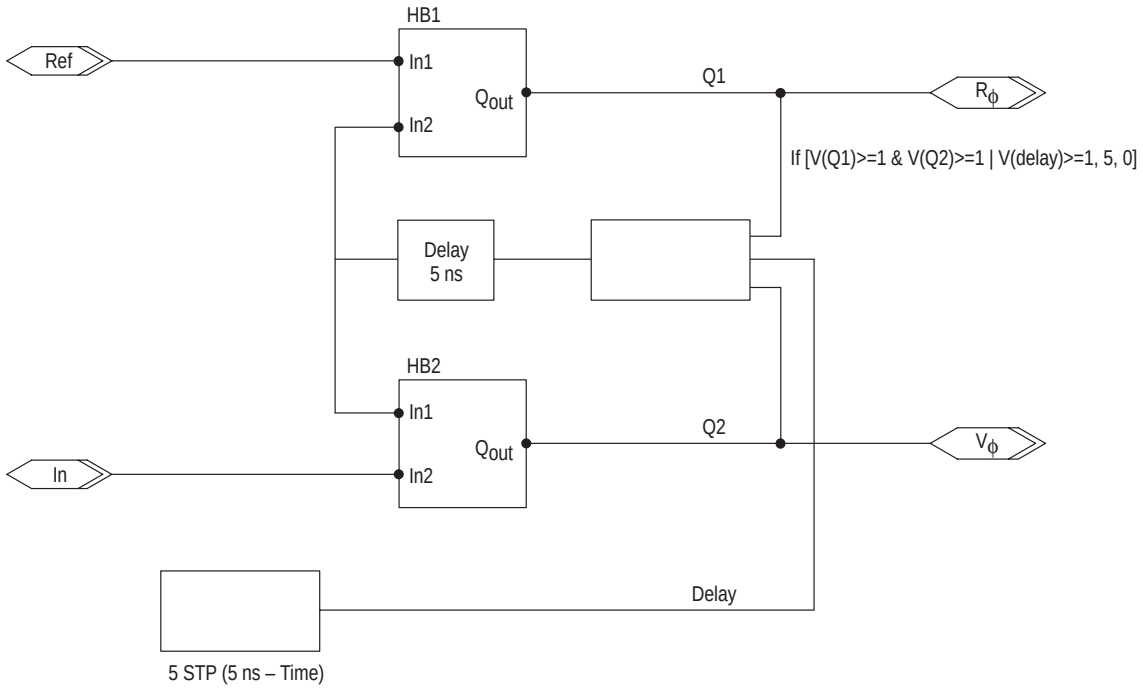
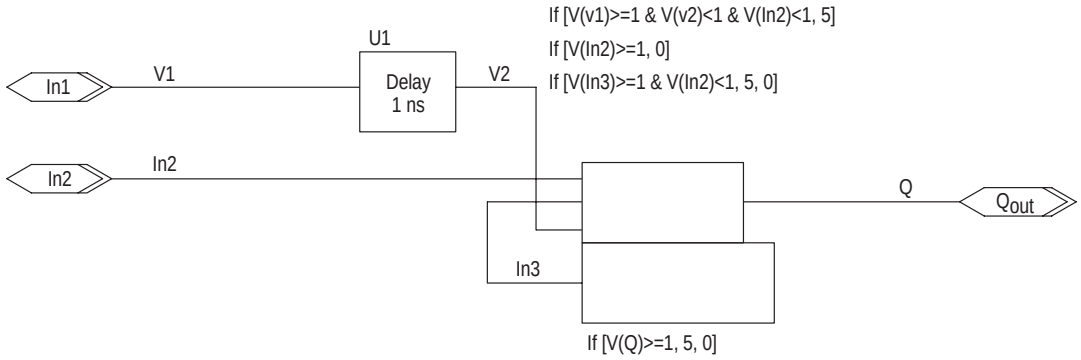


Figure 45. Behavioral RS Flip–flop



Charge Pump Model

The schematic used for the charge pump in the phase–frequency detector model is shown in Figure 46. Each charge pump is made from two analog behavioral blocks. The blocks chosen are three input behavioral blocks with current outputs. The two blocks are connected in push–pull to generate the appropriate source and sink output. The output of each block is defined using an “If” statement to monitor the input signals and generate the correct output at the appropriate time.

One note about this type of design. SPICE does not limit the output voltage swing necessary to generate the programmed current. It is possible to implement values for the loop filter, which will cause the charge pump to exceed the rail voltage. To limit the output voltage to prevent exceeding the value of the rails, the two behavioral blocks, voltage–controlled switches S1 and S2, and constants VCPHH and VCPHL are added. S1 and S2 on/off resistance is set to 1 Ω and 1 x 10^{12} Ω, and the off/on voltage is set to 0 V and 1 V to correspond to the behavioral blocks. The values defined by the constants are accessible from the parameter tables on the top level schematic.

VCO Model

The model used for simulating the VCO is shown in Figure 47. The VCO is composed of a sine wave generator and a control element. An analog behavioral block is used as a sine wave generator and a GVALUE element is used as a control element. The GVALUE is operated as an integrator. The output of the integrator is defined as

$$v(int) = k1\ v(ctrl)\ Q_C \quad .$$

The block designated to provide the feedback to the phase–frequency detector uses a single input analog behavioral block. The signal shift generated by V1 in the phase–frequency detector block is used to define the output frequency of the behavioral block. In this manner, the switching of the N and R values for the programmable counters can be simulated. In the implementation shown, the two frequencies will be either 25 kHz or 100 kHz when locked to the reference oscillator.

The other behavioral block is used to generate a VCO output dependent on the loop, but not contributing to the operation of the loop. This is used to emulate the actual VCO output with one modification. “H” has been added to the equation generating the sine wave. If H is defined as 1, the sine wave generated will be the same as the expected VCO output. If H is chosen as some value greater than 1, the frequency of the output will be reduced accordingly. This is useful when running simulations designed to show reference spur levels.

In cases where it is desirable to view reference spur levels, simulation can become difficult or impossible. For example, consider the circuit that is being discussed. This circuit represents the evaluation kit (MC145230EVK) using a VCO tunable between 733 MHz to 742 MHz, with a step frequency of 25 kHz.

NOTE

This example is for reference only. The maximum operating frequency of the MC145181 is 550 MHz. Operation of the VCO at frequencies greater than 550 MHz requires the inclusion of additional external division such as a prescaler.

To obtain useful information from the simulation, a sampling rate greater than the Nyquist limit must be used (three to five samples per cycle). This dictates a step size less than 1/2 nanosecond. Additionally, the reference frequency is only 25 kHz. To accurately represent the conditions for spur generation, the simulation time must be long enough to include a sufficient number of f_r periods. Otherwise, no spurs are generated. In addition, the data file system is limited to 2 Gbyte, either in the NT 4.0 operating system or in PSpice itself. If the file exceeds 2 Gbyte, the data is discarded. To simulate reference spur generation at 730 MHz, a 1 ms simulation time was chosen. The simulation ran for several hours and generated a data file just under 2 Gbyte. The result is shown in Figure 48. The plot obtained from the EVK is shown in Figure 49 for comparison.

Figure 46. CPL and CPH Charge Pumps

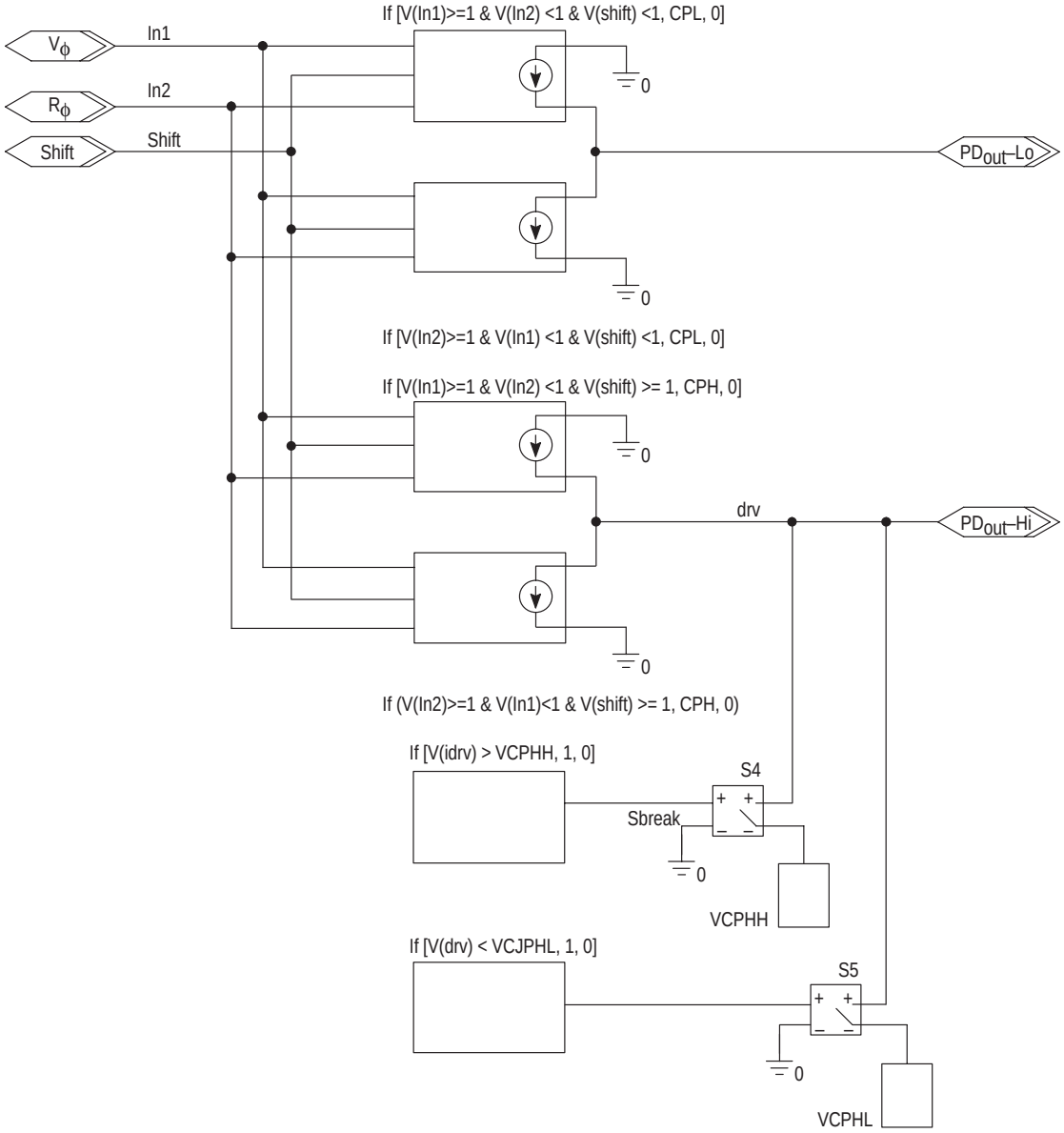


Figure 47. VCO Model

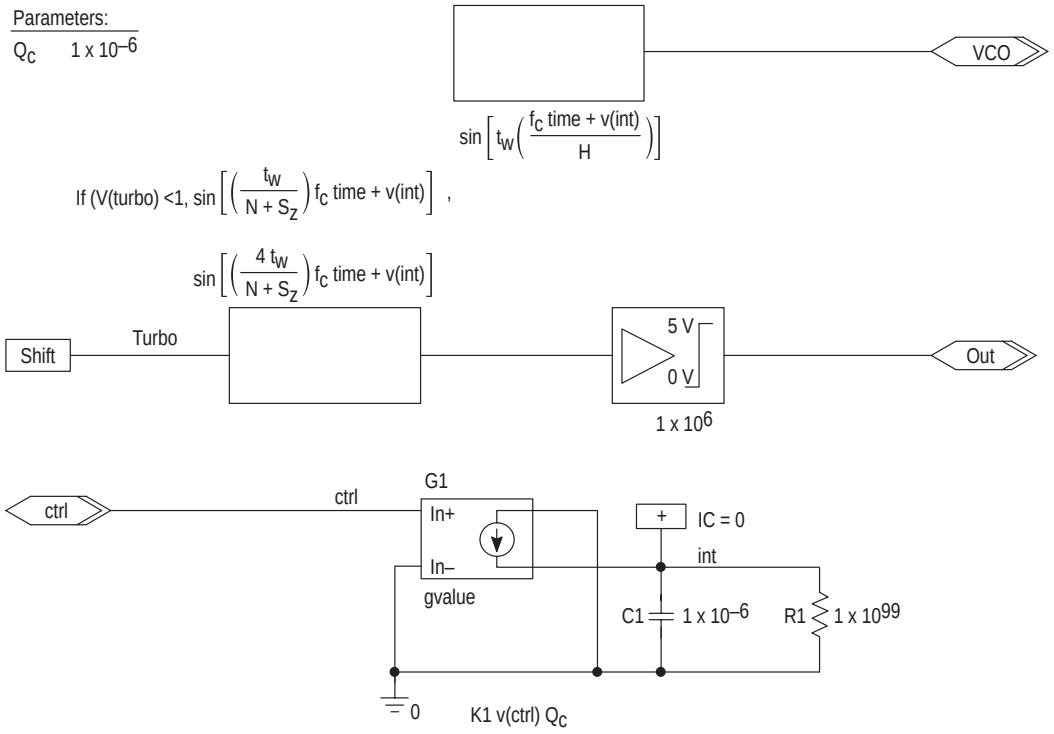


Figure 48. Reference Spur Simulation at 730 MHz

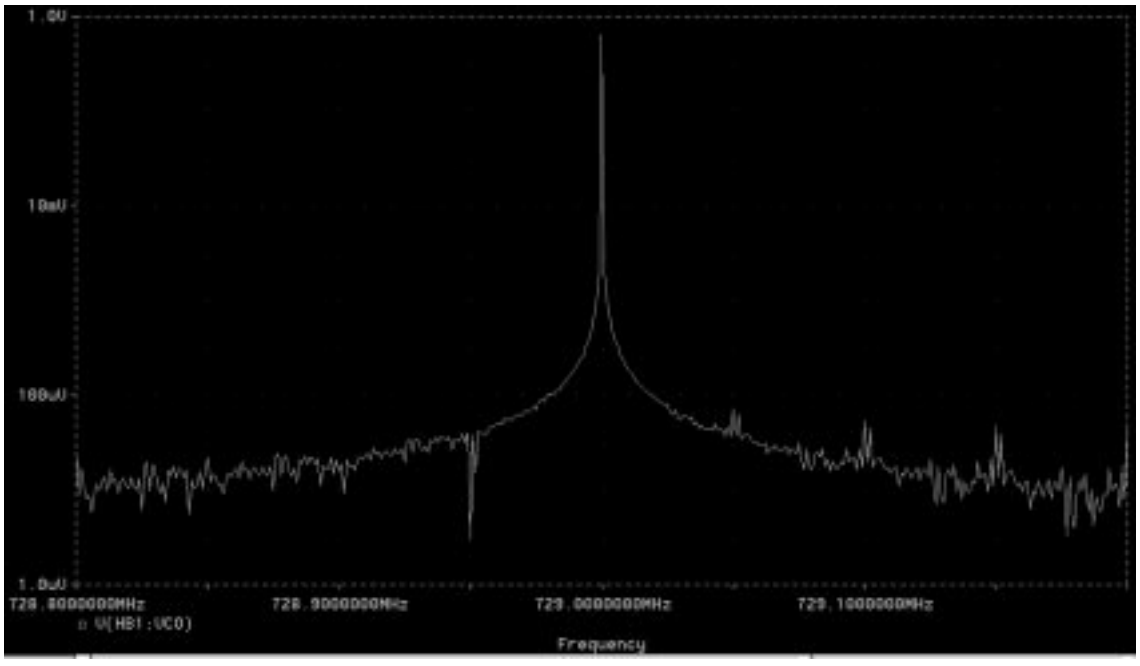
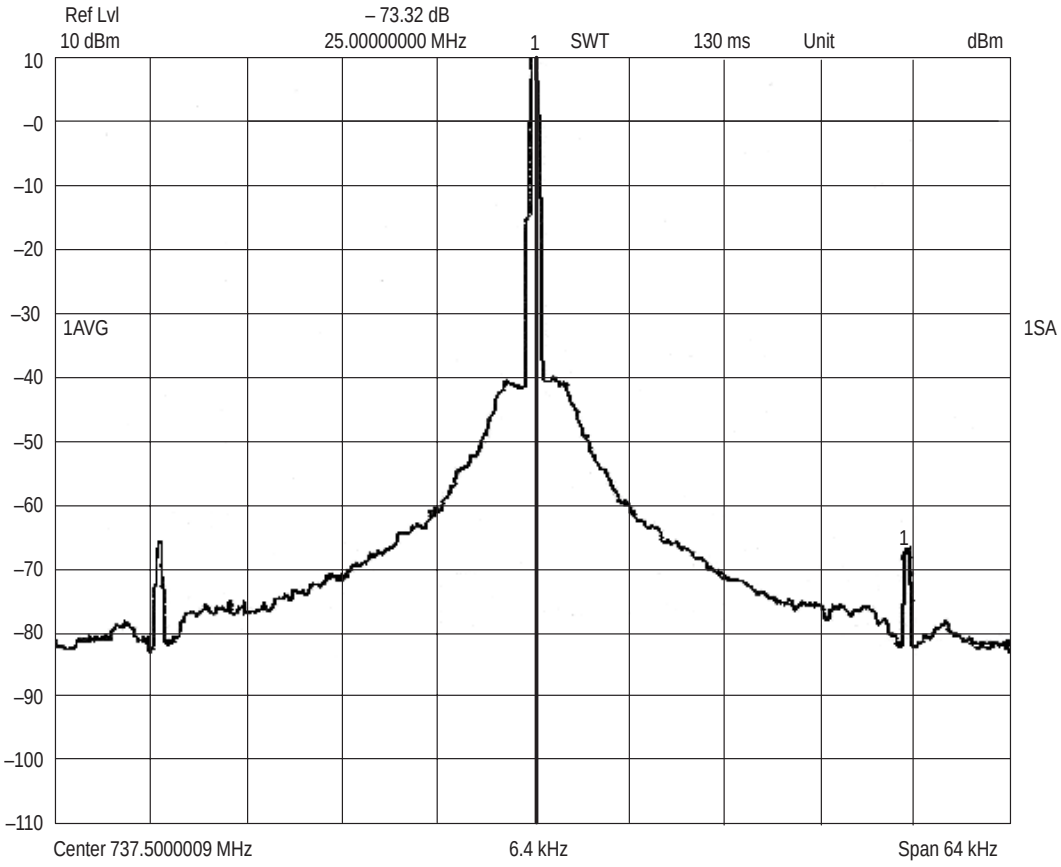


Figure 49. Sybil EVK Reference Spur Measurements



It should be noted that the reference spur values obtained from the simulation are lower than the values obtained from the actual EVK. This is because the simulation model is an "ideal" modeling of the PLL. To obtain results closer to the actual implementation, the models should be "massaged" to be more representative of the actual circuit. For example, spur levels more consistent with actual circuitry can be obtained by adding a resistance to ground at the input of the VCO to represent leakage. The value chosen should be consistent with VCO and circuit component performance.

To reduce simulation time, the H value may be used. By reducing the frequency of the VCO output, the number of samples required for simulation can also be reduced. The output shown in Figure 50 shows the result of dividing the VCO output of 730 MHz by 7.3 to produce a 100 MHz output. The reference spurs are better represented since adequate simulation time is possible.

To generate these outputs, the parameter values used were those shown on the top level schematic. The simulator was set to run a transient sweep, with t_d set for a delay that would prevent the 4X frequency from being started. The initial conditions were set to 1 V and the simulation run for 1 ms. VCO was monitored and the probe display button FFT was initiated. The X and Y axis were adjusted to those shown.

Note: These simulations are presented as the result of "ideal" models and may not accurately display real hardware. It would be best to load the VCO input with additional leakage devices such as a large resistance, to accurately display real conditions. These models are starting points for more accurate implementations.

Loop filter analysis is more accurate, since the predominate factors are in the loop filter itself. To simulate the performance of the loop filter, t_d is set for 0, N is set to the desired divider value, and S_Z is set to the desired step. For this example, 733 MHz was chosen.

NOTE

These values are for reference only. The maximum operating frequency of the MC145181 is 550 MHz. For VCO frequencies greater than 550 MHz, an added external divider such as a prescaler is necessary.

With the VCO model shown, V(ctrl) = 0 produces an output of 727.6 MHz and at V(ctrl) = 1.35 V, the VCO frequency would be 733 MHz; the minimum MC145230EVK default operating frequency. To show the response of the loop filter to a 10 MHz step at this operating frequency, S_Z = 10 MHz/ 25 kHz = 400. The simulation is run for 1 ms with a step ceiling of 100 ns. The result is shown in Figure 51.

If the simulation is examined over a longer period of time, the long term settling can be compared to the performance of the actual circuitry. The plot shown in Figure 52 shows the VCO control voltage with the display resolution set to 1 mV. This compares to the plot of frequency variation measurements made on the actual EVK. This plot is shown in Figure 53.

Figure 50. H Set to Generate a 100 MHz Output

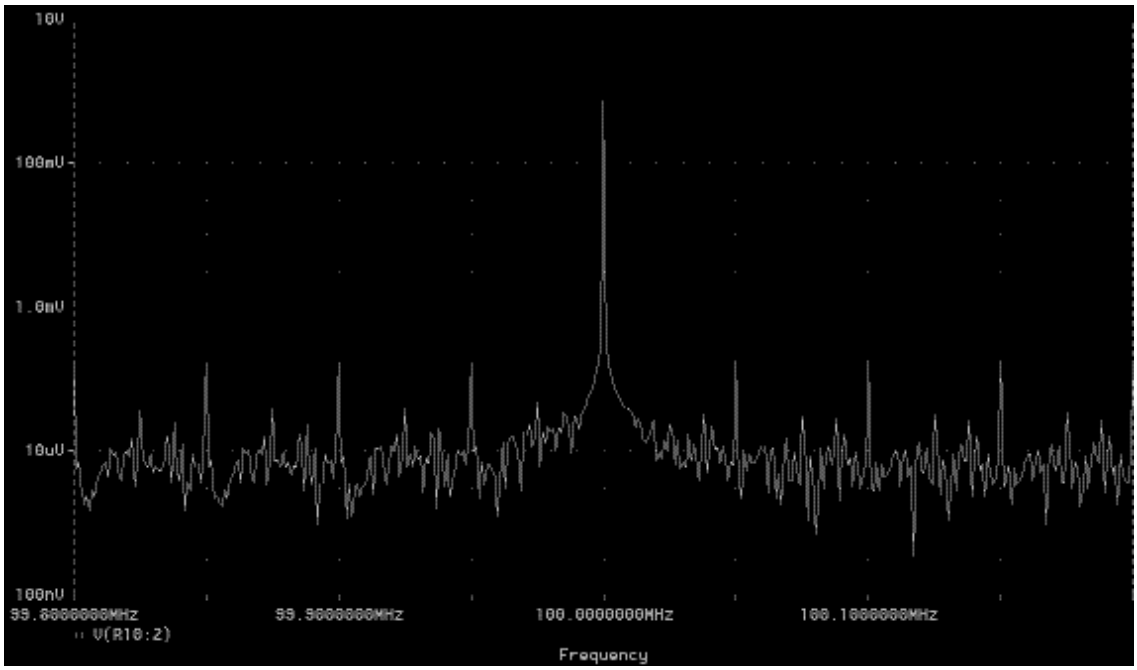


Figure 51. 10 MHz Step for an Operating Frequency of 729 MHz

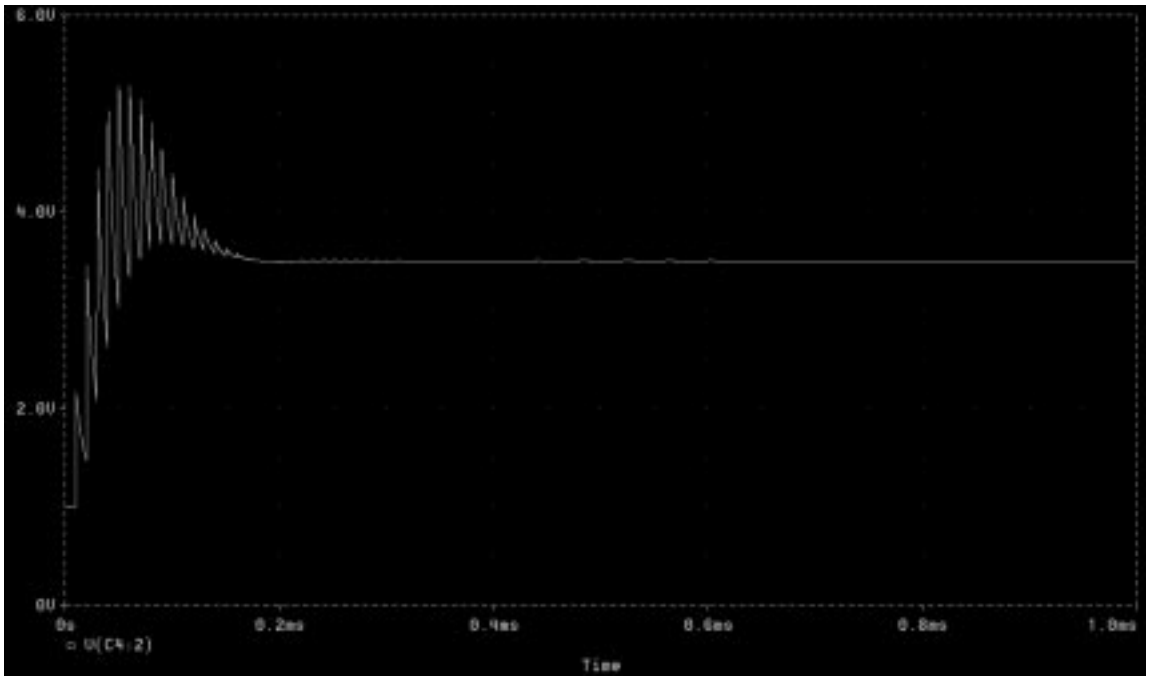


Figure 52. VCO Settling

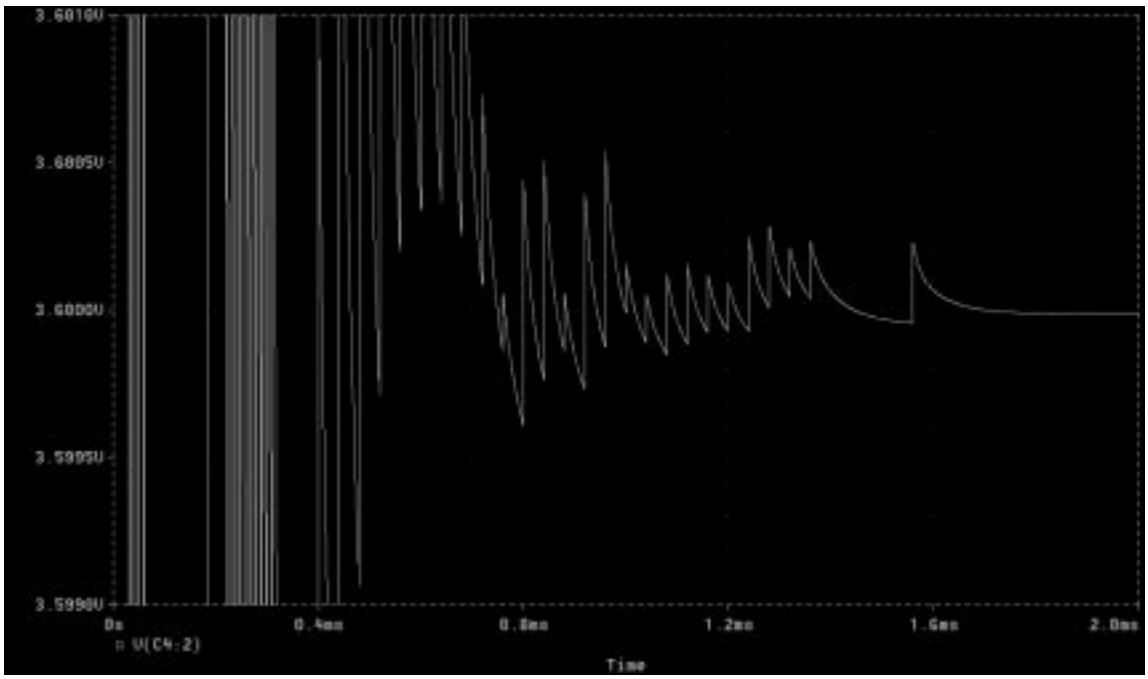
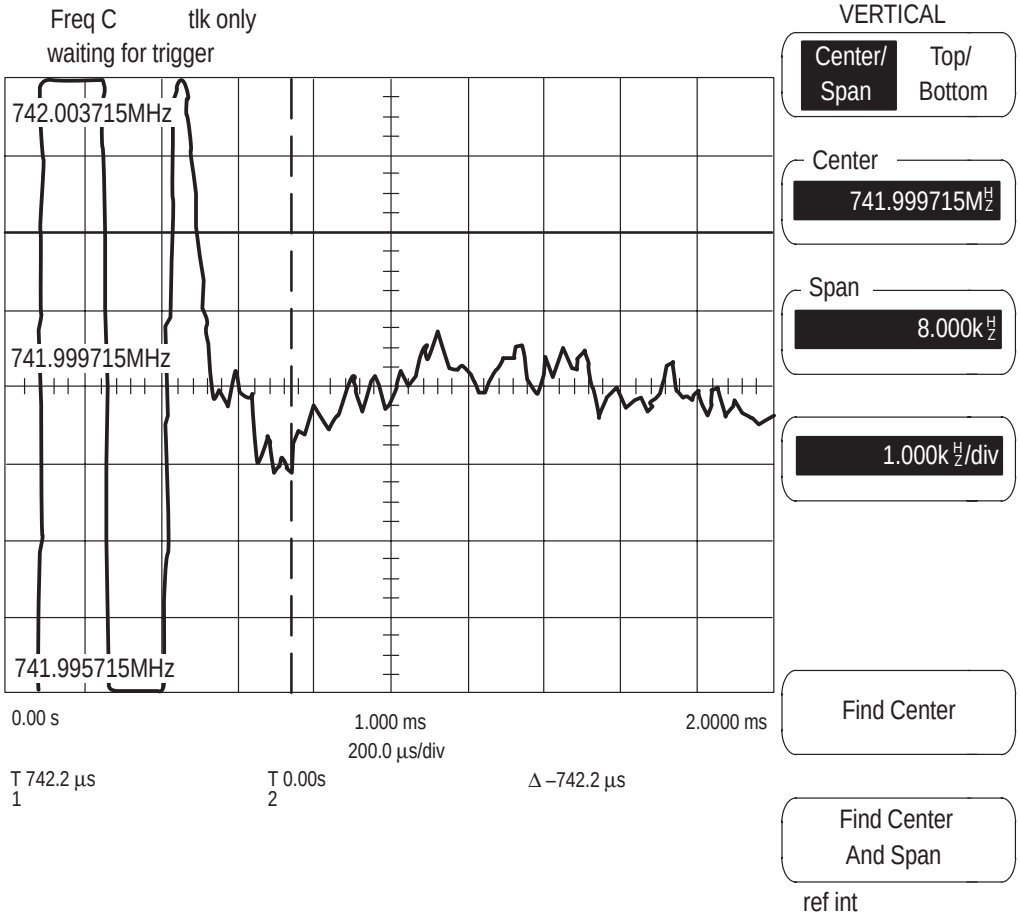


Figure 53. Frequency Settling of the EVK



It is noted that the results obtained from the simulation compare favorably to those obtained from the measurements of the EVK. The simulation display resolution is adjusted to represent the same ±4 kHz deviation as shown in Figure 53. Since variation in VCO control voltage is equal to the VCO frequency divided by the VCO gain, this axis may be redefined to show change in frequency rather than change in control voltage.

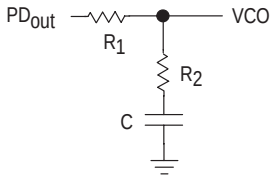
The models shown represent a “skeleton” that may be used to develop extensive and reliable simulations that can greatly reduce actual breadboarding and testing. In addition to the basic simulations shown, PSpice provides a method by which worst case and Monte Carlo evaluation can be performed on all, or selected components. By limiting the circuit to minimum necessary components, simulation can be performed using only the PSpice evaluation copy. In addition, the optional PSpice program Optimizer should allow refining the loop filter more easily.

While PSpice is a powerful tool, it is not without limits. Since it was designed to run on large mainframe computers, the PC is just now becoming powerful enough to make use of the capability of the simulator. A fast Pentium class processor with a large RAM and a hard drive of the Gbyte size is a necessity. Even with the most judicious planning, some simulations will “bump” the limits of the system.

7D. SECONDARY LOOP FILTER DESIGN

Low Pass Filter Design for PD_{out}'

The design of low pass filtering for PD_{out}' for the device can be accomplished using the following design information. In addition to the example included here, Motorola Application Note AN1207, also includes examples of active filtering which may be used to supplement this information.



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n\left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

Definitions:
N = Total Division Ratio in Feedback Loop
K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ V/radian for PD_{out}'
K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ V/radian for ϕ_V and ϕ_R

$$K_{VCO}\ (\text{VCO Gain}) = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$, where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Recommended Reading:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.

Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN*. March 5, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

AN1207, The MC145170 in Basic HF and VHF Oscillators, Motorola Semiconductor Products, Inc., 1992.

AN1671, MC145170 PSpice Modeling Kit, Motorola Semiconductor Products, Inc., 1998.

Example:

Given the following information:

VCO frequency = 45.555 MHz,

Frequency step size = 5 kHz,

VCO gain = 3.4 MHz/V.

Design a loop filter with a damping factor of 0.707.

The VCO is assumed to have a linear response throughout the range used in this example. The gain for the VCO has been given as 3.4 MHz/V and is multiplied by 2π rad/s/Hz for calculating loop filter values.

$K_{VCO} = 2\pi$ rad/s/Hz x 3.4 MHz/V = 2.136 x 10^7 rad/s/V .

The gain for the phase detector is defined as

$$K_\phi = \frac{V_{DD}}{4\pi}\ \text{V/rad for } PD_{out}' \ .$$

Using a value for V_{DD} (phase detector supply voltage) of 3.6 V with the output voltage multiplier turned off, the value is

$$K_\phi = \frac{3.6}{4\pi} = 0.2865\ \text{V/rad} \ .$$

Let

$$\omega_n = \frac{2\pi\, f_r}{50} = 628.3\ \text{rad/s}$$

and

$$N = \frac{F_{VCO}}{F_{\text{step size}}} = \frac{45.555\ \text{MHz}}{5\ \text{kHz}} = 9111 \ .$$

Choosing C = 0.05 μF and calculating R1 + R2,

$$R1 + R2 = \frac{K_\phi\, K_{VCO}}{N\, C\, \omega_n^2} = 34\ \text{k}\Omega \ .$$

With a damping factor of 0.707,

$$R2 = \frac{\dfrac{0.707}{0.5\,\omega_n} - \dfrac{N}{K_\phi\, K_{VCO}}}{C} = 15\ \text{k}\Omega \ ,$$

$R1 = (R2 + R1) – R2 = 34\ \text{k} – 15\ \text{k} = 19\ \text{k}\Omega \sim 20\ \text{k}\Omega$.

The choice for C is somewhat arbitrary, however, its value does impact the performance of the loop filter. If possible, a range of choices for C should be used to calculate potential loop filters and the resultant filters simulated, as will be shown below, to determine the best balance.

If additional filtering is desired, R1 may be split into two equal resistors and a capacitor to ground inserted. Since the closest resistance to one–half of 9 k is 4.7 kΩ, this value is chosen for $R1_a$ and $R1_b$. The maximum value for the added capacitance is based on the bandwidth of the original loop filter.

The general form for the transfer function for the passive filter shown in Figure 54, can be shown to have the form:

$$F(s) = K_h \left[\frac{s + \omega_2}{(s + \omega_1)(s + \omega_3)} \right]$$

where

$$\omega_1 = \frac{1}{(R1_a + R1_b + R2)\, C} \quad ,$$

$$\omega_2 = \frac{1}{R2C} \quad ,$$

$$\omega_3 = \frac{1}{\left[\frac{R1_a\, R1_b + R1_a\, R2}{(R1 + R2)} \right] C_c} \quad ,$$

where

$$R1 = R1_a + R1_b$$

and

$$\omega_3 > \omega_2 \quad .$$

Since splitting R1 into two equal values, $R1_a$ and $R1_b$, and inserting the capacitance between the junction of $R1_a$ and $R1_b$ does not change the position of the pole located at ω_1, the value of ω_1 remains

$$\omega_1 = \frac{1}{(R1_a + R1_b + R2)\, C} = \frac{1}{(R1 + R2)\, C} \quad .$$

The 0 identified at $\omega_2 = 1/R2\ C$ is also unaffected by the addition of C_c if $\omega_3 > \omega_2$.

Since

$$R1_a = R1_b = \frac{R1}{2} \quad .$$

the value of C_c can be determined by specifying the value for ω_3 and using the values already determined for R1 and R2. The rule of thumb is to choose ω_3 to be 10 x ω_B so as not to impact the original filter. ω_B can be found as

$$\omega_B = \omega_n \sqrt{[1 + 2\zeta^2 + \sqrt{(2 + 4\zeta^2 + 4\zeta^4)}]}$$

$$\omega_B = 628.3 \text{ rad/s} \sqrt{[1 + 2\,(0.707)^2 + \sqrt{(2 + 4\,(0.707)^2 + 4\,(0.707)^4)}]}$$

$$= 1.293 \times 10^3 \text{ rad/s} \quad .$$

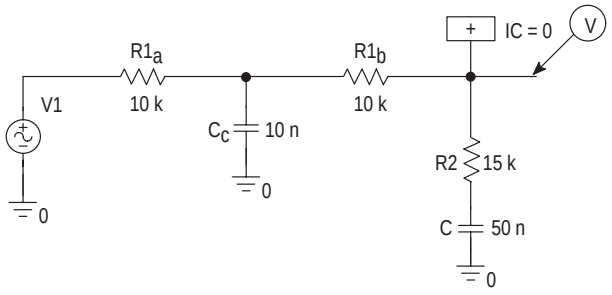
$$10\ \omega_B = 12.93 \times 10^3 \text{ rad/s} \quad .$$

The circuit for the passive loop filter is shown in Figure 54. R1 is split into two equal values and C_c inserted at the junction of $R1_a$ and $R1_b$. Using the values defined above, C_c is determined to be

$$C_c = \frac{1}{\left[\frac{R1_a\, R1_b + R1_a\, R2}{(R1 + R2)\ \omega_3} \right]}$$

$$= \frac{1}{\left[\frac{R1_a\, R1_b + R1_a\, R2}{(R1 + R2)\ 10} \right] \omega_B} = 10.83 \text{ nfd} \sim 10 \text{ nfd} \quad .$$

Figure 54. Passive Loop Filter for PD_{out}'



Open Loop AC Analysis of the Loop Filter

AC analysis is chosen for the mode of simulation for PSpice and VSIN is chosen for V1 and is set to produce a 1 V peak output signal. The simulation is then run and the result shown in Figure 55.

A Bode plot of the loop filter is obtained which describes the open loop characteristics of the loop filter. The corner frequencies of the filter can be modified and the simulation rerun until the desired wave shape is obtained. Since AC analysis runs much faster than transient analysis, the AC open loop analysis of the loop filter is much quicker and requires less resources than the closed loop transient analysis.

Closed Loop Filter Simulations Using PSpice

The top level schematic for simulating a simple loop filter for PD_{out}' operating closed loop, is shown in Figure 56. This filter uses the values calculated above.

The schematic represents the PLL function using the internal phase detector, PD_{out}', the loop filter calculated above, and a VCO. The parameter table allows altering the divider value of N, the maximum current obtained from PD_{out}', and PD_{out} charge pump voltage from the top level schematic.

The schematic for the VCO is shown in Figure 57. Analog behavioral modeling is used rather than discrete transistor modeling to reduce component count and improve simulation efficiency.

The behavioral VCO is composed of an integrator that transforms the input ctrl into the voltage control V(int) and a sine wave generator function whose frequency is controlled by V(int). EVALUE and GVALUE functions are used to perform the transforms. The analog behavioral models, ABM and ABMI, can also be used.

Figure 55. Bode Plot of the Passive Loop Filter

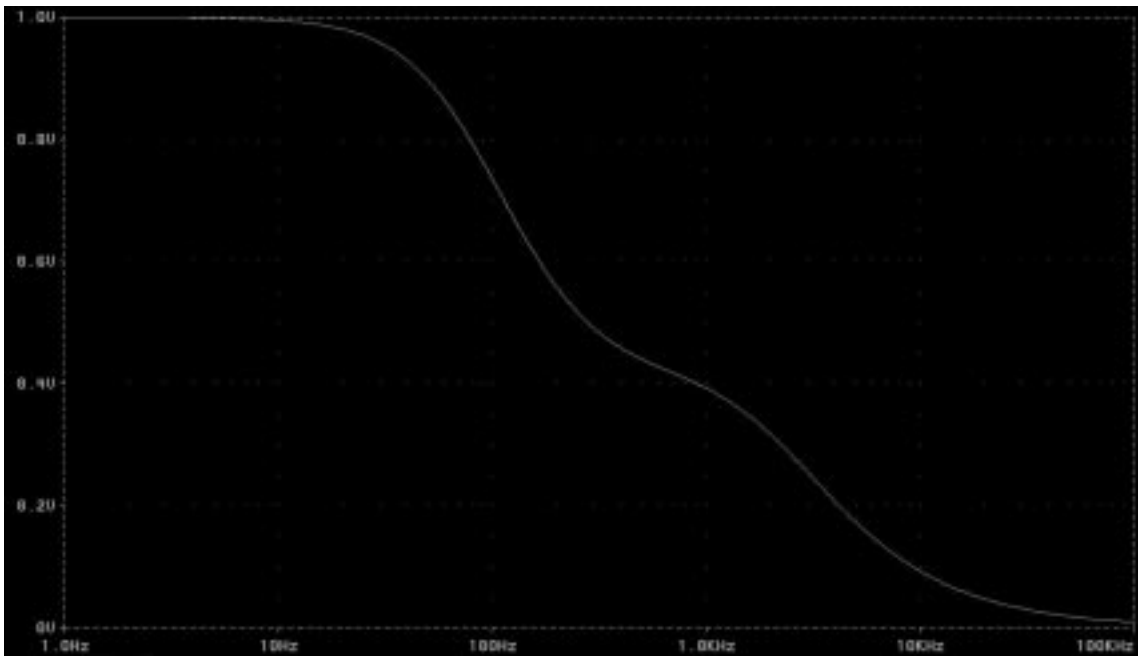


Figure 56. Passive Loop Filter

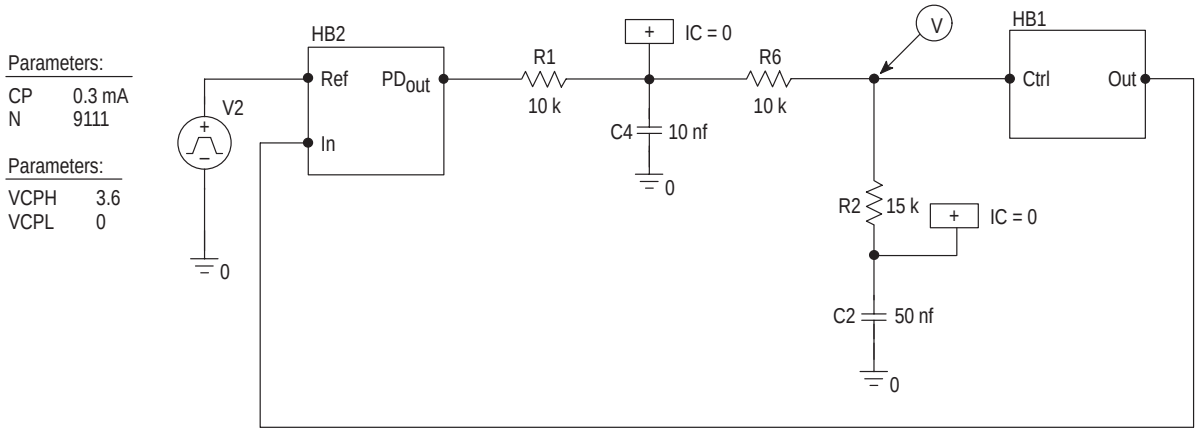
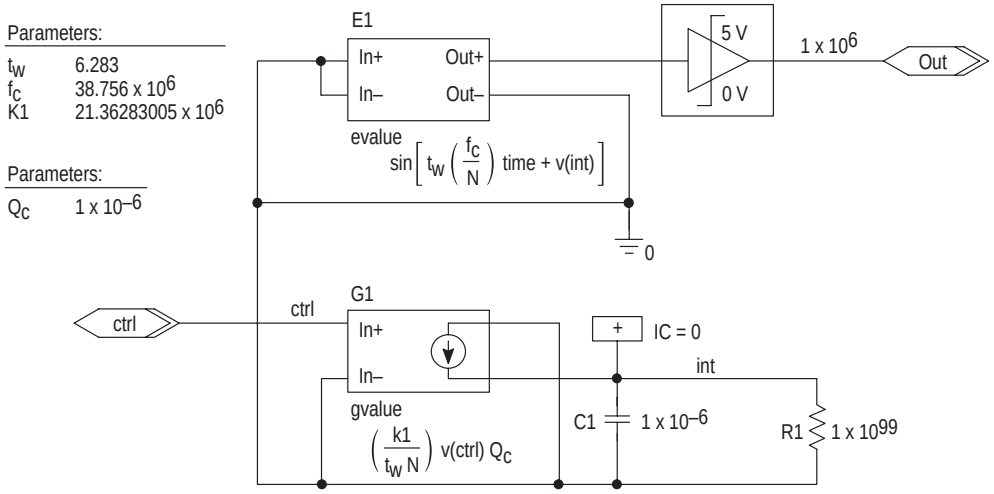


Figure 57. VCO Behavioral Model



G1 performs the operation [k1/(t_W N)] v(ctrl) Q_C. This integrates the input ctrl to produce a voltage ramp used by E1 to produce the desired output. This input is integrated by C1 whose value should equal Q_C for most applications. R1 is required by SPICE to prevent a floating node error.

E1 performs the calculations necessary to generate a sine wave of the desired frequency based on the values listed in the parameter tables and the value of ctrl. The output of E1 is multiplied by 1 x 10^6 and limited to 0 and 5 to obtain a square wave with a fast rise/fall time. Since I/O_STM is a standard model whose values are 0 and 5, these are used here and in the phase detector rather than modifying the component libraries.

The parameter tables provide a convenient method for setting VCO parameters. t_W is 2π, f_C is the zero control voltage VCO frequency, and K1 is the VCO gain in rad/s/V.

The sub–schematic for the phase/frequency detector section of the drawing is shown in Figure 58. This is composed of two blocks, HB3 and HB4. HB3 performs the PD_{out}' function with HB4 performing the actual phase detector operation.

The circuit for the phase/frequency detector is shown in Figure 59. The model is made up of two pulse generators, two RS flip–flops, and appropriate behavioral gates.

HB1 and HB2 are RS flip–flops. These are constructed from behavioral blocks as shown in Figure 60. A behavioral AND gate with a 5 ns delay completes the three state (±2π) phase/frequency detector. The STP function ensures the RS flip–flops are reset at initiation.

To perform the phase detector function, the Ref and f_{in} inputs of the behavioral RS flip–flops are configured to simulate edge triggered operation. This is achieved by placing a 1 ns delay in the Ref and f_{in} signal paths. The input and output of the delay are compared by the input behavioral block and interpreted as a 1 ns pulse. These pulses are used to set HB1 and HB2. If f_{in} leads Ref, the In flip–flop, HB2, will be set first. When Ref leads f_{in}, the Ref flip–flop, HB1, will be set first. The lagging edge drives the second flip–flop output high and the behavioral AND gate then resets both flip–flops. The delay line at the output of the behavioral AND gate prevents PSpice from being confused and also completes the simulation of the phase detector. The outputs of the two RS flip=flops are labeled R_ϕ and V_ϕ. The time between the leading and lagging edges is reflected in the pulse width of the leading edge flip–flop. The lagging edge flip–flop will display a narrow pulse equal in width to the value chosen for the delay at the output of the behavioral AND gate. This should be programmed to the minimum value as specified by the data sheet and is usually 5 ns or less.

Since the outputs R_ϕ and V_ϕ are pure logic signals, additional circuitry is necessary to produce the output PD_{out}'. This output should be high impedance when not driving, and pull either high or low depending on which function (R_ϕ or V_ϕ) is active. The circuitry shown in Figure 61 performs this function.

To eliminate the need for discrete modeling of PD_{out}', analog behavioral modeling is used. Analog behavioral blocks ABMI/2, generate a current source/sink output whenever the appropriate input is high.

A second set of behavioral blocks monitor the output idrive, and switch on the appropriate voltage controlled switch whenever the output rises to the value of V_{DD} (phase detector supply voltage) or drops to 0.

To model PD_{out}', either a model of the transistors used for PD_{out}' must be used or this behavioral arrangement can be used. Since the output is specified by a specific output level and current capability, this arrangement suffices. The output swing becomes VCPH in the schematic and the current capability is CP. If a non–zero value is desired for V_{lo}, the value VCPL is adjusted from the parameter table on the top level schematic.

This arrangement allows setting the output voltage swing of PD_{out}' by specifying VCPH, the current drive of PD_{out}' by specifying the desired value for CP, and leakage values can be simulated by setting the appropriate attributes for S1 and S4 or by adding additional resistance.

Simulation

Figures 62 and 63 are the simulation results of running a transient analysis on the example shown above. The time to lock from power on is simulated by setting the initial condition (IC1) to 0 and running the simulation. Figure 62 is the time versus value of the VCO control voltage. Figure 63 shows the output at the input of the loop filter and can be used to determine lock time.

Figure 58. Phase/Frequency Detector

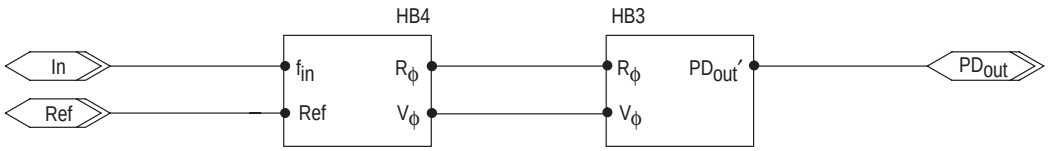


Figure 59. Phase Detector Logic

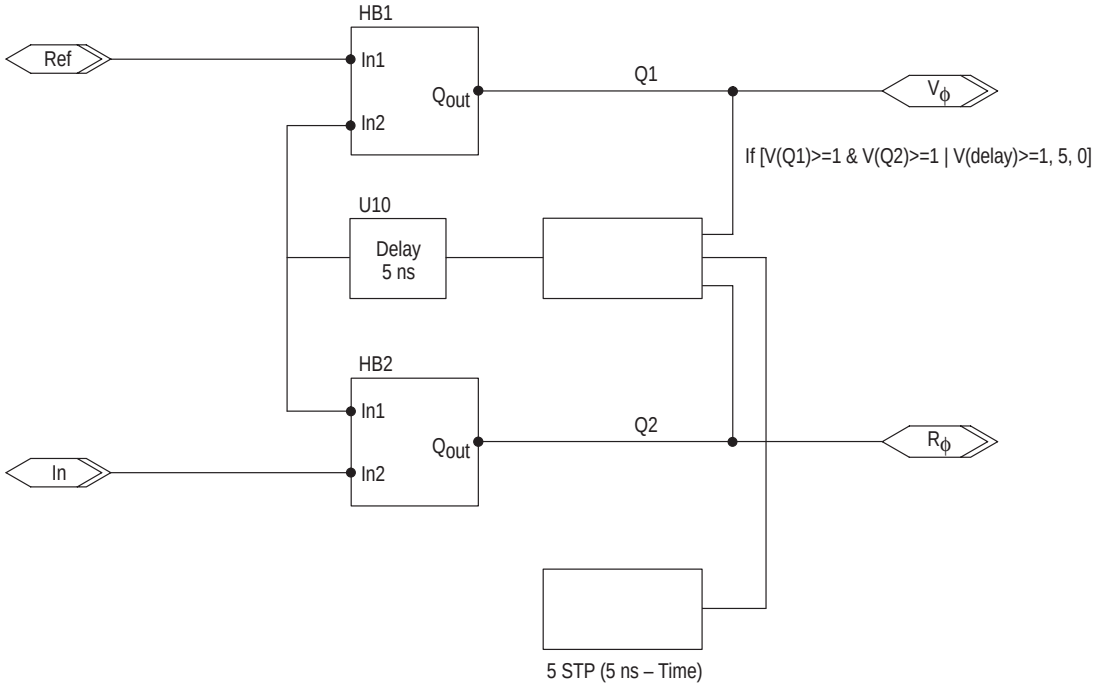


Figure 60. Behavioral RS Flip–flop

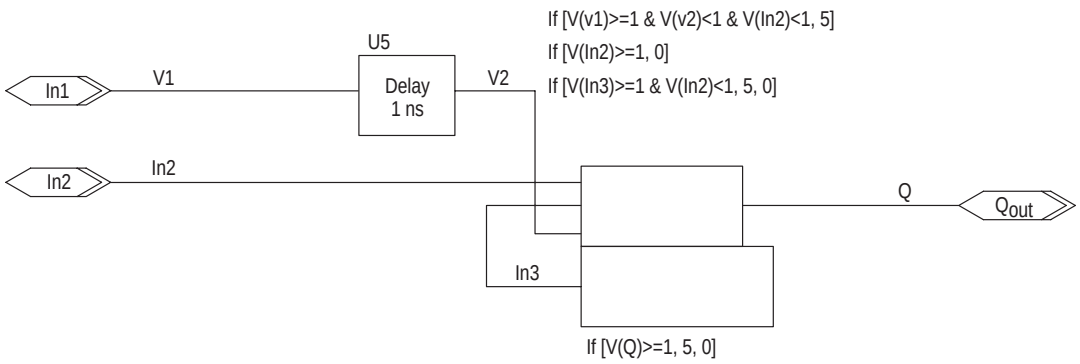


Figure 61. R_ϕ / V_ϕ to PD_{out}' Conversion

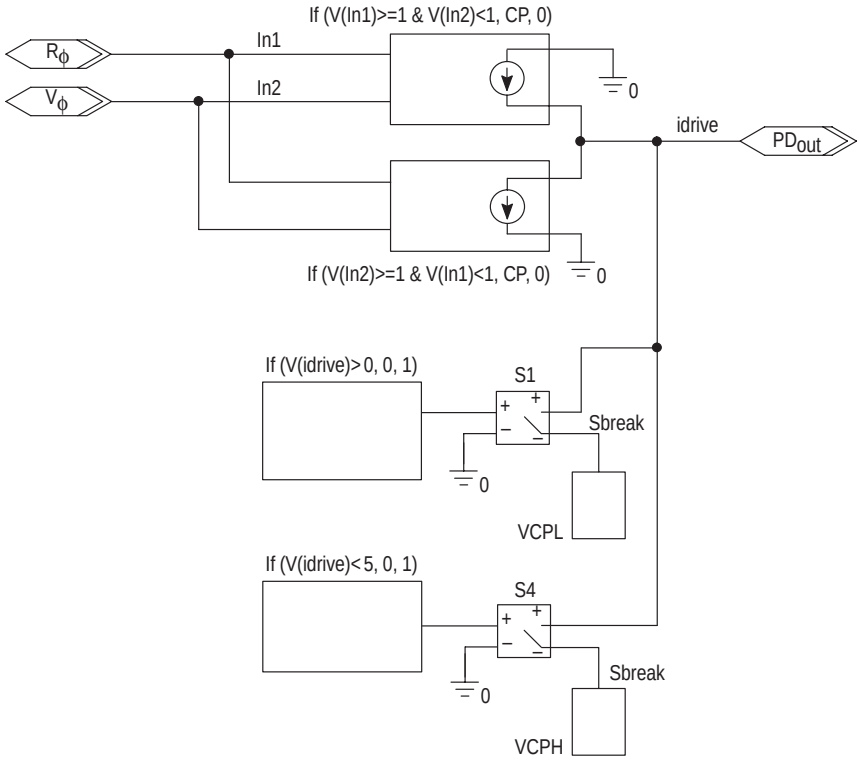


Figure 62. VCO Control Voltage versus Time

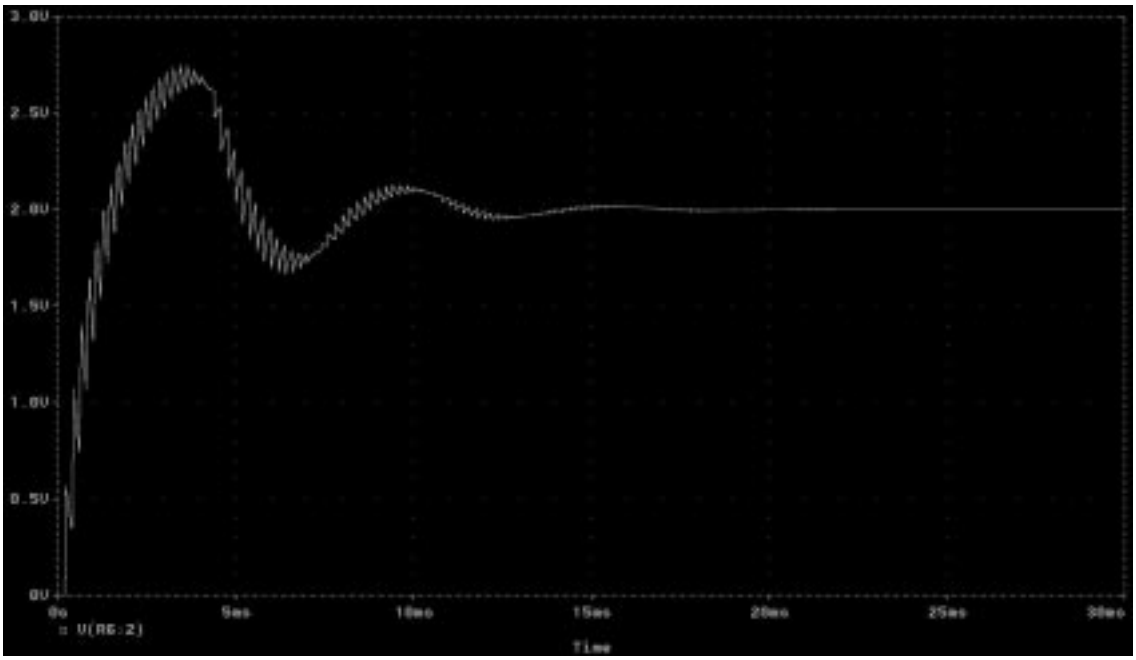
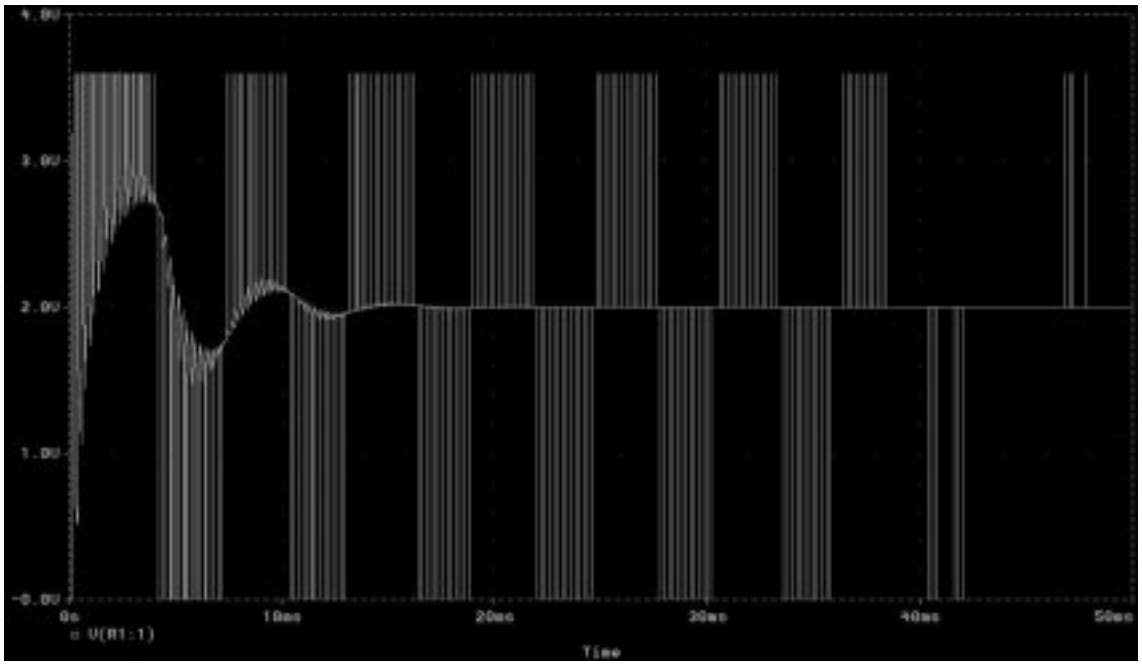


Figure 63. PD_{out}' at Input to Loop Filter



Summary

PSpice provides a method by which the performance of PLL circuitry can be simulated prior to, or in addition to, laboratory testing. The use of behavioral modeling allows the creation of simulation circuits that can provide valuable information for loop filter design and adjustment. By judicious attention to VCO modeling, expected output characteristics can be verified prior to laboratory testing. While simulation does not replace laboratory testing, it can be used to find solutions to “what if” questions without the need for extensive empirical data gathering.

7E. VOLTAGE MULTIPLIER STALL AVOIDANCE

There are three important criteria to note, highlighted in the following sections: **Allowing for Voltage Build, Ensuring Valid Counter Programming,** and **Allowing for Overshoot.** Violation of any of these may cause the voltage multiplier to collapse. Once the voltage collapses, the loop goes out of lock and can not recover until the voltage is allowed to build up again. For an active loop, the voltage multiplier is designed to *maintain* the multiplied voltage on the phase/frequency detector supply pin (C_{mult}). If the main loop is active, the multiplier cannot build the voltage.

Allowing for Voltage Build

After power up, a sufficient time interval must be provided for the on–chip voltage multiplier to build up the voltage on the C_{mult} pin. During this interval, the phase/frequency detector outputs for the main loop (PD_{out}–Hi and PD_{out}–Lo) must be inactive (floating outputs). The POR (power–on reset) circuit forces this "float" condition, thus allowing the voltage to build on the C_{mult} pin.

The duration of the interval to build the voltage is determined by the external capacitor size tied to the C_{mult} pin and the charging current which is 100 μA minimum. The following formula may be used:

$$T = CV/I$$

where

T is the interval in seconds,

C is the C_{mult} capacitor size in farads,

V is the desired voltage on C_{mult} in volts, and

I is the charging current, 1×10^{-4} amps.

The desired voltage on C_{mult} is 4 V for a nominal 2 V supply and 5 V for any supply above 2.6 V.

After this interval, the chip can maintain the voltage on the C_{mult} pin and the phase detectors may be safely placed in the active state.

The interval above also applies when the voltage multiplier is turned off (with power applied) via bits R′19 R′18 R′17 being 000. After the multiplier is turned back on, sufficient time must be allowed for the voltage to build on C_{mult}. In this case, typically an external resistor does not allow the C_{mult} voltage to discharge below approximately V_{pos} (see Section 5E, under **C_{mult}**). Note that if the voltage multiplier is NOT turned off (that is, the above bits are unequal to 000), the keep–alive circuit maintains the multiplied voltage on C_{mult}.

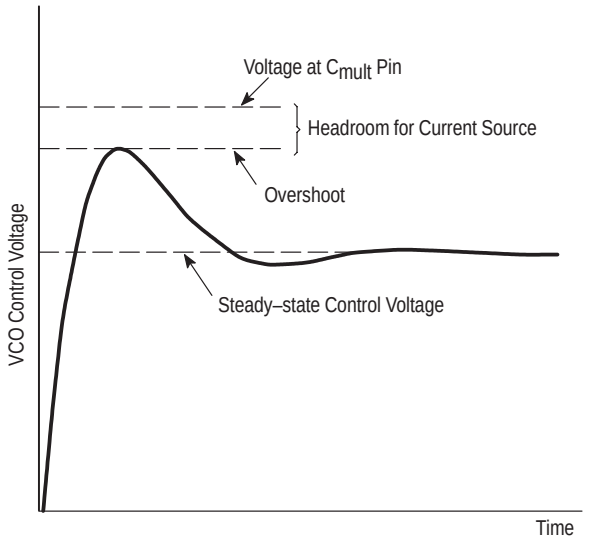
Ensuring Valid Counter Programming

Before the PLLs and/or phase detectors are taken out of standby, legitimate divide ratios (pertinent to the application) must be loaded in the registers. For example, proper divide ratios must be loaded for the R, N, R′, and N′ counters. Also, proper values for all other bits must be loaded. For example: selection of crystal or external reference mode must be made prior to activation of the loops.

After the IC is initialized with the proper bits loaded, the main loop may then be safely activated via the phase detector float bit and/or the PLL standby bit being programmed to 0.

Allowing for Overshoot

The VCO control voltage overshoot for the main loop must not be allowed to exceed the capability of the phase/frequency detectors' maximum output voltage. The detectors' maximum output voltage is determined by the minimum voltage at C_{mult} and the headroom required for the current source. See the following figure.



For example, if the main supply voltage (V_{pos}) is 3 V and the voltage multiplier is utilized, the minimum voltage at C_{mult} is 4.75 V. Then, to allow for current source headroom, the maximum output voltage from the parameter table in Section 3C is approximately C_{mult} – 0.6 V or 4.2 V approximately. Thus, the maximum output overshoot voltage at the phase/frequency detector outputs should be no more than 4.2 V.

Continuing the above example, if the loop is designed with 20% overshoot in the VCO control voltage, then the overshoot must be subtracted off of the 4.2 V shown above. Therefore, the upper end of the control voltage to the VCO must be no more than approximately 3.64 V.

The equations below can be used to determine constraints:

$$\Delta V \leq \frac{V_\phi - 1.2}{2\alpha + 1}$$

$$SSV_{max} = V_\phi - \alpha\,(\Delta V) - 0.6$$

where

ΔV is the VCO control voltage range, the maximum minus the minimum voltage,

V_ϕ is the minimum phase detector supply voltage (at the C_{mult} pin) per the following table,

α is the control voltage overshoot in decimal; for example, 20% overshoot is 0.2, and

SSV_{max} is the maximum allowed steady–state VCO control voltage.

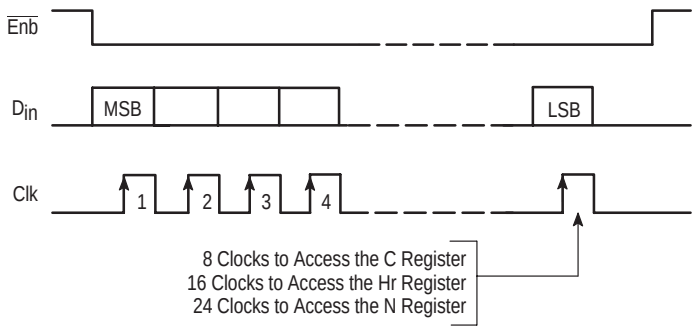
MINIMUM PHASE DETECTOR VOLTAGE FROM VOLTAGE MULTIPLIER

Supply Voltage, V_{pos}	Minimum Phase Detector Voltage, V_ϕ
1.8 V	3.32 V
2.0 V	3.72 V
2.5 V	4.75 V
3.6 V	4.75 V

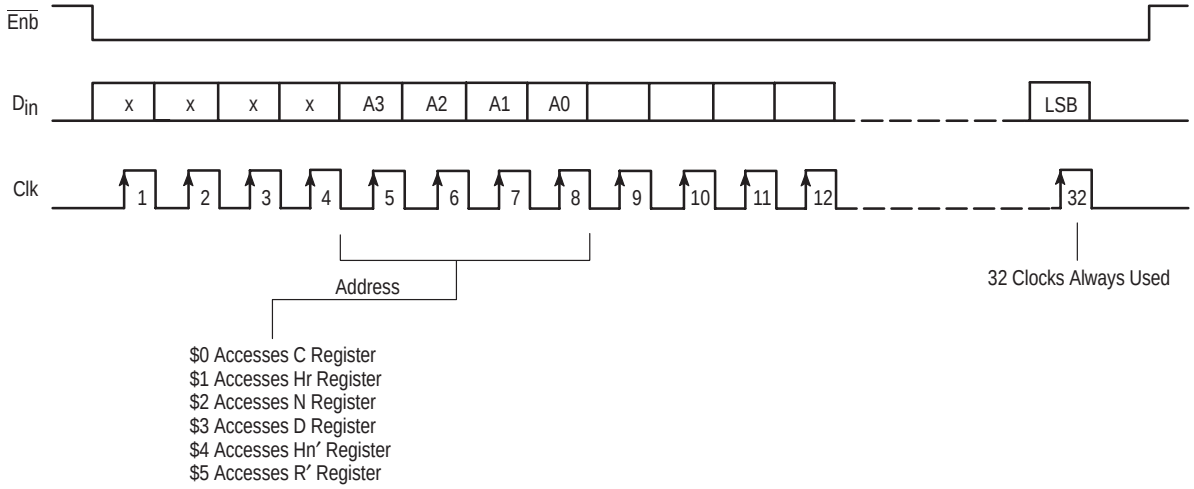
8. PROGRAMMER'S GUIDE

8A. QUICK REFERENCE

BitGrabber ACCESS OF THE REGISTERS



CONVENTIONAL ACCESS OF THE REGISTERS

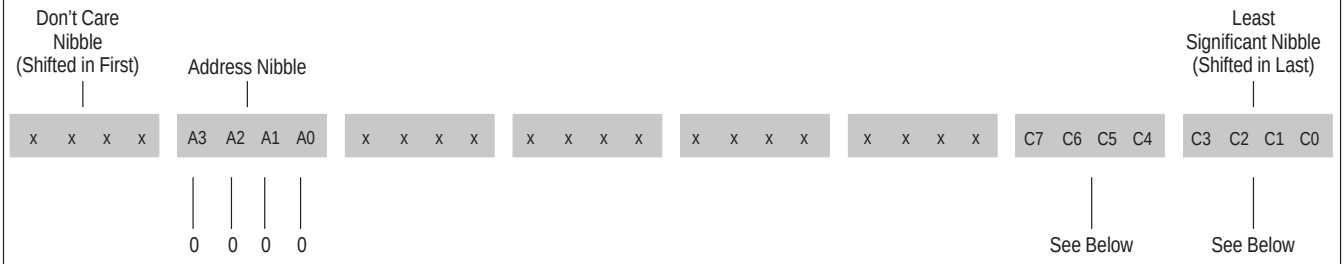


↑ = when the PLL device loads the data bit.

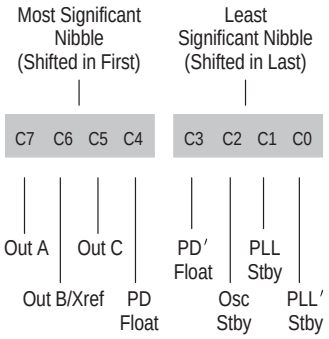
8A. QUICK REFERENCE (continued)

C REGISTER

Conventional Access



BitGrabber Access



Out A = Output A Pin Logic State
0 = Pin is forced to 0 (power up default)
1 = Pin is forced to 1
See Note 1

Out B/XRef = Output B Pin Logic State/ External Reference Selection
See table below

Out C = Output C Pin Logic State
0 = Pin is forced to 0 (power up default)
1 = Pin is forced to high impedance

PD Float = Phase Detector Float
0 = Active, normal operation (power up default)
1 = PD_{out}–Hi/PD_{out}–Lo are forced to high impedance

PD′ Float = Phase Detector′ Float
0 = Active, normal operation (power up default)
1 = PD_{out}′ is forced to high impedance

Osc Stby = Oscillator Standby
0 = Active, normal operation (power up default)
1 = Oscillator/reference circuit in standby
See Note 2

PLL Stby = PLL Standby
0 = Active, normal operation
1 = Main PLL in standby (power up default)
See table below

PLL′ Stby = PLL′ Standby
0 = Active, normal operation
1 = Secondary PLL in standby (power up default)

NOTES: 1. For the Out A bit to control the Output A pin as a port expander, bits R′21 R′20 must be 0 0, which selects Output A as a general–purpose output. If R′21 R′20 are not equal to 0 0, then the Out A bit is a don't care.
2. Whenever Osc Stby = 1, both PLL Stby and PLL′ Stby must be 1, also.

Mode Pin and Bit Summary

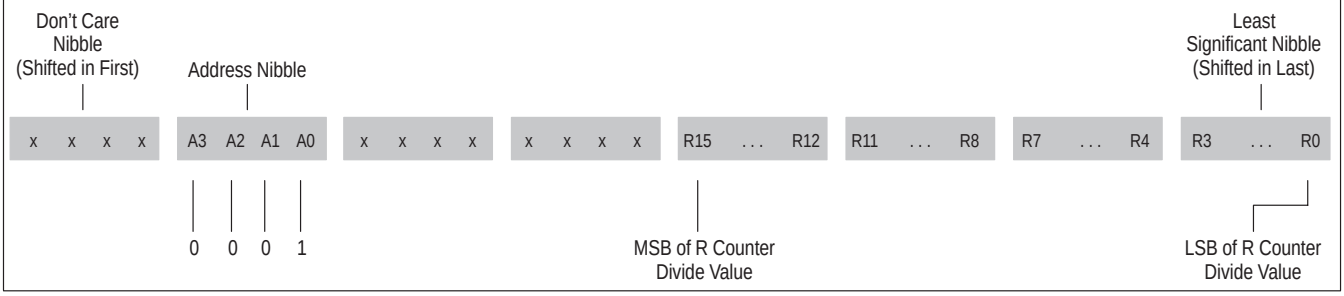
Mode Pin	Out B/XRef Bit	PLL Stby Bit	Reference Circuit	Output B Pin	Main PLL
0	0	0	Xtal Osc mode	0	Active
0	0	1	Xtal Osc mode	Z	Standby
0	1	0	Xtal Osc mode	1	Active
0	1	1	Xtal Osc mode	Z	Standby
1	0	0	Xtal Osc mode	0	Active
1	0	1	Xtal Osc mode	Z	Standby
1	1	0	External Reference mode	1	Active
1	1	1	External Reference mode	Z	Standby

NOTES: Xtal osc = crystal oscillator. Z = high impedance.

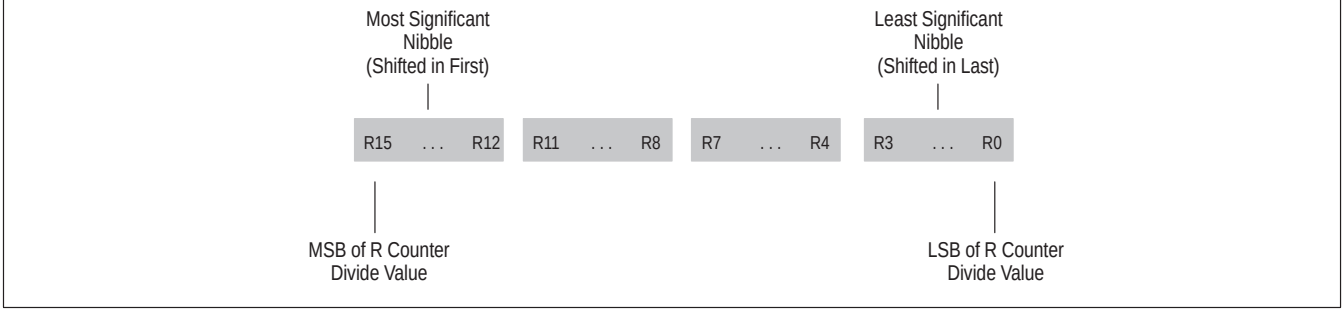
8A. QUICK REFERENCE (continued)

Hr REGISTER

Conventional Access



BitGrabber Access



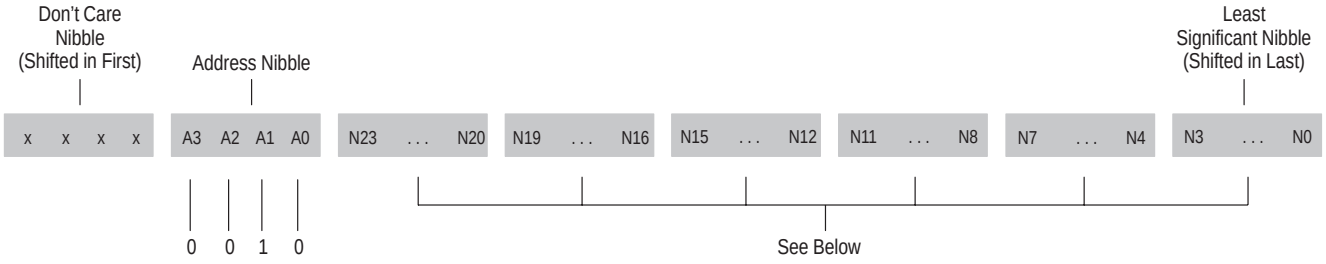
EXAMPLE: To program the R counter to divide by 1000 in decimal, first multiply 1000 by 2 which is 2000. Convert 2000 to hexadecimal: $7D0. Then, add leading 0s to form 2 bytes (4 nibbles): $07D0. Finally, load the Hr register bits R15 to R0 with $07D0. When the N register is subsequently loaded, data passes from the first Hr register (buffer) to the second R register (buffer). (Data is still retained in the Hr register.)
With BitGrabber, no address bits are needed. With a conventional load, address bits A3 to A0 must be included.

NOTE: Hexadecimal numbers are preceded with a dollar sign. For example: hexadecimal 1234 is shown as $1234.

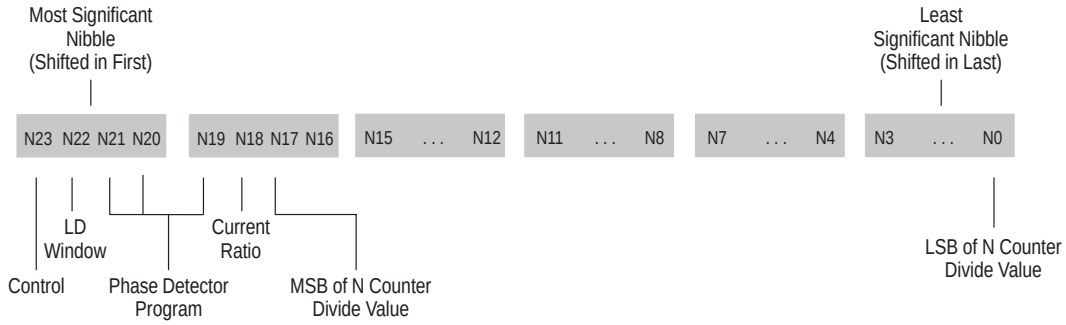
8A. QUICK REFERENCE (continued)

N REGISTER

Conventional Access



BitGrabber Access



Control = Control for Auxiliary Divider
See Table A

LD Window = Lock Detector Window for Main Loop
0 = 32 Osc_e periods
1 = 128 Osc_e periods

Phase Detector Program = Detector Program for Main Loop
See Table B

Current Ratio = PD_{out}–Hi to PD_{out}–Lo Current Ratio
0 = 4:1
1 = 8:1

EXAMPLE: To program the N counter to divide by 1000 in decimal, first convert to hexadecimal: $3E8. Then, add leading 0s to form 2 leading bits plus 2 bytes (2 bits plus 4 nibbles); this is N17 to N0. Bits N23 to N18 should be appropriate to control the above functions. Finally, load the N register. Loading the N register also causes data to pass from the Hr register to the R register and data from the Hn′ register to pass to the N′ register.
With BitGrabber, no address bits are needed. With a conventional load, address bits A3 to A0 must be included.

Table A. Osc_e to f_{out} Frequency Ratio, Mode = Low

N23	R′1	R′0	Osc_e to f_{out} Frequency Ratio
0	0	0	10:1
0	0	1	12.5:1
0	1	0	12.5:1
0	1	1	12.5:1
1	0	0	8:1
1	0	1	10:1
1	1	0	10:1
1	1	1	10:1

NOTE: When the Mode pin is high, the f_{out} pins are configured as polarity inputs and N23 must be programmed to 1.

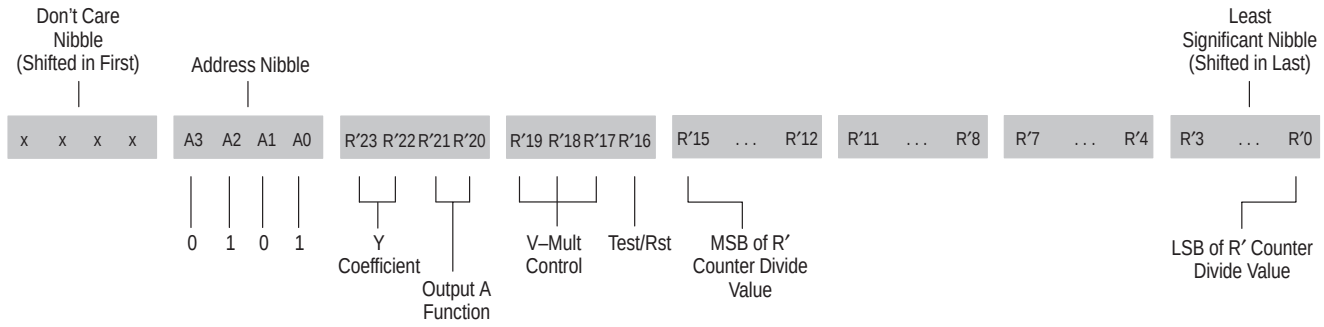
Table B. Main Phase Detector Control

N21	N20	N19	Result
0	0	0	Both PD_{out}–Hi and PD_{out}–Lo floating
0	0	1	PD_{out}–Hi floating, PD_{out}–Lo enabled
0	1	0	PD_{out}–Hi enabled, PD_{out}–Lo floating
0	1	1	Both PD_{out}–Hi and PD_{out}–Lo enabled
1	0	0	PD_{out}–Hi enabled and PD_{out}–Lo floating for 16 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled
1	0	1	PD_{out}–Hi enabled and PD_{out}–Lo floating for 32 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled
1	1	0	PD_{out}–Hi enabled and PD_{out}–Lo floating for 64 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled
1	1	1	PD_{out}–Hi enabled and PD_{out}–Lo floating for 128 f_R cycles, then PD_{out}–Hi floating and PD_{out}–Lo enabled

8A. QUICK REFERENCE (continued)

R′ REGISTER

Conventional Access only



Y Coefficient
- 0 0 = Maximum frequency on $f_{in} \leq 550$ MHz
- 0 1 = Maximum frequency on $f_{in} \leq 1.2$ GHz
- 1 0 = Maximum frequency on $f_{in} \leq 2.2$ GHz
- 1 1 = Not used

Output A Function = Controls Output A Mux
- 0 0 = General–Purpose Output
- 0 1 = f_R
- 1 0 = $f_{R'}$
- 1 1 = Phase Detector pulse

V–Mult Control = Voltage Multiplier Control
- 0 0 0 = Multiplier OFF, 9 MHz ≤ $Osc_e \leq 80$ MHz
- 0 0 1 = Multiplier ON, 9 MHz ≤ $Osc_e \leq 20$ MHz
- 0 1 0 = Multiplier ON, 20 MHz < $Osc_e \leq 40$ MHz
- 0 1 1 = Multiplier ON, 40 MHz < $Osc_e \leq 80$ MHz

Test/Rst = Test/Reset
- 0 = only programming value allowed

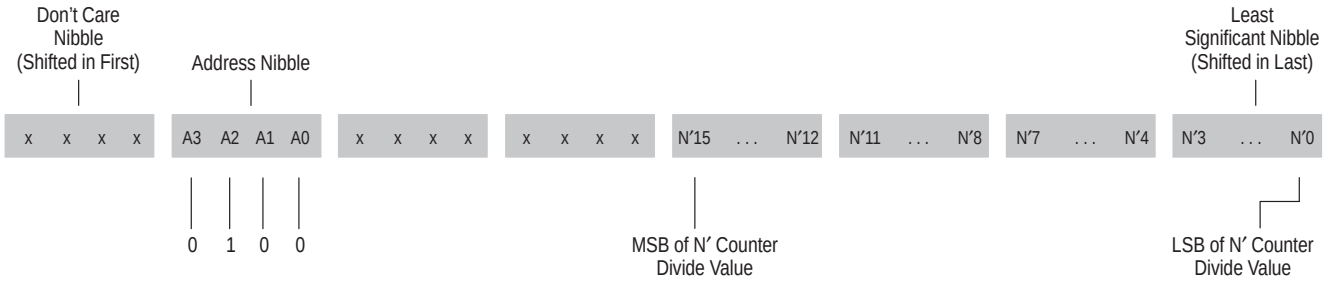
EXAMPLE: When the Mode pin is tied low, see Table 21 for R′ counter programming. When the Mode pin is tied high, to program the R′ counter to divide by 1000 in decimal, first multiply 1000 by 2, which is 2000. Convert 2000 to hexadecimal: $7D0. Then, add leading 0s to form 2 bytes (4 nibbles); this becomes bits R′15 to R′0. Bits R′23 to R′16 should be appropriate to control the above functions. Finally, load the R′ register.
With a conventional load, address bits A3 to A0 must be included.

NOTE: Hexadecimal numbers are preceded with a dollar sign. For example: hexadecimal 1234 is shown as $1234.

8A. QUICK REFERENCE (continued)

Hn′ REGISTER

Conventional Access only

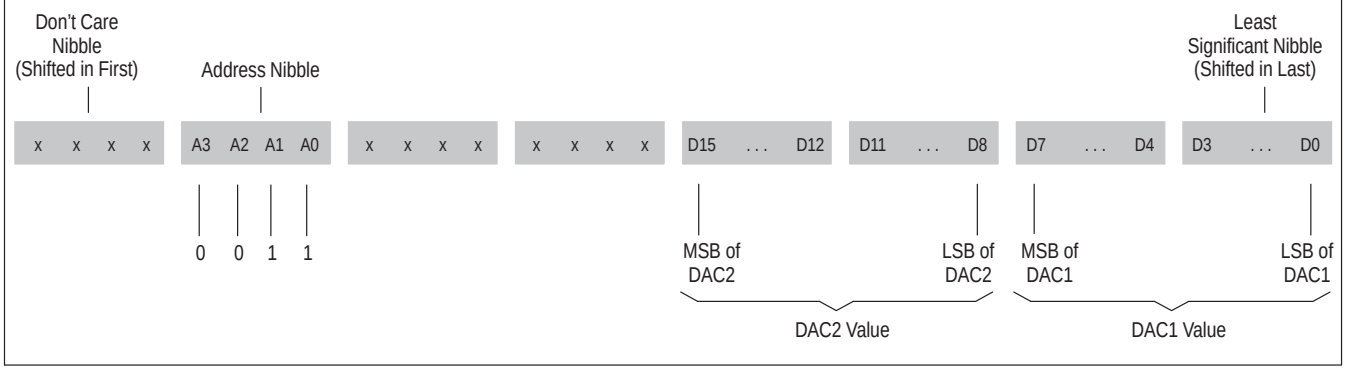


EXAMPLE: To program the N′ counter to divide by 1000 in decimal, first convert 1000 to hexadecimal: $3E8. Then, add leading 0s (if necessary) to form 2 bytes (4 nibbles): $03E8. Finally, configure address bits A3 to A0 and load the Hn′ register. When the N register is subsequently loaded, data passes from the first Hn′ register (buffer) to the second N′ register (buffer). (Data is still retained in the Hn′ register.)

8A. QUICK REFERENCE (continued)

D REGISTER

Conventional Access only



DAC2 Value = Analog Output Level of DAC2
- $00 = zero output
- $01 = zero + 1 LSB output
- $02 = zero + 2 LSBs output
- $03 = zero + 3 LSBs output
- •
- •
- •
- $FD = full scale – 2 LSBs output
- $FE = full scale – 1 LSB output
- $FF = full scale output

DAC1 Value = Analog Output Level of DAC1
- $00 = zero output
- $01 = zero + 1 LSB output
- $02 = zero + 2 LSBs output
- $03 = zero + 3 LSBs output
- •
- •
- •
- $FD = full scale – 2 LSBs output
- $FE = full scale – 1 LSB output
- $FF = full scale output

8B. INITIALIZING THE DEVICE

Introduction

The registers retain data as long as power is applied to the device. The R and N registers contain counter divide ratios for the main loop, PLL. The R′ and N′ registers contain counter divide ratios for the secondary loop, PLL′. Additional control bits are located in the R′, N, and C registers. The D register controls the DACs. Section 8A is a handy reference for register access and bit definitions.

The C, D, R′, and N registers can be directly written, and have an immediate impact on chip operation. The Hr and Hn′ registers can be directly written, but have no immediate impact on chip operation. This is because the Hr and Hn′ registers are the front–ends of double buffers. The Hr register feeds the R register. The Hn′ register feeds the N′ register. Changing data in the R and/or N′ registers is done with a write to the Hr and/or Hn′ register, respectively, followed by a write to the N register. The transfer of data from the Hr to R and Hn′ to N′ registers is triggered with a write to the N register.

Typically, the Hr and Hn′ registers are written once, during initialization after power up. The Hr and Hn′ registers only need to be accessed if their data is changing.

An Example

Following is an initialization example for a system with a main loop that covers 1.8 to 2.1 GHz in 30 kHz steps. An external reference of 19.44 MHz is utilized. The secondary loop is selected to run at 200 MHz. Both VCOs are positive polarity meaning that when the input control voltage increases, the output frequency increases. A divided–down reference is not needed (f_{out} and $\overline{f_{out}}$). Therefore, the Mode pin is tied to V_{pos} and the Pol and Pol′ pins are tied to ground.

The following initialization gives serial data examples for BitGrabber access of the C, Hr, and N registers.

Initialization

Below is the six–step initialization sequence used after power up for the example given above.

Programming the C register first is recommended if the voltage multiplier is utilized. There are three important criteria to note. Violation of any criterion may cause the voltage multiplier to collapse. The first criterion is that after power up, a sufficient time interval must be provided (after the C and R′ registers are initialized) for the on–chip voltage multiplier to build up the voltage on the C_{mult} pin. This interval is determined by the external capacitor size tied to the C_{mult} pin and the charging current which is about 100 μA. After this interval, the chip can maintain the voltage on the C_{mult} pin and the phase/frequency detectors for the main loop may be safely activated. The second criterion is that before the phase/frequency detectors are activated, legitimate divide ratios (pertinent to the application) must be loaded in the registers. The third criterion is a hardware issue. The three criteria are discussed with more detail in Section 7E.

If the voltage multiplier is not used, Step 1 is eliminated and the initialization sequence starts with Step 2.

Step 1: Load the C Register

The C register is programmed such that the main loop's phase/frequency detector outputs are floating (PD Float bit C4 = 1), the reference circuit is active (Osc Stby bit C2 = 0), and an external reference is accommodated (Out B/Xref bit C6 = 1, with the Mode pin high). When the voltage multiplier is enabled by programming the R′ register, the voltage is allowed to build on the C_{mult} pin such that a voltage higher than the main supply voltage is providing power to the phase/frequency detectors. Both loops are active (PLL Stby bits C1 = C0 = 0). Also, for this example, Output A and Output C are programmed low (Out bits C7 = C5 = 0).

In summary, hexadecimal 58 or $58 is serially transferred (BitGrabber access with no address bits).

Step 2: Load the R′ Register

For the secondary loop, the 19.44 MHz reference is divided down to 80 kHz by the R′ counter; the divide ratio is 243. Per Section 8A, the value is doubled to 486. The 16 LSBs of the R′ register determine the R′ counter divide ratio. Therefore, 486 is converted to $01E6 and becomes the 16 LSBs (R′15 to R′0) in the R′ register. Test/Rst bit R′16 must be a 0. Bits R′19 to R′17 determine the refresh rate of the voltage multiplier. The frequency at Osc_e is <20 MHz. Therefore, per Section 8A, bits R′19 to R′17 must be 001. If Output A is needed as a MCU port expander, bits R′21 = R′20 = 0. Per Section 8A, Y Coefficient bits R′23 R′22 = 10.

In summary, $058201E6 is serially transferred (conventional access with an address of 0101).

Step 3: Load the Hr Register

For the main loop, the 19.44 MHz reference must be divided down to 30 kHz by the R counter; the divide ratio is 648. Per Section 8A, the ratio 648 is doubled to 1296 and then converted to $510. The Hr register value is programmed as $0510. When the Hr register contents are transferred to the R register, the R counter divide ratio is determined.

In summary, $0510 is serially transferred (BitGrabber access). This value is transferred from the Hr to the R register when the N register is accessed in Step 5.

Step 4: Load the Hn′ Register

For the secondary loop, the phase detector is chosen to run at 80 kHz. Therefore, 80 kHz must be multiplied up to 200 MHz which is a factor of 2500. The factor is converted to $9C4. The Hn′ register is programmed as $09C4. When the Hn′ register contents are transferred to the N′ register, the N′ counter divide ratio is determined.

In summary, $040009C4 is serially transferred (conventional access with an address of 0100). The value $09C4 is transferred to the N′ register when the N register is accessed in Step 5.

Step 5: Load the N Register

For this example, the IC is initialized to tune the lowest end of the main loop. The lowest end of the main loop's frequency range is 1.8 GHz. Therefore, the 30 kHz must be multiplied up to 1.8 GHz which is a factor of 60,000 or $EA60 to be loaded into bits N17 to N0 of the N register. Bit N18 is programmed to 0 for a PD_{out}–Hi to PD_{out}–Lo current ratio of 4:1. If PD_{out}–Lo is used for the main loop, bits N21 to N19 must be 001. (PD_{out}–Lo must be used to initialize the device when *adapt* is used, see Section 8D.) Bit N22 = 0 to select a lock detect window of approximately $32 / Osc_e$ = 32/19.44 MHz or 1.6 μs. Bit N23 must be programmed to 1 by the user. (When the Mode pin is high, programming N23 to a 0 is for Motorola use only.)

In summary, $88EA60 is serially transferred (BitGrabber access). The N register access also causes double–buffer transfers of Hr to R and Hn′ to N′.

Step 6: Load the C Register

Now that legitimate divide ratios are programmed for the counters, the main loop may be activated. Thus, the PD float bit C4 is now programmed to 0. The standby bits are unchanged: C2 = C1 = C0 = 0. Bit C5 could be used to control Output C to either a low level or high impedance; for a low level, C5 = 0. Whenever an external reference is utilized, bit C6 must be 1. Bit C7 may be used to control Output A to a low or high level because it is selected as “port expander” by bit R′21 and R′20; for a low level, C7 = 0.

In summary, $40 is serially transferred (BitGrabber access). This causes the main loop to tune to 1.8 GHz, the secondary loop to tune to 200 MHz, and both the Output A and Output C pins to be forced low.

The device is now initialized.

8C. PROGRAMMING WITHOUT ADAPT

Tuning the Top of the Band

After initializing the device via steps 1 through 6 in Section 8B, the only register that needs to be loaded to tune the main loop is the N register.

For this example, tuning the upper end of the band (2.1 GHz) requires that the 30 kHz at the phase/frequency detector be multiplied up to 2.1 GHz. This is a loop multiplying factor of 70,000. This value is converted to $11170 and is loaded for bits N17 to N0. Bits N23 to N18 are not changed and are programmed as indicated in Section 8B, step 5.

In summary, $891170 is transferred to tune the main loop. No other registers are loaded.

Tuning Other Channels

Tuning other channels for the main loop, while keeping the secondary loop at a constant frequency, only requires programming the N register. See Table 22 for example frequencies.

Table 22. Main Loop Tuning Examples

Frequency Desired (MHz)	Multiplying Factor (Decimal)	Multiplying Factor (Hexadecimal)	N Register Data (Hexadecimal)
1800.000	60,000	$EA60	$88EA60
1800.030	60,001	$EA61	$88EA61
1800.060	60,002	$EA62	$88EA62
1800.090	60,003	$EA63	$88EA63
1950.000	65,000	$FDE8	$88FDE8
1966.080	65,536	$10000	$890000
2088.960	69,632	$11000	$891000
2100.000	70,000	$11170	$891170

8D. PROGRAMMING UTILIZING HORSESHOE WITH ADAPT

Introduction

A unique adapt feature can be used with the MC145225 or MC145230 when conventional tuning cannot meet the lock–time requirements of a system and the annoying spurs or noise cannot be tolerated from a fractional–N scheme. The adapt feature is available on the main loop only.

For adapt, a timer is engaged which causes an internal data update of the R and N registers to be delayed. The IC supports the *Horseshoe* scheme for adapt by allowing a fairly–close quickly–tuned *approximate* frequency to be tuned, followed by the tuning of the *exact* frequency. Two sets of R and N data are sent to the device. The first set {R1, N1} is for tuning the approximate frequency. The second set {R2, N2} is for tuning the exact frequency. Use of the timer delays the transfer of {R2, N2} until a programmed interval has elapsed. In addition, after the interval has elapsed, the main loop control switches from PD_{out}–Hi to PD_{out}–Lo.

Tuning Near the Top of the Band

Continuing the example, after initializing the device via steps 1 through 6 in Section 8B, Horseshoe with adapt can be used to tune the main loop to obtain fast frequency jumps. Use of the BitGrabber access is recommended to minimize the number of serial data clocks required for sending the four “words”.

In this example, the first phase of adapt utilizes approximate tuning with the phase/frequency detector running at 4x the step size. Therefore, the approximate tuning runs the detector at about 120 kHz. The second phase, with exact tuning, runs the detector at 30 kHz. Horseshoe with adapt requires that two data sets be serially sent to the device for every frequency tuned. The first set is for approximate tuning {R1, N1}; the second set is for exact tuning {R2, N2}.

Approximate tuning with Horseshoe is unique. This method involves two key elements: (1) increasing the phase detector frequency and (2) varying *both* the R and N divide values such that the approximate frequency is within a certain predetermined range. The Horseshoe algorithm contained in the development system software also allows placing a constraint on the loop–gain variation that the user can tolerate.

For example, to tune 1800.270 MHz, the first {R1, N1} data set could contain divide ratios for the R and N counters of 138.5 and 12,826, respectively. With this data set, the phase detector is running at about 140 kHz and the approximate frequency is about 325 Hz from the exact frequency. The second data set contains R and N divide ratios of 648 and 60,009, respectively. This achieves the exact (target) frequency of 1800.270 MHz.

The timer must be programmed to determine the interval that the device is in the approximate–tune mode. For this example, assume this is 32 f_R cycles; thus, bits N21 N20 N19 = 1 0 1 in the first data set. Note that this time interval is 32 cycles of f_R, with the phase detector running at about 140 kHz (approximate tune) or about 230 μs plus the MCU

shift time shown in Figure 64. Included in the first data set are N23 = 1 which is required when the Mode pin is high, N22 = 0 for the lock detect window of 1.6 μs, and N18 = 0 for a current ratio of 4:1 (because the phase detector is running at approximately 4x the step size). Note that bits N23, N22, and N18 are unchanged from the initialization values.

For the second data set, bits N23, N22, and N18 are unchanged. Bits N21, N20, and N19 must be programmed as 001. This enables PD_{out}–Lo for the exact tune after time out.

In summary, two data sets need to be sent to the device: {R1, N1} and {R2, N2}. They are sent in succession as R1, N1, R2, N2; where R1 is the R register value for the first data set, N1 is the N register value for the first set, etc. For the example, these values are {R1, N1} = {$0115, $A8321A} and {R2, N2} = {$0510, $88EA69}. See Figure 64.

Tuning Other Channels

Tuning other channels for the main loop, while keeping the secondary loop at a constant frequency, requires sending two data sets to the part {R1, N1} and {R2, N2}. See Table 23.

8E. CONTROLLING THE DACs

Introduction

The two 8–bit DACs are independent circuit blocks on the chip. They have no interaction with other circuits on the chip. A single 16–bit register, called the D register, holds the binary value which controls both DACs.

Programming the DACs

A DAC programmed for 0 scale is in the low–power mode. The 0 scale is programmed as $00 for each 8–bit DAC.

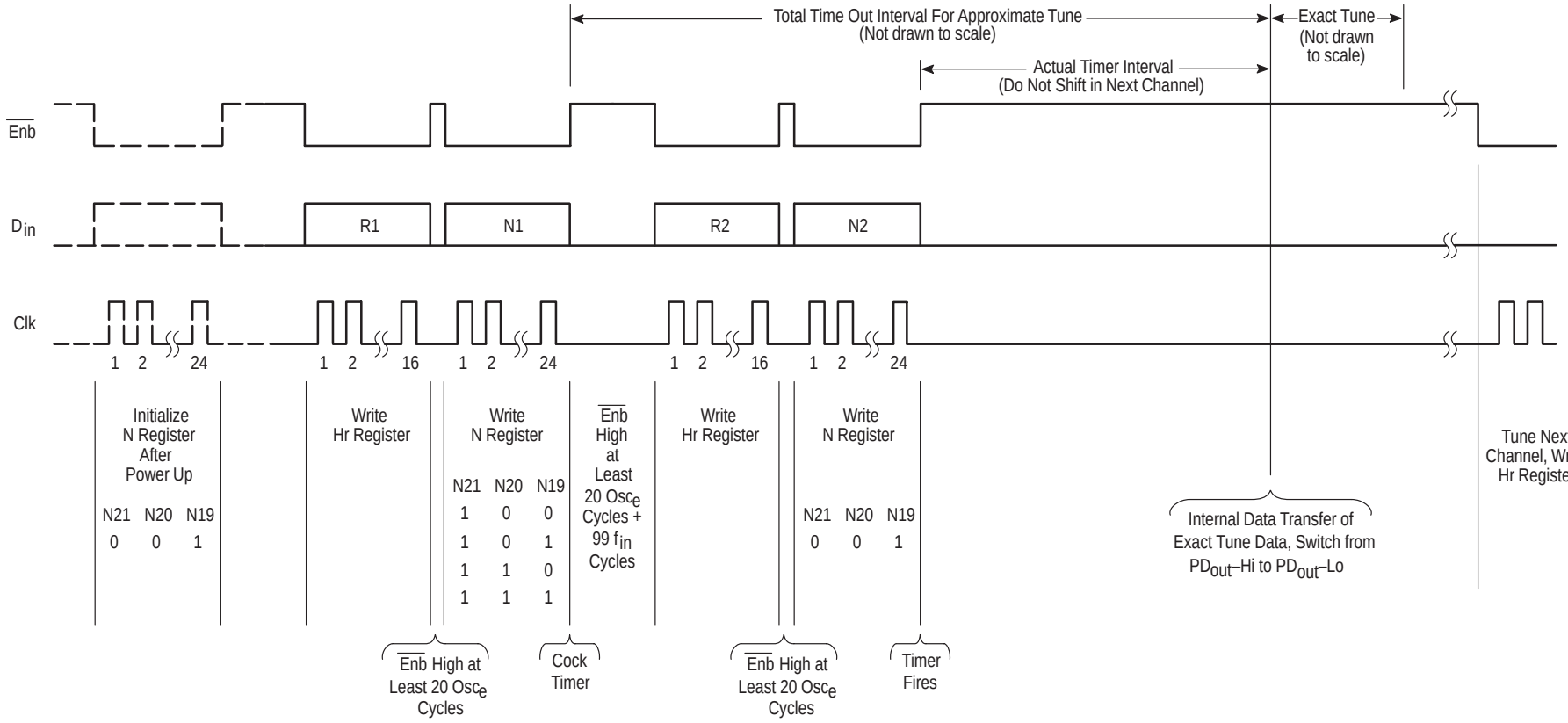
As an example, consider a system that uses just one of the DACs (DAC 1). The other DAC output is unused and is programmed for 0 output. If a condition for a system requires that the DAC have a half–scale output, then DAC 1 is programmed as $80.

In summary, $03000080 is serially transferred (conventional access with an address of 0011).

Table 23. Main Loop Tuning Using Horseshoe With Adapt

Desired Target Frequency (MHz)	Approximate Tuning			Exact Tuning	
	R1	N1	Frequency Error (Hz)	R2	N2
1800.000	$0144	$A83A98	0	$0510	$88EA60
1800.270	$0115	$A8321A	325	$0510	$88EA69
1808.220	$0184	$A8467D	619	$0510	$88EB72
2061.300	$00EC	$A830E0	1017	$0510	$890C66
2063.010	$00F6	$A830E0	732	$0510	$890C9F
2100.000	$0144	$A8445C	0	$0510	$891170

Figure 64. Serial Data Format for Horseshoe with Adapt

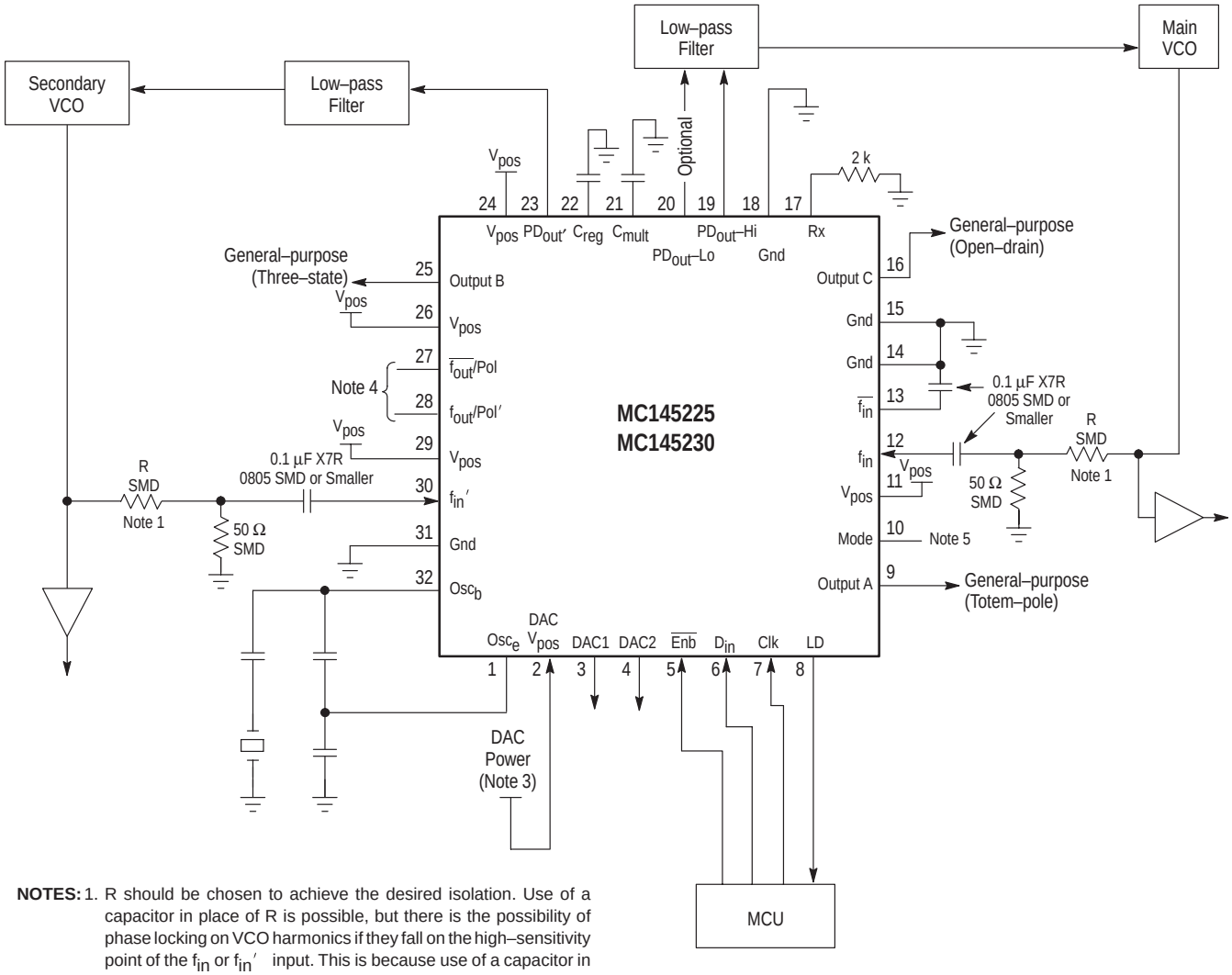


NOTE: The interval for shifting in Exact Tune {R2, N2} data adds to the actual Approximate Tuning time. However, this is usually insignificant. For example, at a data rate of 2 Mbps (2 megabits per second), approximately 20 μs is added to the Approximate Tuning time.

MC145225 MC145230

9. APPLICATION CIRCUIT

Figure 65. Application Circuit



NOTES: 1. R should be chosen to achieve the desired isolation. Use of a capacitor in place of R is possible, but there is the possibility of phase locking on VCO harmonics if they fall on the high–sensitivity point of the f_{in} or f_{in}' input. This is because use of a capacitor in place of R forms a high–pass filter.
2. V_{pos} may range from 1.8 to 3.6 V.
3. DAC power may be any potential between 1.8 V and 3.6 V.
4. Configurable pins. See Pin Descriptions.
5. Tie mode to Gnd or V_{pos}.

MC145220EVK

Technical Summary

MC145220 Evaluation Board

INTRODUCTION

The MC145220EVK makes it easy to exercise features of the MC145220 and build PLLs which meet individual performance requirements. The EVK is controlled through menu driven software operating on an IBM PC or compatible. Other Motorola PLL EVKs (MC145190, MC145191, MC145192, MC145200, MC145201, MC145202) in up to three–board cascades can use the same program. Frequency defaults that apply to each are automatically selected. All board functions are controlled through the printer port of an IBM PC. Up to three different EVKs may be controlled at the same time from one printer port. The functional block diagram is given in Figure 1.

This technical summary contains the hardware description for the evaluation board and a summary of the software section. For complete information, consult the manual that is provided in the evaluation kit.

ORDERING INFORMATION

These kits may be ordered through your local Motorola Semiconductor sales office or authorized distributor. Ask your Motorola representative to order the kits from the finished goods warehouse, not the literature distribution center. Request the part number shown below.

Part Number	Description
MC145220EVK	Kit with the MC145220 installed.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 2
1/99 TN98012100

SECTION 1 – HARDWARE

FEATURES

1. The EVK is a complete working synthesizer, including VCOs.
2. Board is controlled by an IBM PC–compatible computer through the printer port.
3. Up to three boards can be operated independently through one printer port.
4. A prototype area and mounting holes are provided for VCOs, mixers, and amplifiers.
5. External reference input can be used.
6. Five element loop filter is included.
7. Frequency range of operation, step size and reference frequency can be changed in the control program.
8. Lock Detect, Out A, and Out B on any single board are accessible through the printer port.

CONTENTS OF EVALUATION KIT

1. Assembled evaluation board.
2. Nine–foot flat cable with four DB–25 male connectors.
3. MC145220EVK manual.
4. 3.5″ PC–compatible disk containing compiled program.
5. PLL device data sheets.

GETTING STARTED

To perform basic functions, do the following:

1. Plug in 12 volts at J8, observing the polarity marked on the board.
2. Short circuit section 1 of the DIP switch (S1) and open circuit all other sections.
3. Connect the supplied flat cable between the computer printer port and the DB–25 connector on the board (J9).
4. Type PLL at the DOS prompt. Then press enter.
5. Type the number that corresponds with the type of board given in the on–screen menu. The MC145220 may operate in single loop or dual loop mode. Then press Q.

You should now see the main menu displayed. There should be a signal present at J5 if single loop, or J12 if dual loop. The frequency will be the current output frequency given in the main menu. If the signal is not on the correct frequency, check to see if your printer port address is $278 (hexadecimal 278). If not, then select the P menu item and enter the correct address. After returning to the main menu, select the I menu item to send data to the board. You should now be on frequency.

MODIFICATIONS

The user may modify the hardware, such as utilizing a different VCO, by using the prototyping area of the board. After such modifications are made, the default values in the software may need to be changed. This is facilitated from the ‘Select from the available options’ screen.

Note that the on–board voltage regulators allow for a maximum VCO control voltage range of 0.5 – 4.5 volts.

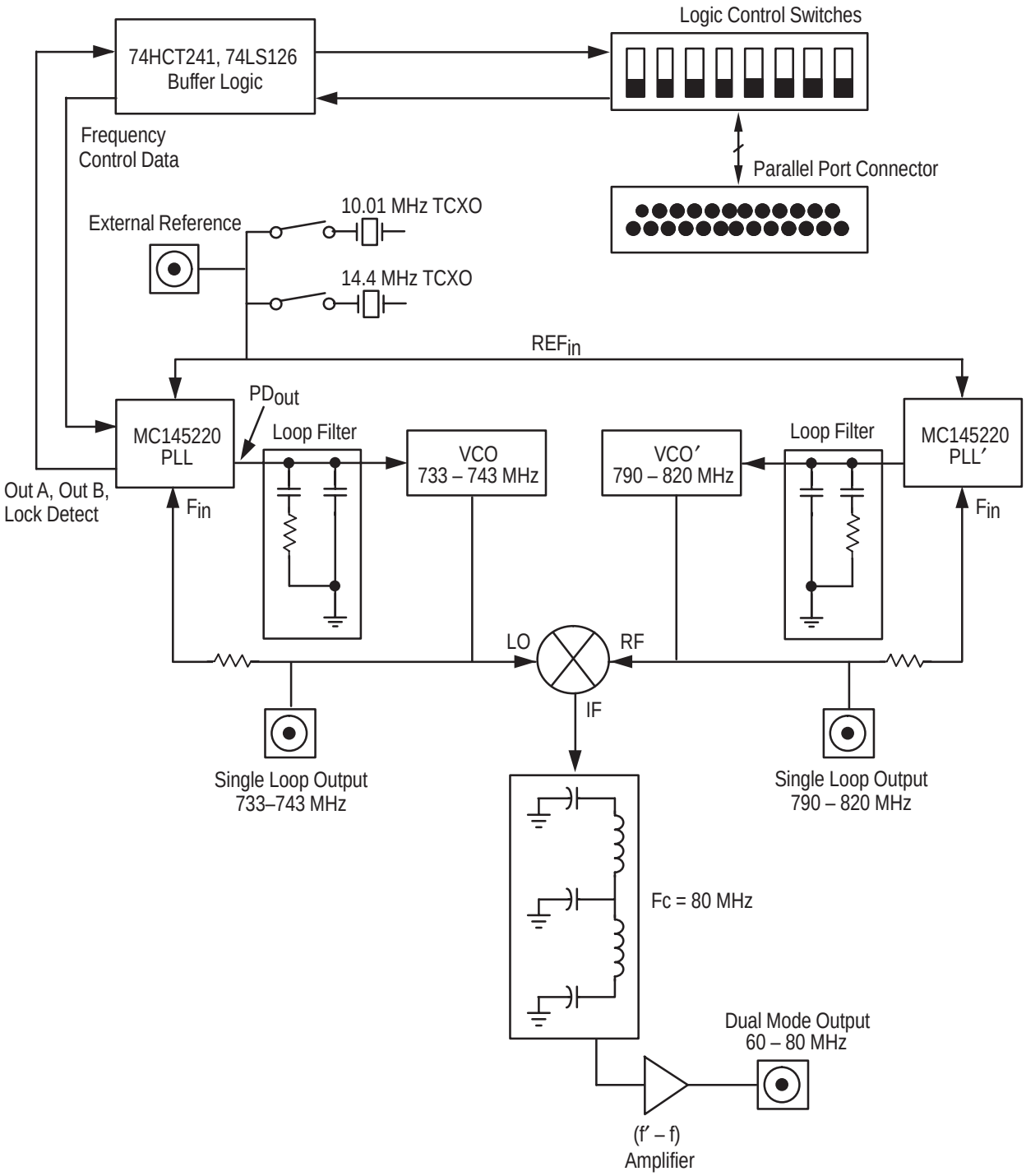


Figure 1. Evaluation Kit Block Diagram

TYPICAL PERFORMANCE

Typical performance applies only to the configuration as shipped. The MC145220EVK is shipped with V+ = 5 V. For lowest phase noise in single or dual loop mode, a 50 Ω load must be connected to J12.

	Single Loop PLL	Single Loop PLL′	Dual Loop PLL
Supply Voltage (J8)	11.5 – 12.5 V		
Supply Current (J8) (Note 1)	177 mA		
Available Current (Note 2)	45 mA		
Frequency Range (Note 3)	733 – 743 MHz	790 – 820 MHz	60 – 80 MHz
Reference Frequency (M1)	10.01 MHz		
Temperature Stability (M1, – 30°C to + 70°C)	< ± 2.5 ppm		
Reference Frequency (M5)	14.4 MHz		N/A
Temperature Stability (M5, – 30°C to + 85°C)	< ± 2 ppm		N/A
TCXO Aging (M1, M5)	< ± 1 ppm / year		
Step Size	10 kHz		10 Hz
Power Output	– 3.0 dBm	– 5.0 dBm	4.5 – 7.5 dBm
Frequency Accuracy	± 1.5 kHz	± 1.5 kHz	± 50 Hz
Reference Sidebands (Note 4)	– 57 dB	– 74 dB	– 57 dB
Phase Noise (100 Hz)	– 65 dBc/Hz	– 56 dBc/Hz	– 50 dBc/Hz
Phase Noise (10 kHz) (Note 5)	– 104 dBc/Hz	– 90 dBc/Hz	– 89 dBc/Hz
Switching Time (Note 6)	24 ms	40 ms	45 ms

NOTES:

1. Supply current is current the board requires without user modifications.
2. Available current is the sum of currents available to the user (in the prototype area) from the 5 V and 8.5 V supply. The 12 V supply is not regulated. Current at 12 V is limited by the external power supply. If the on–board VCO and amplifier are disconnected from the power bus, more current can be drawn in the prototype area. The current flowing into U5 (the 8.5 V regulator) should not exceed 180 mA. This will limit temperature rise in U5.
3. Frequency ranges require use of the 5 V default charge pump supply voltage.
4. VCO sidebands on PLL at low step sizes (10 kHz) are limited by control line leakage of the VCO. Up to 24 nA of leakage has been seen. At higher step sizes (100 kHz and above), this effect is much less noticable. This did not affect PLL′ because its VCO leakage was less than 10 pA.
5. 10 kHz phase noise is limited by the PLL device noise. For low noise designs, the loop bandwidth is made narrower and the VCO is relied upon to provide the 10 kHz phase noise. This can be seen on the EVKs since the VCOs have much lower noise.
6. 10 MHz step, within ± 1 kHz of final frequency ('220).
   Due to the software architecture, when the user is measuring the switching time of a single board in dual loop mode, it takes 20 ms to load the data as compared to single loop mode, which takes 8 ms to load the data. This is a limitation of the software, not the IC.
   To find the actual PLL switching time, subtract 8 or 20 ms from the switching time stated in the table.

SUPPORT MATERIAL

The following documents are included in the appendix:

1. Schematic diagram of MC145220EVK.
2. Bill of materials.
3. Parts layout diagram.
4. Mechanical drawing of board.
5. MC145220 data sheet.
6. Typical signal plots.

PRODUCTION TEST

After assembly is complete, the following alignment and test is performed:

1. The control program is started in ’220 single loop mode.
2. [L]! is selected to set PLL frequency to 733 MHz.
3. Power is applied to the board. DIP switch section 1 is closed circuit with all others being open circuit.
4. After attaching computer cable, [I]! is selected.
5. Trim resistor VR1 is adjusted to obtain an output frequency at J5 of 733 MHz $\pm$ 500 Hz.
6. Voltage at the control voltage test point (TP2) is measured. It must be > 0.5 V.
7. [H]! is selected.
8. Voltage at the control voltage test point (TP2) is measured. It must be < 4.4 V.
9. [T]! is selected to toggle to PLL′.
10. [L]! is selected to set PLL′ frequency to 790 MHz.
11. Voltage at the control voltage test point (TP9) is measured. It must be > 0.5 V.
12. [H]! is selected to set PLL′ frequency to 820 MHz.
13. Voltage at the control voltage test point (TP9) is measured. It must be < 4.4 V.
14. [G] is selected and the board type is changed to ’220 dual loop mode.
15. [Q]!, then [I]!, is selected to initialize the dual mode output (J12) to 70 MHz. The frequency should be 70 MHz $\pm$ 50 Hz.

If in step 5 it isn’t possible to obtain a signal on frequency, the adjustment screw in M1 may be turned for further frequency adjustment range. If neither adjustment works, [P] should be selected and the correct printer port address entered. [I]! is then selected to reload the data.

BOARD OPERATION

A computer is connected to the DB–25 connector J9. Data is output from the printer port. The printer card is in slot 0 using the default address in the control program. Data is sent to the PLL device (U1) through the DIP switch (S1), and 74HCT241 buffer (U2). D1, D2, D3, R7, R8, and R12 are in the data path between the ’HCT241 and PLL device. This limits the high level output voltage of the buffer. Voltage on PLL device inputs must be no greater than 0.5 V above V+. A ’220 PLL has three output lines which are routed through a 74LS126 line driver (U3) back to the computer.

U2, the 74HCT241, provides isolation and logic translation for PLL input lines. Logic translation is needed from the TTL levels on the printer port to the CMOS levels on the ’220 inputs.

A 12 V power supply should be used to power the board at J8 (Augat 2SV–02 connector). The 2SV–02 will accept 18–24 AWG bare copper power leads. No tools are needed for connection. If power is properly connected, LED D4 will be lit.

Power passes from J8 to U5 (LM317 regulator) configured as an 8.5 V regulator. 8.5 V powers the VCOs. Regulators U6 and U7 use the 8.5 V supply to produce 3 V and 5 V. The ’220 board can use either to power the logic and charge pump. V+ voltage is selected by J11. U6 and U7 are cascaded with U5 to equalize their individual voltage drops.

The ’220 operates in both a single loop and dual loop mode. There are no component changes between the two modes. The differences are in the programming of the counters and the SMA connector that is used.

The PLL loop is composed of the MC145220 (U1), 733 – 743 MHz VCO (M2), and a passive loop filter (R4, R5, C6, C7, C8). In single loop mode, output is taken from J5. A passive loop filter was used to keep the design simple, reduce noise, and reduce the quantity of traces susceptible to stray pickup. The PLL′ loop is composed of the MC145220 (U1), 790 – 820 MHz VCO (M3), and a passive loop filter (R22, R25, C24, C26, C30). In single loop mode, output is taken from J10.

Dual mode output is the (f′ – f) frequency output from the mixer. It is low pass filtered (L1, L2, C15, C21, C22) then amplified (U4). The output is available at J12.

Phase detector current is 2 mA. J1 is a removable jumper used for current measurement of V+.

Two TCXOs, a Motorola Saber 14.4 MHz (M5), and Raltron 10.01 MHz (M1) are supplied. As shipped from the factory, the 10.01 MHz TCXO is in use. This allows both the 10 kHz and 10 Hz step sizes to be used with one TCXO. 10.01 MHz cannot be divided for larger step sizes such as 100 kHz. For larger step sizes use the Saber. Jumpers J3, J4, J13, and J14 determine which TCXO or the external reference input is in use.

DUAL MODE OUTPUT

The dual mode output (J12) is the difference frequency from mixing PLL and PLL′. By using a reference frequency of 10.01 MHz, PLL can be operated with a 10.01 kHz step size and PLL′ with a 10 kHz step size. If both PLL and PLL′ step down in frequency, the mixed output will step up by 10 Hz. More information on the offset reference technique is in **AN1277/D, Offset Reference PLLs for Fine Resolution or Fast Hopping**. The block diagram, formulas, and an example are shown in Figure 2.

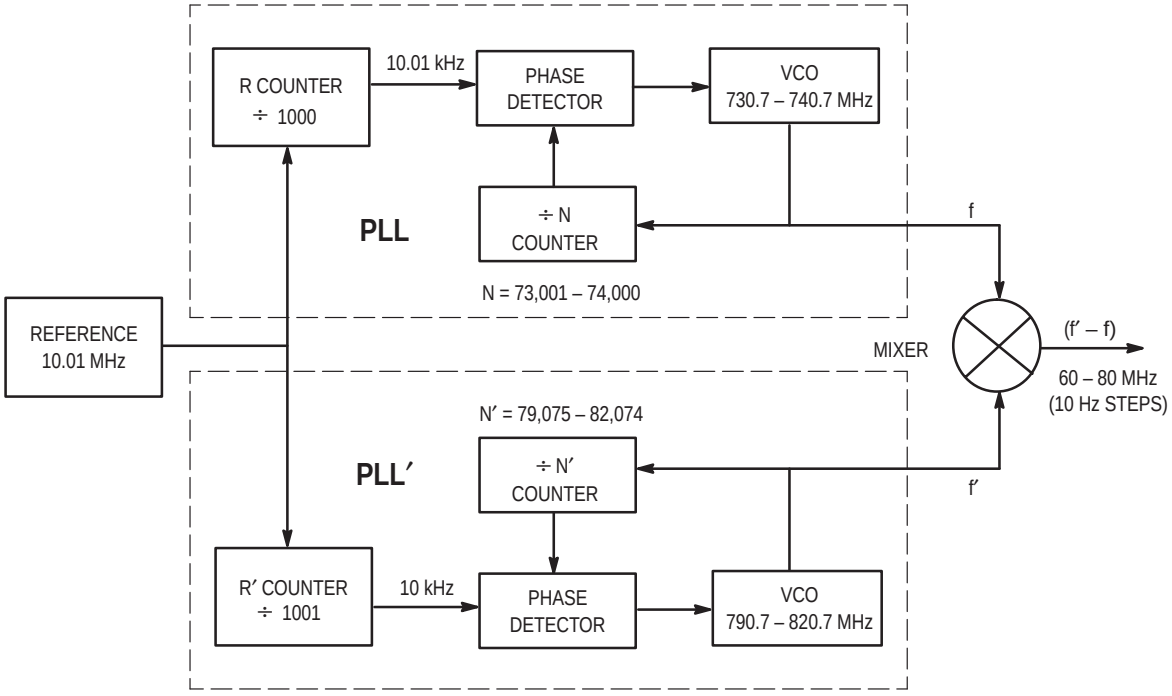


Figure 2. Dual Mode Block Diagram

PLL	PLL′
$f = N\ (10.01\ kHz)$	$f' = N'\ (10\ kHz)$
$f = 10.01\ kHz \left[74{,}000 - \frac{r(f' - f)}{10\ Hz}\right]$	$f' = 10\ kHz \left[\frac{w(f' - f) + 740\ kHz}{10\ kHz} + N\right]$
$N = 74{,}000 - \frac{r(f' - f)}{10\ Hz}$	$N' = N + 74 + \frac{w(f' - f)}{10\ kHz}$
$(f' - f) = w(f' - f) + r(f' - f)$	
$(f' - f)$ = Desired Output Frequency	
$w(f' - f)$ = Output Frequency Portion that Divides Evenly by 10 kHz	
$r(f' - f)$ = Remainder from Output Frequency Division by 10 kHz	

Dual Mode Formulas

Example: Synthesize 76.849 930 MHz

$r(f' - f) = 9.930\ kHz$, $w(f' - f) = 76.840\ MHz$

$N = 74{,}000 - \frac{9.930\ kHz}{10\ Hz} = 73{,}007$ $f = 73{,}007\ (10.01\ kHz) = 730.800\ 070\ MHz$

$N' = 73{,}007 + 74 + \frac{76.840\ MHz}{10\ kHz} = 80{,}765$ $f' = 80{,}765\ (10\ kHz) = 807.650\ 000\ MHz$

$(f' - f) = 807.650\ 000\ MHz - 730.800\ 070\ MHz = 76.849\ 930\ MHz$

EXTERNAL REFERENCE INPUT

To use an external reference, disconnect J3, J4, J13, and J14. Use a reference signal at J2 which complies with data sheet requirements. Then modify the reference frequency in the program main menu to reflect the changes made (F menu item).

DATA TRANSFER FROM COMPUTER TO EVK

To control the serial input EVK with the parallel printer port, a conversion is done. Printer cards are designed to output eight bits through eight lines. A bit mask is used to obtain the bit combination for the three required output lines (Data, Clock, Load). As bytes are sent to the printer card in sequence, it appears to be a serial transfer. The printer port is used because data transfer using the serial port would be much slower. A standard IBM PC can support a parallel port data rate of 4.77 MHz.

IBM PCs and compatibles can accept up to three printer port configurations. These ports are called LPT1, LPT2, and LPT3. Each printer port has a unique address. Two sets of addresses are in common use. One set applies to IBM PC XT, AT, and clones. The other is for the PS 2 line. To load data into the EVK, the correct address must be selected. The program default is $278. If $278 is not the address in use, it must be modified by entering the P menu item in the main menu. All allowed addresses given in hexadecimal are as follows:

Label	IBM PC and Clones	PS 2
LPT1	278	3BC
LPT2	378	378
LPT3	3BC	278

Up to three EVK boards can operate independently from one printer port. All lines on the printer port are connected to every EVK. Even with three boards operating, only three output lines (Clock, Data, and Load) from the printer card are used. If two boards are controlled together, data for the second board is received from the Output A of the first. Output A is a configurable output on ’220 devices, which in this case is used to shift data through chip 1 into chip 2. Output A and Data are connected using a printer port input line. This was done to avoid connecting extra wires. Fortunately not all port input lines are needed for computer input. Load and Clock are common to both boards.

A three–board cascade is handled similarly to a two–board cascade. Out A on the first board is fed to Data on the second. Out A on the second connects to Data on the third. Instructing the program on the quantity of boards connected together allows it to modify the number of bits sent.

All boards have a DIP switch S1 which gives each a unique address. The configuration menu is used to tell the program what type of board is connected at a board address. Switch positions for all possible addresses are given in Figure 2.

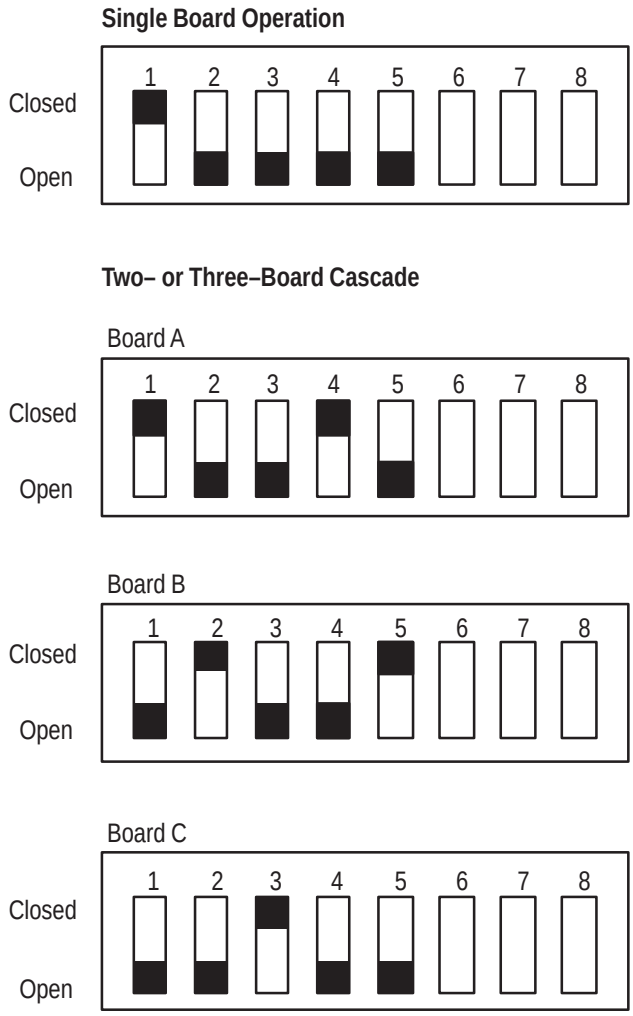


Figure 3. Switch Positions

In Figure 2, DIP switch sections 6, 7, and 8 allow the computer to read Out A, Lock Detect′, or Lock Detect from the PLL device. Each of the inputs can only be read on one board at a time, but each item could be read on a different board. In a three–board cascade, Out A could be read from the first board, Out B from the second, and Lock Detect from the third. There is no way to determine the board address of a particular input with software. The control program does not make use of these inputs; however, source code could be modified as required. Pin assignment on the printer port connector is:

Label	Pin Number
Out A	12
Out B	13
Lock Detect	15

PRINTER PORT CONFIGURATION

Printer port outputs on an IBM PC or clone use TTL–LS logic levels. Inputs are one TTL–LS load. Signal lines can be used for any purpose. The standard names, direction of data flow, true and inverted data are shown in Figure 3.

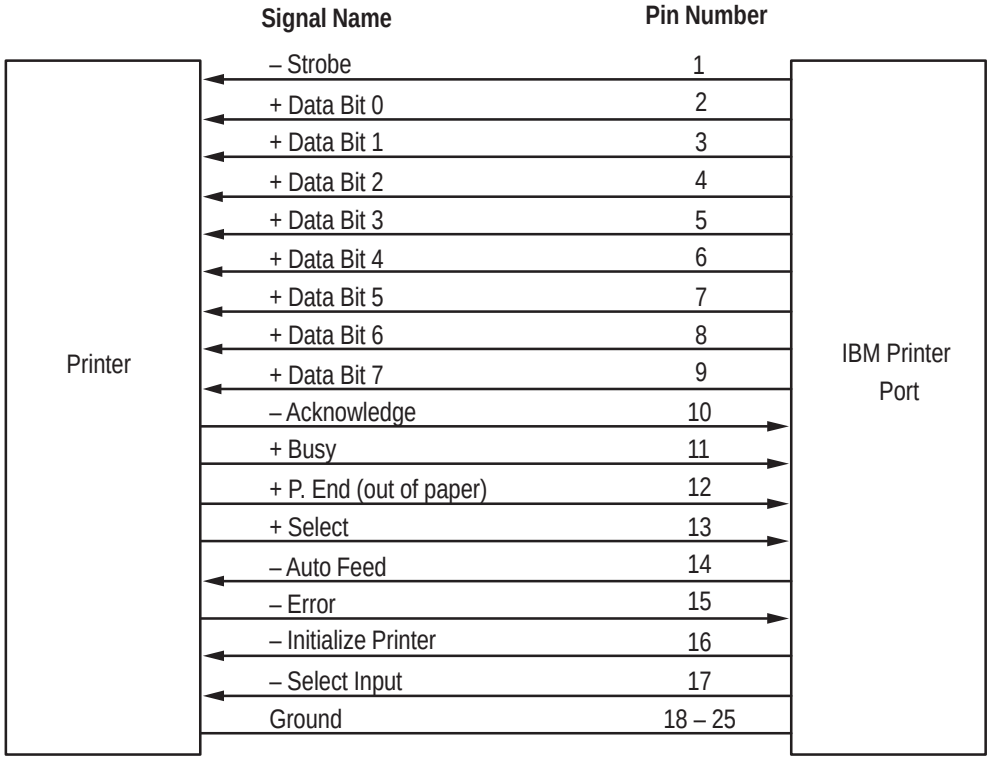


Figure 4. Printer Port Data Lines

Pin numbers for the port connector are shown in Figure 4.

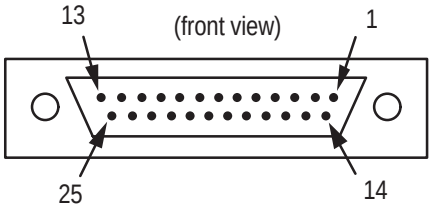


Figure 5. DB–25 Male Connector

SECTION 2 – SOFTWARE DESCRIPTIONS SUMMARY

INTRODUCTION

The MC145xxx EVK control program is used to program all PLL evaluation kits. It will simultaneoulsy control up to three different boards independently from one printer port. All features of the PLL device may be accessed. Default frequencies can be modified to allow use of different channel spacings and VCOs.

User input errors are detected and appropriate messages are displayed.

To show the format of the program, a sample screen is shown below:

‘Select from the available options’

```
                    Welcome to MC145xxx EVK Demonstration Program, rev 4.0
                              Select from the available options

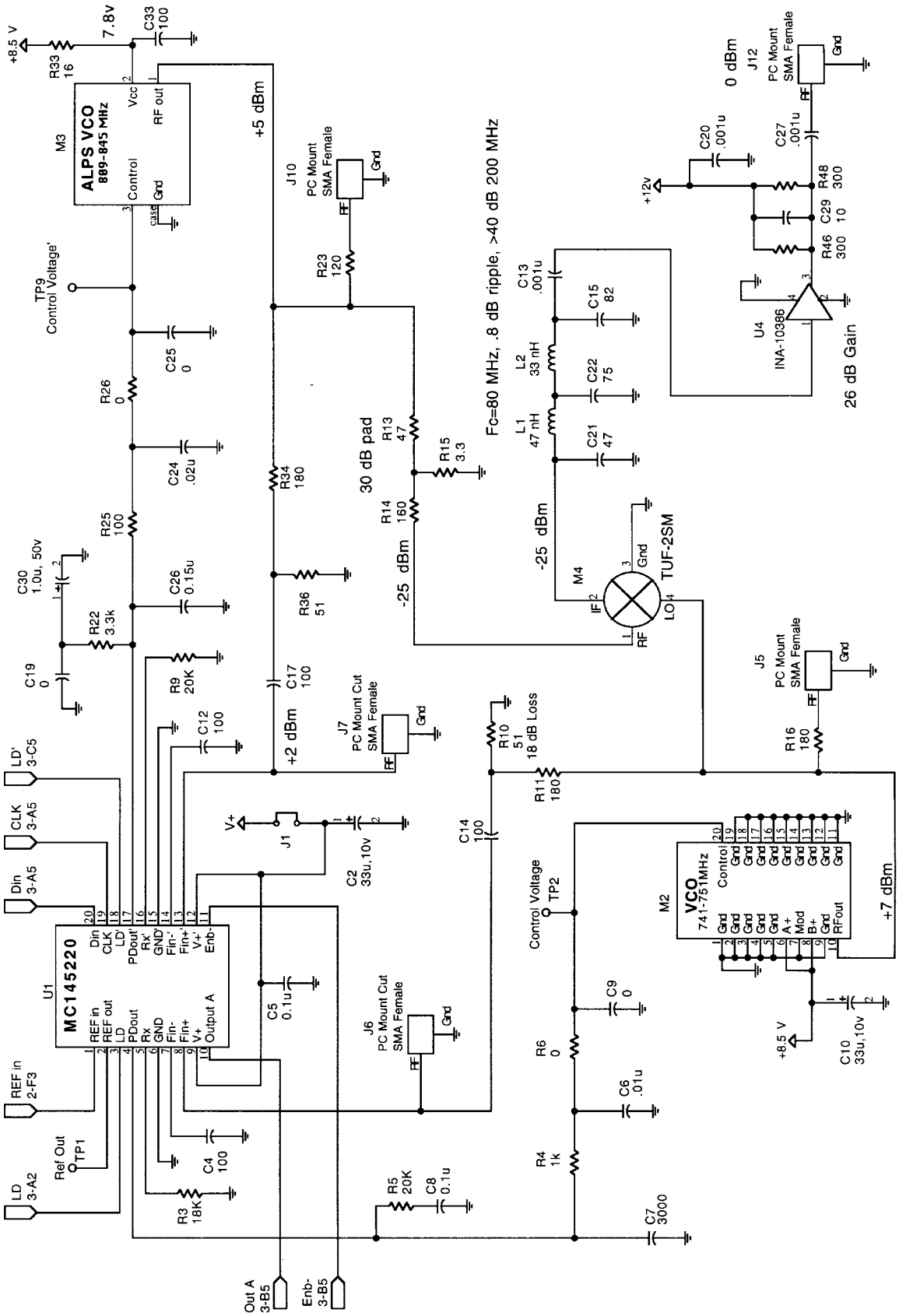
Available Boards – Current target board is: A, MC145220 Dual
 Brd [A]!: MC145220 Dual    Brd [–]!: N/A            Brd [–]!: N/A
--------------------------------------------------------------------------------
MC145xxx Frequency Commands – Current Output Frequency is 70 MHz
 [L]! Set to low freq.     60 MHz [W] Change default low freq.
 [M]! Set to med. freq.    70 MHz [Y] Change default med. freq.
 [H]! Set to high freq.    80 MHz [Z] Change default high freq.
 [U]! Step frequency up by step size    [O] Set PLL output frequency
 [D]! Step frequency down by step size  [F] REFin freq. & channel spacing
MC145xxx Additional Commands
 [E]  Set function of output A          [N] Change C register and Prescale
 [R]  Set crystal/reference mode – Current mode is Ref. mode, REFout low


--------------------------------------------------------------------------------
Initialization/System Setup Commands:
 [P]  Set output port address – Current address is $278
 [G]  Change board definitions
 [I]  Initialize board(s), Write all registers

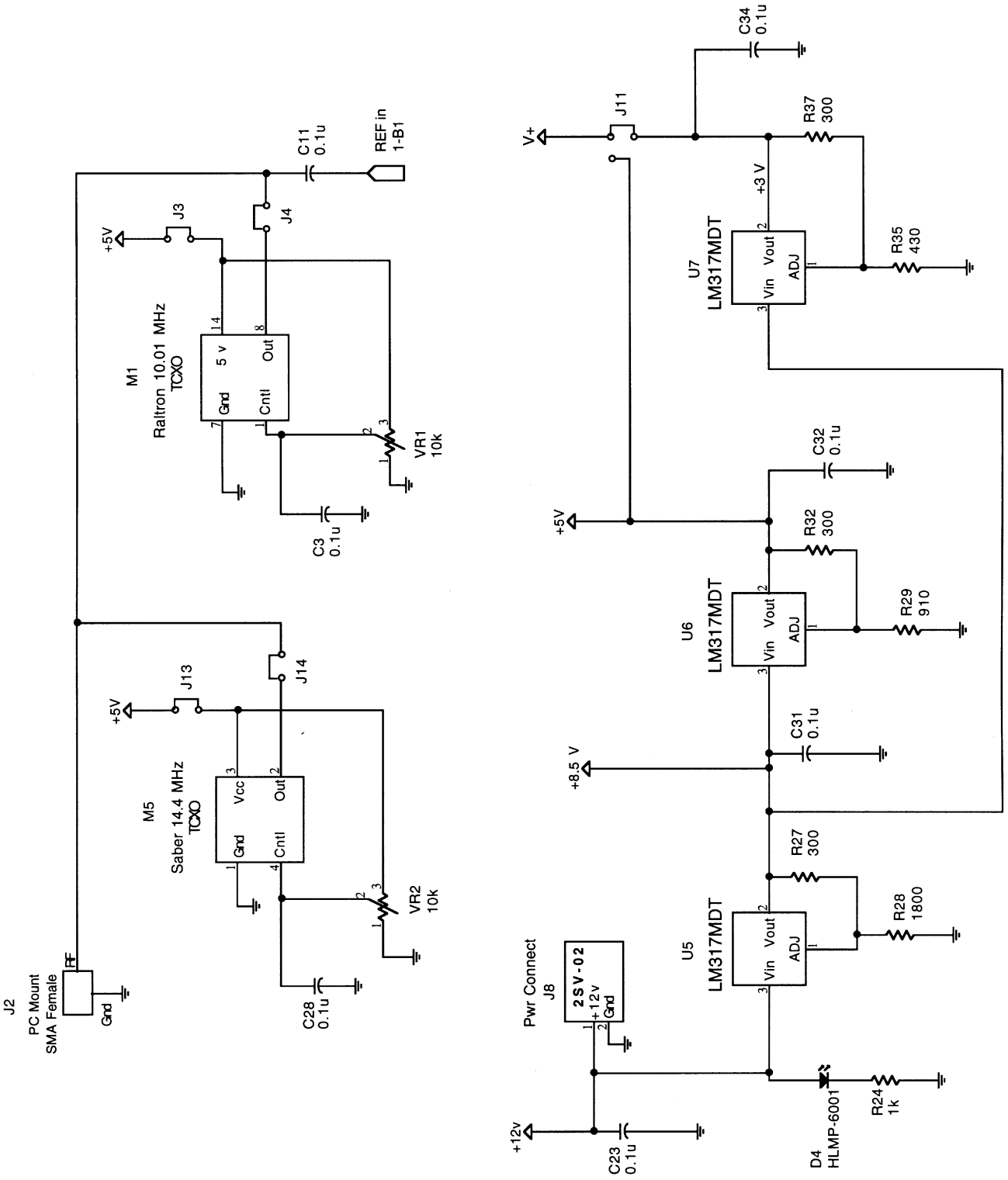
                [X]! Terminate demonstration program. [?]! View help screen.
```

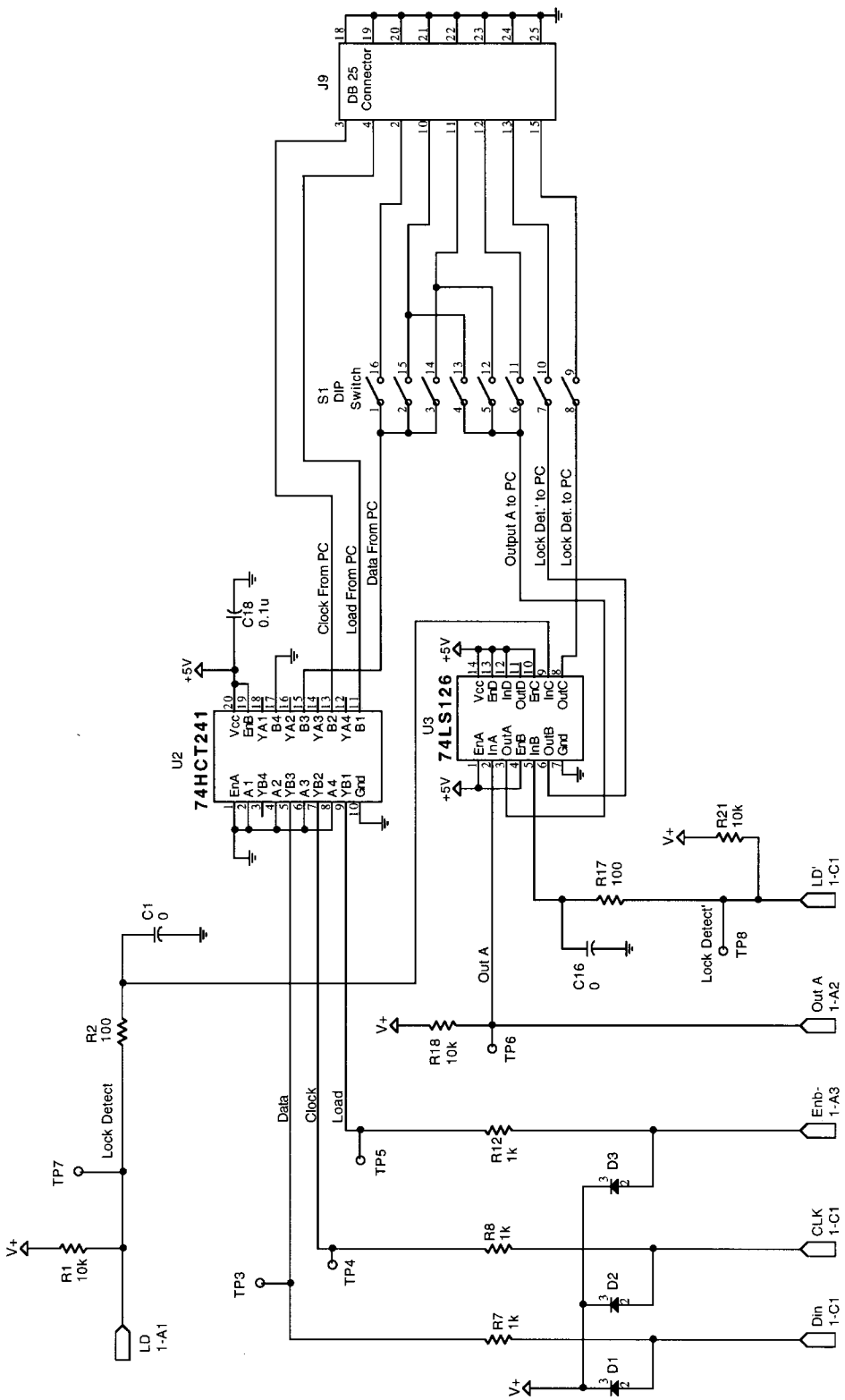
APPENDIX

MC145220 PLL Evaluation Board

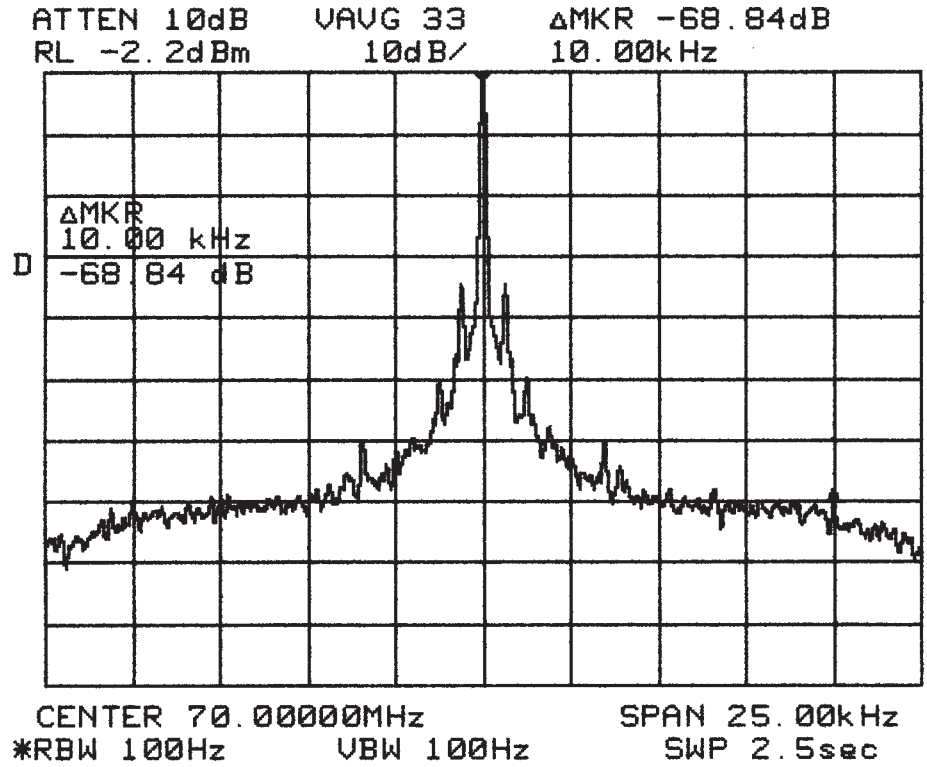


MC145220 Power Supply and Reference

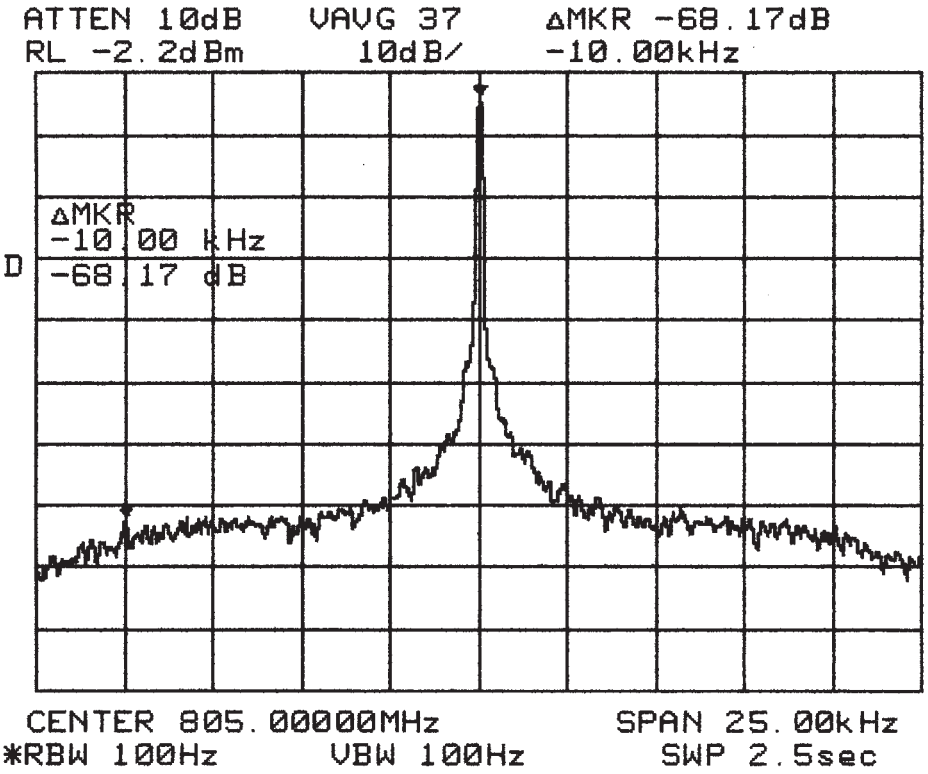



J9
DB 25 Connector
S1
DIP Switch
Clock From PC
Load From PC
Data From PC
Output A to PC
Lock Det.' to PC
Lock Det. to PC
U2
74HCT241
U3
74LS126
C18
0.1u
+5V
C1
0
R2
100
Lock Detect
TP7
V+
R1
10k
LD
1-A1
TP3
TP4
TP5
TP6
TP8
Data
Clock
Load
Out A
R18
10k
R12
1k
R8
1k
R7
1k
D3
D2
D1
R17
100
R21
10k
C16
0
Lock Detect'
LD'
1-C1
Out A
1-A2
Enb-
1-A3
CLK
1-C1
Din
1-C1

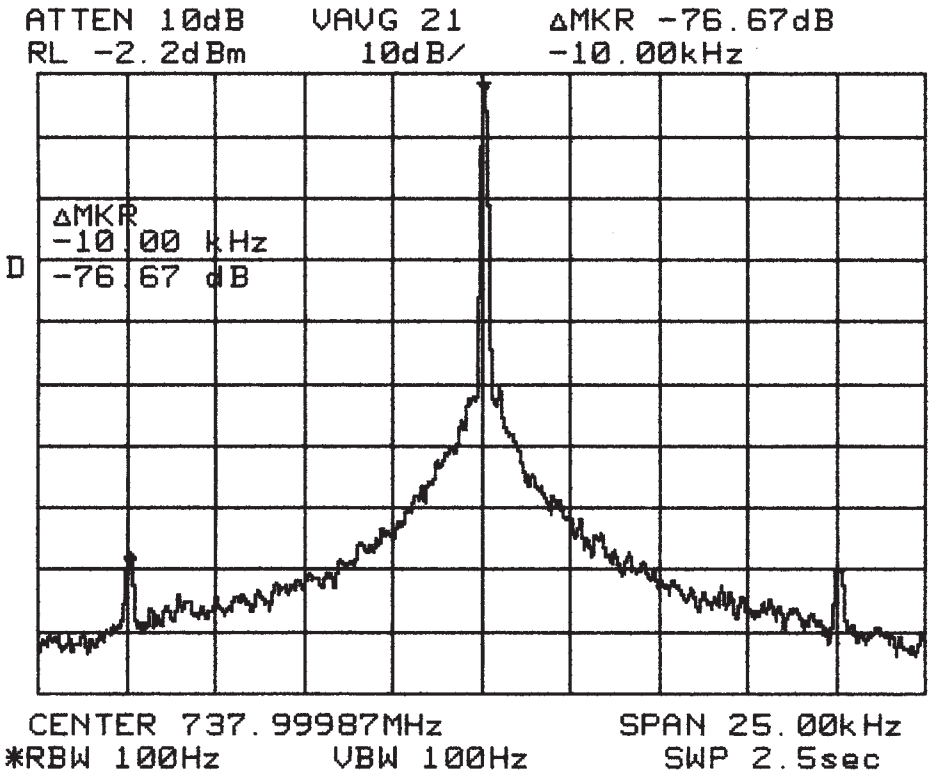
MC145220EVK Signal Plot — Dual Loop Mode Output at 70 MHz



MC145220EVK Signal Plot — Single Loop Mode PLL on 805 MHz



MC145220EVK Signal Plot — Single Loop Mode PLL on 738 MHz



Chapter Five

RF Discrete Transistors

Section One 5.1–0

RF Discrete Transistors – Selector Guide

Section Two 5.2–0

RF Discrete Transistors – Data Sheets

Section One
Selector Guide

Motorola RF Discrete Transistors

Motorola offers the most extensive group of RF Discrete Transistors offered by any semiconductor manufacturer anywhere in the world today.

From Bipolar to FET, from Low Power to High Power, the user can choose from a variety of packages. They include plastic and ceramic that are microstrip circuit compatible or surface mountable. Many are designed for automated assembly equipment.

Major sub–headings are Small Signal, Medium Power, Power MOSFETs and Bipolar Transistors.

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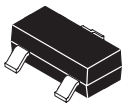
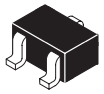
Motorola RF Small Signal Transistors

Motorola's broad line of RF Small Signal Transistors includes NPN Silicon Bipolar Transistors characterized for low noise amplifiers, mixers, oscillators, multipliers, non–saturated switches and low–power drivers.

These devices are available in a variety of package types. Most of these transistors are fully characterized with s–parameters.

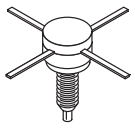
Plastic Packages

Table 1. Plastic

Device	Gain–Bandwidth @		NF_{min} @ f		Gain @ f		Maximum Ratings		Package
	f_T Typ GHz	I_C mA	Typ dB	MHz	Typ dB	MHz	$V_{(BR)CEO}$ Volts	I_C mA	
Case 318–08/6 — SOT–23									
MMBR941LT1[18c]	8.0	15	2.1	2000	8.5	2000	10	50	
MMBR941LT3[18d]	8.0	15	2.1	2000	8.5	2000	10	50	
MMBR941BLT1[18c]	8.0	15	2.1	2000	8.5	2000	10	50	
MMBR951LT1[18c]	8.0	30	2.1	2000	7.5	2000	10	100	
Case 419 — SC–70/SOT–323									
MRF947T1[18c,d]	8.0	15	2.1	2000	10.5	1500	10	50	
MRF947T3[18d]	8.0	15	2.1	2000	10.5	1500	10	50	
MRF947AT1[18c]	8.0	15	2.1	2000	10.5	1500	10	50	
MRF947BT1[18c,d]	8.0	15	2.1	2000	10.5	1500	10	50	
MRF957T1[18c]	9.0	30	2.0	2000	9.0	1500	10	100	
MRF1047T1[18c]	12	15	1.0	1000	13	1000	5.0	45	
Case 463/1 — SC–90/SC–75									
MRF949T1[18c]	9.0	15	1.5	1000	14	1000	–	50	
MRF959T1[18c]	9.0	30	1.6	1000	8.0	1000	–	100	

Ceramic SOE Case

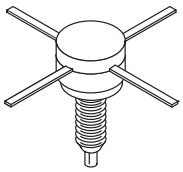
Table 2. Ceramic SOE Case

Device	Gain–Bandwidth @		NF @ f		Gain @ f		Maximum Ratings		Package
	f_T Typ GHz	I_C mA	Typ dB	MHz	Typ dB	MHz	$V_{(BR)CEO}$ Volts	I_C mA	
Case 244A/1									
MRF587	5.5	90	3.0	500	13	500	15	200	

[17]PNP

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

RF Small Signal Transistors Packages



CASE 244A
STYLE 1



CASE 318–08
STYLE 6
(SOT–23)



CASE 419
(SC–70/SOT–323)



CASE 463
STYLE 1
(SC–90/SC–75)

Motorola RF Medium Power Transistors

RF Medium Power Transistors are used in portable transmitter applications and low voltage drivers for higher power devices. They can be used for analog cellular, GSM and the newer digital handheld cellular phones. GaAs, LDMOS and Bipolar devices are available. RF Medium Power Transistors are supplied in Motorola's high performance PLD line of surface mount power RF packages. Other applications include talkback pagers, wireless modems and LANs, cable modems, highspeed drivers and instrumentation.

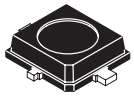
Discrete Wireless Transmitter Devices

Device	Freq. MHz	V_{DD} V	Typical Output Power dBm	Typical Drain Eff. %	Typical Gain dB	Semiconductor Technology	Case No./ Package
MRF9382T1 (18f, 46a)	900	6.0	36.5	65	10.5	LDMOS	449/PLD–1
MRF9482T1 (18f, 46a)	900	4.8	36.0	65	10	LDMOS	449/PLD–1

(18) Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

(46) To be introduced: a) 1Q00 b) 2Q00 c) 3Q00

RF Medium Power Transistors Packages



CASE 449
(PLD–1)

Motorola RF High Power Transistors

RF Power MOSFETs

Motorola RF Power MOSFETs are constructed using a planar process to enhance manufacturing repeatability. They are *N–channel field effect transistors* with an oxide insulated gate which controls vertical current flow.

Compared with bipolar transistors, RF Power FETs exhibit higher gain, higher input impedance, enhanced thermal stability and lower noise. The FETs listed in this section are specified for operation in RF Power Amplifiers and are grouped by frequency range of operation and type of application. Arrangement within each group is first by order of voltage then by increasing output power.

Table 1. 2 to 150 MHz HF/SSB – Vertical MOSFETs

For military and commercial HF/SSB fixed, mobile and marine transmitters.

Device	Frequency Band(37)	P_{out} Watts	Gain (Typ) @ 30 MHz dB	Typical IMD d_3 dB	Typical IMD d_{11} dB	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB							
MRF171A	U	2–225	30	20	–32	—	1.52	211–07/2
V_{DD} = 50 Volts, Class AB							
MRF148A	U	2–225	30	18	–35	–60	1.5	211–07/2
MRF150	U	2–150	150	17	–32	–60	0.6	211–11/2
MRF154	U	2–100	600	17	–25	—	0.13	368/2
MRF157	U	2–100	600	20	–25	—	0.13	368/2

Table 2. 2 to 225 MHz VHF AM/FM – Vertical MOSFETs

For VHF military and commercial aircraft radio transmitters.

Device	Frequency Band(37)	P_{out} Watts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB						
MRF134	U	30–225	5	14/150	55	10	211–07/2
MRF136	U	30–225	15	16/150	60	3.2	211–07/2
MRF171A	U	30–225	45	19.5/150	65	1.52	211–07/2
MRF173	U	30–225	80	13/150	65	0.8	211–11/2
MRF174	U	30–225	125	11.8/150	60	0.65	211–11/2
MRF141	U	2–175	150	10/175	55	0.6	211–11/2
MRF141G	U	2–175	300	13/175	55	0.35	375/2
V_{DD} = 50 Volts, Class AB						
MRF151	U	2–175	150	13/175	45	0.6	211–11/2
MRF151G	U	2–175	300	16/175	55	0.35	375/2

(37)M = Matched Frequency Band; U = Unmatched Frequency Band.

Table 3. 30 to 512 MHz VHF/UHF AM/FM

For VHF/UHF military and commercial aircraft radio transmitters.

Device	Frequency Band(37)		P_{out} Watts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB – Vertical MOSFETs							
MRF158	U	30–512	2	17.5/500	52	13.2	305A/2
MRF160	U	30–512	4	17/500	55	7.2	249/3
MRF166C	U	30–512	20	16/500	55	2.5	319/3
MRF166W	U	30–512	40	16/500	55	1.0	412/1
MRF177	U	100–400	100	12/400	60	0.65	744A/2
MRF275L	U	150–512	100	8.8/500	55	0.65	333/2
MRF275G	U	150–512	150	11.2/500	55	0.44	375/2

Table 4. Mobile – To 520 MHz

Designed for broadband VHF & UHF commercial and industrial applications. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 12.5/7.5 volt mobile, portable and base station operation.

Device	Frequency Band(37)		P_{out} Watts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Package/Style
VHF & UHF, V_{DD} = 7.5 Volts, Class AB, Land Mobile Radio – LDMOS Die							
MRF1511T1(18f,46a)	U	136–175	8	11.5/175	55	2.0	466/1
MRF1517T1(18f,46a)	U	430–520	8	11/520	55	2.0	466/1
VHF & UHF, V_{DD} = 7.5/12.5 Volts, Class AB, Land Mobile Radio – LDMOS Die							
MRF1513T1(18f,46a)	U	400–520	3	11/520	55	2.0	466/1
VHF & UHF, V_{DD} = 12.5 Volts, Class AB, Land Mobile Radio – LDMOS Die							
MRF1518T1(18f,46a)	U	400–520	8	11/520	55	2.0	466/1

Table 5. Broadcast – To 1.0 GHz – Lateral MOSFETs

Device	Frequency Band(37)		P_{out} Watts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	IMD dBc	Package/Style
470 – 1000 MHz, V_{DD} = 28 Volts, Class AB – LDMOS Die								
MRF373	U	470–1000	60	14.7/860	54	1.0	—	360B/1
MRF373S	U	470–1000	60	14.7/860	54	0.75	—	360C/1
MRF372(9)	M	470–1000	180 PEP	14.0/860	35	0.4	–30	375B/2
MRF374	U	470–1000	100 PEP	13.5/860	36	0.5	–31	375F/2
470 – 1000 MHz, V_{DD} = 50 Volts, Class AB – LDMOS Die								
MRF376(9)	M	470–1000	240	14/860	55	0.3	—	375B/2

(9)In development.

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

(37)M = Matched Frequency Band; U = Unmatched Frequency Band.

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

Table 6. Cellular – To 1.0 GHz – Lateral MOSFETs

Device	Frequency Band(37)		P_{out} Watts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Package/Style
800 – 1.0 GHz, V_{DD} = 26 Volts, Class AB – LDMOS Die							
MRF6522–5R1(18a,46a)	U	960	5 CW	18/960	53	15	458A/1
MRF6522–10R1(18a,46a)	U	960	10 CW	17.5/960	55	6.0	458A/1
MRF6522–70(18i)★	M	921–960	70 CW	16/921–960	58	1.1	465D/1
MRF187	M	880	85 PEP	13/880	33	0.7	465/1
MRF187S	M	880	85 PEP	13/880	33	0.7	465A/1
MRF9085(46a)	M	880	85 PEP	17/880	38	0.7	465/1
MRF9085S(46a)	M	880	85 PEP	17/880	38	0.7	465A/1
MRF9180(46a)	M	880	180 PEP	17/880	38	0.4	375D/2
800 – 1.0 GHz, V_{DD} = 28 Volts, Class AB – LDMOS Die							
MRF181SR1(18a,46a)	U	945	8 PEP	17/945	35	3.6	458/1
MRF181ZR1(18a,46a)	U	945	8 PEP	17/945	35	3.6	458A/1
MRF182	U	945	30 CW	14/945	58	1.75	360B/1
MRF182S(18a)	U	945	30 CW	14/945	58	1.75	360C/1
MRF183	U	945	45 PEP	13.5/945	38	1.5	360B/1
MRF183S(18a)	U	945	45 PEP	13.5/945	38	1.5	360C/1
MRF9045(46a)	U	945	45 PEP	18/945	42	1.3	360B/1
MRF9045S(46a)	U	945	45 PEP	18/945	42	1.3	360C/1
MRF9045M(46a)	U	945	45 PEP	16/945	40	TBD	1265/–
MRF184	U	945	60 CW	13.5/945	60	1.1	360B/1
MRF184S(18a)	U	945	60 CW	13.5/945	60	1.1	360C/1
MRF185(3)	M	960	85 CW	14/960	53	0.7	375B/2
MRF186(3)	M	945	120 PEP	12/945	35	0.6	375B/2

Table 7. PCS and 3G – To 2.1 GHz – Lateral MOSFETs

Device	Frequency Band(37)		P_{out} Watts	Class	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Package/Style
1805 – 1990 MHz, V_{DD} = 26 Volts – LDMOS Die (GSM1800, GSM1900 and PCS TDMA)								
MRF18060A★	M	1805–1880	60 CW	AB	13/1805–1880	45	0.97	465/1
MRF18060AS★	M	1805–1880	60 CW	AB	13/1805–1880	45	0.97	465A/1
MRF18060B★	M	1930–1990	60 CW	AB	13/1930–1990	45	0.97	465/1
MRF18060BS★	M	1930–1990	60 CW	AB	13/1930–1990	45	0.97	465A/1
MRF18090A★	M	1805–1880	90 CW	AB	13.5/1805–1880	52	0.7	465B/1
MRF18090AS★	M	1805–1880	90 CW	AB	13.5/1805–1880	52	0.7	465C/1
MRF18090B★	M	1930–1990	90 CW	AB	13.5/1930–1990	45	0.7	465B/1
MRF18090BS★	M	1930–1990	90 CW	AB	13.5/1930–1990	45	0.7	465C/1
1.9 GHz, V_{DD} = 26 Volts – LDMOS Die (PCS CDMA)								
MRF19030(46a)	M	1930–1990	30 PEP	AB	13/1990	36	1.2	465E/1
MRF19030S(46a)	M	1930–1990	30 PEP	AB	13/1990	36	1.2	465F/1
MRF19045(46a)	M	1930–1990	45 PEP	AB	14/1990	37	0.84	465E/1
MRF19045S(46a)	M	1930–1990	45 PEP	AB	14/1990	37	0.84	465F/1
MRF19060★	M	1930–1990	60 PEP	AB	12.5/1990	36	0.97	465/1
MRF19060S★	M	1930–1990	60 PEP	AB	12.5/1990	36	0.97	465A/1

(3)Internal Impedance Matched Push-Pull Transistors

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

(37)M = Matched Frequency Band; U = Unmatched Frequency Band.

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

★New Product

Table 7. PCS and 3G – To 2.1 GHz – Lateral MOSFETs (continued)

Device	Frequency Band(37)	P_{out} Watts	Class	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Package/Style
1.9 GHz, V_{DD} = 26 Volts – LDMOS Die (PCS CDMA) (continued)							
MRF19090★	M	1930–1990	90 PEP	AB	11.5/1990	35	0.65	465B/1
MRF19090S(18a)★	M	1930–1990	90 PEP	AB	11.5/1990	35	0.65	465C/1
MRF19085(46a)	M	1930–1990	90 PEP	AB	12.5/1990	37	0.64	465/1
MRF19085S(46a)	M	1930–1990	90 PEP	AB	12.5/1990	37	0.64	465A/1
MRF19120(3,46a)	M	1930–1990	120 PEP	AB	11.8/1990	34.5	0.45	375D/2
MRF19120S(3,46a)	M	1930–1990	120 PEP	AB	11.8/1990	34.5	0.45	375E/2
MRF19125(46a)	M	1930–1990	125 PEP	AB	12.5/1990	35	0.53	465B/1
MRF19125S(46a)	M	1930–1990	125 PEP	AB	12.5/1990	35	0.53	465C/1
2.0 GHz, V_{DD} = 26 Volts – LDMOS Die							
MRF281SR1(18a,46a)	U	1930–2000	4 PEP	A, AB	13.6/2000	41	8.75	458/1
MRF281ZR1(18a,46a)	U	1930–2000	4 PEP	A, AB	13.6/2000	41	8.75	458A/1
MRF282SR1(18a,46a)	U	1930–2000	10 PEP	A, AB	12.5/2000	34	2.9	458/1
MRF282ZR1(18a,46a)	U	1930–2000	10 PEP	A, AB	12.5/2000	34	2.9	458A/1
MRF284	U	1930–2000	30 PEP	A, AB	10.5/2000	35	2.0	360B/1
MRF284SR1(18a)	U	1930–2000	30 PEP	A, AB	10.5/2000	35	2.0	360C/1
MRF286(46a)	M	1930–2000	60 PEP	A, AB	10.5/2000	31	0.73	465/1
MRF286S(46a)	M	1930–2000	60 PEP	A, AB	10.5/2000	31	0.73	465A/1
2.1 GHz, V_{DD} = 28 Volts – LDMOS Die (W–CDMA, UMTS)							
MRF21030(46a)	M	2110–2170	30 PEP	AB	13.5/2170	33	1.2	465E/1
MRF21030S(46a)	M	2110–2170	30 PEP	AB	13.5/2170	33	1.2	465F/1
MRF21060★	M	2110–2170	60 PEP	AB	12.5/2170	34	1.02	465/1
MRF21060S★	M	2110–2170	60 PEP	AB	12.5/2170	34	1.02	465A/1
MRF21090(46a)	M	2110–2170	90 PEP	AB	11.7/2170	33	0.65	465B/1
MRF21090S(46a)	M	2110–2170	90 PEP	AB	11.7/2170	33	0.65	465C/1
MRF21120(3,46a)	M	2110–2170	120 PEP	AB	11.3/2170	35	0.45	375D/2
MRF21120S(3,46a)	M	2110–2170	120 PEP	AB	11.3/2170	35	0.45	375E/2
MRF21125(26,46a)	M	2110–2170	125 PEP	AB	12/2170	34	0.53	465B/1
MRF21125S(26,46a)	M	2110–2170	125 PEP	AB	12/2170	34	0.53	465C/1
MRF21180(3,46a)	M	2110–2170	160 PEP	AB	11.3/2170	33	0.39	375D/2
MRF21180S(3,46a)	M	2110–2170	160 PEP	AB	11.3/2170	33	0.39	375E/2

(3)Internal Impedance Matched Push-Pull Transistors

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

(26)W–CDMA = 20 W P_{out}, 13 dB Gain, 18% Efficiency, 2.1125–2.1675 GHz.

(37)M = Matched Frequency Band; U = Unmatched Frequency Band.

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

RF Power Bipolar Transistors

Motorola's broad line of bipolar RF power transistors are characterized for operation in RF power amplifiers. Typical applications are in base stations, military and commercial landmobile, avionics and marine radio transmitters. Groupings are by frequency band and type of application. Within each group, the arrangement of devices is by major supply voltage rating, then in the order of increasing output power. All devices are NPN polarity except where otherwise noted.

UHF Transistors

Table 1. 100 – 500 MHz Band

Designed for UHF military and commercial aircraft radio transmitters.

Device	Frequency Band(37)		P_{out} Watts	Gain (Min)/Freq. dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class C						
MRF392(3)	M	100–400	125	8/400	0.65	744A/1
MRF393(3)	M	100–512	100	7.5/500	0.65	744A/1

900 MHz Transistors

Table 2. 900 – 960 MHz Band

Designed specifically for the 900 MHz mobile radio band, these devices offer superior gain, ruggedness, stability and broadband operation. Devices are for mobile and base station applications.

Device	Frequency Band(37)		P_{out} Watts	Class	Gain (Min)/Freq. dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 24 Volts — Si Bipolar							
MRF858S	U	840–900	3.6 (CW)	A	11/900	6.9	319A/2
MRF897(3)	M	900	30	AB	10/900	1.7	395B/1
MRF897R(3)	M	900	30	AB	10.5/900	1.7	395E/1
MRF898(2)	M	850–900	60 (CW)	C	7/900	1	333A/1
V_{CC} = 26 Volts — Si Bipolar							
MRF6409	M	921–960	20	AB	10/960	3.8	319/2
MRF6414	M	921–960	50	AB	8.5/960	1.3	333A/2
MRF899(3)	M	900	150	AB	8/900	0.8	375A/1

1.5 GHz Transistors

Table 3. 1600 – 1640 MHz Band

Device	Frequency Band(37)		P_{out} Watts	Class	Gain (Min)/Freq. dB/MHz	η Eff. (Min) %	θ_{JC} °C/W	Package/Style
MRF16006	M	1600–1640	6	C	7.4/1600	40	6.8	395C/2
MRF16030	M	1600–1640	30	C	7.5/1600	40	1.7	395C/2

(2)Internal Impedance Matched

(3)Internal Impedance Matched Push-Pull Transistors

(37)M = Matched Frequency Band; U = Unmatched Frequency Band.

Microwave Transistors

Table 4. L–Band Long Pulse Power

These products are designed for pulse power amplifier applications in the 960–1215 MHz frequency range. They are capable of handling up to 10 μs pulses in long pulse trains resulting in up to a 50% duty cycle over a 3.5 millisecond interval. Overall duty cycle is limited to 25% maximum. The primary applications for devices of this type are military systems, specifically JTIDS and commercial systems, specifically Mode S. Package types are hermetic.

Device	Frequency Band(37)		P_{out} Watts	Gain (Min) @ 1215 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts — Class C Common Base						
MRF10005	M	960–1215	5	8.5	8	336E/1
V_{CC} = 36 Volts — Class C Common Base						
MRF10031	M	960–1215	30	10	3	376B/1
MRF10120	M	960–1215	120	8	0.6	355C/1
V_{CC} = 50 Volts — Class C Common Base						
MRF10150	M	1025–1150	150	10(7)	0.25	376B/1
MRF10350	M	1025–1150	350	9(7)	0.11	355E/1
MRF10502	M	1025–1150	500	9(7)	0.12	355J/1

Linear Transistors

The following sections describe a wide variety of devices specifically characterized for linear amplification. Included are medium power and high power parts covering frequencies to 2.0 GHz.

Table 5. UHF Ultra Linear For TV Applications

The following device has been characterized for ultra–linear applications such as low–power TV transmitters in Band IV and Band V and features diffused ballast resistors and an all–gold metal system to provide enhanced reliability and ruggedness.

Device	Frequency Band(37)		P_{out} Watts	Gain (Typ)/Freq. Small Signal Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class AB						
TPV8100B	M	470–860	100(11)	9.5/860	0.7	398/1

Table 6. Microwave Linear for PCN Applications

The following devices have been developed for linear amplifiers in the 1.5–2 GHz region and have characteristics particularly suitable for PDC, PCS or DCS1800 base station applications.

Device	Frequency Band(37)		P_{out} Watts	Class	Gain (Typ)/Freq. dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 26 Volts–Bipolar Die							
MRF6404(16)	M	1860–1900	30	AB	8.2/1880	1.4	395C/1
MRF20030R	M	2000	30	AB	11/2000	1.4	395C/1
MRF20060R	M	2000	60	AB	9.8/2000	0.7	451/1
MRF20060RS	M	2000	60	AB	9.8/2000	0.7	451A/1

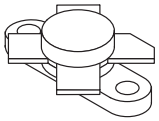
(7)Typical @ 1090 MHz

(11)Output power (Min) at 1 dB compression in Class AB

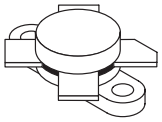
(16)Formerly known as “TP4035”

(37)M = Matched Frequency Band; U = Unmatched Frequency Band.

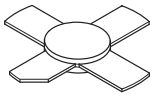
RF Power MOSFETs and Bipolar Transistors Packages



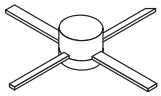
CASE 211–07
STYLE 2
(.380″ FLANGE)



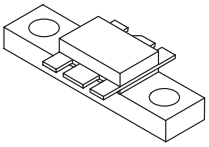
CASE 211–11
STYLE 2
(.500″ FLANGE)



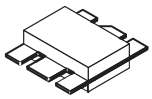
CASE 249–06
STYLE 3



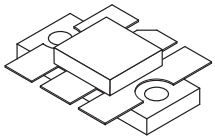
CASE 305A
STYLE 1, 2
(.204″ PILL)



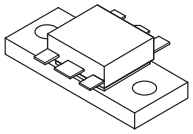
CASE 319
STYLE 1, 2, 3
(CS–12)



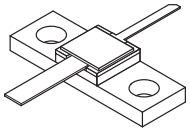
CASE 319A
STYLE 2



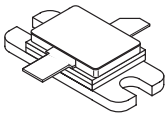
CASE 333
STYLE 2



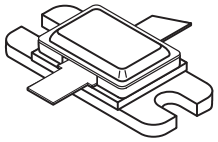
CASE 333A
STYLE 1, 2
(MAAC PAC)



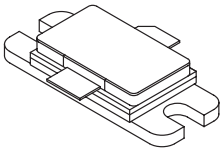
CASE 336E
STYLE 1



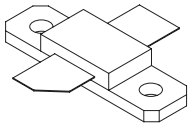
CASE 355C
STYLE 1



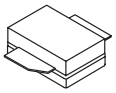
CASE 355E
STYLE 1



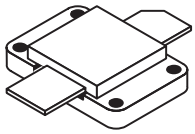
CASE 355J–02
STYLE 1



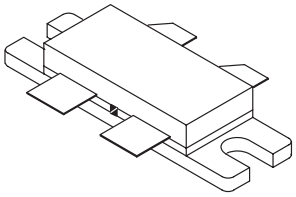
CASE 360B
STYLE 1
(Micro 250)



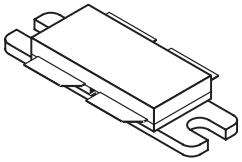
CASE 360C
STYLE 1
(Micro 250S)



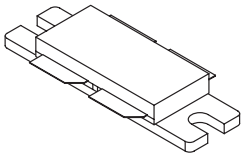
CASE 368
STYLE 2
(HOG PAC)



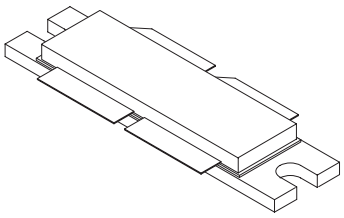
CASE 375
STYLE 2



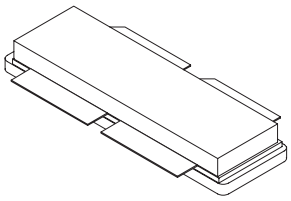
CASE 375A
STYLE 1



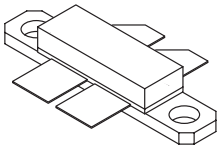
CASE 375B
STYLE 2
(Micro 860)



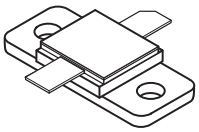
CASE 375D
STYLE 2



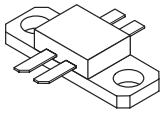
CASE 375E
STYLE 2



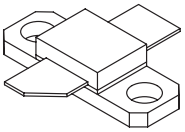
CASE 375F
STYLE 1



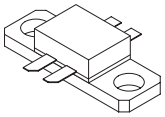
CASE 376B
STYLE 1



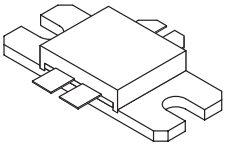
CASE 395B
STYLE 1



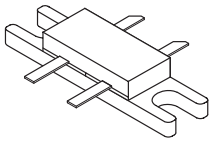
CASE 395C
STYLE 1, 2



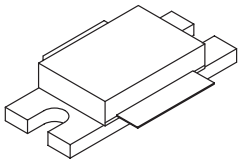
CASE 395E
STYLE 1



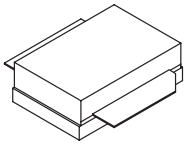
CASE 398
STYLE 1



CASE 412
STYLE 1



CASE 451
STYLE 1



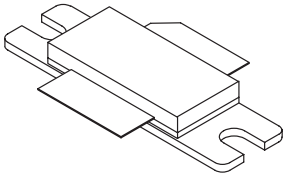
CASE 451A
STYLE 1



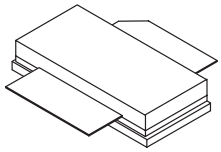
CASE 458
STYLE 1
(Micro 200S)



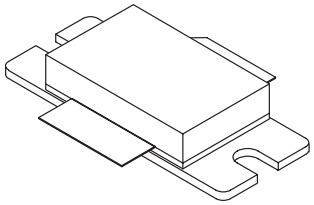
CASE 458A
STYLE 1
(Micro 200Z)



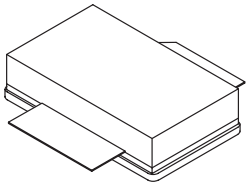
CASE 465
STYLE 1



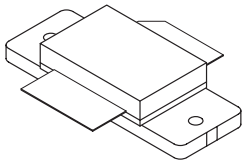
CASE 465A
STYLE 1



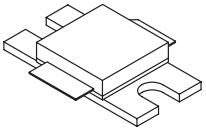
CASE 465B
STYLE 1



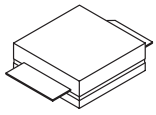
CASE 465C
STYLE 1



CASE 465D
STYLE 1



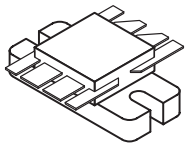
CASE 465E
STYLE 1



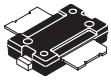
CASE 465F
STYLE 1



CASE 466
STYLE 1
PLASTIC
(PLD 1.5)



CASE 744A
STYLE 1, 2



CASE 1265
PLASTIC
(TO–270)

Section Two

Motorola RF Discrete Transistors – Data Sheets

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MRF136	5.2–35
MRF141	5.2–45
MRF141G	5.2–54
MRF148A	5.2–62
MRF150	5.2–67
MRF151	5.2–74
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MRF157	5.2–95
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MRF183	5.2–179
MRF183S, R1	5.2–179
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MRF282ZR1	5.2–238
MRF284	5.2–247
MRF284SR1	5.2–247
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MRF373S	5.2–258
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MRF947AT1	5.2–3
MRF947BT1	5.2–3
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MRF949T1	5.2–310
MRF957	5.2–15
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MRF959T1	5.2–321
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MRF9382T1	5.2–368
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MRF18060B	5.2–402
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Device Number	Page Number
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MRF18090AS	5.2–408
MRF18090B	5.2–414
MRF18090BS	5.2–414
MRF19060	5.2–420
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MRF20060R	5.2–439
MRF20060RS	5.2–439
MRF21060	5.2–446
MRF21060S	5.2–446
TPV8100B	5.2–452

The RF Line

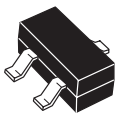
NPN Silicon Low Noise, High-Frequency Transistors

Designed for use in high gain, low noise small–signal amplifiers. This series features excellent broadband linearity and is offered in a variety of packages.

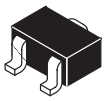
- Fully Implanted Base and Emitter Structure
- 9 Finger, 1.25 Micron Geometry with Gold Top Metal
- Gold Sintered Back Metal
- Available in tape and reel packaging options:
  T1 suffix = 3,000 units per reel
  T3 suffix = 10,000 units per reel

MMBR941
MRF947
SERIES

I_C = 50 mA
LOW NOISE
HIGH–FREQUENCY
TRANSISTORS



CASE 318–08, STYLE 6
SOT–23
LOW PROFILE
MMBR941LT1, T3, MMBR941BLT1



CASE 419–02, STYLE 3
MRF947AT1, MRF947BT1,
MRF947T1, T3

MAXIMUM RATINGS

Rating	Symbol	MMBR941LT1, T3	MRF947 Series	Unit
Collector–Emitter Voltage	V_{CEO}	10	10	Vdc
Collector–Base Voltage	V_{CBO}	20	20	Vdc
Emitter–Base Voltage	V_{EBO}	1.5	1.5	Vdc
Power Dissipation (1) T_C = 75°C Derate linearly above T_{case} = 75°C @	P_{Dmax}	0.25 3.33	0.188 2.5	Watts mW/°C
Collector Current — Continuous (2)	I_C	50	50	mA
Maximum Junction Temperature	T_{Jmax}	150	150	°C
Storage Temperature	T_{stg}	–55 to +150	–55 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	300	400	°C/W

DEVICE MARKING

MMBR941LT1 = 7Y MMBR941BLT1 = 7N MRF947T1, T3 = A MRF947BT1 = H
MRF947AT1 = G

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (3)						
Collector–Emitter Breakdown Voltage (I_C = 0.1 mA, I_B = 0)	All	$V_{(BR)CEO}$	10	12	—	Vdc
Collector–Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)	All	$V_{(BR)CBO}$	20	23	—	Vdc
Emitter Cutoff Current (V_{EB} = 1.0 V, I_C = 0)	All	I_{EBO}	—	—	0.1	μAdc
Collector Cutoff Current (V_{CB} = 10 V, I_E = 0)	All	I_{CBO}	—	—	0.1	μAdc
ON CHARACTERISTICS (3)						
DC Current Gain (V_{CE} = 6.0 V, I_C = 5.0 mA)	(MMBR941LT1) (MMBR941BLT1)	h_{FE}	50 100	— —	200 200	—
DC Current Gain (V_{CE} = 1.0 V, I_C = 500 μA)	MRF947T1, MRF947BT1	h_{FE_1}	50	—	—	—
DC Current Gain (V_{CE} = 6.0 V, I_C = 5.0 mA)	MRF947T1, T3 MRF947AT1 MRF947BT1	h_{FE_2} h_{FE_3} h_{FE_4}	50 75 100	— — —	— 150 200	—
DYNAMIC CHARACTERISTICS						
Collector–Base Capacitance (V_{CB} = 10 V, I_E = 0, f = 1.0 MHz)	All	C_{cb}	—	0.35	—	pF
Current Gain — Bandwidth Product (V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)	All	f_T	—	8.0	—	GHz

NOTE:
1. To calculate the junction temperature use $T_J = P_D \times R_{\theta JC} + T_{CASE}$. Case temperature measured on collector lead immediately adjacent to body of package.
2. I_C — Continuous (MTBF ≈ 10 years).
3. Pulse width ≤ 300 μs, duty cycle ≤ 2% pulsed.

PERFORMANCE CHARACTERISTICS

Conditions	Symbol	MMBR941LT1, T3			MRF947 Series			Unit
		Min	Typ	Max	Min	Typ	Max	
Insertion Gain	$\|S_{21}\|^2$							dB
(V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)		—	14	—	—	14	—	
(V_{CE} = 6.0 V, I_C = 15 mA, f = 2.0 GHz)		—	8.0	—	—	10.8	—	
Maximum Unilateral Gain (1)	$G_{U\ max}$							dB
(V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)		—	16	—	—	14.8	—	
(V_{CE} = 6.0 V, I_C = 15 mA, f = 2.0 GHz)		—	10	—	—	11.6	—	
Noise Figure — Minimum (Figure 9)	NF_{MIN}							dB
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)		—	1.5	—	—	1.5	—	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 2.0 GHz)		—	2.1	—	—	2.1	—	
Associated Gain at Minimum NF (Figure 9)	G_{NF}							dB
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)		—	14	—	—	14	—	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 2.0 GHz)		—	8.5	—	—	10	—	
Noise Figure — 50 ohm Source	$NF_{50\ \Omega}$	—	1.9	2.8	—	1.9	2.8	dB
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)								

NOTE:
1. Maximum Unilateral Gain is $GU_{max} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$

TYPICAL CHARACTERISTICS
MMBR941LT1, T3; MMBR941BLT1

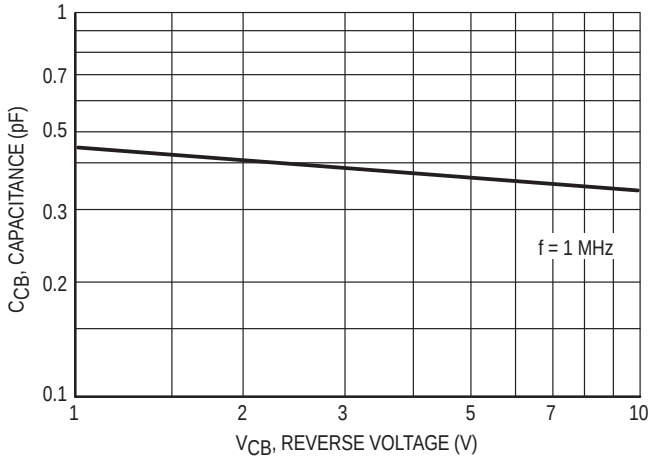


Figure 1. Collector–Base Capacitance versus Voltage

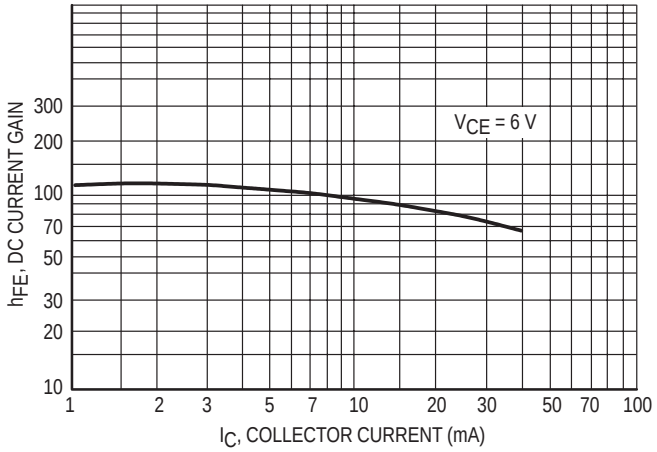


Figure 2. DC Current Gain versus Collector Current

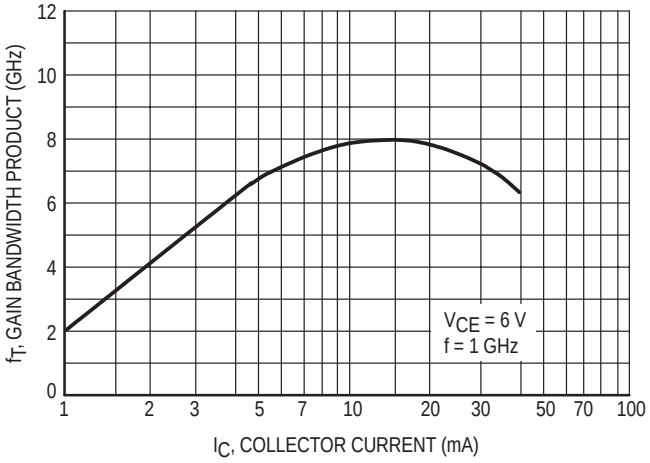


Figure 3. Gain Bandwidth Product versus Collector Current

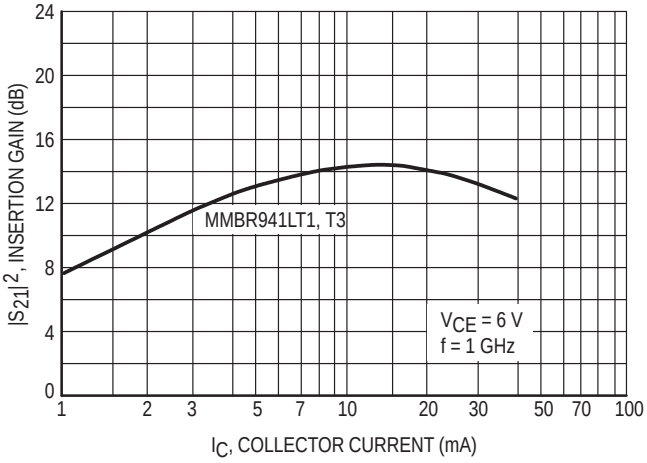


Figure 4. Insertion Gain versus Collector Current

FORWARD INSERTION GAIN AND MAXIMUM UNILATERAL GAIN versus FREQUENCY

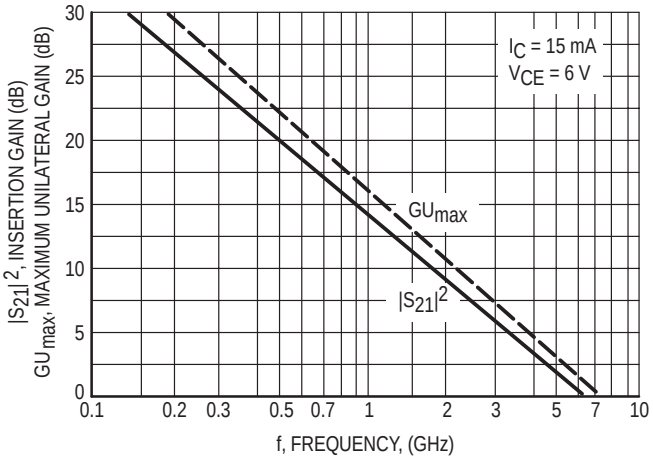


Figure 5. MMBR941LT1, T3

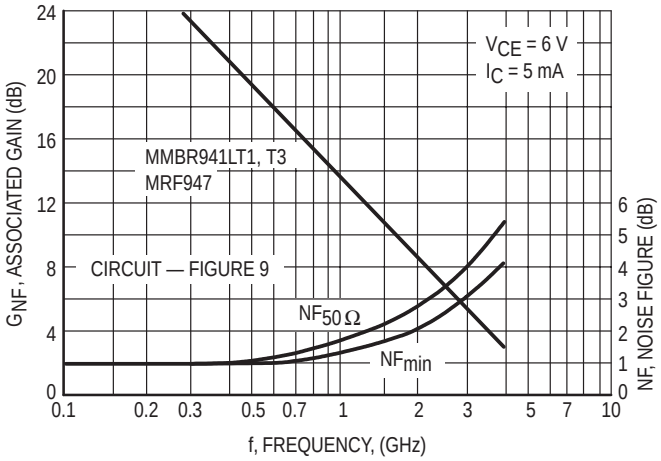


Figure 6. Noise Figure and Associated Gain versus Frequency

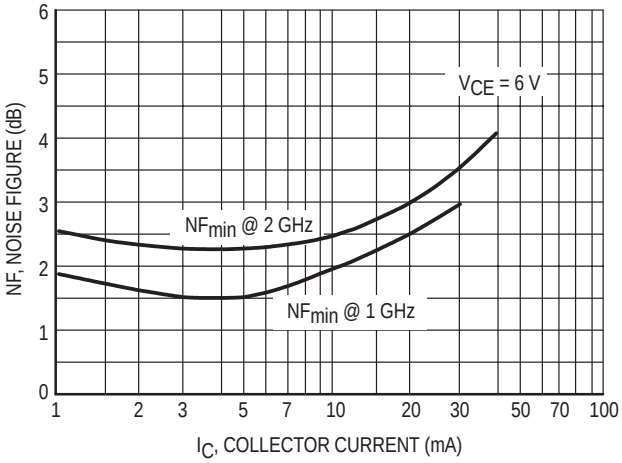


Figure 7. Minimum Noise Figure versus Collector Current

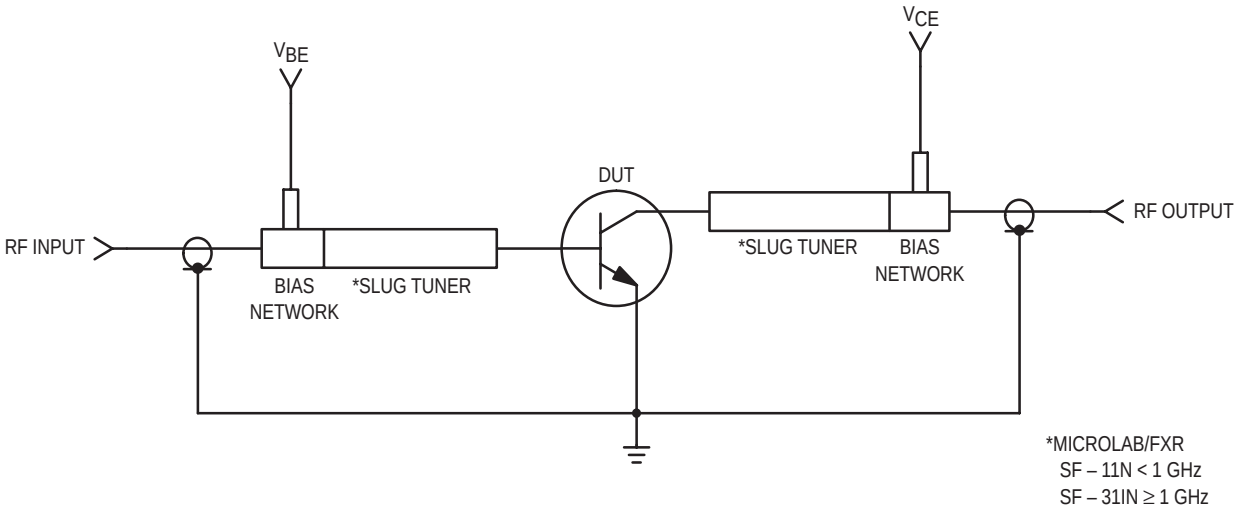


Figure 8. Functional Circuit Schematic (all devices)

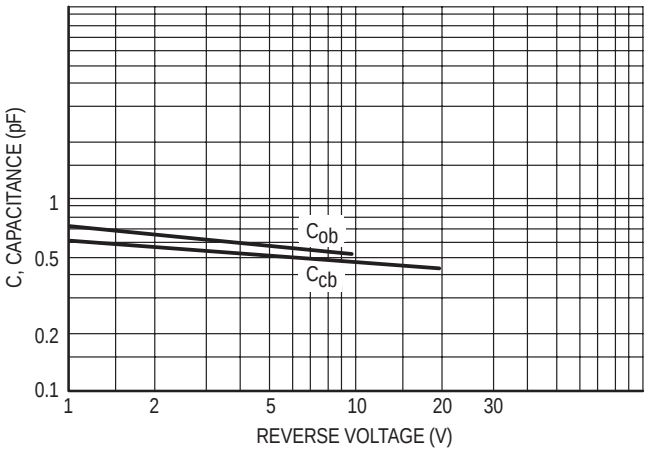


Figure 9. Capacitance versus Voltage

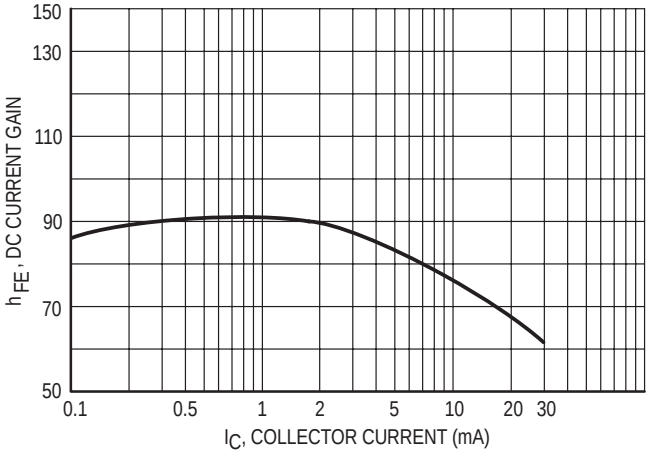


Figure 10. DC Current Gain versus Collector Current

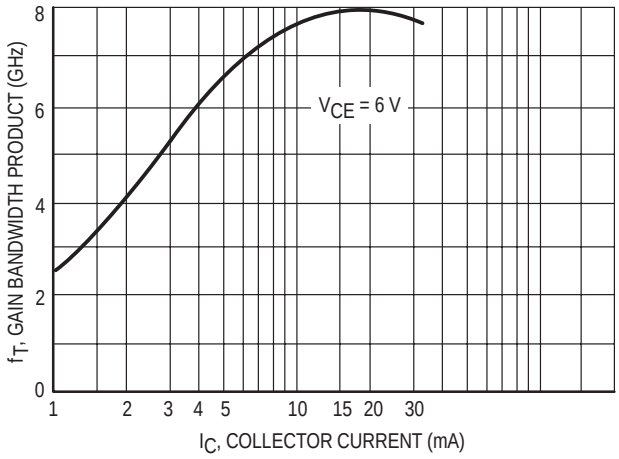


Figure 11. Gain–Bandwidth Product versus Collector Current

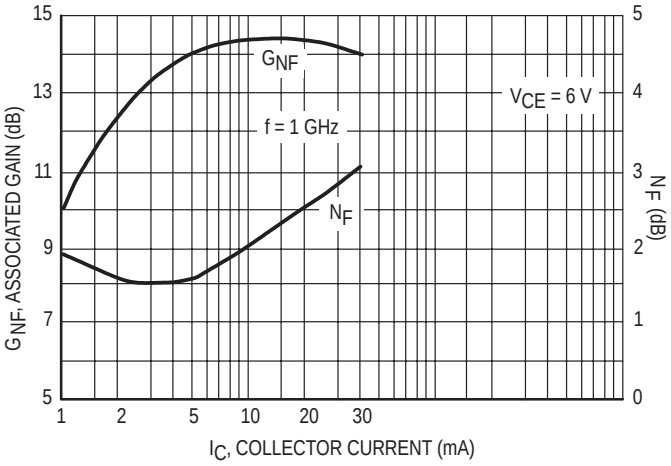


Figure 12. Associated Gain and Minimum Noise Figure versus Collector Current

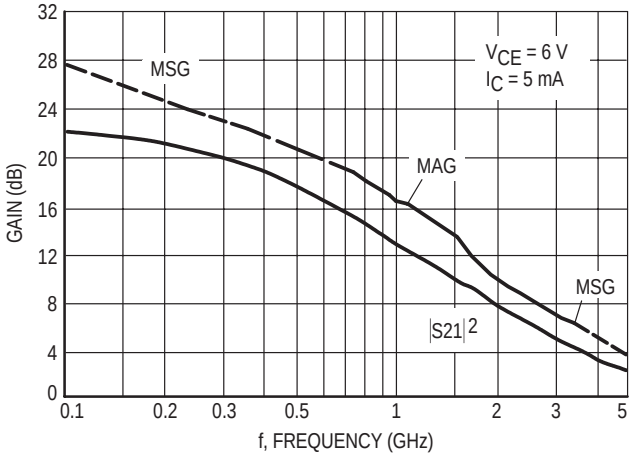


Figure 13. Forward Insertion Gain and Maximum Stable/Available Power Gain versus Frequency

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			Mag	ϕ	Mag	ϕ	Mag	ϕ	Mag	ϕ
1.0	0.5	100	0.97	−11	1.78	170	0.03	83	0.99	−4.7
		200	0.96	−22	1.74	161	0.06	76	0.99	−9.1
		500	0.90	−53	1.60	133	0.13	56	0.93	−21
		900	0.75	−89	1.37	105	0.18	37	0.83	−33
		1000	0.72	−98	1.32	100	0.18	33	0.82	−36
		1500	0.63	−132	1.07	74	0.19	20	0.75	−47
		2000	0.57	−163	0.89	55	0.16	15	0.72	−57
		3000	0.55	144	0.67	30	0.15	40	0.71	−76
	1.0	100	0.95	−13	3.37	169	0.03	81	0.99	−6.2
		200	0.93	−27	3.27	158	0.06	73	0.98	−12
		500	0.81	−62	2.85	128	0.12	52	0.86	−26
		900	0.63	−101	2.21	101	0.15	37	0.73	−38
		1000	0.60	−110	2.08	96	0.15	34	0.71	−40
		1500	0.51	−144	1.59	73	0.16	27	0.64	−49
		2000	0.46	−173	1.28	56	0.16	29	0.61	−58
		3000	0.46	138	0.95	30	0.19	44	0.60	−75
6.0	5.0	100	0.82	−25	14.6	159	0.02	77	0.94	−13
		200	0.75	−47	12.6	142	0.04	68	0.85	−22
		400	0.55	−79	9.2	120	0.05	61	0.69	−31
		600	0.42	−98	6.9	106	0.07	60	0.60	−32
		800	0.33	−114	5.3	97	0.08	61	0.56	−33
		1000	0.28	−129	4.5	90	0.09	62	0.52	−33
		1500	0.25	−155	3.1	77	0.13	67	0.51	−37
		2000	0.16	176	2.4	66	0.16	68	0.51	−36
		2500	0.21	151	2.0	57	0.20	69	0.48	−40
		3000	0.18	122	1.7	50	0.23	68	0.48	−44
		3500	0.30	108	1.5	42	0.27	66	0.45	−46
		4000	0.29	91	1.4	37	0.32	64	0.42	−53
	10	100	0.67	−37	23.5	149	0.02	74	0.88	−18
		200	0.54	−64	18.1	129	0.03	68	0.73	−28
		400	0.37	−96	11.3	108	0.05	67	0.56	−31
		600	0.26	−114	8.0	98	0.06	67	0.50	−30
		800	0.21	−130	6.0	91	0.08	70	0.47	−30
		1000	0.18	−147	5.1	85	0.09	70	0.45	−30
		1500	0.18	−167	3.4	74	0.13	72	0.46	−34
		2000	0.11	159	2.6	64	0.17	71	0.46	−34
		2500	0.17	140	2.2	56	0.21	69	0.44	−38
		3000	0.15	107	1.8	59	0.25	67	0.45	−41
		3500	0.27	100	1.7	42	0.28	65	0.42	−42
		4000	0.26	85	1.5	37	0.33	61	0.39	−49
	15	100	0.56	−46	28.6	143	0.02	73	0.83	−22
		200	0.43	−75	20.2	122	0.03	67	0.65	−30
		400	0.29	−107	11.8	104	0.04	70	0.50	−30
		600	0.22	−125	8.2	95	0.06	74	0.46	−28
		800	0.18	−141	6.2	88	0.08	74	0.45	−27
		1000	0.16	−158	5.1	83	0.09	74	0.43	−28
		1500	0.17	−174	3.4	72	0.13	73	0.44	−32
		2000	0.11	150	2.6	63	0.17	72	0.45	−33
		2500	0.17	138	2.2	55	0.21	70	0.43	−37
		3000	0.15	102	1.9	49	0.25	67	0.44	−39
		3500	0.28	98	1.7	42	0.29	65	0.40	−41
		4000	0.25	82	1.5	37	0.32	61	0.38	−47

Table 1. MMBR941LT1, T3 Common Emitter S–Parameters

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			Mag	ϕ	Mag	ϕ	Mag	ϕ	Mag	ϕ
6.0	20	100	0.49	−52	31.5	139	0.01	70	0.79	−23
		200	0.36	−84	21.1	118	0.02	69	0.60	−29
		400	0.25	−115	12.1	101	0.04	73	0.48	−29
		600	0.20	−134	8.3	93	0.06	74	0.45	−26
		800	0.16	−150	6.2	87	0.07	75	0.44	−26
		1000	0.15	−166	5.1	82	0.09	75	0.42	−26
		1500	0.16	−176	3.5	75	0.14	74	0.44	−31
		2000	0.12	144	2.6	63	0.17	73	0.45	−32
		2500	0.17	133	2.2	55	0.22	70	0.43	−36
		3000	0.16	101	1.9	49	0.25	68	0.44	−39
		3500	0.28	98	1.6	41	0.29	65	0.41	−40
		4000	0.26	82	1.5	36	0.33	61	0.39	−47
	30	100	0.41	−65	34.3	134	0.01	70	0.74	−25
		200	0.30	−99	21.6	113	0.02	70	0.56	−28
		400	0.23	−131	11.9	98	0.04	76	0.47	−25
		600	0.20	−147	8.1	91	0.06	76	0.45	−24
		800	0.18	−163	6.1	84	0.07	78	0.44	−23
		1000	0.17	−177	5.0	80	0.09	78	0.43	−24
		1500	0.18	174	3.4	70	0.13	76	0.45	−30
		2000	0.14	141	2.5	61	0.17	74	0.47	−31
		2500	0.20	131	2.1	54	0.21	71	0.45	−36
		3000	0.18	104	1.8	47	0.25	69	0.46	−39
		3500	0.31	100	1.6	40	0.29	65	0.42	−42
		4000	0.29	84	1.5	35	0.33	62	0.40	−48

Table 1. MMBR941LT1, T3 Common Emitter S–Parameters (continued)

V_{CE} (Vdc)	I_C (mA)	f (MHz)	NF_{min} (dB)	Γ_o (MAG, ANGLE)	r_N
6	5	1000 1500	1.5 1.75	0.33 77 0.26 141	0.28 0.3

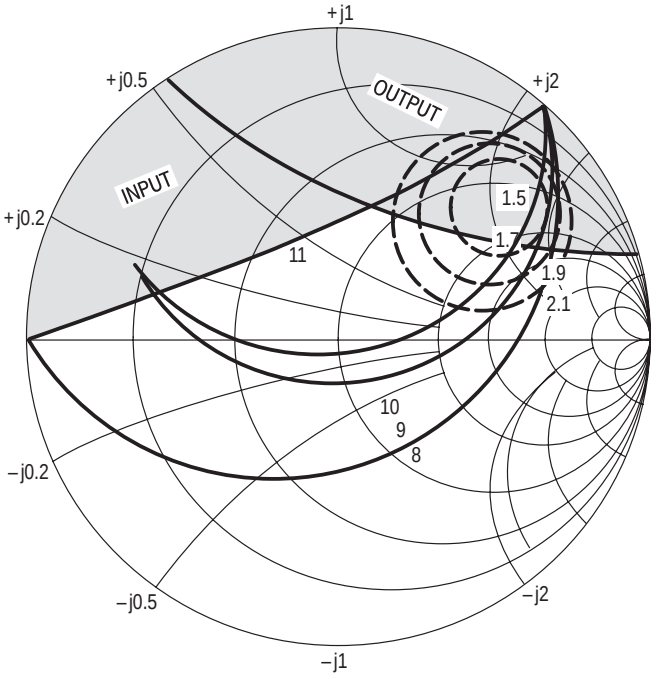
Table 2. MRF947 Series Typical Noise Parameters

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			Mag	ϕ	Mag	ϕ	Mag	ϕ	Mag	ϕ
1.0	0.5	100	0.966	−11	1.776	170	0.031	83	0.998	−5
		200	0.956	−23	1.735	161	0.061	75	0.991	−9
		500	0.892	−55	1.587	132	0.135	55	0.923	−21
		900	0.749	−91	1.355	104	0.185	35	0.827	−34
		1000	0.720	−100	1.300	98	0.190	32	0.808	−36
		1500	0.637	−134	1.057	73	0.196	18	0.743	−47
		2000	0.587	−164	0.883	53	0.176	12	0.708	−58
		3000	0.572	149	0.672	27	0.149	33	0.680	−82
	1.0	100	0.941	−14	3.391	168	0.031	81	0.991	−6
		200	0.921	−28	3.285	158	0.060	73	0.974	−12
		500	0.806	−65	2.844	128	0.123	51	0.852	−27
		900	0.638	−104	2.196	101	0.158	35	0.717	−39
		1500	0.533	−146	1.580	72	0.168	25	0.619	−50
		2000	0.495	−174	1.281	55	0.164	25	0.581	−60
		3000	0.494	144	0.956	29	0.187	39	0.554	−81
2.0	0.5	100	0.979	−9	1.827	173	0.030	85	0.996	−4
		200	0.960	−18	1.909	165	0.060	80	0.991	−9
		500	0.920	−43	1.652	144	0.132	65	0.940	−19
		1000	0.749	−77	1.451	116	0.196	47	0.842	−32
		1500	0.674	−105	1.190	94	0.214	36	0.774	−39
		2000	0.548	−128	1.077	79	0.189	33	0.692	−43
		3000	0.480	−178	0.808	60	0.153	55	0.625	−52
	2.0	100	0.907	−16	6.640	167	0.029	81	0.977	−9
		200	0.846	−32	6.419	156	0.054	73	0.944	−17
		500	0.711	−68	4.874	128	0.104	57	0.770	−32
		1000	0.495	−106	3.178	103	0.138	50	0.603	−41
		1500	0.405	−131	2.358	86	0.157	52	0.542	−45
		2000	0.314	−155	1.910	75	0.173	58	0.490	−44
		3000	0.296	158	1.394	59	0.228	68	0.454	−47
	5.0	100	0.780	−28	14.100	159	0.027	78	0.932	−15
		200	0.676	−51	12.219	142	0.046	67	0.831	−27
		500	0.470	−95	7.373	113	0.078	59	0.568	−40
		1000	0.327	−132	4.148	92	0.114	62	0.436	−43
		1500	0.271	−153	2.921	81	0.151	66	0.413	−44
		2000	0.218	−177	2.295	72	0.188	69	0.394	−41
		3000	0.237	138	1.661	58	0.265	70	0.372	−43

Table 3. MRF947 Series Common Emitter S–Parameters

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			Mag	ϕ	Mag	ϕ	Mag	ϕ	Mag	ϕ
2.0	10	100	0.608	−43	21.812	149	0.022	72	0.859	−23
		200	0.488	−73	16.618	129	0.038	65	0.689	−35
		500	0.330	−119	8.427	103	0.065	66	0.438	−41
		1000	0.262	−152	4.484	87	0.109	71	0.354	−40
		1500	0.227	−169	3.114	77	0.155	73	0.358	−42
		2000	0.197	166	2.423	69	0.198	73	0.355	−38
		3000	0.233	128	1.755	57	0.281	71	0.338	−40
	30	100	0.353	−100	25.543	131	0.018	70	0.653	−29
		200	0.353	−135	15.823	112	0.026	68	0.484	−34
		500	0.346	−163	6.979	93	0.054	76	0.367	−29
		1000	0.337	177	3.637	80	0.103	79	0.351	−30
		1500	0.324	166	2.518	71	0.150	79	0.372	−36
		2000	0.319	148	1.975	63	0.197	78	0.378	−35
		3000	0.374	122	1.441	51	0.290	75	0.363	−42
6.0	0.5	100	0.978	−9	1.791	173	0.024	86	0.995	−4
		200	0.964	−17	1.889	166	0.049	80	0.994	−7
		500	0.932	−40	1.643	146	0.110	67	0.953	−16
		1000	0.765	−73	1.473	121	0.165	50	0.869	−28
		1500	0.688	−100	1.206	98	0.184	39	0.812	−35
		2000	0.554	−123	1.099	84	0.162	38	0.735	−38
		3000	0.463	−174	0.823	64	0.136	63	0.671	−46
	2.0	100	0.918	−15	6.614	168	0.023	84	0.983	−7
		200	0.862	−29	6.456	157	0.045	75	0.956	−14
		500	0.729	−62	5.010	131	0.089	60	0.809	−27
		1000	0.504	−99	3.344	106	0.121	53	0.654	−35
		1500	0.397	−123	2.485	90	0.137	55	0.599	−38
		2000	0.295	−146	2.013	78	0.152	62	0.553	−37
		3000	0.257	162	1.452	62	0.202	73	0.523	−40
	5.0	100	0.806	−24	14.025	161	0.022	78	0.947	−13
		200	0.704	−45	12.425	144	0.040	70	0.861	−23
		500	0.487	−85	7.751	116	0.068	62	0.627	−33
		1000	0.316	−120	4.399	95	0.101	65	0.505	−35
		1500	0.245	−141	3.112	83	0.134	69	0.488	−36
		2000	0.177	−166	2.447	74	0.167	72	0.473	−33
		3000	0.185	140	1.743	61	0.237	74	0.457	−36
	10	100	0.657	−37	22.098	151	0.019	75	0.888	−18
		200	0.526	−64	17.304	132	0.033	68	0.741	−29
		500	0.328	−105	9.028	106	0.056	67	0.509	−33
		1000	0.228	−138	4.844	89	0.096	73	0.438	−31
		1500	0.184	−156	3.359	80	0.138	75	0.440	−34
		2000	0.140	175	2.591	72	0.175	76	0.441	−31
		3000	0.172	126	1.852	60	0.249	75	0.430	−33
	20	100	0.492	−53	28.934	142	0.017	72	0.808	−23
		200	0.372	−85	19.971	121	0.028	70	0.630	−31
		500	0.249	−127	9.335	100	0.053	74	0.454	−28
		1000	0.201	−156	4.878	86	0.094	78	0.418	−27
		1500	0.174	−171	3.358	77	0.138	79	0.432	−30
		2000	0.149	161	2.580	70	0.177	78	0.444	−28
		3000	0.193	121	1.852	58	0.253	76	0.435	−32

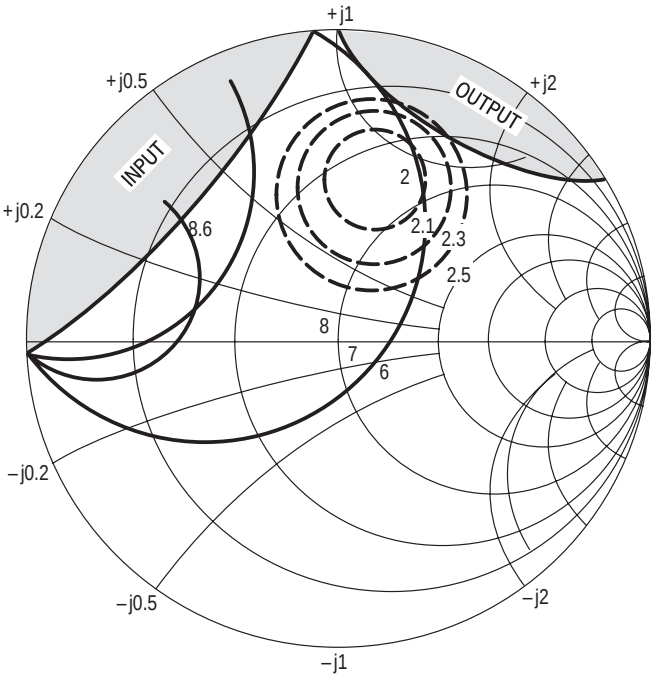
Table 3. MRF947 Series Common Emitter S–Parameters (continued)



V_{CE} = 1.0 V
I_C = 0.5 mA
— AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
0.5	1.54	0.71 39°	38	0.28

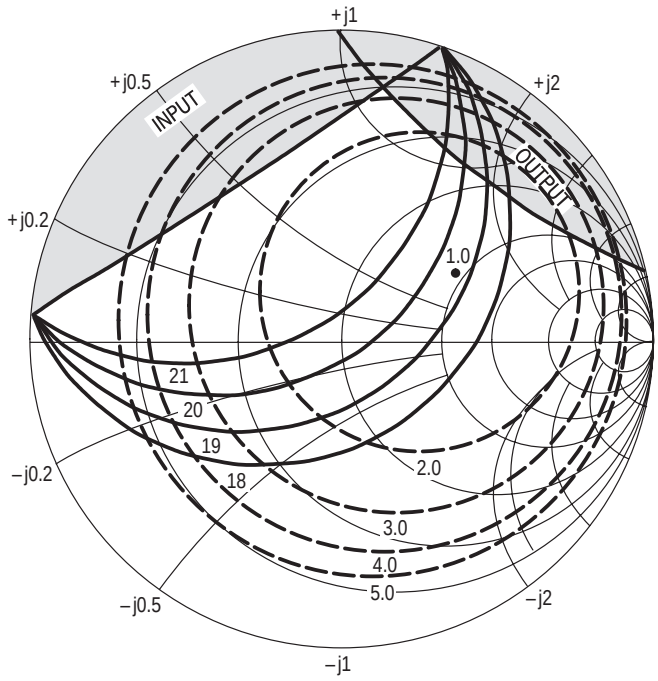
Figure 14. MMBR941LT1, T3 Constant Gain and Noise Figure Contours (f = 1.0 GHz)



V_{CE} = 1.0 V
I_C = 0.5 mA
— AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
1.0	1.95	0.55 76°	28	0.51

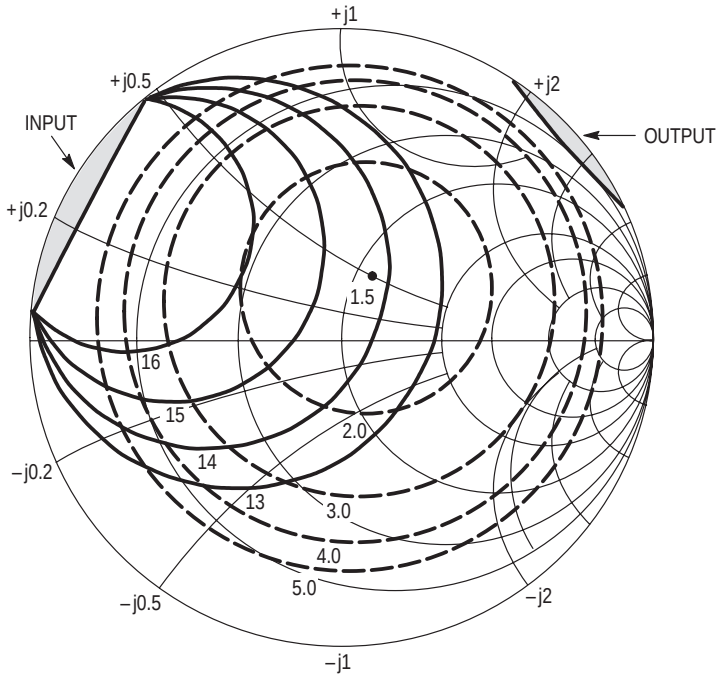
Figure 15. MMBR941LT1, T3 Constant Gain and Noise Figure Contours (f = 0.5 GHz)



V_{CE} = 6.0 V
I_C = 5.0 mA
— AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
0.5	1.0	0.43 30°	18	0.58

Figure 16. MMBR941LT1, T3 Constant Gain and Noise Figure Contours (f = 0.5 GHz)



V_{CE} = 6.0 V
I_C = 5.0 mA
— AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
1.0	1.5	0.22 64°	13	0.93

Figure 17. MMBR941LT1, T3 Constant Gain and Noise Figure Contours (f = 1.0 GHz)

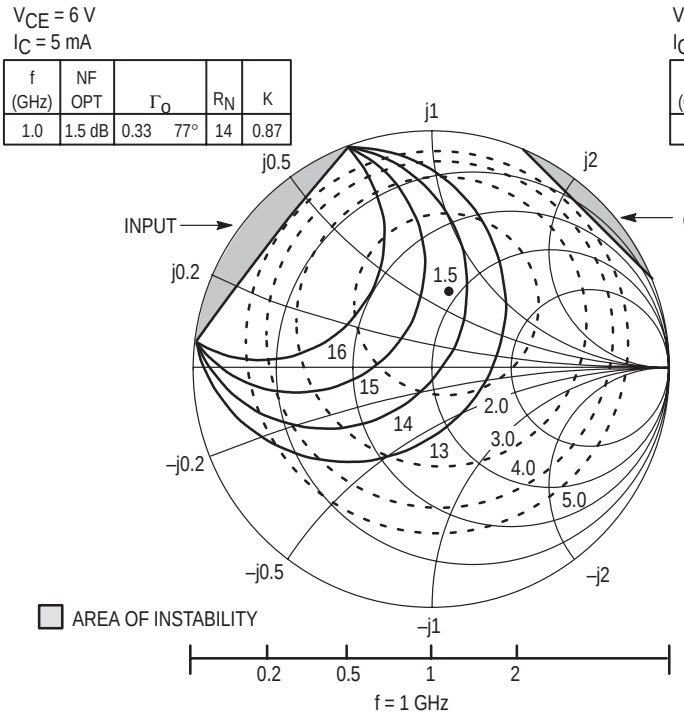


Figure 18. MRF947 Series Constant Gain and Noise Figure Contours

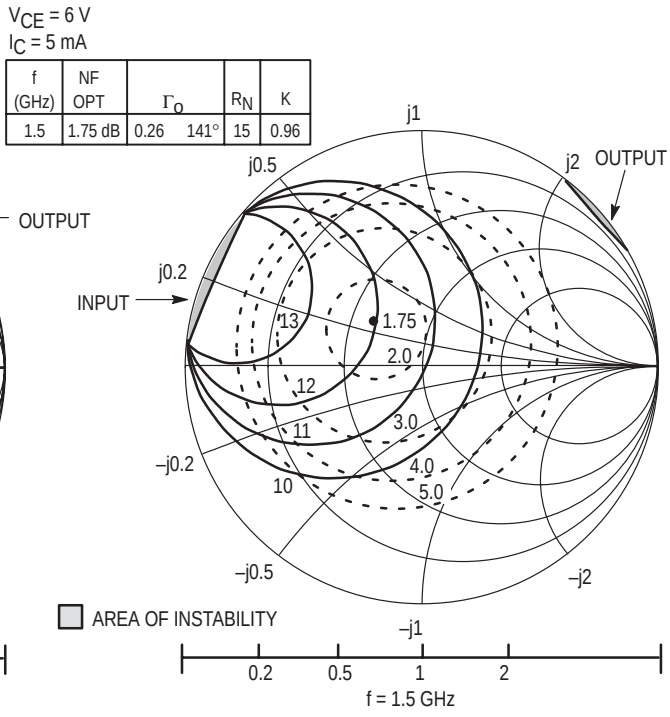


Figure 19. MRF947 Series Constant Gain and Noise Figure Contours

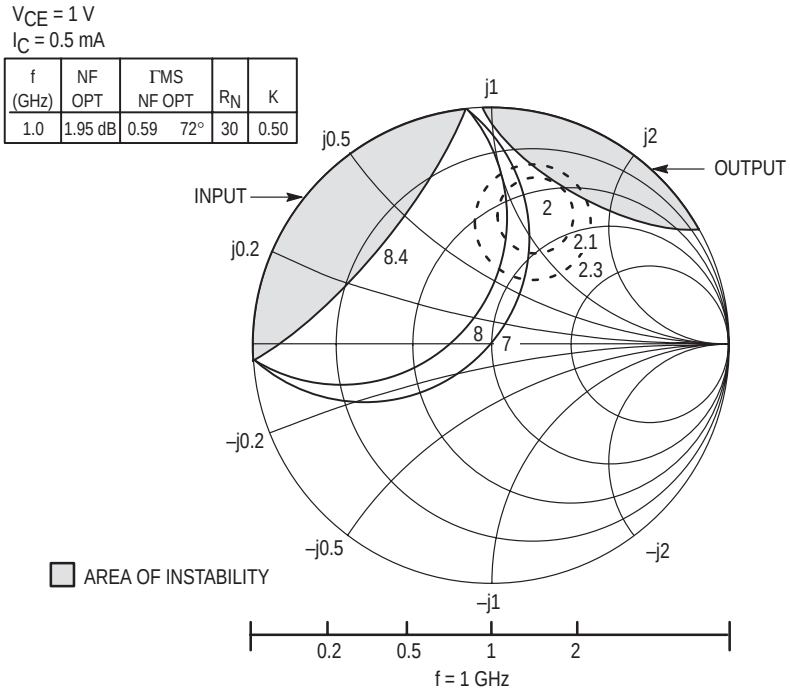


Figure 20. MRF947 Series Constant Gain and Noise Figure Contours

The RF Line

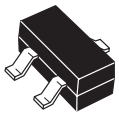
NPN Silicon Low Noise, High-Frequency Transistors

Designed for use in high gain, low noise small–signal amplifiers. This series features excellent broadband linearity and is offered in a variety of packages.

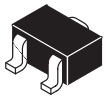
- Fully Implanted Base and Emitter Structure
- 18 Finger, 1.25 Micron Geometry with Gold Top Metal
- Gold Sintered Back Metal
- Available in tape and reel packaging options:
  T1 suffix = 3,000 units per reel

MMBR951 MRF957 SERIES

I_C = 100 mA
LOW NOISE
HIGH–FREQUENCY
TRANSISTORS



CASE 318–08, STYLE 6
SOT–23
LOW PROFILE
MMBR951LT1



CASE 419–02, STYLE 3
MRF957T1

MAXIMUM RATINGS0

Rating	Symbol	MMBR951LT1	MRF957T1	Unit
Collector–Emitter Voltage	V_{CEO}	10	10	Vdc
Collector–Base Voltage	V_{CBO}	20	20	Vdc
Emitter–Base Voltage	V_{EBO}	1.5	15	Vdc
Power Dissipation (1) T_C = 75°C Derate linearly above T_{case} = 75°C @	$P_{D(max)}$	0.322 4.29	0.227 3.03	Watts mW/°C
Collector Current — Continuous (2)	I_C	100	100	mA
Maximum Junction Temperature	T_{Jmax}	150	150	°C
Storage Temperature	T_{stg}	–55 to +150	–55 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	233	330	°C/W

DEVICE MARKING

MMBR951LT1 = 7Z MRF957T1 = B

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (3)					
Collector–Emitter Breakdown Voltage (I_C = 0.1 mA, I_B = 0)	$V_{(BR)CEO}$	10	13	—	Vdc
Collector–Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)	$V_{(BR)CBO}$	20	25	—	Vdc
Emitter Cutoff Current (V_{EB} = 1.0 V, I_C = 0)	I_{EBO}	—	—	0.1	μAdc
Collector Cutoff Current (V_{CB} = 10 V, I_E = 0)	I_{CBO}	—	—	0.1	μAdc
ON CHARACTERISTICS (3)					
DC Current Gain (V_{CE} = 6.0 V, I_C = 5.0 mA)	h_{FE}	50	—	200	—
DYNAMIC CHARACTERISTICS					
Collector–Base Capacitance (V_{CB} = 10 V, I_E = 0, f = 1.0 MHz)	C_{cb}	—	0.45	1.0	pF
Current Gain — Bandwidth Product (V_{CE} = 6.0 V, I_C = 30 mA, f = 1.0 GHz) MMBR951LT1 MRF957T1	f_T	— —	8.0 9.0	— —	GHz

NOTES:
1. To calculate the junction temperature use $T_J = (P_D \times R_{\theta JA}) + T_{CASE}$. Case temperature measured on collector lead immediately adjacent to body of package.
2. I_C — Continuous (MTBF ≈ 10 years).
3. Pulse width ≤ 300 μs, duty cycle ≤ 2% pulsed.

PERFORMANCE CHARACTERISTICS

Conditions	Symbol	MMBR951LT1			MRF957T1			Unit
		Min	Typ	Max	Min	Typ	Max	
Insertion Gain	$\|S_{21}\|^2$							dB
(V_{CE} = 6.0 V, I_C = 30 mA, f = 1.0 GHz)		—	12.5	—	—	13.3	—	
(V_{CE} = 6.0 V, I_C = 30 mA, f = 2.0 GHz)		—	7.0	—	—	—	—	
(V_{CE} = 5.0 V, I_C = 30 mA, f = 1.5 GHz)		—	—	—	—	10.1	—	
Maximum Unilateral Gain (1)	$G_{U\ max}$							dB
(V_{CE} = 8.0 V, I_C = 30 mA, f = 1.0 GHz)		—	14	—	—	14	—	
(V_{CE} = 8.0 V, I_C = 30 mA, f = 2.0 GHz)		—	8.0	—	—	—	—	
(V_{CE} = 5.0 V, I_C = 30 mA, f = 1.5 GHz)		—	—	—	—	10.8	—	
Noise Figure — Minimum (Figure 9)	NF_{MIN}							dB
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)		—	1.3	—	—	1.5	—	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 2.0 GHz)		—	2.1	—	—	—	—	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.5 GHz)		—	—	—	—	2.0	—	
Associated Gain at Minimum NF (Figure 9)	G_{NF}							dB
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)		—	13	—	—	11.8	—	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 2.0 GHz)		—	7.5	—	—	—	—	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.5 GHz)		—	—	—	—	9.0	—	
Noise Figure — 50 ohm Source	$NF_{50\ \Omega}$	—	1.9	2.8	—	1.9	2.8	dB
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)								

NOTE:

1. Maximum Unilateral Gain is $GU_{max} = \dfrac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$

TYPICAL CHARACTERISTICS
MMBR951LT1

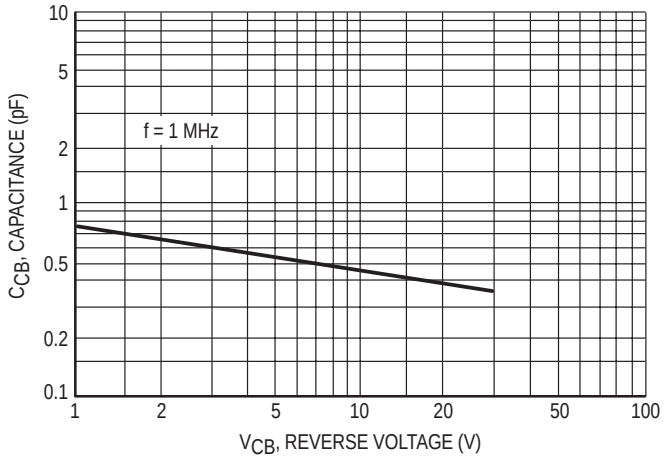


Figure 1. Collector–Base Capacitance versus Voltage

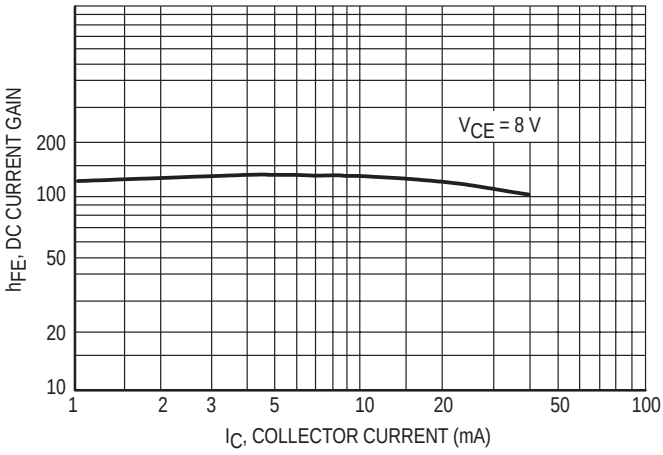


Figure 2. DC Current Gain versus Collector Current

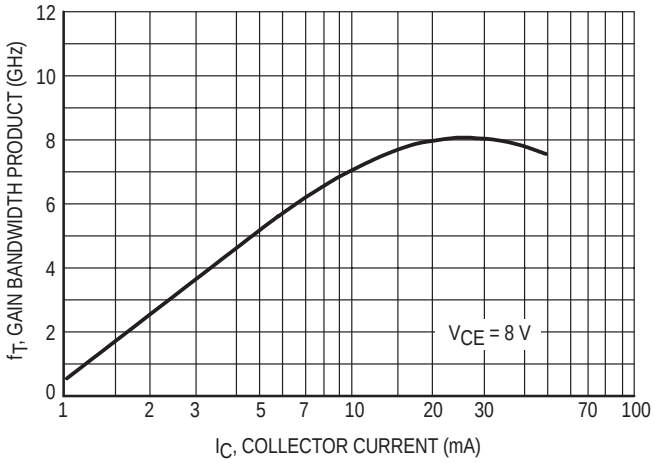


Figure 3. Gain Bandwidth Product versus Collector Current

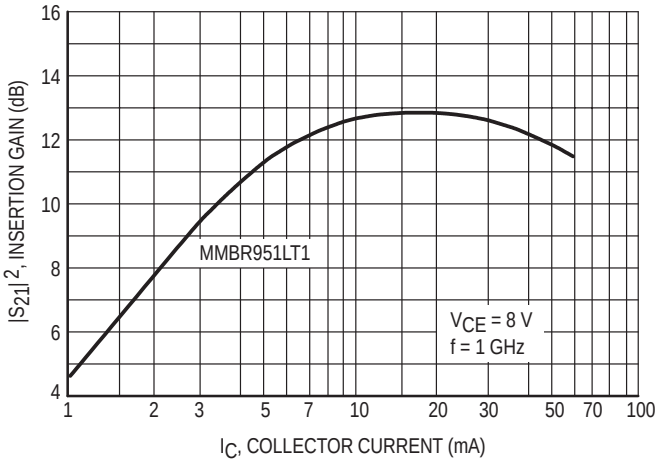


Figure 4. Insertion Gain versus Collector Current

TYPICAL FORWARD INSERTION GAIN AND MAXIMUM UNILATERAL GAIN versus FREQUENCY

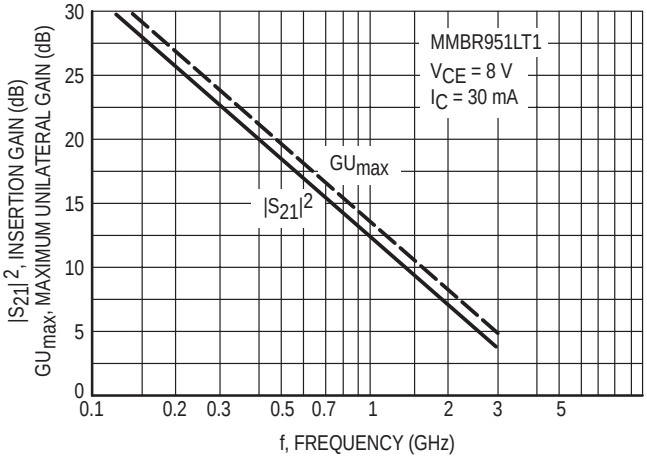


Figure 6. MMBR951LT1

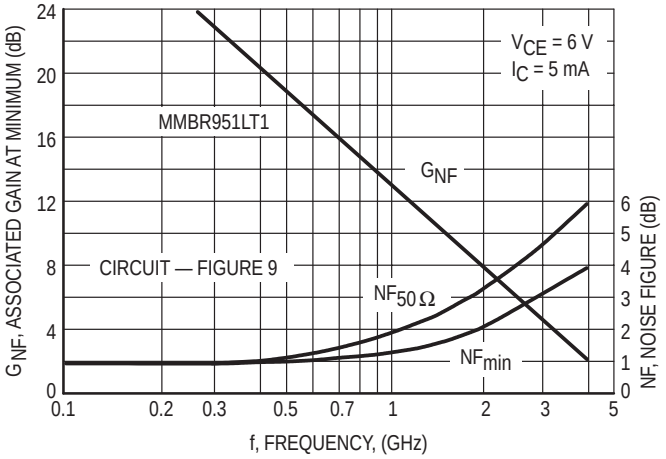


Figure 5. Typical Noise Figure and Associated Gain versus Frequency

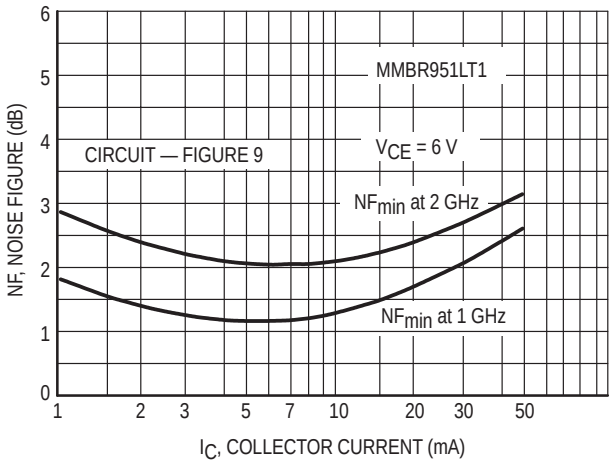


Figure 7. Typical Noise Figure versus Collector Current

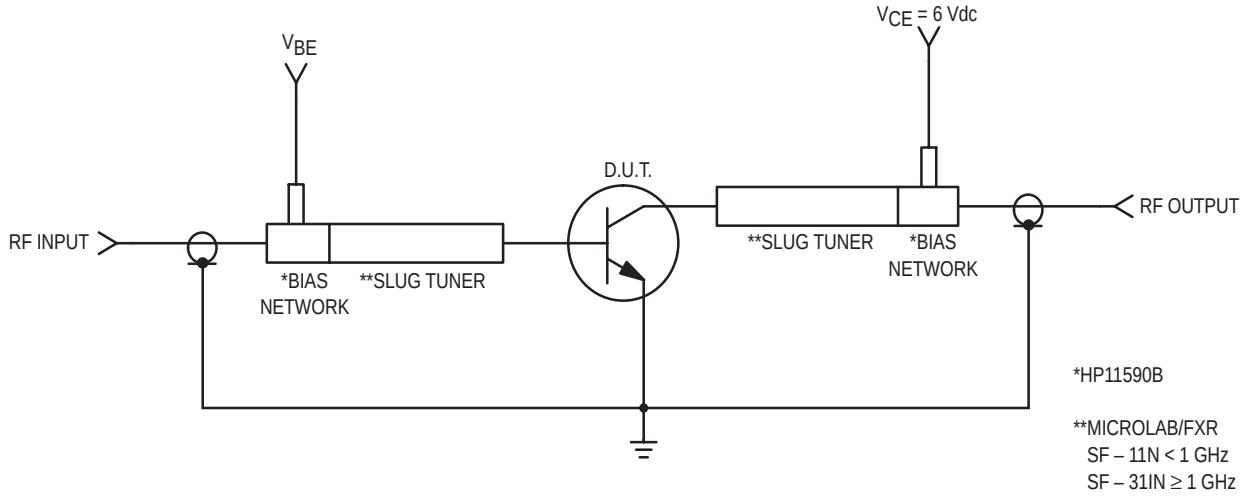
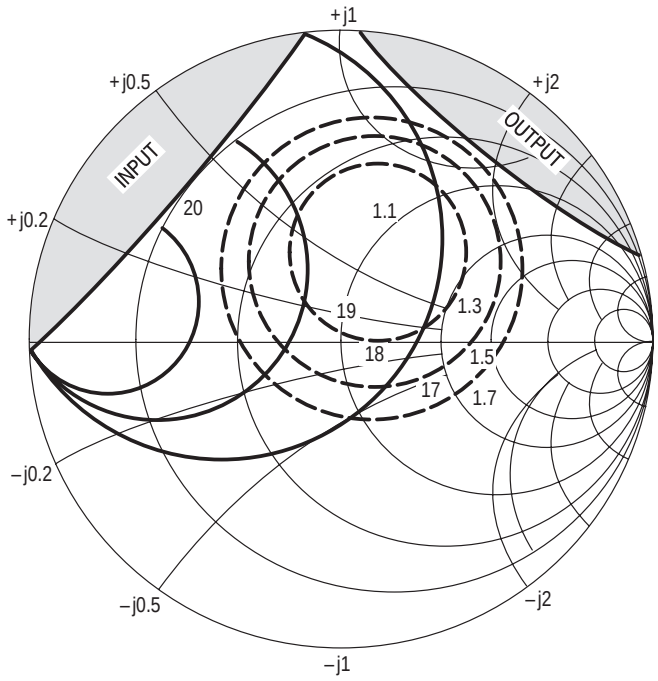


Figure 8. Functional Circuit Schematic (All Devices)

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
6.0	5.0	100	0.82	−36.6	14.0	153	0.04	44.7	0.88	−18.2
		500	0.50	−119	6.6	104	0.07	48.2	0.52	−40
		1000	0.39	−162	3.5	81	0.11	55	0.43	−43
		2000	0.32	150	1.9	57	0.21	66	0.42	−50
		3000	0.36	110	1.4	40	0.31	66	0.40	−67
	10	100	0.66	−54	22.6	142	0.03	60	0.78	−29
		500	0.38	−138	7.8	96	0.07	55	0.40	−42
		1000	0.32	−176	4.0	78	0.13	71	0.34	−47
		2000	0.26	142	2.2	57	0.22	70	0.36	−46
		3000	0.31	105	1.6	41	0.32	64	0.33	−62
	20	100	0.49	−76	30	131	0.01	85	0.67	−37
		500	0.32	−153	8.3	92	0.08	76	0.34	−39
		1000	0.29	175	4.3	77	0.11	67	0.29	−44
		2000	0.24	137	2.3	57	0.24	71	0.32	−48
		3000	0.28	102	1.6	42	0.34	63	0.29	−60
	30	100	0.40	−94	33	125	0.03	87	0.58	−42
		500	0.30	−162	8.4	90	0.07	84	0.31	−35
		1000	0.29	170	4.3	76	0.12	80	0.27	−39
		2000	0.24	134	2.3	56	0.23	71	0.33	−48
		3000	0.30	101	1.6	41	0.35	66	0.30	−60
	60	100	0.38	−126	31	116	0.03	74	0.49	−37
		500	0.37	−176	7.3	77.6	0.05	84	0.34	−26
		1000	0.36	163	3.7	73.4	0.12	84	0.34	−37
		2000	0.33	130	2.0	52	0.22	78	0.37	−48
		3000	0.38	98	1.4	37	0.34	69	0.34	−62
8.0	5.0	100	0.83	−35	13.9	154	0.04	92	0.90	−19
		500	0.51	−117	6.7	104	0.08	51	0.55	−38
		1000	0.38	−160	3.6	82	0.10	72	0.44	−42
		2000	0.31	151	1.9	58	0.20	73	0.46	−47
		3000	0.35	110	1.4	41	0.32	71	0.43	−63
	10	100	0.67	−52	23	143	0.02	96	0.81	−28
		500	0.37	−135	7.9	97	0.07	64	0.43	−38
		1000	0.30	−173	4.1	80	0.11	78	0.37	−41
		2000	0.25	143	2.2	57	0.21	74	0.38	−47
		3000	0.30	105	1.6	42	0.31	67	0.34	−60
	20	100	0.51	−72	30	131	0.02	68	0.68	−35
		500	0.31	−150	8.5	92	0.07	75	0.36	−36
		1000	0.28	177	4.3	77	0.13	76	0.32	−39
		2000	0.23	138	2.3	57	0.22	72	0.35	−45
		3000	0.27	103	1.6	42	0.31	64	0.31	−58
	30	100	0.42	−87	33	125	0.02	71	0.61	−38
		500	0.31	−159	8.6	90	0.07	71	0.33	−33
		1000	0.27	172	4.4	76	0.11	74	0.32	−39
		2000	0.23	135	2.3	57	0.22	73	0.34	−42
		3000	0.28	102	1.6	41	0.31	65	0.33	−55
	60	100	0.39	−119	32	117	0.02	31	0.52	−31
		500	0.36	−174	7.4	87	0.06	84	0.37	−25
		1000	0.35	164	3.8	74	0.11	78	0.35	−33
		2000	0.32	131	2.0	53	0.22	81	0.42	−41
		3000	0.37	100	1.4	38	0.33	70	0.40	−62

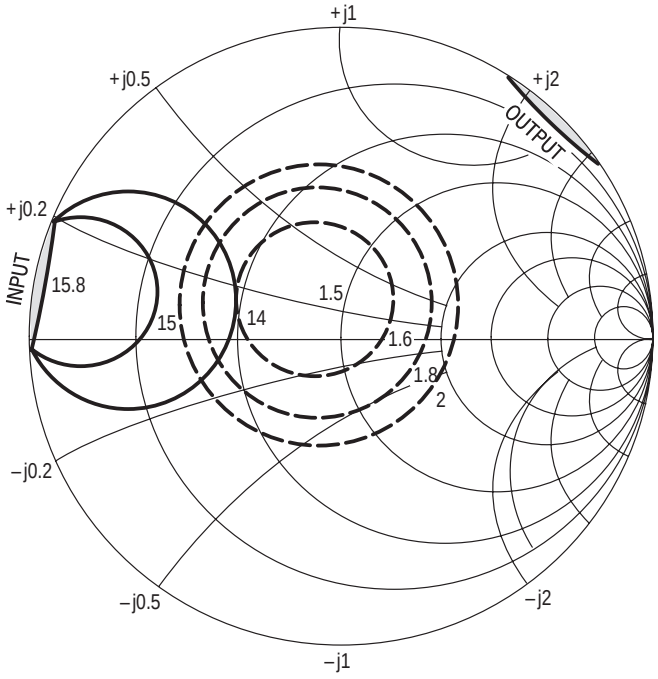
Table 1. MMBR951LT1 Common Emitter S–Parameters



V_{CE} = 6.0 V
I_C = 5.0 mA
— AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	Rn	K
0.5	1.13	0.35 68°	9	0.68

Figure 9. MMBR951LT1 Constant Gain and Noise Figure Contours (f = 0.5 GHz)



V_{CE} = 6.0 V
I_C = 5.0 mA
— AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	Rn	K
1.0	1.45	0.16 124°	8	0.97

Figure 10. MMBR951LT1 Constant Gain and Noise Figure Contours (f = 1.0 GHz)

V_{CE} (Vdc)	I_C (mA)	f (MHz)	NF_{min} (dB)	Γ_o (MAG, ANG)	r_N (ohms)
6.0	5.0	1000 1500	1.7 2.0	0.27 97 0.21 54	0.2 0.28

Table 2. MRF957T1 Typical Noise Parameters

TYPICAL CHARACTERISTICS
MRF957T1

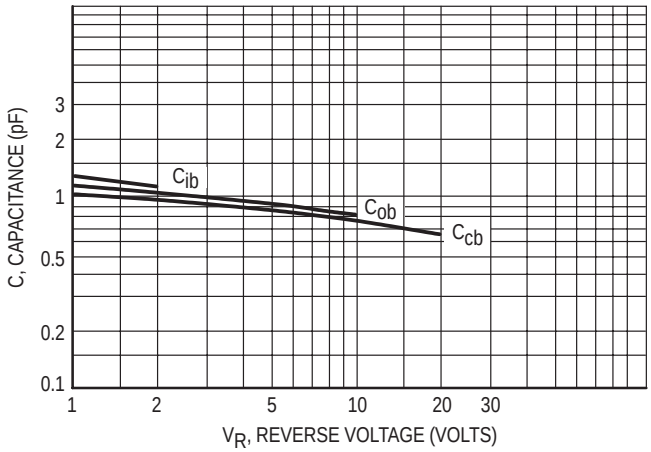


Figure 11. Capacitance versus Voltage

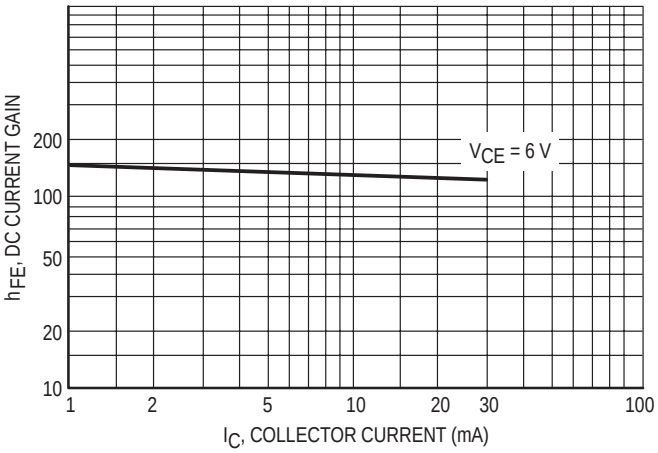


Figure 12. DC Current Gain versus Collector Current

TYPICAL CHARACTERISTICS
MRF957T1

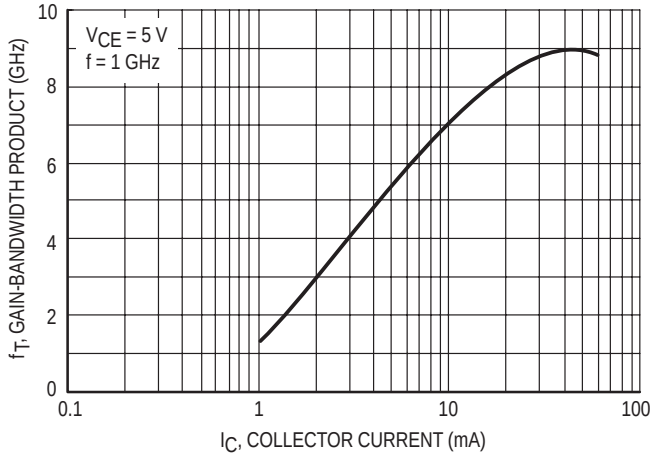


Figure 13. Gain–Bandwidth Product versus Collector Current

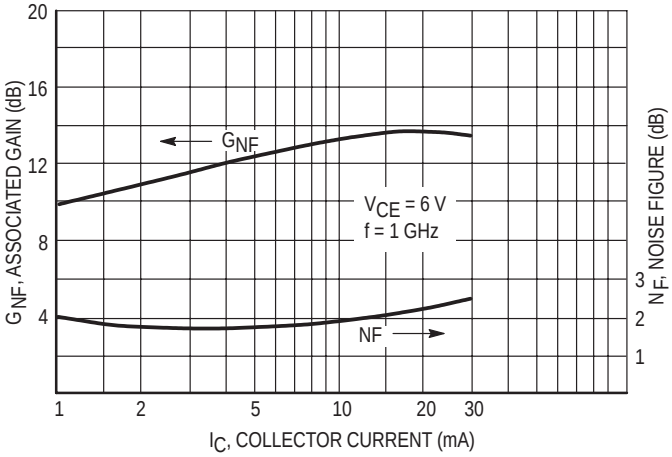


Figure 14. Associated Gain versus Collector Current

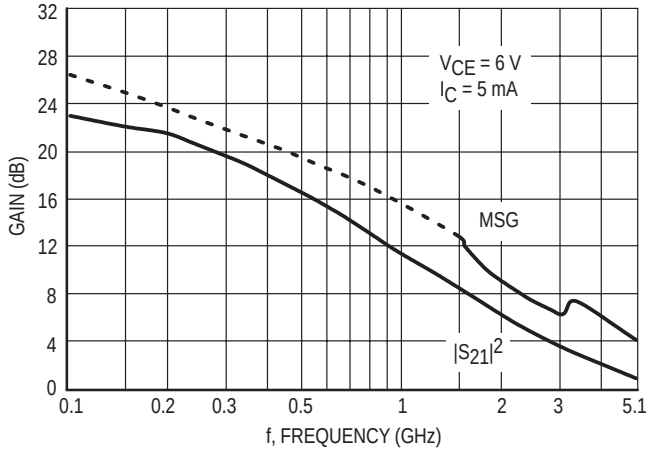


Figure 15. Insertion Gain and Maximum Stable Power Gain versus Frequency

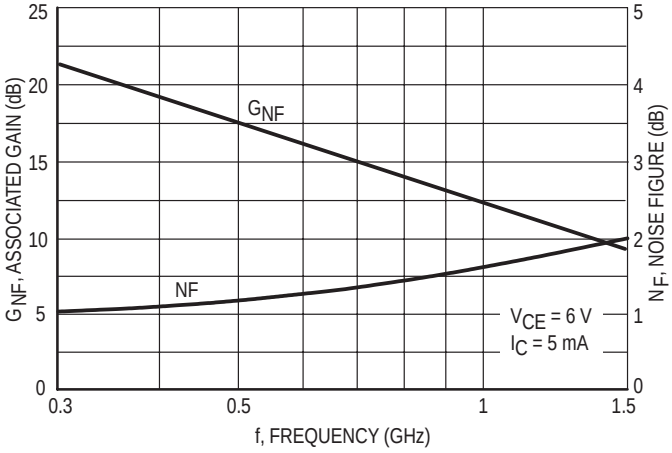


Figure 16. Noise Figure and Associated Gain versus Frequency

V_{CE} = 6.0 V I_C = 5.0 mA

f (GHz)	NF OPT	Γ_o	R_N	K
1.0	1.5 dB	0.27 97°	10	0.91

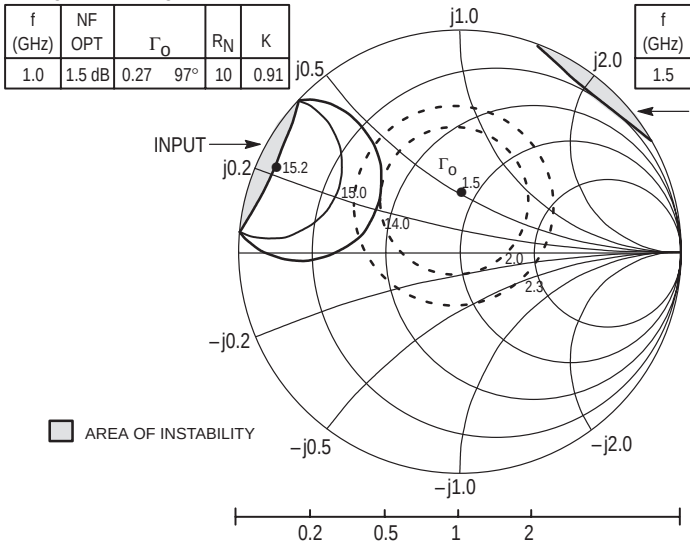


Figure 17. Constant Gain and Noise Figure Contours f = 1.0 GHz

V_{CE} = 6.0 V I_C = 5.0 mA

f (GHz)	NF OPT	Γ_o	R_N	K
1.5	2.0 dB	0.21 54°	14	1.02

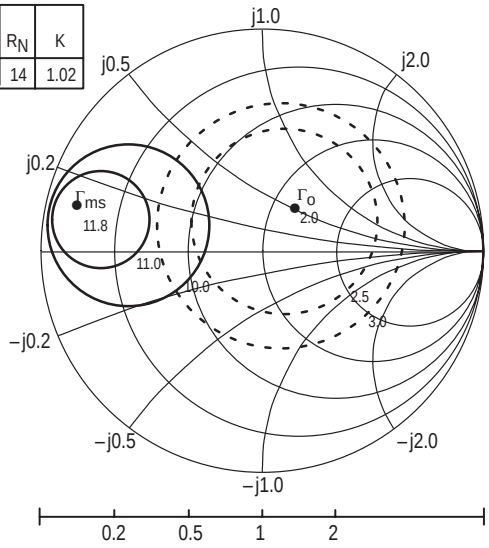


Figure 18. Constant Gain and Noise Figure Contours f = 1.5 GHz

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
2.0	1.0	100	0.959	−19.22	3.518	166.25	0.044	78.43	0.986	−8.12
		200	0.922	−38.32	3.482	153.75	0.079	69.06	0.948	−15.98
		500	0.825	−81.94	2.614	122.98	0.146	44.99	0.803	−30.02
		1000	0.690	−125.83	1.737	93.40	0.167	30.15	0.662	−41.41
		2000	0.600	−174.02	1.079	63.65	0.131	44.93	0.576	−51.42
		3000	0.640	147.15	0.791	50.62	0.196	80.39	0.517	−64.42
	2.0	100	0.922	−24.97	6.598	162.54	0.042	75.55	0.967	−12.35
		200	0.862	−48.55	6.177	147.47	0.075	64.60	0.893	−23.28
		500	0.713	−96.45	4.140	116.09	0.123	43.92	0.671	−38.55
		1000	0.586	−137.24	2.483	90.37	0.140	38.71	0.524	−46.93
		2000	0.506	179.54	1.462	64.47	0.158	57.00	0.456	−51.97
		3000	0.546	144.80	1.079	49.98	0.232	74.13	0.416	−61.22
	5.0	100	0.815	−39.45	14.163	153.09	0.038	70.19	0.895	−22.63
		200	0.708	−71.89	11.635	133.50	0.061	58.57	0.739	−38.46
		500	0.541	−121.43	6.284	104.78	0.090	49.12	0.454	−52.31
		1000	0.461	−155.05	3.428	85.44	0.123	54.90	0.337	−56.38
		2000	0.406	169.75	1.921	65.04	0.198	65.80	0.304	−54.16
		3000	0.438	139.42	1.424	51.41	0.282	69.61	0.276	−57.77
	10	100	0.667	−57.75	22.121	142.36	0.032	64.38	0.788	−34.26
		200	0.559	−95.89	15.709	121.54	0.048	57.27	0.574	−52.06
		500	0.447	−140.52	7.417	98.06	0.075	58.00	0.317	−63.32
		1000	0.405	−166.70	3.921	82.59	0.123	66.07	0.235	−65.49
		2000	0.360	162.90	2.155	65.25	0.222	69.45	0.220	−57.93
		3000	0.390	134.95	1.597	52.60	0.311	68.14	0.196	−57.79
	30	100	0.435	−99.80	31.662	125.82	0.023	62.49	0.570	−51.69
		200	0.421	−135.04	18.696	108.07	0.034	64.74	0.360	−68.74
		500	0.398	−162.97	8.025	91.81	0.069	71.43	0.192	−75.85
		1000	0.382	−179.33	4.163	79.67	0.127	74.17	0.151	−77.73
		2000	0.347	155.68	2.269	64.55	0.240	72.04	0.155	−63.30
		3000	0.379	130.21	1.686	52.60	0.336	67.80	0.132	−60.40
	60	100	0.442	−131.87	26.755	118.52	0.021	62.60	0.422	−56.23
		200	0.483	−155.78	15.086	103.17	0.032	66.87	0.261	−70.51
		500	0.484	−173.89	6.390	88.79	0.067	74.30	0.154	−73.64
		1000	0.472	172.69	3.317	76.81	0.127	76.73	0.140	−74.96
		2000	0.452	149.80	1.834	60.68	0.243	72.97	0.155	−66.57
		3000	0.496	126.23	1.393	48.59	0.345	68.81	0.131	−71.10

(continued)

Table 3. MRF957T1 Typical Common Emitter S–Parameters

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
5.0	1.0	100	0.965	−17.73	3.508	167.36	0.035	78.18	0.990	−6.80
		200	0.931	−35.39	3.495	155.78	0.065	71.66	0.958	−13.35
		500	0.835	−77.08	2.680	126.50	0.122	48.12	0.839	−25.23
		1000	0.694	−120.78	1.820	97.22	0.143	33.67	0.713	−35.51
		2000	0.583	−170.80	1.133	67.35	0.115	50.88	0.629	−44.48
		3000	0.615	148.45	0.813	53.19	0.182	85.71	0.565	−55.47
	2.0	100	0.932	−22.38	6.532	164.05	0.034	77.81	0.975	−9.92
		200	0.875	−44.00	6.217	150.00	0.061	67.15	0.914	−18.98
		500	0.726	−89.77	4.314	119.58	0.106	47.42	0.724	−31.79
		1000	0.582	−131.10	2.638	93.76	0.122	41.23	0.586	−39.20
		2000	0.483	−176.30	1.544	67.35	0.140	60.85	0.521	−43.55
		3000	0.515	146.92	1.117	52.27	0.208	78.88	0.479	−51.26
	5.0	100	0.836	−34.35	14.112	155.49	0.031	71.72	0.920	−18.06
		200	0.731	−63.59	11.971	137.05	0.052	61.40	0.785	−31.06
		500	0.539	−112.00	6.737	107.93	0.080	51.32	0.522	−41.63
		1000	0.438	−147.18	3.710	88.06	0.110	57.59	0.408	−43.94
		2000	0.364	175.10	2.050	67.58	0.175	68.31	0.383	−42.49
		3000	0.392	142.26	1.501	53.59	0.251	73.36	0.357	−45.46
	10	100	0.704	−49.02	22.526	145.79	0.027	67.46	0.831	−27.03
		200	0.577	−83.93	16.647	125.23	0.042	59.78	0.634	−41.45
		500	0.421	−129.59	8.120	100.71	0.069	60.52	0.385	−47.31
		1000	0.361	−158.62	4.290	84.82	0.109	67.54	0.305	−46.57
		2000	0.307	168.57	2.330	67.52	0.196	71.46	0.305	−42.00
		3000	0.332	137.50	1.706	54.85	0.277	71.05	0.288	−42.21
	20	100	0.559	−66.34	30.018	136.00	0.023	64.88	0.720	−35.45
		200	0.453	−103.91	19.598	116.12	0.036	61.80	0.501	−48.64
		500	0.358	−143.87	8.835	96.19	0.064	68.23	0.298	−49.15
		1000	0.324	−167.05	4.595	83.08	0.112	72.95	0.247	−47.12
		2000	0.278	163.88	2.462	67.27	0.208	72.96	0.263	−41.09
		3000	0.306	133.94	1.809	55.45	0.291	70.31	0.249	−39.38
	30	100	0.492	−73.65	32.055	131.68	0.022	64.17	0.669	−37.70
		200	0.412	−110.53	20.121	113.25	0.033	64.60	0.459	−49.28
		500	0.345	−147.89	8.900	94.88	0.062	69.52	0.278	−48.58
		1000	0.319	−169.39	4.646	82.13	0.113	74.20	0.234	−46.64
		2000	0.277	162.38	2.492	67.55	0.210	73.10	0.255	−40.63
		3000	0.305	133.57	1.821	55.24	0.295	70.42	0.239	−38.73

Table 3. MRF957T1 Typical Common Emitter S–Parameters (continued)

The RF MOSFET Line

RF Power Field-Effect Transistor

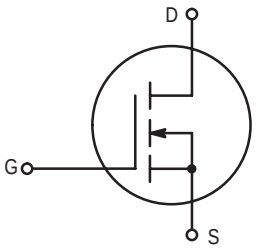
N–Channel Enhancement–Mode

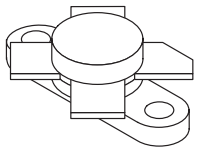
MRF134

. . . designed for wideband large–signal amplifier and oscillator applications up to 400 MHz range.

- Guaranteed 28 Volt, 150 MHz Performance
  Output Power = 5.0 Watts
  Minimum Gain = 11 dB
  Efficiency — 55% (Typical)
- Small–Signal and Large–Signal Characterization
- Typical Performance at 400 MHz, 28 Vdc, 5.0 W
  Output = 10.6 dB Gain
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 2.0 dB (Typ) at 200 mA, 150 MHz
- Excellent Thermal Stability, Ideally Suited For Class A Operation

5.0 W, to 400 MHz
N–CHANNEL MOS
BROADBAND RF POWER
FET





CASE 211–07, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	0.9	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	17.5 0.1	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

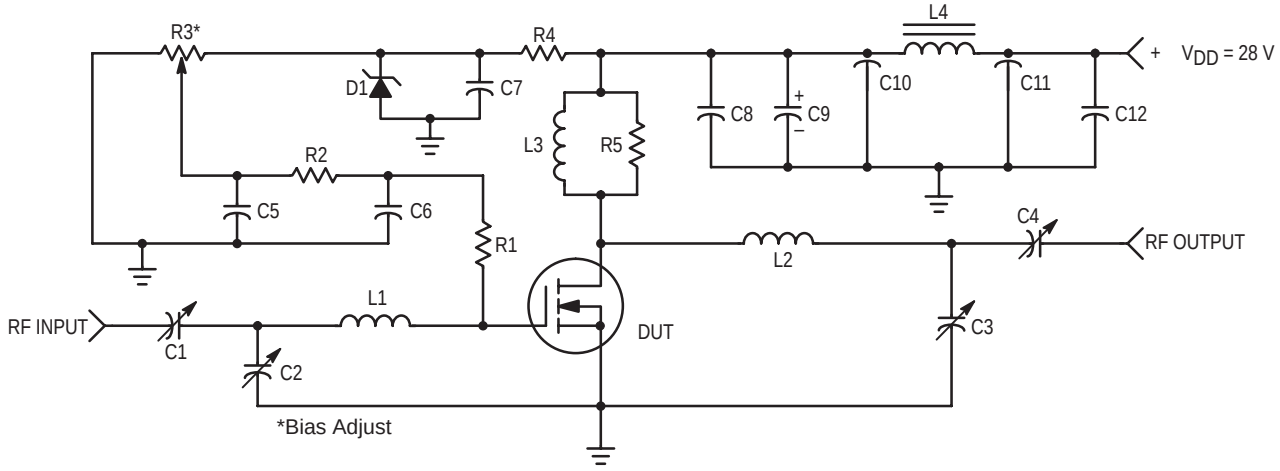
THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (I_D = 10 mA, V_{DS} = 10 V)	$V_{GS(th)}$	1.0	3.5	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 100 mA)	g_{fs}	80	110	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	7.0	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	9.7	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	2.3	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DS} = 28 Vdc, I_D = 200 mA, f = 150 MHz)	NF	—	2.0	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 5.0 W, I_{DQ} = 50 mA) f = 150 MHz (Fig. 1) f = 400 MHz (Fig. 14)	G_{ps}	 11 —	 14 10.6	 — —	dB
Drain Efficiency (Fig. 1) (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 150 MHz, I_{DQ} = 50 mA)	η	50	55	—	%
Electrical Ruggedness (Fig. 1) (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 150 MHz, I_{DQ} = 50 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			



C1, C4 — Arco 406, 15–115 pF
C2 — Arco 403, 3.0–35 pF
C3 — Arco 402, 1.5–20 pF
C5, C6, C7, C8, C12 — 0.1 μF Erie Redcap
C9 — 10 μF, 50 V
C10, C11 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 3 Turns, 0.310″ ID, #18 AWG Enamel, 0.2″ Long
L2 — 3–1/2 Turns, 0.310″ ID, #18 AWG Enamel, 0.25″ Long
L3 — 20 Turns, #20 AWG Enamel Wound on R5
L4 — Ferroxcube VK–200 — 19/4B
R1 — 68 Ω, 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
R5 — 1.0 MΩ, 2.0 W Carbon
Board — G10, 62 mils

Figure 1. 150 MHz Test Circuit

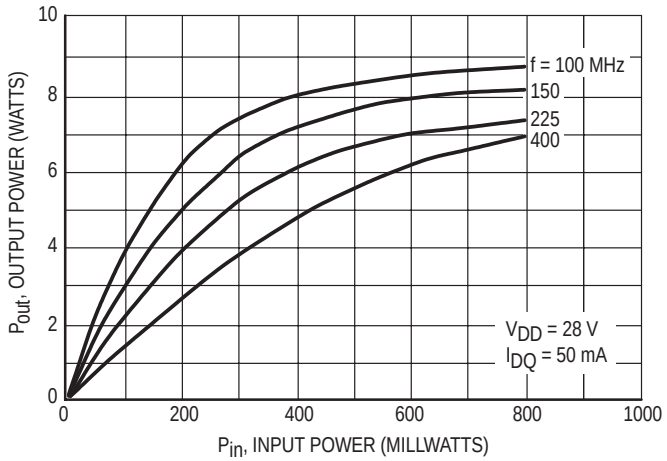


Figure 2. Output Power versus Input Power

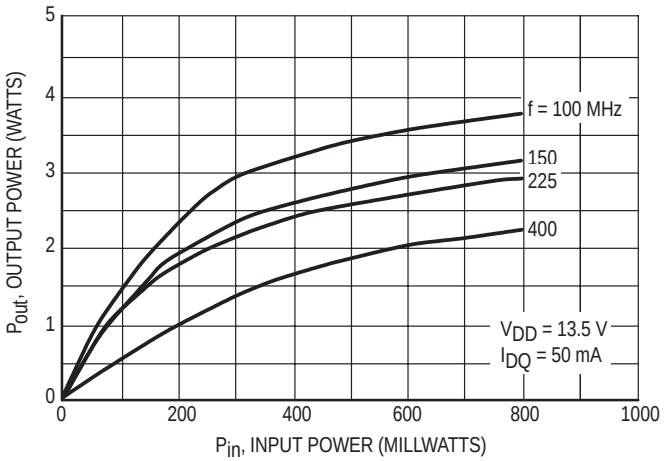


Figure 3. Output Power versus Input Power

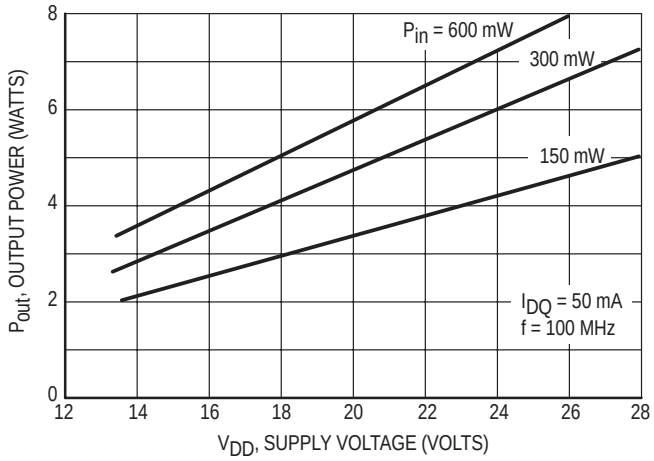


Figure 4. Output Power versus Supply Voltage

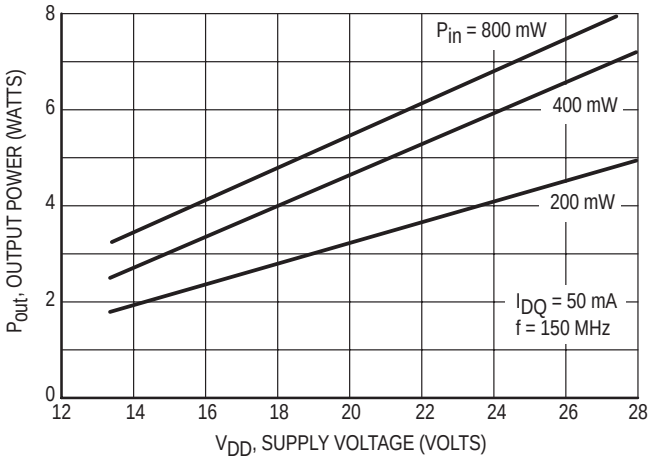


Figure 5. Output Power versus Supply Voltage

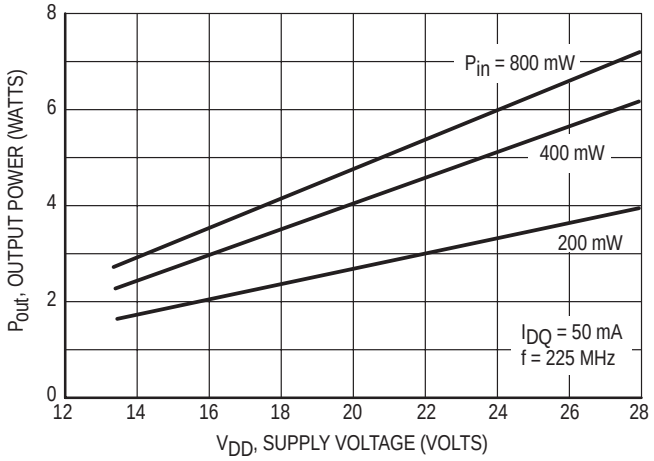


Figure 6. Output Power versus Supply Voltage

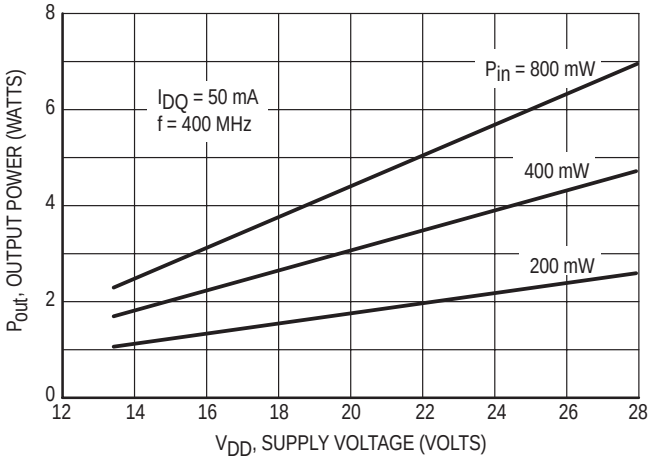


Figure 7. Output Power versus Supply Voltage

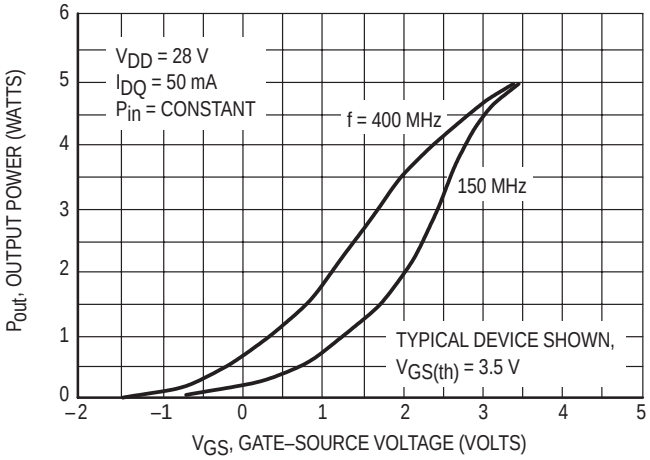


Figure 8. Output Power versus Gate Voltage

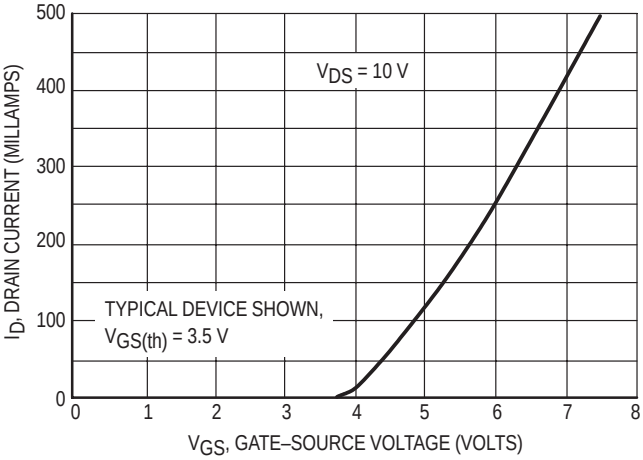


Figure 9. Drain Current versus Gate Voltage (Transfer Characteristics)

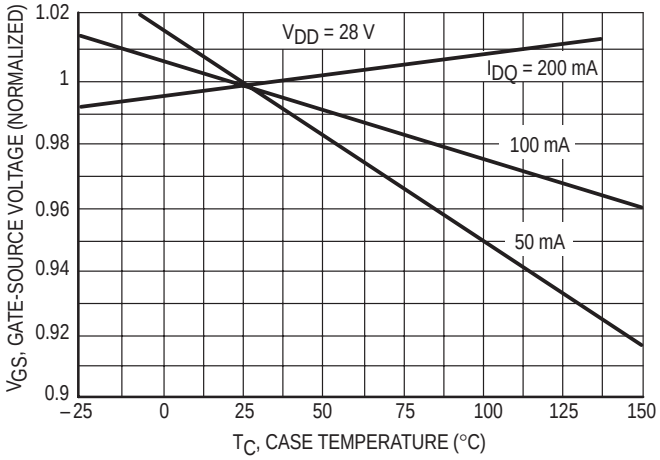


Figure 10. Gate–Source Voltage versus Case Temperature

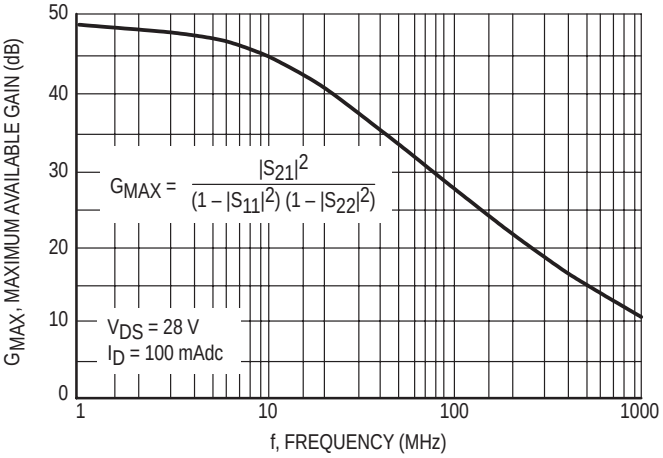


Figure 11. Maximum Available Gain versus Frequency

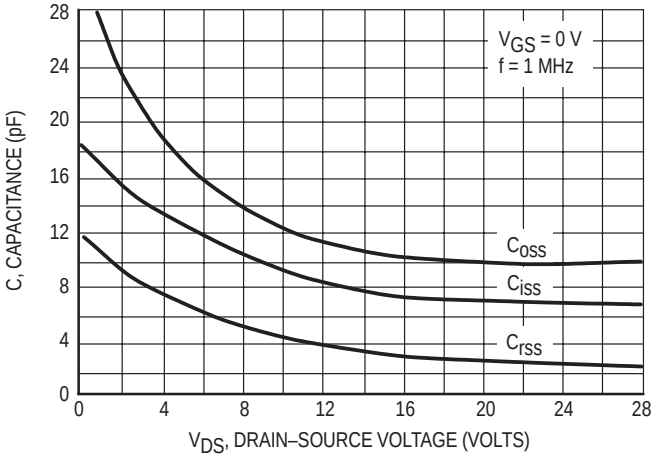


Figure 12. Capacitance versus Voltage

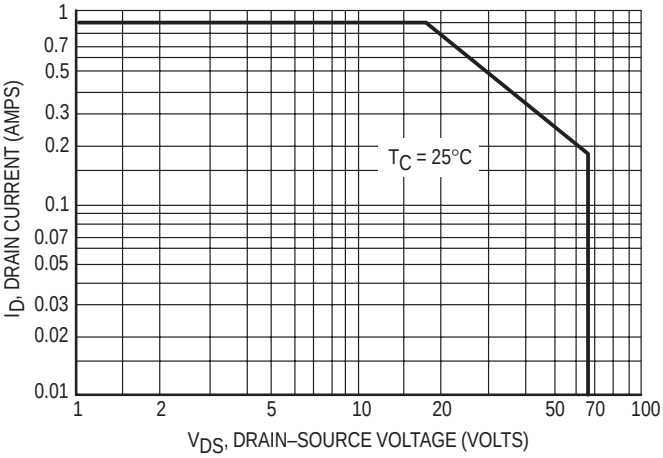
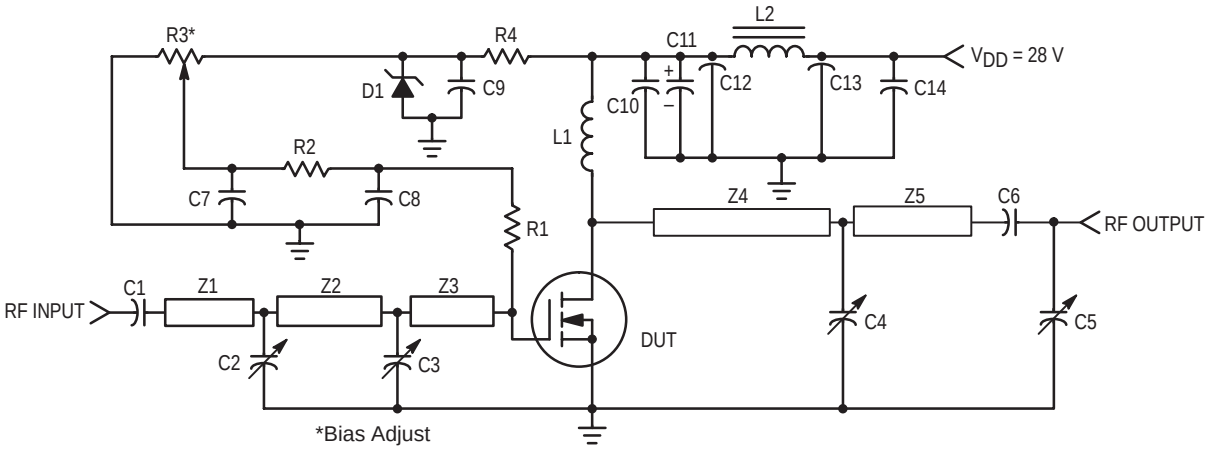
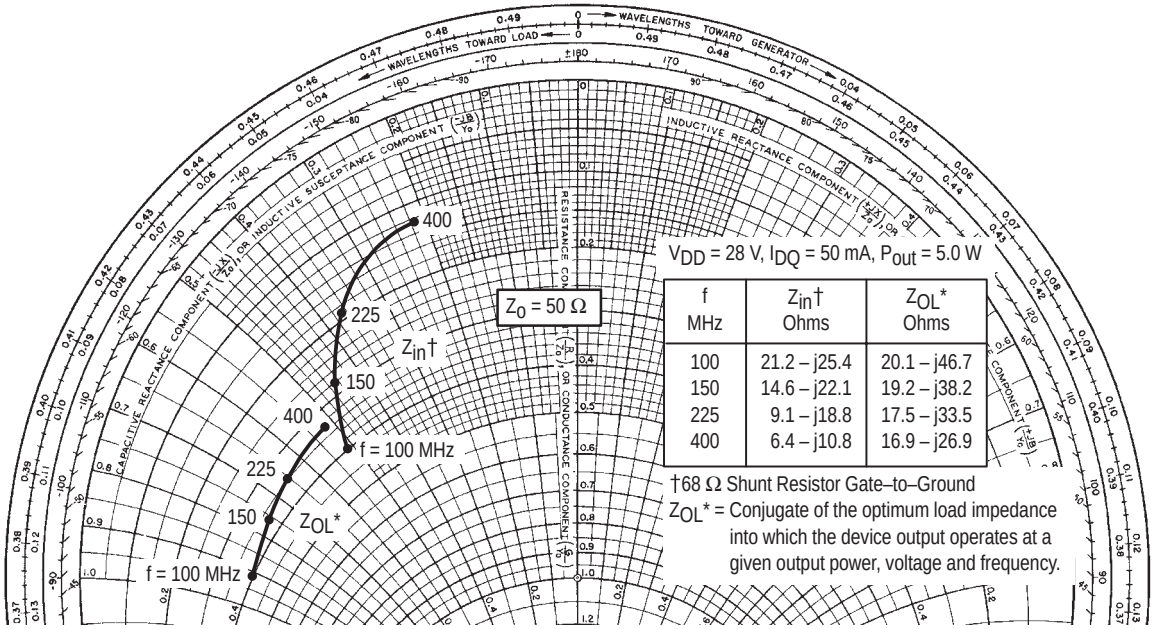


Figure 13. Maximum Rated Forward Biased Safe Operating Area



C1, C6 — 270 pF, ATC 100 mils
C2, C3, C4, C5 — 0–20 pF Johanson
C7, C9, C10, C14 — 0.1 μF Erie Redcap, 50 V
C8 — 0.001 μF
C11 — 10 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 6 Turns, 1/4″ ID, #20 AWG Enamel
L2 — Ferroxcube VK–200 — 19/4B
R1 — 68 Ω, 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
Z1 — 1.4″ x 0.166″ Microstrip
Z2 — 1.1″ x 0.166″ Microstrip
Z3 — 0.95″ x 0.166″ Microstrip
Z4 — 2.2″ x 0.166″ Microstrip
Z5 — 0.85″ x 0.166″ Microstrip
Board — Glass Teflon, 62 mils

Figure 14. 400 MHz Test Circuit



f MHz	Z_{in}† Ohms	Z_{OL}* Ohms
100	21.2 – j25.4	20.1 – j46.7
150	14.6 – j22.1	19.2 – j38.2
225	9.1 – j18.8	17.5 – j33.5
400	6.4 – j10.8	16.9 – j26.9

†68 Ω Shunt Resistor Gate–to–Ground
Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 15. Large–Signal Series Equivalent Input/Output Impedances, Z_{in}†, Z_{OL}*

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
1.0	0.989	−1.0	11.27	179	0.0014	89	0.954	−1.0
2.0	0.989	−2.0	11.27	179	0.0028	89	0.954	−2.0
5.0	0.988	−5.0	11.26	176	0.0069	86	0.954	−4.0
10	0.985	−10	11.20	173	0.014	83	0.951	−9.0
20	0.977	−20	10.99	166	0.027	76	0.938	−18
30	0.965	−30	10.66	159	0.039	69	0.918	−26
40	0.950	−39	10.25	153	0.051	63	0.895	−34
50	0.931	−47	9.777	147	0.060	57	0.867	−42
60	0.912	−53	9.359	142	0.069	53	0.846	−49
70	0.892	−58	8.960	138	0.077	49	0.828	−56
80	0.874	−62	8.583	135	0.085	46	0.815	−62
90	0.855	−66	8.190	131	0.091	43	0.801	−68
100	0.833	−70	7.808	128	0.096	40	0.785	−74
110	0.827	−73	7.661	125	0.101	38	0.784	−77
120	0.821	−76	7.515	122	0.107	36	0.784	−82
130	0.814	−79	7.368	119	0.113	34	0.784	−85
140	0.808	−82	7.222	116	0.119	32	0.783	−88
150	0.802	−86	7.075	114	0.125	31	0.783	−90
160	0.788	−89	6.810	112	0.127	30	0.780	−92
170	0.774	−92	6.540	110	0.128	28	0.774	−94
180	0.763	−94	6.220	108	0.130	26	0.762	−98
190	0.751	−97	5.903	106	0.132	24	0.760	−100
200	0.740	−100	5.784	104	0.134	23	0.758	−103
225	0.719	−104	5.334	100	0.136	20	0.757	−107
250	0.704	−108	4.904	97	0.139	19	0.758	−110
275	0.687	−113	4.551	92	0.141	16	0.757	−114
300	0.673	−117	4.219	89	0.141	14	0.750	−117
325	0.668	−120	3.978	86	0.142	12	0.757	−120
350	0.669	−123	3.737	83	0.142	10	0.766	−121
375	0.662	−125	3.519	80	0.143	9.0	0.768	−123
400	0.654	−127	3.325	77	0.142	8.0	0.772	−124
425	0.650	−129	3.170	75	0.140	7.0	0.772	−125
450	0.638	−131	3.048	72	0.141	6.0	0.783	−125
475	0.614	−132	2.898	71	0.136	6.0	0.786	−126
500	0.641	−133	2.833	68	0.136	5.0	0.795	−127
525	0.638	−135	2.709	66	0.135	5.0	0.801	−127
550	0.633	−137	2.574	64	0.133	4.0	0.802	−128
575	0.628	−138	2.481	62	0.131	5.0	0.805	−128
600	0.625	−140	2.408	60	0.129	5.0	0.814	−128

The Power RF characterization data were measured with a 68 ohm resistor shunting the MRF134 input port. (continued)
The scattering parameters were measured on the MRF134 device alone with no external components.

Table 1. Common Source Scattering Parameters
V_{DS} = 28 V, I_D = 100 mA

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
625	0.619	–142	2.334	58	0.128	5.0	0.818	–129
650	0.617	–144	2.259	56	0.125	6.0	0.824	–130
675	0.618	–146	2.192	55	0.123	7.0	0.834	–130
700	0.619	–147	2.124	53	0.122	8.0	0.851	–131
725	0.618	–150	2.061	51	0.120	9.0	0.859	–132
750	0.614	–152	1.983	49	0.118	11	0.857	–133
775	0.609	–154	1.908	48	0.119	13	0.865	–133
800	0.562	–155	1.877	49	0.118	15	0.872	–133
825	0.587	–156	1.869	46	0.119	16	0.869	–134
850	0.593	–158	1.794	44	0.118	18	0.875	–135
875	0.597	–160	1.749	43	0.119	18	0.881	–135
900	0.598	–162	1.700	41	0.118	18	0.889	–136
925	0.592	–164	1.641	40	0.115	18	0.888	–138
950	0.588	–166	1.590	39	0.112	20	0.877	–138
975	0.586	–168	1.572	39	0.108	23	0.864	–137
1000	0.590	–171	1.551	37	0.107	28	0.863	–137

The Power RF characterization data were measured with a 68 ohm resistor shunting the MRF134 input port. The scattering parameters were measurd on the MRF134 device alone with no external components.

Table 1. Common Source Scattering Parameters (continued)
V_{DS} = 28 V, I_D = 100 mA

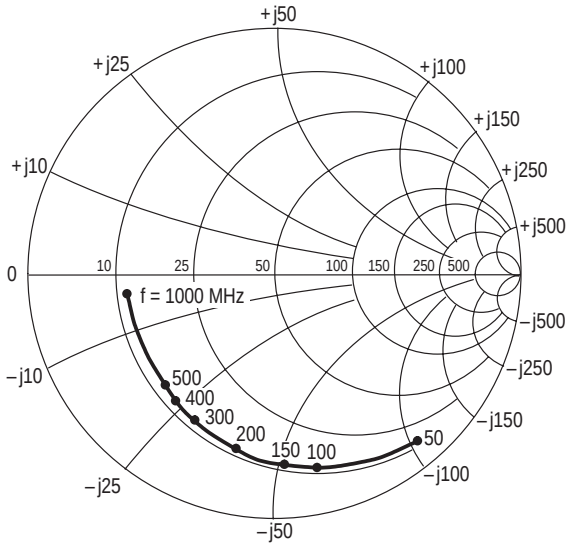


Figure 16. S_{11}, Input Reflection Coefficient versus Frequency
V_{DS} = 28 V I_D = 100 mA

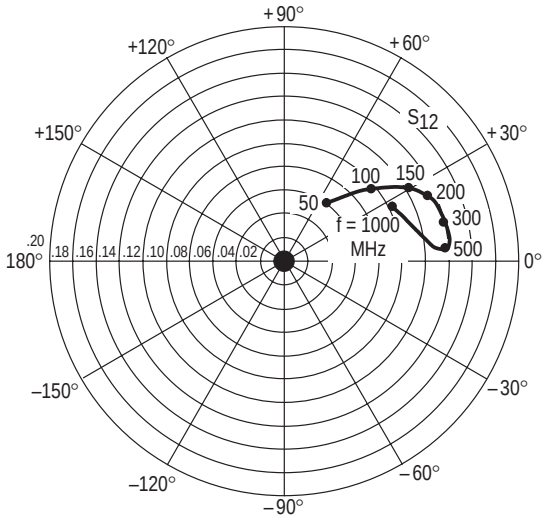


Figure 17. S_{12}, Reverse Transmission Coefficient versus Frequency
V_{DS} = 28 V I_D = 100 mA

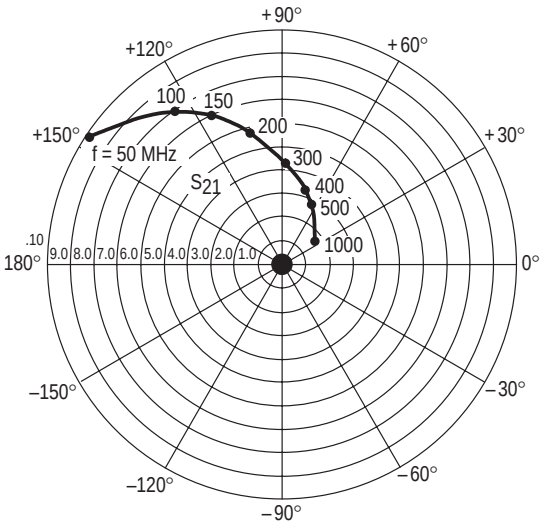


Figure 18. S_{21}, Forward Transmission Coefficient versus Frequency
V_{DS} = 28 V I_D = 100 mA

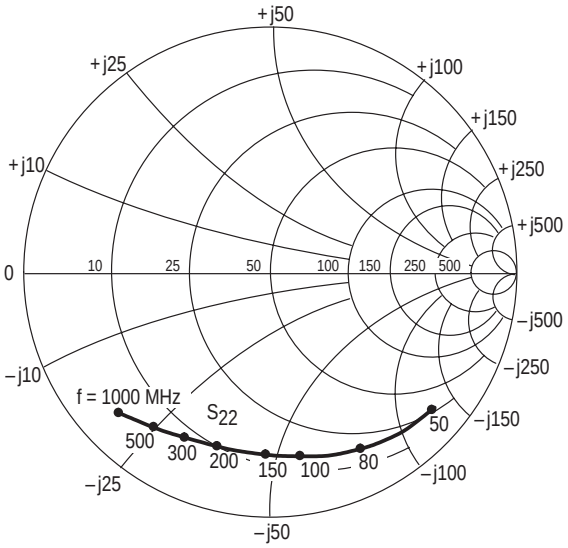


Figure 19. S_{22}, Output Reflection Coefficient versus Frequency
V_{DS} = 28 V I_D = 100 mA

DESIGN CONSIDERATIONS

The MRF134 is a RF power N–Channel enhancement mode field–effect transistor (FET) designed especially for VHF power amplifier and oscillator applications. Motorola RF MOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V–groove vertical power FETs.

Motorola Application Note AN–211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF134 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF134 was characterized at I_{DQ} = 50 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF134 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF134. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF134, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The MRF134 was characterized with a 68–ohm input shunt loading resistor. Two port parameter stability analysis with the MRF134 s–parameters provides a useful–tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A for a discussion of two port network theory and stability.

Input resistive loading is not feasible in low noise applications. The MRF134 noise figure data was generated in a circuit with drain loading and a low loss input network.

The RF MOSFET Line

RF Power Field-Effect Transistors

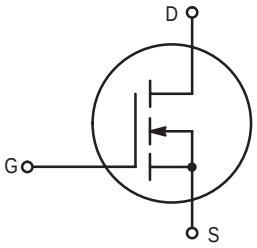
N-Channel Enhancement-Mode MOSFET

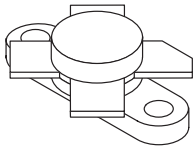
MRF136

15 W, to 400 MHz
N–CHANNEL
MOS BROADBAND
RF POWER FET

Designed for wideband large–signal amplifier and oscillator applications up to 400 MHz range, in single ended configuration.

- Guaranteed 28 Volt, 150 MHz Performance
  Output Power = 15 Watts
  Narrowband Gain = 16 dB (Typ)
  Efficiency = 60% (Typical)
- Small–Signal and Large–Signal Characterization
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques





CASE 211–07, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	2.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	55 0.314	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

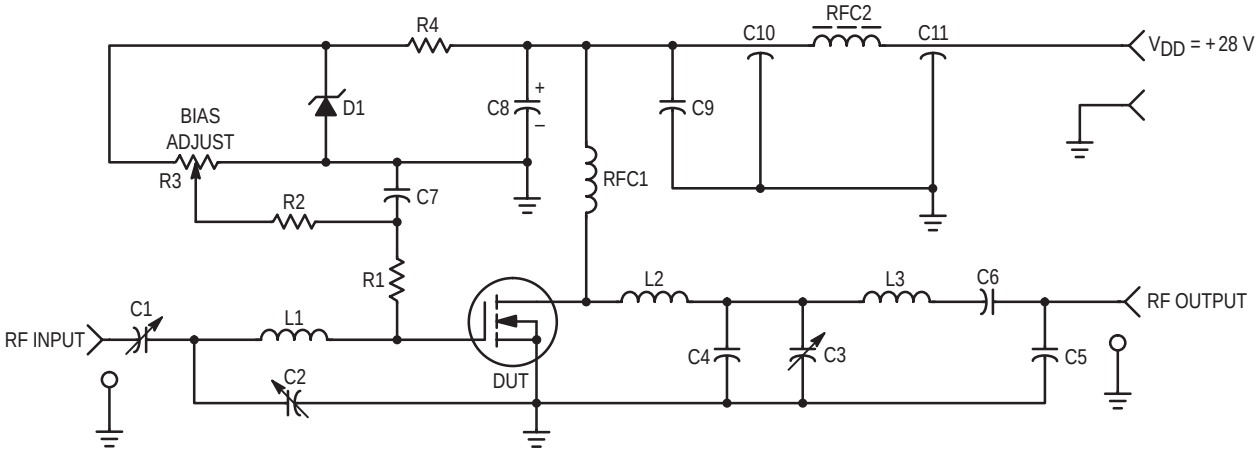
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.2	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero–Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	2.0	mAdc
Gate–Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 250 mA)	g_{fs}	250	400	—	mmhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	24	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	27	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	5.5	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DS} = 28 Vdc, I_D = 500 mA, f = 150 MHz)	NF	—	1.0	—	dB
Common Source Power Gain (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 150 MHz, I_{DQ} = 25 mA)	G_{ps}	13	16	—	dB
Drain Efficiency (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 150 MHz, I_{DQ} = 25 mA)	η	50	60	—	%
Electrical Ruggedness (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 150 MHz, I_{DQ} = 25 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each side measured separately.



C1, C2 — Arco 406, 15–115 pF or Equivalent
C3 — Arco 404, 8–60 pF or Equivalent
C4 — 43 pF Mini–Unelco or Equivalent
C5 — 24 pF Mini–Unelco or Equivalent
C6 — 680 pF, 100 Mils Chip
C7 — 0.01 μF Ceramic
C8 — 100 μF, 40 V
C9 — 0.1 μF Ceramic
C10, C11 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — 2 Turns, 0.29″ ID, #18 AWG, 0.10″ Long
L2 — 2 Turns, 0.23″ ID, #18 AWG, 0.10″ Long
L3 — 2–1/4 Turns, 0.29″ ID, #18 AWG, 0.125″ Long
RFC1 — 20 Turns, 0.30″ ID, #20 AWG Enamel Closewound
RFC2 — Ferroxcube VK–200 — 19/4B
R1 — 27 Ω, 1 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ
R4 — 1.8 kΩ, 1/2 W
Board Material — 0.062″ G10, 1 oz. Cu Clad, Double Sided

Figure 1. 150 MHz Test Circuit

TYPICAL CHARACTERISTICS

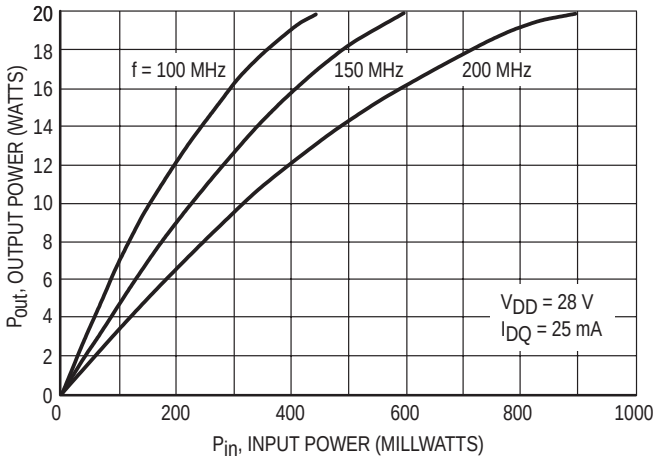


Figure 2. Output Power versus Input Power

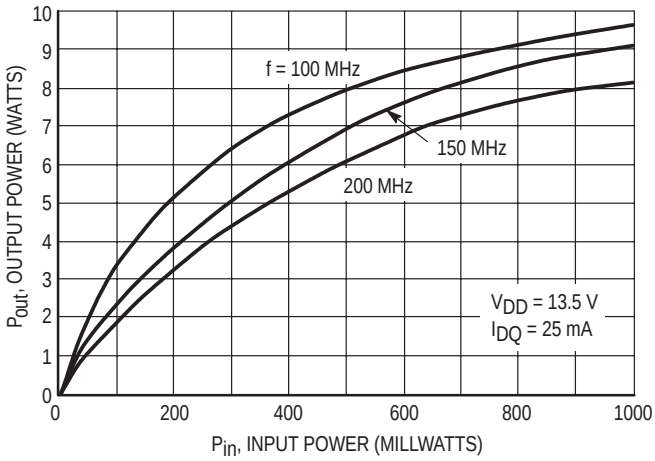


Figure 3. Output Power versus Input Power

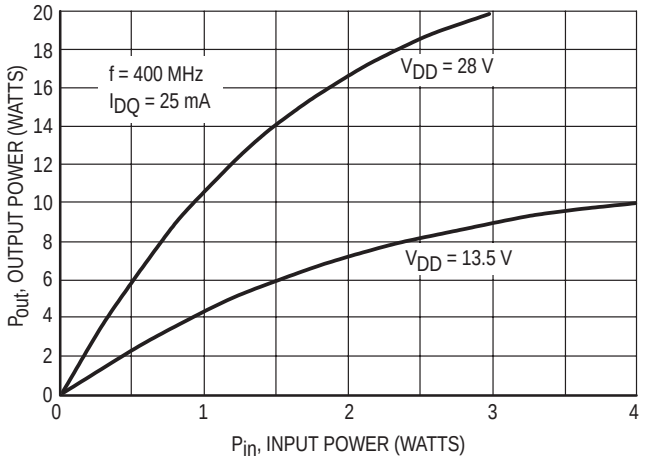


Figure 4. Output Power versus Input Power

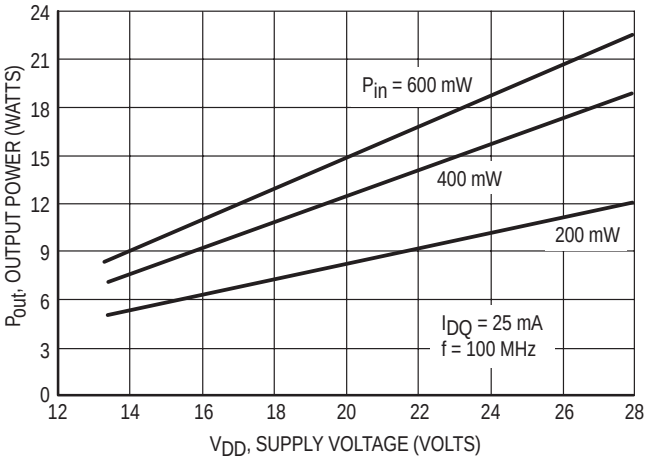


Figure 5. Output Power versus Supply Voltage

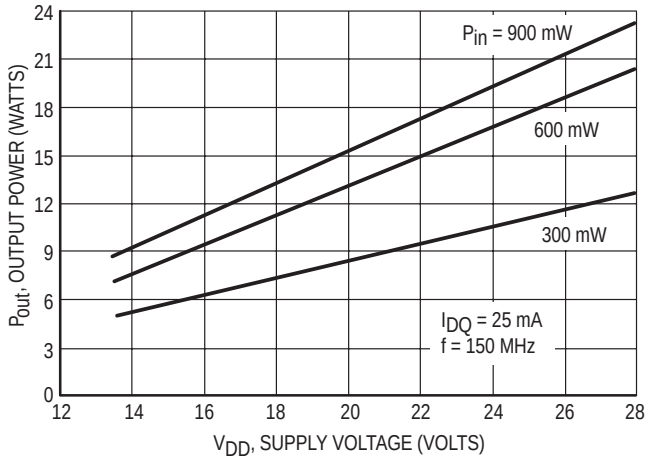


Figure 6. Output Power versus Supply Voltage

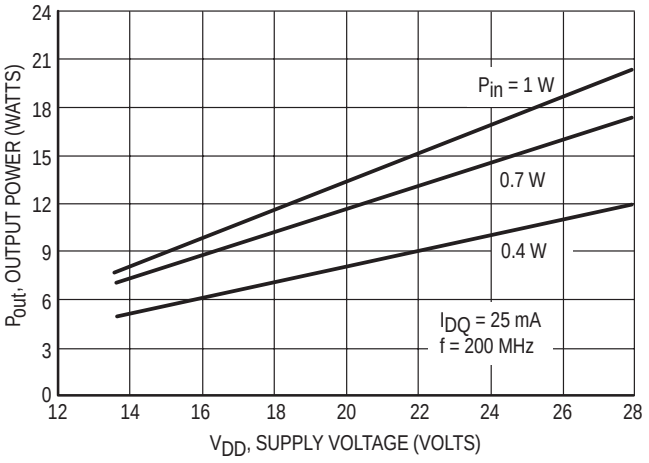


Figure 7. Output Power versus Supply Voltage

TYPICAL CHARACTERISTICS

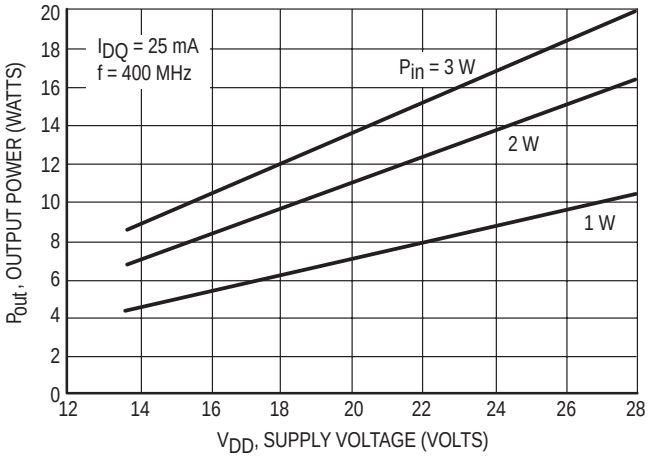


Figure 8. Output Power versus Supply Voltage

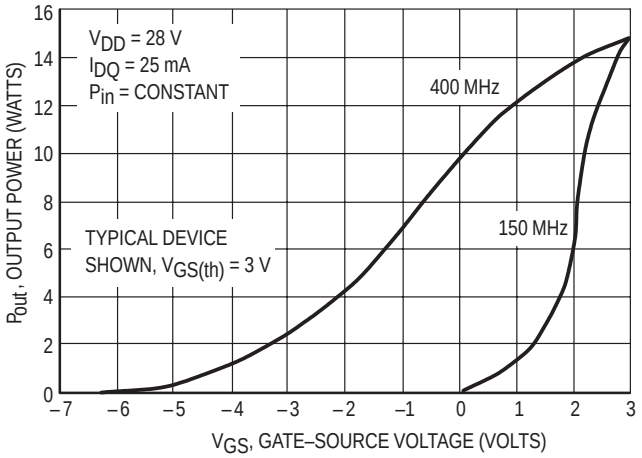


Figure 9. Output Power versus Gate Voltage

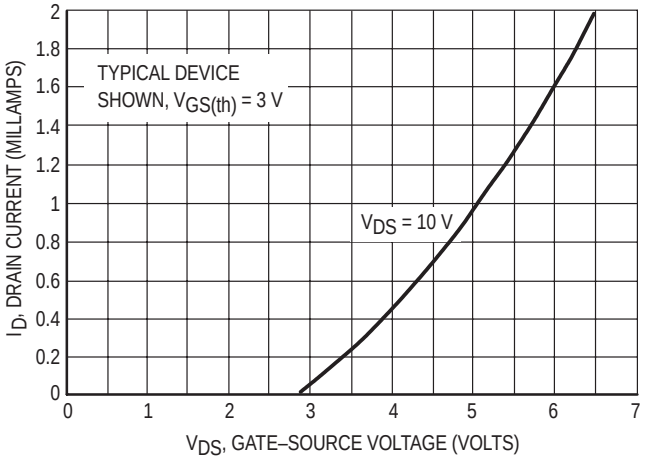


Figure 10. Drain Current versus Gate Voltage (Transfer Characteristics)

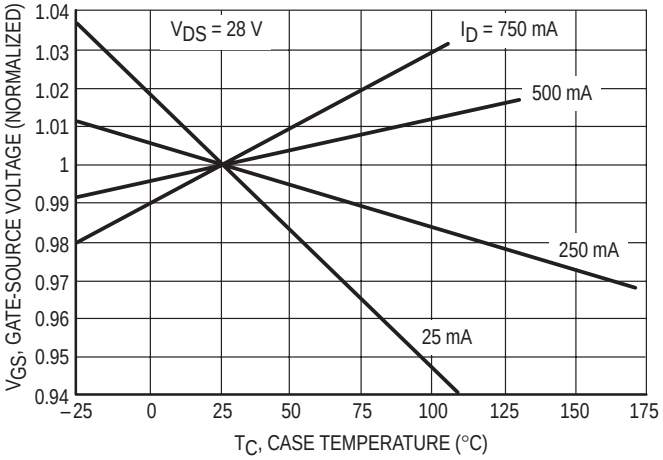


Figure 11. Gate–Source Voltage versus Case Temperature

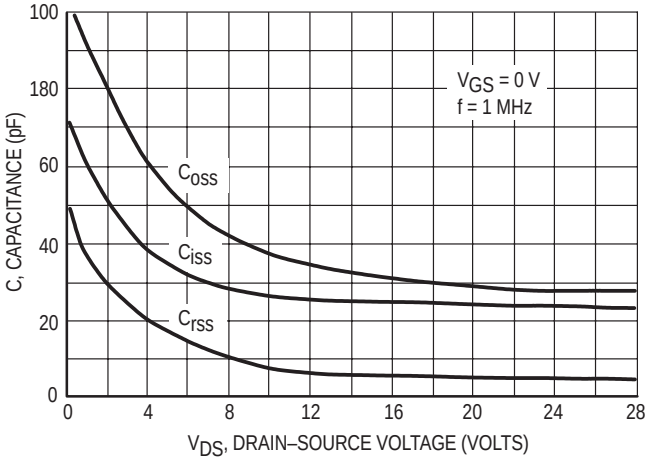


Figure 12. Capacitance versus Drain–Source Voltage

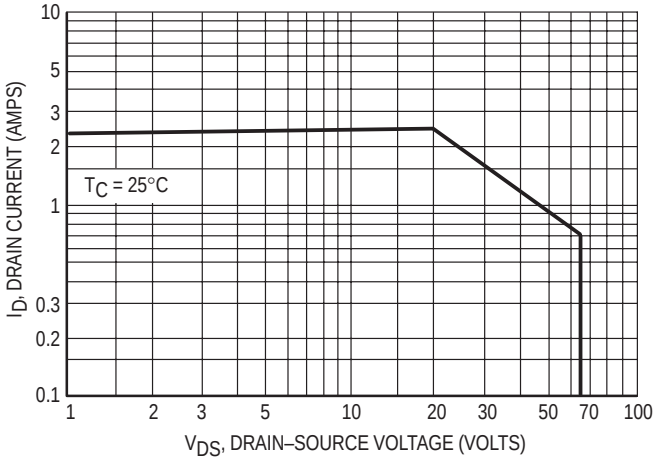


Figure 13. DC Safe Operating Area

TYPICAL CHARACTERISTICS

TYPICAL 400 MHz PERFORMANCE

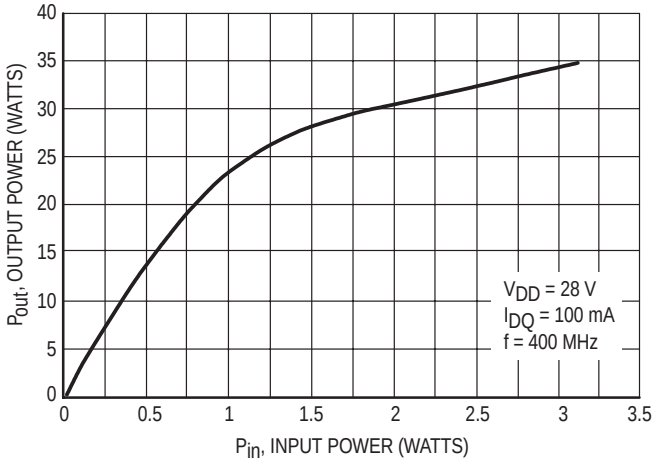


Figure 14. Output Power versus Input Power

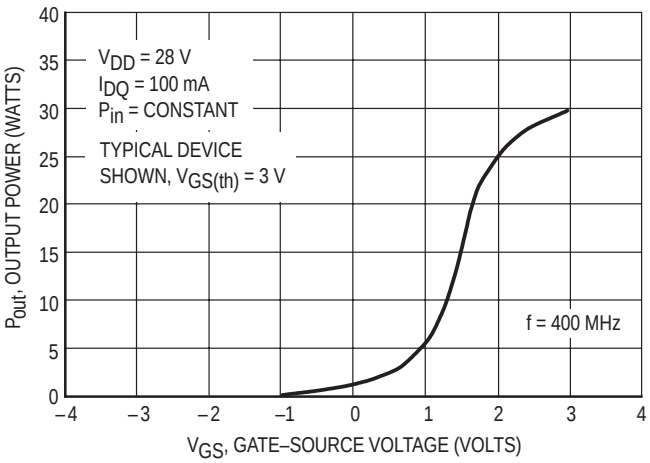


Figure 15. Output Power versus Gate Voltage

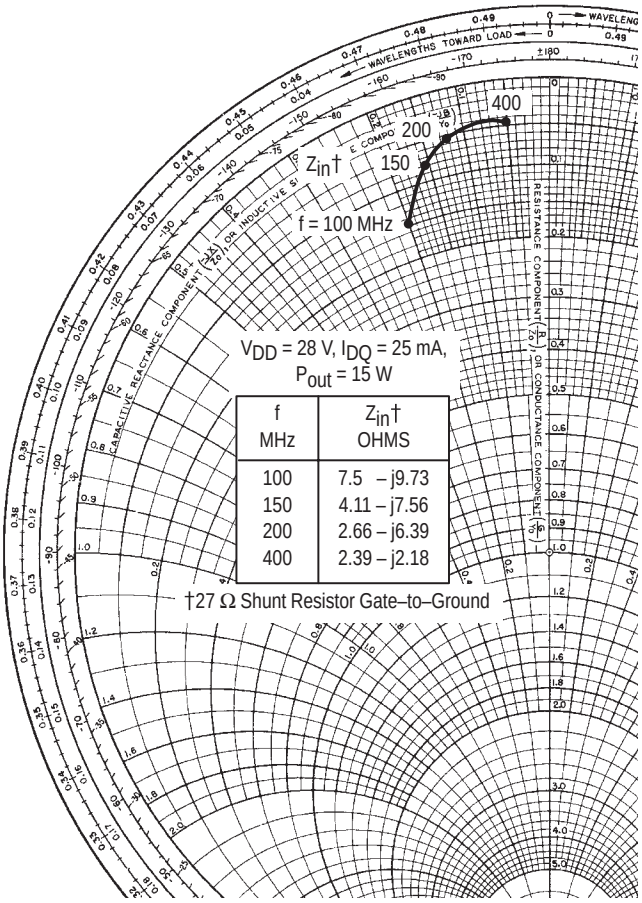


Figure 16. Large–Signal Series Equivalent Input Impedance, Z_{in}†

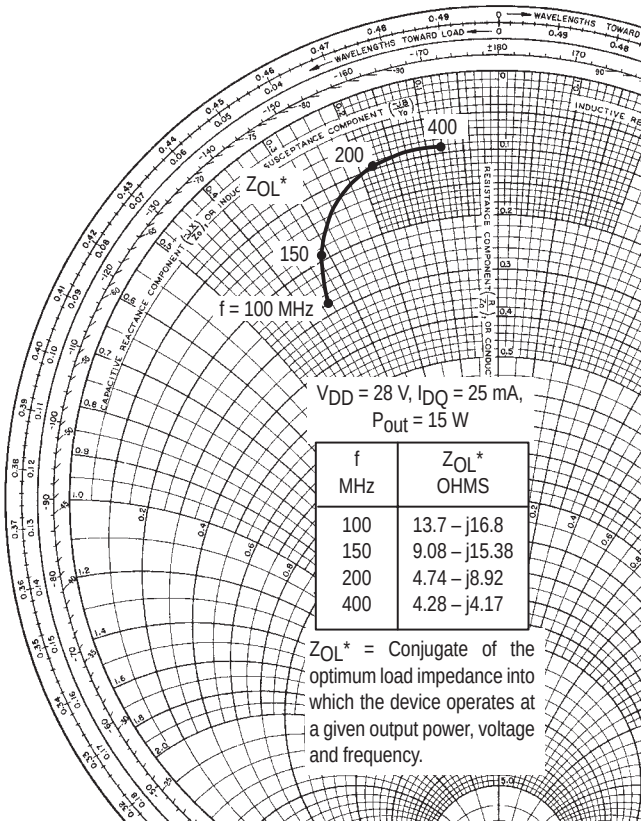


Figure 17. Large–Signal Series Equivalent Output Impedance, Z_{OL}*

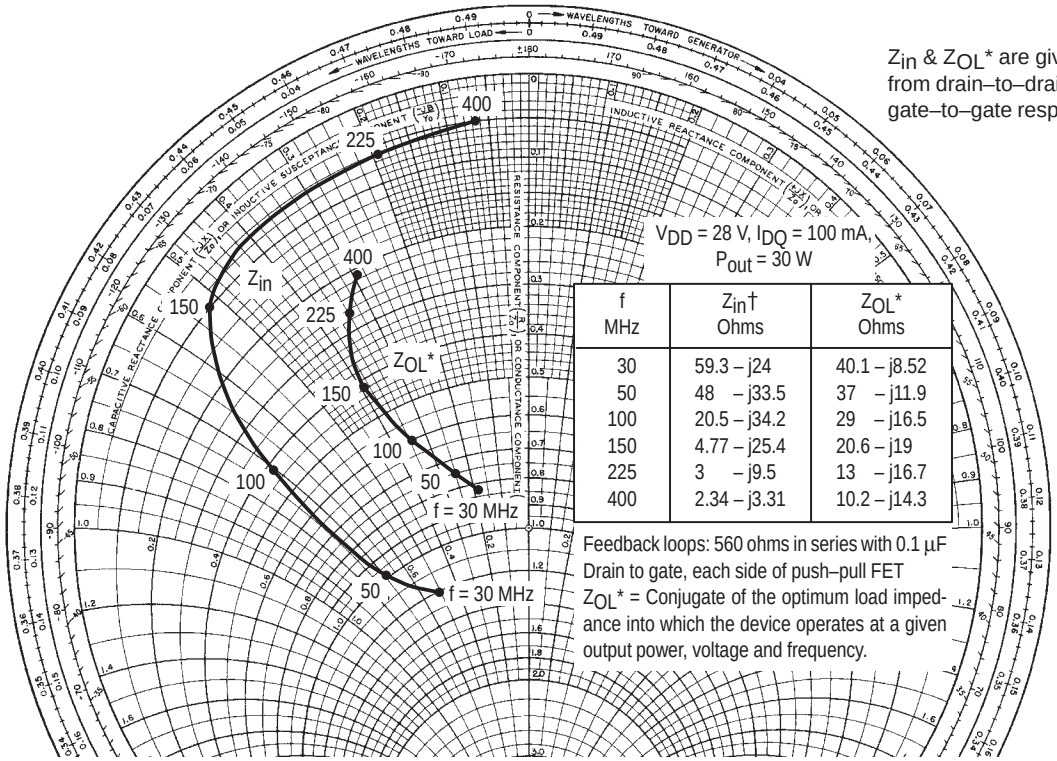


Figure 18. Input and Outut Impedance

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
2.0	0.988	–11	41.19	173	0.006	67	0.729	–12
5.0	0.970	–27	40.07	164	0.014	62	0.720	–31
10	0.923	–52	35.94	149	0.026	54	0.714	–58
20	0.837	–88	27.23	129	0.040	36	0.690	–96
30	0.784	–111	20.75	117	0.046	27	0.684	–118
40	0.751	–125	16.49	108	0.048	22	0.680	–131
50	0.733	–135	13.41	103	0.050	19	0.679	–139
60	0.720	–142	11.43	99	0.050	16	0.678	–145
70	0.709	–147	9.871	96	0.050	14	0.679	–149
80	0.707	–152	8.663	93	0.051	13	0.683	–153
90	0.706	–155	7.784	91	0.051	13	0.682	–155
100	0.708	–157	7.008	88	0.051	13	0.680	–157
110	0.711	–159	6.435	86	0.051	14	0.681	–158
120	0.714	–161	5.899	85	0.051	15	0.682	–159
130	0.717	–163	5.439	82	0.052	16	0.684	–160
140	0.720	–164	5.068	80	0.052	17	0.684	–161
150	0.723	–165	4.709	80	0.052	18	0.686	–161
160	0.727	–166	4.455	78	0.052	18	0.690	–161
170	0.732	–167	4.200	77	0.052	18	0.694	–162
180	0.735	–168	3.967	75	0.052	19	0.699	–162
190	0.738	–169	3.756	74	0.052	19	0.703	–163
200	0.740	–170	3.545	73	0.052	20	0.706	–163
225	0.746	–171	3.140	69	0.053	22	0.717	–163
250	0.742	–172	2.783	67	0.053	25	0.724	–163
275	0.744	–173	2.540	64	0.054	27	0.724	–163
300	0.751	–174	2.323	60	0.055	29	0.736	–163
325	0.757	–175	2.140	58	0.058	32	0.749	–163
350	0.760	–176	1.963	54	0.059	35	0.758	–163
375	0.762	–177	1.838	52	0.062	38	0.768	–163
400	0.774	–179	1.696	50	0.065	41	0.783	–163
425	0.775	–179	1.590	48	0.068	43	0.793	–163
450	0.781	+179	1.493	46	0.071	46	0.805	–163
475	0.787	+177	1.415	43	0.074	47	0.813	–164
500	0.792	+176	1.332	40	0.079	48	0.825	–164
525	0.797	+175	1.259	38	0.083	50	0.831	–164
550	0.801	+175	1.185	37	0.088	51	0.843	–164
575	0.810	+174	1.145	36	0.094	52	0.855	–164
600	0.816	+173	1.091	34	0.101	52	0.869	–165
625	0.818	+171	1.041	32	0.106	53	0.871	–165
650	0.825	+170	0.994	30	0.112	53	0.884	–165
675	0.834	+169	0.962	29	0.119	53	0.890	–165
700	0.837	+168	0.922	27	0.127	53	0.906	–166
725	0.836	+167	0.879	25	0.133	52	0.909	–167
750	0.841	+166	0.838	25	0.140	53	0.917	–167
775	0.844	+165	0.824	24	0.148	52	0.933	–167
800	0.846	+163	0.785	21	0.154	50	0.941	–168

Table 1. Common Source Scattering Parameters
V_{DS} = 28 V, I_D = 0.5 A

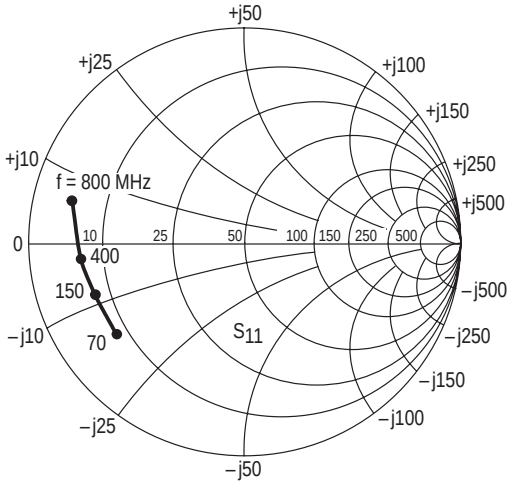


Figure 19. S_{11}, Input Reflection Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

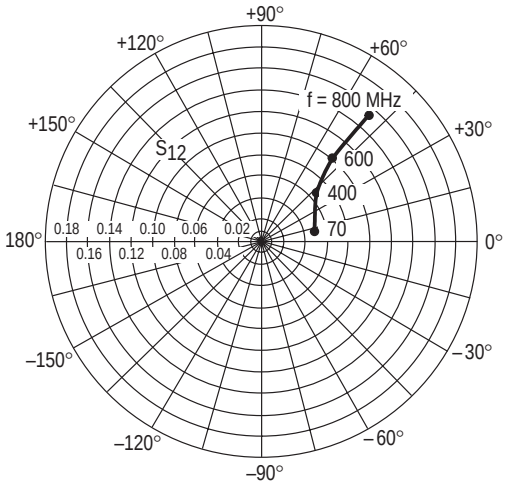


Figure 20. S_{12}, Reverse Transmission Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

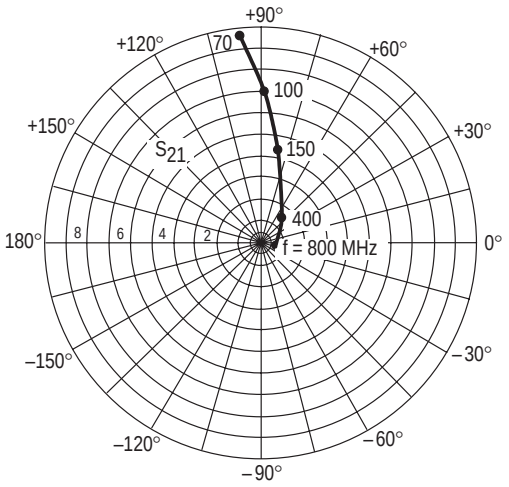


Figure 21. S_{21}, Forward Transmission Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

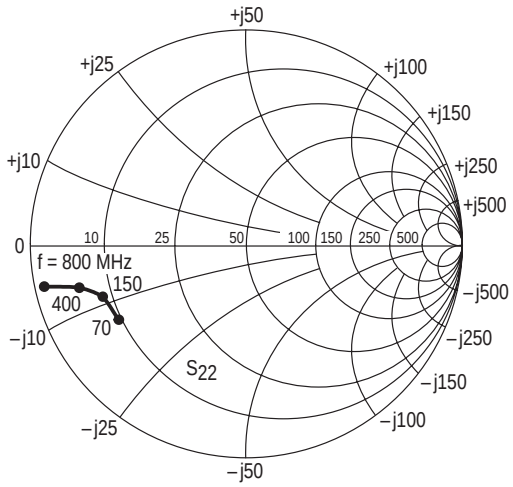


Figure 22. S_{22}, Output Reflection Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

DESIGN CONSIDERATIONS

The MRF136 is an RF power N–Channel enhancement mode field–effect transistor (FET) designed especially for HF and VHF power amplifier applications. Motorola RF MOS FETs feature planar design for optimum manufacturability.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF136 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied without gate bias. A positive gate voltage causes drain current to flow (see Figure 10). RF power FETs require forward bias for optimum gain and power output. A Class AB condition with quiescent drain current (I_{DQ}) in the 25–100 mA range is sufficient for many applications. For special requirements such as linear amplification, I_{DQ} may have to be adjusted to optimize the critical parameters.

The MOS gate is a dc open circuit. Since the gate bias circuit does not have to deliver any current to the FET, a simple resistive divider arrangement may sometimes suffice for this function. Special applications may require more elaborate gate bias systems.

GAIN CONTROL

Power output of the MRF136 may be controlled from rated values down to the milliwatt region (>20 dB reduction in power output with constant input power) by varying the dc gate voltage. This feature, not available in bipolar RF power devices, facilitates the incorporation of manual gain control, AGC/ALC and modulation schemes into system designs. A full range of power output control may require dc gate voltage excursions into the negative region.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for MRF136. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. Both small signal scattering parameters and large signal impedance parameters are provided. Large signal impedances should be used for network designs wherever possible. While the s parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is particularly useful at frequencies outside those presented in the large signal impedance plots.

RF power FETs are triode devices and are therefore not unilateral. This, coupled with the very high gain, yields a device capable of self oscillation. Stability may be achieved using techniques such as drain loading, input shunt resistive loading, or feedback. S parameter stability analysis can provide useful information in the selection of loading and/or feedback to insure stable operation. The MRF136 was characterized with a 27 ohm input shunt loading resistor.

For further discussion of RF amplifier stability and the use of two port parameters in RF amplifier design, see Motorola Application Note AN215A.

LOW NOISE OPERATION

Input resistive loading will degrade noise performance, and noise figure may vary significantly with gate driving impedance. A low loss input matching network with its gate impedance optimized for lowest noise is recommended.

The RF MOSFET Line

RF Power Field-Effect Transistor

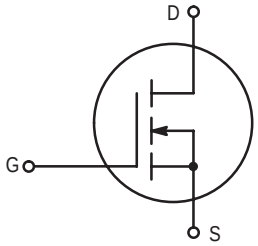
N–Channel Enhancement–Mode MOSFET

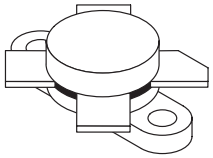
MRF141

Designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 30 MHz, 28 V:
  Output Power — 150 W
  Gain — 18 dB (22 dB Typ)
  Efficiency — 40%
- Typical Performance at 175 MHz, 50 V:
  Output Power — 150 W
  Gain — 13 dB
- Low Thermal Resistance
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability
- S–Parameters Available for Download into Frequency Domain Simulators. See http://motorola.com/sps/rf/designtds/

150 W, 28 V, 175 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET





CASE 211–11, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage	V_{DGO}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.71	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

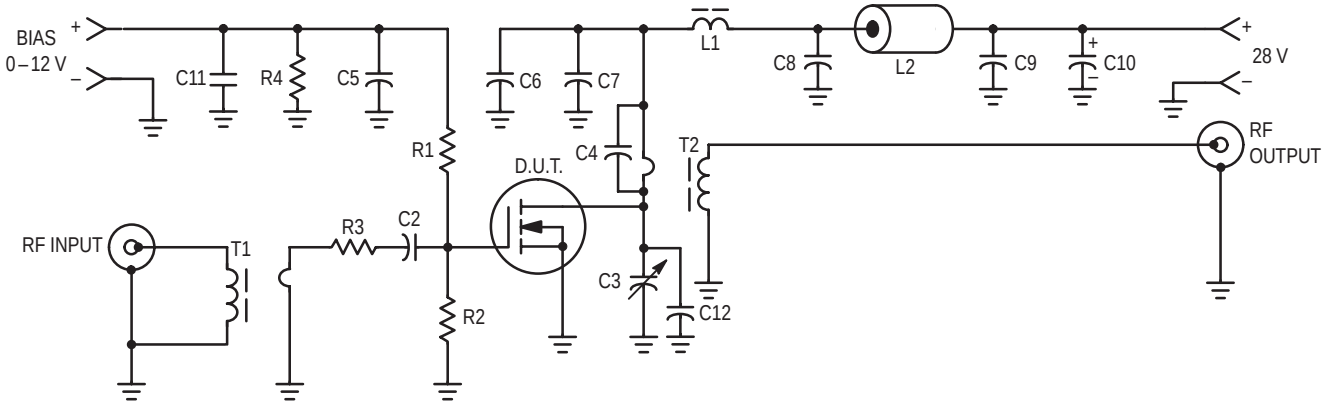
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	0.1	0.9	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	5.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	350	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	420	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	35	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain, f = 30; 30.001 MHz (V_{DD} = 28 V, P_{out} = 150 W (PEP), I_{DQ} = 250 mA) f = 175 MHz	G_{ps}	16 —	20 10	— —	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 250 mA, I_D (Max) = 5.95 A)	η	40	45	—	%
Intermodulation Distortion (1) (V_{DD} = 28 V, P_{out} = 150 W (PEP), f = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 250 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	–30 –60	–28 —	dB
Load Mismatch (V_{DD} = 28 V, P_{out} = 150 W (PEP), f1 = 30; 30.001 MHz, I_{DQ} = 250 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{DD} = 28 V, P_{out} = 50 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 4.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9–13)}$	— — —	23 –50 –75	— — —	dB

NOTE:
1. To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C2, C5, C6, C7, C8, C9 — 0.1 μF Ceramic Chip or Monolythic with Short Leads
C3 — Arco 469
C4 — 820 pF Unencapsulated Mica or Dipped Mica with Short Leads
C10 — 10 μF/100 V Electrolytic
C11 — 1 μF, 50 V, Tantalum
C12 — 330 pF, Dipped Mica (Short leads)
L1 — VK200/4B Ferrite Choke or Equivalent, 3.0 μH
L2 — Ferrite Bead(s), 2.0 μH
R1, R2 — 51 Ω/1.0 W Carbon
R3 — 1.0 Ω/1.0 W Carbon or Parallel Two 2 Ω, 1/2 W Resistors
R4 — 1 kΩ/1/2 W Carbon
T1 — 16:1 Broadband Transformer
T2 — 1:25 Broadband Transformer
Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, ε_r = 5

Figure 1. 30 MHz Test Circuit (Class AB)

TYPICAL CHARACTERISTICS

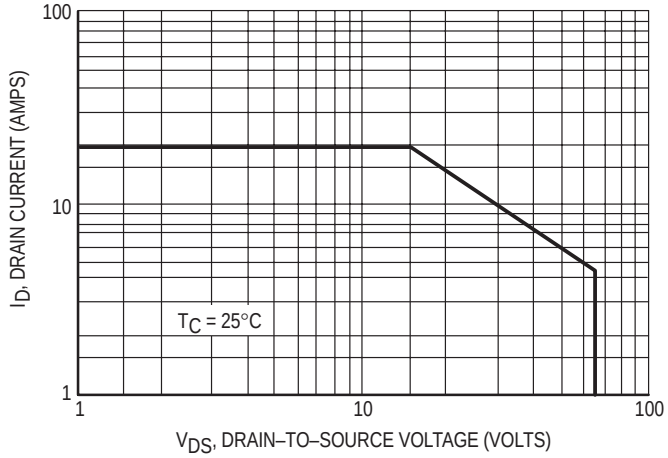


Figure 2. DC Safe Operating Area

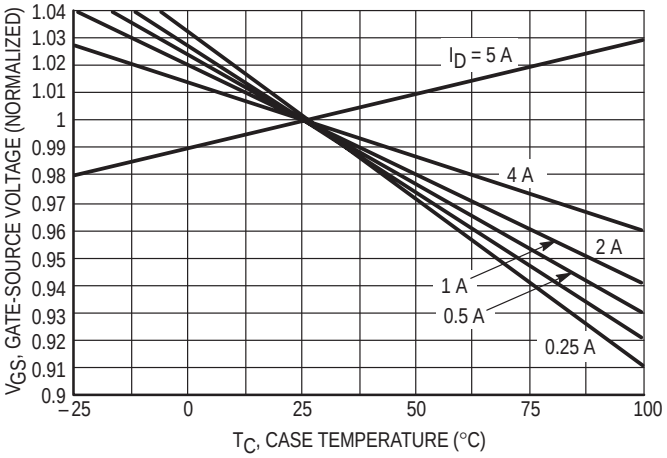


Figure 3. Gate–Source Voltage versus Case Temperature

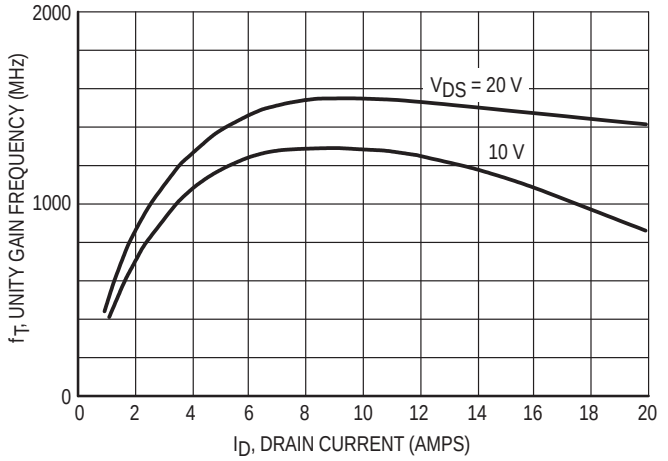


Figure 4. Common Source Unity Gain Frequency versus Drain Current

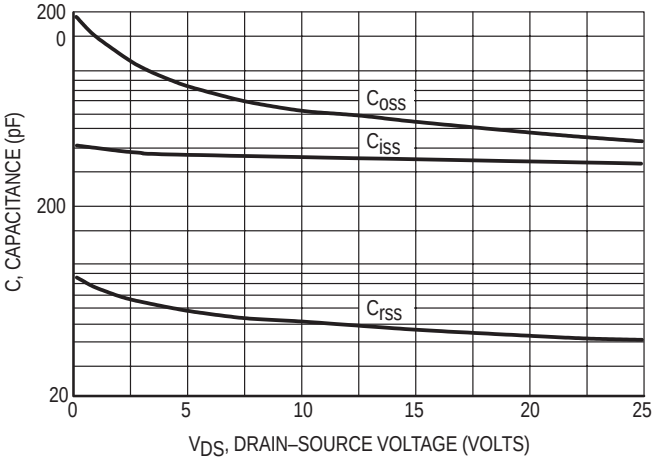


Figure 5. Capacitance versus Drain–Source Voltage

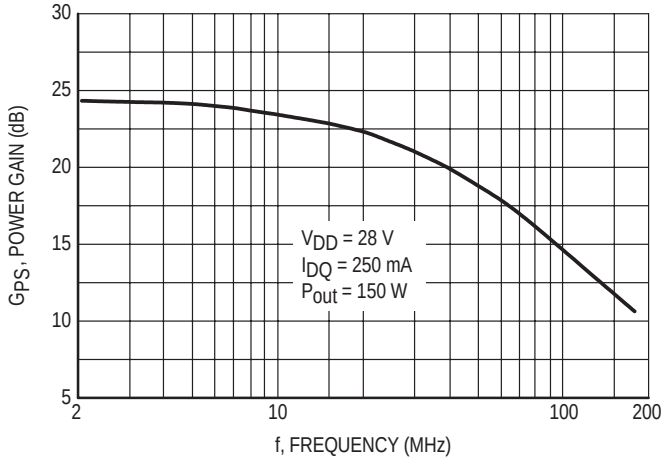


Figure 6. Power Gain versus Frequency

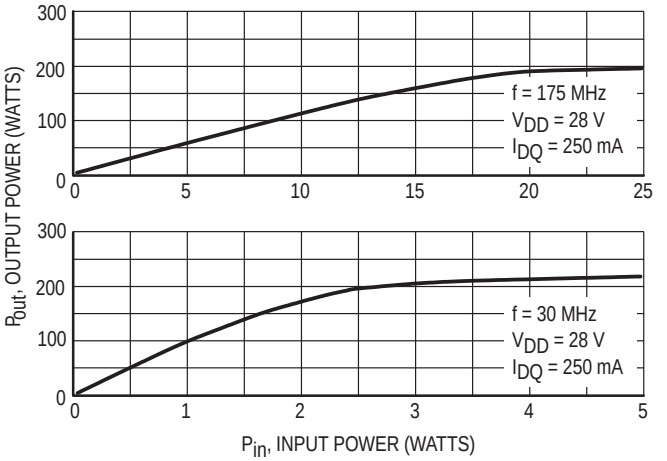


Figure 7. Output Power versus Input Power

TYPICAL CHARACTERISTICS

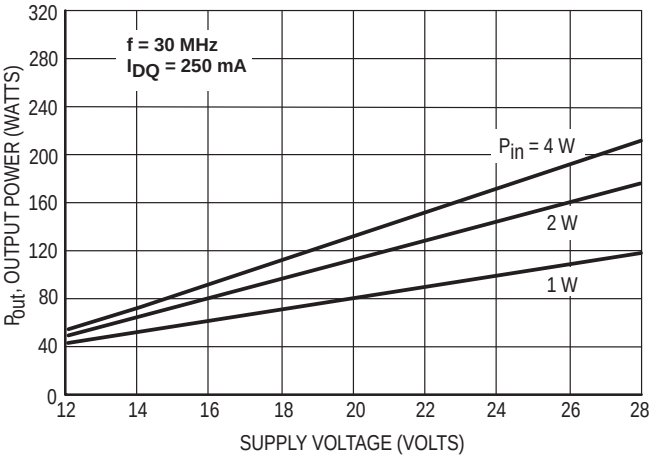


Figure 8. Output Power versus Supply Voltage

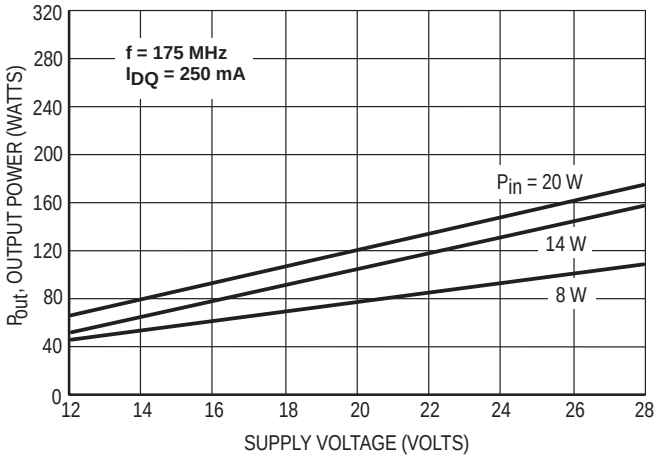


Figure 9. Output Power versus Supply Voltage

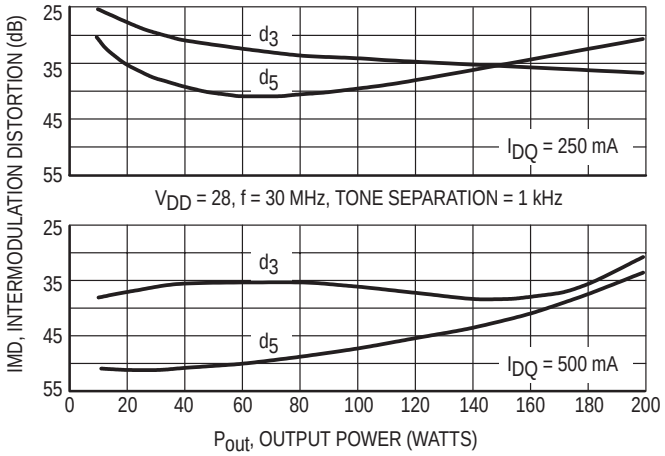


Figure 10. IMD versus P_{out} (PEP)

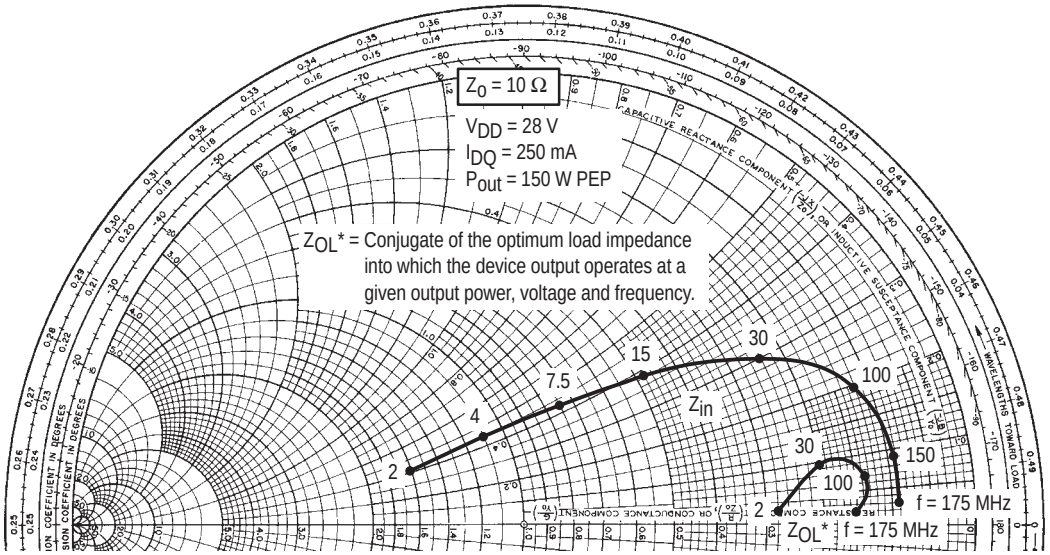
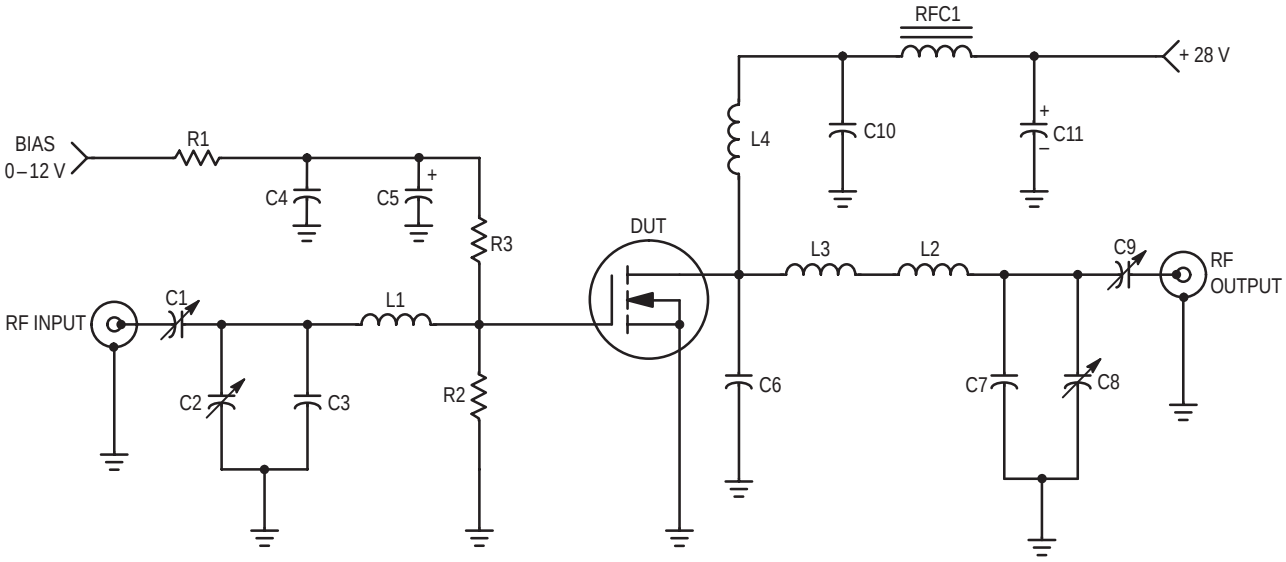


Figure 11. Input and Output Impedances



C1, C2, C8 — Arco 463 or equivalent
C3 — 25 pF, Unelco
C4 — 0.1 μF, Ceramic
C5 — 1.0 μF, 15 WV Tantalum
C6 — 25 pF, Unelco J101
C7 — 25 pF, Unelco J101
C9 — Arco 262 or equivalent
C10 — 0.05 μF, Ceramic
C11 — 15 μF, 35 WV Electrolytic

L1 — 3/4″, #18 AWG into Hairpin
L2 — Printed Line, 0.200″ x 0.500″
L3 — 7/8″, #16 AWG into Hairpin
L4 — 2 Turns, #16 AWG, 5/16 ID
RFC1 — 5.6 μH, Molded Choke
RFC2 — VK200–4B
R1 — 150 Ω, 1.0 W Carbon
R2 — 10 kΩ, 1/2 W Carbon
R3 — 120 Ω, 1/2 W Carbon

Figure 12. 175 MHz Test Circuit (Class AB)

Table 1. Common Source S–Parameters (V_{DS} = 24 V, I_D = 5 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.916	–177	4.23	83	0.008	32	0.876	–177
40	0.919	–178	3.23	76	0.009	39	0.885	178
50	0.922	–178	2.55	72	0.010	45	0.914	–180
60	0.923	–179	2.14	68	0.010	46	0.893	179
70	0.927	–179	1.77	63	0.011	48	0.878	179
80	0.929	–179	1.48	61	0.013	53	0.864	180
90	0.931	–180	1.28	60	0.015	61	0.850	180
100	0.934	–180	1.15	55	0.016	66	0.893	178
110	0.935	180	1.05	53	0.016	69	0.913	177
120	0.939	180	0.91	51	0.017	69	0.930	180
130	0.941	179	0.82	48	0.019	67	0.916	–180
140	0.943	179	0.76	46	0.022	68	0.926	179
150	0.946	179	0.67	42	0.024	70	0.940	177
160	0.946	179	0.63	40	0.025	73	0.915	178
170	0.948	178	0.57	39	0.024	78	0.891	178
180	0.949	178	0.52	37	0.026	75	0.906	178
190	0.950	178	0.49	37	0.028	74	0.899	176
200	0.950	177	0.45	35	0.030	78	0.915	176
210	0.938	177	0.43	31	0.043	108	0.966	174
220	0.958	178	0.39	33	0.029	61	0.972	175
230	0.961	177	0.36	27	0.038	77	1.033	174
240	0.960	177	0.36	28	0.036	76	0.943	174
250	0.961	176	0.32	30	0.038	77	0.912	175
260	0.962	176	0.30	31	0.040	76	0.918	174
270	0.961	176	0.27	30	0.044	77	0.933	171
280	0.963	176	0.26	30	0.045	79	0.943	172
290	0.964	175	0.25	25	0.045	78	0.940	172
300	0.965	175	0.26	27	0.047	77	0.930	172
310	0.966	175	0.25	27	0.051	78	0.977	172
320	0.964	175	0.24	26	0.053	75	0.947	171
330	0.966	174	0.22	21	0.056	75	0.946	170
340	0.967	174	0.23	26	0.056	75	0.944	170
350	0.967	174	0.22	24	0.058	78	0.946	171
360	0.965	174	0.21	28	0.062	74	0.956	171
370	0.966	174	0.20	28	0.048	61	0.968	170
380	0.968	173	0.20	27	0.053	74	0.931	168
390	0.970	173	0.18	31	0.063	74	0.962	168
400	0.970	173	0.17	26	0.071	79	0.965	172
410	0.970	172	0.17	29	0.076	78	0.982	169
420	0.971	172	0.17	30	0.076	76	0.956	167
430	0.970	172	0.15	29	0.070	76	0.912	165
440	0.970	171	0.13	32	0.074	76	0.933	167

Table 1. Common Source S–Parameters (V_{DS} = 24 V, I_D = 5 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
450	0.970	171	0.15	31	0.081	76	0.967	167
460	0.970	171	0.15	32	0.090	73	0.982	164
470	0.969	170	0.15	30	0.095	77	0.945	165
480	0.964	170	0.16	34	0.099	80	0.956	165
490	0.960	170	0.15	31	0.107	75	0.947	163
500	0.959	170	0.15	23	0.103	68	0.962	163

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 5 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.914	–177	4.60	82	0.007	25	0.874	–176
40	0.915	–178	3.51	76	0.008	26	0.879	–179
50	0.918	–178	2.76	71	0.009	34	0.888	–179
60	0.920	–178	2.32	67	0.010	45	0.881	179
70	0.924	–179	1.92	62	0.010	56	0.887	179
80	0.927	–179	1.61	60	0.009	62	0.899	–179
90	0.930	–179	1.39	58	0.010	61	0.874	–177
100	0.933	–180	1.23	53	0.012	57	0.875	–179
110	0.934	–180	1.13	51	0.015	63	0.884	179
120	0.938	180	0.98	49	0.017	73	0.926	179
130	0.940	180	0.88	46	0.018	81	0.959	–179
140	0.942	179	0.81	44	0.018	82	0.966	–179
150	0.945	179	0.71	40	0.018	77	0.961	–179
160	0.946	179	0.67	38	0.021	73	0.910	–179
170	0.948	178	0.61	37	0.023	77	0.871	179
180	0.950	178	0.54	35	0.026	78	0.912	178
190	0.950	178	0.52	34	0.029	76	0.959	177
200	0.952	178	0.47	33	0.034	64	0.971	178
210	0.949	177	0.46	28	0.067	17	1.023	–178
220	0.953	178	0.41	31	0.019	94	0.954	177
230	0.959	177	0.38	26	0.037	76	1.014	174
240	0.960	177	0.37	25	0.040	79	0.943	174
250	0.961	177	0.33	27	0.042	84	0.972	175
260	0.962	176	0.30	27	0.041	86	0.969	176
270	0.961	176	0.29	27	0.041	83	0.951	175
280	0.963	176	0.27	27	0.042	80	0.929	174
290	0.964	175	0.26	23	0.045	79	0.930	172
300	0.965	175	0.27	25	0.051	81	0.963	171
310	0.966	175	0.26	24	0.052	83	1.012	173
320	0.965	175	0.25	23	0.053	81	0.984	171
330	0.966	174	0.23	19	0.055	78	0.955	172
340	0.967	174	0.24	25	0.054	76	0.929	171
350	0.967	174	0.22	22	0.057	79	0.917	170

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 5 A) (contlinued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
360	0.967	174	0.21	26	0.060	91	0.978	169
370	0.967	174	0.20	26	0.084	89	1.030	167
380	0.969	173	0.20	23	0.081	82	0.994	170
390	0.970	173	0.19	29	0.072	80	0.963	170
400	0.970	173	0.17	25	0.069	80	0.951	172
410	0.970	172	0.17	27	0.072	71	0.985	167
420	0.972	172	0.16	28	0.078	68	0.970	165
430	0.971	172	0.15	27	0.084	70	0.953	165
440	0.971	171	0.13	29	0.086	74	0.949	168
450	0.971	171	0.15	29	0.087	79	0.962	167
460	0.970	171	0.15	32	0.081	72	0.976	164
470	0.969	170	0.15	29	0.079	65	0.969	164
480	0.964	170	0.16	32	0.081	57	0.972	165
490	0.959	170	0.15	29	0.081	54	0.976	165
500	0.958	170	0.15	21	0.086	58	0.953	167

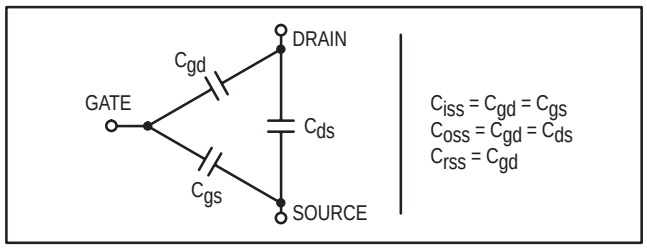
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 4 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of this device is essentially capacitor. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the device due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — This device does not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

DESIGN CONSIDERATIONS

The MRF141 is an RF Power, MOS, N–channel enhancement mode field–effect transistor (FET) designed for HF and VHF power amplifier applications.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power MOSFETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

The MRF141 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF141 was characterized at I_{DQ} = 250 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias sytem.

GAIN CONTROL

Power output of the MRF141 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

The RF MOSFET Line

RF Power Field-Effect Transistor

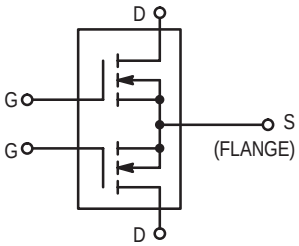
N–Channel Enhancement–Mode MOSFET

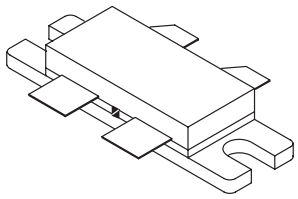
MRF141G

Designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 175 MHz, 28 V:
  Output Power — 300 W
  Gain — 12 dB (14 dB Typ)
  Efficiency — 50%
- Low Thermal Resistance — 0.35°C/W
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability
- S–Parameters Available for Download into Frequency Domain Simulators. See http://motorola.com/sps/rf/designtds/

300 W, 28 V, 175 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET





CASE 375–04, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage	V_{DGO}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	32	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	500 2.85	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

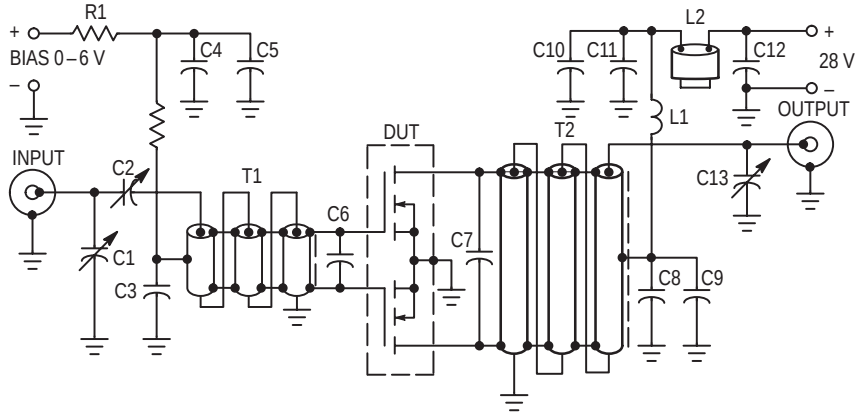
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.35	°C/W

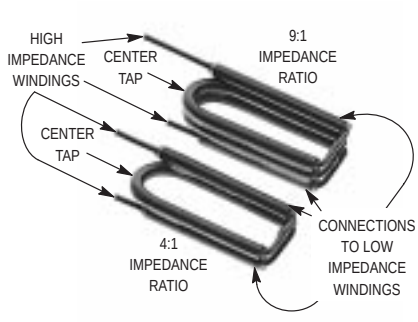
NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	0.1	0.9	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	5.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	350	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	420	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	35	—	pF
FUNCTIONAL TESTS (2)					
Common Source Amplifier Power Gain (V_{DD} = 28 V, P_{out} = 300 W, I_{DQ} = 500 mA, f = 175 MHz)	G_{ps}	12	14	—	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 300 W, f = 175 MHz, I_D (Max) = 21.4 A)	η	45	55	—	%
Load Mismatch (V_{DD} = 28 V, P_{out} = 300 W, I_{DQ} = 500 mA, f = 175 MHz, VSWR 5:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each side measured separately.
2. Measured in push–pull configuration.





C1 — Arco 402, 1.5–20 pF
C2 — Arco 406, 15–115 pF
C3, C4, C8, C9, C10 — 1000 pF Chip
C5, C11 — 0.1 μF Chip
C6 — 330 pF Chip
C7 — 200 pF and 180 pF Chips in Parallel
C12 — 0.47 μF Ceramic Chip, Kemet 1215 or Equivalent
C13 — Arco 403, 3.0–35 pF
L1 — 10 Turns AWG #16 Enameled Wire, Close Wound, 1/4″ I.D.
L2 — Ferrite Beads of Suitable Material for 1.5–2.0 μH Total Inductance
R1 — 100 Ohms, 1/2 W
R2 — 1.0 kOhm, 1/2 W

T1 — 9:1 RF Transformer. Can be made of 15–18 Ohms Semirigid Co–Ax, 62–90 Mils O.D.
T2 — 1:9 RF Transformer. Can be made of 15–18 Ohms Semirigid Co–Ax, 70–90 Mils O.D.

Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, ε_r = 5

NOTE: For stability, the input transformer T1 must be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

See pictures for construction details.

Unless Otherwise Noted, All Chip Capacitors are ATC Type 100 or Equivalent.

Figure 1. 175 MHz Test Circuit

TYPICAL CHARACTERISTICS

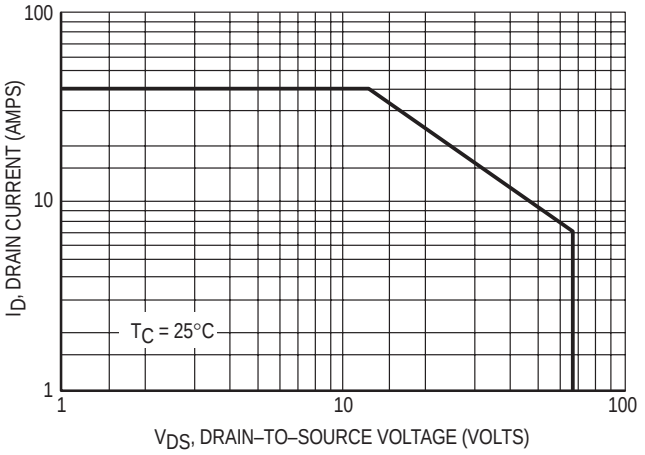


Figure 2. DC Safe Operating Area

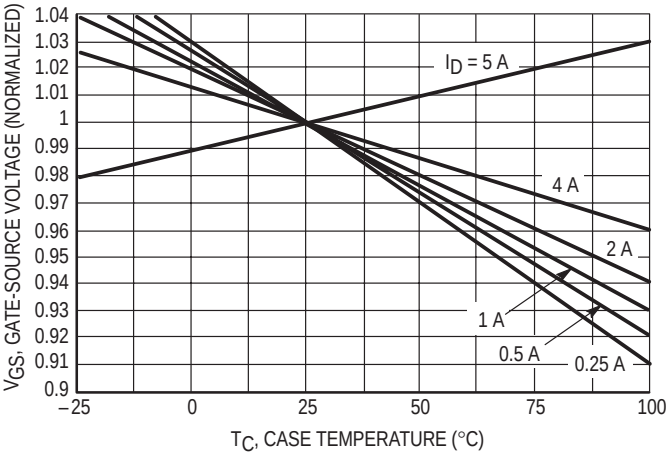
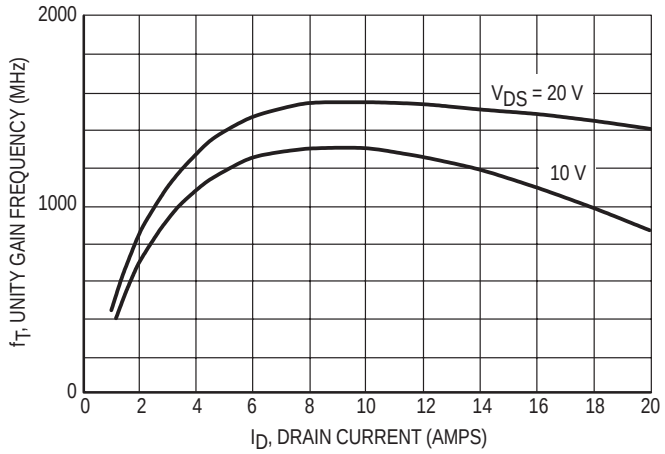


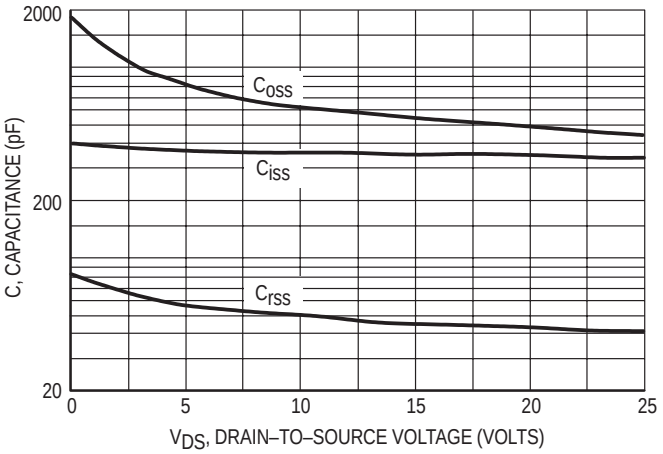
Figure 3. Gate–Source Voltage versus Case Temperature

TYPICAL CHARACTERISTICS



NOTE: Data shown applies to each half of MRF141G.

Figure 4. Common Source Unity Gain Frequency versus Drain Current



NOTE: Data shown applies to each half of MRF141G.

Figure 5. Capacitance versus Drain–Source Voltage

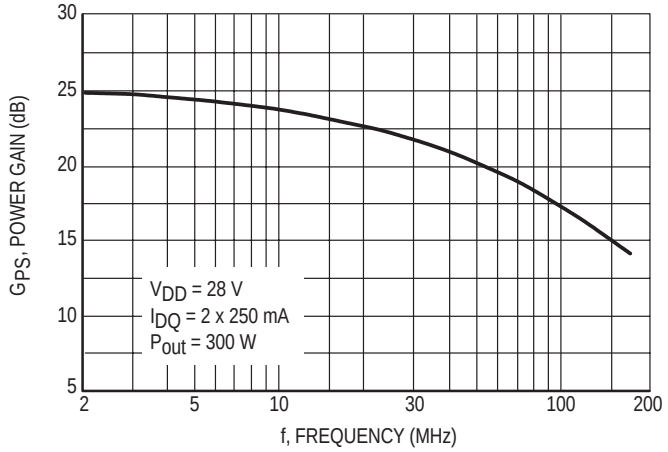


Figure 6. Power Gain versus Frequency

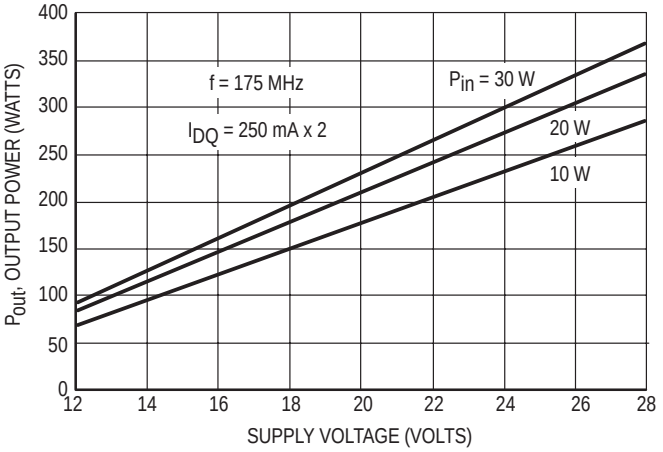
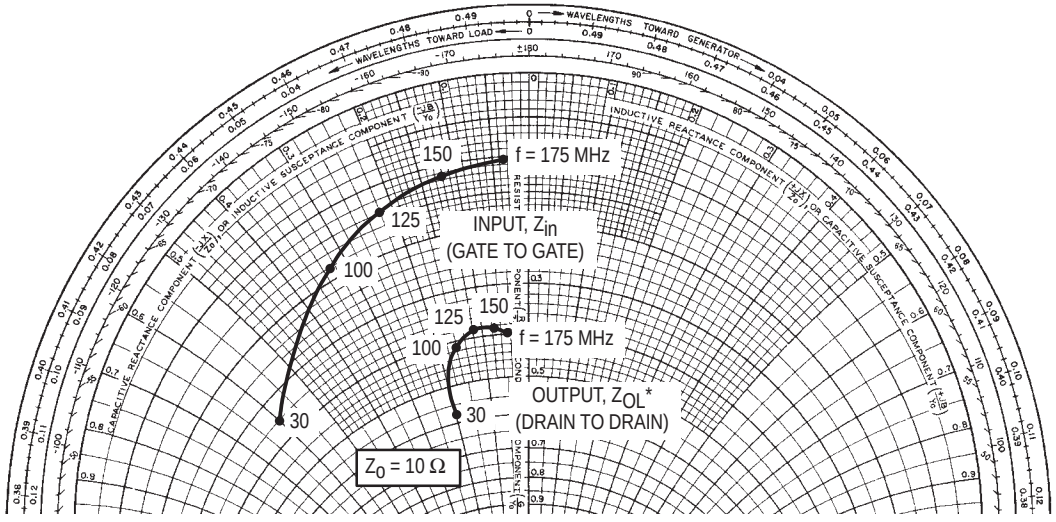


Figure 7. Output Power versus Supply Voltage



Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 8. Input and Output Impedances

NOTE: S–Parameter data represents measurements taken from one chip only.

Table 1. Common Source S–Parameters (V_{DS} = 24 V, I_D = 0.57 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.845	–174	4.88	78	0.014	–5	0.939	–174
40	0.867	–174	3.23	66	0.013	–14	0.856	–172
50	0.876	–174	2.62	62	0.013	–17	0.868	–175
60	0.883	–174	2.12	59	0.012	–15	0.938	–176
70	0.890	–175	1.85	58	0.012	–12	1.036	–177
80	0.899	–175	1.57	56	0.011	–10	1.110	–177
90	0.909	–175	1.36	50	0.010	–11	1.190	–176
100	0.920	–176	1.13	43	0.009	–13	1.160	–176
110	0.930	–176	0.95	37	0.007	–16	1.100	–177
120	0.938	–176	0.78	33	0.007	–11	1.010	–175
130	0.944	–176	0.67	31	0.006	–3	0.954	–176
140	0.948	–177	0.60	31	0.006	10	0.964	–177
150	0.951	–177	0.56	32	0.005	23	1.023	–178
160	0.954	–178	0.52	32	0.005	31	1.130	–179
170	0.958	–178	0.48	29	0.006	37	1.190	–178
180	0.962	–178	0.45	24	0.006	39	1.260	–179
190	0.965	–179	0.40	17	0.007	41	1.200	180
200	0.968	–179	0.34	15	0.008	49	1.090	–179
210	0.970	–179	0.30	15	0.008	60	0.980	–178
220	0.972	–180	0.27	15	0.008	68	0.960	–177
230	0.973	–180	0.25	17	0.008	68	1.045	–179
240	0.974	180	0.24	20	0.009	67	1.030	179
250	0.975	180	0.24	19	0.011	68	1.100	179
260	0.977	179	0.21	17	0.012	69	1.200	179
270	0.978	179	0.22	13	0.013	72	1.210	177
280	0.979	179	0.19	13	0.012	72	1.170	177
290	0.979	178	0.17	1	0.012	68	1.040	180
300	0.980	178	0.16	8	0.013	65	0.998	179
310	0.980	178	0.16	13	0.015	70	0.977	179
320	0.981	178	0.16	15	0.017	76	0.979	178
330	0.982	177	0.13	10	0.017	83	1.033	178
340	0.982	177	0.15	19	0.016	81	1.110	176
350	0.982	177	0.13	16	0.016	73	1.140	177
360	0.983	177	0.13	8	0.020	63	1.150	177
370	0.982	176	0.10	6	0.023	65	1.120	176
380	0.982	176	0.10	7	0.023	72	1.050	177
390	0.982	176	0.10	10	0.021	81	0.993	177
400	0.982	176	0.09	14	0.018	83	0.959	179
410	0.983	175	0.10	12	0.020	71	1.040	176
420	0.983	175	0.09	16	0.025	65	1.090	174
430	0.984	175	0.09	15	0.028	70	1.100	174

Table 1. Common Source S–Parameters (V_{DS} = 24 V, I_D = 0.57 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
440	0.983	174	0.09	12	0.028	77	1.100	175
450	0.983	174	0.09	13	0.025	82	1.090	176
460	0.983	174	0.07	14	0.022	66	1.080	174
470	0.983	174	0.07	13	0.024	56	0.992	175
480	0.983	174	0.07	16	0.032	60	0.970	175
490	0.984	173	0.07	13	0.036	74	0.996	174
500	0.984	173	0.07	18	0.035	85	1.040	174

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 0.65 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.849	–174	5.41	79	0.013	–6	0.934	–174
40	0.869	–174	3.59	67	0.013	–16	0.849	–172
50	0.878	–174	2.91	62	0.012	–17	0.859	–174
60	0.884	–174	2.36	60	0.011	–13	0.928	–176
70	0.890	–175	2.06	59	0.010	–11	1.029	–177
80	0.899	–175	1.75	56	0.009	–14	1.110	–177
90	0.910	–176	1.52	51	0.009	–18	1.190	–175
100	0.920	–176	1.26	43	0.009	–19	1.150	–175
110	0.929	–176	1.07	37	0.008	–15	1.100	–177
120	0.937	–176	0.88	34	0.006	–4	1.000	–175
130	0.943	–176	0.75	32	0.004	5	0.953	–176
140	0.947	–177	0.67	32	0.003	6	0.966	–177
150	0.950	–177	0.63	32	0.004	6	1.030	–178
160	0.953	–178	0.58	32	0.005	18	1.120	–178
170	0.957	–178	0.54	29	0.006	36	1.180	–178
180	0.961	–178	0.51	24	0.006	53	1.250	–179
190	0.964	–179	0.45	18	0.006	65	1.200	180
200	0.967	–179	0.39	15	0.005	69	1.110	–179
210	0.969	–179	0.35	15	0.005	63	1.030	–178
220	0.971	–180	0.31	15	0.006	59	0.975	–177
230	0.972	–180	0.28	17	0.009	66	1.040	–179
240	0.973	180	0.27	20	0.010	78	1.030	179
250	0.974	180	0.27	19	0.010	88	1.090	180
260	0.976	179	0.24	17	0.009	85	1.200	179
270	0.977	179	0.24	12	0.010	73	1.220	177
280	0.978	179	0.21	12	0.011	66	1.170	178
290	0.979	178	0.19	2	0.013	70	1.040	180
300	0.979	178	0.18	8	0.013	78	1.000	179
310	0.979	178	0.17	13	0.013	89	0.975	179
320	0.980	178	0.17	14	0.012	88	0.988	177

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 0.65 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
330	0.981	177	0.14	9	0.013	80	1.050	177
340	0.982	177	0.16	17	0.015	75	1.110	176
350	0.982	177	0.15	14	0.018	80	1.130	177
360	0.982	177	0.14	8	0.018	82	1.160	177
370	0.982	176	0.12	6	0.017	82	1.120	176
380	0.982	176	0.12	6	0.015	77	1.060	177
390	0.982	176	0.11	9	0.016	72	0.992	177
400	0.982	176	0.10	13	0.018	78	0.958	179
410	0.983	175	0.11	11	0.021	83	1.050	176
420	0.983	175	0.10	15	0.021	87	1.070	175
430	0.983	175	0.10	14	0.019	85	1.090	175
440	0.983	174	0.10	10	0.018	76	1.130	175
450	0.983	174	0.10	9	0.021	71	1.130	176
460	0.982	174	0.08	10	0.024	70	1.080	174
470	0.983	174	0.08	11	0.023	82	0.996	175
480	0.983	174	0.08	15	0.021	90	0.974	176
490	0.983	173	0.08	12	0.019	87	0.971	175
500	0.983	173	0.08	17	0.021	78	1.010	174

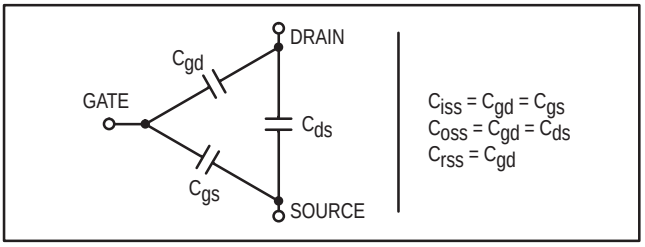
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 4 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of this device is essentially capacitor. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the device due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — This device does not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

DESIGN CONSIDERATIONS

The MRF141G is an RF Power, MOS, N–channel enhancement mode field–effect transistor (FET) designed for HF and VHF power amplifier applications.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power MOSFETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

The MRF141G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF141G was characterized at I_{DQ} = 250 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF141G may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

The RF MOSFET Line

RF Power Field-Effect Transistor

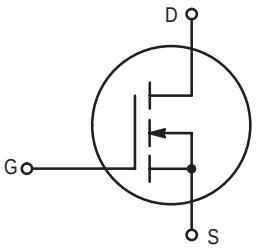
N–Channel Enhancement–Mode

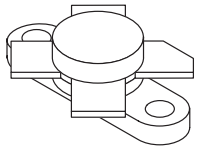
MRF148A

Designed for power amplifier applications in industrial, commercial and amateur radio equipment to 175 MHz.

- Superior High Order IMD
- Specified 50 Volts, 30 MHz Characteristics
  Output Power = 30 Watts
  Power Gain = 18 dB (Typ)
  Efficiency = 40% (Typ)
- $IMD_{(d3)}$ (30 W PEP) — –35 dB (Typ)
- $IMD_{(d11)}$ (30 W PEP) — –60 dB (Typ)
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Lower Reverse Transfer Capacitance (3.0 pF Typical)

30 W, to 175 MHz
N–CHANNEL MOS
LINEAR RF POWER
FET





CASE 211–07, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	120	Vdc
Drain–Gate Voltage	V_{DGO}	120	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	6.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.66	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

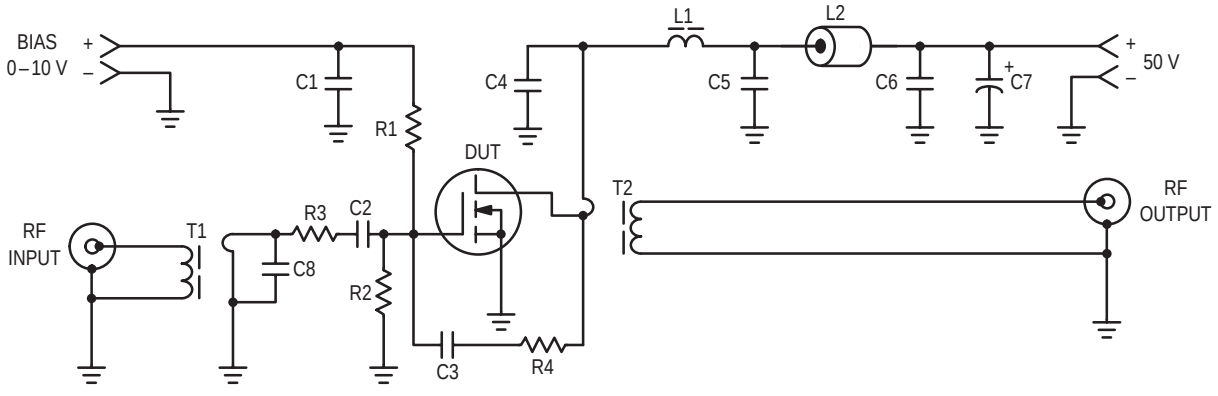
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 mA)	$V_{GS(th)}$	1.0	2.5	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 2.5 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	0.8	1.2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	62	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	35	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	3.0	—	pF
FUNCTIONAL TESTS (SSB)					
Common Source Amplifier Power Gain (30 MHz) (V_{DD} = 50 V, P_{out} = 30 W (PEP), I_{DQ} = 100 mA) (175 MHz)	G_{ps}	— —	18 15	— —	dB
Drain Efficiency (30 W PEP) (V_{DD} = 50 V, f = 30 MHz, I_{DQ} = 100 mA) (30 W CW)	η	— —	40 50	— —	%
Intermodulation Distortion (V_{DD} = 50 V, P_{out} = 30 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 100 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	–35 –60	— —	dB
Load Mismatch (V_{DD} = 50 V, P_{out} = 30 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{DD} = 50 V, P_{out} = 10 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 1.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9–13)}$	— — —	20 –50 –70	— — —	dB

NOTE:
1. To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C1, C2, C3, C4, C5, C6 — 0.1 μF Ceramic Chip or Equivalent
C7 — 10 μF, 100 V Electrolytic
C8 — 100 pF Dipped Mica
L1 — VK200 20/4B Ferrite Choke or Equivalent (3.0 μH)
L2 — Ferrite Bead(s), 2.0 μH
R1, R2 — 200 Ω, 1/2 W Carbon
R3 — 4.7 Ω, 1/2 W Carbon
R4 — 470 Ω, 1.0 W Carbon
T1 — 4:1 Impedance Transformer
T2 — 1:2 Impedance Transformer

Figure 1. 2.0 to 50 MHz Broadband Test Circuit

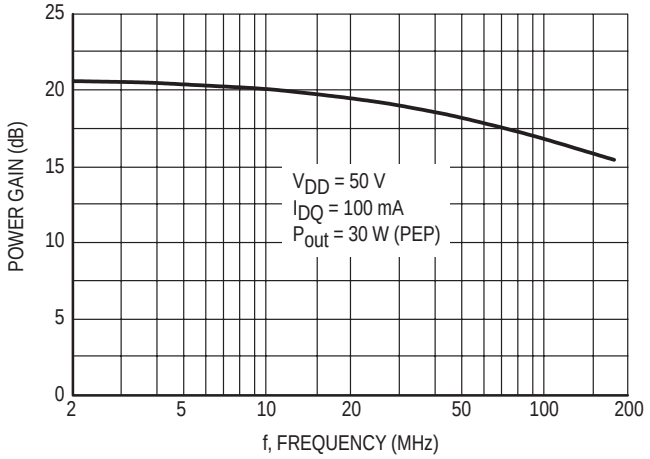


Figure 2. Power Gain versus Frequency

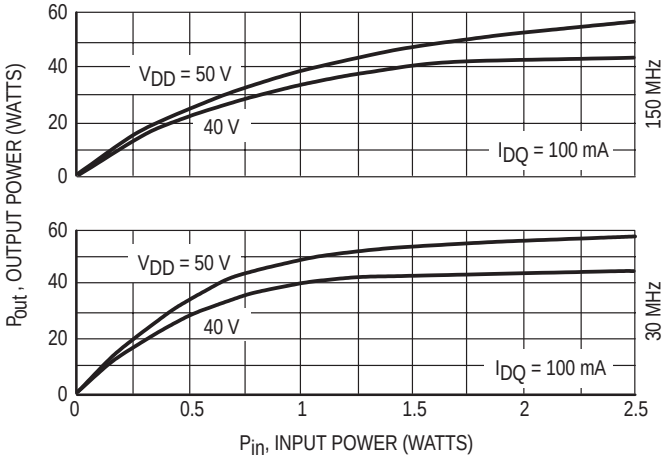


Figure 3. Output Power versus Input Power

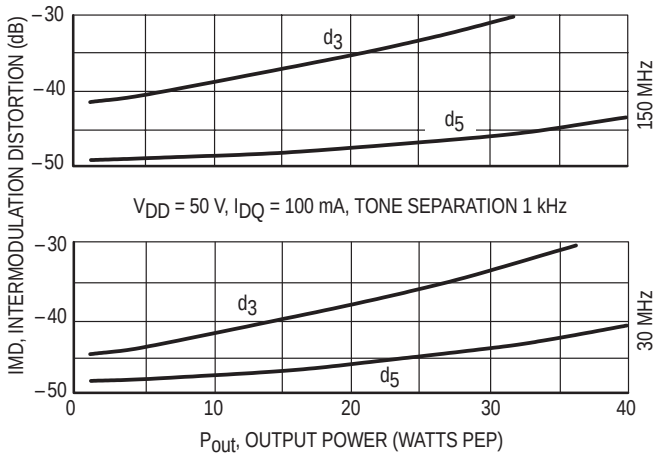


Figure 4. IMD versus P_{out}

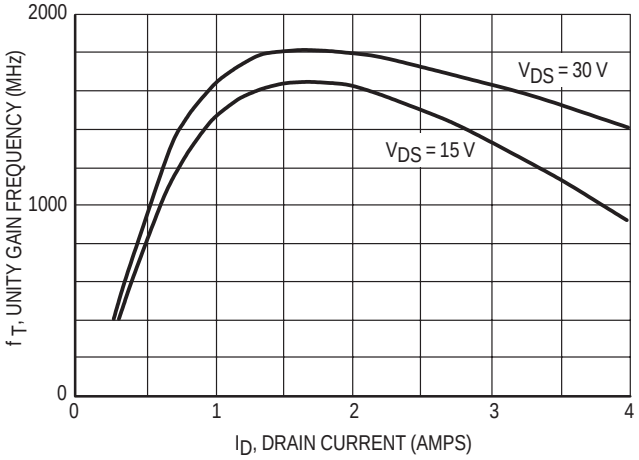
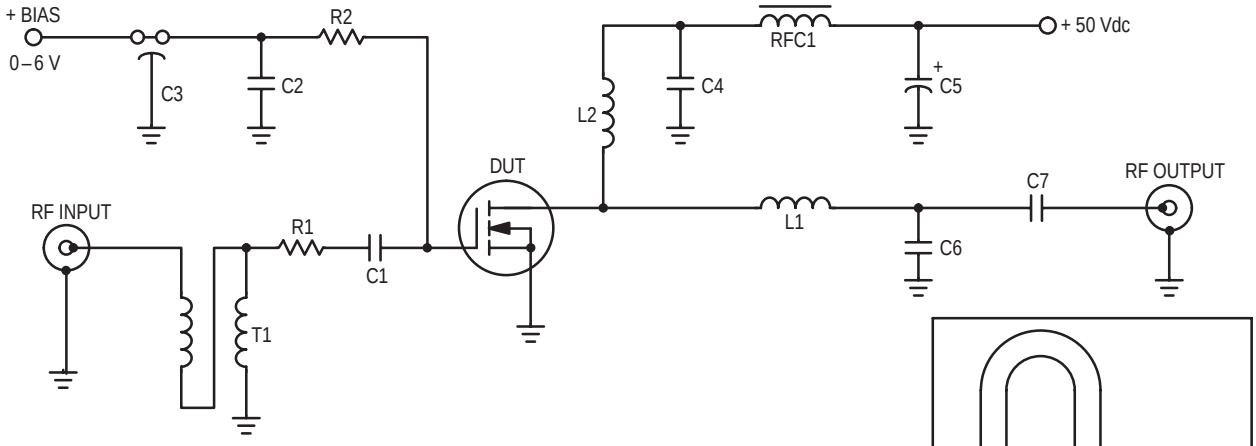


Figure 5. Common Source Unity Gain Frequency versus Drain Current



C1 — 91 pF Unelco Type MCM 01/010
C2, C4 — 0.1 μF Erie Red Cap
C3 — Allen Bradley 680 pF Feed Thru
C5 — 1.0 μF, 50 Vdc Electrolytic
C6 — 15 pF Unelco Type J101
C7 — 24 pF Unelco Type MCM 01/010
L1 — 2 Turns #18 AWG, 5/16″ ID
L2 — 4 Turns #18 AWG, 5/16″ ID
R1 — 1.0 Ohm, 1/4 W Carbon
R2 — 2000 Ohm, 1/4 W Carbon
RFC1 — VK200 21/4B
T1 — 4:1 Transformer, 1.75″ Subminiature Coaxial Cable

T1 — 4:1 Impedance Ratio Transformer, Line Impedance = 25 Ω

Figure 6. 150 MHz Test Circuit

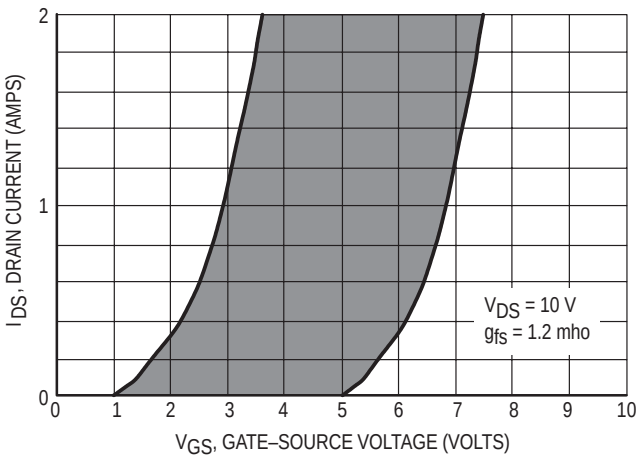


Figure 7. Gate Voltage versus Drain Current

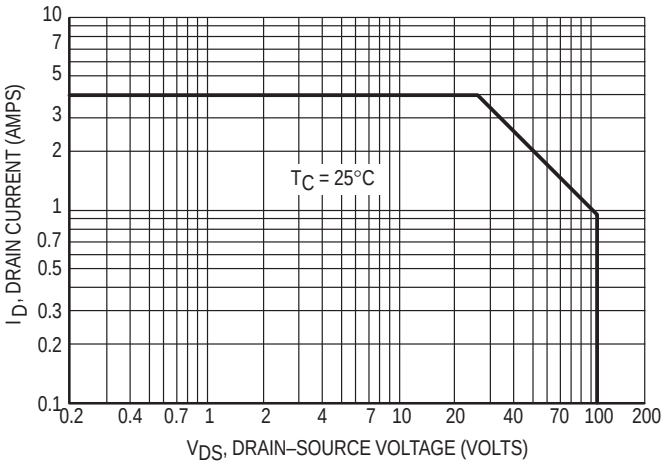
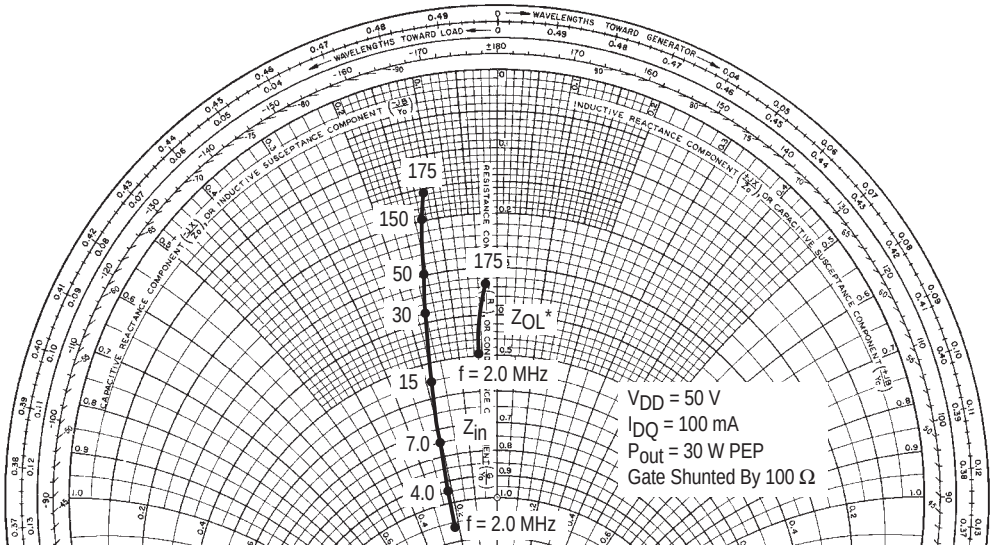


Figure 8. DC Safe Operating Area (SOA)



Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 9. Impedance Coordinates — 50 Ohm Characteristic Impedance

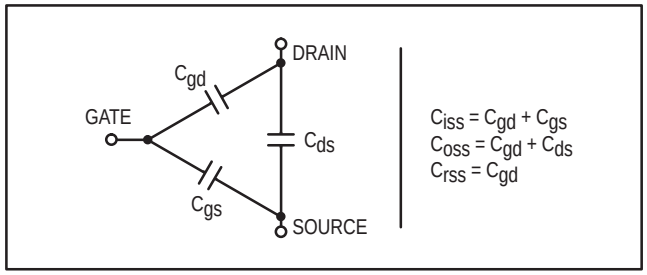
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

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2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

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GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

The RF MOSFET Line

RF Power Field-Effect Transistor

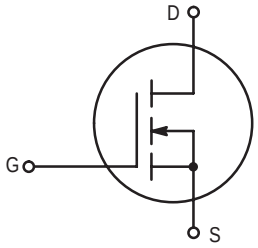
N–Channel Enhancement–Mode

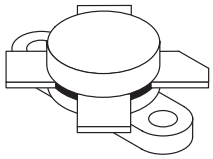
MRF150

150 W, to 150 MHz
N–CHANNEL MOS
LINEAR RF POWER
FET

Designed primarily for linear large–signal output stages up to 150 MHz frequency range.

- Specified 50 Volts, 30 MHz Characteristics
  Output Power = 150 Watts
  Power Gain = 17 dB (Typ)
  Efficiency = 45% (Typ)
- Superior High Order IMD
- $IMD_{(d3)}$ (150 W PEP) — –32 dB (Typ)
- $IMD_{(d11)}$ (150 W PEP) — –60 dB (Typ)
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- S–Parameters Available for Download into Frequency Domain Simulators. See http://motorola.com/sps/rf/designtds/





CASE 211–11, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Drain–Gate Voltage	V_{DGO}	125	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.71	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

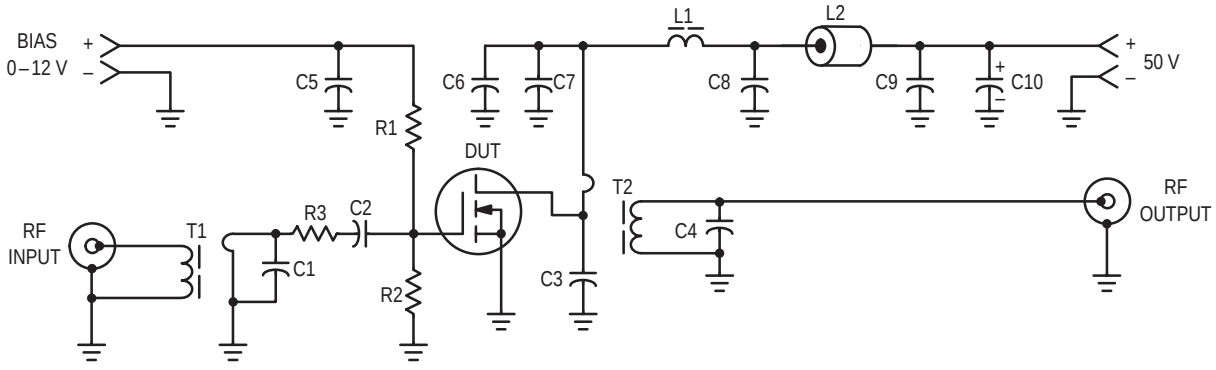
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	4.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	400	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	240	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	40	—	pF
FUNCTIONAL TESTS (SSB)					
Common Source Amplifier Power Gain f = 30 MHz (V_{DD} = 50 V, P_{out} = 150 W (PEP), I_{DQ} = 250 mA) f = 150 MHz	G_{ps}	— —	17 8.0	— —	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_D (Max) = 3.75 A)	η	—	45	—	%
Intermodulation Distortion (1) (V_{DD} = 50 V, P_{out} = 150 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 250 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	–32 –60	— —	dB
Load Mismatch (V_{DD} = 50 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 250 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{DD} = 50 V, P_{out} = 50 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 3.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9-13)}$	— — —	20 –50 –75	— — —	dB

NOTE:
1. To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C1 — 470 pF Dipped Mica
C2, C5, C6, C7, C8, C9 — 0.1 μF Ceramic Chip or Monolythic with Short Leads
C3 — 200 pF Unencapsulated Mica or Dipped Mica with Short Leads
C4 — 15 pF Unencapsulated Mica or Dipped Mica with Short Leads
C10 — 10 μF/100 V Electrolytic
L1 — VK200/4B Ferrite Choke or Equivalent, 3.0 μH
L2 — Ferrite Bead(s), 2.0 μH
R1, R2 — 51 Ω/1.0 W Carbon
R3 — 3.3 Ω/1.0 W Carbon (or 2.0 x 6.8 Ω/1/2 W in Parallel
T1 — 9:1 Broadband Transformer
T2 — 1:9 Broadband Transformer

Figure 1. 30 MHz Test Circuit (Class AB)

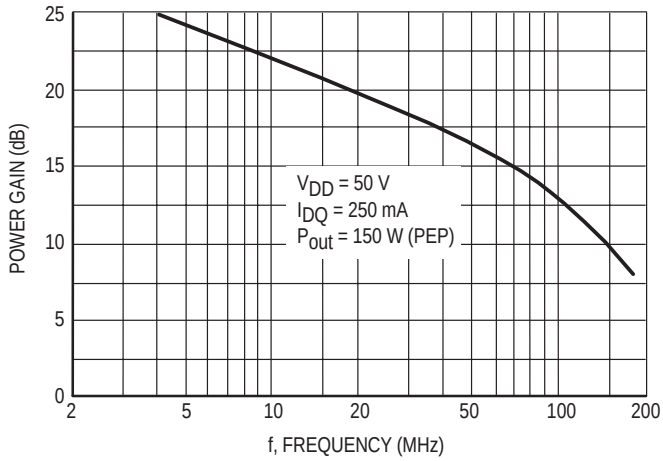


Figure 2. Power Gain versus Frequency

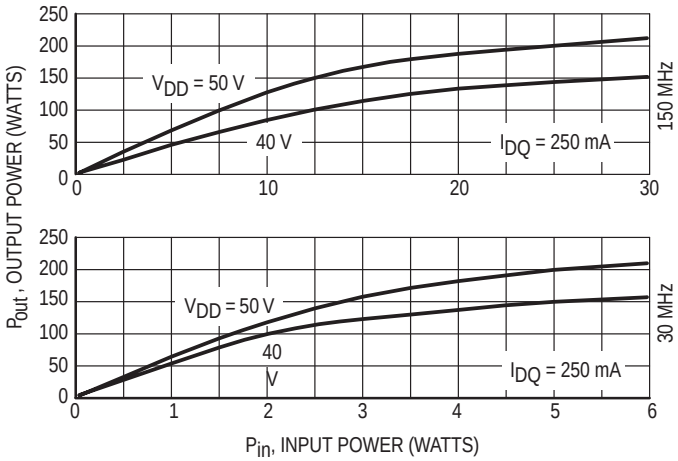


Figure 3. Output Power versus Input Power

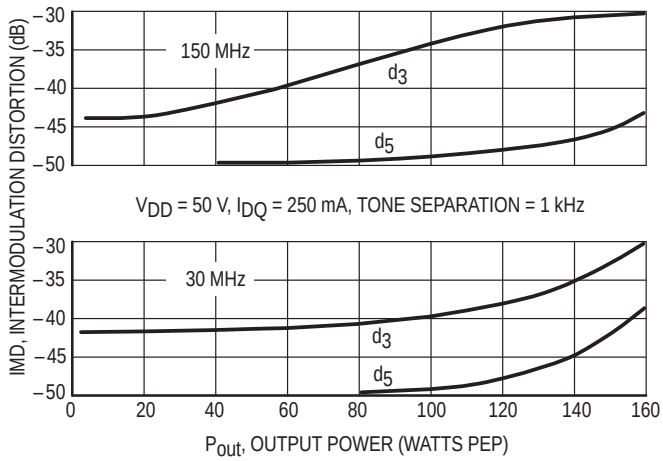


Figure 4. IMD versus P_{out}

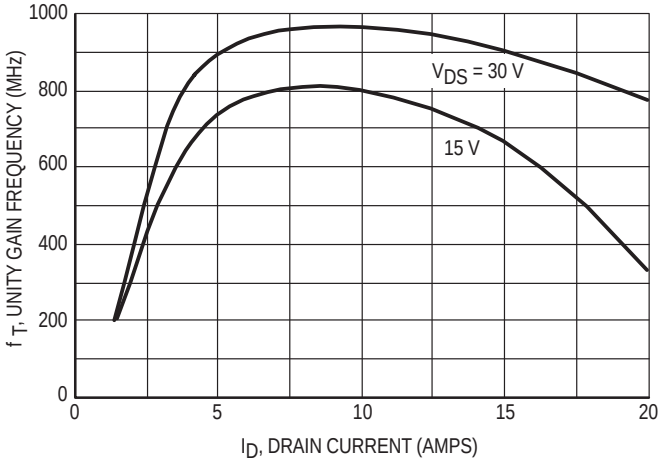


Figure 5. Common Source Unity Gain Frequency versus Drain Current

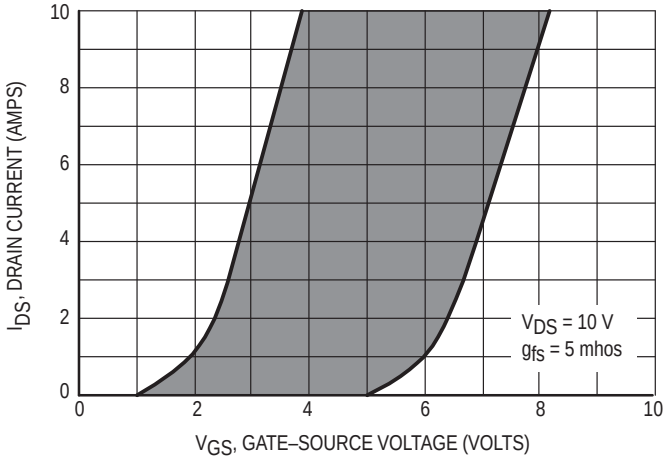
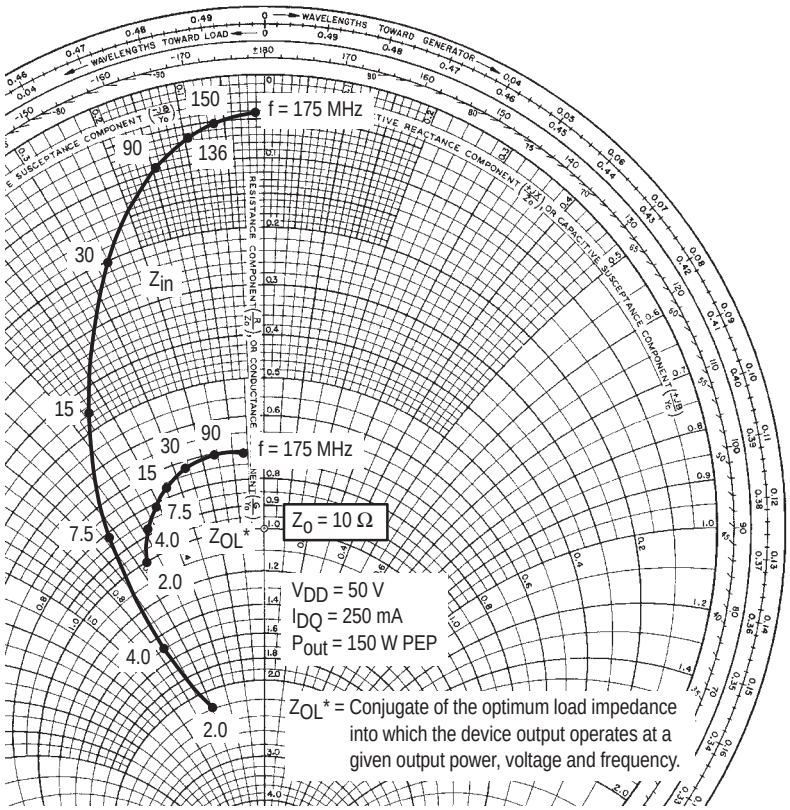
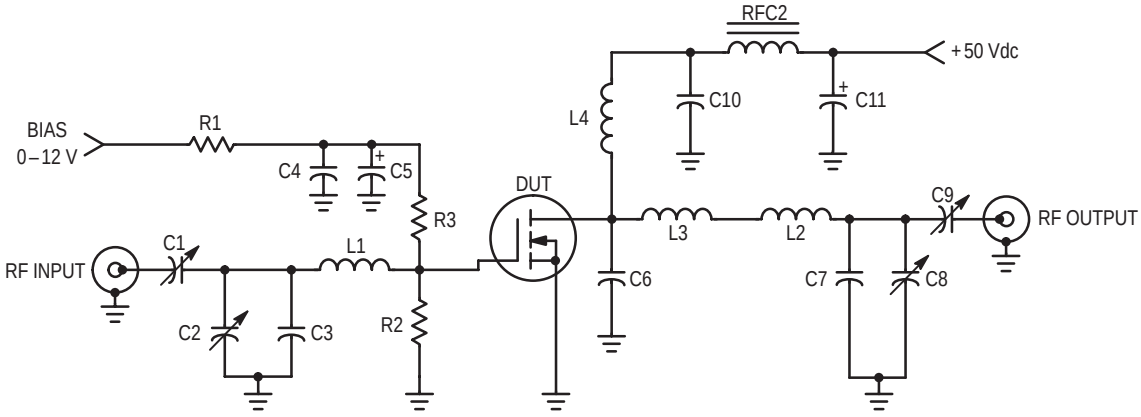


Figure 6. Gate Voltage versus Drain Current



NOTE: Gate Shunted by 25 Ohms.

Figure 7. Series Equivalent Impedance



C1, C2, C8 — Arco 463 or equivalent
C3 — 25 pF, Unelco
C4 — 0.1 μF, Ceramic
C5 — 1.0 μF, 15 WV Tantalum
C6 — 25 pF, Unelco J101
C7 — 25 pF, Unelco J101
C9 — Arco 262 or equivalent
C10 — 0.05 μF, Ceramic
C11 — 15 μF, 60 WV Electrolytic
L1 — 3/4″, 18 AWG into Hairpin
L2 — Printed Line, 0.200″ x 0.500″
L3 — 1″, #16 AWG into Hairpin
L4 — 2 Turns #16 AWG, 5/16 ID
RFC1 — 5.6 μH, Choke
RFC2 — VK200–4B
R1 — 150 Ω, 1.0 W Carbon
R2 — 10 kΩ, 1/2 W Carbon
R3 — 120 Ω, 1/2 W Carbon

Figure 8. 150 MHz Test Circuit (Class AB)

Table 1. Common Source S–Parameters (V_{DS} = 50 V, I_D = 2 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.936	–179	4.13	84	0.011	22	0.844	–176
40	0.936	–179	3.16	79	0.012	23	0.842	–180
50	0.936	–180	2.52	75	0.013	29	0.855	–179
60	0.937	180	2.13	72	0.014	36	0.854	179
70	0.939	179	1.81	68	0.013	42	0.870	179
80	0.940	179	1.53	67	0.013	45	0.868	–179
90	0.941	179	1.34	65	0.014	46	0.855	–178
100	0.942	179	1.21	60	0.016	46	0.874	180
110	0.942	179	1.11	58	0.018	52	0.875	178
120	0.945	178	0.99	56	0.019	61	0.893	180
130	0.946	178	0.88	53	0.019	67	0.902	–179
140	0.947	178	0.83	52	0.019	68	0.919	–179
150	0.949	177	0.74	49	0.020	63	0.910	–179
160	0.949	177	0.71	46	0.024	62	0.889	–180
170	0.952	177	0.65	44	0.026	68	0.878	179
180	0.953	177	0.59	42	0.029	72	0.921	179
190	0.954	176	0.57	41	0.029	75	0.949	178
200	0.956	176	0.52	39	0.028	74	0.929	178
210	0.955	176	0.51	38	0.030	71	0.934	179
220	0.957	175	0.49	35	0.034	70	0.918	177
230	0.960	175	0.43	32	0.039	71	0.977	175
240	0.959	175	0.42	32	0.040	74	0.941	175
250	0.961	175	0.39	32	0.040	77	0.944	176
260	0.961	175	0.36	31	0.040	76	0.948	177
270	0.960	174	0.35	29	0.043	74	0.947	175
280	0.963	174	0.34	29	0.046	73	0.929	174
290	0.963	174	0.32	25	0.048	74	0.918	172
300	0.965	173	0.32	28	0.051	78	0.925	174
310	0.966	173	0.29	27	0.052	79	0.953	174
320	0.963	173	0.28	26	0.054	76	0.954	172
330	0.965	172	0.26	22	0.057	74	0.914	171
340	0.966	172	0.26	27	0.058	72	0.925	171
350	0.965	172	0.26	25	0.062	75	0.934	171
360	0.968	171	0.25	25	0.065	74	0.979	171
370	0.967	171	0.23	24	0.064	73	0.993	168
380	0.967	171	0.24	22	0.068	74	0.952	172
390	0.969	170	0.22	26	0.069	74	0.942	170
400	0.968	170	0.21	23	0.072	76	0.936	172
410	0.968	170	0.21	24	0.076	73	0.984	168
420	0.970	169	0.20	25	0.078	71	0.977	167
430	0.969	169	0.18	25	0.082	72	0.959	168
440	0.970	169	0.19	25	0.082	73	0.953	169

Table 1. Common Source S–Parameters (V_{DS} = 50 V, I_D = 2 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
450	0.971	168	0.19	24	0.085	75	0.960	168
460	0.972	168	0.17	26	0.086	70	0.960	164
470	0.972	168	0.17	23	0.087	70	0.952	165
480	0.969	167	0.18	26	0.093	70	0.977	166
490	0.969	167	0.18	25	0.099	71	0.966	166
500	0.969	166	0.17	26	0.101	71	0.972	164

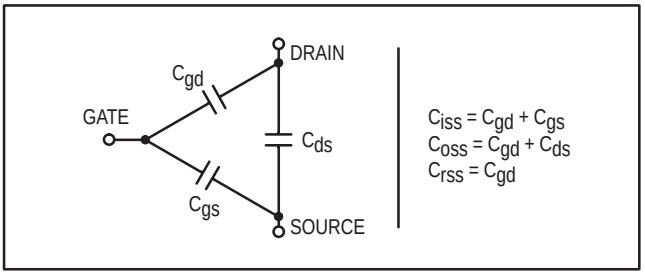
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

The RF MOSFET Line

RF Power Field-Effect Transistor

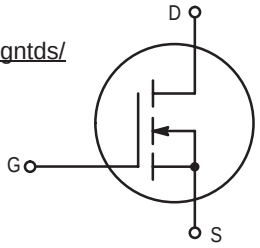
N–Channel Enhancement–Mode MOSFET

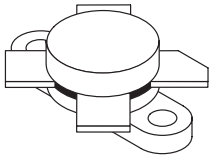
MRF151

Designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 30 MHz, 50 V:
  Output Power — 150 W
  Gain — 18 dB (22 dB Typ)
  Efficiency — 40%
- Typical Performance at 175 MHz, 50 V:
  Output Power — 150 W
  Gain — 13 dB
- Low Thermal Resistance
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability
- S–Parameters Available for Download into Frequency Domain Simulators. See http://motorola.com/sps/rf/designtds/

150 W, 50 V, 175 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET





CASE 211–11, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Drain–Gate Voltage	V_{DGO}	125	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.71	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

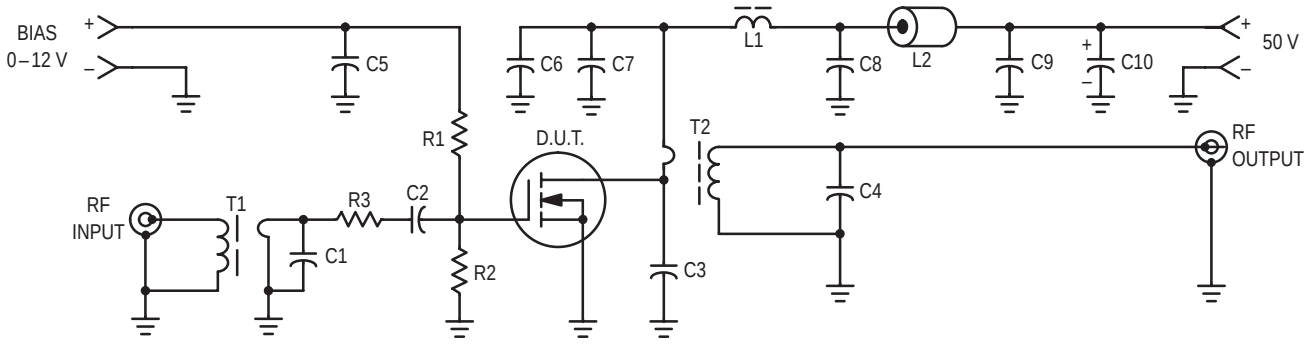
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

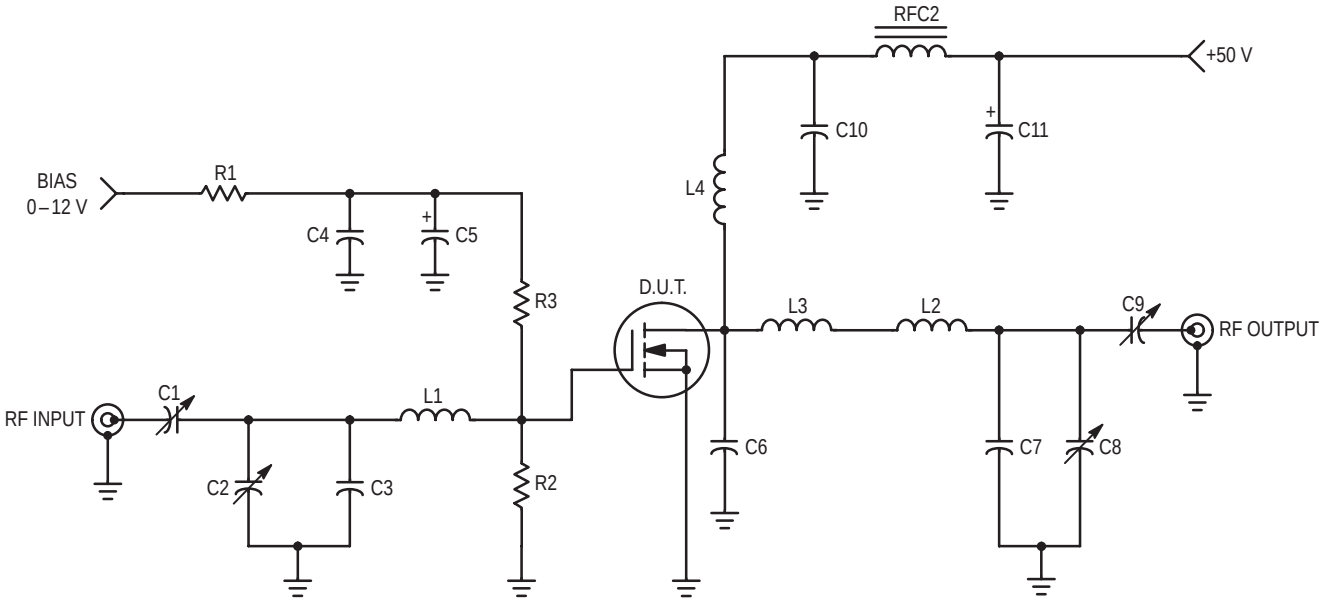
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	5.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	350	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	220	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	15	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain, f = 30; 30.001 MHz (V_{DD} = 50 V, P_{out} = 150 W (PEP), I_{DQ} = 250 mA) f = 175 MHz	G_{ps}	18 —	22 13	— —	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_D (Max) = 3.75 A)	η	40	45	—	%
Intermodulation Distortion (1) (V_{DD} = 50 V, P_{out} = 150 W (PEP), f = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 250 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	–32 –60	–30 —	dB
Load Mismatch (V_{DD} = 50 V, P_{out} = 150 W (PEP), f1 = 30; 30.001 MHz, I_{DQ} = 250 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{DD} = 50 V, P_{out} = 50 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 3.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9-13)}$	— — —	23 –50 –75	— — —	dB

NOTE:
1. To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C1 — 470 pF Dipped Mica
C2, C5, C6, C7, C8, C9 — 0.1 μF Ceramic Chip or Monolythic with Short Leads
C3 — 200 pF Unencapsulated Mica or Dipped Mica with Short Leads
C4 — 15 pF Unencapsulated Mica or Dipped Mica with Short Leads
C10 — 10 μF/100 V Electrolytic
L1 — VK200/4B Ferrite Choke or Equivalent, 3.0 μH
L2 — Ferrite Bead(s), 2.0 μH
R1, R2 — 51 Ω/1.0 W Carbon
R3 — 3.3 Ω/1.0 W Carbon (or 2.0 x 6.8 Ω/1/2 W in Parallel)
T1 — 9:1 Broadband Transformer
T2 — 1:9 Broadband Transformer
Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, ε_r = 5

Figure 1. 30 MHz Test Circuit



C1, C2, C8 — Arco 463 or equivalent
C3 — 25 pF, Unelco
C4 — 0.1 μF, Ceramic
C5 — 1.0 μF, 15 WV Tantalum
C6 — 15 pF, Unelco J101
C7 — 25 pF, Unelco J101
C9 — Arco 262 or equivalent
C10 — 0.05 μF, Ceramic
C11 — 15 μF, 60 WV Electrolytic
D1 — 1N5347 Zener Diode

L1 — 3/4″, #18 AWG into Hairpin
L2 — Printed Line, 0.200″ x 0.500″
L3 — 1″, #16 AWG into Hairpin
L4 — 2 Turns, #16 AWG, 5/16 ID
RFC1 — 5.6 μH, Choke
RFC2 — VK200–4B
R1 — 150 Ω, 1.0 W Carbon
R2 — 10 kΩ, 1/2 W Carbon
R3 — 120 Ω, 1/2 W Carbon
Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, ε_r = 5.0

Figure 2. 175 MHz Test Circuit

TYPICAL CHARACTERISTICS

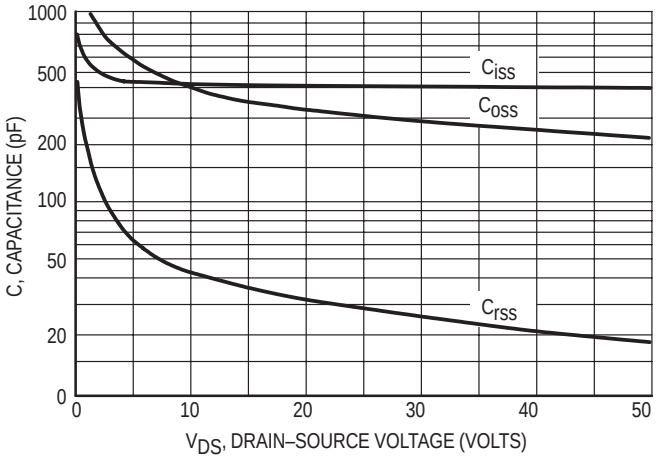


Figure 3. Capacitance versus Drain–Source Voltage

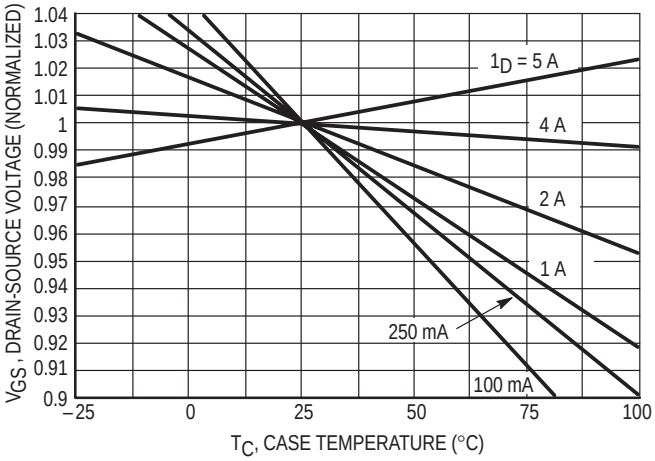


Figure 4. Gate–Source Voltage versus Case Temperature

TYPICAL CHARACTERISTICS

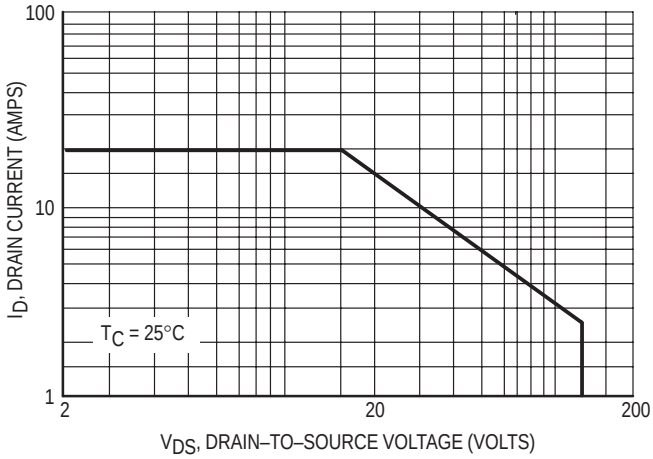


Figure 5. DC Safe Operating Area

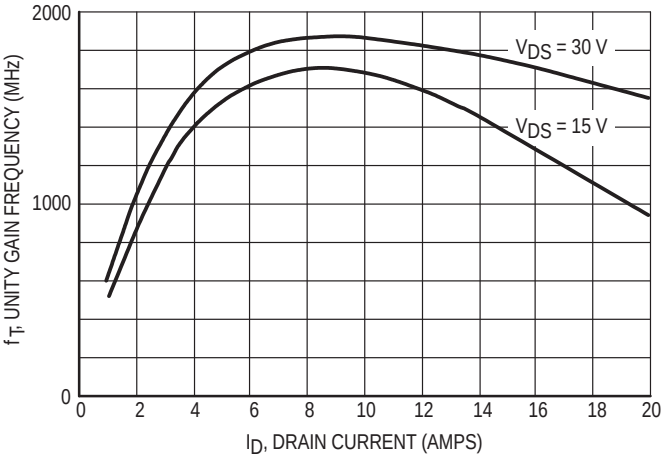


Figure 6. Common Source Unity Gain Frequency versus Drain Current

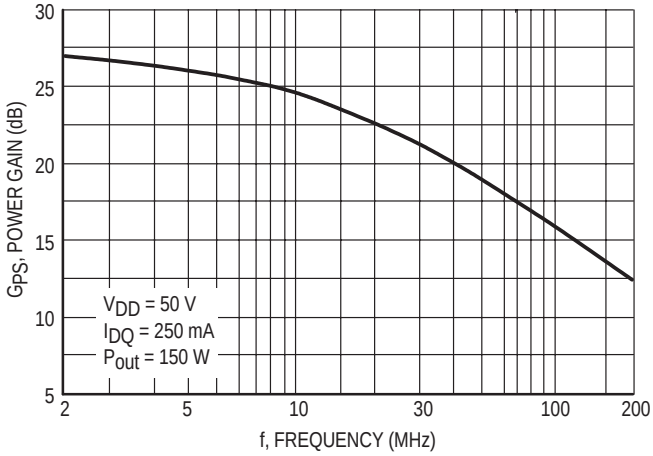


Figure 7. Power Gain versus Frequency

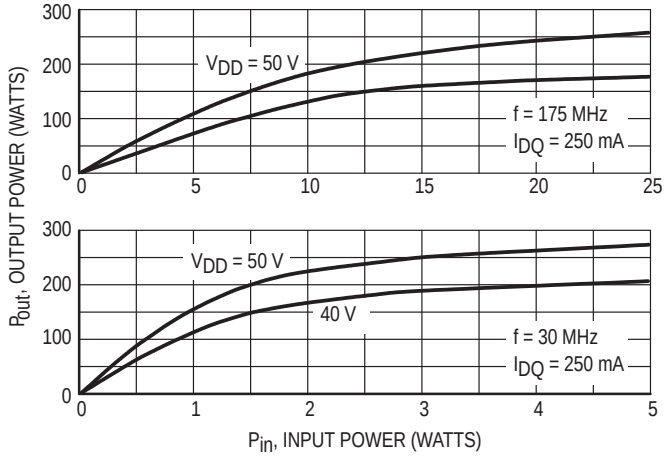


Figure 8. Output Power versus Input Power

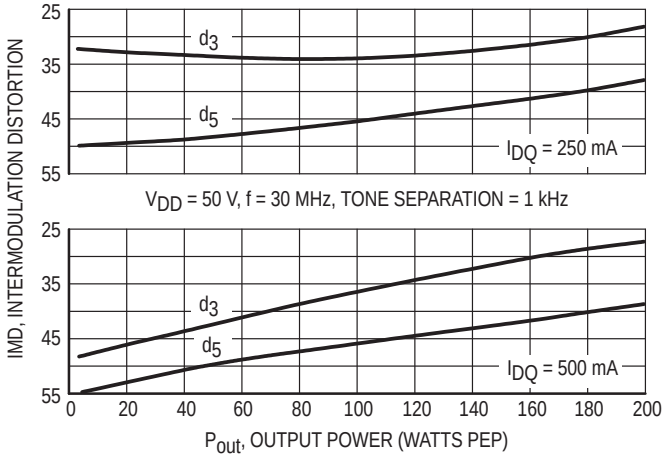


Figure 9. IMD versus P_{out}

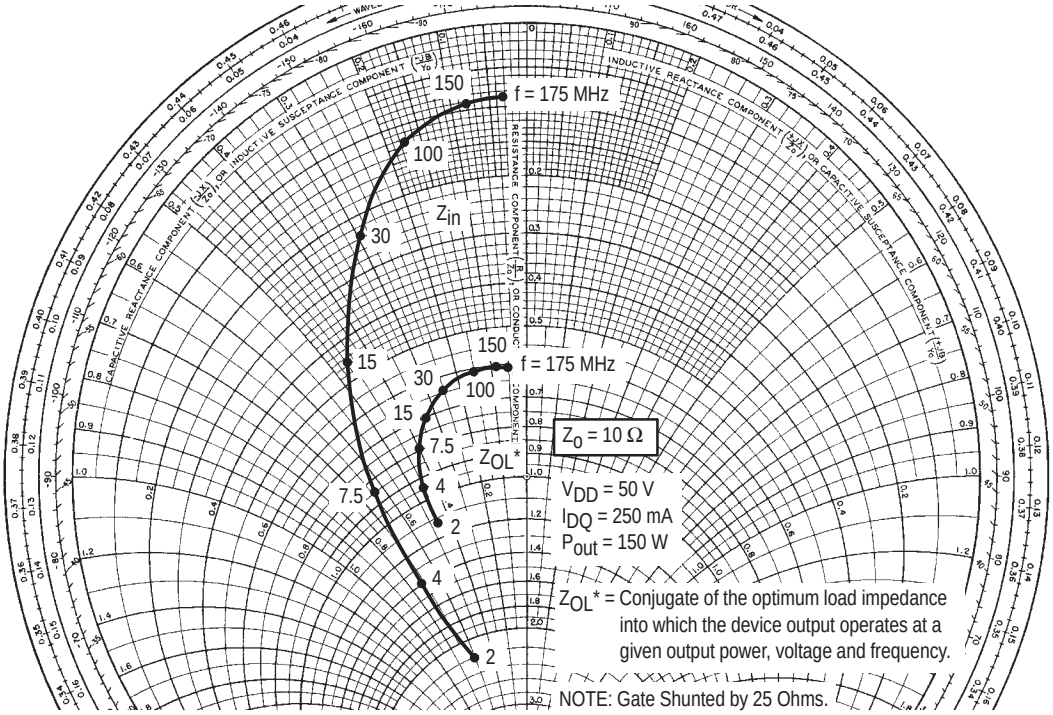


Figure 10. Series Equivalent Impedance

Table 1. Common Source S–Parameters (V_{DS} = 50 V, I_D = 2 A)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.877	–174	10.10	77	0.008	19	0.707	–169
40	0.886	–175	7.47	69	0.009	24	0.715	–172
50	0.895	–175	5.76	63	0.008	33	0.756	–171
60	0.902	–176	4.73	58	0.009	39	0.764	–171
70	0.912	–176	3.86	52	0.009	46	0.784	–172
80	0.918	–177	3.19	48	0.010	54	0.802	–171
90	0.925	–177	2.69	45	0.011	62	0.808	–171
100	0.932	–177	2.34	40	0.013	67	0.850	–173
110	0.936	–178	2.06	37	0.014	72	0.865	–175
120	0.942	–178	1.77	35	0.015	76	0.875	–173
130	0.946	–179	1.55	32	0.017	77	0.874	–172
140	0.950	–179	1.39	30	0.019	77	0.884	–174
150	0.954	–180	1.23	27	0.021	78	0.909	–175
160	0.957	–180	1.13	24	0.023	79	0.911	–176
170	0.960	180	1.01	22	0.024	82	0.904	–177
180	0.962	179	0.90	20	0.026	82	0.931	–176
190	0.964	179	0.84	19	0.028	80	0.929	–178
200	0.967	179	0.75	18	0.030	79	0.922	–179
210	0.967	178	0.71	16	0.032	80	0.937	–180
220	0.969	178	0.67	14	0.035	82	0.949	180
230	0.971	178	0.60	12	0.038	81	0.950	179
240	0.970	177	0.57	12	0.037	80	0.950	179
250	0.972	177	0.51	12	0.039	80	0.935	179

Table 1. Common Source S–Parameters (V_{DS} = 50 V, I_D = 2 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
260	0.973	177	0.47	11	0.041	79	0.954	178
270	0.972	176	0.45	9	0.044	80	0.953	176
280	0.974	176	0.41	9	0.046	80	0.965	175
290	0.974	176	0.40	6	0.046	79	0.944	175
300	0.975	176	0.39	10	0.048	82	0.929	176
310	0.976	175	0.36	9	0.049	82	0.943	176
320	0.974	175	0.33	7	0.053	78	0.954	173
330	0.975	174	0.31	4	0.056	78	0.935	172
340	0.976	174	0.30	10	0.056	77	0.948	172
350	0.975	174	0.29	7	0.058	80	0.950	174
360	0.977	174	0.28	8	0.059	79	0.978	172
370	0.976	173	0.26	8	0.061	76	0.981	170
380	0.976	173	0.26	7	0.065	75	0.944	171
390	0.977	173	0.24	10	0.066	76	0.960	171
400	0.976	172	0.23	7	0.068	80	0.955	173
410	0.976	172	0.22	9	0.071	77	0.999	170
420	0.977	172	0.21	9	0.071	76	0.962	168
430	0.976	171	0.19	10	0.073	76	0.950	168
440	0.976	171	0.20	12	0.075	75	0.953	168
450	0.978	171	0.19	10	0.080	77	0.982	168
460	0.978	170	0.18	13	0.082	74	0.990	165
470	0.978	170	0.18	10	0.081	77	0.953	168
480	0.974	170	0.18	13	0.085	78	0.944	167
490	0.973	169	0.17	13	0.086	75	0.966	165
500	0.972	169	0.17	14	0.089	73	0.980	165

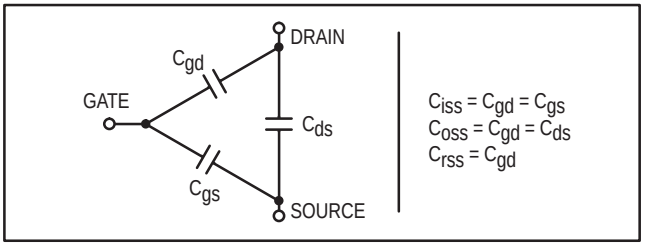
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 6 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of this device is essentially capacitor. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the device due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — This device does not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

DESIGN CONSIDERATIONS

The MRF151 is an RF Power, MOS, N–channel enhancement mode field–effect transistor (FET) designed for HF and VHF power amplifier applications.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power MOSFETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

The MRF151 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF151 was characterized at I_{DQ} = 250 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF151 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

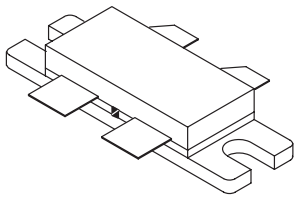
The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode MOSFET

MRF151G

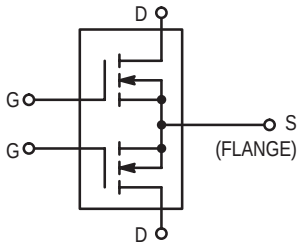
Designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 175 MHz, 50 V:
  Output Power — 300 W
  Gain — 14 dB (16 dB Typ)
  Efficiency — 50%
- Low Thermal Resistance — 0.35°C/W
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability
- S–Parameters Available for Download into Frequency Domain Simulators. See http://motorola.com/sps/rf/designtds/

300 W, 50 V, 175 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET



CASE 375–04, STYLE 2



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Drain–Gate Voltage	V_{DGO}	125	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	40	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	500 2.85	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

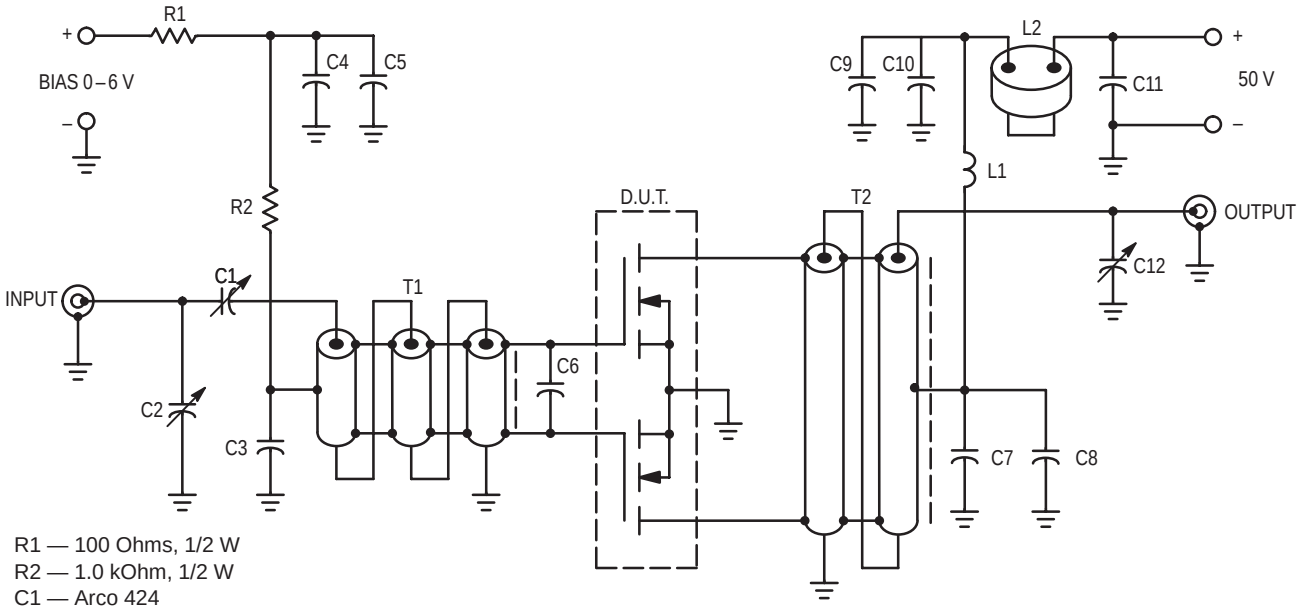
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.35	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Each Side)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (Each Side)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	5.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS (Each Side)					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	350	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	220	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	15	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain (V_{DD} = 50 V, P_{out} = 300 W, I_{DQ} = 500 mA, f = 175 MHz)	G_{ps}	14	16	—	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 300 W, f = 175 MHz, I_D (Max) = 11 A)	η	50	55	—	%
Load Mismatch (V_{DD} = 50 V, P_{out} = 300 W, I_{DQ} = 500 mA, VSWR 5:1 at all Phase Angles)	ψ	No Degradation in Output Power			



R1 — 100 Ohms, 1/2 W
R2 — 1.0 kOhm, 1/2 W
C1 — Arco 424
C2 — Arco 404
C3, C4, C7, C8, C9 — 1000 pF Chip
C5, C10 — 0.1 μF Chip
C6 — 330 pF Chip
C11 — 0.47 μF Ceramic Chip, Kemet 1215 or Equivalent (100 V)
C12 — Arco 422
L1 — 10 Turns AWG #18 Enameled Wire, Close Wound, 1/4″ I.D.
L2 — Ferrite Beads of Suitable Material for 1.5–2.0 μH Total Inductance

Unless Otherwise Noted, All Chip Capacitors are ATC Type 100 or Equivalent.

T1 — 9:1 RF Transformer. Can be made of 15–18 Ohms Semirigid Co–Ax, 62–90 Mils O.D.
T2 — 1:4 RF Transformer. Can be made of 16–18 Ohms Semirigid Co–Ax, 70–90 Mils O.D.
Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, ε_r = 5.0

NOTE: For stability, the input transformer T1 must be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

See Figure 6 for construction details of T1 and T2.

Figure 1. 175 MHz Test Circuit

TYPICAL CHARACTERISTICS

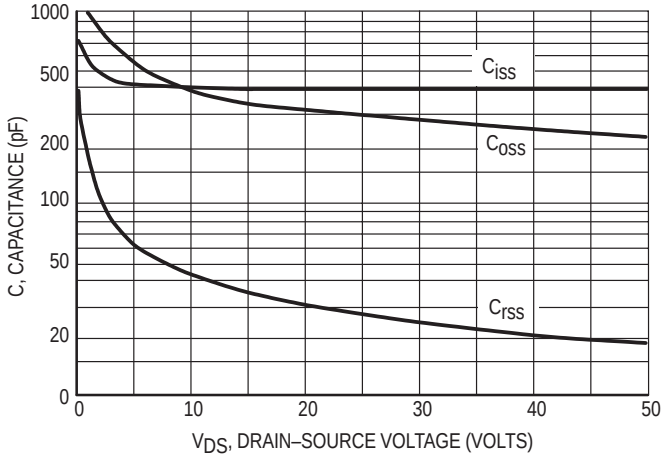


Figure 2. Capacitance versus Drain–Source Voltage*

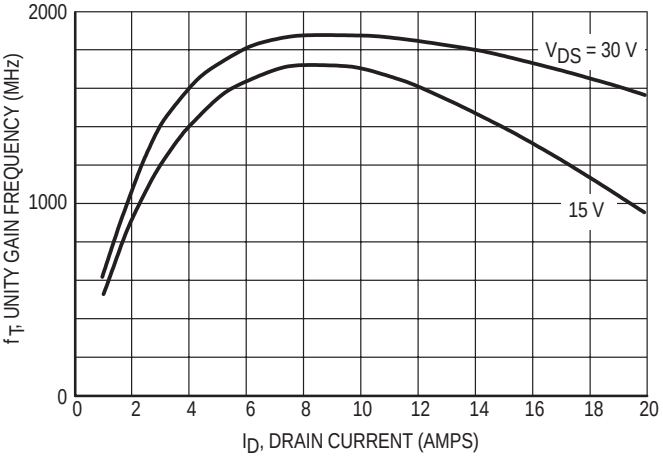


Figure 3. Common Source Unity Gain Frequency versus Drain Current*

*Data shown applies to each half of MRF151G.

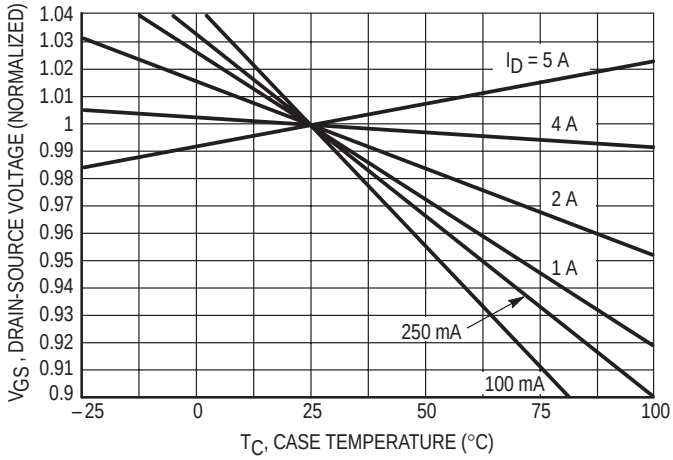


Figure 4. Gate–Source Voltage versus Case Temperature*

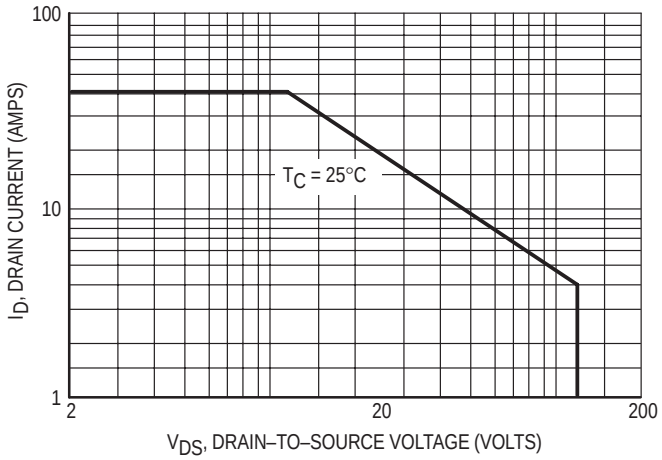


Figure 5. DC Safe Operating Area

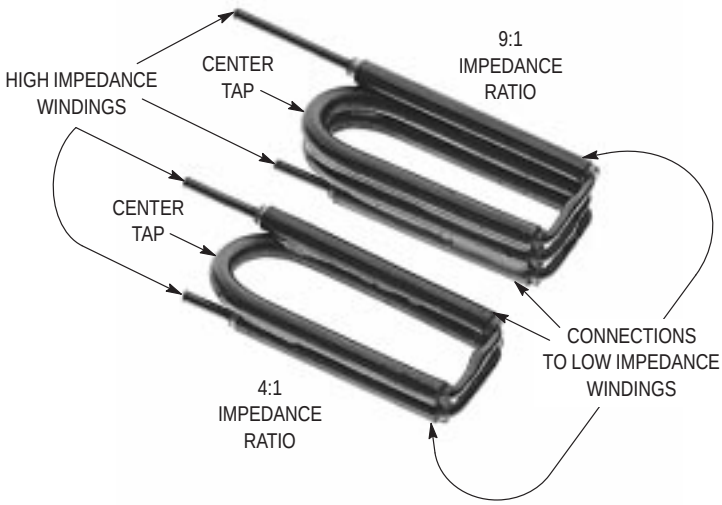


Figure 6. RF Transformer

TYPICAL CHARACTERISTICS

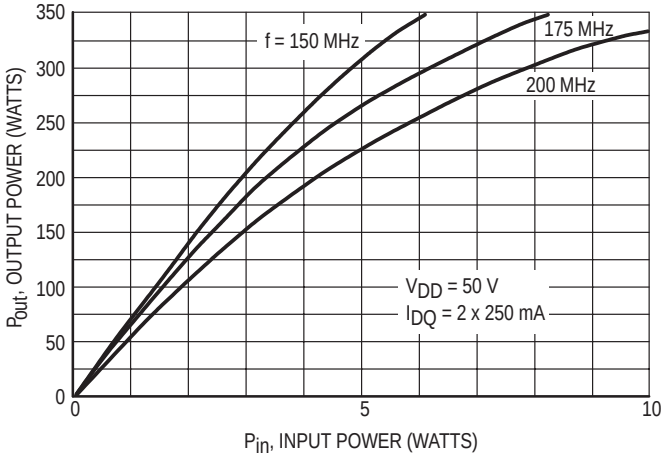


Figure 7. Output Power versus Input Power

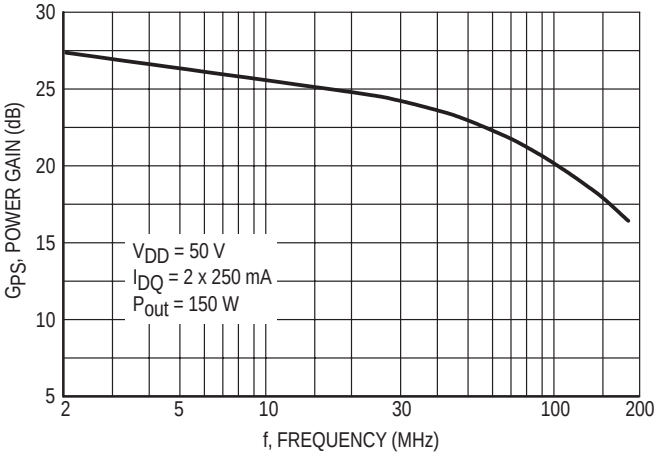
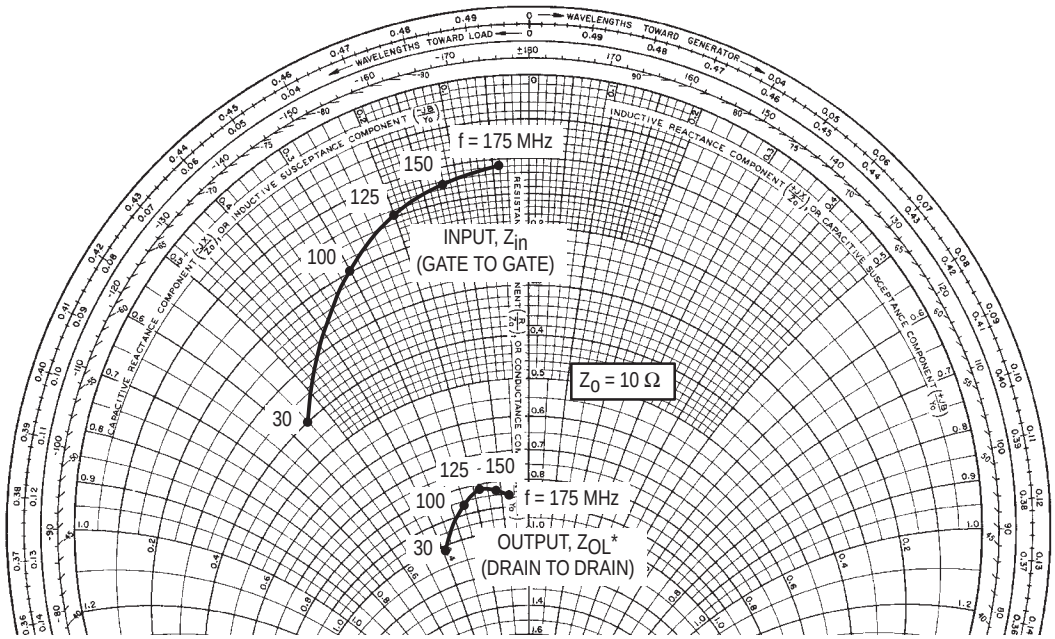


Figure 8. Power Gain versus Frequency



Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 9. Input and Output Impedance

NOTE: S–Parameter data represents measurements taken from one chip only.

Table 1. Common Source S–Parameters (V_{DS} = 50 V, I_D = 2 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.877	–174	10.10	77	0.008	19	0.707	–169
40	0.886	–175	7.47	69	0.009	24	0.715	–172
50	0.895	–175	5.76	63	0.008	33	0.756	–171
60	0.902	–176	4.73	58	0.009	39	0.764	–171
70	0.912	–176	3.86	52	0.009	46	0.784	–172
80	0.918	–177	3.19	48	0.010	54	0.802	–171
90	0.925	–177	2.69	45	0.011	62	0.808	–171
100	0.932	–177	2.34	40	0.013	67	0.850	–173
110	0.936	–178	2.06	37	0.014	72	0.865	–175
120	0.942	–178	1.77	35	0.015	76	0.875	–173
130	0.946	–179	1.55	32	0.017	77	0.874	–172
140	0.950	–179	1.39	30	0.019	77	0.884	–174
150	0.954	–180	1.23	27	0.021	78	0.909	–175
160	0.957	–180	1.13	24	0.023	79	0.911	–176
170	0.960	180	1.01	22	0.024	82	0.904	–177
180	0.962	179	0.90	20	0.026	82	0.931	–176
190	0.964	179	0.84	19	0.028	80	0.929	–178
200	0.967	179	0.75	18	0.030	79	0.922	–179
210	0.967	178	0.71	16	0.032	80	0.937	–180
220	0.969	178	0.67	14	0.035	82	0.949	180
230	0.971	178	0.60	12	0.038	81	0.950	179
240	0.970	177	0.57	12	0.037	80	0.950	179
250	0.972	177	0.51	12	0.039	80	0.935	179
260	0.973	177	0.47	11	0.041	79	0.954	178
270	0.972	176	0.45	9	0.044	80	0.953	176
280	0.974	176	0.41	9	0.046	80	0.965	175
290	0.974	176	0.40	6	0.046	79	0.944	175
300	0.975	176	0.39	10	0.048	82	0.929	176
310	0.976	175	0.36	9	0.049	82	0.943	176
320	0.974	175	0.33	7	0.053	78	0.954	173
330	0.975	174	0.31	4	0.056	78	0.935	172
340	0.976	174	0.30	10	0.056	77	0.948	172
350	0.975	174	0.29	7	0.058	80	0.950	174
360	0.977	174	0.28	8	0.059	79	0.978	172
370	0.976	173	0.26	8	0.061	76	0.981	170
380	0.976	173	0.26	7	0.065	75	0.944	171
390	0.977	173	0.24	10	0.066	76	0.960	171
400	0.976	172	0.23	7	0.068	80	0.955	173
410	0.976	172	0.22	9	0.071	77	0.999	170
420	0.977	172	0.21	9	0.071	76	0.962	168
430	0.976	171	0.19	10	0.073	76	0.950	168

Table 1. Common Source S–Parameters (V_{DS} = 50 V, I_D = 2 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
440	0.976	171	0.20	12	0.075	75	0.953	168
450	0.978	171	0.19	10	0.080	77	0.982	168
460	0.978	170	0.18	13	0.082	74	0.990	165
470	0.978	170	0.18	10	0.081	77	0.953	168
480	0.974	170	0.18	13	0.085	78	0.944	167
490	0.973	169	0.17	13	0.086	75	0.966	165
500	0.972	169	0.17	14	0.089	73	0.980	165

Table 2. Common Source S–Parameters (V_{DS} = 50 V, I_D = 0.38 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.834	–168	9.70	74	0.014	–10	0.747	–162
40	0.869	–169	6.47	62	0.013	–19	0.731	–159
50	0.883	–170	5.13	55	0.012	–24	0.754	–161
60	0.892	–171	4.03	51	0.011	–24	0.823	–164
70	0.901	–172	3.39	50	0.010	–20	0.912	–167
80	0.911	–173	2.80	47	0.009	–16	0.996	–168
90	0.924	–173	2.39	42	0.008	–14	1.100	–167
100	0.935	–174	1.99	35	0.006	–15	1.100	–167
110	0.945	–174	1.67	29	0.005	–17	1.070	–169
120	0.953	–175	1.36	25	0.004	–10	0.988	–167
130	0.958	–175	1.14	23	0.004	4	0.934	–169
140	0.962	–176	1.01	23	0.004	26	0.935	–170
150	0.964	–177	0.93	24	0.004	45	0.983	–172
160	0.966	–177	0.85	24	0.004	58	1.080	–173
170	0.969	–178	0.79	21	0.005	61	1.170	–173
180	0.972	–178	0.74	17	0.006	57	1.250	–173
190	0.975	–178	0.65	10	0.007	56	1.210	–174
200	0.977	–179	0.56	8	0.008	63	1.110	–174
210	0.979	–179	0.50	7	0.008	72	1.010	–174
220	0.980	–179	0.44	9	0.008	81	0.958	–172
230	0.980	–180	0.41	9	0.009	79	1.020	–175
240	0.981	180	0.38	12	0.009	74	1.020	–178
250	0.982	180	0.38	11	0.011	74	1.060	–176
260	0.983	179	0.34	8	0.014	76	1.180	–179
270	0.984	179	0.34	4	0.014	80	1.220	–180
280	0.984	179	0.30	3	0.013	79	1.180	–179
290	0.984	178	0.27	–4	0.012	73	1.040	–177
300	0.984	178	0.25	0	0.014	69	0.996	–178
310	0.984	178	0.24	4	0.017	74	0.951	–178
320	0.985	177	0.23	7	0.019	83	0.964	179
330	0.985	177	0.20	3	0.019	90	1.060	180
340	0.986	177	0.22	7	0.017	87	1.100	179

Table 2. Common Source S–Parameters (V_{DS} = 50 V, I_D = 0.38 A) (continued)

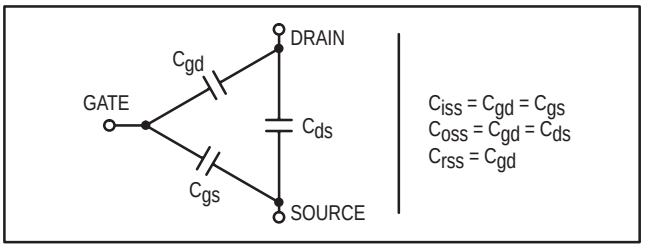
f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
350	0.986	177	0.20	5	0.017	76	1.140	–180
360	0.986	176	0.19	–2	0.021	67	1.160	180
370	0.985	176	0.17	–3	0.024	69	1.100	180
380	0.985	176	0.16	–3	0.024	77	1.070	–180
390	0.985	176	0.15	0	0.021	85	0.993	–180
400	0.985	175	0.14	3	0.018	85	0.962	–180
410	0.985	175	0.14	2	0.021	72	1.040	179
420	0.986	175	0.13	5	0.027	68	1.060	177
430	0.986	174	0.13	4	0.031	73	1.100	177
440	0.986	174	0.13	0	0.030	81	1.140	177
450	0.985	174	0.13	–1	0.025	87	1.110	178
460	0.984	174	0.11	–2	0.022	68	1.090	176
470	0.984	174	0.10	–1	0.025	59	1.020	177
480	0.985	173	0.10	3	0.034	66	0.993	179
490	0.986	173	0.10	1	0.038	79	1.020	178
500	0.986	173	0.10	6	0.035	93	1.010	177

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 3 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

DESIGN CONSIDERATIONS

The MRF151G is an RF Power, MOS, N–channel enhancement mode field–effect transistor (FET) designed for HF and VHF power amplifier applications.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power MOSFETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

The MRF151G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF151G was characterized at I_{DQ} = 250 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF151G may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

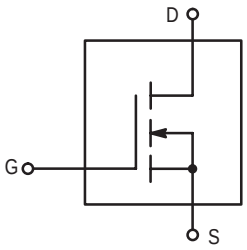
The RF MOSFET Line
RF Power Field Effect Transistor
N–Channel Enhancement–Mode MOSFET

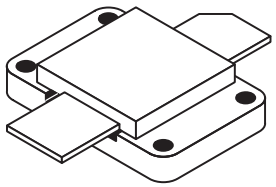
MRF154

Designed primarily for linear large–signal output stages in the 2.0–100 MHz frequency range.

- Specified 50 Volts, 30 MHz Characteristics
  Output Power = 600 Watts
  Power Gain = 17 dB (Typ)
  Efficiency = 45% (Typ)

600 W, 50 V, 80 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET





CASE 368–03, STYLE 2
(HOG PAC)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Drain–Gate Voltage	V_{DGO}	125	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	60	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1350 7.7	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

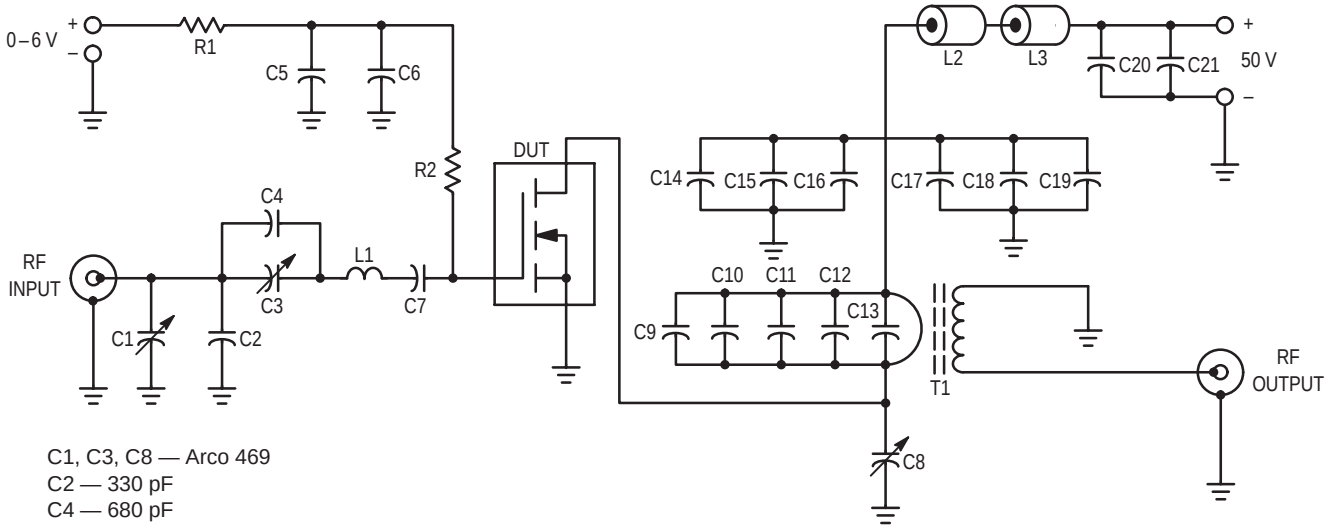
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.13	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	20	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	5.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 40 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 20 A)	g_{fs}	16	20	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1600	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	950	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	175	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain (V_{DD} = 50 V, P_{out} = 600 W, I_{DQ} = 800 mA, f = 30 MHz)	G_{ps}	—	17	—	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 600 W, I_{DQ} = 800 mA, f = 30 MHz)	η	—	45	—	%
Intermodulation Distortion (V_{DD} = 50 V, P_{out} = 600 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 800 mA)	$IMD_{(d3)}$	—	–25	—	dB



C1, C3, C8 — Arco 469
C2 — 330 pF
C4 — 680 pF
C5, C19, C20 — 0.47 μF, RMC Type 2225C
C6, C7, C14, C15, C16 — 0.1 μF
C9, C10, C11 — 470 pF
C12 — 1000 pF
C13 — Two Unencapsulated 1000 pF Mica, in Series
C17, C18 — 0.039 μF
C21 — 10 μF/100 V Electrolytic
L1 — 2 Turns #16 AWG, 1/2″ ID, 3/8″ Long
L2, L3 — Ferrite Beads, Fair–Rite Products Corp. #2673000801
R1, R2 — 10 Ohms/2.0 W Carbon
T1 — RF Transformer, 1:25 Impedance Ratio. See Motorola Application Note AN749, Figure 4 for details. Ferrite Material: 2 Each, Fair–Rite Products Corp. #2667540001

All capacitors ATC type 100/200 chips or equivalent unless otherwise noted.

Figure 1. 30 MHz Test Circuit

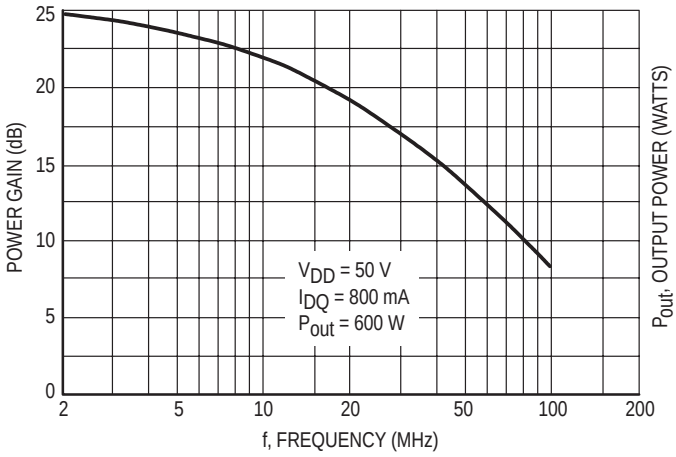


Figure 2. Power Gain versus Frequency

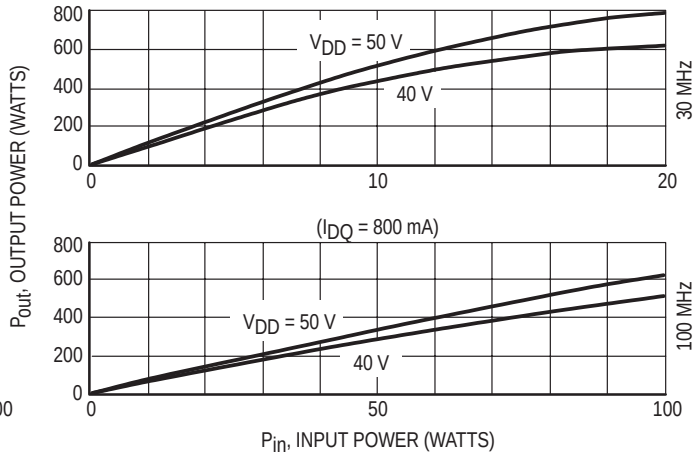


Figure 3. Output Power versus Input Power

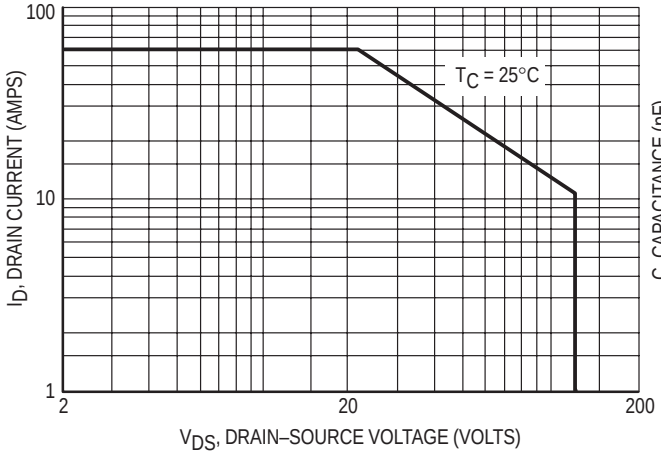


Figure 4. DC Safe Operating Area

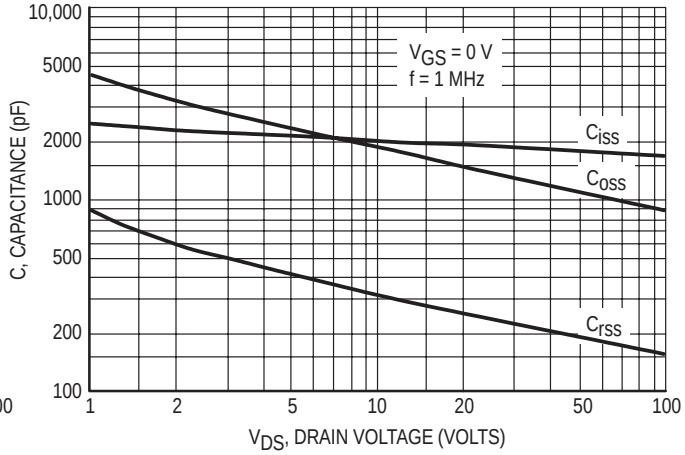


Figure 5. Capacitance versus Drain Voltage

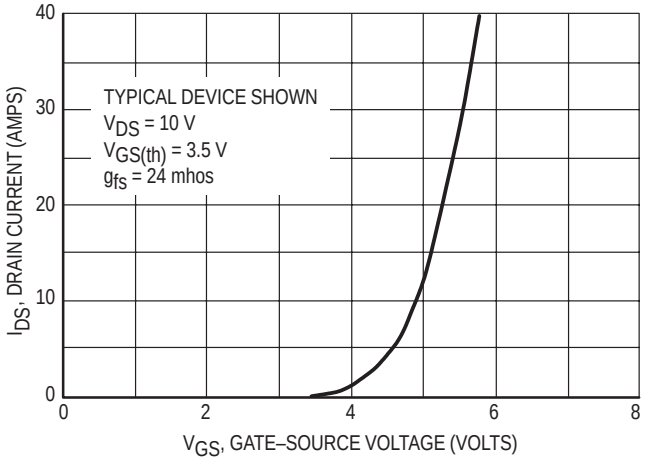


Figure 6. Gate Voltage versus Drain Current

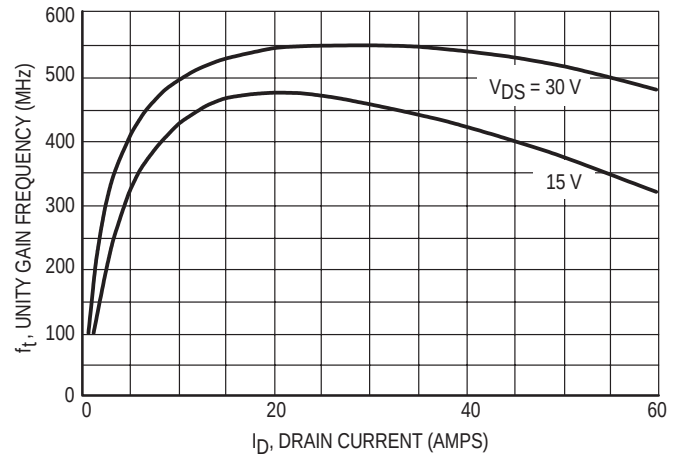


Figure 7. Common Source Unity Gain Frequency versus Drain Current

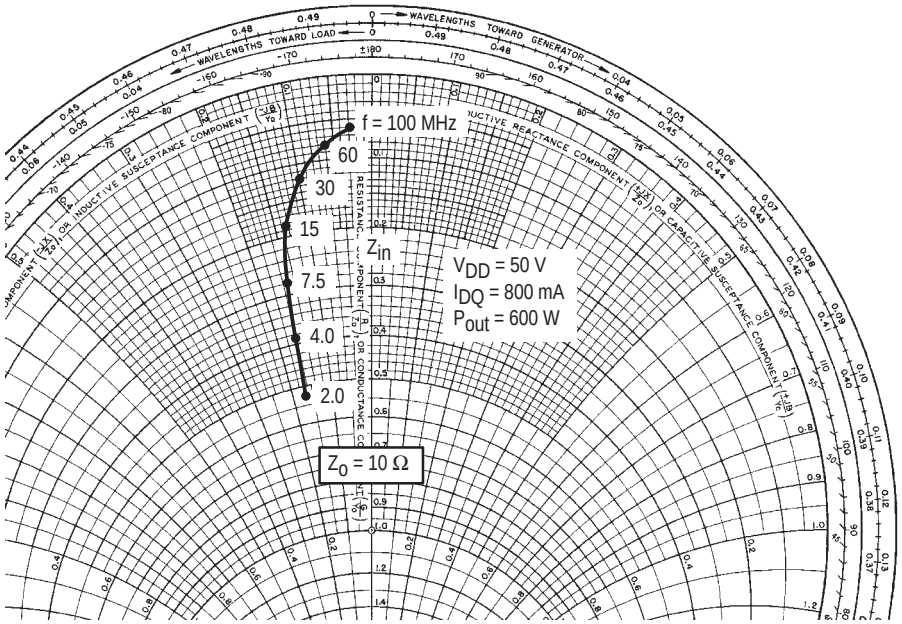
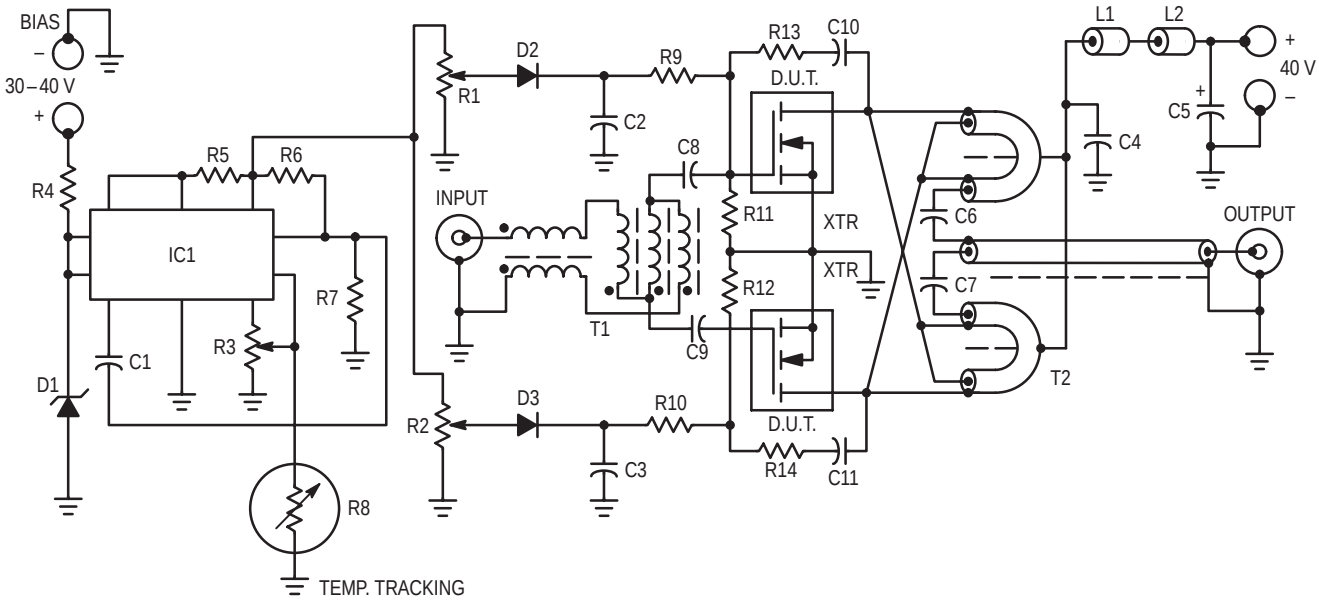


Figure 8. Series Equivalent Impedance



C1 — 1000 pF Ceramic
C2, C3, C4, C8, C9, C10, C11 — 0.1 μF Ceramic
C5 — 10 μF/100 V Electrolytic
C6, C7 — 0.1 μF Ceramic, (ATC 200/823 or Equivalent)
D1 — 28 V Zener, 1N5362 or Equivalent
D3 — 1N4148
IC1 — MC1723
L1, L2 — Fair–Rite Products Corp. Ferrite Beads #2673000801
R1, R2, R3 — 10 k Trimpot
R4 — 1.0 k/1.0 W
R5 — 10 Ohms
R6 — 2.0 k
R7 — 10 k
R8 — Thermistor, 10 k (25°C), 2.5 k (75°C)
R9, R10 — 100 Ohms
R11, R12 — 1.0 k
R13, R14 — 50–100 Ohms, 4.0 x 2.0 W Carbon in Parallel
T1 — 9:1 Transformer, Trifilar and Balun Wound on Separate Fair–Rite Products Corp. Balun Cores #286100012, 5 Turns Each.
T2 — 1:9 Transformer, Balun 50 Ohm CO–AX Cable RG–188, Low Impedance Lines W.L. Gore 16 Ohms CO–AX Type CXN 1837. Each Winding Threaded Through Two Fair–Rite Products Corp. #2661540001 Ferrite Sleeves (6 Each).
XTR — MRF154

Figure 9. 20–80 MHz 1.0 kW Broadband Amplifier

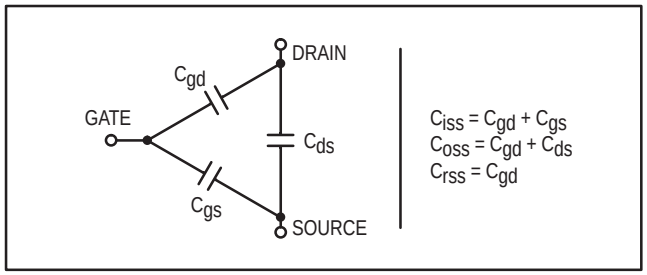
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

MOUNTING OF HIGH POWER RF POWER TRANSISTORS

The package of this device is designed for conduction cooling. It is extremely important to minimize the thermal resistance between the device flange and the heat dissipator.

Since the device mounting flange is made of soft copper, it may be deformed during various stages of handling or during transportation. It is recommended that the user makes a final inspection on this before the device installation. ±0.0005″ is considered sufficient for the flange bottom.

The same applies to the heat dissipator in the device mounting area. If copper heatsink is not used, a copper head spreader is strongly recommended between the device mounting surfaces and the main heatsink. It should be at least 1/4″ thick and extend at least one inch from the flange edges. A thin layer of thermal compound in all interfaces is, of course, essential. The recommended torque on the 4–40 mounting screws should be in the area of 4–5 lbs.–inch, and spring type lock washers along with flat washers are recommended.

For die temperature calculations, the Δ temperature from a corner mounting screw area to the bottom center of the flange is approximately 5°C and 10°C under normal operating conditions (dissipation 150 W and 300 W respectively).

The main heat dissipator must be sufficiently large and have low R_θ for moderate air velocity, unless liquid cooling is employed.

CIRCUIT CONSIDERATIONS

At high power levels (500 W and up), the circuit layout becomes critical due to the low impedance levels and high RF currents associated with the output matching. Some of the components, such as capacitors and inductors must also withstand these currents. The component losses are directly proportional to the operating frequency. The manufacturers specifications on capacitor ratings should be consulted on these aspects prior to design.

Push–pull circuits are less critical in general, since the ground referenced RF loops are practically eliminated, and the impedance levels are higher for a given power output. High power broadband transformers are also easier to design than comparable LC matching networks.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

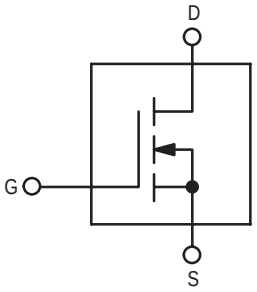
The RF Power MOS Line
Power Field Effect Transistor
N–Channel Enhancement Mode

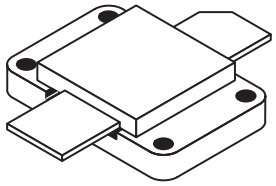
MRF157

600 W, to 80 MHz
MOS LINEAR
RF POWER FET

Designed primarily for linear large–signal output stages to 80 MHz.

- Specified 50 Volts, 30 MHz Characteristics
  Output Power = 600 Watts
  Power Gain = 21 dB (Typ)
  Efficiency = 45% (Typ)





CASE 368–03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Drain–Gate Voltage	V_{DGO}	125	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	60	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1350 7.7	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

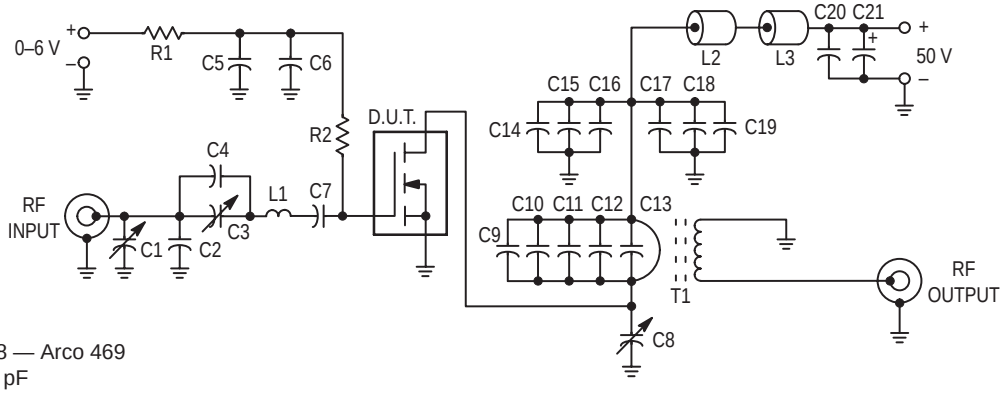
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.13	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	20	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	5.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 40 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 20 A)	g_{fs}	16	24	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	1800	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	750	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	75	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain (V_{DD} = 50 V, P_{out} = 600 W, I_{DQ} = 800 mA, f = 30 MHz)	G_{ps}	15	21	—	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 600 W, f = 30 MHz, I_{DQ} = 800 mA)	h	40	45	—	%
Intermodulation Distortion (V_{DD} = 50 V, P_{out} = 600 W(PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 800 mA)	$IMD_{(d3)}$	—	–25	—	dB



C1, C3, C8 — Arco 469
C2 — 330 pF
C4 — 680 pF
C5, C19, C20 — 0.47 μF, RMC Type 2225C
C6, C7, C14, C15, C16 — 0.1 μF
C9, C10, C11 — 470 pF
C12 — 1000 pF
C13 — Two Unencapsulated 1000 pF Mica, in Series
C17, C18 — 0.039 μF
C21 — 10 μF/100 V Electrolytic
L1 — 2 Turns #16 AWG, 1/2″ ID, 3/8″ Long
L2, L3 — Ferrite Beads, Fair–Rite Products Corp. #2673000801
R1, R2 — 10 Ohms/2W Carbon
T1 — RF Transformer, 1:25 Impedance Ratio. See Motorola Application Note AN749, Figure 4 for details. Ferrite Material: 2 Each, Fair–Rite Products Corp. #2667540001

All capacitors ATC type 100/200 chips or equivalent unless otherwise noted.

Figure 1. 30 MHz Test Circuit

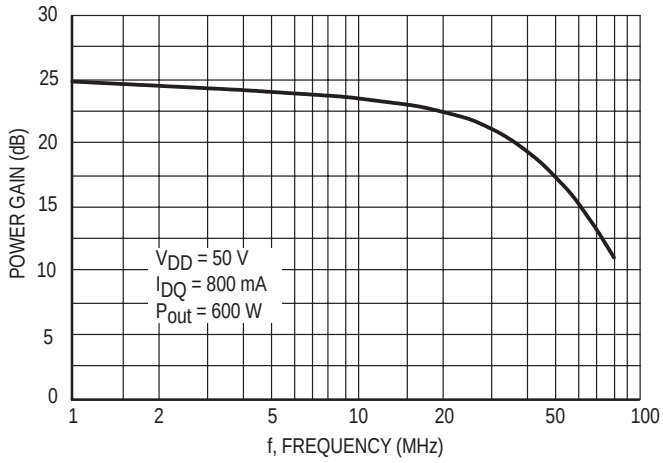


Figure 2. Power Gain versus Frequency

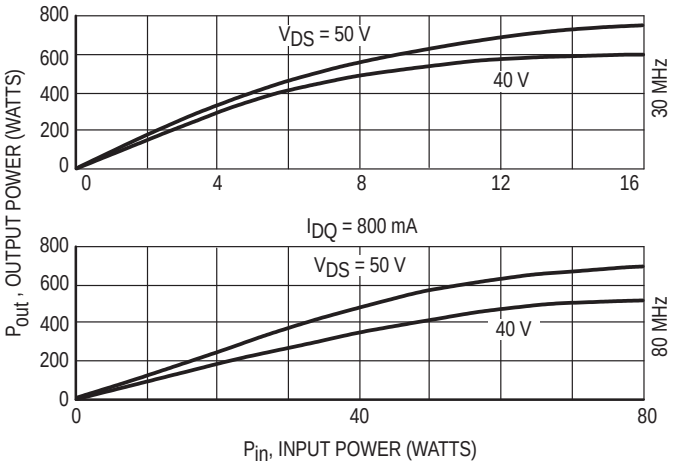


Figure 3. Output Power versus Input Power

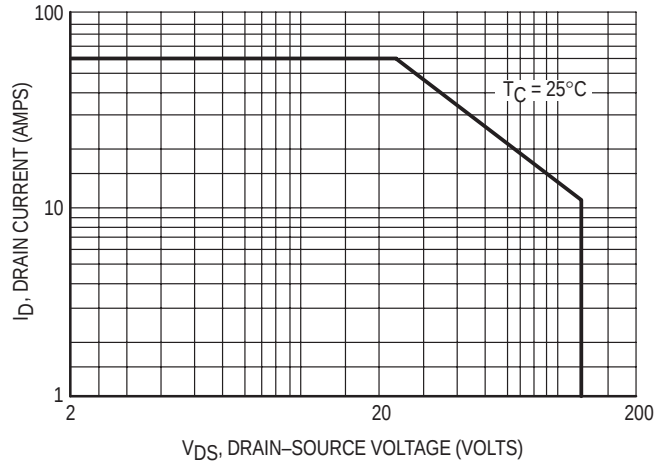


Figure 4. DC Safe Operating Area

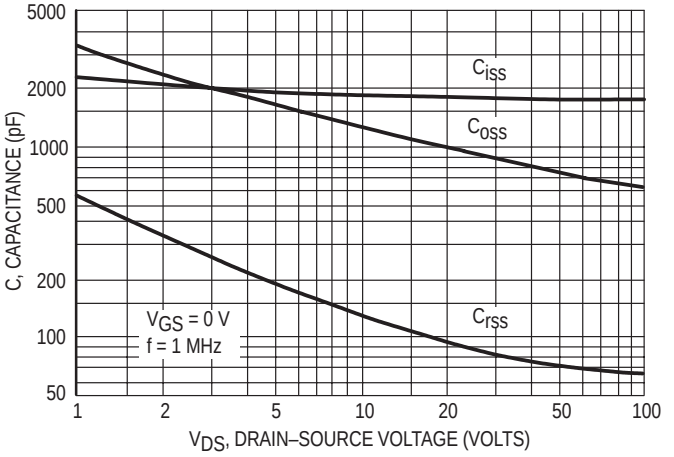


Figure 5. Capacitance versus Drain Voltage

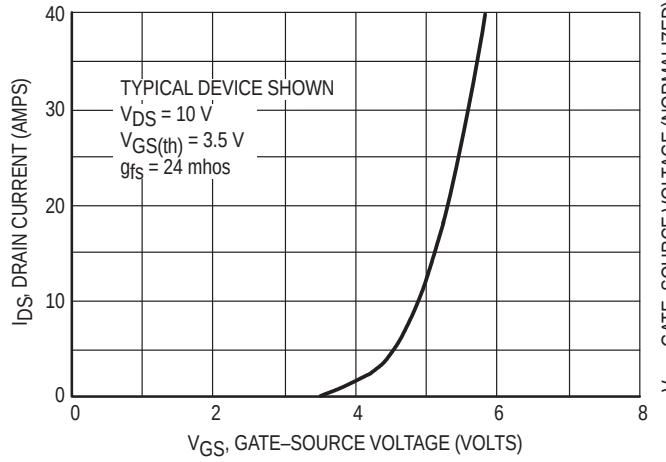


Figure 6. Gate Voltage versus Drain Current

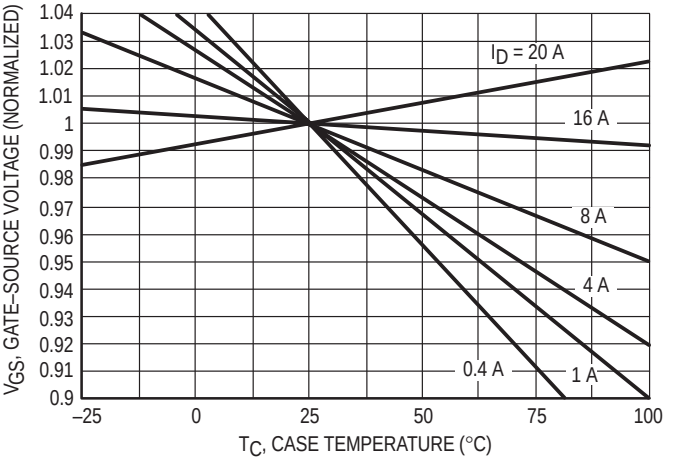


Figure 7. Gate–Source Voltage versus Case Temperature

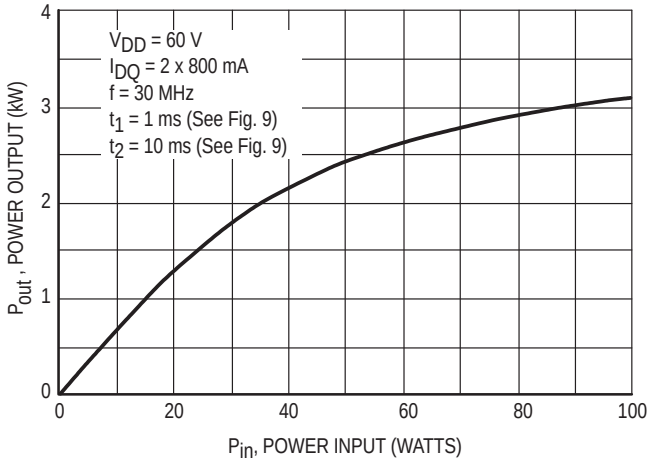


Figure 8. Output Power versus Input Power Under Pulse Conditions (2 x MRF157)

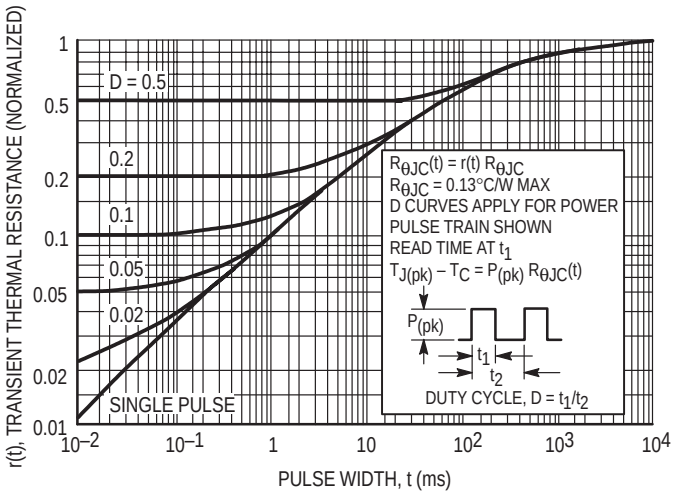
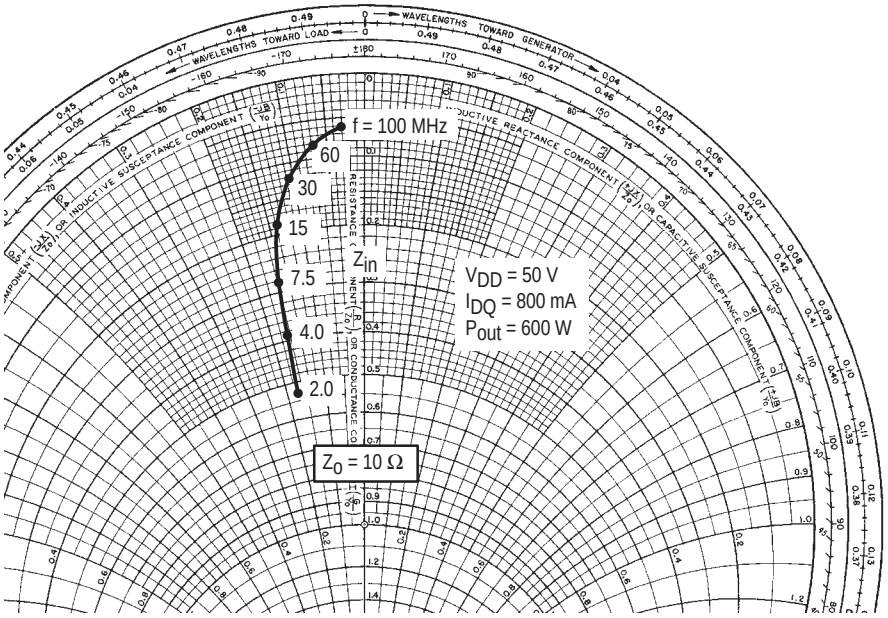


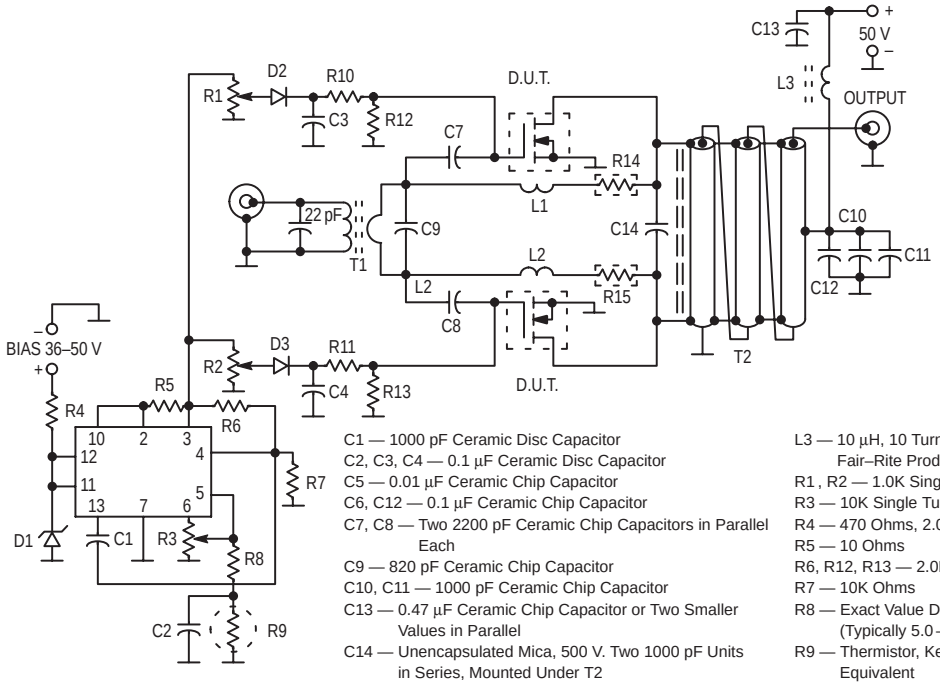
Figure 9. Thermal Response versus Pulse Width

Note: Pulse data for this graph was taken in a push–pull circuit similar to the one shown. However, the output matching network was modified for the higher level of peak power.



Note: To determine Z_{OL}*, use formula $\frac{(V_{CC} - V_{sat})^2}{2\ P_o} = Z_{OL}$*

Figure 10. Series Equivalent Impedance



C1 — 1000 pF Ceramic Disc Capacitor
C2, C3, C4 — 0.1 μF Ceramic Disc Capacitor
C5 — 0.01 μF Ceramic Chip Capacitor
C6, C12 — 0.1 μF Ceramic Chip Capacitor
C7, C8 — Two 2200 pF Ceramic Chip Capacitors in Parallel Each
C9 — 820 pF Ceramic Chip Capacitor
C10, C11 — 1000 pF Ceramic Chip Capacitor
C13 — 0.47 μF Ceramic Chip Capacitor or Two Smaller Values in Parallel
C14 — Unencapsulated Mica, 500 V. Two 1000 pF Units in Series, Mounted Under T2
D1 — 1N5357A or Equivalent
D2, D3 — 1N4148 or Equivalent.
IC1 — MC1723 (723) Voltage Regulator
L1, L2 — 15 ηH, Connecting Wires to R14 and R15, 2.5 cm Each #20 AWG
L3 — 10 μH, 10 Turns #12 AWG Enameled Wire on Fair–Rite Products Corp. Ferrite Toroid #5961000401 or Equivalent
R1 , R2 — 1.0K Single Turn Trimpots
R3 — 10K Single Turn Trimpot
R4 — 470 Ohms, 2.0 Watts
R5 — 10 Ohms
R6, R12, R13 — 2.0K Ohms
R7 — 10K Ohms
R8 — Exact Value Depends on Thermistor R9 used (Typically 5.0 – 10K)
R9 — Thermistor, Keystone RL1009–5820–97–D1 or Equivalent
R10, R11 — 100 Ohms, 1.0W Carbon
R14, R15 — EMC Technology Model 5308 or KDI Pyrofilm PPR 870–150–3 Power Resistors, 25 Ohms
T1, T2 — 9:1 and 1:9 Impedance Ratio RF Transformers

Unless otherwise noted, all resistors are 1/2 watt metal film type. All chip capacitors except C13 are ATC type 100/200B or Dielectric Laboratories type C17.

Figure 11. 2.0 to 50 MHz, 1.0 kW Wideband Amplifier

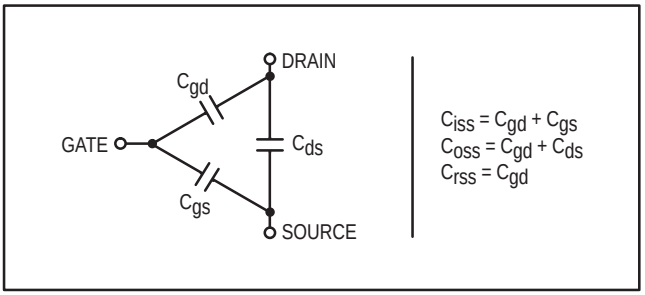
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the TMOS® FET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the interterminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the TMOS FET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

IMPEDANCE CHARACTERISTICS

Device input and output impedances are normally obtained by measuring their conjugates in an optimized narrow band test circuit. These test circuits are designed and constructed for a number of frequency points depending on the frequency coverage of characterization. For low frequencies the circuits consist of standard LC matching networks including variable capacitors for peak tuning. At increasing power levels the output impedance decreases, resulting in higher RF currents in the matching network. This makes the practicality of output impedance measurements in the manner described questionable at power levels higher than 200–300 W for devices operated at 50 V and 150–200 W for devices operated at 28 V. The physical sizes and values required for the components to withstand the RF currents increase to a point where physical construction of the output matching network gets difficult if not impossible. For this reason the output impedances are not given for high power devices such as the MRF154 and MRF157. However, formulas like $\frac{(V_{DS} - V_{sat})^2}{2P_{out}}$ for a single ended design or $\frac{2((V_{DS} - V_{sat})^2)}{P_{out}}$ for a push–pull design can be used to obtain reasonably close approximations to actual values.

MOUNTING OF HIGH POWER RF POWER TRANSISTORS

The package of this device is designed for conduction cooling. It is extremely important to minimize the thermal resistance between the device flange and the heat dissipator.

If a copper heatsink is not used, a copper head spreader is strongly recommended between the device mounting surfaces and the main heatsink. It should be at least 1/4″ thick and extend at least one inch from the flange edges. A thin layer of thermal compound in all interfaces is, of course, essential. The recommended torque on the 4–40 mounting screws should be in the area of 4–5 lbs.–inch, and spring type lock washers along with flat washers are recommended.

For die temperature calculations, the Δ temperature from a corner mounting screw area to the bottom center of the flange is approximately 5°C and 10°C under normal operating conditions (dissipation 150 W and 300 W respectively).

The main heat dissipator must be sufficiently large and have low R_θ for moderate air velocity, unless liquid cooling is employed.

CIRCUIT CONSIDERATIONS

At high power levels (500 W and up), the circuit layout becomes critical due to the low impedance levels and high RF currents associated with the output matching. Some of the components, such as capacitors and inductors must also withstand these currents. The component losses are directly proportional to the operating frequency. The manufacturers specifications on capacitor ratings should be consulted on these aspects prior to design.

Push–pull circuits are less critical in general, since the ground referenced RF loops are practically eliminated, and the impedance levels are higher for a given power output. High power broadband transformers are also easier to design than comparable LC matching networks.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$R_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

The RF TMOS® Line

Power Field Effect Transistor

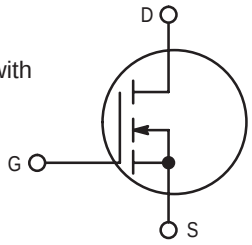
N–Channel Enhancement Mode

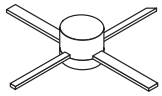
MRF158

2.0 W, to 500 MHz
TMOS
BROADBAND
RF POWER FET

Designed for wideband large–signal amplifier and oscillator applications to 500 MHz.

- Guaranteed 28 Volt, 400 MHz Performance
  Output Power = 2.0 Watts
  Minimum Gain = 16 dB
  Efficiency = 55% (Typical)
- Grounded Source Package for High Gain and Excellent Heat Dissipation (MRF158R)
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.
- S–Parameters Available for Download into Frequency Domain Simulators. See http://motorola.com/sps/rf/designtds/





CASE 305A–01, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	8.0 45	Watts mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

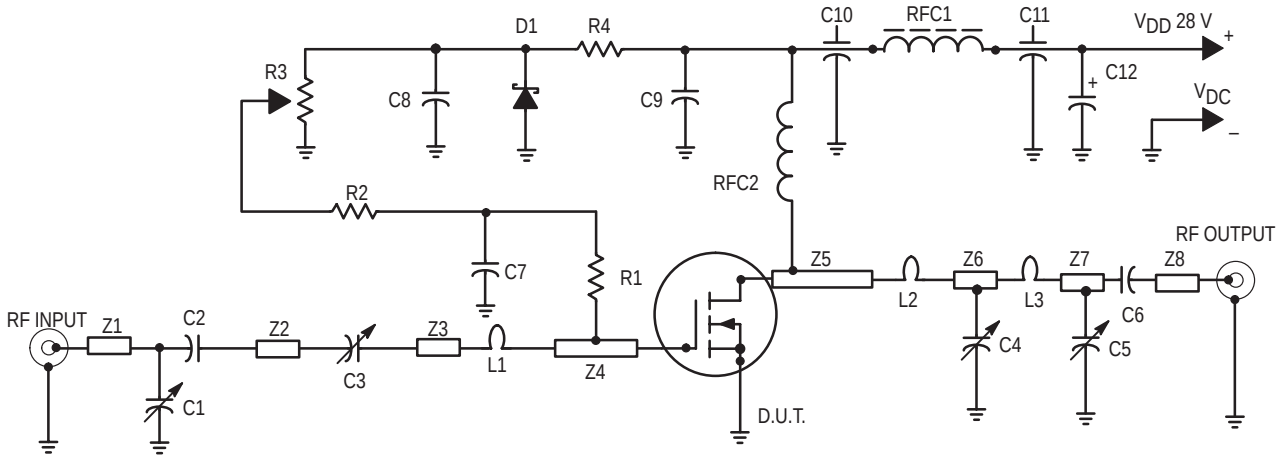
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	13.2	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

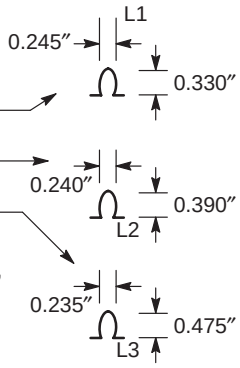
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	0.5	mAdc
Gate–Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (I_D = 10 mA, V_{DS} = 10 V)	$V_{GS(th)}$	1.0	4.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 100 mA)	g_{fs}	50	85	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	3.0	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	4.2	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	0.45	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	G_{ps}	16	20	—	dB
Drain Efficiency (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	η	45	55	—	%
Electrical Ruggedness (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{DD} = 28 V, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	Z_{in}	—	8.8 – j27.37	—	Ohms
Series Equivalent Output Impedance (V_{DD} = 28 V, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	Z_{out}	—	16.96 – j62	—	Ohms



C1, C4, C5 — Johanson Trimmer Capacitor, 2 – 20 pF
C2, C6 — 270 pF Chip Capacitor
C3 — Arco 404
C7, C8, C9 — 0.1 μF
C10, C11 — 680 pF Feed Through
C12 — 50 μF, 50 V
D1 — 1N5925A Motorola Zener
L1 — #18 AWG, Hairpin 0.825″ long, bend into hairpin
L2 — #18 AWG, Hairpin 0.875″ long, bend into hairpin
L3 — #18 AWG, Hairpin 0.965″ long, bend into hairpin

Board Material — 0.062″, Teflon Fiberglass, 2 oz., Copper clad both sides, ϵ_r = 2.55



R1 — 91 Ω 1/2 Watt
R2 — 10 kΩ 1/2 Watt
R3 — 10 kΩ, 10 Turns Bourns
R4 — 1.8 k 1.4 Watt
RFC1 — Ferroxcube VK200–19/4B
RFC2 — 10 Turns #20 AWG Enameled, 0.250″ ID
Z1 — Microstrip Line 0.150″ wide, 0.420″ long
Z2 — Microstrip Line 0.150″ wide, 0.420″ long
Z3 — Microstrip Line 0.150″ wide, 0.475″ long
Z4 — Microstrip Line 0.150″ wide, 0.825″ long
Z5 — Microstrip Line 0.150″ wide, 0.750″ long
Z6 — Microstrip Line 0.150″ wide, 0.500″ long
Z7 — Microstrip Line 0.150″ wide, 0.500″ long
Z8 — Microstrip Line 0.150″ wide, 0.450″ long

Figure 1. 400 MHz Test Circuit

TYPICAL CHARACTERISTICS

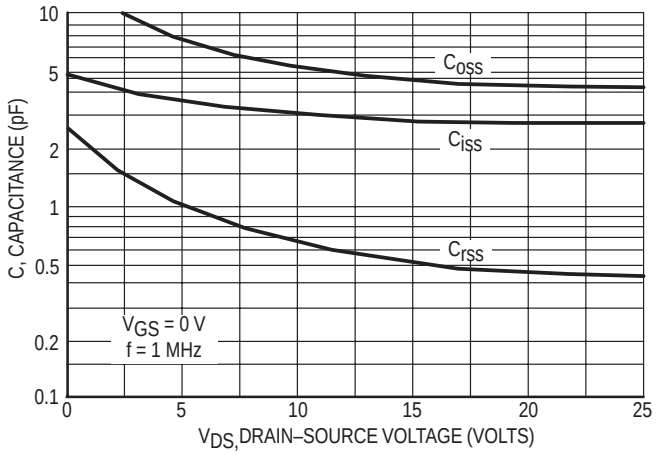


Figure 2. Capacitance versus Drain–Source Voltage

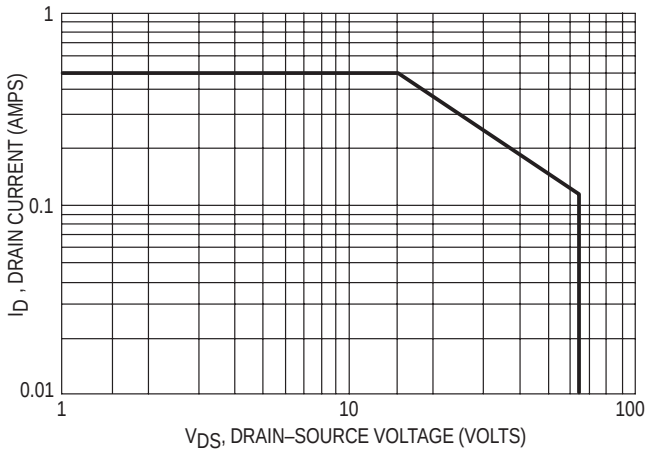


Figure 3. DC Safe Operating Area

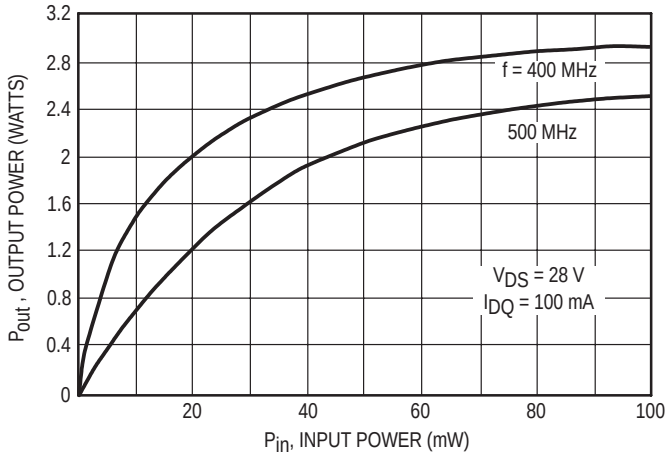


Figure 4. Output Power versus Input Power

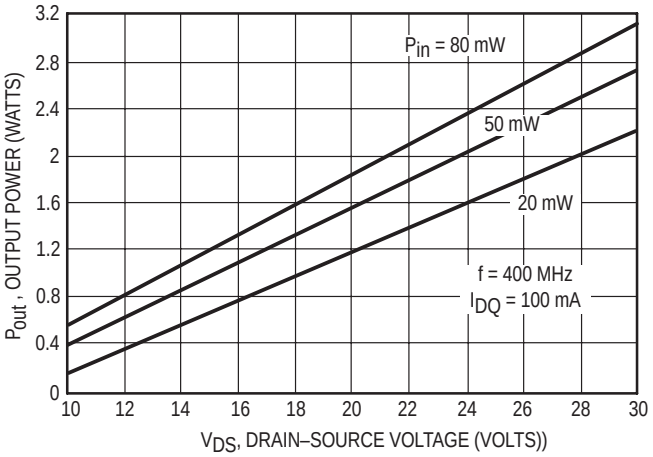


Figure 5. Output Power versus Voltage

Table 1. Common Source S–Parameters (V_{DS} = 13 V, I_D = 100 mA)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
5	1.000	–2	9.45	179	0.000	89	0.965	–1
10	0.997	–4	9.45	177	0.005	92	0.969	–3
15	0.999	–5	9.50	176	0.007	86	0.962	–5
20	0.997	–7	9.45	174	0.009	91	0.958	–6
25	0.997	–9	9.44	173	0.012	88	0.958	–7
30	0.996	–10	9.40	172	0.014	82	0.960	–8
35	0.994	–12	9.38	170	0.016	78	0.956	–10
40	0.993	–14	9.35	169	0.016	77	0.958	–11
45	0.990	–15	9.34	167	0.020	79	0.957	–12
50	0.988	–17	9.29	166	0.021	76	0.957	–14
55	0.985	–19	9.25	165	0.023	77	0.955	–15
60	0.983	–21	9.26	163	0.026	75	0.952	–17
65	0.980	–22	9.19	162	0.028	74	0.947	–18
70	0.977	–24	9.15	160	0.029	74	0.943	–20
75	0.973	–25	9.11	159	0.031	74	0.942	–21
80	0.970	–27	9.04	158	0.034	70	0.935	–22
85	0.967	–29	8.98	157	0.035	71	0.932	–24
90	0.963	–30	8.91	155	0.037	67	0.929	–25
95	0.961	–32	8.90	154	0.039	68	0.924	–26
100	0.957	–33	8.81	153	0.040	67	0.917	–27
105	0.953	–35	8.77	151	0.041	64	0.916	–28
109	0.950	–36	8.69	150	0.042	65	0.914	–30
114	0.943	–38	8.62	149	0.045	63	0.906	–31
119	0.940	–40	8.56	148	0.045	62	0.907	–32
124	0.933	–41	8.49	146	0.049	61	0.901	–33
129	0.933	–43	8.46	145	0.049	60	0.901	–35
134	0.923	–44	8.37	144	0.052	59	0.896	–36
139	0.921	–45	8.29	143	0.052	58	0.890	–37
144	0.917	–47	8.22	142	0.055	57	0.885	–39
149	0.913	–48	8.16	140	0.055	55	0.878	–40
154	0.911	–50	8.11	140	0.057	53	0.874	–41
159	0.905	–51	8.02	138	0.059	54	0.868	–42
164	0.902	–52	7.94	137	0.059	53	0.863	–43
169	0.896	–54	7.87	136	0.062	52	0.856	–44
174	0.893	–55	7.79	135	0.063	50	0.851	–45
179	0.890	–56	7.71	134	0.062	50	0.846	–46
184	0.882	–58	7.64	133	0.065	48	0.845	–47
189	0.881	–59	7.59	132	0.065	47	0.840	–48
194	0.874	–60	7.53	131	0.066	47	0.834	–49
199	0.868	–61	7.43	130	0.067	47	0.828	–50
204	0.864	–62	7.36	129	0.068	46	0.829	–51
209	0.861	–63	7.31	128	0.070	45	0.824	–52

Table 1. Common Source S–Parameters (V_{DS} = 13 V, I_D = 100 mA) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
214	0.856	–65	7.24	127	0.070	44	0.820	–53
219	0.853	–66	7.17	126	0.070	43	0.813	–54
224	0.848	–67	7.10	125	0.072	41	0.806	–55
229	0.847	–68	7.02	124	0.074	41	0.803	–56
234	0.841	–69	6.94	124	0.075	40	0.800	–57
239	0.839	–70	6.92	122	0.074	39	0.789	–58
244	0.832	–71	6.80	122	0.076	40	0.783	–59
249	0.828	–72	6.73	121	0.077	38	0.780	–60
254	0.825	–73	6.68	120	0.077	39	0.778	–60
259	0.820	–74	6.60	119	0.078	36	0.772	–61
264	0.816	–75	6.54	118	0.078	35	0.769	–62
269	0.813	–76	6.48	117	0.078	36	0.765	–63
274	0.810	–77	6.42	117	0.079	34	0.765	–64
279	0.806	–78	6.34	116	0.080	35	0.762	–64
284	0.799	–79	6.29	115	0.080	34	0.757	–65
289	0.800	–80	6.23	114	0.081	31	0.756	–66
294	0.795	–81	6.18	113	0.081	33	0.753	–67
299	0.789	–82	6.12	113	0.084	31	0.750	–67
304	0.791	–83	6.07	112	0.082	31	0.742	–68
308	0.790	–84	5.99	111	0.084	30	0.742	–69
313	0.787	–85	5.95	110	0.084	29	0.737	–70
318	0.784	–85	5.88	109	0.083	30	0.729	–70
323	0.779	–86	5.80	109	0.084	28	0.726	–71
328	0.778	–87	5.77	108	0.085	27	0.723	–72
333	0.773	–88	5.69	107	0.085	28	0.720	–72
338	0.771	–89	5.64	107	0.084	26	0.716	–73
343	0.766	–89	5.60	106	0.086	25	0.716	–74
348	0.766	–90	5.55	106	0.086	25	0.712	–74
353	0.763	–91	5.50	105	0.086	24	0.708	–75
358	0.761	–92	5.43	104	0.086	24	0.708	–75
363	0.761	–93	5.41	104	0.086	24	0.706	–76
368	0.755	–94	5.35	103	0.086	23	0.702	–77
373	0.753	–94	5.29	102	0.087	23	0.704	–77
378	0.752	–95	5.25	101	0.086	23	0.700	–78
383	0.750	–96	5.20	101	0.087	22	0.697	–79
388	0.747	–96	5.15	100	0.089	21	0.692	–79
393	0.742	–97	5.08	100	0.087	21	0.693	–80
398	0.741	–98	5.04	99	0.088	20	0.689	–81
403	0.743	–98	5.01	98	0.088	20	0.684	–81
408	0.740	–99	4.97	98	0.088	19	0.682	–81
413	0.734	–100	4.90	97	0.089	19	0.682	–82
418	0.738	–100	4.87	97	0.088	18	0.677	–83

Table 1. Common Source S–Parameters (V_{DS} = 13 V, I_D = 100 mA) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
423	0.733	–101	4.82	96	0.089	18	0.676	–83
428	0.735	–102	4.80	96	0.089	17	0.674	–84
433	0.731	–102	4.74	95	0.088	16	0.672	–84
438	0.732	–103	4.70	94	0.088	17	0.673	–85
443	0.728	–104	4.67	94	0.089	16	0.670	–85
448	0.729	–105	4.64	93	0.090	16	0.671	–86
453	0.727	–105	4.59	93	0.088	16	0.668	–86
458	0.723	–105	4.56	92	0.089	15	0.668	–87
463	0.721	–106	4.50	91	0.088	15	0.668	–87
468	0.720	–107	4.46	91	0.088	15	0.665	–87
473	0.719	–107	4.42	90	0.089	13	0.662	–88
478	0.717	–107	4.38	90	0.089	13	0.662	–89
483	0.717	–108	4.35	89	0.088	13	0.658	–89
488	0.715	–109	4.32	89	0.088	13	0.660	–89
493	0.714	–109	4.28	88	0.090	13	0.655	–90
498	0.714	–110	4.25	88	0.090	12	0.655	–91
503	0.713	–110	4.22	87	0.089	12	0.652	–91
507	0.712	–111	4.17	87	0.090	11	0.650	–91
512	0.711	–111	4.15	86	0.089	11	0.649	–92
517	0.706	–112	4.11	86	0.090	11	0.650	–92
522	0.705	–112	4.07	85	0.089	10	0.650	–93
527	0.706	–113	4.07	85	0.089	10	0.648	–93
532	0.705	–113	4.02	84	0.088	10	0.649	–93
537	0.704	–114	4.00	84	0.088	9	0.645	–94
542	0.704	–114	3.95	83	0.089	9	0.646	–94
547	0.704	–115	3.93	82	0.087	10	0.646	–95
552	0.704	–116	3.90	82	0.090	8	0.645	–95
557	0.702	–116	3.87	82	0.089	8	0.646	–96
562	0.699	–117	3.83	81	0.088	8	0.646	–96
567	0.699	–117	3.80	81	0.089	8	0.641	–96
572	0.700	–117	3.76	80	0.088	7	0.640	–97
577	0.699	–118	3.74	80	0.087	7	0.640	–97
582	0.698	–118	3.70	80	0.088	7	0.641	–98
587	0.699	–118	3.69	79	0.087	7	0.637	–98
592	0.697	–119	3.67	79	0.088	6	0.638	–98
597	0.698	–119	3.64	78	0.088	6	0.633	–99
602	0.698	–119	3.62	78	0.087	6	0.638	–99
607	0.695	–120	3.58	77	0.087	6	0.637	–99
612	0.696	–120	3.57	77	0.087	6	0.637	–100
617	0.694	–121	3.54	76	0.086	5	0.636	–100
622	0.695	–121	3.52	76	0.087	5	0.635	–100
627	0.692	–121	3.48	75	0.088	5	0.637	–101

Table 1. Common Source S–Parameters (V_{DS} = 13 V, I_D = 100 mA) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
632	0.691	–122	3.46	75	0.085	4	0.634	–101
637	0.691	–122	3.44	74	0.087	4	0.641	–102
642	0.689	–123	3.41	74	0.087	3	0.637	–102
647	0.687	–123	3.38	74	0.087	3	0.634	–103
652	0.689	–124	3.36	73	0.085	3	0.636	–103
657	0.686	–124	3.34	73	0.086	1	0.635	–103
662	0.688	–125	3.30	72	0.086	3	0.634	–104
667	0.689	–125	3.28	72	0.086	2	0.634	–104
672	0.693	–125	3.27	72	0.086	2	0.631	–104
677	0.687	–126	3.24	71	0.086	1	0.632	–104
682	0.689	–126	3.22	71	0.083	1	0.629	–105
687	0.687	–126	3.20	70	0.083	1	0.630	–105
692	0.686	–127	3.17	70	0.083	1	0.630	–105
697	0.690	–127	3.16	70	0.083	0	0.630	–106
702	0.687	–127	3.14	69	0.084	0	0.627	–106
706	0.688	–128	3.12	69	0.083	1	0.630	–106
711	0.685	–128	3.10	68	0.083	0	0.632	–107
716	0.686	–128	3.08	68	0.085	0	0.636	–107
721	0.688	–128	3.08	68	0.084	–1	0.634	–107
726	0.685	–129	3.05	67	0.083	0	0.634	–108
731	0.685	–130	3.02	67	0.083	–1	0.634	–108
736	0.684	–130	3.01	66	0.083	–1	0.635	–108
741	0.680	–130	2.98	66	0.082	–1	0.631	–109
746	0.681	–130	2.97	65	0.083	–2	0.636	–109
751	0.682	–131	2.96	65	0.082	–2	0.631	–110
756	0.683	–131	2.93	65	0.082	–2	0.632	–109
761	0.681	–132	2.90	64	0.082	–1	0.630	–110
766	0.683	–132	2.89	64	0.083	–3	0.632	–110
771	0.684	–132	2.87	64	0.082	–3	0.631	–110
776	0.682	–133	2.85	63	0.081	–4	0.628	–111
781	0.684	–133	2.85	63	0.080	–3	0.630	–111
786	0.686	–133	2.83	63	0.079	–4	0.629	–111
791	0.684	–134	2.81	62	0.080	–3	0.632	–112
796	0.685	–134	2.79	62	0.080	–4	0.631	–112
801	0.683	–134	2.77	62	0.079	–4	0.634	–112
806	0.685	–134	2.75	61	0.079	–2	0.632	–112
811	0.683	–135	2.75	61	0.078	–4	0.635	–113
816	0.684	–135	2.73	60	0.079	–4	0.637	–113
821	0.683	–135	2.70	60	0.077	–3	0.633	–113
826	0.682	–135	2.69	60	0.078	–5	0.637	–114
831	0.682	–136	2.67	59	0.077	–4	0.635	–114
836	0.681	–136	2.66	59	0.077	–5	0.638	–114

Table 1. Common Source S–Parameters (V_{DS} = 13 V, I_D = 100 mA) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
841	0.681	–136	2.64	58	0.079	–4	0.635	–115
846	0.679	–137	2.63	58	0.078	–4	0.637	–115
851	0.678	–137	2.61	58	0.077	–5	0.634	–115
856	0.682	–137	2.59	57	0.077	–5	0.635	–115
861	0.680	–137	2.59	57	0.077	–4	0.634	–115
866	0.681	–138	2.57	57	0.077	–6	0.635	–116
871	0.682	–138	2.55	56	0.075	–6	0.633	–116
876	0.684	–139	2.54	56	0.075	–5	0.631	–116
881	0.683	–139	2.53	56	0.075	–5	0.635	–117
886	0.681	–139	2.52	55	0.074	–6	0.633	–117
891	0.685	–140	2.50	55	0.074	–6	0.633	–117
896	0.683	–140	2.49	55	0.075	–6	0.638	–117
901	0.680	–140	2.47	54	0.073	–5	0.640	–118
905	0.681	–140	2.46	54	0.074	–7	0.637	–118
910	0.684	–140	2.44	54	0.074	–8	0.639	–118
915	0.683	–141	2.43	53	0.073	–6	0.639	–119
920	0.686	–141	2.42	53	0.074	–6	0.643	–119
925	0.683	–141	2.40	53	0.073	–7	0.641	–119
930	0.684	–141	2.39	52	0.072	–7	0.640	–120
935	0.682	–142	2.38	52	0.073	–6	0.638	–120
940	0.685	–142	2.37	52	0.072	–6	0.639	–120
945	0.683	–142	2.36	51	0.072	–7	0.638	–120
950	0.683	–143	2.34	51	0.071	–7	0.639	–120
955	0.683	–143	2.33	51	0.070	–7	0.638	–120
960	0.683	–143	2.32	51	0.073	–8	0.640	–121
965	0.683	–143	2.31	50	0.070	–8	0.640	–121
970	0.684	–144	2.30	50	0.071	–7	0.643	–121
975	0.684	–144	2.28	50	0.069	–8	0.640	–121
980	0.682	–144	2.27	49	0.068	–6	0.641	–122
985	0.685	–144	2.26	49	0.069	–9	0.643	–122
990	0.684	–145	2.25	48	0.067	–8	0.644	–122
995	0.683	–145	2.24	48	0.069	–8	0.644	–123
1000	0.684	–145	2.23	48	0.068	–8	0.643	–123

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 100 mA)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
5	1.002	–1	7.98	179	0.001	80	0.966	–1
10	0.999	–3	7.99	178	0.003	105	0.969	–2
15	0.999	–4	8.03	176	0.005	87	0.962	–3
20	0.998	–6	7.99	175	0.007	72	0.959	–4
25	0.999	–7	8.00	174	0.008	82	0.959	–5
30	0.997	–9	7.97	173	0.010	89	0.962	–6
35	0.999	–10	7.95	172	0.012	85	0.961	–7
40	0.996	–12	7.94	170	0.014	74	0.962	–8
45	0.994	–13	7.95	169	0.015	77	0.960	–9
50	0.991	–15	7.91	168	0.017	79	0.959	–10
55	0.990	–16	7.88	167	0.017	83	0.959	–11
60	0.988	–18	7.91	165	0.021	77	0.957	–12
65	0.989	–19	7.85	164	0.020	76	0.957	–13
70	0.983	–20	7.83	163	0.022	74	0.954	–15
75	0.981	–22	7.80	162	0.025	78	0.952	–16
80	0.980	–23	7.76	161	0.026	73	0.948	–17
85	0.979	–25	7.72	160	0.026	72	0.946	–18
90	0.977	–26	7.67	158	0.029	72	0.944	–19
95	0.973	–28	7.68	157	0.030	68	0.939	–19
100	0.970	–29	7.62	156	0.031	68	0.934	–20
105	0.970	–30	7.60	155	0.031	68	0.932	–21
109	0.967	–32	7.54	154	0.034	66	0.931	–22
114	0.961	–33	7.49	153	0.034	67	0.926	–23
119	0.960	–34	7.46	152	0.036	66	0.925	–24
124	0.956	–36	7.42	150	0.038	65	0.923	–25
129	0.954	–37	7.41	149	0.039	65	0.923	–26
134	0.948	–38	7.35	148	0.041	63	0.920	–27
139	0.946	–40	7.29	147	0.042	61	0.916	–28
144	0.944	–41	7.25	146	0.044	61	0.913	–29
149	0.939	–42	7.20	145	0.044	60	0.909	–30
154	0.939	–43	7.17	144	0.046	60	0.904	–31
159	0.935	–45	7.11	143	0.046	58	0.900	–32
164	0.932	–46	7.06	142	0.048	57	0.897	–33
169	0.928	–47	7.01	141	0.049	59	0.891	–34
174	0.927	–48	6.94	140	0.049	55	0.885	–34
179	0.922	–49	6.89	139	0.051	55	0.882	–35
184	0.918	–51	6.85	138	0.052	54	0.883	–36
189	0.915	–52	6.82	137	0.053	53	0.878	–36
194	0.912	–53	6.78	136	0.053	50	0.874	–37
199	0.904	–54	6.71	135	0.054	52	0.867	–38
204	0.902	–55	6.65	134	0.054	51	0.868	–39
209	0.902	–56	6.62	133	0.056	50	0.866	–39

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 100 mA) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
214	0.898	–58	6.57	132	0.058	50	0.863	–40
219	0.896	–59	6.52	132	0.059	49	0.858	–41
224	0.888	–60	6.47	131	0.059	48	0.850	–42
229	0.887	–61	6.42	130	0.060	46	0.847	–43
234	0.885	–62	6.36	129	0.061	46	0.846	–44
239	0.882	–63	6.35	128	0.062	46	0.837	–45
244	0.876	–64	6.25	127	0.062	45	0.833	–45
249	0.872	–65	6.19	126	0.063	43	0.829	–46
254	0.869	–66	6.15	125	0.064	43	0.828	–47
259	0.867	–67	6.09	125	0.065	43	0.823	–47
264	0.863	–68	6.06	124	0.065	42	0.818	–48
269	0.860	–69	6.01	123	0.065	42	0.816	–48
274	0.856	–70	5.95	122	0.067	41	0.815	–49
279	0.854	–71	5.91	121	0.068	40	0.812	–50
284	0.848	–72	5.87	120	0.068	39	0.809	–50
289	0.849	–73	5.84	120	0.068	38	0.807	–51
294	0.845	–74	5.78	119	0.069	38	0.805	–52
299	0.840	–75	5.73	118	0.070	36	0.800	–53
304	0.839	–75	5.68	117	0.068	37	0.795	–53
308	0.840	–76	5.63	117	0.069	35	0.793	–54
313	0.835	–77	5.59	116	0.071	35	0.790	–55
318	0.832	–78	5.54	115	0.071	35	0.784	–55
323	0.829	–79	5.48	114	0.070	34	0.783	–56
328	0.829	–80	5.45	114	0.072	33	0.778	–56
333	0.825	–81	5.39	113	0.071	33	0.776	–57
338	0.821	–82	5.35	112	0.073	32	0.771	–58
343	0.818	–82	5.31	111	0.072	32	0.770	–58
348	0.816	–83	5.25	111	0.074	30	0.765	–59
353	0.814	–84	5.23	110	0.074	31	0.764	–59
358	0.810	–85	5.18	110	0.073	30	0.764	–59
363	0.810	–85	5.16	109	0.074	30	0.761	–60
368	0.807	–86	5.11	108	0.074	29	0.756	–61
373	0.805	–87	5.07	107	0.075	29	0.760	–61
378	0.801	–88	5.03	107	0.075	27	0.753	–62
383	0.799	–88	4.98	106	0.075	27	0.752	–62
388	0.796	–89	4.94	105	0.074	27	0.748	–63
393	0.796	–90	4.88	105	0.077	26	0.748	–63
398	0.790	–91	4.85	104	0.075	26	0.743	–64
403	0.794	–91	4.82	103	0.076	25	0.739	–64
408	0.789	–92	4.78	103	0.077	26	0.738	–65
413	0.785	–92	4.73	102	0.076	25	0.736	–66
418	0.788	–93	4.70	102	0.076	24	0.732	–66

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 100 mA) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
423	0.783	–94	4.66	101	0.077	24	0.730	–66
428	0.784	–95	4.64	101	0.079	23	0.728	–67
433	0.779	–95	4.60	100	0.078	23	0.727	–67
438	0.779	–96	4.55	99	0.078	22	0.727	–68
443	0.775	–97	4.52	99	0.077	21	0.725	–68
448	0.778	–98	4.51	98	0.078	21	0.725	–69
453	0.776	–98	4.46	98	0.078	21	0.719	–69
458	0.771	–99	4.43	97	0.078	21	0.720	–70
463	0.771	–99	4.39	96	0.079	20	0.723	–70
468	0.769	–100	4.36	95	0.079	19	0.716	–71
473	0.767	–100	4.31	95	0.079	18	0.716	–71
478	0.765	–101	4.28	95	0.078	20	0.716	–72
483	0.764	–101	4.24	94	0.079	19	0.710	–72
488	0.763	–102	4.22	94	0.079	19	0.711	–72
493	0.762	–103	4.18	93	0.079	18	0.709	–73
498	0.760	–103	4.15	93	0.080	17	0.706	–73
503	0.760	–104	4.12	92	0.079	16	0.705	–74
507	0.758	–104	4.10	91	0.079	17	0.701	–74
512	0.758	–105	4.08	91	0.079	16	0.700	–74
517	0.751	–105	4.03	90	0.078	16	0.700	–75
522	0.750	–106	4.00	90	0.080	15	0.700	–75
527	0.753	–106	4.00	89	0.079	16	0.698	–76
532	0.750	–107	3.96	89	0.079	14	0.699	–76
537	0.749	–107	3.94	88	0.079	15	0.696	–76
542	0.748	–108	3.90	87	0.080	13	0.696	–77
547	0.749	–109	3.88	87	0.080	13	0.697	–77
552	0.750	–109	3.85	87	0.079	14	0.693	–78
557	0.747	–110	3.82	86	0.078	13	0.697	–78
562	0.743	–110	3.78	86	0.079	12	0.695	–79
567	0.744	–111	3.75	85	0.079	12	0.689	–79
572	0.742	–111	3.73	85	0.078	11	0.690	–79
577	0.743	–112	3.70	84	0.080	12	0.689	–80
582	0.743	–112	3.67	84	0.080	11	0.691	–80
587	0.742	–112	3.64	83	0.078	11	0.688	–80
592	0.740	–113	3.62	83	0.080	10	0.685	–81
597	0.741	–113	3.61	82	0.078	10	0.682	–81
602	0.739	–114	3.59	82	0.078	10	0.685	–82
607	0.736	–114	3.56	82	0.079	9	0.682	–82
612	0.737	–115	3.53	81	0.077	9	0.684	–82
617	0.735	–115	3.52	81	0.078	10	0.682	–82
622	0.736	–115	3.50	80	0.078	9	0.680	–83
627	0.732	–116	3.47	80	0.078	8	0.681	–83

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 100 mA) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
632	0.733	–117	3.45	79	0.077	8	0.682	–84
637	0.730	–117	3.41	79	0.078	8	0.684	–84
642	0.731	–117	3.40	78	0.077	8	0.683	–85
647	0.728	–118	3.37	78	0.077	7	0.679	–85
652	0.730	–118	3.35	77	0.077	8	0.679	–85
657	0.725	–119	3.32	77	0.077	7	0.679	–85
662	0.725	–119	3.29	76	0.079	6	0.679	–86
667	0.727	–120	3.27	76	0.078	5	0.677	–86
672	0.731	–120	3.26	75	0.077	6	0.676	–86
677	0.727	–120	3.24	75	0.077	5	0.675	–87
682	0.725	–121	3.21	75	0.077	4	0.673	–87
687	0.726	–121	3.19	74	0.078	6	0.672	–87
692	0.724	–121	3.17	74	0.076	6	0.672	–88
697	0.728	–122	3.17	74	0.075	6	0.672	–88
702	0.724	–122	3.13	73	0.075	5	0.672	–88
706	0.724	–122	3.12	73	0.077	5	0.670	–89
711	0.722	–123	3.10	72	0.077	5	0.674	–89
716	0.722	–123	3.09	72	0.076	4	0.676	–89
721	0.723	–124	3.08	71	0.075	2	0.674	–90
726	0.720	–124	3.05	71	0.075	4	0.672	–90
731	0.719	–124	3.03	70	0.075	4	0.676	–90
736	0.720	–125	3.02	70	0.076	3	0.675	–91
741	0.716	–125	2.99	70	0.075	2	0.672	–91
746	0.718	–126	2.98	69	0.075	3	0.677	–91
751	0.715	–126	2.97	69	0.075	3	0.670	–92
756	0.717	–126	2.94	68	0.075	3	0.673	–92
761	0.716	–127	2.92	68	0.075	2	0.668	–92
766	0.717	–127	2.90	67	0.075	2	0.673	–93
771	0.717	–128	2.88	67	0.073	2	0.669	–93
776	0.714	–128	2.86	67	0.076	1	0.668	–93
781	0.718	–128	2.86	66	0.074	1	0.668	–93
786	0.718	–129	2.85	66	0.073	1	0.670	–94
791	0.718	–129	2.82	66	0.073	1	0.670	–94
796	0.716	–129	2.81	65	0.072	0	0.668	–94
801	0.715	–130	2.79	65	0.073	–1	0.671	–95
806	0.718	–130	2.77	65	0.071	1	0.669	–95
811	0.714	–130	2.77	64	0.072	0	0.672	–95
816	0.714	–130	2.74	64	0.072	0	0.673	–96
821	0.714	–131	2.72	63	0.070	0	0.671	–96
826	0.715	–131	2.71	63	0.073	0	0.675	–96
831	0.713	–131	2.69	63	0.071	0	0.672	–96
836	0.713	–131	2.68	62	0.072	–1	0.672	–97

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 100 mA) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
841	0.712	–132	2.67	62	0.069	0	0.671	–97
846	0.710	–132	2.65	61	0.071	–1	0.672	–97
851	0.708	–132	2.63	61	0.071	–1	0.670	–97
856	0.712	–133	2.62	61	0.071	–2	0.669	–98
861	0.710	–133	2.61	61	0.071	–2	0.669	–98
866	0.710	–134	2.59	60	0.071	–2	0.669	–98
871	0.710	–134	2.58	60	0.071	–2	0.669	–98
876	0.713	–134	2.57	59	0.069	–3	0.666	–99
881	0.711	–135	2.56	59	0.068	–3	0.667	–99
886	0.710	–135	2.54	59	0.069	–3	0.666	–99
891	0.711	–135	2.52	58	0.067	–3	0.668	–100
896	0.711	–136	2.52	58	0.070	–2	0.670	–100
901	0.709	–136	2.50	57	0.069	–5	0.669	–101
905	0.711	–136	2.49	57	0.069	–3	0.671	–101
910	0.711	–136	2.47	57	0.068	–4	0.674	–101
915	0.710	–137	2.46	56	0.068	–2	0.673	–101
920	0.712	–137	2.45	56	0.066	–4	0.673	–102
925	0.708	–137	2.42	56	0.067	–4	0.673	–102
930	0.709	–137	2.42	55	0.068	–3	0.673	–102
935	0.709	–138	2.41	55	0.066	–4	0.670	–102
940	0.709	–138	2.40	55	0.066	–2	0.672	–102
945	0.709	–138	2.39	54	0.065	–3	0.672	–103
950	0.708	–139	2.38	54	0.066	–4	0.671	–103
955	0.711	–139	2.36	54	0.065	–5	0.669	–103
960	0.709	–139	2.35	54	0.064	–4	0.672	–103
965	0.708	–140	2.34	53	0.064	–3	0.671	–104
970	0.707	–140	2.33	53	0.065	–5	0.673	–104
975	0.706	–140	2.32	52	0.065	–4	0.671	–104
980	0.707	–140	2.30	52	0.065	–4	0.669	–104
985	0.707	–140	2.29	51	0.064	–6	0.674	–105
990	0.708	–141	2.28	51	0.063	–4	0.674	–105
995	0.708	–141	2.28	51	0.063	–5	0.674	–105
1000	0.710	–141	2.26	50	0.063	–5	0.676	–106

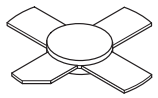
The RF MOSFET Line
Power Field Effect Transistor
N–Channel Enhancement–Mode MOSFET

Designed primarily for wideband large–signal output and driver from 30–500 MHz.

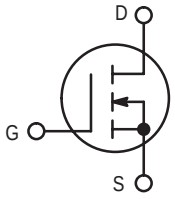
- Typical Performance at 400 MHz, 28 Vdc
  Output Power = 4.0 Watts
  Gain = 17 dB
  Efficiency = 50%
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Low C_{rss} – 0.8 pF Typical at V_{DS} = 28 Volts
- S–Parameters Available for Download into Frequency Domain Simulators. See http://motorola.com/sps/rf/designtds/

MRF160

4.0 W, to 400 MHz
MOSFET BROADBAND
RF POWER FET



CASE 249–06, STYLE 3



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Gate Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	± 40	Vdc
Drain Current–Continuous	I_D	1.0	ADC
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	24 0.14	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

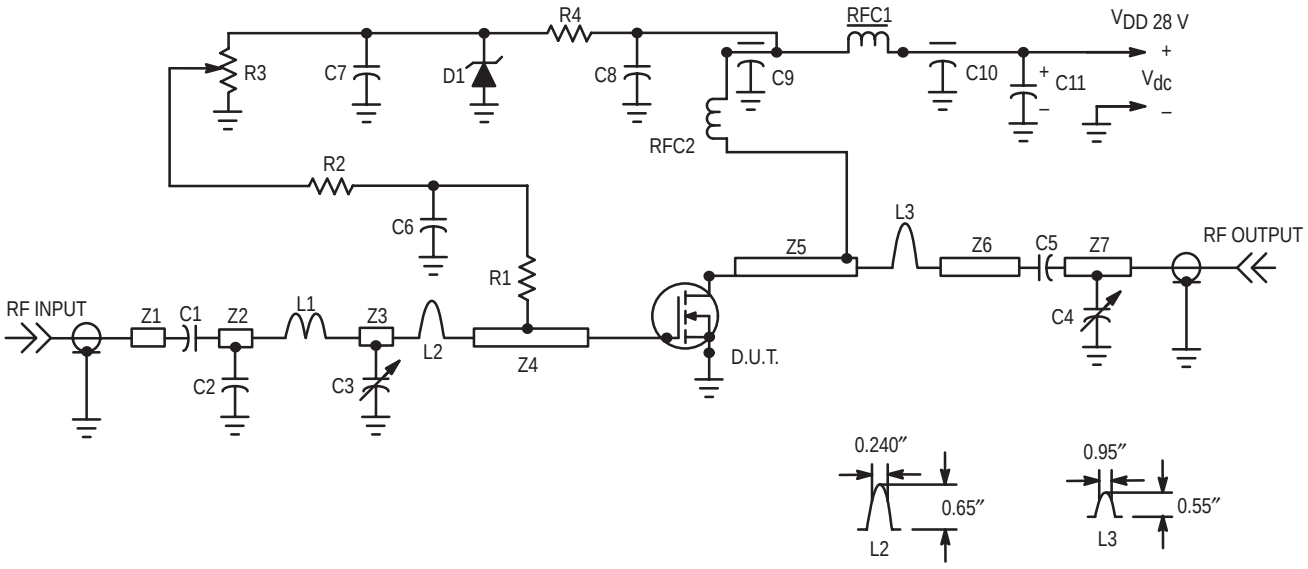
THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	7.2	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{DS} = 0 Vdc, V_{GS} = 0 Vdc, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 V)	I_{DSS}	—	—	0.8	mA
Gate–Source Leakage Current (V_{GS} = 40 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1.0	μA
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 10 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain Source On–Voltage ($V_{DS\ (on)}$, V_{GS} = 10 Vdc, I_D = 500 mA)	$V_{DS(on)}$	—	3.8	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 250 mA)	g_{fs}	110	160	—	mS
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	6.0	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{oss}	—	8.0	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{rss}	—	0.8	—	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 4.0 W, f = 400 MHz, I_{DQ} = 50 mA)	G_{ps}	15	17	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 4.0 W, f = 400 MHz, I_{DQ} = 50 mA)	η	45	50	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 4.0 W, f = 400 MHz, I_{DQ} = 50 mA) Load VSWR = 30:1 at All Phase Angles at Frequency of Test	ψ	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{DD} = 28 Vdc, P_{out} = 4.0 W, f = 400 MHz, I_{DQ} = 50 mA)	Z_{in}	—	5.23–j 27.2	—	Ohms
Series Equivalent Output Impedance (V_{DD} = 28 Vdc, P_{out} = 4.0 W, f = 400 MHz, I_{DQ} = 50 mA)	Z_{out}	—	14.7–j 31.2	—	Ohms



C1, C5	220 pF, Chip Capacitor	R3	10 kΩ, 10 Turns Bourns
C2	18 pF, ATC Chip Capacitor	R4	1.8 kΩ, 1/4 Watt
C3	2.0–20 pF, Johanson Trimmer Capacitor	RFC1	Ferroxcube VK200–19/4B
C4	2.0–10 pF, Johanson Trimmer Capacitor	RFC2	10 Turns, #20 AWG, Enameled Close Wound, 0.250″ ID
C6, C7, C8	0.1 μF		
C9, C10	680 pF, Feed Through	Z1	Microstrip Line 0.167″ wide, 0.820″ long
C11	50 μF, 50 V	Z2	Microstrip Line 0.240″ wide, 0.240″ long
L1	#20 AWG, 1 Turn 0.255″ ID	Z3	Microstrip Line 0.240″ wide, 0.240″ long
L2	#20 AWG, Hairpin 1.3″ long, bend into hairpin	Z4	Microstrip Line 0.230″ wide, 0.590″ long
L3	#20 AWG, Hairpin 1.1″ long, bend into hairpin	Z5	Microstrip Line 0.230″ wide, 0.580″ long
R1	160 Ω, 1/2 Watt	Z6	Microstrip Line 0.167″ wide, 0.620″ long
R2	10 kΩ, 1/2 Watt	Z7	Microstrip Line 0.167″ wide, 0.800″ long

Board Material 0.060″ Glass Teflon® 2 oz. Copper clad both sides ε_r = 2.55

Figure 1. 400 MHz Test Circuit

Typical Characteristics

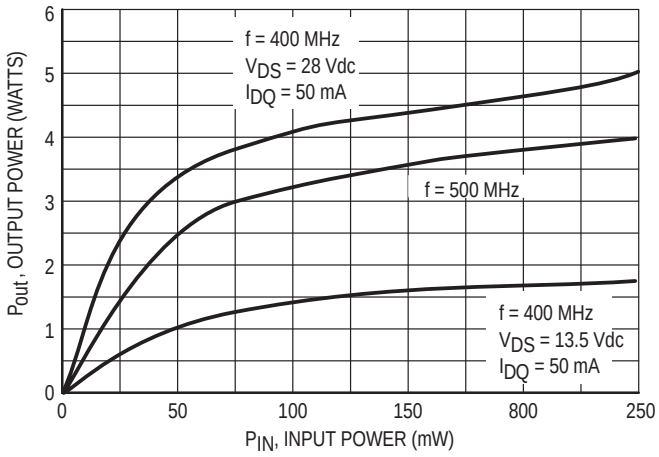


Figure 2. Output Power versus Input Power

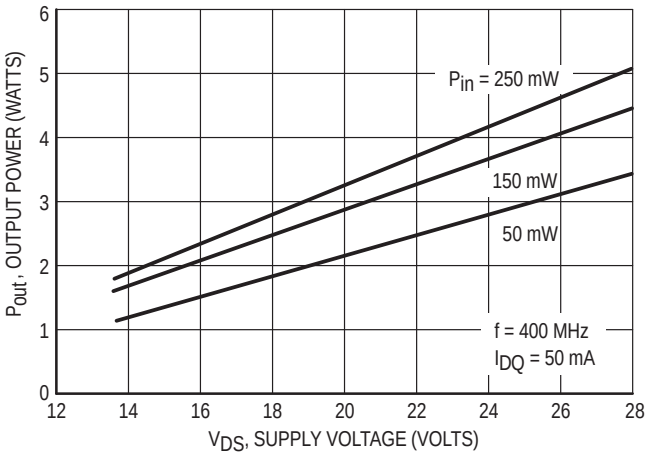


Figure 3. Output Power versus Voltage

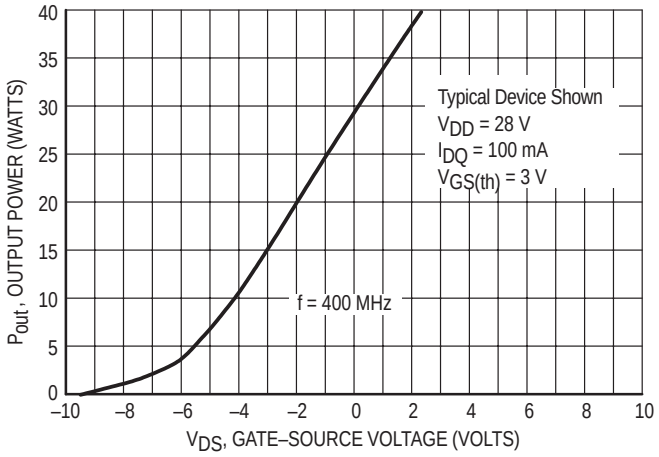


Figure 4. Output Power versus Gate Voltage

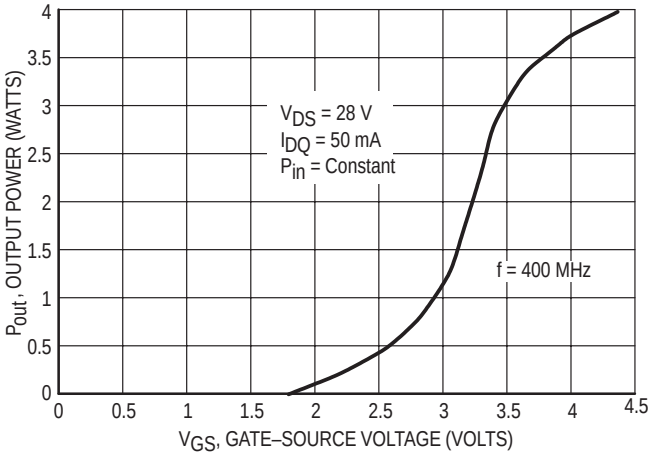


Figure 5. Output Power versus Gate Voltage

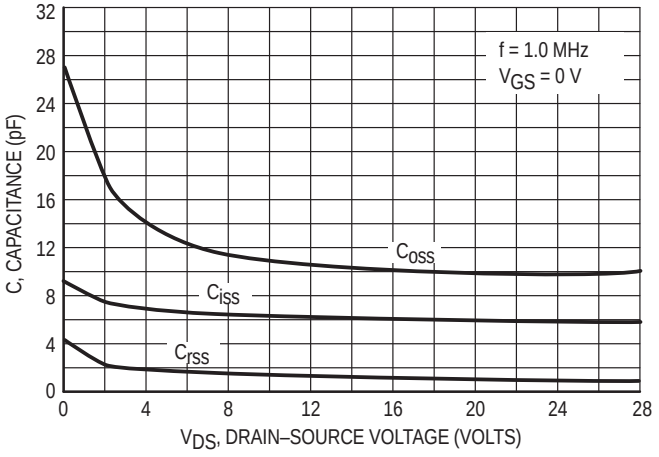


Figure 6. Capacitance versus Drain–Source Voltage

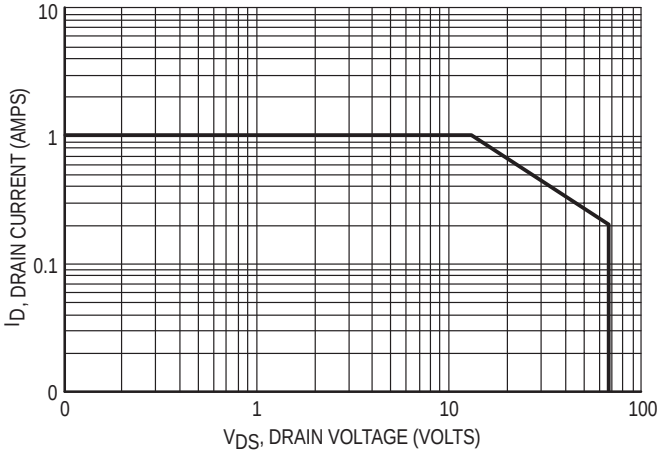


Figure 7. DC Safe Operating Area

Table 1. Common Source S–Parameters (V_{DS} = 12.5 V, I_D = 120 mA)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.991	–19	15.80	166	0.019	77	0.938	–19
40	0.970	–25	15.50	161	0.025	72	0.933	–25
50	0.959	–31	15.20	156	0.030	67	0.918	–31
60	0.943	–37	14.80	151	0.035	63	0.900	–37
70	0.925	–42	14.30	147	0.040	59	0.880	–42
80	0.912	–48	13.90	143	0.044	56	0.863	–47
85	0.903	–51	13.70	141	0.046	54	0.857	–49
90	0.896	–53	13.50	139	0.048	52	0.851	–52
100	0.872	–58	12.90	135	0.051	48	0.830	–57
110	0.853	–63	12.40	131	0.054	46	0.812	–60
120	0.841	–67	11.90	128	0.056	43	0.796	–63
130	0.831	–71	11.50	126	0.059	40	0.788	–67
140	0.814	–75	11.10	122	0.061	37	0.777	–70
150	0.797	–79	10.70	119	0.063	34	0.760	–74
160	0.782	–82	10.20	117	0.064	32	0.739	–78
170	0.776	–85	9.81	115	0.066	32	0.740	–79
180	0.769	–89	9.55	112	0.068	28	0.737	–83
190	0.754	–92	9.24	109	0.069	25	0.725	–87
200	0.737	–94	8.83	107	0.068	23	0.707	–90
210	0.731	–96	8.47	105	0.068	22	0.692	–92
220	0.730	–99	8.20	103	0.069	21	0.692	–94
230	0.724	–101	7.94	101	0.071	20	0.697	–95
240	0.713	–104	7.69	99	0.072	16	0.696	–99
250	0.705	–106	7.44	97	0.070	15	0.676	–100
260	0.699	–108	7.18	96	0.070	15	0.673	–102
270	0.697	–109	6.91	94	0.070	14	0.661	–103
280	0.697	–111	6.70	93	0.071	13	0.654	–104
290	0.693	–113	6.54	92	0.071	11	0.658	–106
300	0.686	–115	6.36	90	0.072	9	0.664	–108
310	0.679	–116	6.12	88	0.069	7	0.639	–111
320	0.679	–117	5.96	87	0.070	9	0.642	–110
330	0.679	–119	5.80	86	0.070	8	0.648	–112
340	0.679	–121	5.63	84	0.071	7	0.648	–114
350	0.674	–122	5.47	83	0.070	5	0.645	–114
360	0.669	–123	5.33	82	0.070	4	0.650	–116
370	0.667	–124	5.18	80	0.068	3	0.644	–118
380	0.672	–125	5.02	80	0.066	3	0.614	–119
390	0.675	–127	4.96	78	0.071	4	0.655	–116
400	0.672	–129	4.83	77	0.070	2	0.655	–119
410	0.668	–130	4.70	75	0.069	0	0.654	–121
420	0.666	–131	4.56	74	0.067	–1	0.644	–122
430	0.667	–131	4.48	74	0.066	–1	0.646	–122

Table 1. Common Source S–Parameters (V_{DS} = 12.5 V, I_D = 120 mA) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
440	0.671	–132	4.39	72	0.066	–1	0.651	–123
450	0.670	–134	4.29	71	0.068	–1	0.663	–123
460	0.662	–135	4.15	70	0.067	–6	0.677	–127
470	0.663	–135	4.05	69	0.065	–5	0.664	–127
480	0.666	–136	3.95	68	0.064	–5	0.663	–128
490	0.670	–137	3.88	67	0.064	–5	0.663	–128
500	0.670	–138	3.81	66	0.063	–6	0.670	–128
600	0.693	–147	3.06	55	0.053	–17	0.689	–136
700	0.708	–152	2.61	46	0.044	–14	0.723	–142
800	0.731	–158	2.22	40	0.037	–15	0.733	–146
900	0.724	–165	1.93	32	0.037	–32	0.760	–151
1000	0.748	–169	1.73	28	0.027	–6	0.778	–153

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 250 mA)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.995	–18	15.00	167	0.014	78	0.919	–15
40	0.978	–24	14.70	162	0.018	73	0.913	–19
50	0.971	–30	14.50	158	0.022	69	0.900	–23
60	0.961	–36	14.20	153	0.026	65	0.885	–28
70	0.947	–41	13.80	149	0.029	62	0.867	–32
80	0.938	–46	13.40	145	0.033	58	0.851	–35
85	0.932	–49	13.30	143	0.034	56	0.845	–37
90	0.927	–51	13.10	141	0.036	55	0.839	–39
100	0.908	–56	12.70	138	0.038	51	0.825	–43
110	0.893	–61	12.20	134	0.040	49	0.802	–46
120	0.884	–65	11.80	131	0.043	46	0.788	–48
130	0.875	–69	11.40	128	0.045	44	0.781	–51
140	0.862	–74	11.10	125	0.047	40	0.772	–54
150	0.848	–78	10.70	122	0.048	37	0.754	–57
160	0.836	–81	10.30	119	0.049	35	0.733	–60
170	0.830	–84	9.86	117	0.050	35	0.718	–60
180	0.824	–88	9.64	115	0.053	31	0.729	–64
190	0.813	–91	9.38	112	0.053	29	0.719	–67
200	0.798	–94	9.00	109	0.053	26	0.701	–70
210	0.792	–96	8.63	107	0.053	25	0.682	–72
220	0.790	–98	8.36	105	0.054	24	0.677	–73
230	0.785	–101	8.10	104	0.055	22	0.677	–75
240	0.777	–104	7.92	101	0.057	19	0.694	–78
250	0.769	–106	7.65	99	0.055	18	0.663	–80
260	0.764	–108	7.40	97	0.055	18	0.662	–81
270	0.761	–109	7.13	96	0.055	17	0.649	–82
280	0.760	–111	6.91	95	0.055	16	0.640	–82

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 250 mA) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
290	0.757	–113	6.75	93	0.055	14	0.641	–84
300	0.751	–115	6.59	91	0.056	12	0.645	–86
310	0.743	–117	6.37	89	0.055	9	0.635	–90
320	0.744	–118	6.17	88	0.054	11	0.619	–89
330	0.744	–120	6.01	87	0.055	11	0.628	–90
340	0.743	–121	5.85	85	0.055	10	0.629	–92
350	0.738	–123	5.70	84	0.055	8	0.629	–92
360	0.733	–124	5.55	82	0.054	6	0.631	–94
370	0.730	–126	5.40	81	0.054	4	0.623	–96
380	0.732	–127	5.21	80	0.052	4	0.593	–98
390	0.737	–129	5.17	79	0.055	7	0.627	–93
400	0.734	–130	5.04	77	0.055	4	0.639	–97
410	0.731	–131	4.92	76	0.054	3	0.641	–99
420	0.728	–132	4.78	75	0.052	1	0.630	–100
430	0.729	–133	4.67	74	0.051	0	0.628	–101
440	0.731	–134	4.57	72	0.051	1	0.626	–102
450	0.731	–136	4.47	71	0.053	1	0.630	–102
460	0.723	–137	4.37	69	0.054	–4	0.673	–106
470	0.724	–137	4.24	68	0.050	–3	0.647	–107
480	0.727	–138	4.13	68	0.049	–3	0.642	–108
490	0.730	–139	4.05	67	0.048	–3	0.641	–107
500	0.730	–140	3.99	66	0.048	–4	0.647	–108
600	0.736	–150	3.54	56	0.037	–14	0.657	–118
700	0.745	–156	2.99	46	0.029	–9	0.699	–126
800	0.765	–161	2.54	39	0.025	–5	0.713	–131
900	0.759	–168	2.20	31	0.022	–34	0.742	–136
1000	0.769	–173	1.98	27	0.018	19	0.756	–139

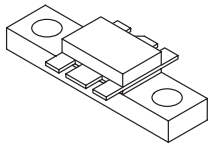
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement Mode MOSFETs

MRF166C

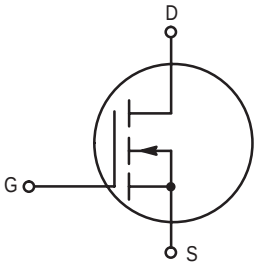
20 W, 500 MHz
MOSFET
BROADBAND
RF POWER FETs

Designed primarily for wideband large–signal output and driver from 30–500 MHz.

- MRF166C — Guaranteed Performance at 500 MHz, 28 Vdc
  Output Power = 20 W
  Gain = 13.5 dB
  Efficiency = 50%
- Replacement for Industry Standards such as MRF136, DV2820, BLF244, SD1902, and ST1001
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Low C_{rss} — 4.0 pF @ V_{DS} = 28 V
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.
- S–Parameters Available for Download into Frequency Domain Simulators. See http://mot–sps.com/rf/designtds/



CASE 319–07, STYLE 3



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Gate Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Adc
Drain Current — Continuous	I_D	4.0	Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	70 0.4	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Operating Junction Temperature	T_J	200	°C

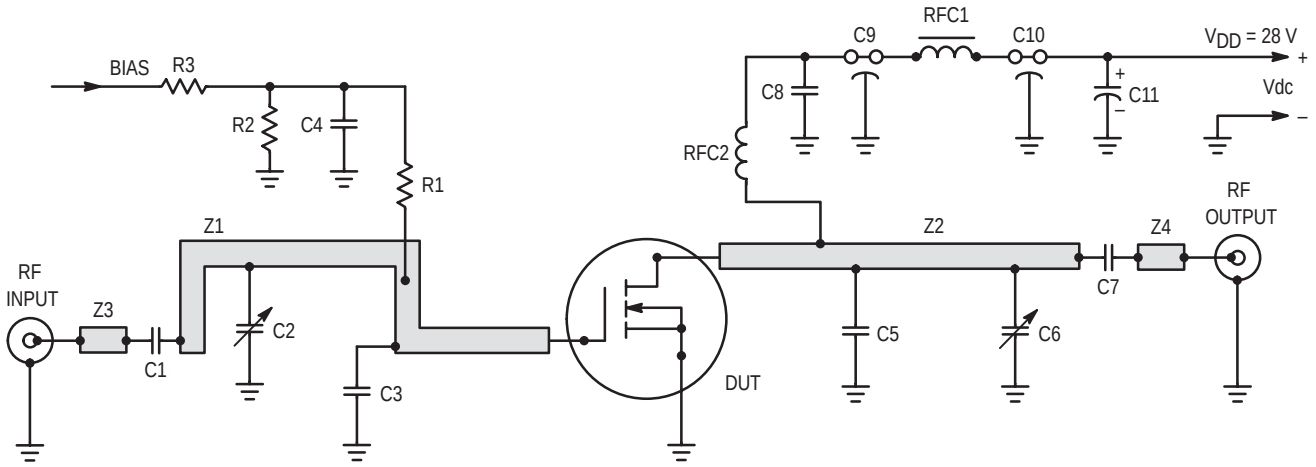
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

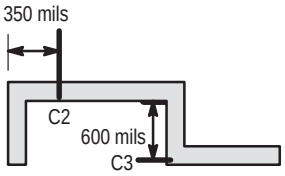
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 V, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	V
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	0.5	mA
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0 V)	I_{GSS}	—	—	1.0	μA
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.5	3.0	4.5	V
Forward Transconductance (V_{DS} = 10 V, I_D = 1.5 A)	g_{fs}	0.8	1.1	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	28	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{oss}	—	30	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{rss}	—	4.0	—	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 20 W, f = 500 MHz, I_{DQ} = 25 mA)	G_{ps}	13.5	16	—	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 20 W, f = 500 MHz, I_{DQ} = 25 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 28 V, P_{out} = 20 W, f = 500 MHz, I_{DQ} = 25 mA, Load VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			

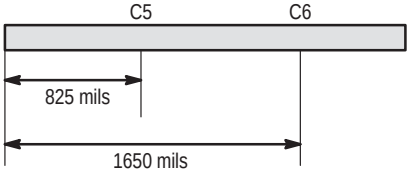


C1, C7	200 pF, Chip Capacitor
C2, C6	2–10 pF, Trimmer Capacitor, Johansen
C3	27 pF, ATC 100 mil Chip Capacitor
C4, C8	0.1 μF, Chip Capacitor
C5	15 pF, ATC 100 mil Chip Capacitor
C9, C10	680 pF, Feedthru Capacitor
C11	50 μF, 50 V, Electrolytic Capacitor
R1	120 Ω, 1/2 W Resistor
R2	10 kΩ, 1/2 W Resistor
R3	1 kΩ, 1/2 W Resistor
RFC1	Ferroxcube VK200 19/4B
RFC2	10 Turns AWG #18, 0.125″ I.D., Enameled
Board Material	0.062″ Teflon® Fiberglass 1 oz. Copper Clad Both Sides ε_r = 2.56

Z1 0.120″ x 3.3″, Microstrip Line



Z2 0.120″ x 2.1″, Microstrip Line



Z3, Z4 0.120″ x 0.25″, Microstrip Line

Figure 1. MRF166C 500 MHz Test Circuit

TYPICAL CHARACTERISTICS

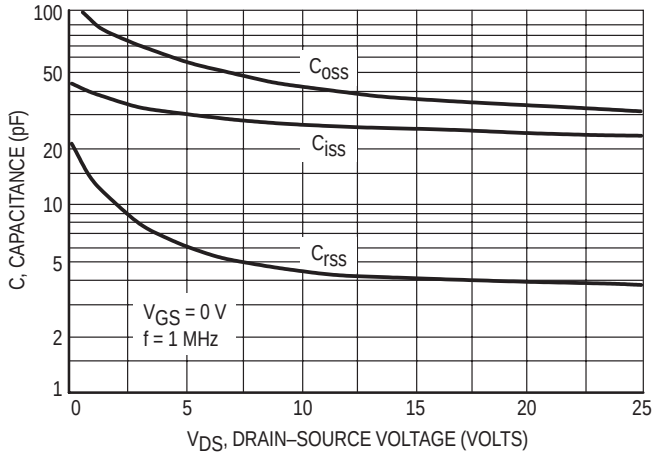


Figure 2. Capacitance versus Drain–Source Voltage

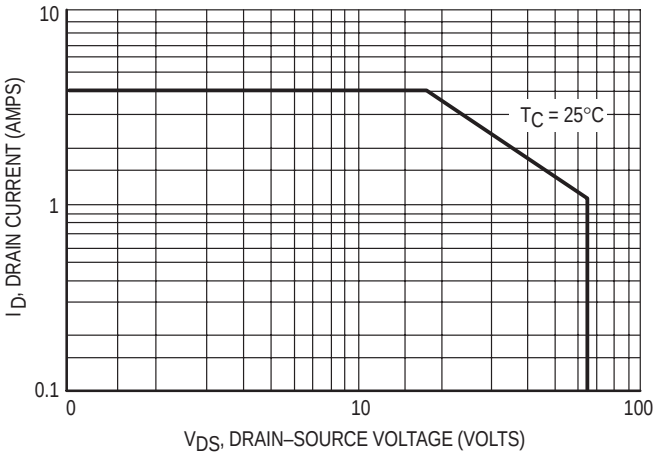


Figure 3. DC Safe Operating Area

TYPICAL CHARACTERISTICS

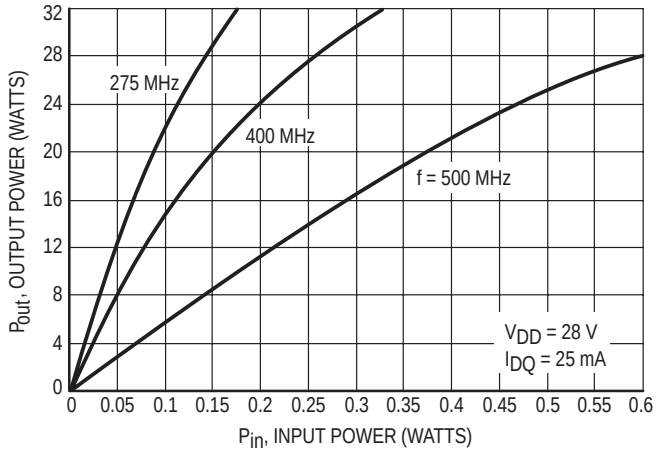


Figure 4. Output Power versus Input Power

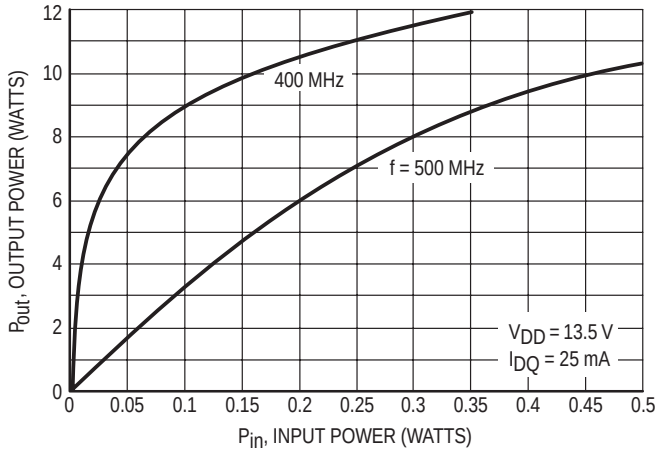


Figure 5. Output Power versus Input Power

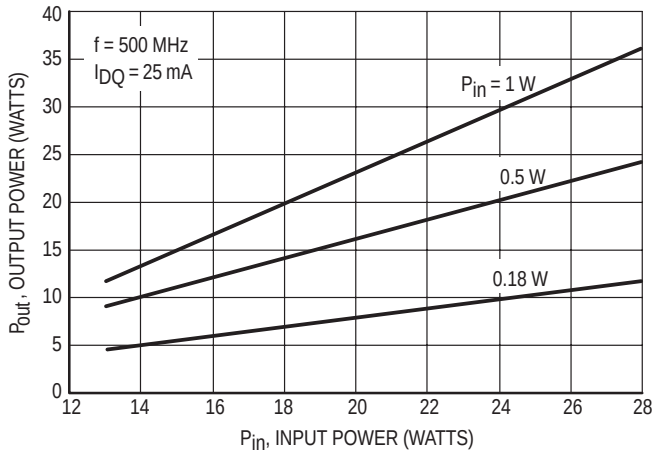


Figure 6. Output Power versus Supply Voltage

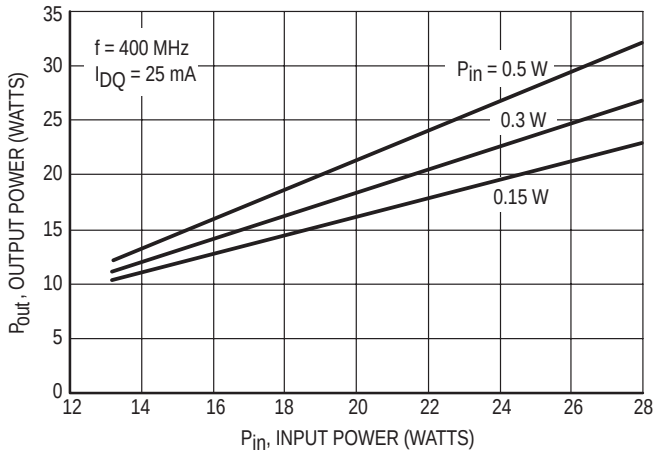
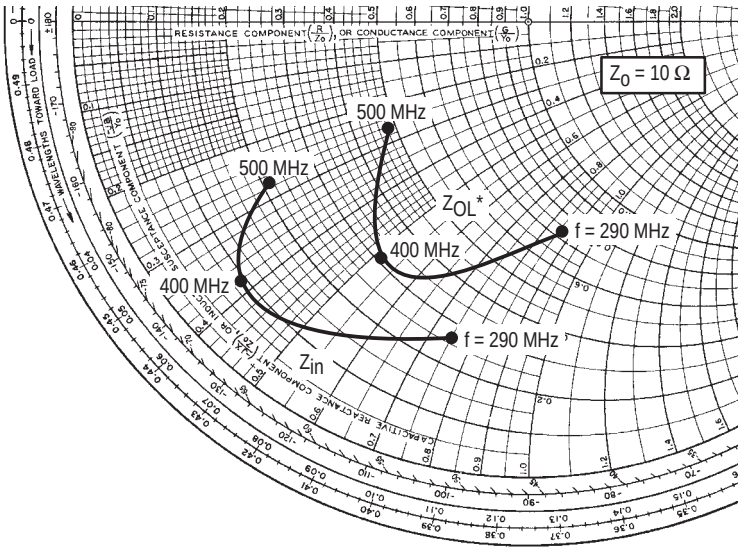


Figure 7. Output Power versus Supply Voltage



V_{DD} = 28 V, I_{DQ} = 25 mA, P_{out} = 20 Watts

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
500	2.09 – j2.77	4.87 – j2.63
400	0.93 – j3.80	3.09 – j5.24
290	2.63 – j7.58	7.35 – j8.67

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 8. Series Equivalent Input and Output Impedance

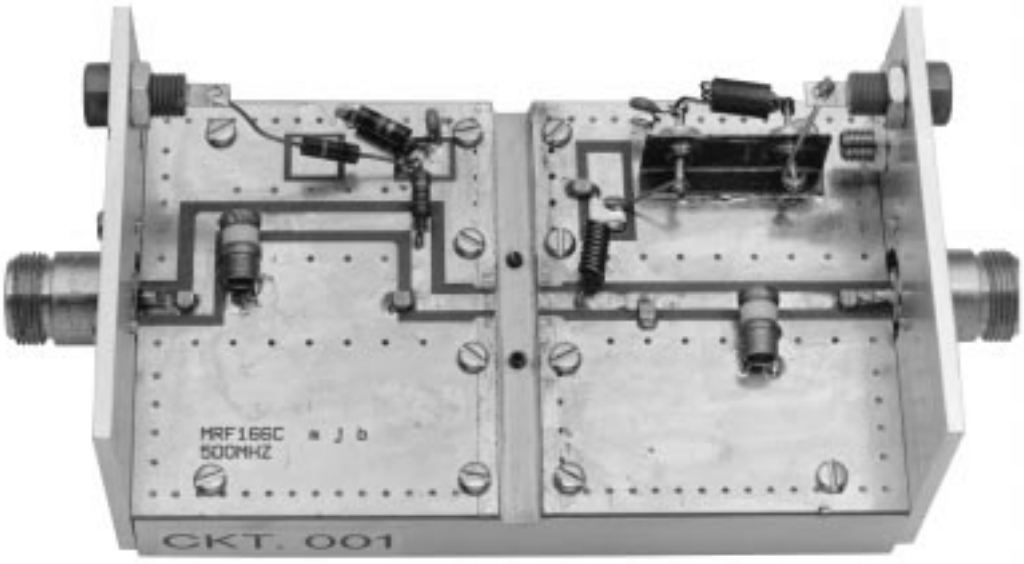


Figure 9. MRF166C Test Fixture

Table 1. Common Source S–Parameters (V_{DS} = 12.5 V, I_D = 1.25 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.840	–142	22.59	105	0.025	20	0.727	–155
40	0.836	–151	17.4	100	0.025	17	0.743	–161
50	0.832	–156	14.1	97	0.026	15	0.751	–164
60	0.829	–159	12.0	94	0.026	14	0.764	–166
70	0.826	–162	10.4	91	0.026	14	0.763	–168
80	0.822	–164	9.09	90	0.026	14	0.763	–169
90	0.818	–165	8.07	89	0.027	14	0.765	–170
100	0.819	–167	7.28	87	0.027	14	0.774	–171
110	0.821	–168	6.61	85	0.027	14	0.773	–172
120	0.821	–169	6.00	83	0.026	15	0.771	–172
130	0.820	–169	5.56	83	0.027	16	0.778	–172
140	0.818	–170	5.22	82	0.027	17	0.785	–172
150	0.820	–170	4.86	80	0.027	17	0.786	–173
160	0.821	–171	4.52	79	0.027	17	0.781	–173
170	0.820	–171	4.23	79	0.027	20	0.774	–172
180	0.820	–171	4.03	78	0.027	20	0.799	–173
190	0.820	–172	3.86	76	0.027	20	0.799	–174
200	0.821	–172	3.62	75	0.027	20	0.784	–175
210	0.822	–173	3.39	75	0.027	22	0.780	–174
220	0.823	–173	3.25	74	0.027	24	0.795	–173
230	0.825	–173	3.12	72	0.028	23	0.823	–175
240	0.827	–173	2.96	71	0.026	24	0.791	–175
250	0.827	–174	2.83	70	0.027	26	0.789	–174
260	0.827	–174	2.71	70	0.026	27	0.791	–174
270	0.829	–174	2.62	69	0.027	28	0.801	–174
280	0.831	–174	2.52	68	0.027	29	0.807	–175
290	0.832	–174	2.42	66	0.027	30	0.788	–175
300	0.832	–174	2.32	66	0.027	32	0.792	–175
310	0.831	–174	2.25	66	0.027	33	0.797	–174
320	0.833	–175	2.18	65	0.027	34	0.810	–174
330	0.836	–175	2.10	63	0.028	35	0.812	–175
340	0.837	–175	2.00	62	0.027	35	0.789	–176
350	0.838	–175	1.95	62	0.028	39	0.806	–173
360	0.839	–175	1.90	61	0.028	39	0.817	–174
370	0.840	–176	1.84	60	0.028	40	0.817	–175
380	0.843	–176	1.77	59	0.028	41	0.811	–175
390	0.845	–176	1.71	59	0.028	42	0.805	–175
400	0.846	–176	1.66	58	0.029	46	0.801	–172
410	0.846	–176	1.64	57	0.030	46	0.845	–174
420	0.847	–176	1.59	56	0.030	46	0.836	–176
430	0.848	–176	1.52	56	0.030	47	0.823	–176
440	0.850	–176	1.48	56	0.030	49	0.816	–174

Table 1. Common Source S–Parameters (V_{DS} = 12.5 V, I_D = 1.25 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
450	0.851	–176	1.47	54	0.032	51	0.851	–174
460	0.853	–177	1.42	53	0.032	48	0.849	–178
470	0.853	–177	1.37	53	0.031	51	0.830	–176
480	0.856	–177	1.34	53	0.032	53	0.834	–176
490	0.857	–177	1.32	52	0.033	54	0.841	–175
500	0.859	–177	1.28	51	0.034	54	0.847	–175
600	0.857	178	0.988	41	0.032	73	0.877	180
700	0.884	176	0.789	34	0.047	65	0.881	179
800	0.881	173	0.684	30	0.031	83	0.890	174
900	0.890	172	0.580	26	0.069	71	0.885	176
1000	0.897	170	0.503	24	0.090	60	0.931	173

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 1.25 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.842	–125	29.6	113	0.024	28	0.586	–136
40	0.831	–136	23.2	106	0.025	22	0.607	–145
50	0.822	–143	19.0	101	0.026	19	0.613	–151
60	0.816	–148	16.2	98	0.026	17	0.626	–155
70	0.812	–152	14.1	95	0.027	16	0.635	–157
80	0.806	–155	12.4	92	0.026	15	0.643	–159
90	0.801	–157	11.1	90	0.027	14	0.650	–160
100	0.802	–159	9.97	88	0.027	13	0.656	–161
110	0.805	–161	9.04	86	0.027	13	0.654	–163
120	0.805	–162	8.22	84	0.026	13	0.654	–163
130	0.803	–163	7.59	83	0.026	14	0.663	–163
140	0.801	–164	7.09	82	0.026	14	0.673	–164
150	0.803	–165	6.61	80	0.026	14	0.675	–164
160	0.804	–165	6.16	79	0.026	14	0.674	–164
170	0.803	–166	5.77	78	0.026	16	0.672	–164
180	0.804	–166	5.49	77	0.026	17	0.697	–164
190	0.806	–166	5.25	75	0.026	16	0.700	–165
200	0.806	–167	4.92	73	0.025	16	0.688	–166
210	0.807	–168	4.60	73	0.025	17	0.680	–165
220	0.809	–168	4.40	72	0.025	19	0.689	–165
230	0.812	–168	4.21	70	0.025	19	0.713	–167
240	0.814	–169	3.99	69	0.024	20	0.701	–167
250	0.815	–169	3.83	68	0.024	21	0.707	–166
260	0.816	–169	3.66	67	0.024	22	0.711	–166
270	0.818	–169	3.52	66	0.024	23	0.715	–166
280	0.821	–169	3.39	65	0.025	24	0.718	–167
290	0.822	–170	3.25	63	0.024	26	0.708	–168
300	0.823	–170	3.11	62	0.023	28	0.715	–167

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 1.25 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
310	0.822	–170	2.99	62	0.023	29	0.725	–166
320	0.825	–170	2.89	61	0.024	31	0.734	–166
330	0.828	–171	2.78	60	0.024	33	0.736	–167
340	0.830	–171	2.66	59	0.024	33	0.724	–168
350	0.832	–171	2.59	58	0.024	37	0.739	–166
360	0.834	–171	2.52	57	0.024	39	0.757	–166
370	0.836	–171	2.44	56	0.023	39	0.755	–167
380	0.839	–172	2.34	55	0.023	38	0.745	–167
390	0.840	–172	2.26	54	0.024	40	0.738	–168
400	0.841	–172	2.19	54	0.024	46	0.735	–166
410	0.842	–172	2.14	53	0.025	46	0.787	–167
420	0.844	–172	2.09	51	0.026	46	0.790	–168
430	0.845	–173	1.99	51	0.027	49	0.777	–168
440	0.846	–173	1.93	51	0.026	52	0.770	–167
450	0.849	–173	1.91	49	0.027	53	0.794	–167
460	0.853	–173	1.84	48	0.027	51	0.803	–171
470	0.855	–173	1.77	47	0.027	54	0.787	–170
480	0.857	–174	1.72	47	0.027	57	0.789	–169
490	0.857	–174	1.68	47	0.027	56	0.796	–168
500	0.859	–174	1.64	46	0.029	57	0.802	–169
600	0.862	–179	1.18	33	0.036	77	0.851	–173
700	0.893	178	0.921	26	0.043	75	0.856	–175
800	0.890	175	0.771	22	0.043	78	0.880	–178
900	0.895	173	0.635	17	0.065	74	0.882	–178
1000	0.905	171	0.544	14	0.086	69	0.931	178

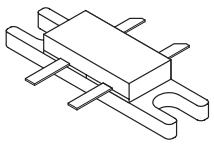
The RF MOSFET Line
Power Field Effect Transistor
N–Channel Enhancement–Mode MOSFET

MRF166W

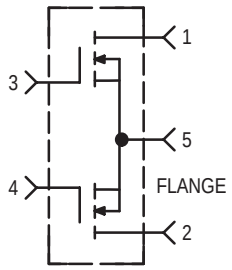
40 W, 500 MHz
TMOS BROADBAND
RF POWER FET

Designed primarily for wideband large–signal output and driver stages to 30 – 500 MHz.

- Push–Pull Configuration Reduces Even Numbered Harmonics
- Guaranteed Performance at 500 MHz, 28 Vdc
  Output Power = 40 Watts
  Gain = 14 dB
  Efficiency = 50%
- Typical Performance at 175 MHz, 28 Vdc
  Output Power = 40 Watts
  Gain = 17 dB
  Efficiency = 60%
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Low C_{rss} — 4.0 pF @ V_{DS} = 28 Volts
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.
- S–Parameters Available for Download into Frequency Domain Simulators. See http://motorola.com/sps/rf/designtds/



CASE 412–01, Style 1



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Gate Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	± 20	Adc
Drain Current — Continuous	I_D	8.0	ADC
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	175 1.0	Watts °C/W
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

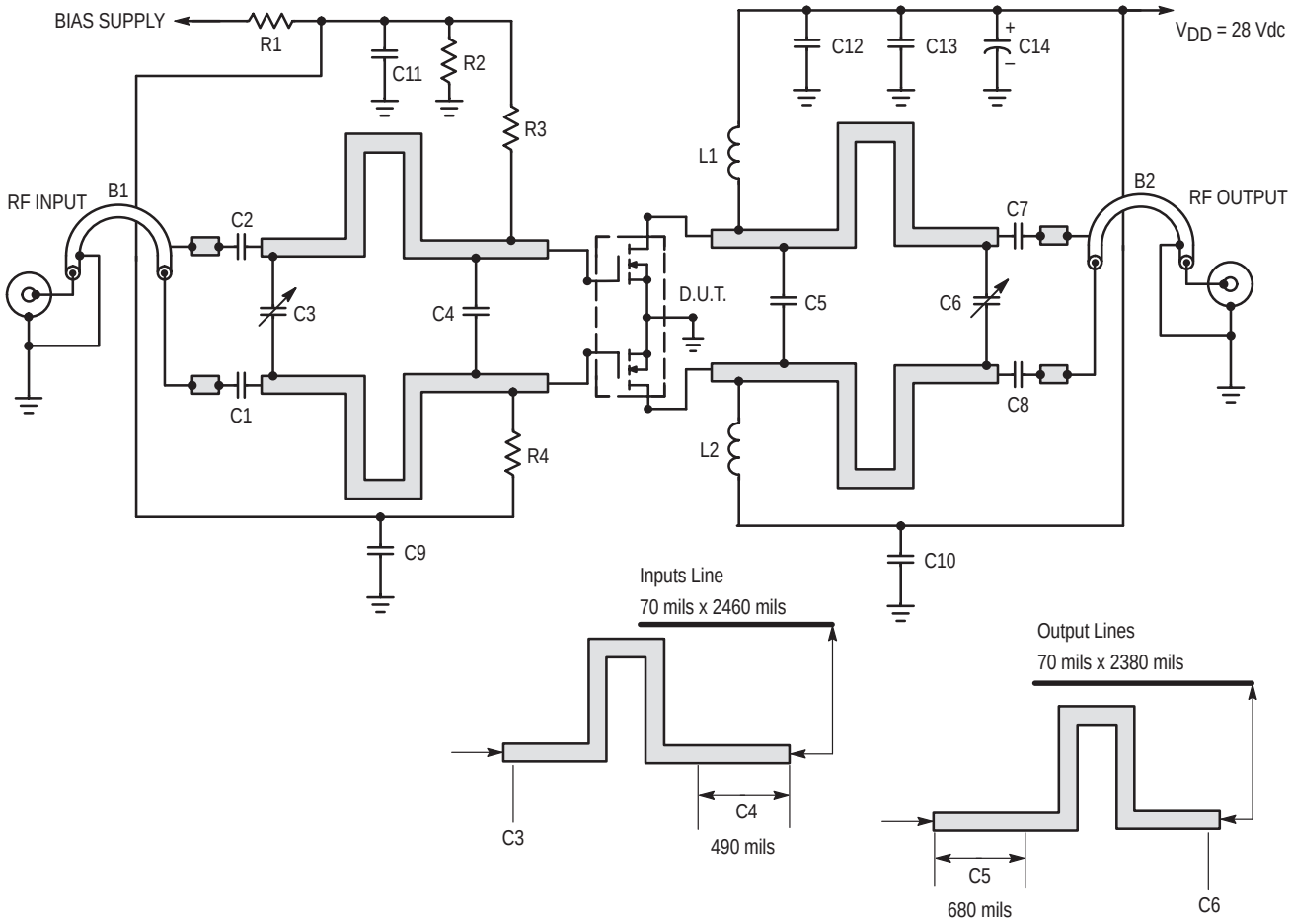
Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.0	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	0.5	mA
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1.0	μA
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS}= 10 Vdc, I_D = 25 mA)	$V_{GS(th)}$	1.5	3.0	4.5	Vdc
Forward Transconductance (V_{DS}= 10 Vdc, I_D = 1.5 A)	g_{fs}	0.9	1.1	—	mS
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	28	—	pF
Output Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{oss}	—	30	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{rss}	—	4.0	—	pF
FUNCTIONAL CHARACTERISTICS (2)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 40 W, f = 500 MHz, I_{DQ} = 100 mA)	G_{ps}	14	16	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 40 W, f = 500 MHz, I_{DQ} = 100 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 40 W, f = 500 MHz, I_{DQ} = 100 mA) Load VSWR = 30:1, All phase angles at frequency of test	Ψ	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{DD} = 28 Vdc, P_{out} = 40 W, f = 500 MHz, I_{DQ} = 100 mA)	Z_{in}	—	2.88 –j7.96	—	Ohms
Series Equivalent Output Impedance (V_{DD} = 28 Vdc, P_{out} = 40 W, f = 500 MHz, I_{DQ} = 100 mA)	Z_{out}	—	6.12 –j9.43	—	Ohms

(1) Each transistor chip measured separately.
(2) Both transistor chips operating in a push–pull amplifier.



C1, C2, C7, C8	220 pF, 100 mil Chip Capacitor, ATC
C3, C6	0 – 10 pF, Johanson
C4	27 pF, 100 mil Chip Capacitor, ATC
C5	22 pF, 100 mil Chip Capacitor, ATC
C9, C10, C11, C12	0.01 μF Blue Capacitor
C13	470 pF, 100 mil Chip Capacitor, ATC
C14	50 μF, 50 V Electrolytic Capacitor
L1, L2	8 Turns #20 AWG, 0.100 mils ID
B1, B2	6″ long, ID = 550 mils, 50 Ω Semi–Rigid Coax
R1	1.0 kΩ 1/2 Watt
R2	10 kΩ 1/2 Watt
R3, R4	45 Ω 1/2 Watt

Board Material – Teflon® Fiberglass
Dielectric Thickness = 0.30″, ε_r = 2.55 Copper Clad, 2.0 oz. Copper

Figure 1. MRF166W 500 MHz Test Circuit Schematic

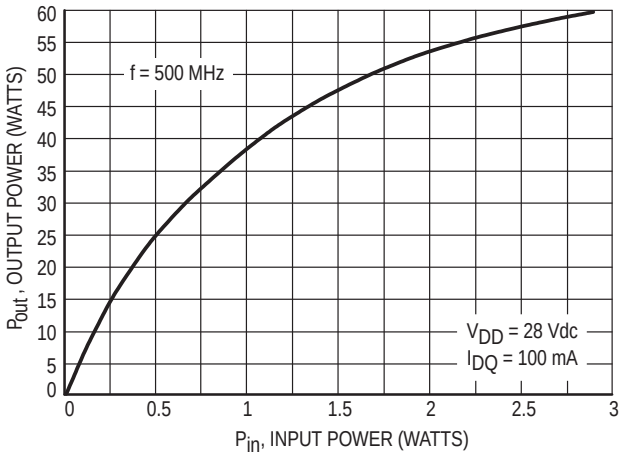


Figure 2. Output Power versus Input Power, 28 Vdc

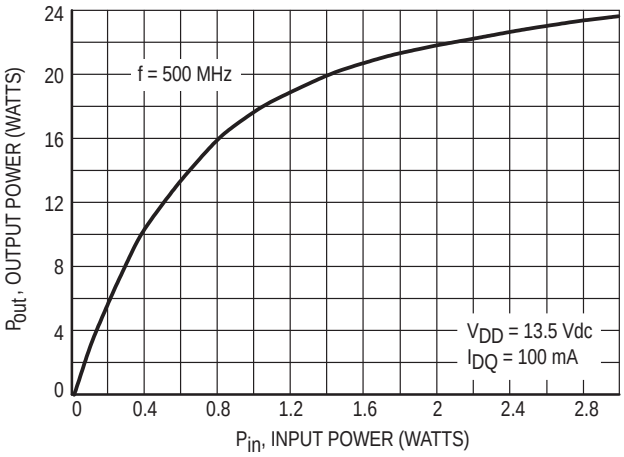


Figure 3. Output Power versus Input Power, 13.5 Vdc

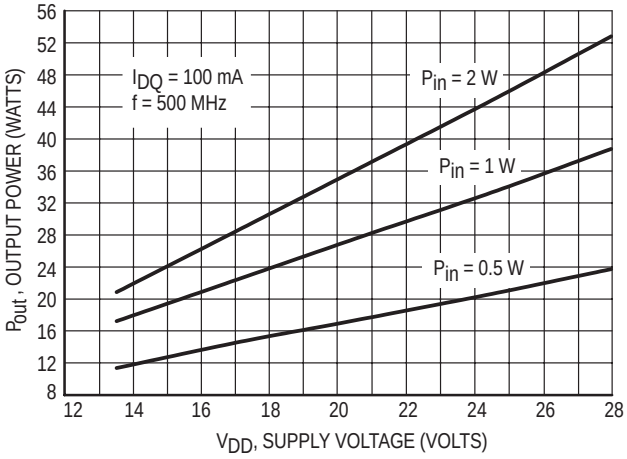


Figure 4. Output Power versus Supply Voltage

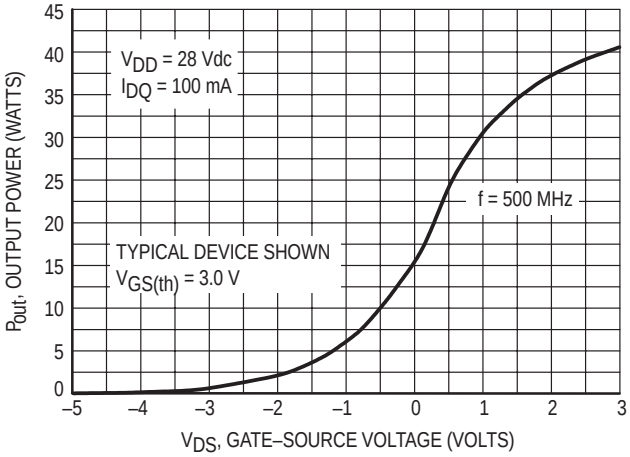


Figure 5. Output Power versus Gate Voltage

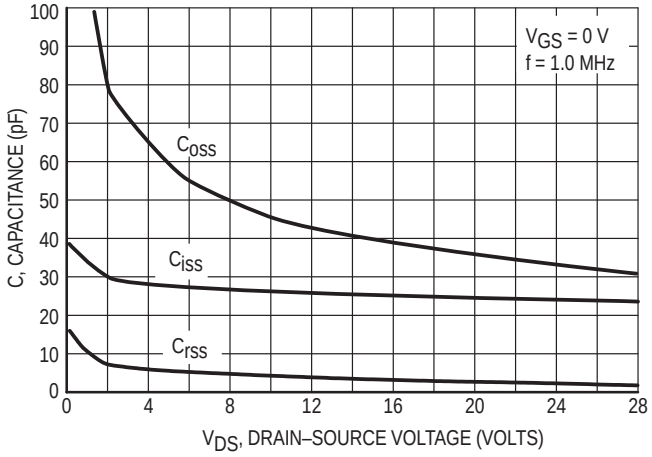
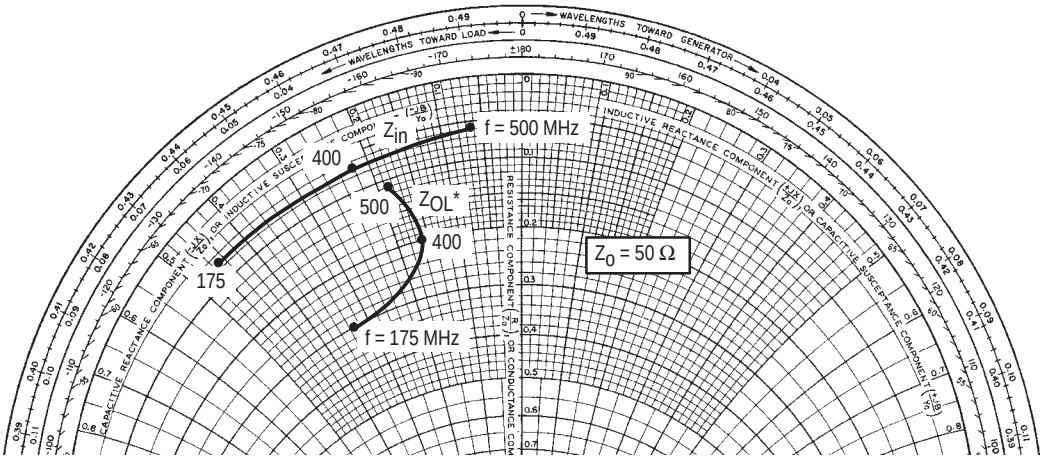


Figure 6. Capacitance versus Voltage



V_{DD} = 28 Vdc, I_{DQ} = 100 mA, P_{out} = 40 W

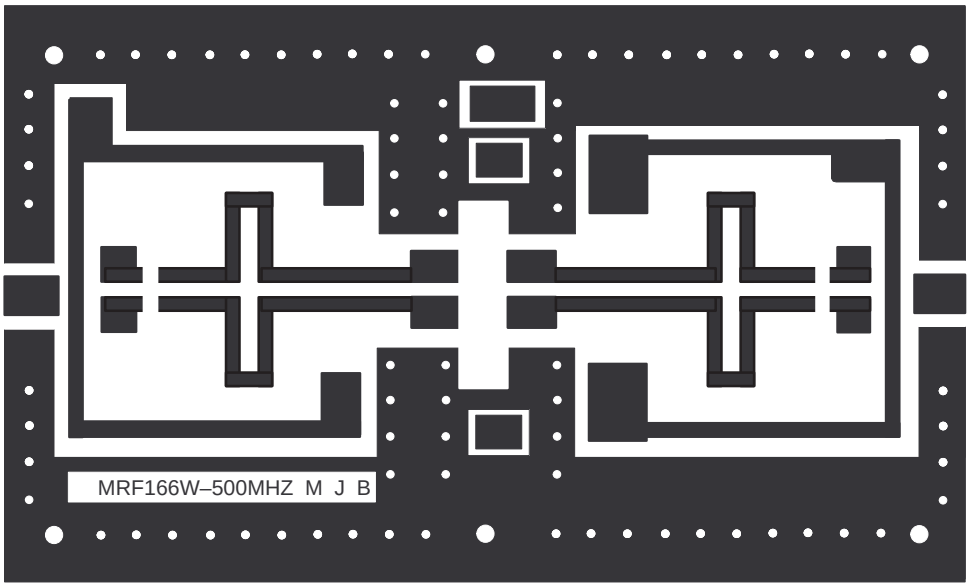
f MHz	Z_{in} Ohms	Z_{OL}* Ohms
175	3.7 – j 22.4	15.2 – j 16.6
400	3.6 – j 10.99	10.3 – j 7.99
500	2.88 – j 7.96	6.12 – j 9.43

Table 1. Input and Output Impedances

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

NOTE: Input and output impedance values given are measured from gate to gate and drain to drain respectively.

Figure 7. Series Equivalent Input/Output Impedance



(Scale 1:1)

NOTES: 1) 3 X 5 inch Glass Teflon® 32 Mil Board, Copper Both Sides
2) Small Holes are 40 Mils ID and Plated Through
3) Large Holes are 140 Mils ID and Plated Through

Figure 8. MRF166W Circuit Board Photomaster
(Reduced 18% in printed data book, DL110/D)

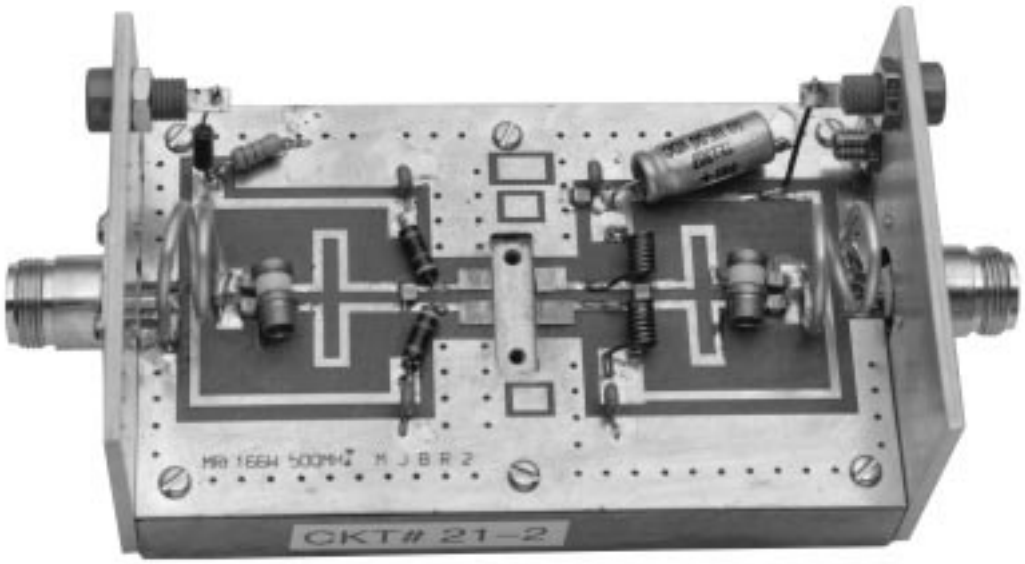


Figure 9. MRF166W Test Fixture

Table 1. Common Source S–Parameters (V_{DS} = 24 V, I_D = 230 mA)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.554	–85	20.30	128	0.044	28	0.628	–121
40	0.775	–113	20.00	113	0.040	26	0.632	–123
50	0.758	–124	17.50	107	0.041	20	0.652	–135
60	0.711	–132	14.60	100	0.050	20	0.570	–135
70	0.751	–139	12.70	100	0.042	11	0.666	–145
80	0.742	–143	11.30	95	0.043	9	0.666	–149
90	0.724	–146	10.00	92	0.042	8	0.657	–151
100	0.730	–149	8.97	90	0.042	6	0.663	–154
110	0.735	–151	8.29	87	0.043	3	0.683	–156
120	0.732	–153	7.53	84	0.042	2	0.666	–158
130	0.734	–155	7.01	83	0.042	1	0.688	–159
140	0.740	–156	6.57	81	0.043	0	0.701	–160
150	0.747	–157	6.01	78	0.042	–2	0.688	–162
160	0.748	–159	5.66	76	0.041	–4	0.715	–162
170	0.741	–160	5.22	76	0.040	–4	0.690	–161
180	0.746	–160	4.94	74	0.041	–4	0.719	–164
190	0.753	–161	4.67	73	0.041	–6	0.725	–165
200	0.756	–162	4.51	70	0.040	–7	0.729	–166
210	0.755	–162	4.15	69	0.039	–8	0.727	–165
220	0.759	–163	3.91	68	0.039	–8	0.724	–166
230	0.767	–163	3.75	65	0.039	–10	0.751	–169
240	0.769	–164	3.56	64	0.038	–12	0.733	–167
250	0.766	–164	3.41	63	0.037	–12	0.726	–167
260	0.767	–165	3.26	63	0.035	–10	0.725	–167
270	0.773	–165	3.07	61	0.035	–10	0.725	–167
280	0.777	–165	3.03	61	0.035	–11	0.753	–167
290	0.777	–166	2.89	58	0.034	–13	0.732	–169
300	0.782	–166	2.80	57	0.034	–11	0.744	–169
310	0.788	–166	2.66	57	0.034	–12	0.764	–169
320	0.794	–167	2.54	55	0.033	–12	0.760	–167
330	0.796	–167	2.47	54	0.032	–13	0.787	–169
340	0.795	–168	2.38	54	0.031	–13	0.753	–170
350	0.799	–168	2.27	52	0.030	–11	0.772	–168
360	0.804	–168	2.17	51	0.030	–11	0.782	–169
370	0.805	–168	2.15	50	0.030	–11	0.796	–169
380	0.807	–169	2.06	48	0.029	–12	0.782	–170
390	0.812	–169	2.00	48	0.028	–12	0.796	–170
400	0.818	–170	1.91	47	0.027	–10	0.784	–168
410	0.821	–170	1.86	46	0.029	–11	0.830	–170
420	0.821	–170	1.83	44	0.028	–11	0.823	–171
430	0.822	–171	1.74	44	0.026	–9	0.791	–170
440	0.826	–171	1.67	43	0.025	–7	0.788	–170

Table 1. Common Source S–Parameters (V_{DS} = 24 V, I_D = 230 mA) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
450	0.830	–171	1.68	42	0.025	–7	0.820	–170
460	0.831	–172	1.64	41	0.026	–10	0.843	–174
470	0.832	–172	1.54	41	0.025	–7	0.827	–173
480	0.835	–173	1.50	39	0.024	–3	0.836	–172
490	0.835	–173	1.43	38	0.024	1	0.835	–171
500	0.823	–174	1.43	37	0.025	3	0.849	–172
600	0.874	–176	1.12	29	0.003	–171	0.873	–176
700	0.910	–179	0.86	23	0.013	89	0.867	–177
800	0.932	179	0.74	18	0.035	61	0.904	178
900	0.966	176	0.63	12	0.029	68	0.897	179
1000	0.975	172	0.54	5	0.042	49	0.953	174

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 250 mA)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.601	–86	22.20	128	0.040	29	0.796	–119
40	0.783	–112	21.20	114	0.037	27	0.616	–122
50	0.764	–122	18.50	108	0.038	21	0.637	–133
60	0.727	–131	15.50	101	0.045	21	0.574	–135
70	0.759	–138	13.50	100	0.039	12	0.648	–143
80	0.751	–142	12.10	95	0.040	9	0.649	–148
90	0.732	–146	10.70	93	0.040	8	0.641	–150
100	0.737	–149	9.55	90	0.040	6	0.648	–153
110	0.741	–150	8.81	88	0.040	4	0.670	–155
120	0.738	–153	8.01	85	0.040	3	0.654	–156
130	0.740	–154	7.47	83	0.040	2	0.675	–157
140	0.747	–156	7.01	82	0.040	1	0.684	–158
150	0.754	–157	6.43	79	0.040	–2	0.669	–161
160	0.757	–159	6.07	77	0.039	–3	0.693	–161
170	0.749	–159	5.59	76	0.038	–3	0.670	–161
180	0.753	–160	5.28	75	0.039	–4	0.701	–163
190	0.759	–161	4.99	73	0.039	–5	0.712	–164
200	0.761	–161	4.81	70	0.038	–7	0.719	–165
210	0.759	–162	4.44	70	0.037	–6	0.713	–163
220	0.762	–163	4.18	69	0.037	–7	0.709	–164
230	0.771	–164	4.03	66	0.037	–9	0.733	–167
240	0.775	–164	3.83	65	0.036	–10	0.715	–165
250	0.774	–165	3.69	64	0.035	–10	0.713	–166
260	0.775	–165	3.52	63	0.034	–10	0.715	–168
270	0.780	–165	3.29	61	0.034	–10	0.712	–168
280	0.782	–165	3.24	61	0.034	–11	0.741	–168
290	0.781	–166	3.10	59	0.032	–12	0.722	–168
300	0.785	–166	3.01	58	0.033	–11	0.733	–168

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 250 mA) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
310	0.792	–167	2.87	57	0.032	–12	0.750	–167
320	0.798	–167	2.75	56	0.032	–12	0.739	–166
330	0.801	–168	2.68	53	0.031	–13	0.760	–170
340	0.800	–168	2.58	53	0.030	–14	0.727	–172
350	0.803	–169	2.44	52	0.029	–12	0.755	–170
360	0.807	–169	2.33	50	0.029	–12	0.772	–171
370	0.808	–169	2.30	50	0.029	–12	0.787	–169
380	0.809	–169	2.19	48	0.028	–13	0.768	–170
390	0.813	–170	2.14	49	0.027	–13	0.775	–169
400	0.820	–170	2.06	47	0.026	–11	0.765	–167
410	0.823	–170	2.02	45	0.027	–12	0.805	–170
420	0.823	–171	1.98	44	0.026	–13	0.794	–173
430	0.824	–171	1.89	44	0.025	–12	0.778	–174
440	0.828	–172	1.83	43	0.024	–11	0.785	–173
450	0.832	–172	1.81	41	0.024	–10	0.812	–172
460	0.833	–172	1.75	41	0.025	–13	0.838	–175
470	0.835	–172	1.65	41	0.023	–11	0.817	–173
480	0.840	–172	1.60	40	0.022	–10	0.818	–172
490	0.844	–173	1.55	38	0.022	–10	0.819	–172
500	0.845	–173	1.56	37	0.022	–10	0.833	–173
600	0.879	–176	1.21	29	0.002	138	0.870	–176
700	0.912	–179	0.92	23	0.017	77	0.862	–176
800	0.935	179	0.79	18	0.039	58	0.887	179
900	0.966	176	0.67	11	0.030	69	0.892	179
1000	0.974	172	0.57	5	0.043	49	0.945	175

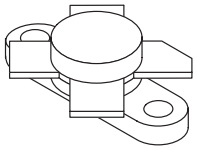
The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode MOSFET

MRF171A

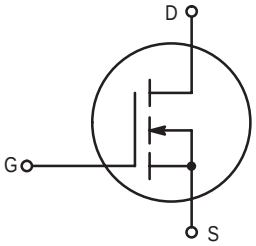
45 W, 150 MHz
MOSFET BROADBAND
RF POWER FET

Designed primarily for wideband large–signal output and driver stages from 30–200 MHz.

- Guaranteed Performance at 150 MHz, 28 Vdc
  Output Power = 45 Watts
  Power Gain = 17 dB (Min)
  Efficiency = 60% (Min)
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested for Load Mismatch At All Phase Angles with 30:1 VSWR
- Low Crss – 8 pF @ V_{DS} = 28 V
- Gold Top Metal



CASE 211–07, STYLE 2



Typical Data For Power Amplifier Applications in Industrial, Commercial and Amateur Radio Equipment

- Typical Performance at 30 MHz, 28 Vdc
  Output Power = 30 Watts (PEP)
  Power Gain = 20 dB (Typ)
  Efficiency = 50% (Typ)
  IMD(d3) (30 Watts PEP) –32 dB (Typ)
- S–Parameters Available for Download into Frequency Domain Simulators.
  See http://motorola.com/sps/rf/designtds/

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Gate Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Adc
Drain Current — Continuous	I_D	4.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.66	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

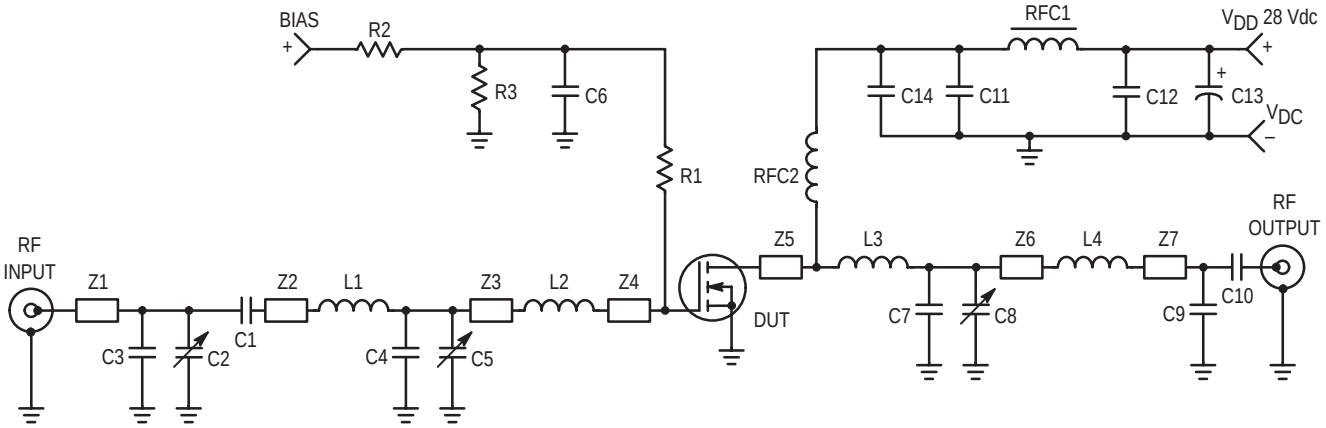
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (I_D = 50 mA, V_{GS} = 0)	$V_{(BR)DSS}$	65	80	—	Vdc
Zero Gate Voltage Drain Current (V_{GS} = 0, V_{DS} = 28 V)	I_{DSS}	—	—	1.0	mAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

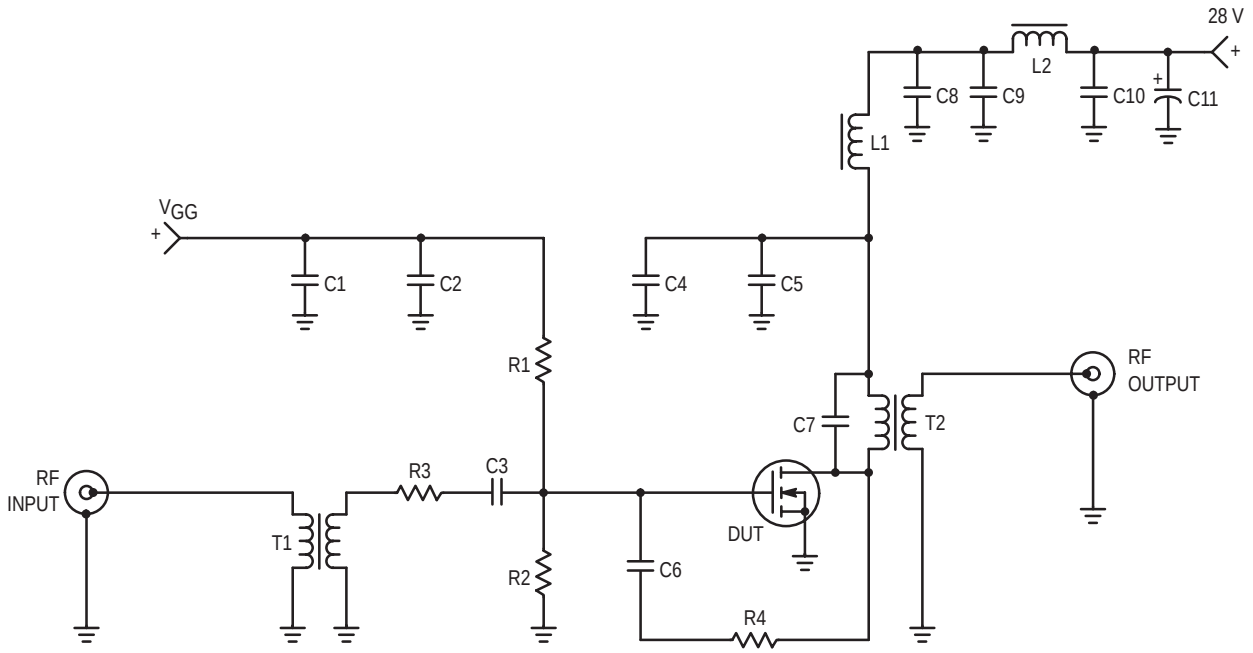
ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 50 mA)	$V_{GS(th)}$	1.5	2.5	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3 A)	$V_{DS(on)}$	—	1.0	—	V
Forward Transconductance (V_{DS} = 10 V, I_D = 2 A)	g_{fs}	1.4	1.8	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	60	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	70	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	8	—	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 45 W, f = 150 MHz, I_{DQ} = 25 mA)	G_{ps}	17	19.5	—	dB
Drain Efficiency (V_{DD} = 28 V, Pout = 45 W, f = 150 MHz, I_{DQ} = 25 mA)	η	60	70	—	%
Electrical Ruggedness (V_{DD} = 28 V, P_{out} = 45 W, f = 150 MHz, I_{DQ} = 25 mA, VSWR 30:1 at All Phase Angles)		No Degradation in Output Power			
TYPICAL FUNCTIONAL TESTS (SSB)					
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 30 W (PEP), I_{DQ} = 100 mA, f = 30; 30.001 MHz)	G_{ps}	—	20	—	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 30 W (PEP), I_{DQ} = 100 mA, f = 30; 30.001 MHz)	η	—	50	—	%
Intermodulation Distortion (V_{DD} = 28 V, P_{out} = 30 W (PEP), I_{DQ} = 100 mA, f = 30; 30.001 MHz)	IMD(d3)	—	–32	—	dB



C1, C10	1000 pF, Chip Capacitor	R2	1 kΩ, 1/2 W Chip Resistor
C2, C5, C8	2–20 pF, Trimmer Capacitors, Johanson	R3	10 kΩ, 1/2 W Chip Resistor
C3	43 pF, 100 mil Chip Capacitor, ATC	Z1	0.160″ x 0.400″ Microstrip
C4	120 pF, 100 mil Chip Capacitor, ATC	Z2	0.160″ x 0.600″ Microstrip
C6, C14	0.1 μF, Capacitors	Z3	0.160″ x 0.600″ Microstrip
C7	50 pF, 100 mil Chip Capacitor, ATC	Z4	0.160″ x 0.900″ Microstrip
C9	12 pF, 100 mil Chip Capacitor, ATC	Z5	0.160″ x 0.800″ Microstrip
C11, C12	680 pF, Feedthru Capacitors	Z6	0.160″ x 0.800″ Microstrip
C13	50 μF, 50 V, Electrolytic Capacitor	Z7	0.160″ x 0.400″ Microstrip
L1	2 Turns, 0.297″ ID, 18 AWG	RFC1	Ferroxcube VK200–19/4B
L2	1–1/2 Turns, 0.265″ ID, 18 AWG	RFC2	10 Turns, 0.250″ ID, 20 AWG, Enamel
L3	1–1/4 Turns, 0.234″ ID, 18 AWG	Board	0.062″, G10 1 oz. Copper Clad
L4	1–1/2 Turns, 0.250″ ID, 18 AWG		Both Sides, ε_r = 2.56
R1	68 Ω, 1/2 W Chip Resistor		

Figure 1. MRF171A 150 MHz Test Circuit



C1, C3, C5, C6	0.1 μF, Chip Capacitors	L1, L2	VK200 20/4B Ferrite Choke
C2, C4	1000 pF, Chip Capacitors	R1, R2	200 Ω, 1/2 W Carbon
C7	68 pF, Dipped Mica	R3	3 Ω, 1/2 W Carbon
C8	0.1 μF, Ceramic Cap or Equivalent	R4	270 Ω, 2 W Carbon
C9, C10	680 pF, Feedthru Capacitors	T1	4:1 Impedance Broadband Transformer
C11	250 μF, 50 V, Electrolytic Capacitor	T2	1:4 Impedance Broadband Transformer

Figure 2. MRF171A 30 MHz Test Circuit

TYPICAL CHARACTERISTICS

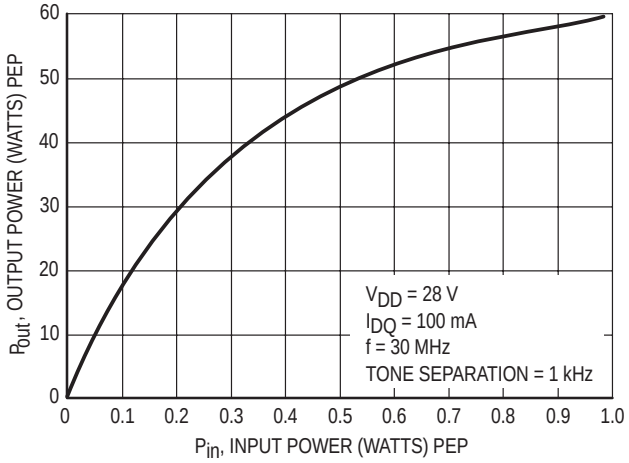


Figure 3. Output Power versus Input Power

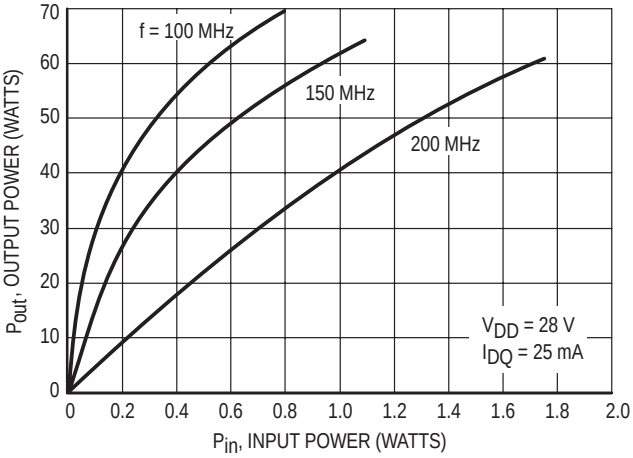


Figure 4. Output Power versus Input Power

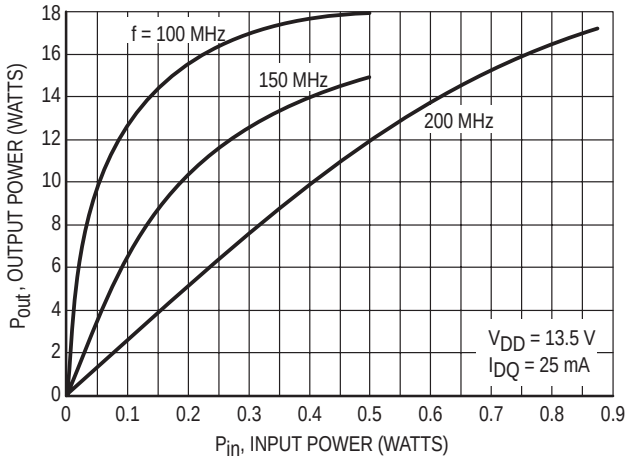


Figure 5. Output Power versus Input Power

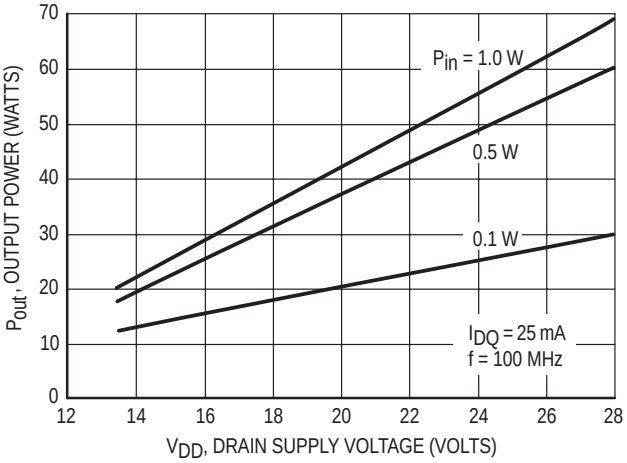


Figure 6. Output Power versus Supply Voltage

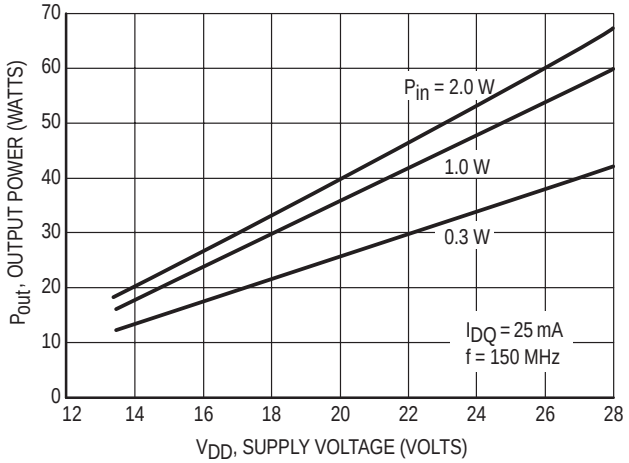


Figure 7. Output Power versus Supply Voltage

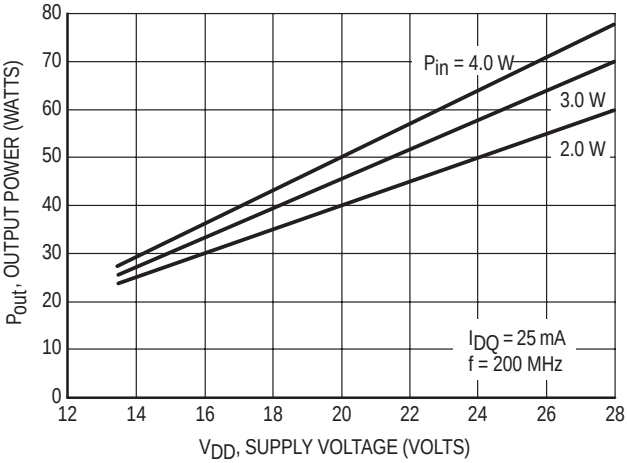


Figure 8. Output Power versus Supply Voltage

TYPICAL CHARACTERISTICS

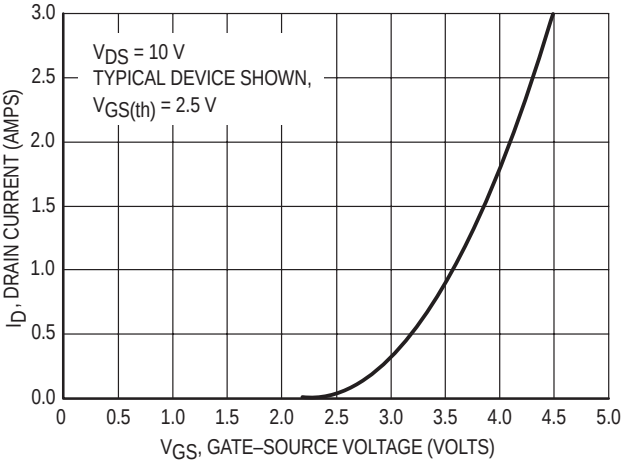


Figure 9. Drain Current versus Gate Voltage (Transfer Characteristics)

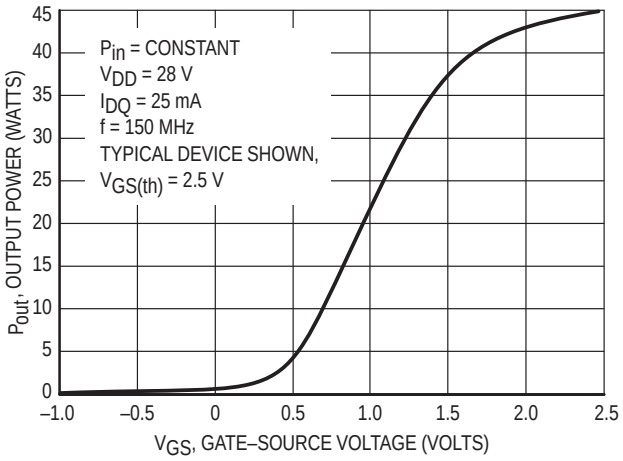


Figure 10. Output Power versus Gate Voltage

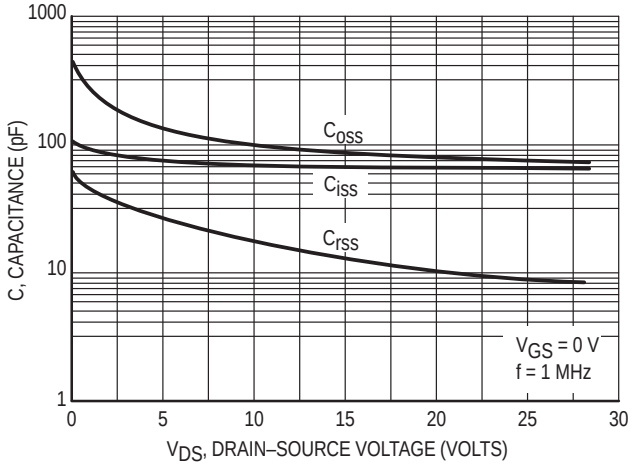
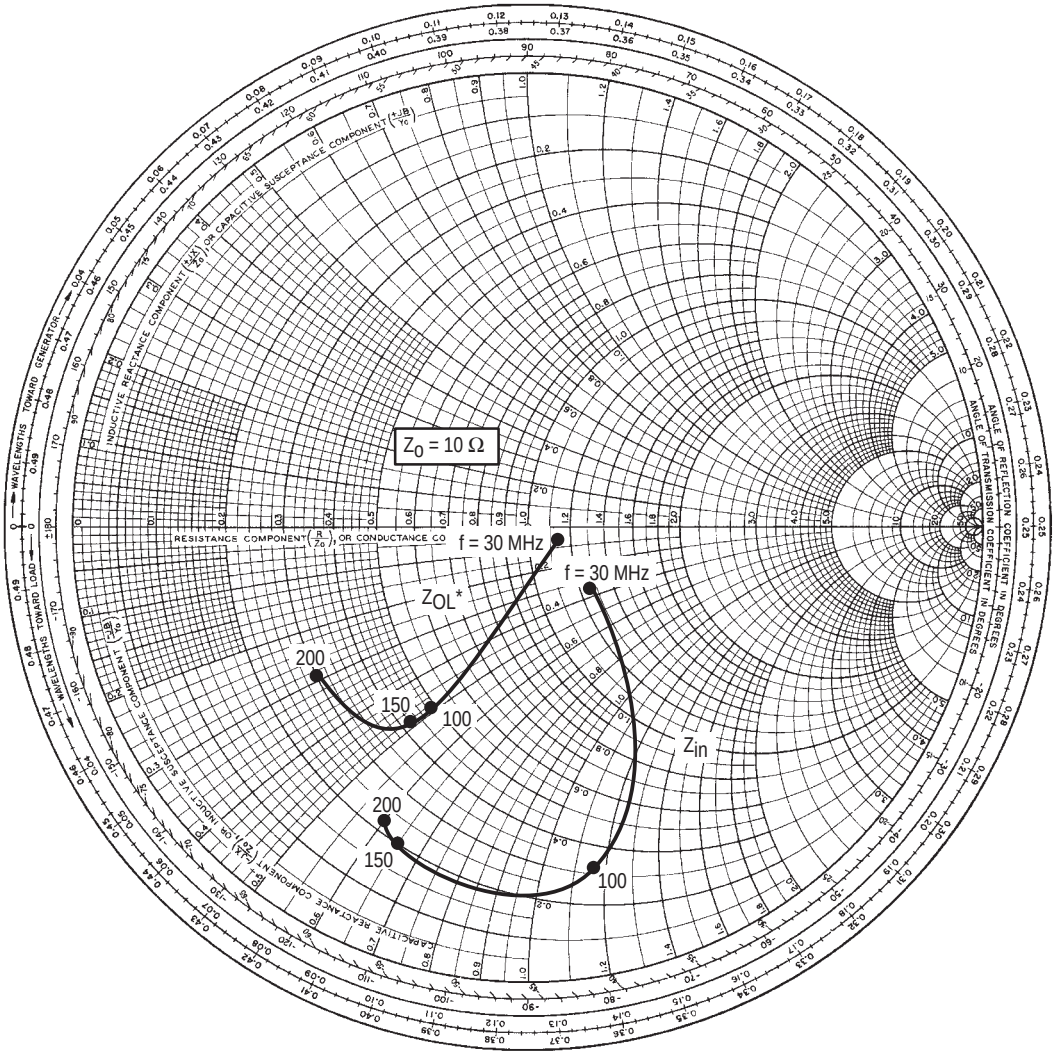


Figure 11. Capacitance versus Drain–Source Voltage



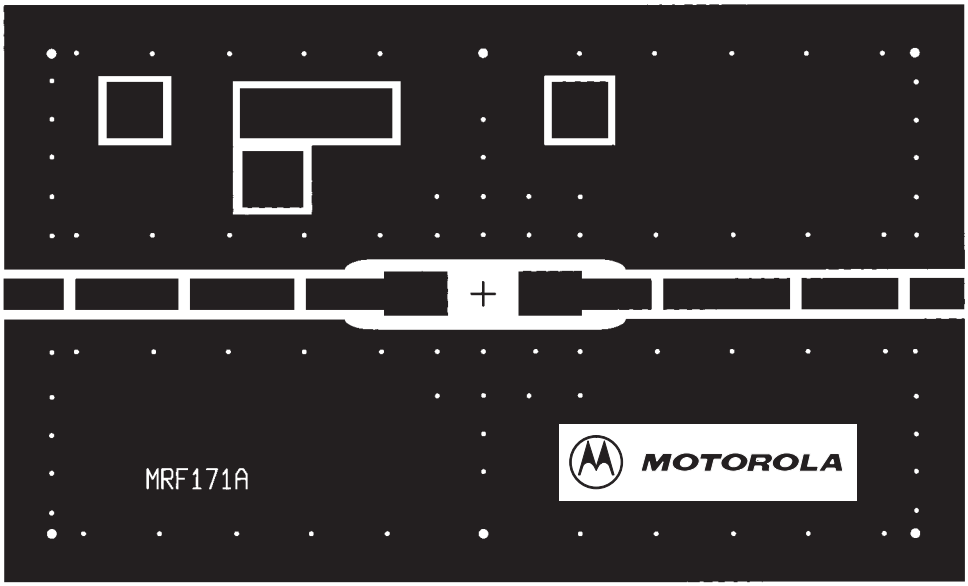
V_{DD} = 28 V, I_{DQ} = 25 mA, P_{out} = 45 W

f MHz	Z_{in}(1) Ω	Z_{OL}(2) Ω
30	12.8 – j3.6	11.5 – j0.99
100	3.1 – j11.6	4.9 – j4.9
150	2.0 – j6.5	4.2 – j4.9
200	2.2 – j6.0	3.0 – j2.9

(1) 68 Ω shunt resistor gate–to–ground.

(2) Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

Figure 12. Large–Signal Series Equivalent Input/Output Impedance



(Scale 1:1)

Figure 13. MRF171A Circuit Board Photo Master
(Reduced 18% in printed data book, DL110/D)

Table 1. Common Source S–Parameters (V_{DS} = 12.5 V, I_D = 0.5 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.801	–162	11.90	96	0.026	13	0.811	–166
40	0.809	–166	9.12	91	0.028	11	0.812	–171
50	0.810	–169	7.29	88	0.027	11	0.831	–172
60	0.808	–170	6.22	85	0.028	9	0.824	–174
70	0.814	–172	5.30	82	0.028	9	0.831	–176
80	0.811	–173	4.56	81	0.027	10	0.837	–175
90	0.811	–174	4.04	80	0.027	13	0.829	–174
100	0.814	–174	3.66	77	0.027	12	0.846	–176
110	0.812	–175	3.37	75	0.027	11	0.842	–177
120	0.816	–175	3.00	74	0.027	13	0.850	–176
130	0.816	–176	2.75	73	0.027	14	0.849	–175
140	0.817	–176	2.57	72	0.027	17	0.851	–176
150	0.821	–176	2.37	69	0.027	17	0.863	–177
160	0.820	–176	2.27	67	0.027	17	0.853	–177
170	0.821	–177	2.08	66	0.026	19	0.838	–177
180	0.824	–177	1.93	65	0.027	19	0.861	–177
190	0.825	–177	1.89	64	0.027	21	0.873	–177
200	0.830	–177	1.74	62	0.027	23	0.873	–178
210	0.831	–177	1.67	60	0.027	25	0.874	–177
220	0.831	–178	1.62	59	0.026	28	0.870	–178
230	0.836	–178	1.48	57	0.027	27	0.909	–179
240	0.836	–178	1.43	56	0.027	26	0.865	–180
250	0.839	–178	1.37	57	0.028	30	0.873	–178
260	0.844	–178	1.30	54	0.028	34	0.882	–179
270	0.842	–178	1.28	52	0.028	36	0.887	–180
280	0.845	–179	1.21	52	0.027	37	0.881	–180
290	0.849	–179	1.14	50	0.027	36	0.869	179
300	0.849	–179	1.12	50	0.029	39	0.852	–180
310	0.855	–179	1.06	49	0.029	42	0.891	–179
320	0.856	–179	1.03	46	0.030	43	0.889	180
330	0.856	–180	0.96	45	0.031	47	0.868	180
340	0.858	–180	0.96	46	0.030	47	0.888	179
350	0.860	180	0.93	44	0.031	49	0.875	–180
360	0.862	180	0.91	44	0.033	48	0.901	179
370	0.866	180	0.86	43	0.034	50	0.913	178
380	0.867	179	0.84	41	0.036	52	0.897	178
390	0.869	179	0.82	42	0.035	54	0.893	178
400	0.870	179	0.78	40	0.035	57	0.880	180
410	0.872	179	0.77	39	0.037	55	0.923	178
420	0.876	178	0.73	37	0.039	54	0.915	176
430	0.877	178	0.69	38	0.040	56	0.903	177
440	0.879	178	0.68	39	0.041	58	0.921	178

Table 1. Common Source S–Parameters (V_{DS} = 12.5 V, I_D = 0.5 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
450	0.882	177	0.68	36	0.040	61	0.926	178
460	0.884	177	0.65	36	0.041	59	0.937	175
470	0.886	177	0.62	35	0.041	60	0.896	176
480	0.885	176	0.62	33	0.044	61	0.907	176
490	0.886	176	0.61	32	0.046	63	0.907	176
500	0.887	176	0.59	31	0.047	65	0.916	175

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 0.5 A)

f MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.783	–152	17.10	100	0.025	17	0.730	–158
40	0.793	–158	13.20	94	0.027	13	0.730	–164
50	0.793	–162	10.50	90	0.027	12	0.754	–167
60	0.791	–165	9.00	87	0.027	11	0.746	–169
70	0.798	–167	7.68	83	0.026	10	0.760	–171
80	0.795	–169	6.63	82	0.026	10	0.770	–170
90	0.795	–170	5.85	80	0.026	12	0.760	–170
100	0.799	–170	5.30	77	0.026	10	0.779	–172
110	0.798	–171	4.86	75	0.026	11	0.775	–174
120	0.802	–172	4.35	74	0.025	13	0.785	–172
130	0.801	–172	3.97	72	0.025	14	0.788	–171
140	0.803	–173	3.70	71	0.025	15	0.791	–172
150	0.809	–173	3.42	68	0.025	14	0.808	–173
160	0.808	–173	3.27	66	0.025	15	0.796	–172
170	0.809	–174	2.99	65	0.024	18	0.783	–174
180	0.814	–174	2.77	63	0.025	19	0.809	–173
190	0.815	–175	2.71	62	0.024	21	0.820	–174
200	0.822	–175	2.49	60	0.024	22	0.826	–175
210	0.824	–175	2.37	57	0.024	24	0.836	–175
220	0.825	–175	2.23	57	0.024	26	0.807	–175
230	0.831	–176	2.08	56	0.024	29	0.839	–175
240	0.830	–176	2.00	54	0.024	29	0.818	–176
250	0.832	–176	1.92	55	0.024	33	0.828	–174
260	0.838	–176	1.81	53	0.024	35	0.829	–175
270	0.837	–176	1.79	50	0.025	37	0.834	–175
280	0.840	–177	1.69	50	0.025	39	0.832	–176
290	0.844	–177	1.60	48	0.025	39	0.836	–177
300	0.844	–177	1.55	48	0.025	44	0.814	–175
310	0.849	–178	1.48	47	0.026	46	0.848	–175
320	0.852	–178	1.43	44	0.027	45	0.855	–177
330	0.852	–178	1.35	43	0.028	48	0.833	–177
340	0.855	–178	1.32	44	0.028	49	0.861	–177
350	0.856	–178	1.29	41	0.029	53	0.842	–176

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 0.5 A) (continued)

f MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
360	0.859	–179	1.25	42	0.030	54	0.872	–178
370	0.863	–179	1.18	39	0.030	55	0.886	–178
380	0.864	–179	1.15	38	0.031	55	0.864	–178
390	0.867	–179	1.12	39	0.032	57	0.862	–179
400	0.869	–180	1.07	37	0.032	60	0.853	–177
410	0.872	–180	1.05	35	0.035	60	0.898	–179
420	0.876	180	1.00	34	0.036	60	0.889	180
430	0.877	179	0.95	35	0.037	62	0.884	–179
440	0.879	179	0.93	34	0.038	64	0.902	–179
450	0.882	179	0.91	32	0.039	65	0.901	–180
460	0.884	178	0.88	32	0.041	64	0.922	179
470	0.885	178	0.84	32	0.040	66	0.877	179
480	0.885	178	0.83	30	0.042	66	0.892	179
490	0.886	177	0.81	29	0.044	68	0.891	179
500	0.887	177	0.80	28	0.045	68	0.900	178

The RF MOSFET Line

RF Power Field Effect Transistor

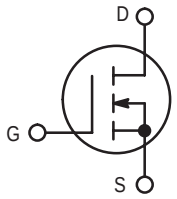
N–Channel Enhancement Mode MOSFET

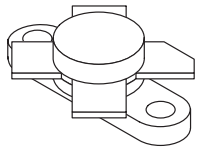
MRF173

80 W, 28 V, 175 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET

Designed for broadband commercial and military applications up to 200 MHz frequency range. The high–power, high–gain and broadband performance of this device make possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 150 MHz, 28 V:
  Output Power = 80 W
  Gain = 11 dB (13 dB Typ)
  Efficiency = 55% Min. (60% Typ)
- Low Thermal Resistance
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability
- Low Noise Figure — 1.5 dB Typ at 2.0 A, 150 MHz
- Excellent Thermal Stability; Suited for Class A Operation
- S–Parameters Available for Download into Frequency Domain Simulators. See http://motorola.com/sps/rf/designtds/





CASE 211–11, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage	V_{DGO}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	9.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	220 1.26	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Temperature Range	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.8	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

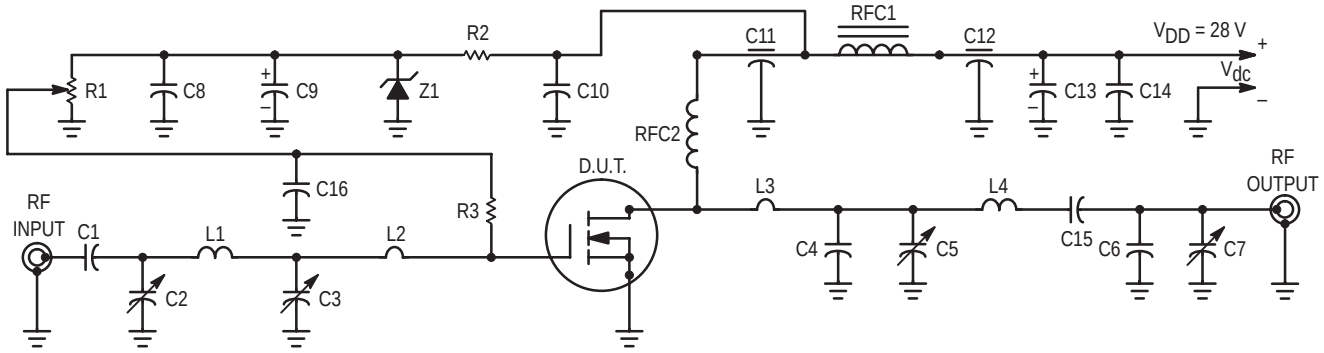
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{DS} = 0 V, V_{GS} = 0 V) I_D = 50 mA	$V_{(BR)DSS}$	65	—	—	V
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	2.0	mA
Gate–Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0 V)	I_{GSS}	—	—	1.0	μA
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 50 mA)	$V_{GS(th)}$	1.0	3.0	6.0	V
Drain–Source On–Voltage ($V_{DS(on)}$, V_{GS} = 10 V, I_D = 3.0 A)	$V_{DS(on)}$	—	—	1.4	V
Forward Transconductance (V_{DS} = 10 V, I_D = 2.0 A)	g_{fs}	1.8	2.2	—	mhos

(continued)

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	110	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{oss}	—	105	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{rss}	—	10	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DD} = 28 V, f = 150 MHz, I_{DQ} = 50 mA)	NF	—	1.5	—	dB
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	G_{ps}	11	13	—	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	η	55	60	—	%
Electrical Ruggedness (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA) Load VSWR 30:1 at all phase angles	ψ	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	Z_{in}	—	2.99–j4.5	—	Ohms
Series Equivalent Output Impedance (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	Z_{out}	—	2.68–j1.3	—	Ohms



C1, C15 — 470 pF Unelco
C2, C3, C5 — 9–180 pF, Arco 463
C4, C6 — 15 pF, Unelco
C7 — 5–80 pF, Arco 462
C8, C10, C14, C16 — 0.1 μF
C9, C13 — 50 μF, 50 Vdc
C11, C12 — 680 pF, Feed Through
L1 — #16 AWG, 1–1/4 Turns, 0.3″ ID
L2 — #16 AWG Hairpin 1″ long

L3 — #14 AWG Hairpin 0.8″ long
L4 — #14 AWG Hairpin 1.1″ long
RFC1 — Ferroxcube VK200–19/4B
RFC2 — 18 Turns #18 AWG Enameled, 0.3″ ID
R1 — 10 kΩ, 10 Turns Bourns
R2 — 1.8 kΩ, 1/4 W
R3 — 10 kΩ, 1/2 W
Z1 — 1N5925A Motorola Zener

Figure 1. 150 MHz Test Circuit

TYPICAL CHARACTERISTICS

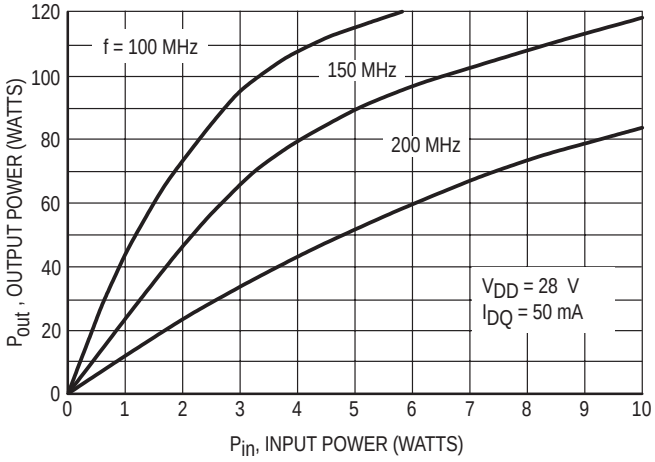


Figure 2. Output Power versus Input Power

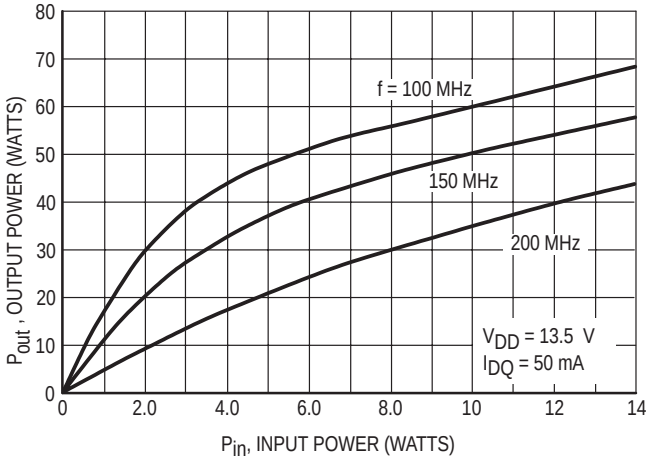


Figure 3. Output Power versus Input Power

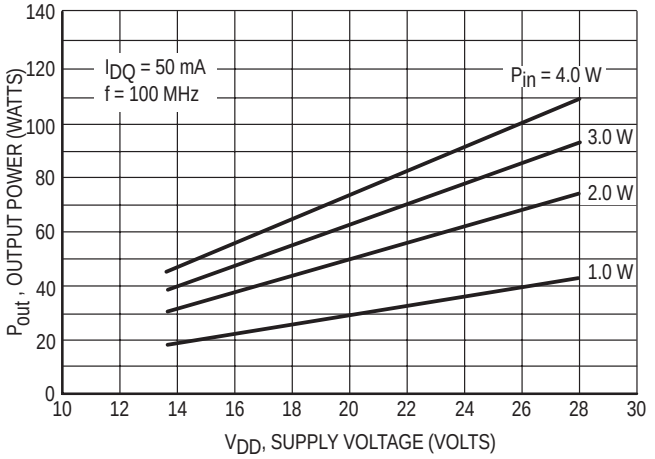


Figure 4. Output Power versus Supply Voltage

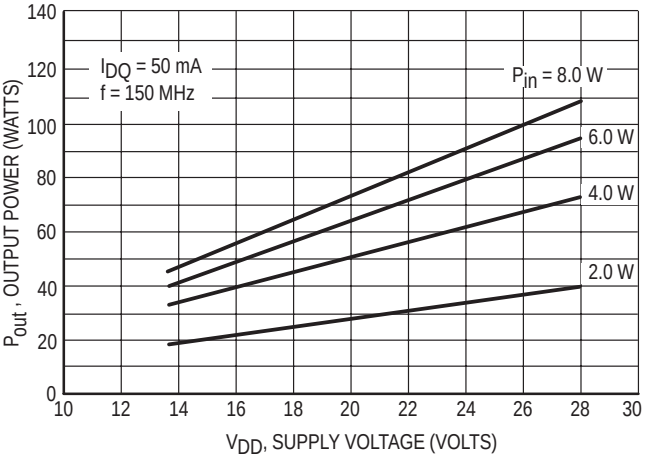


Figure 5. Output Power versus Supply Voltage

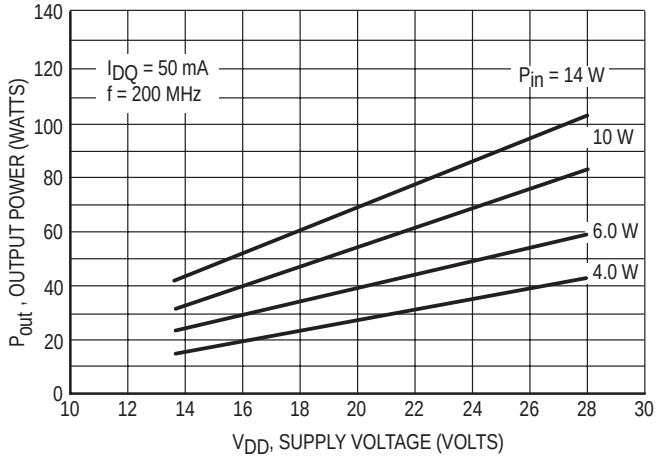


Figure 6. Output Power versus Supply Voltage

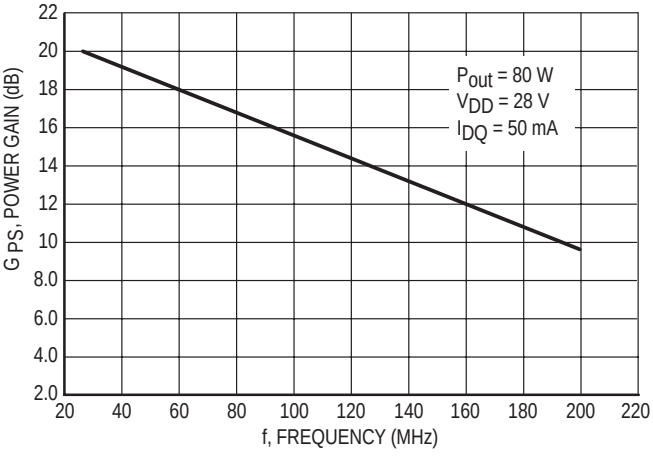


Figure 7. Power Gain versus Frequency

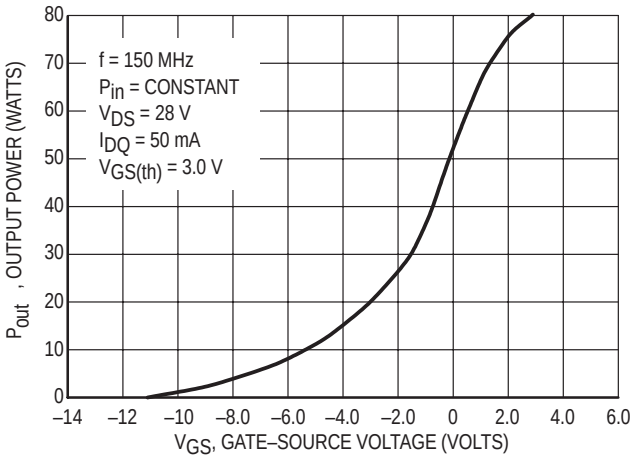


Figure 8. Output Power versus Gate Voltage

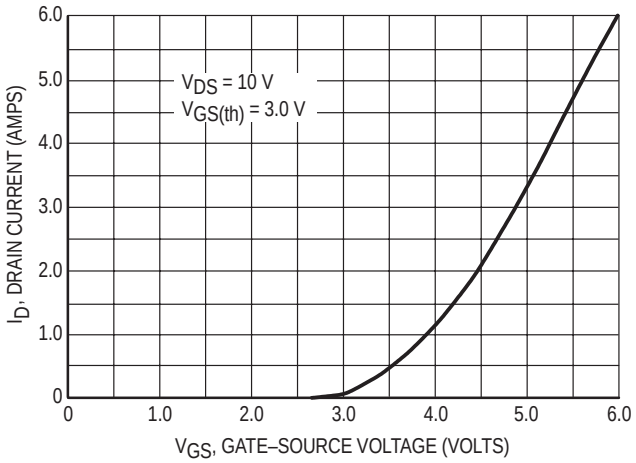


Figure 9. Drain Current versus Gate Voltage

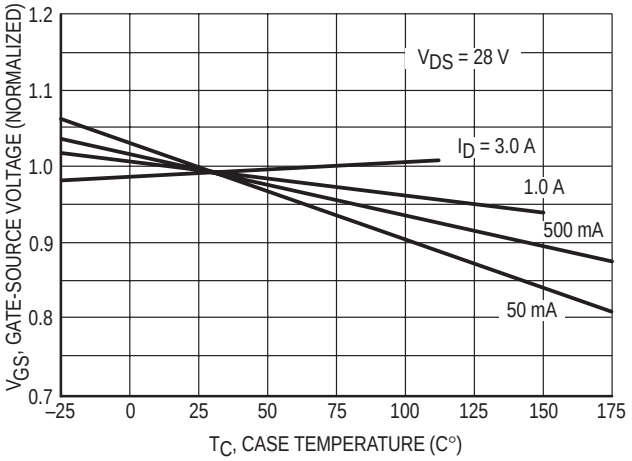


Figure 10. Gate–Source Voltage versus Case Temperature

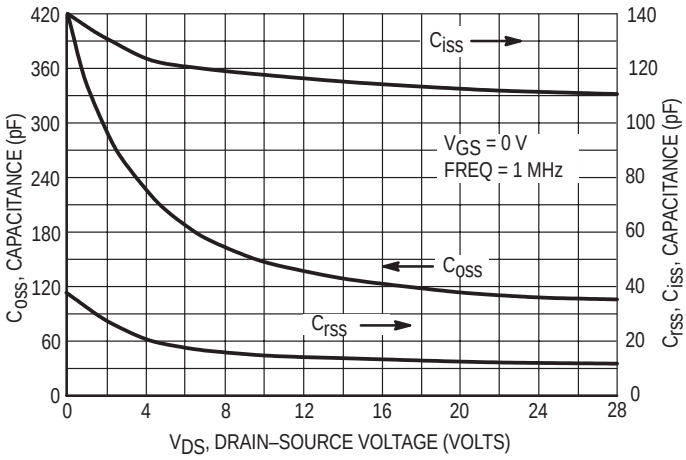


Figure 11. Capacitance versus Drain Voltage

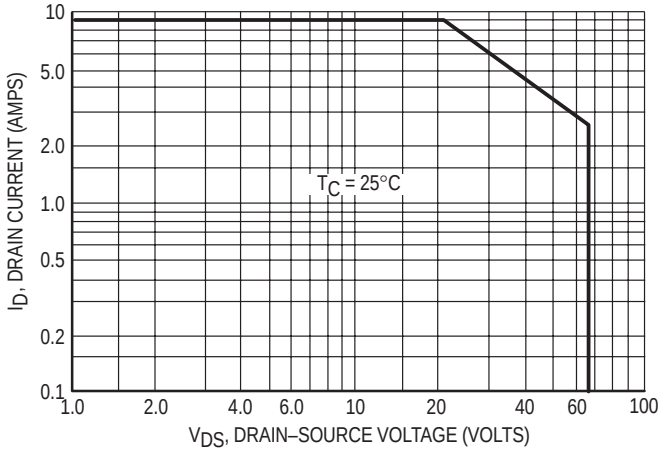


Figure 12. DC Safe Operating Area

Table 1. Common Source S–Parameters (V_{DS} = 12.5 V, I_D = 4 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.879	–170	8.09	92	0.014	23	0.839	–174
40	0.883	–173	6.19	87	0.016	24	0.839	–179
50	0.885	–174	4.94	84	0.016	28	0.853	–178
60	0.885	–175	4.21	81	0.017	30	0.845	180
70	0.888	–176	3.57	77	0.017	34	0.849	179
80	0.888	–177	3.06	77	0.017	37	0.852	–179
90	0.888	–178	2.71	76	0.018	42	0.842	–179
100	0.890	–178	2.45	72	0.019	43	0.858	180
110	0.888	–179	2.28	70	0.020	46	0.859	179
120	0.892	–179	2.02	69	0.021	50	0.872	–180
130	0.893	–179	1.84	67	0.022	52	0.870	–179
140	0.894	–180	1.73	66	0.023	55	0.880	–180
150	0.896	–180	1.58	64	0.024	55	0.887	180
160	0.896	180	1.51	61	0.026	56	0.863	180
170	0.898	179	1.38	60	0.026	60	0.850	179
180	0.899	179	1.28	58	0.028	60	0.871	179
190	0.899	179	1.25	57	0.030	62	0.890	178
200	0.902	179	1.15	55	0.030	63	0.884	178
210	0.902	179	1.12	53	0.032	63	0.899	178
220	0.904	178	1.08	51	0.034	65	0.893	178
230	0.907	178	0.97	49	0.037	65	0.941	176
240	0.907	178	0.95	48	0.037	65	0.884	176
250	0.909	178	0.90	49	0.039	67	0.896	177
260	0.911	177	0.85	48	0.039	68	0.888	176
270	0.909	177	0.83	46	0.042	68	0.895	176
280	0.913	177	0.78	45	0.044	69	0.893	175
290	0.914	177	0.74	42	0.044	69	0.882	174
300	0.915	176	0.74	42	0.047	72	0.877	175
310	0.917	176	0.70	41	0.048	73	0.909	176
320	0.916	176	0.69	39	0.052	71	0.912	175
330	0.917	176	0.65	37	0.055	71	0.885	173
340	0.919	176	0.65	38	0.055	70	0.898	173
350	0.919	175	0.62	36	0.057	72	0.887	174
360	0.920	175	0.60	37	0.059	72	0.918	172
370	0.921	175	0.57	35	0.061	71	0.929	172
380	0.923	175	0.56	34	0.063	71	0.900	172
390	0.925	175	0.54	36	0.065	71	0.907	171
400	0.926	174	0.51	34	0.067	75	0.902	173
410	0.927	174	0.51	33	0.070	73	0.942	170
420	0.929	174	0.49	31	0.071	71	0.926	169
430	0.929	173	0.46	32	0.072	72	0.901	170
440	0.930	173	0.45	32	0.076	73	0.904	170

Table 1. Common Source S–Parameters (V_{DS} = 12.5 V, I_D = 4 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
450	0.932	173	0.45	29	0.079	75	0.924	170
460	0.932	172	0.44	30	0.082	71	0.938	167
470	0.933	172	0.42	30	0.081	73	0.908	168
480	0.931	172	0.42	29	0.086	72	0.933	168
490	0.931	171	0.41	28	0.089	72	0.926	167
500	0.931	171	0.41	27	0.092	71	0.936	167

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 4 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.840	–163	11.48	92	0.016	20	0.718	–169
40	0.849	–167	8.80	86	0.017	22	0.713	–174
50	0.853	–170	6.99	82	0.017	24	0.748	–174
60	0.854	–171	5.92	79	0.017	23	0.746	–175
70	0.859	–172	5.00	74	0.018	25	0.746	–175
80	0.859	–174	4.29	73	0.018	30	0.741	–174
90	0.861	–174	3.77	71	0.019	38	0.735	–174
100	0.866	–175	3.39	67	0.018	40	0.768	–176
110	0.865	–175	3.12	64	0.018	41	0.782	–177
120	0.871	–176	2.75	63	0.019	42	0.794	–175
130	0.875	–176	2.49	60	0.021	45	0.783	–172
140	0.877	–177	2.31	59	0.023	51	0.776	–175
150	0.883	–177	2.10	56	0.023	55	0.806	–176
160	0.884	–177	1.99	53	0.023	58	0.807	–176
170	0.886	–178	1.82	51	0.023	61	0.806	–176
180	0.890	–178	1.66	49	0.025	59	0.820	–175
190	0.891	–179	1.62	48	0.027	60	0.815	–176
200	0.896	–179	1.47	46	0.030	63	0.819	–177
210	0.898	–179	1.41	43	0.031	67	0.842	–178
220	0.901	–179	1.36	41	0.032	70	0.855	–178
230	0.905	–180	1.22	38	0.033	70	0.906	–178
240	0.906	–180	1.19	38	0.034	67	0.845	–178
250	0.909	180	1.11	39	0.037	68	0.831	–178
260	0.913	180	1.03	37	0.038	70	0.837	–180
270	0.912	179	0.10	35	0.041	72	0.859	179
280	0.916	179	0.93	34	0.042	74	0.876	178
290	0.918	179	0.88	31	0.041	73	0.865	179
300	0.919	178	0.87	31	0.044	74	0.837	–180
310	0.922	178	0.83	31	0.046	74	0.863	180
320	0.922	178	0.80	27	0.051	73	0.879	177
330	0.924	177	0.75	26	0.054	74	0.878	176
340	0.926	177	0.74	27	0.053	74	0.897	177
350	0.926	177	0.71	24	0.054	77	0.879	179

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 4 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
360	0.927	177	0.68	26	0.056	75	0.888	177
370	0.929	177	0.64	24	0.058	73	0.893	175
380	0.931	176	0.62	23	0.062	72	0.885	174
390	0.934	176	0.60	25	0.064	74	0.903	174
400	0.934	176	0.57	22	0.065	78	0.898	177
410	0.936	175	0.56	21	0.068	77	0.931	175
420	0.938	175	0.53	20	0.070	74	0.906	173
430	0.938	174	0.51	21	0.072	73	0.885	173
440	0.939	174	0.49	21	0.075	75	0.895	172
450	0.941	174	0.48	19	0.080	78	0.923	172
460	0.941	173	0.47	19	0.082	75	0.940	171
470	0.942	173	0.45	18	0.080	75	0.904	172
480	0.940	173	0.44	18	0.083	74	0.910	171
490	0.940	172	0.43	18	0.088	72	0.906	169
500	0.940	172	0.42	17	0.092	72	0.927	168

DESIGN CONSIDERATIONS

The MRF173 is a RF MOSFET power N–channel enhancement mode field–effect transistor (FET) designed for VHF power amplifier applications. Motorola's RF MOSFETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V–groove power FETs.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF173 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF173 was characterized at I_{DQ} = 50 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF173 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (see Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF173. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOSFETs helps ease the task of broadband network design. Both small–signal scattering parameters and large–signal impedances are provided. While the s–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

The RF MOSFET Line

RF Power Field Effect Transistor

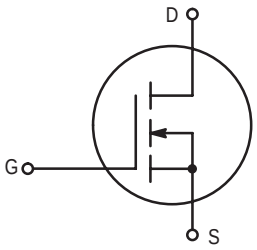
N–Channel Enhancement–Mode

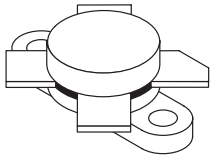
MRF174

. . . designed primarily for wideband large–signal output and driver stages up to 200 MHz frequency range.

- Guaranteed Performance at 150 MHz, 28 Vdc
  Output Power = 125 Watts
  Minimum Gain = 9.0 dB
  Efficiency = 50% (Min)
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 3.0 dB Typ at 2.0 A, 150 MHz

125 W, to 200 MHz
N–CHANNEL MOS
BROADBAND RF POWER
FET





CASE 211–11, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	13	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

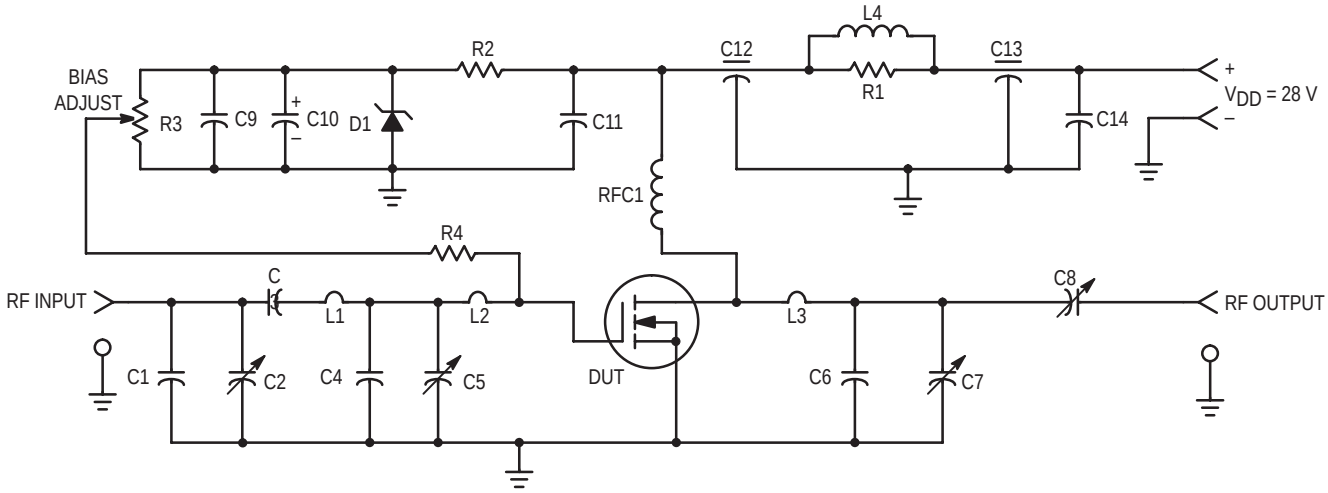
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	10	mAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3.0 A)	g_{fs}	1.75	2.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	175	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	190	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	40	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DD} = 28 Vdc, I_D = 2.0 A, f = 150 MHz)	NF	—	3.0	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA)	G_{ps}	9.0	11.8	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA)	η	50	60	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			



C1 — 15 pF Unelco
C2 — Arco 462, 5.0–80 pF
C3 — 100 pF Unelco
C4 — 25 pF Unelco
C6 — 40 pF Unelco
C7 — Arco 461, 2.7–30 pF
C5, C8 — Arco 463, 9.0–180 pF
C9, C11, C14 — 0.1 μF Erie Redcap
C10 — 50 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — #16 AWG, 1–1/4 Turns, 0.213″ ID
L2 — #16 AWG, Hairpin 0.25″ 0.062″
L3 — #14 AWG, Hairpin 0.47″ 0.2″
L4 — 10 Turns #16 AWG Enameled Wire on R1
RFC1 — 18 Turns #16 AWG Enameled Wire, 0.3″ ID
R1 — 10 Ω, 2.0 W
R2 — 1.8 kΩ, 1/2 W
R3 — 10 kΩ, 10 Turn Bourns
R4 — 10 kΩ, 1/4 W

Figure 1. 150 MHz Test Circuit

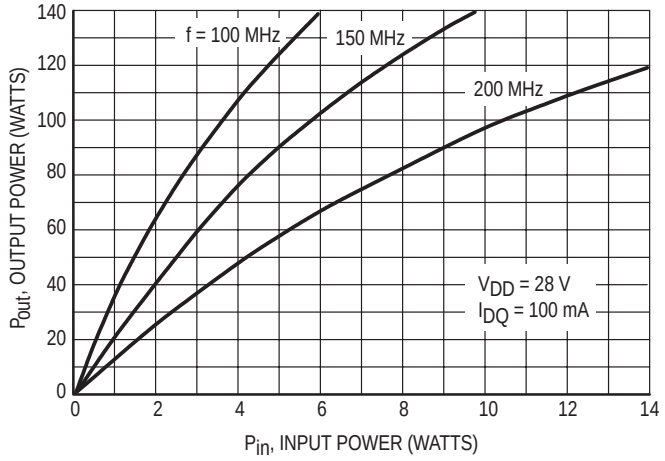


Figure 2. Output Power versus Input Power

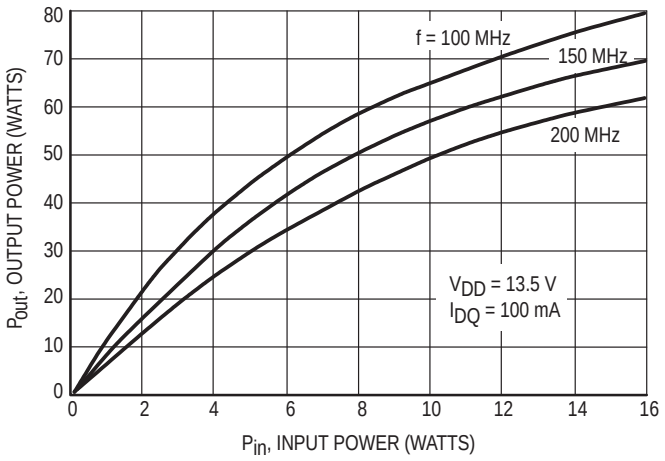


Figure 3. Output Power versus Input Power

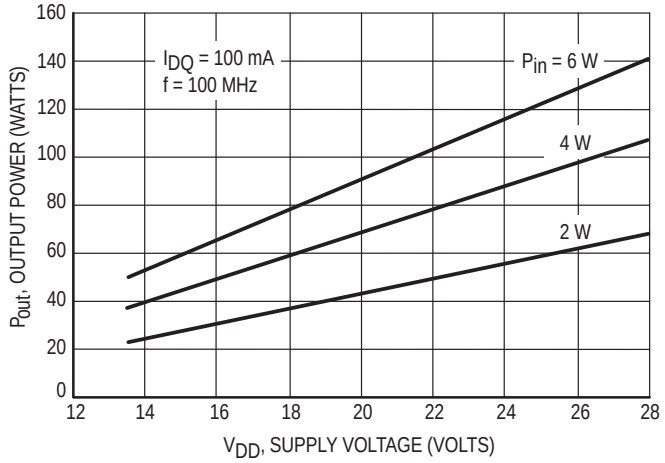


Figure 4. Output Power versus Supply Voltage

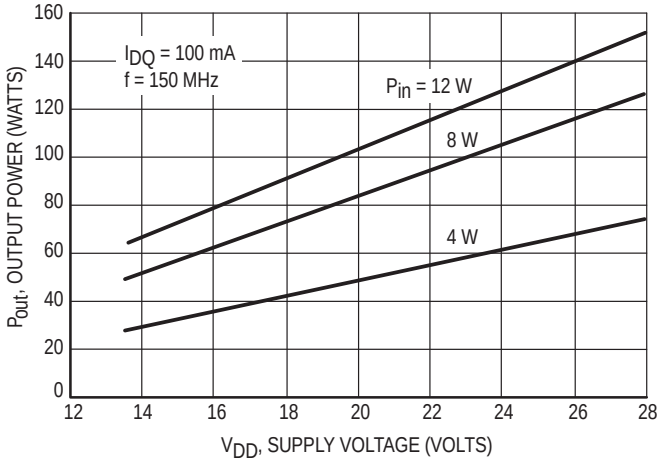


Figure 5. Output Power versus Supply Voltage

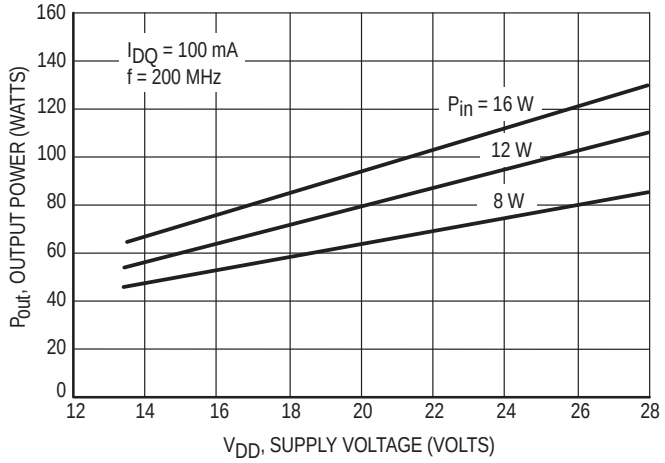


Figure 6. Output Power versus Supply Voltage

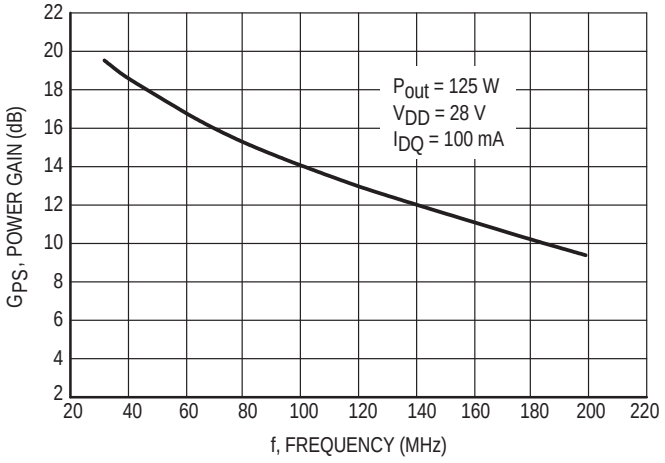


Figure 7. Power Gain versus Frequency

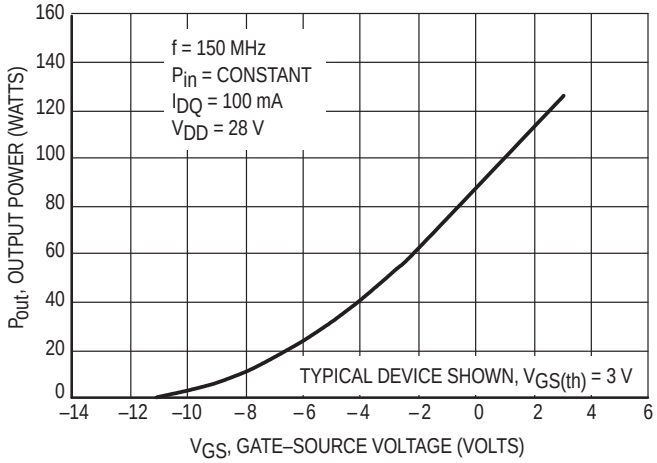


Figure 8. Output Power versus Gate Voltage

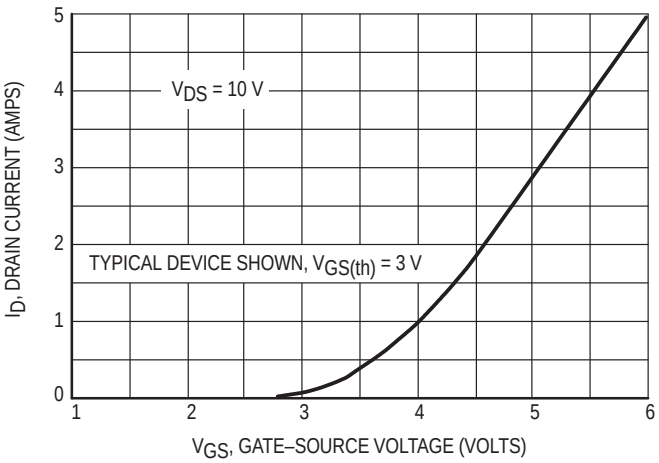


Figure 9. Drain Current versus Gate Voltage (Transfer Characteristics)

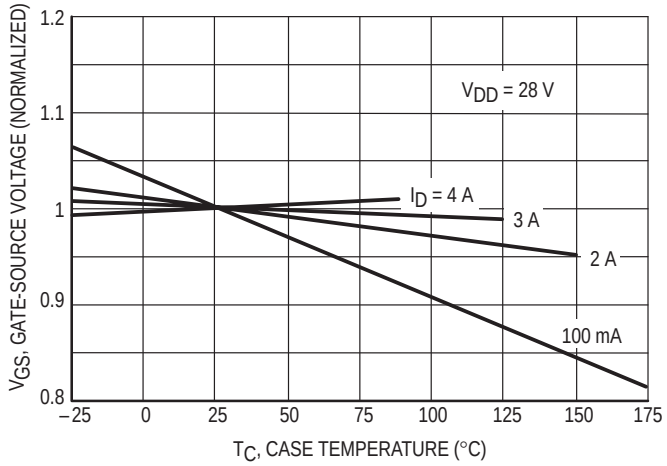


Figure 10. Gate–Source Voltage versus Case Temperature

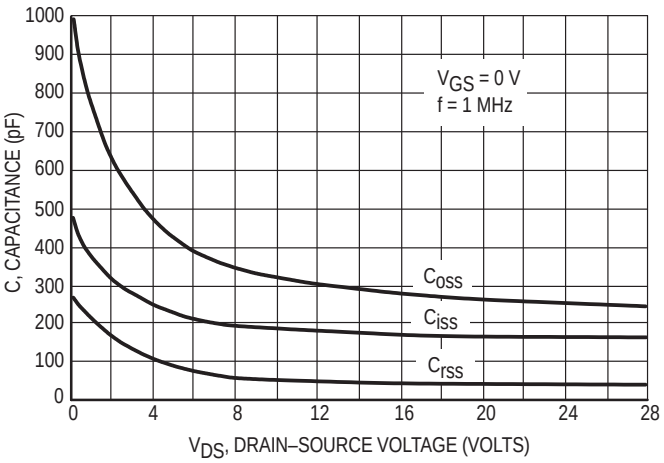


Figure 11. Capacitance versus Drain Voltage

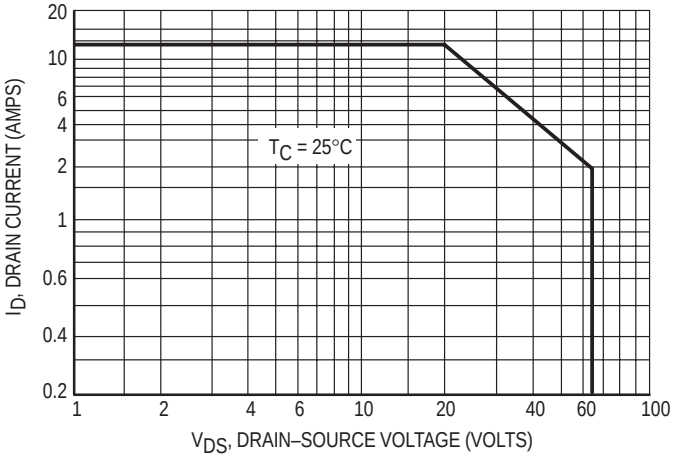


Figure 12. DC Safe Operating Area

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
2.0	0.932	−133	74.0	112	0.011	23	0.835	−151
5.0	0.923	−160	31.6	98	0.011	12	0.886	−168
10	0.921	−170	16.0	93	0.011	10	0.896	−174
20	0.921	−175	8.00	88	0.011	12	0.899	−177
30	0.921	−177	5.32	86	0.011	16	0.900	−178
40	0.921	−177	3.98	83	0.012	21	0.901	−178
50	0.922	−178	3.17	81	0.012	26	0.902	−178
60	0.923	−178	2.63	79	0.012	30	0.903	−178
70	0.924	−178	2.24	77	0.013	34	0.904	−178
80	0.925	−178	1.95	75	0.013	39	0.906	−178
90	0.927	−178	1.72	73	0.014	43	0.907	−178
100	0.930	−178	1.50	71	0.016	45	0.910	−178
110	0.930	−178	1.31	70	0.018	46	0.912	−178
120	0.931	−178	1.19	68	0.019	47	0.914	−178
130	0.942	−178	1.10	67	0.019	49	0.919	−178
140	0.936	−178	1.01	66	0.021	50	0.921	−178
150	0.938	−178	0.936	65	0.021	53	0.922	−178
160	0.938	−178	0.879	64	0.022	53	0.923	−178
170	0.940	−178	0.830	63	0.023	54	0.923	−177
180	0.942	−178	0.780	61	0.024	56	0.924	−177
190	0.942	−178	0.737	60	0.026	59	0.928	−177
200	0.952	−178	0.705	59	0.027	58	0.929	−177
210	0.950	−178	0.668	57	0.029	61	0.934	−177
220	0.942	−178	0.626	56	0.030	61	0.933	−177
230	0.943	−178	0.592	56	0.032	62	0.939	−177
240	0.946	−177	0.566	55	0.033	64	0.941	−177
250	0.952	−177	0.545	54	0.035	64	0.943	−177
260	0.958	−177	0.523	53	0.036	65	0.946	−177
270	0.956	−177	0.500	52	0.038	67	0.943	−177
280	0.960	−177	0.481	52	0.039	68	0.946	−177
290	0.956	−178	0.460	51	0.042	68	0.944	−177
300	0.955	−178	0.443	50	0.043	68	0.947	−177

Table 1. Common Source Scattering Parameters
V_{DS} = 28 V, I_D = 3.0 A

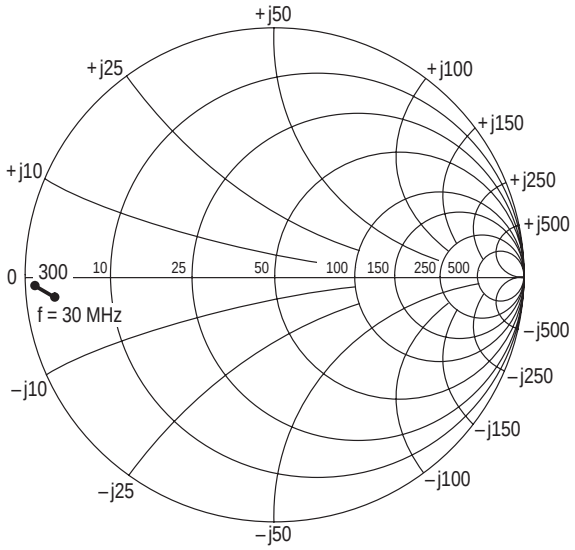


Figure 13. S_{11}, Input Reflection Coefficient versus Frequency
V_{DS} = 28 V, I_D = 3.0 A

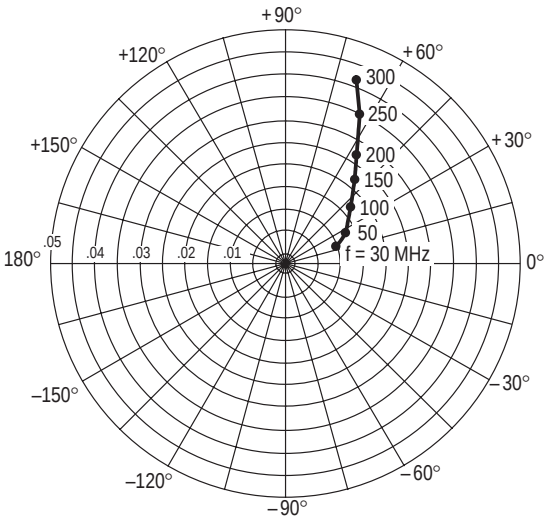


Figure 14. S_{12}, Reverse Transmission Coefficient versus Frequency
V_{DS} = 28 V, I_D = 3.0 A

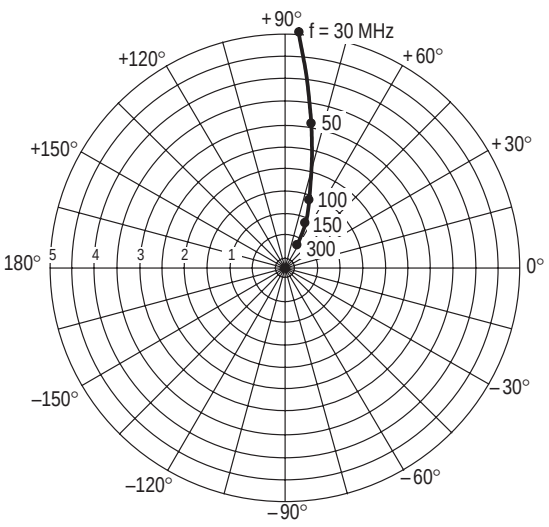


Figure 15. S_{21}, Forward Transmission Coefficient versus Frequency
V_{DS} = 28 V, I_D = 3.0 A

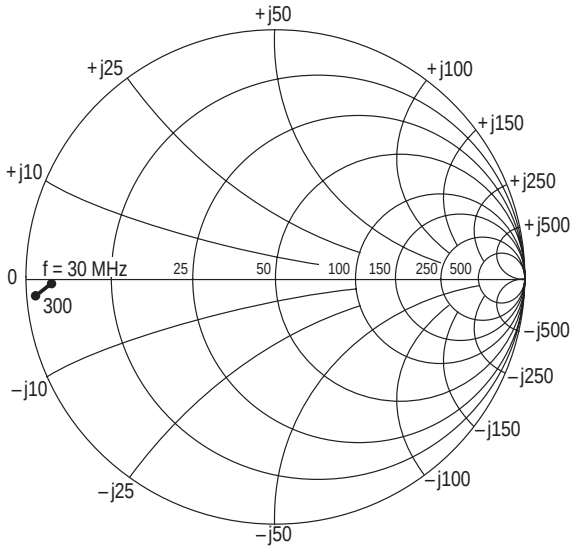


Figure 16. S_{22}, Output Reflection Coefficient versus Frequency
V_{DS} = 28 V, I_D = 3.0 A

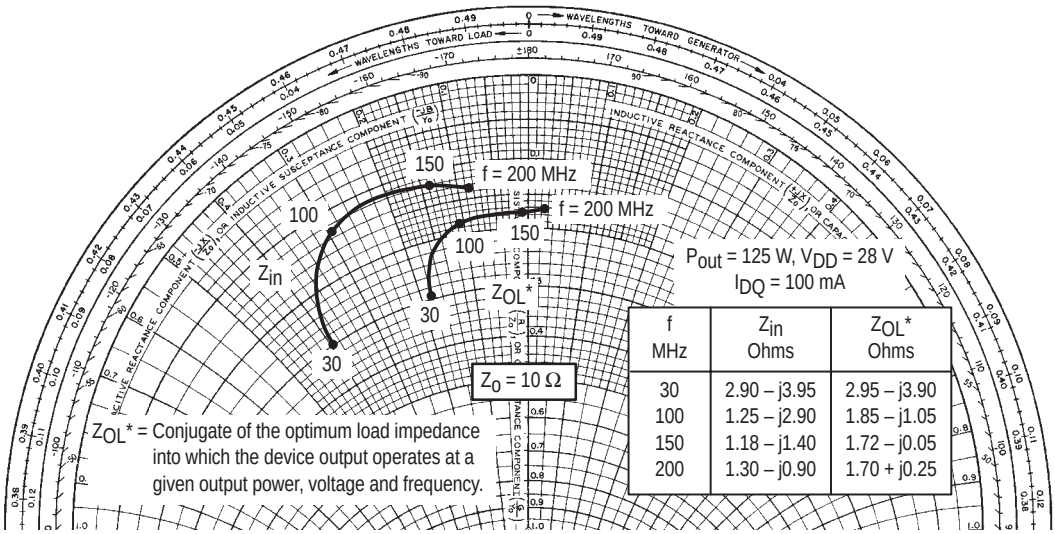


Figure 17. Series Equivalent Input/Output Impedance, Z_{in}, Z_{OL}*

DESIGN CONSIDERATIONS

The MRF174 is a RF power N–Channel enhancement mode field–effect transistor (FET) designed especially for UHF power amplifier and oscillator applications. Motorola RF MOSFETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V–groove vertical power FETs.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF174 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF174 was characterized at I_{DQ} = 100 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF174 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar UHF transistors are suitable for MRF174. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOSFETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

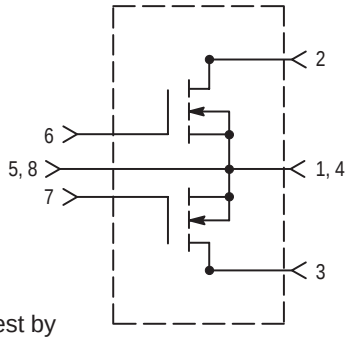
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement Mode MOSFET

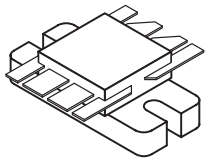
MRF177

100 W, 28 V, 400 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET

Designed for broadband commercial and military applications up to 400 MHz frequency range. Primarily used as a driver or output amplifier in push–pull configurations. Can be used in manual gain control, ALC and modulation circuits.

- Typical Performance at 400 MHz, 28 V:
  Output Power — 100 W
  Gain — 12 dB
  Efficiency — 60%
- Low Thermal Resistance
- Low C_{rss} — 10 pF Typ @ V_{DS} = 28 Volts
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability
- Excellent Thermal Stability; Suited for Class A Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.
- S–Parameters Available for Download into Frequency Domain Simulators. See http://motorola.com/sps/rf/designtds/





CASE 744A–01, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Temperature Range	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	0.65	°C/W

(1) Total device dissipation rating applies only when the device is operated as an RF push–pull amplifier.

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic (1)	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	2.0	mAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 50 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3.0 A)	$V_{DS(on)}$	—	—	1.4	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.0 A)	g_{fs}	1.8	2.2	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	100	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	105	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	10	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 8) (2)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 200 mA)	G_{PS}	10	12	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 200 mA)	η	55	60	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 200 mA, Load VSWR = 30:1, All Phase Angles At Frequency of Test)	ψ	No Degradation in Output Power Before & After Test			

(1) Note each transistor chip measured separately
(2) Both transistor chips operating in push–pull amplifier

TYPICAL CHARACTERISTICS

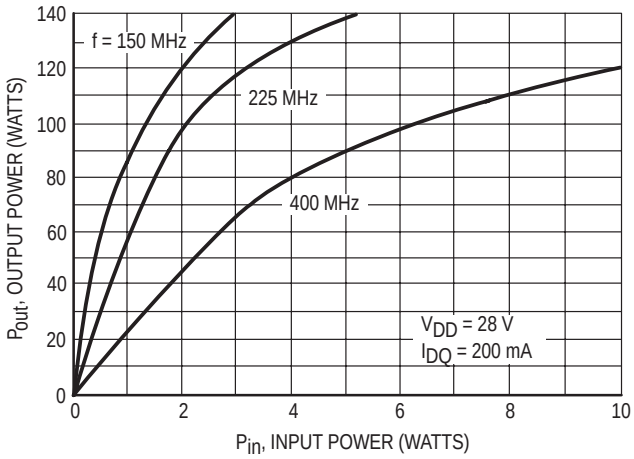


Figure 1. Output Power versus Input Power

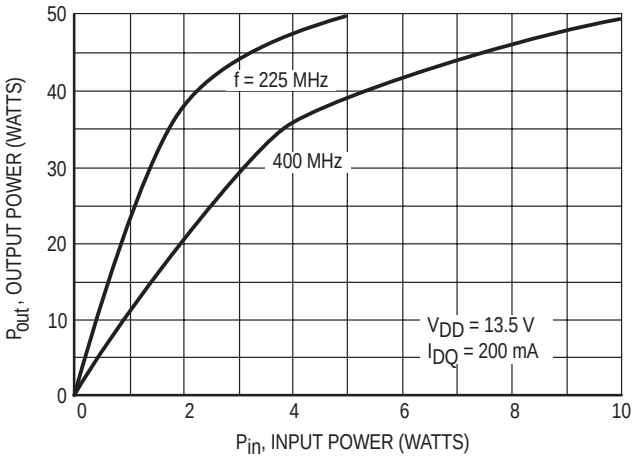


Figure 2. Output Power versus Input Power

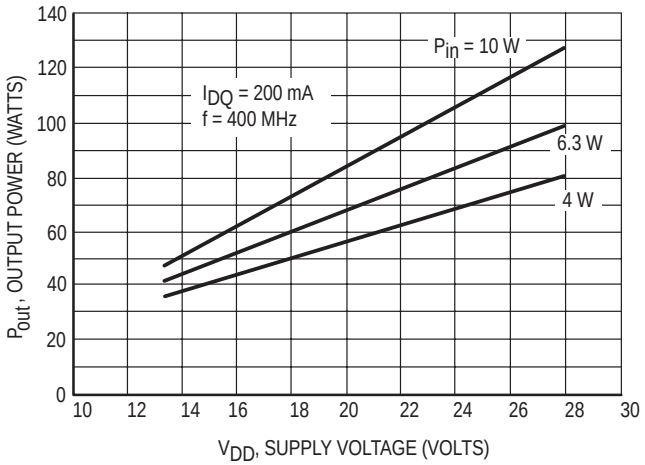


Figure 3. Output Power versus Supply Voltage

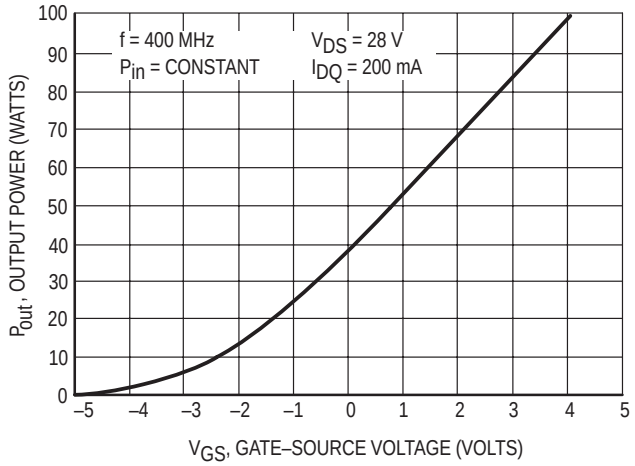


Figure 4. Output Power versus Gate Voltage

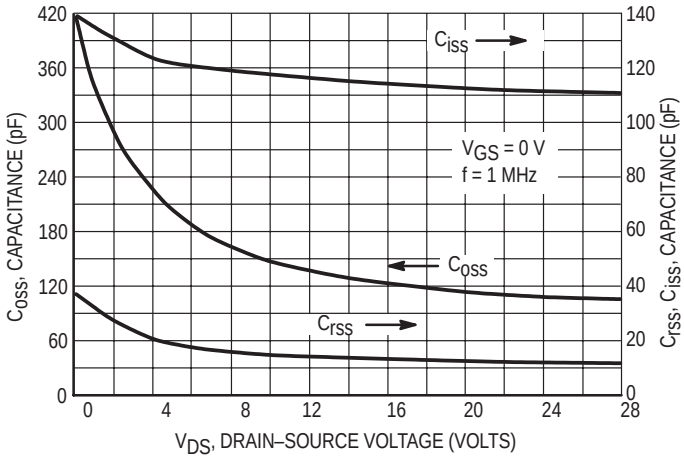


Figure 5. Capacitance versus Drain Voltage

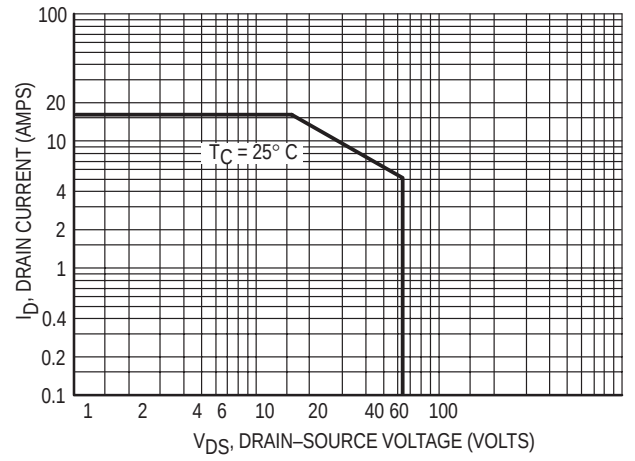
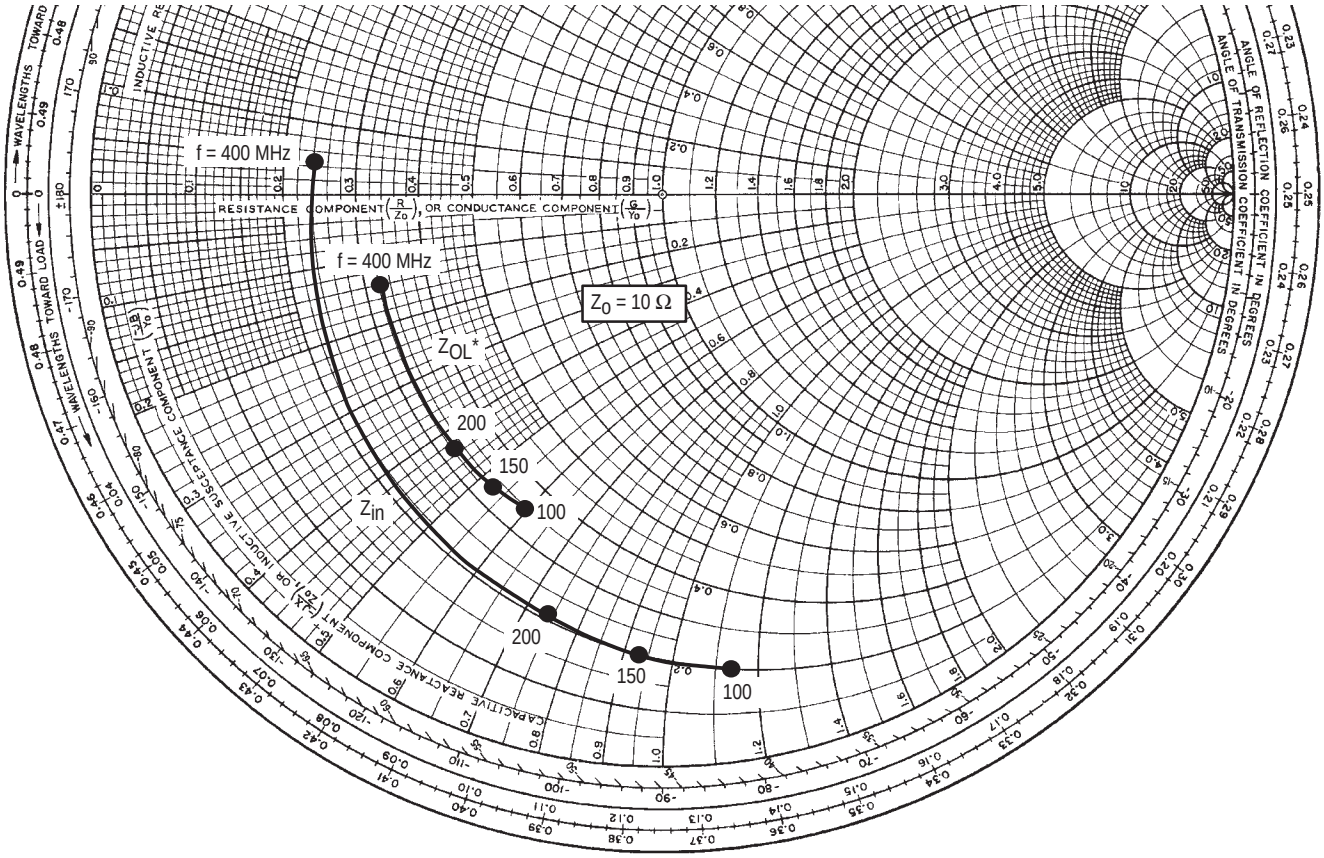


Figure 6. DC Safe Operating Area

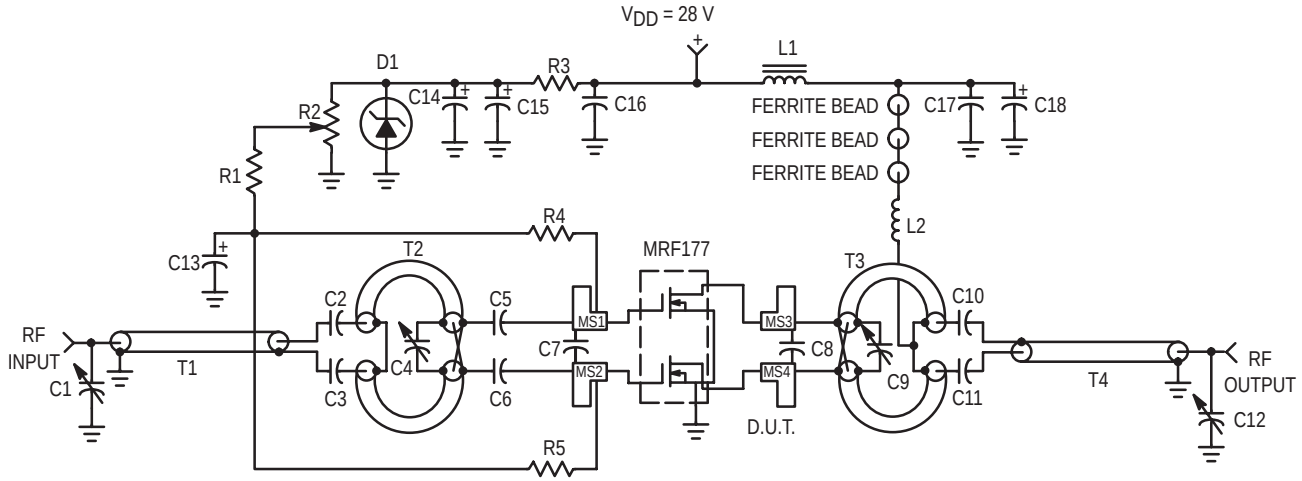


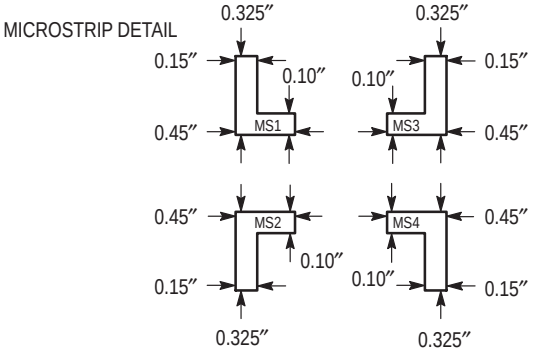
NOTE: Input and Output Impedance values given are measured gate–to–gate and drain–to–drain respectively.

V_{DD} = 28 V I_{DQ} = 200 mA P_{out} = 100 W		
f (MHz)	Z_{in} Ohms	Z_{OL}* Ohms
100	2.0 – j11.5	3.5 – j6
150	2.05 – j9.45	3.35 – j5.34
200	2.1 – j7.5	3.3 – j4.4
400	2.35 + j0.4	3.2 – j1.38

Z_{OL}*: Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

Figure 7. Impedance or Admittance Coordinates





C1, C12	1–10 pF JOHANSON OR EQUIVALENT	D1	1N5347B, 20 Vdc
C2, C3, C5, C6, C10, C11	270 pF ATC 100 MIL CHIP CAP	L1	1–TURN NO. 18, 0.25″, 2–HOLE FERRITE BEAD
C4, C9	1–20 pF	L2	8–1/2 TURNS NO. 18, CLOSE WOUND .375″ DIA.
C7	36 pF CHIP CAP	R1, R4, R5	10 kΩ @ 1/2 W RESISTOR
C8	10 pF CHIP CAP	R2	10 kΩ, 10 TURN RESISTOR
C13, C14	0.1 μFD @ 50 Vdc	R3	2.0 kΩ @ 1/2 W RESISTOR
C15, C18	10 μFD @ 50 Vdc	T1	1–1/2 T, 50 Ω COAX, .034″ DIA. ON DUAL 0.5″ FERRITE CORE
C16	500 pF BUTTON	T2	2.0″ 25 Ω COAX, .075″ DIA.
C17	1000 pF UNCASED MICA	T3	2.1″ 10 Ω COAX, .075″ DIA.
		T4	4.0″ 50 Ω COAX, .0865″ DIA.
		BOARD	Dielectric Thickness = 0.060″ 2oz Copper, Cu–Clad, Teflon Fiberglass, ε_r = 2.55

Figure 8. Test Circuit Electrical Schematic

NOTE: S–Parameter data represents measurements taken from one chip only.

Table 1. Common Source S–Parameters (V_{DS} = 24 V, I_D = 0.4 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.797	–154	12.40	88	0.029	2	0.756	–159
40	0.739	–161	9.06	89	0.027	8	0.702	–165
50	0.749	–164	6.84	85	0.026	7	0.707	–168
60	0.770	–163	6.06	80	0.027	3	0.754	–168
70	0.790	–164	5.40	73	0.027	–1	0.776	–168
80	0.800	–166	4.60	70	0.026	–1	0.777	–168
90	0.808	–167	3.94	67	0.025	–1	0.795	–168
100	0.816	–168	3.47	64	0.024	–1	0.809	–169
110	0.816	–169	3.14	62	0.023	1	0.809	–169
120	0.815	–170	2.76	61	0.022	6	0.794	–169
130	0.821	–171	2.45	59	0.021	12	0.799	–170
140	0.828	–171	2.27	56	0.022	18	0.806	–169
150	0.836	–171	2.10	53	0.028	25	0.805	–169
160	0.861	–172	1.96	51	0.032	–6	0.823	–168
170	0.863	–173	1.77	49	0.020	–4	0.836	–166
180	0.869	–173	1.63	46	0.018	5	0.881	–169
190	0.872	–174	1.52	44	0.017	14	0.894	–169
200	0.873	–175	1.41	43	0.017	25	0.888	–171
210	0.877	–176	1.28	42	0.018	36	0.877	–171
220	0.880	–176	1.18	41	0.019	46	0.868	–171
230	0.881	–177	1.15	38	0.024	51	0.926	–173
240	0.877	–178	1.09	35	0.031	56	0.893	–174
250	0.857	–180	1.04	33	0.049	55	0.903	–173
260	0.758	–178	0.95	31	0.090	24	0.903	–172
270	0.862	–171	0.87	31	0.056	–33	0.933	–173
280	0.902	–174	0.85	32	0.027	–39	0.949	–174
290	0.913	–176	0.77	30	0.017	–28	0.891	–175
300	0.919	–177	0.72	30	0.012	–8	0.894	–175
310	0.922	–178	0.71	28	0.012	11	0.913	–175
320	0.925	–178	0.67	26	0.012	28	0.896	–175
330	0.927	–179	0.64	24	0.012	40	0.929	–176
340	0.929	–179	0.62	24	0.013	46	0.925	–179
350	0.931	–180	0.58	24	0.015	52	0.942	–174
360	0.934	180	0.55	24	0.017	55	0.944	–176
370	0.937	179	0.52	23	0.019	61	0.944	–176
380	0.940	179	0.49	21	0.020	68	0.919	–175
390	0.941	178	0.45	22	0.020	69	0.938	–177
400	0.942	178	0.46	18	0.021	73	0.920	–173
410	0.941	177	0.45	19	0.023	67	0.961	–178
420	0.943	177	0.44	18	0.026	67	0.945	–178
430	0.945	176	0.41	16	0.029	70	0.959	–179

Table 1. Common Source S–Parameters (V_{DS} = 24 V, I_D = 0.4 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
440	0.947	176	0.38	16	0.029	75	0.962	–179
450	0.949	176	0.38	19	0.030	78	0.984	–178
460	0.952	175	0.36	17	0.029	72	0.987	178
470	0.953	175	0.34	18	0.030	70	0.976	179
480	0.952	174	0.34	14	0.035	69	0.968	179
490	0.952	174	0.34	14	0.039	72	0.987	178
500	0.952	174	0.32	13	0.040	76	1.002	179
600	0.938	170	0.22	9	0.047	117	1.013	172
700	0.962	166	0.19	13	0.060	73	0.993	171
800	0.953	162	0.17	18	0.097	68	0.981	171
900	0.953	159	0.14	21	0.097	65	0.949	166
1000	0.952	156	0.14	27	0.110	68	0.982	163

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 0.435 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.803	–153	13.50	89	0.028	3	0.746	–157
40	0.742	–160	9.90	90	0.026	9	0.686	–164
50	0.752	–163	7.48	85	0.025	8	0.692	–168
60	0.773	–163	6.62	80	0.026	4	0.739	–167
70	0.794	–164	5.91	74	0.026	1	0.761	–167
80	0.803	–166	5.04	70	0.025	1	0.763	–167
90	0.812	–167	4.32	68	0.024	1	0.783	–167
100	0.819	–168	3.81	64	0.022	1	0.798	–168
110	0.818	–169	3.44	62	0.022	3	0.797	–168
120	0.817	–170	3.03	61	0.021	9	0.779	–168
130	0.823	–171	2.68	59	0.020	15	0.784	–170
140	0.830	–171	2.49	57	0.021	21	0.793	–169
150	0.838	–171	2.30	53	0.027	27	0.792	–169
160	0.864	–172	2.16	52	0.030	–5	0.816	–167
170	0.865	–173	1.95	49	0.019	–2	0.827	–166
180	0.870	–173	1.79	46	0.017	8	0.869	–168
190	0.873	–174	1.67	44	0.016	18	0.882	–168
200	0.874	–175	1.55	43	0.017	27	0.878	–171
210	0.878	–176	1.40	42	0.017	37	0.866	–171
220	0.881	–176	1.29	41	0.019	47	0.858	–171
230	0.881	–177	1.25	38	0.025	53	0.918	–172
240	0.877	–178	1.20	35	0.031	59	0.882	–173
250	0.856	–180	1.13	33	0.048	57	0.893	–173
260	0.760	–178	1.03	31	0.088	24	0.899	–172
270	0.864	–171	0.96	31	0.056	–33	0.931	–172
280	0.903	–174	0.93	32	0.027	–38	0.946	–173
290	0.914	–176	0.85	30	0.015	–25	0.885	–174

Table 2. Common Source S–Parameters (V_{DS} = 28 V, I_D = 0.435 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
300	0.919	–177	0.79	30	0.010	–7	0.881	–175
310	0.922	–178	0.78	28	0.009	6	0.903	–175
320	0.925	–178	0.75	26	0.010	18	0.900	–175
330	0.927	–179	0.70	24	0.012	31	0.925	–176
340	0.929	–180	0.68	24	0.014	45	0.920	–178
350	0.931	180	0.63	25	0.015	63	0.932	–173
360	0.934	179	0.61	23	0.014	70	0.931	–176
370	0.936	179	0.57	23	0.013	68	0.929	–176
380	0.939	178	0.53	21	0.015	61	0.909	–176
390	0.941	178	0.50	22	0.018	61	0.940	–178
400	0.941	178	0.50	18	0.022	74	0.917	–173
410	0.940	177	0.49	19	0.024	80	0.955	–178
420	0.941	177	0.48	18	0.022	83	0.942	–178
430	0.943	176	0.46	16	0.020	77	0.957	–179
440	0.946	176	0.42	16	0.022	69	0.960	–178
450	0.948	175	0.41	18	0.029	71	0.982	–177
460	0.951	175	0.39	17	0.032	76	0.983	178
470	0.951	175	0.37	17	0.031	88	0.968	179
480	0.950	174	0.37	13	0.027	93	0.965	179
490	0.950	174	0.37	13	0.025	81	0.994	179
500	0.950	173	0.36	12	0.031	69	1.012	180
600	0.936	170	0.24	7	0.063	127	1.005	171
700	0.960	166	0.20	11	0.064	72	0.989	171
800	0.953	162	0.17	15	0.092	66	1.017	169
900	0.954	159	0.15	19	0.092	65	0.952	167
1000	0.952	156	0.15	24	0.082	56	0.988	162

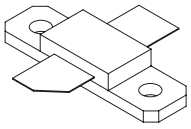
Product Is Not Recommended for New Design.
The next generation of higher performance products are in development. Visit our online Selector Guides (http://mot–sps.com/rf/sg/sg.html) for scheduled introduction dates.

MRF182
MRF182S, R1

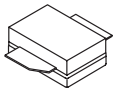
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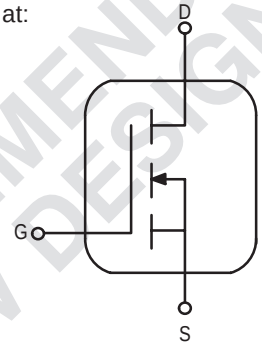
- High Gain, Rugged Device
- Broadband Performance from HF to 1 GHz
- Bottom Side Source Eliminates DC Isolators, Reducing Common Mode Inductances
- MRF182S Available in Tape and Reel by Adding R1 Suffix to Part Number. MRF182SR1 = 500 Units per 24 mm, 13 inch Reel.
- LDMOS Models and Circuit Board Artwork Available at: http://mot–sps.com/rf/designtds/



CASE 360B–03, STYLE 1
(MRF182)



CASE 360C–03, STYLE 1
(MRF182S)



NOT RECOMMENDED FOR NEW DESIGN

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Total Device Dissipation @ T_C = 70°C Derate above 70°C	P_D	74 0.57	W W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

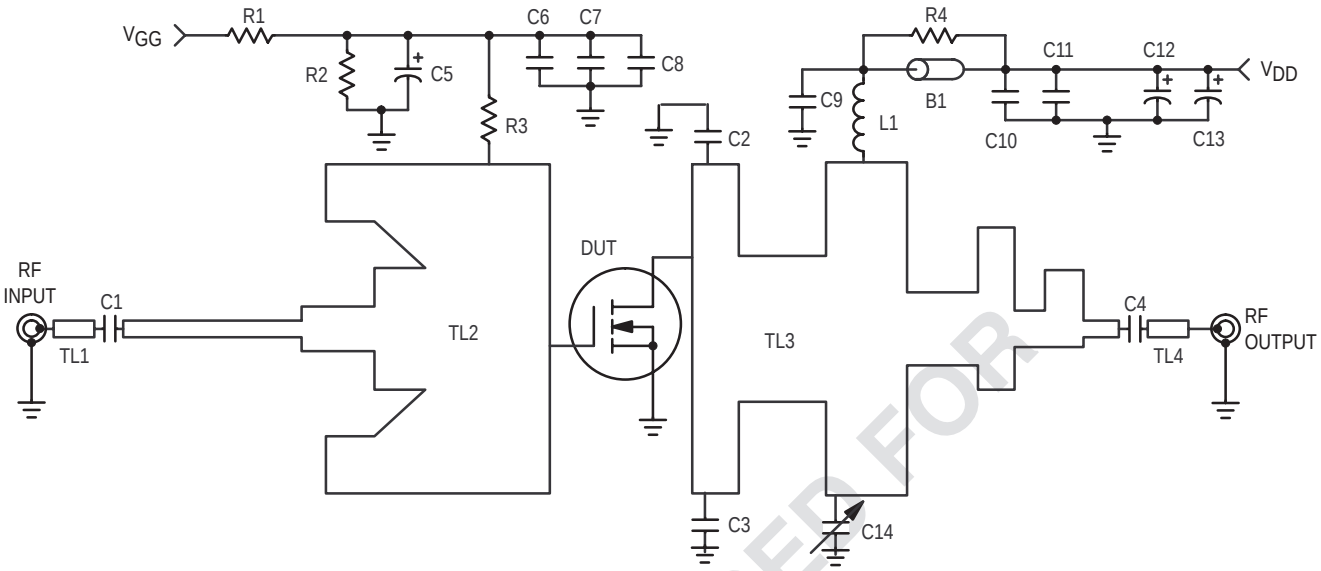
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 1.0 μAdc)	$V_{(BR)DSS}$	65	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	–	–	1	μAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	–	–	1	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 μA)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 50 mA)	$V_{GS(Q)}$	3	4	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3 A)	$V_{DS(on)}$	–	0.9	1.2	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3 A)	g_{fs}	1.6	1.8	–	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	–	56	–	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	–	28	–	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	–	2.5	–	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 50 mA, f = 945 MHz)	G_{ps}	11	14	–	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 50 mA, f = 945 MHz)	η	50	58	–	%
Load Mismatch (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 50 mA, f = 945 MHz, Load VSWR 5:1 at All Phase Angles)	Ψ	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 50 mA, f = 960 MHz)	Z_{in}	–	0.81 + j1.6	–	ohms
Series Equivalent Output Impedance (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 50 mA, f = 960 MHz)	Z_{out}	–	2.15 – j1.7	–	ohms

NOT RECOMMENDED FOR NEW DESIGN



B1	Short RF Bead Fair Rite–274301944	L1	5 Turns, 20 AWG, IDIA 0.126
C1	18 pF Chip Capacitor	R1	10 kΩ, 1/4 W Resistor
C2, C3, C6, C9	43 pF Chip Capacitor	R2	13 kΩ, 1/4 W Resistor
C4	100 pF Chip Capacitor	R3	1.0 kΩ, 1/4 W Chip Resistor
C5, C12	10 μF, 50 Vdc Electrolytic Capacitor	R4	4 x 39 Ω, 1/8 W Chip Resistor
C7, C10	1000 pF Chip Capacitor	TL1–TL4	Microstrip Line See Photomaster
C8, C11	0.1 μF, 50 Vdc Chip Capacitor	Ckt Board	1/32″ Glass Teflon, ε_r = 2.55
C13	250 μF, 50 Vdc Electrolytic Capacitor		ARLON–GX–0300–55–22
C14	0.6–4.5 pF Variable Capacitor		

Figure 1. MRF182 Schematic

NOT RECOMMENDED FOR NEW DESIGN

TYPICAL CHARACTERISTICS

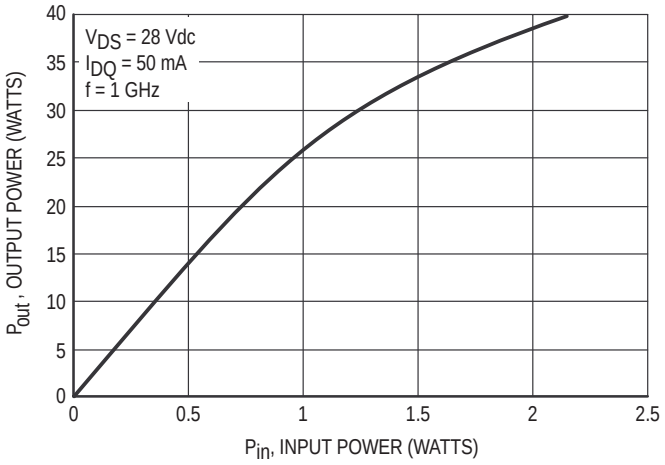


Figure 2. Output Power versus Input Power at 1 GHz

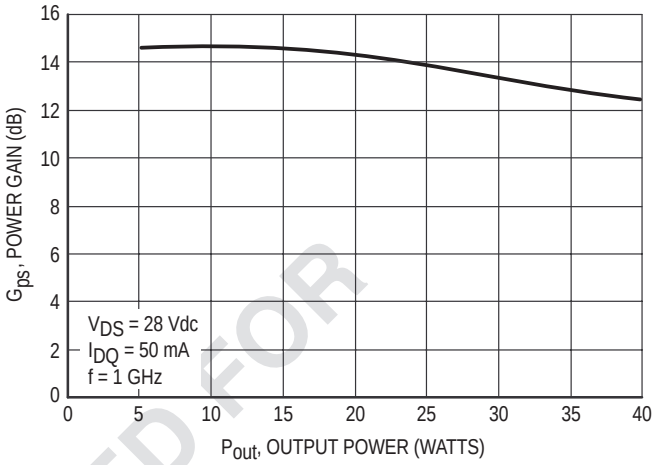


Figure 3. Power Gain versus Output Power at 1 GHz

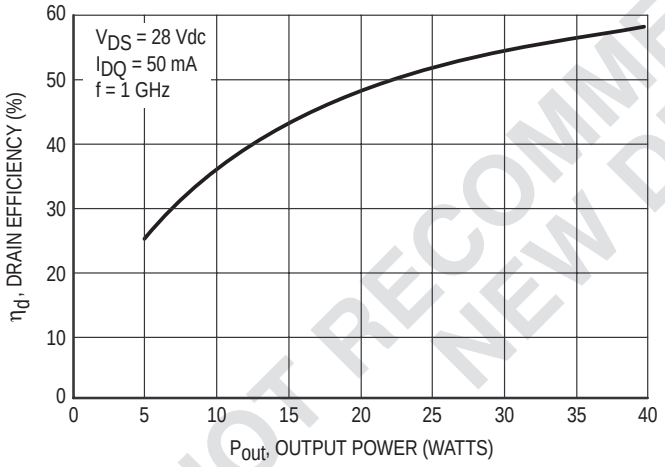


Figure 4. Drain Efficiency versus Output Power at 1 GHz

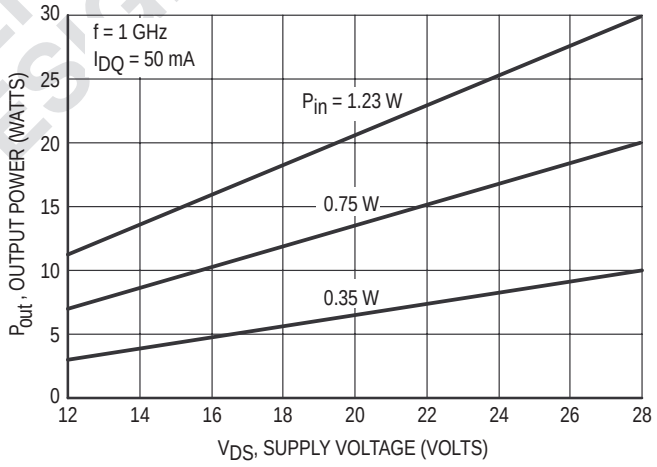


Figure 5. Output Power versus Supply Voltage

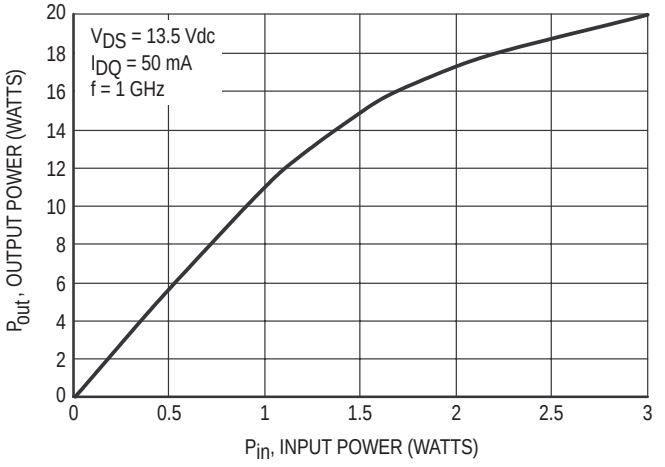


Figure 6. Output Power versus Input Power

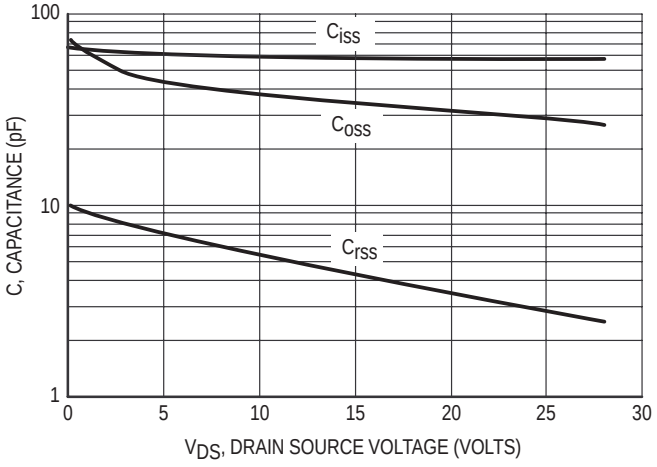


Figure 7. Capacitance versus Drain Source Voltage

NOT RECOMMENDED FOR NEW DESIGN

Table 1. Typical Common Source S–Parameters (V_{DS} = 13.5 V)

I_D = 1.0 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
20	0.933	–131	40.81	112	0.021	22	0.664	–138
30	0.922	–148	29.31	104	0.022	15	0.700	–151
40	0.892	–156	22.19	99	0.022	10	0.718	–158
50	0.877	–161	17.91	95	0.023	7	0.725	–162
60	0.870	–164	14.67	92	0.023	4	0.732	–164
70	0.863	–166	12.57	90	0.022	2	0.735	–166
80	0.860	–168	11.00	89	0.022	1	0.738	–168
90	0.860	–169	9.79	87	0.022	0	0.740	–169
100	0.859	–170	8.79	86	0.022	–1	0.741	–169
150	0.859	–173	5.78	80	0.022	–7	0.750	–172
200	0.862	–175	4.29	74	0.022	–11	0.759	–172
250	0.868	–176	3.38	69	0.021	–14	0.770	–173
300	0.880	–177	2.77	65	0.020	–17	0.780	–173
350	0.877	–177	2.32	61	0.020	–19	0.793	–173
400	0.882	–178	1.98	56	0.019	–22	0.808	–173
450	0.892	–179	1.72	52	0.018	–24	0.816	–173
500	0.899	–180	1.51	49	0.017	–26	0.828	–174
550	0.898	180	1.33	45	0.017	–27	0.838	–174
600	0.907	179	1.19	42	0.016	–28	0.849	–175
650	0.914	179	1.07	38	0.015	–28	0.859	–175
700	0.916	177	0.95	35	0.014	–25	0.867	–176
750	0.920	177	0.88	34	0.015	–26	0.874	–176
800	0.924	176	0.80	30	0.015	–27	0.884	–177
850	0.929	175	0.74	27	0.015	–33	0.891	–178
900	0.929	174	0.68	25	0.013	–38	0.897	–178
950	0.933	173	0.63	22	0.011	–39	0.905	–179
1000	0.934	173	0.58	20	0.010	–37	0.912	–180
1050	0.930	172	0.54	17	0.009	–33	0.918	180
1100	0.938	171	0.52	15	0.009	–29	0.924	179
1150	0.933	170	0.48	13	0.008	–28	0.929	178
1200	0.930	169	0.45	10	0.008	–25	0.930	177
1250	0.939	168	0.42	8	0.007	–23	0.935	177
1300	0.936	168	0.40	6	0.007	–21	0.934	176
1350	0.933	167	0.38	4	0.006	–19	0.936	175
1400	0.937	166	0.35	2	0.005	–14	0.939	174
1450	0.937	165	0.33	0	0.005	–5	0.934	174
1500	0.927	164	0.32	–2	0.004	0	0.930	173

NOT RECOMMENDED FOR NEW DESIGN

Table 2. Typical Common Emitter S–Parameters (V_{DS} = 28 V)

I_D = 1.0 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
20	0.964	–99	54.39	129	0.014	39	0.429	–108
30	0.949	–121	43.46	118	0.017	28	0.478	–125
40	0.909	–134	34.35	109	0.018	20	0.520	–137
50	0.884	–142	28.27	103	0.018	15	0.540	–144
60	0.875	–148	23.38	98	0.019	11	0.553	–149
70	0.862	–152	20.10	95	0.019	8	0.562	–152
80	0.861	–156	17.64	92	0.019	5	0.569	–154
90	0.858	–158	15.72	90	0.019	3	0.575	–156
100	0.858	–160	14.11	88	0.019	1	0.580	–157
150	0.856	–166	9.26	79	0.018	–7	0.606	–160
200	0.862	–169	6.80	71	0.018	–12	0.633	–161
250	0.871	–171	5.29	65	0.017	–16	0.661	–161
300	0.882	–173	4.27	59	0.016	–21	0.690	–162
350	0.883	–174	3.52	54	0.015	–23	0.718	–162
400	0.895	–175	2.97	49	0.014	–26	0.747	–163
450	0.904	–176	2.54	45	0.013	–28	0.767	–164
500	0.911	–177	2.20	41	0.012	–30	0.789	–165
550	0.911	–178	1.90	37	0.011	–30	0.807	–166
600	0.923	–179	1.69	33	0.010	–30	0.825	–167
650	0.929	–180	1.50	30	0.009	–29	0.841	–168
700	0.929	179	1.32	26	0.009	–22	0.855	–169
750	0.933	178	1.21	24	0.010	–22	0.865	–170
800	0.938	177	1.09	21	0.009	–20	0.877	–171
850	0.942	176	1.00	18	0.010	–31	0.886	–172
900	0.942	175	0.92	16	0.008	–37	0.894	–173
950	0.947	174	0.84	13	0.006	–38	0.904	–174
1000	0.946	173	0.77	11	0.005	–28	0.912	–175
1050	0.943	172	0.72	8	0.005	–18	0.919	–176
1100	0.948	171	0.67	6	0.004	–9	0.926	–177
1150	0.945	171	0.62	4	0.005	0	0.932	–178
1200	0.939	170	0.59	1	0.004	3	0.934	–179
1250	0.949	169	0.54	0	0.005	12	0.940	–180
1300	0.947	168	0.51	–3	0.005	18	0.939	180
1350	0.944	167	0.48	–4	0.005	22	0.941	179
1400	0.945	166	0.44	–7	0.004	34	0.943	178
1450	0.944	165	0.42	–9	0.005	45	0.940	177
1500	0.933	164	0.40	–10	0.005	55	0.936	176

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Product Is Not Recommended for New Design.
The next generation of higher performance products are in development. Visit our online Selector Guides (http://mot–sps.com/rf/sg/sg.html) for scheduled introduction dates.

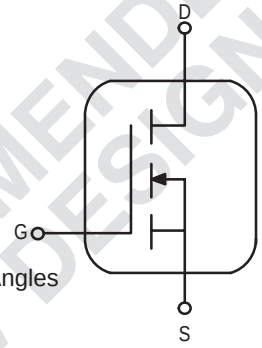
MRF183
MRF183S, R1

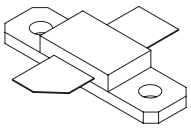
The RF MOSFET Line
RF Power
Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

45 W, 1.0 GHz
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

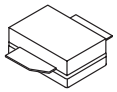
Designed for broadband commercial and industrial applications at frequencies to 1.0 GHz. The high gain and broadband performance of these devices makes them ideal for large–signal, common source amplifier applications in 28 volt base station equipment.

- Guaranteed Performance at 945 MHz, 28 Volts
  Output Power – 45 Watts PEP
  Power Gain – 11.5 dB
  Efficiency – 33%
  IMD – 28 dBc
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 28 Vdc, 945 MHz, 45 Watts CW
- MRF183S Available in Tape and Reel by Adding R1 Suffix to Part Number. MRF183SR1 = 500 Units per 24 mm, 13 inch Reel.
- LDMOS Models, Test Fixture and Circuit Board Artwork Available at: http://mot–sps.com/rf/designtds/





CASE 360B–03, STYLE 1
(MRF183)



CASE 360C–03, STYLE 1
(MRF183S)

NOT RECOMMENDED FOR NEW DESIGN

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (RGS = 1 Meg Ohm)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current – Continuous	I_D	5	Adc
Total Device Dissipation @ T_C = 70°C Derate above 70°C	P_D	86 0.67	W W/°C
Storage Temperature Range	T_{stg}	– 65 to +200	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 50 μAdc)	BV_{DSS}	65	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	–	–	1	μAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	–	–	1	μAdc
ON CHARACTERISTICS					
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 250 mAdc)	$V_{GS(Q)}$	3	–	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3 A)	$V_{DS(on)}$	–	0.7	–	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 5 Adc)	g_{fs}	–	2	–	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	–	82	–	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	–	38	–	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	–	4.5	–	pF

FUNCTIONAL TESTS (In Motorola Test Fixture)

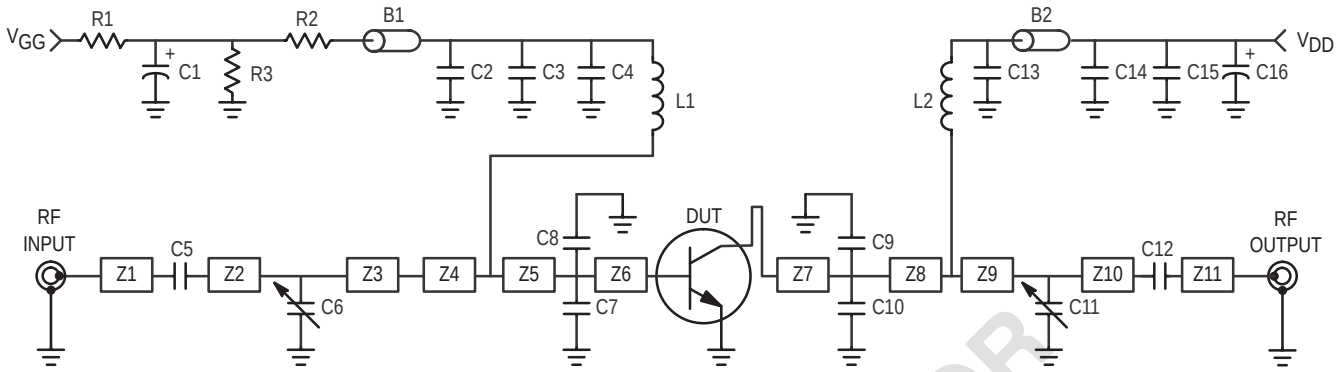
(V_{DD} = 28 Vdc, P_{out} = 45 Watts PEP, f1 = 945.0, f2 = 945.1 MHz, I_{DQ} = 250 mA)

Two–Tone Common Source Amplifier Power Gain	G_{ps}	11.5	13.5	–	dB
Two–Tone Drain Efficiency	η	33	38	–	%
3rd Order Intermodulation Distortion	IMD	–	–32	–28	dBc
Input Return Loss	IRL	9	14	–	dB

(V_{DD} = 28 Vdc, P_{out} = 45 Watts PEP, f1 = 930.0, f2 = 930.1 MHz, and f1 = 960.0, f2 = 960.1 MHz, I_{DQ} = 250 mA)

Two–Tone Common Source Amplifier Power Gain	G_{ps}	–	13	–	dB
Two–Tone Drain Efficiency	η	–	35	–	%
3rd Order Intermodulation Distortion	IMD	–	–32	–	dBc
Input Return Loss	IRL	–	12	–	dB
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 45 Watts CW, I_{DQ} = 250 mA, f = 945 MHz, VSWR 5:1 at All Phase Angles)	Ψ	No Degradation in Output Power Before and After Test			

NOT RECOMMENDED FOR NEW DESIGN



B1	Short Ferrite Bead	R3	4.7 MΩ, 1/4 W Carbon
B2	Long Ferrite Bead	Z1	T–Line, 0.200″ x 0.080″
C1	10 μF, 50 V Electrolytic Capacitor	Z2	T–Line, 0.570″ x 0.120″
C2, C14	0.1 μF Chip Capacitor	Z3	T–Line, 0.610″ x 0.320″
C3	1000 pF Chip Capacitor	Z4	T–Line, 0.160″ x 0.320″ x 0.620″ Tapered Line
C4, C13	47 pf Chip Capacitor		
C5, C12	47 pF Chip Capacitor	Z5	T–Line, 0.650″ x 0.620″
C6, C11	0.8–8.0 pF Trim Capacitor	Z6	T–Line, 0.020″ x 0.620″
C7, C8	10 pF Chip Capacitor	Z7	T–Line, 0.270″ x 0.320″
C9, C10	10 pF Chip Capacitor	Z8	T–Line, 0.130″ x 0.320″
C15	100 pF Chip Capacitor	Z9	T–Line, 0.370″ x 0.080″
C16	250 μF, 50 V Electrolytic Capacitor	Z10	T–Line, 1.050″ x 0.080″
L1, L2	5 Turns, 24 AWG, ID 0.059″	Z11	T–Line, 0.290″ x 0.080″
R1	120 Ω, 1/4 W Carbon	Board	0.030″ Glass Teflon, ε_r = 2.55 ARLON–GX–0300–55–22
R2	18 kΩ, 1/4 W Carbon		

Figure 1. MRF183S Two Tone Test Circuit Schematic

NOT RECOMMENDED FOR NEW DESIGN

TYPICAL CHARACTERISTICS

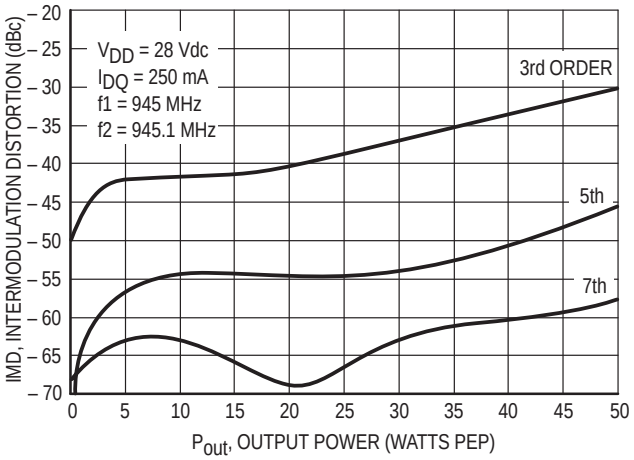


Figure 2. Intermodulation Distortion Products versus Output Power

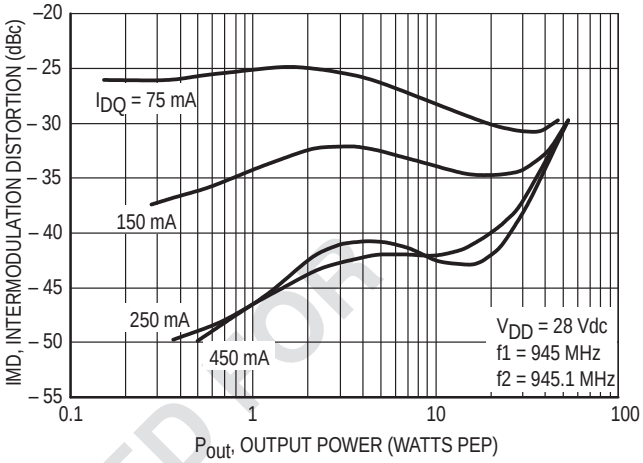


Figure 3. Intermodulation Distortion versus Output Power

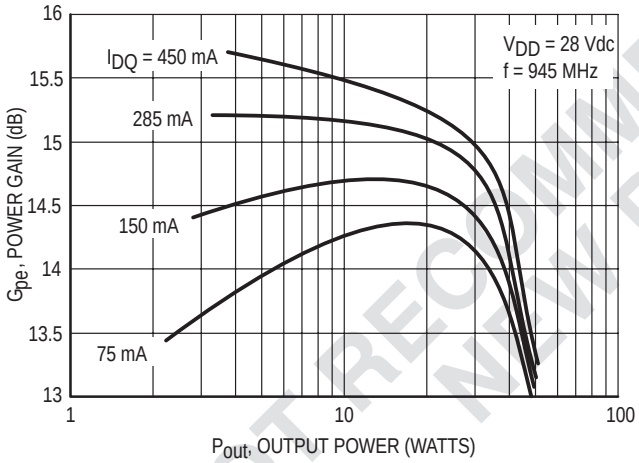


Figure 4. Power Gain versus Output Power

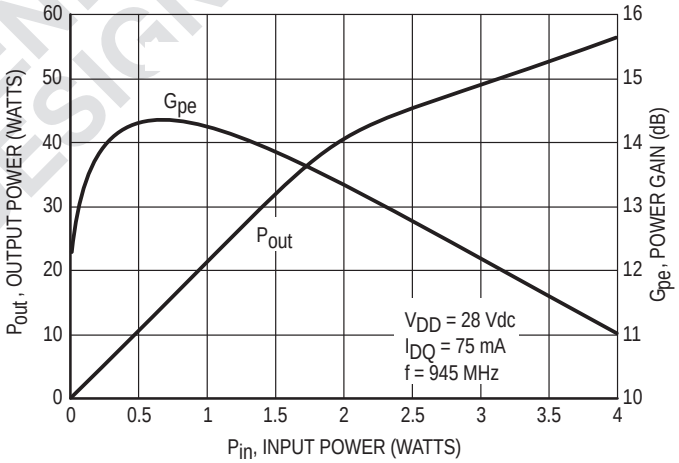


Figure 5. Output Power versus Input Power

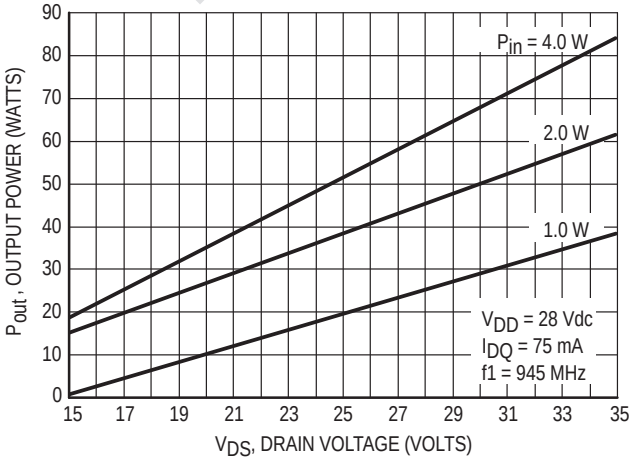


Figure 6. Output Power versus Drain Bias Supply Voltage

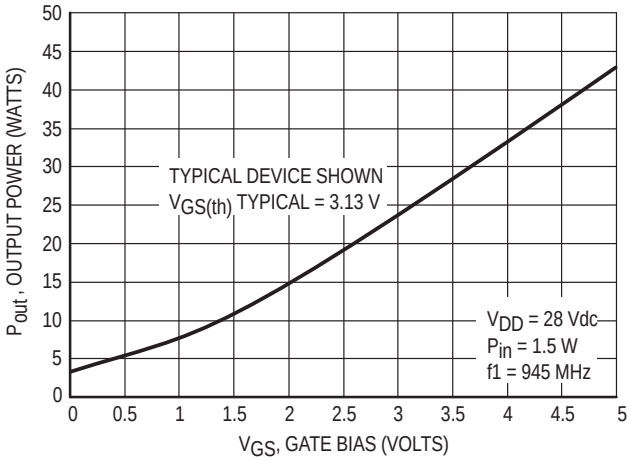


Figure 7. Output Power versus Gate Bias Supply Voltage

NOT RECOMMENDED FOR NEW DESIGN

TYPICAL CHARACTERISTICS

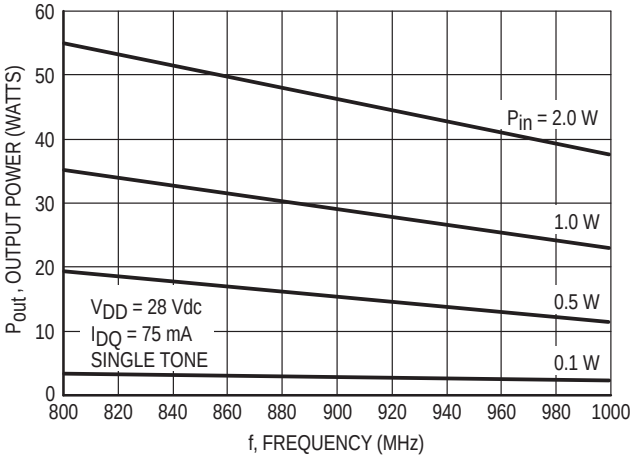


Figure 8. Output Power versus Frequency

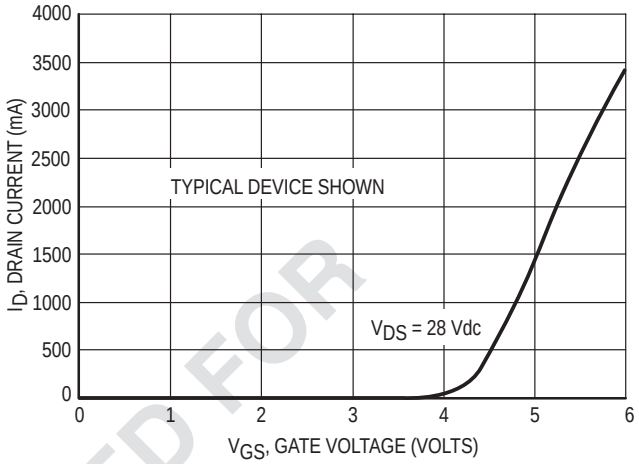


Figure 9. Drain Current versus Gate Voltage

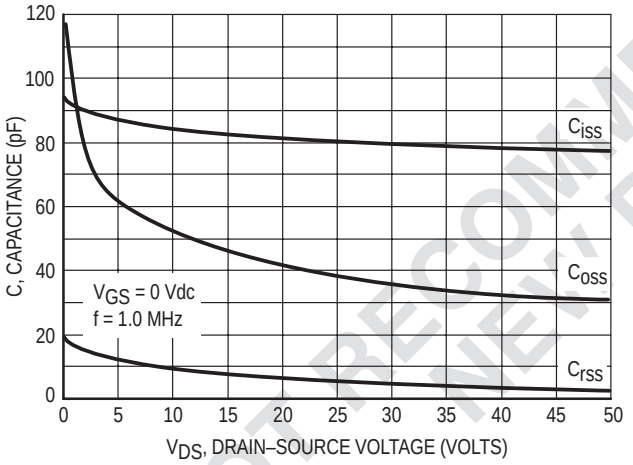


Figure 10. Capacitance versus Voltage

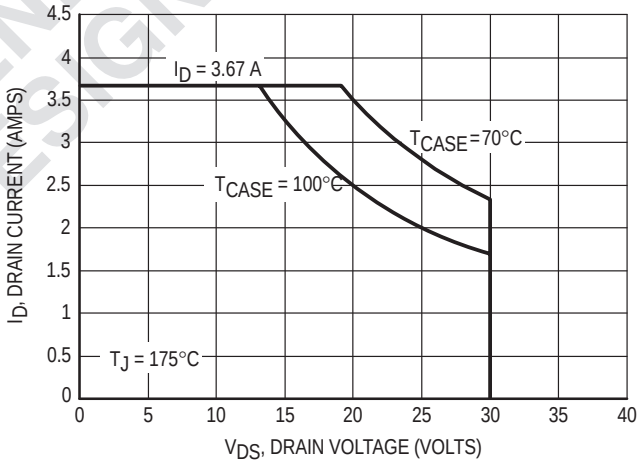


Figure 11. Class A Safe Operating Region

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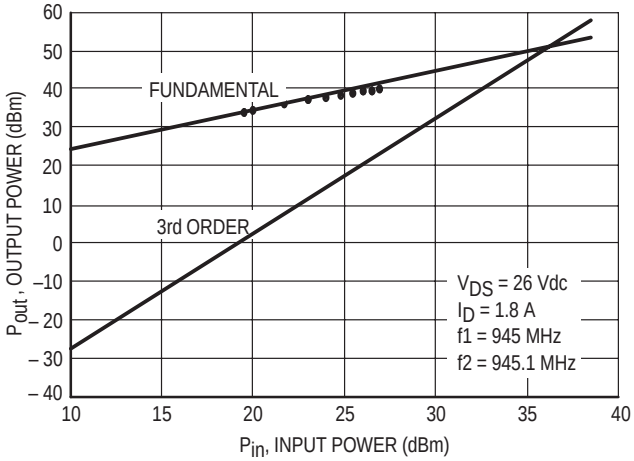


Figure 12. Class A Third Order Intercept Point

TYPICAL CHARACTERISTICS

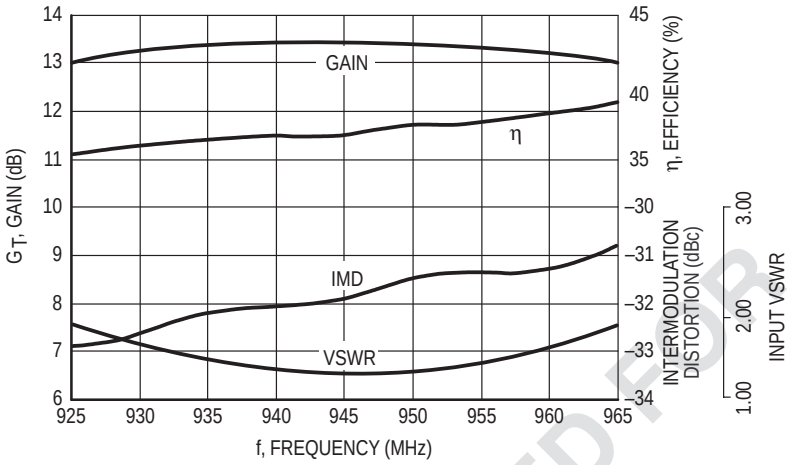


Figure 13. Broadband Power Performance of MRF183S

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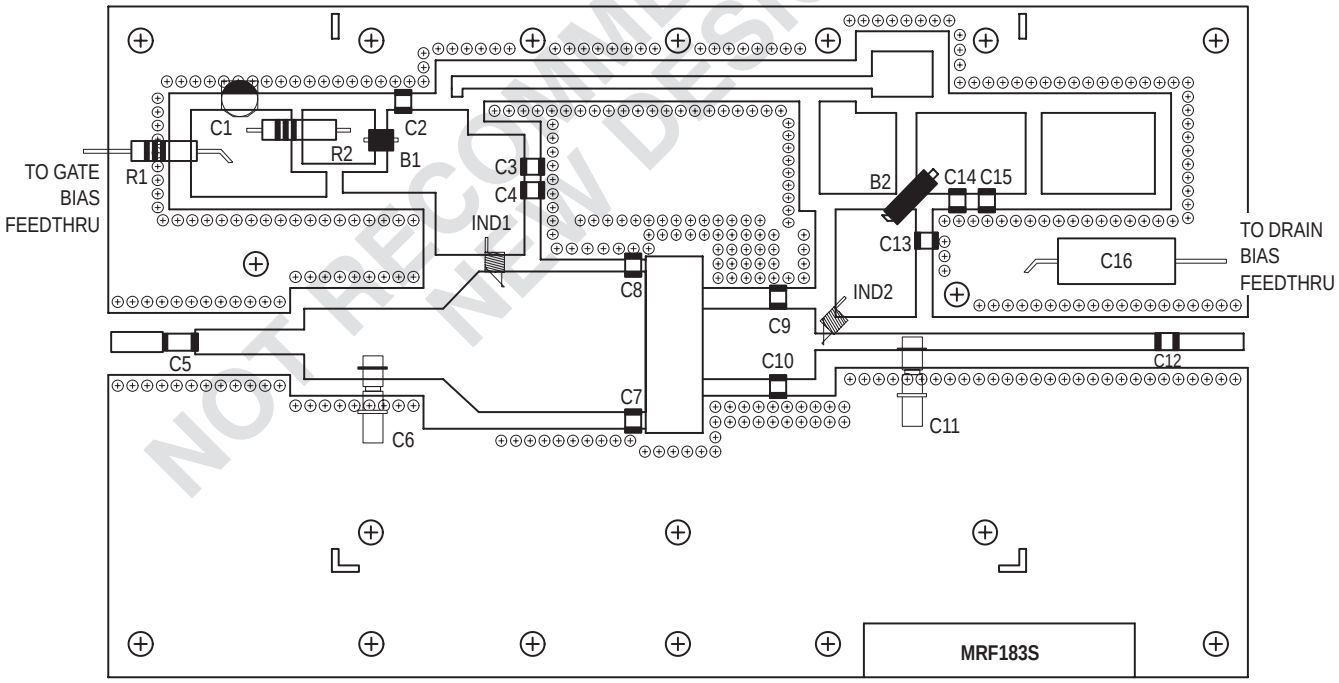
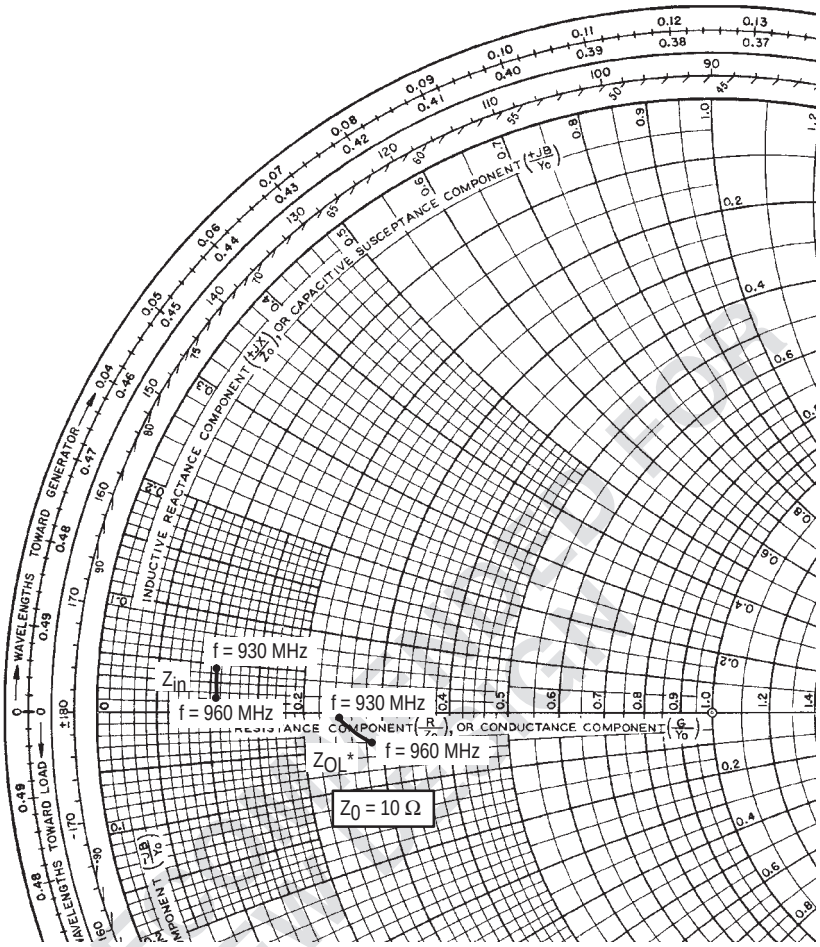


Figure 14. MRF183S Two Tone Test Circuit Component Parts Layout



V_{DD} = 28 V, I_{DQ} = 250 mA, P_{out} = 45 W (PEP)

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
930	1.10 + j0.93	2.60 – j0.13
945	1.10 + j0.78	2.70 – j0.28
960	1.10 + j0.60	2.80 – j0.42

Z_{in} = Conjugate of source impedance.

Z_{OL} = Conjugate of the load impedance at given output power, voltage and current conditions.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

Figure 15. Series Equivalent Input and Output Impedance

NOT RECOMMENDED FOR NEW DESIGN

Table 1. Typical Common Source S–Parameters (V_{DS} = 13.5 V)

I_D = 1.5 A

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
20	0.954	–157	29.58	100	0.017	11	0.778	–161
30	0.941	–164	19.73	96	0.017	8	0.796	–168
40	0.922	–168	14.84	93	0.017	4	0.804	–170
50	0.907	–171	11.94	91	0.017	3	0.808	–172
60	0.903	–172	9.75	89	0.017	2	0.812	–173
70	0.899	–173	8.34	88	0.017	0	0.814	–174
80	0.898	–174	7.29	86	0.017	–1	0.816	–175
90	0.896	–175	6.49	85	0.017	–2	0.816	–175
100	0.897	–175	5.83	84	0.017	–2	0.817	–175
150	0.895	–177	3.82	79	0.017	–6	0.822	–176
200	0.898	–178	2.84	74	0.016	–9	0.828	–176
250	0.902	–178	2.24	70	0.016	–11	0.835	–176
300	0.908	–179	1.84	66	0.015	–14	0.842	–176
350	0.905	–179	1.55	62	0.015	–16	0.850	–176
400	0.913	–180	1.32	58	0.014	–18	0.861	–176
450	0.920	180	1.15	54	0.014	–18	0.865	–176
500	0.924	179	1.01	51	0.013	–20	0.874	–177
550	0.922	179	0.89	47	0.013	–21	0.881	–177
600	0.931	178	0.80	44	0.012	–21	0.889	–177
650	0.935	178	0.72	41	0.011	–20	0.895	–177
700	0.935	177	0.64	38	0.011	–17	0.901	–178
750	0.937	177	0.59	37	0.012	–18	0.905	–178
800	0.940	176	0.54	33	0.012	–20	0.913	–178
850	0.943	176	0.50	30	0.012	–29	0.919	–179
900	0.945	175	0.46	28	0.010	–33	0.924	–179
950	0.947	174	0.43	26	0.009	–34	0.930	–180
1000	0.947	174	0.40	24	0.008	–29	0.935	180
1050	0.947	173	0.37	21	0.007	–24	0.939	179
1100	0.952	172	0.35	19	0.007	–19	0.944	179
1150	0.949	172	0.32	17	0.007	–17	0.948	178
1200	0.946	171	0.30	14	0.006	–16	0.948	177
1250	0.954	170	0.28	12	0.006	–13	0.953	177
1300	0.952	170	0.27	9	0.006	–12	0.950	176
1350	0.949	169	0.26	9	0.006	–10	0.951	176
1400	0.948	168	0.23	8	0.005	–7	0.953	175
1450	0.948	168	0.22	6	0.004	4	0.948	174
1500	0.940	167	0.21	4	0.004	19	0.944	174

NOT RECOMMENDED FOR NEW DESIGN

Table 2. Typical Common Source S–Parameters (V_{DS} = 28 V)

I_D = 1.5 A

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
20	0.968	–132	45.79	113	0.014	24	0.579	–145
30	0.953	–145	31.75	106	0.015	17	0.623	–157
40	0.921	–154	24.33	99	0.015	12	0.648	–161
50	0.904	–159	19.68	95	0.015	7	0.661	–164
60	0.898	–163	16.11	92	0.015	5	0.670	–166
70	0.890	–165	13.79	90	0.015	2	0.677	–167
80	0.886	–167	12.06	87	0.015	1	0.681	–168
90	0.886	–168	10.71	86	0.015	–1	0.684	–169
100	0.887	–169	9.61	84	0.015	–3	0.688	–169
150	0.886	–172	6.26	76	0.015	–9	0.706	–170
200	0.890	–174	4.59	69	0.014	–13	0.724	–170
250	0.898	–175	3.57	64	0.014	–17	0.744	–169
300	0.906	–176	2.88	59	0.013	–19	0.764	–169
350	0.908	–177	2.37	54	0.012	–23	0.785	–169
400	0.915	–178	2.00	49	0.011	–24	0.807	–170
450	0.924	–178	1.71	45	0.010	–25	0.821	–170
500	0.930	–179	1.48	41	0.010	–26	0.838	–171
550	0.928	–180	1.28	37	0.009	–26	0.851	–171
600	0.937	180	1.13	33	0.008	–25	0.865	–172
650	0.944	179	1.00	30	0.007	–22	0.878	–172
700	0.943	178	0.88	27	0.008	–14	0.888	–173
750	0.946	178	0.81	25	0.008	–15	0.895	–173
800	0.949	177	0.73	22	0.009	–17	0.906	–174
850	0.954	177	0.67	20	0.009	–28	0.912	–175
900	0.953	175	0.61	18	0.007	–34	0.919	–175
950	0.957	175	0.56	15	0.005	–32	0.927	–176
1000	0.957	174	0.51	13	0.004	–22	0.934	–177
1050	0.957	174	0.48	10	0.004	–11	0.939	–178
1100	0.962	173	0.45	8	0.004	–2	0.945	–178
1150	0.959	172	0.41	7	0.004	3	0.950	–179
1200	0.955	171	0.39	4	0.004	9	0.950	–180
1250	0.962	170	0.36	2	0.004	13	0.955	180
1300	0.959	170	0.33	0	0.004	17	0.953	179
1350	0.956	169	0.31	–1	0.004	25	0.954	178
1400	0.954	168	0.29	–4	0.004	32	0.957	177
1450	0.955	168	0.28	–6	0.004	46	0.952	177
1500	0.948	167	0.26	–7	0.004	56	0.948	176

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Product Is Not Recommended for New Design.
The next generation of higher performance products are in development. Visit our online Selector Guides (http://mot–sps.com/rf/sg/sg.html) for scheduled introduction dates.

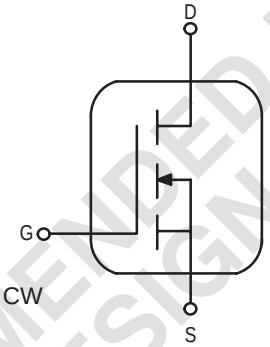
MRF184
MRF184S, R1

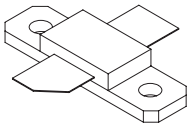
The RF MOSFET Line
RF POWER Field-Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

60 W, 1.0 GHz
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

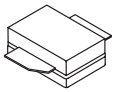
Designed for broadband commercial and industrial applications at frequencies to 1.0 GHz. The high gain and broadband performance of these devices makes them ideal for large–signal, common source amplifier applications in 28 volt base station equipment.

- Guaranteed Performance @ 945 MHz, 28 Volts
  Output Power = 60 Watts
  Power Gain = 11.5 dB
  Efficiency = 53%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 28 Vdc, 945 MHz, 60 Watts CW
- MRF184S Available in Tape and Reel by Adding R1 Suffix to Part Number. MRF184SR1 = 500 Units per 24 mm, 13 inch Reel.
- LDMOS Models, Test Fixture, Reference Design and Circuit Board Artwork Available at: http://mot–sps.com/rf/designtds/





CASE 360B–03, STYLE 1
(MRF184)



CASE 360C–03, STYLE 1
(MRF184S)

NOT RECOMMENDED FOR NEW DESIGN

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	7	Adc
Total Device Dissipation @ T_C = 70°C Derate above 70°C	P_D	118 0.9	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.1	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 V, I_D = 1 μAdc)	$V_{(BR)DSS}$	65	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	–	–	1	μAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0 V)	I_{GSS}	–	–	1	μAdc

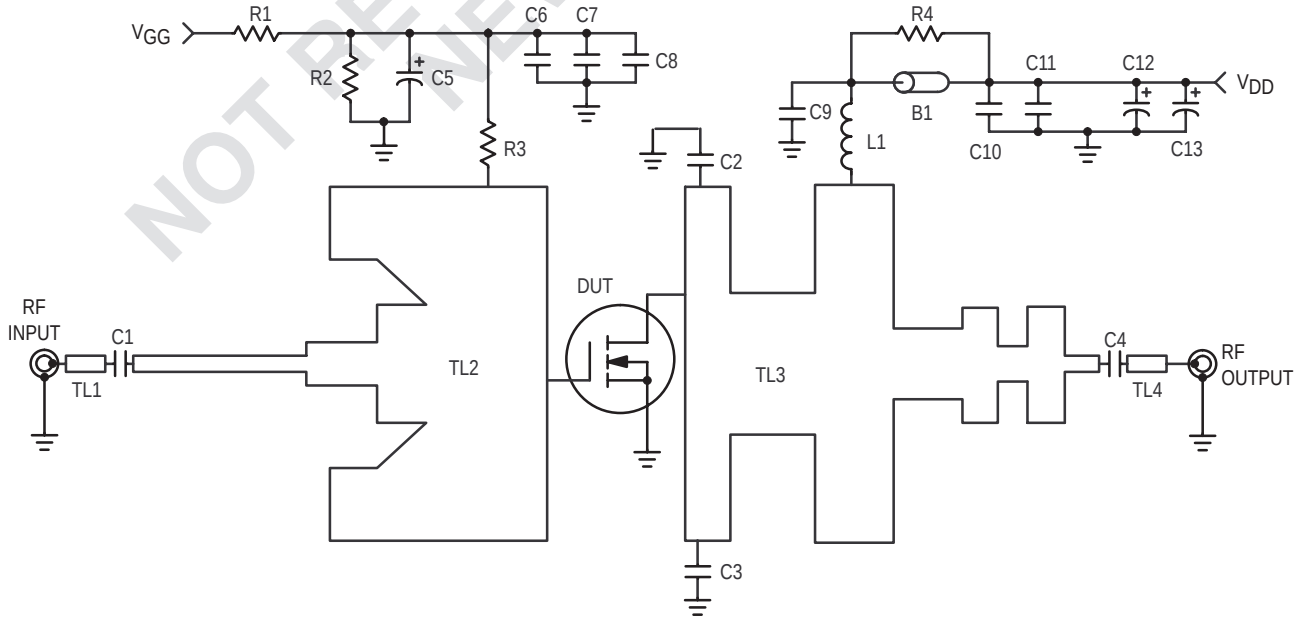
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 7

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 200 μA)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 100 mA)	$V_{GS(Q)}$	3	4	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3 A)	$V_{DS(on)}$	–	0.65	0.8	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3 A)	g_{fs}	2.2	2.6	–	s
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	–	83	–	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1 MHz)	C_{oss}	–	44	–	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1 MHz)	C_{rss}	–	4.3	–	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 60 W, f = 945 MHz, I_{DQ} = 100 mA)	G_{ps}	11.5	13.5	–	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 60 W, f = 945 MHz, I_{DQ} = 100 mA)	η	53	60	–	%
Load Mismatch (V_{DD} = 28 V, P_{out} = 60 W, I_{DQ} = 100 mA, f = 945 MHz, Load VSWR 5:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOT RECOMMENDED FOR NEW DESIGN



B1	Short RF Bead Fair Rite–2743019447	L1	5 Turns, 20 AWG, IDIA 0.126″
C1	18 pF Chip Capacitor	R1	10 kΩ, 1/4 W Resistor
C2, C3, C6, C9	43 pF Chip Capacitor	R2	13 kΩ, 1/4 W Resistor
C4	100 pF Chip Capacitor	R3	1.0 kΩ, 1/4 W Chip Resistor
C5, C12	10 μF, 50 Vdc Electrolytic Capacitor	R4	4 x 39 Ω, 1/8 W Chip Resistor
C7, C10	1000 pF Chip Capacitor	TL1–TL4	Microstrip Line See Photomaster
C8, C11	0.1 μF, 50 Vdc Chip Capacitor	Ckt Board	1/32″ Glass Teflon, ε_r = 2.55
C13	250 μF, 50 Vdc Electrolytic Capacitor		ARLON–GX–0300–55–22

Figure 1. MRF184 Test Circuit Schematic

TYPICAL CHARACTERISTICS

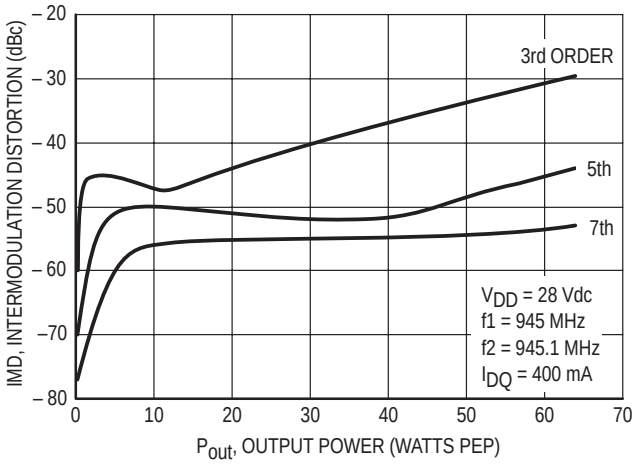


Figure 2. Intermodulation Distortion Products versus Output Power

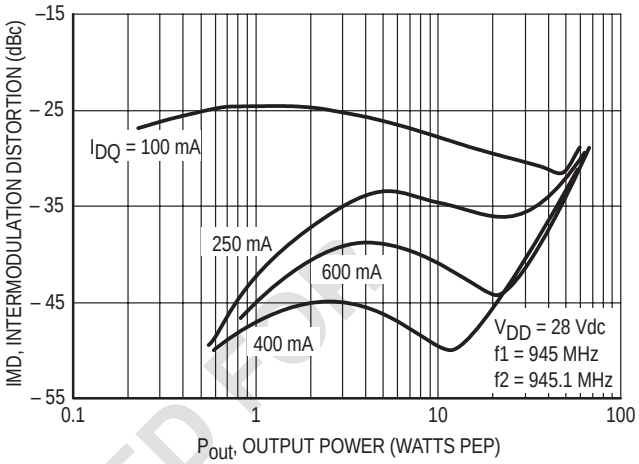


Figure 3. Intermodulation Distortion versus Output Power

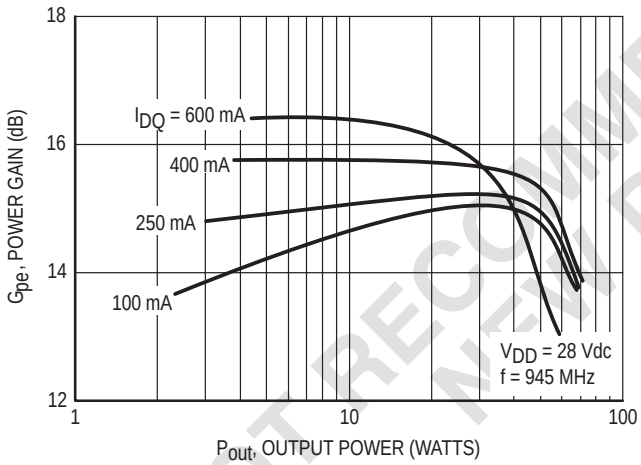


Figure 4. Power Gain versus Output Power

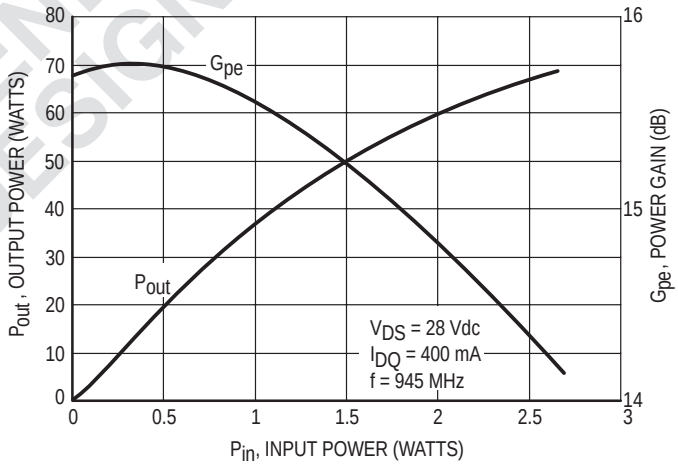


Figure 5. Output Power versus Input Power

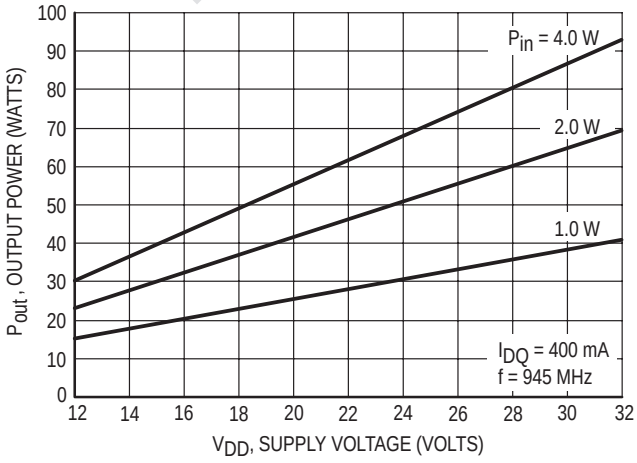


Figure 6. Output Power versus Supply Voltage

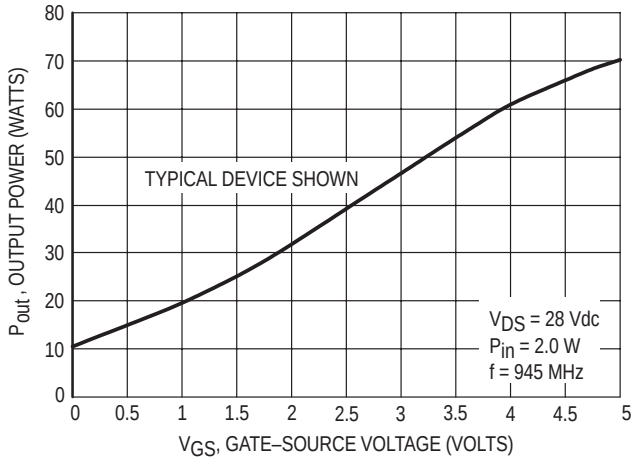


Figure 7. Output Power versus Gate Voltage

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TYPICAL CHARACTERISTICS

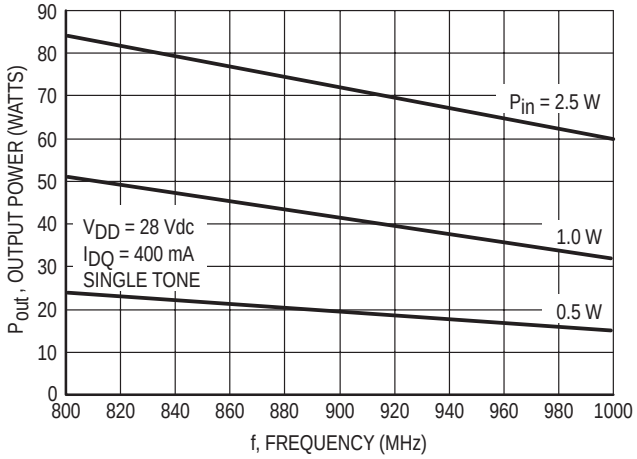


Figure 8. Output Power versus Frequency

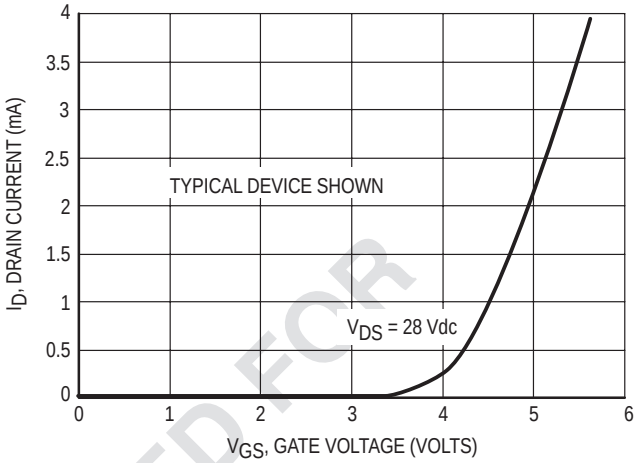


Figure 9. Drain Current versus Gate Voltage

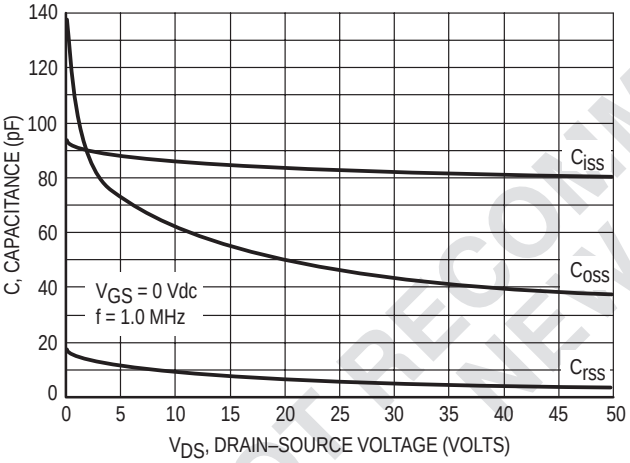


Figure 10. Capacitance versus Voltage

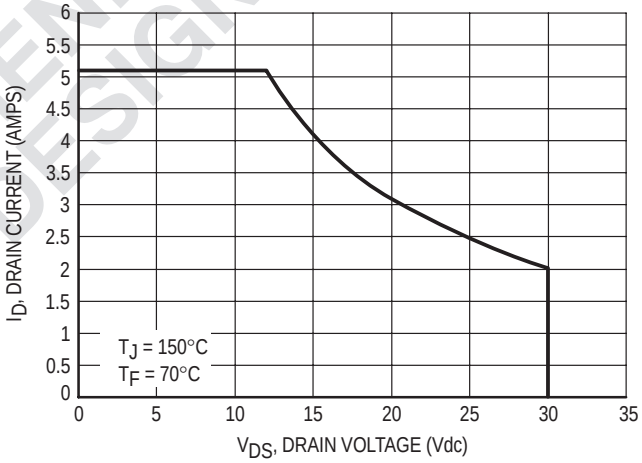


Figure 11. DC Safe Operating Area

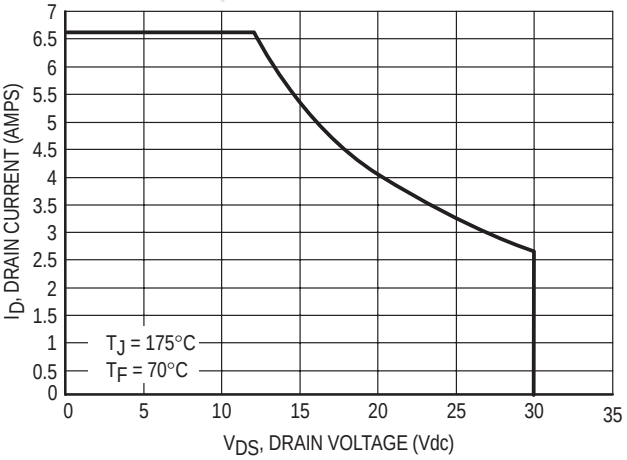


Figure 12. DC Safe Operating Area

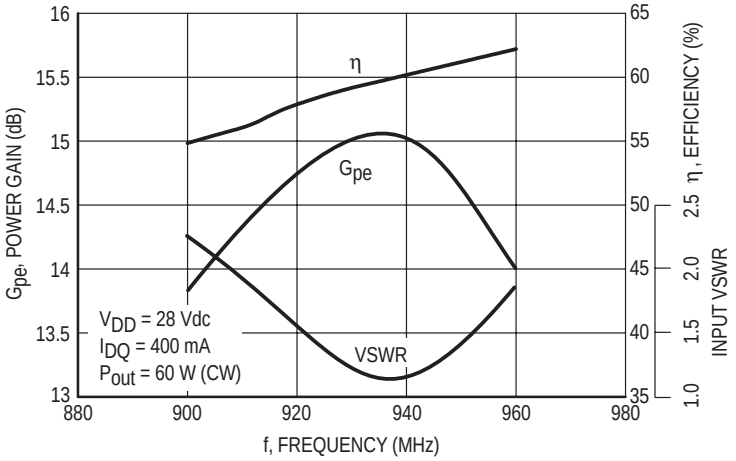


Figure 13. Performance in Broadband Circuit

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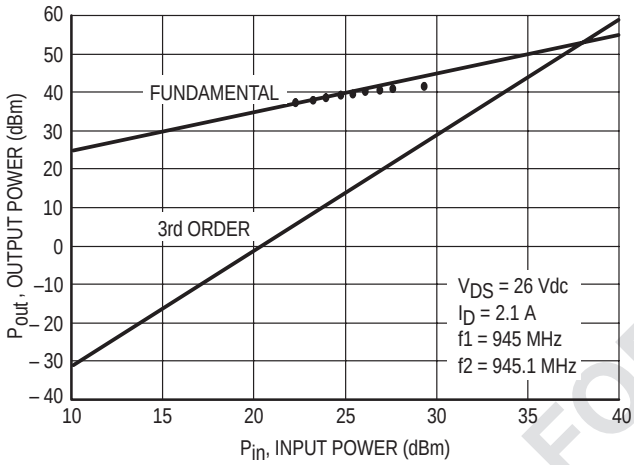
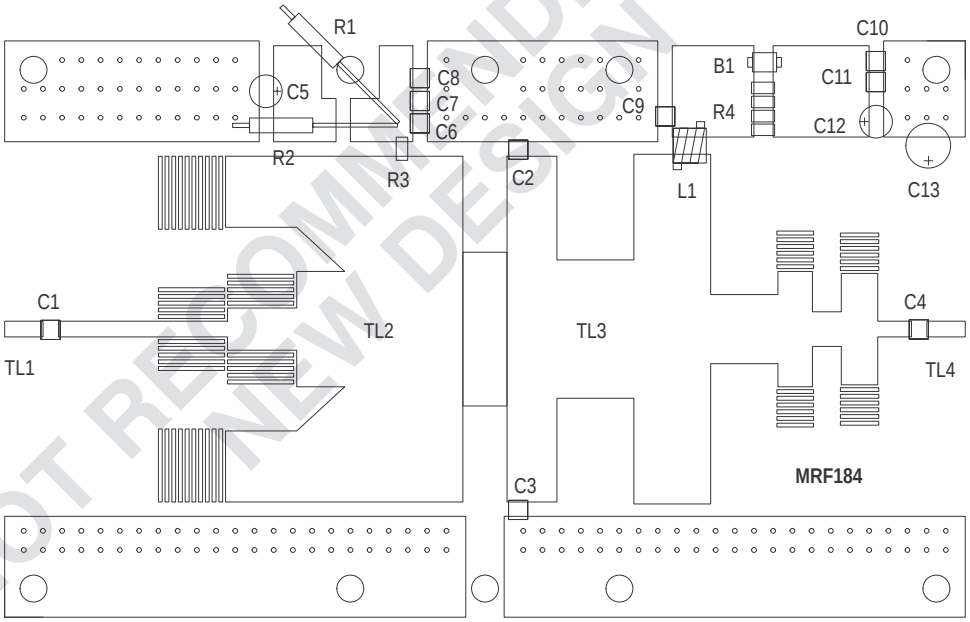
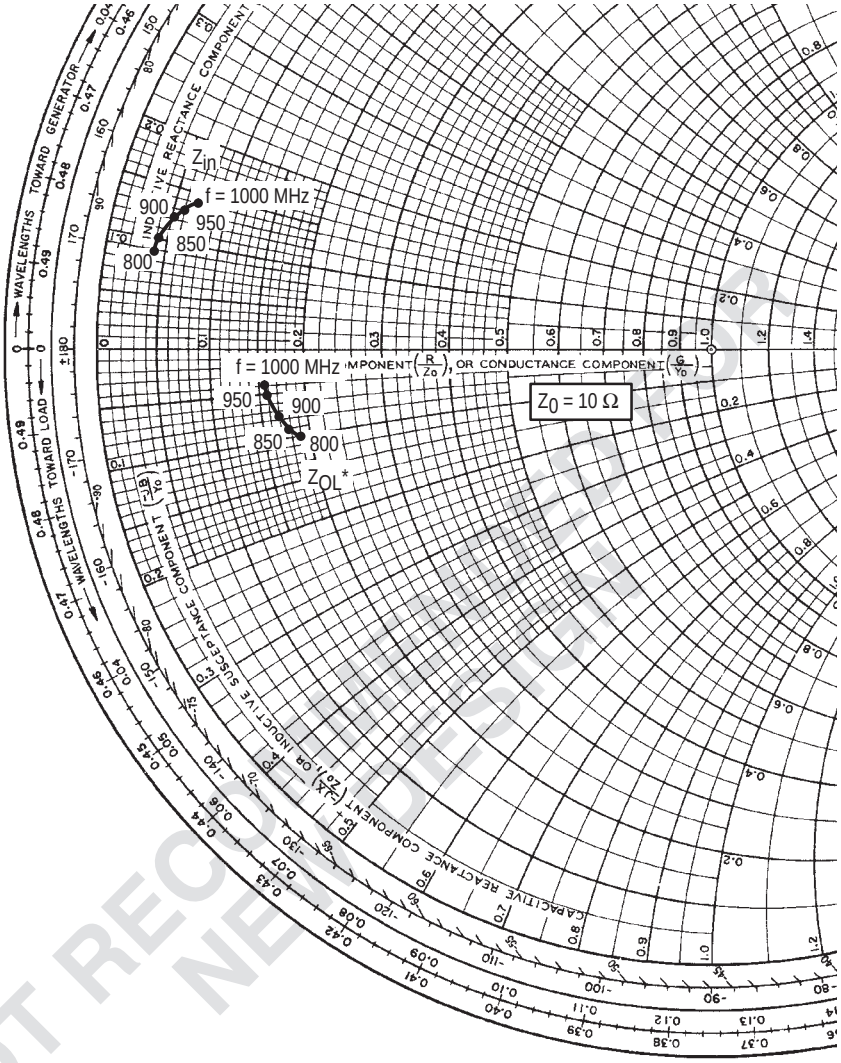


Figure 14. Class A Third Order Intercept Point



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Figure 15. Component Parts Layout



NOT RECOMMENDED FOR NEW DESIGN

V_{DD} = 28 Vdc, I_{DQ} = 100 mA, P_{out} = 60 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	0.40 + j0.90	1.85 – j1.00
850	0.45 + j1.10	1.75 – j0.90
900	0.52 + j1.20	1.70 – j0.75
950	0.60 + j1.30	1.60 – j0.50
1000	0.70 + j1.38	1.57 – j0.40

Z_{in} = Conjugate of source impedance.

Z_{out} = Conjugate of the load impedance at given output power, voltage, frequency and efficiency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, drain efficiency and device stability.

Figure 16. Series Equivalent Input and Output Impedance

Table 1. Common Source S–Parameters (V_{DS} = 13.5 V)

I_D = 2.0 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
20	0.916	179	10.88	80	0.014	–22	0.843	175
30	0.917	178	9.26	79	0.014	–25	0.847	174
40	0.918	177	8.10	78	0.015	–29	0.852	174
50	0.919	176	7.16	77	0.015	–33	0.853	174
100	0.919	175	4.57	75	0.015	–35	0.855	173
150	0.920	174	3.34	67	0.015	–38	0.865	173
200	0.921	173	2.60	62	0.014	–41	0.867	173
250	0.922	173	2.11	59	0.014	–45	0.877	173
300	0.928	172	1.77	55	0.014	–49	0.881	173
350	0.938	172	1.50	50	0.013	–55	0.887	173
400	0.941	171	1.28	47	0.013	–59	0.895	173
450	0.942	171	1.12	44	0.012	–62	0.896	173
500	0.943	171	1.00	41	0.012	–68	0.898	172
550	0.945	171	0.91	38	0.010	–75	0.899	172
600	0.947	171	0.80	35	0.010	–79	0.903	172
650	0.948	171	0.71	33	0.009	–85	0.905	172
700	0.955	170	0.65	30	0.008	–88	0.909	172
750	0.959	170	0.60	28	0.008	–95	0.919	172
800	0.962	169	0.55	25	0.007	–102	0.922	172
850	0.963	169	0.50	23	0.007	–111	0.923	171
900	0.964	169	0.45	21	0.007	–118	0.926	171
950	0.968	169	0.43	19	0.006	–125	0.929	171
1000	0.970	169	0.39	18	0.006	–129	0.933	171
1050	0.971	168	0.36	17	0.005	–134	0.935	171
1100	0.972	168	0.34	14	0.005	–142	0.936	170
1150	0.973	168	0.32	13	0.005	–149	0.938	170
1200	0.974	167	0.29	12	0.006	–156	0.940	169
1250	0.976	167	0.28	10	0.007	–162	0.943	169
1300	0.975	167	0.26	9	0.008	–173	0.945	168
1350	0.972	166	0.25	8	0.009	–178	0.946	167
1400	0.969	166	0.24	7	0.011	175	0.947	167
1450	0.965	165	0.22	6	0.012	172	0.948	167
1500	0.959	164	0.21	5	0.013	169	0.950	167

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Table 2. Common Source S–Parameters (V_{DS} = 28 V)

I_D = 2.0 A

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
20	0.912	–170	16.01	84	0.016	–12	0.746	178
30	0.917	–173	13.73	82	0.015	–15	0.755	177
40	0.918	–174	12.02	80	0.014	–17	0.759	177
50	0.919	–176	10.62	78	0.013	–20	0.766	176
100	0.922	–178	6.76	71	0.012	–22	0.775	176
150	0.930	177	4.92	65	0.011	–25	0.791	176
200	0.931	176	3.82	60	0.010	–27	0.791	176
250	0.933	175	3.07	55	0.009	–29	0.793	176
300	0.941	174	2.53	51	0.009	–31	0.826	176
350	0.943	173	2.14	45	0.008	–35	0.834	176
400	0.945	172	1.83	41	0.008	–45	0.853	176
450	0.948	172	1.58	38	0.007	–52	0.858	176
500	0.950	172	1.39	35	0.007	–57	0.865	176
550	0.955	172	1.24	32	0.007	–61	0.876	176
600	0.960	172	1.10	29	0.006	–64	0.882	176
650	0.965	171	0.96	26	0.006	–68	0.888	175
700	0.967	171	0.89	24	0.006	–71	0.894	175
750	0.970	171	0.80	20	0.005	–73	0.904	175
800	0.973	170	0.73	18	0.005	–78	0.906	175
850	0.974	169	0.66	17	0.004	–83	0.908	174
900	0.975	169	0.61	13	0.004	–91	0.909	173
950	0.976	169	0.57	12	0.004	–94	0.915	173
1000	0.978	168	0.52	11	0.004	–96	0.916	173
1050	0.979	168	0.47	9	0.005	–102	0.919	172
1100	0.980	168	0.43	7	0.005	–115	0.924	172
1150	0.980	167	0.41	6	0.006	–119	0.931	171
1200	0.979	167	0.38	5	0.006	–125	0.934	170
1250	0.978	167	0.36	2	0.006	–139	0.935	170
1300	0.974	167	0.34	1	0.007	–148	0.936	170
1350	0.971	166	0.32	0	0.007	–156	0.937	169
1400	0.970	165	0.31	–1	0.007	–165	0.938	169
1450	0.969	165	0.30	–2	0.008	–171	0.939	169
1500	0.965	164	0.27	–3	0.008	–178	0.946	169

NOT RECOMMENDED FOR NEW DESIGN

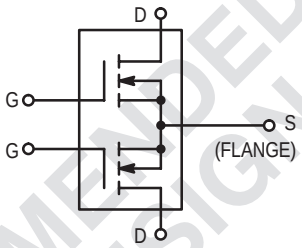
Product Is Not Recommended for New Design.
The next generation of higher performance products are in development. Visit our online Selector Guides (http://mot–sps.com/rf/sg/sg.html) for scheduled introduction dates.

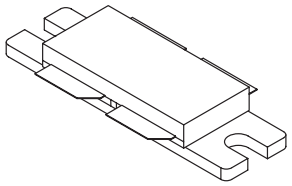
MRF185

The RF MOSFET Line
RF POWER
Field-Effect Transistor
N–Channel Enhancement–Mode Lateral MOSFET

85 WATTS, 1.0 GHz
28 VOLTS
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET

- High Gain, Rugged Device
- Broadband Performance from HF to 1 GHz
- Bottom Side Source Eliminates DC Isolators, Reducing Common Mode Inductances





CASE 375B–02, STYLE 2

NOT RECOMMENDED FOR NEW DESIGN

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.45	Watts W/°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 V, I_D = 1 μAdc)	$V_{(BR)DSS}$	65	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	–	–	1	μAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0 V)	I_{GSS}	–	–	1	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Quiescent Voltage (V_{DS} = 26 V, I_D = 300 mA per side)	$V_{GS(Q)}$	3	4	5	Vdc
Delta Quiescent Voltage between sides (V_{DS} = 26 V, I_D = 300 mA per side)	$\Delta V_{GS(Q)}$	–	0.15	0.3	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3 A per side)	$V_{DS(on)}$	–	0.75	1	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3 A per side)	g_{fs}	1.6	2	–	s
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1 MHz)	C_{oss}	–	38	–	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1 MHz)	C_{rss}	–	4.6	6	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 85 W, f = 960 MHz, I_{DQ} = 600 mA)	G_{ps}	11	14	–	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 85 W, f = 960 MHz, I_{DQ} = 600 mA)	η	45	53	–	%
Load Mismatch (V_{DD} = 28 Vdc, P_{out} = 85 W, f = 960 MHz, I_{DQ} = 600 mA, Load VSWR 5:1 at All Phase Angles)	Ψ	No Degradation in Output Power			

NOT RECOMMENDED FOR NEW DESIGN

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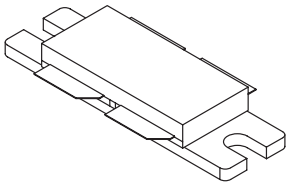
MRF186

The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode Lateral MOSFET

120 W, 1.0 GHz, 28 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET

Designed for broadband commercial and industrial applications at frequencies from 800 MHz to 1.0 GHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 28 volt base station equipment.

- Guaranteed Performance @ 960 MHz, 28 Volts
  Output Power — 120 Watts (PEP)
  Power Gain — 11 dB
  Efficiency — 30%
  Intermodulation Distortion — –28 dBc
- Excellent Thermal Stability
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 28 Vdc, 960 MHz, 120 Watts CW



CASE 375B–02, STYLE 2

NOT RECOMMENDED FOR NEW DESIGN

MAXIMUM RATINGS (2)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	14	Adc
Total Device Dissipation @ T_C = 70°C Derate above 70°C	P_D	162.5 1.25	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.8	°C/W

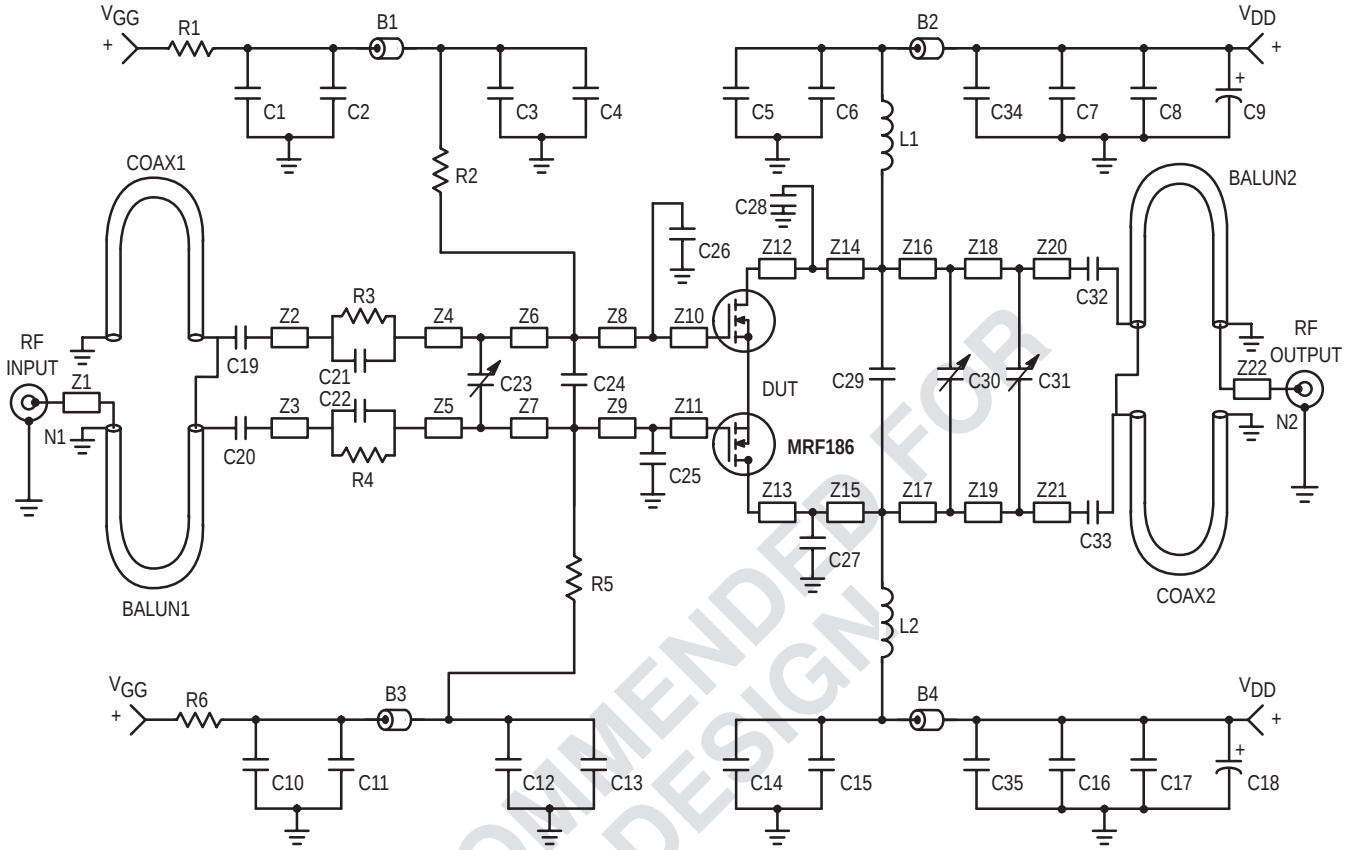
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 50 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (1)					
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 300 μAdc Per Side)	$V_{GS(th)}$	2.5	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 300 mAdc Per Side)	$V_{GS(Q)}$	3.3	4.2	5	Vdc
Delta Gate Threshold Voltage (Side to Side) (V_{DS} = 28 V, I_D = 300 mA Per Side)	$\Delta V_{GS(Q)}$	—	—	0.3	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 3 Adc Per Side)	$V_{DS(on)}$	—	0.58	0.7	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc Per Side)	g_{fs}	2.4	2.8	—	S
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (Per Side) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	177	—	pF
Output Capacitance (Per Side) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	45	—	pF
Reverse Transfer Capacitance (Per Side) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	3.4	—	pF
FUNCTIONAL CHARACTERISTICS (In Motorola Test Fixture) **(2)**					
Two–Tone Common Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 400 mA, f1 = 960.0 MHz, f2 = 960.1 MHz)	G_{ps}	11	12.2	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 400 mA, f1 = 960.0 MHz, f2 = 960.1 MHz)	η	30	35	—	%
3rd Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 400 mA, f1 = 960.0 MHz, f2 = 960.1 MHz)	IMD	—	–32	–28	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 400 mA, f1 = 960.0 MHz, f2 = 960.1 MHz)	IRL	9	16	—	dB
Two–Tone Common Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 400 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	G_{ps}	—	12	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 400 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	η	—	33	—	%
3rd Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 400 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IMD	—	–32	—	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 400 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IRL	—	16	—	dB
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 x 400 mA, f = 960 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Each side of device measured separately.
(2) Device measured in push–pull configuration.

NOT RECOMMENDED FOR NEW DESIGN



NOT RECOMMENDED FOR NEW DESIGN

B1 – B4	Fair Rite Products Short Ferrit Bead, 2743021446
C1, C7, C8, C10, C16, C17	10 μF, 50 V, Tantalum
C2, C11, C34, C35	0.1 μF, Chip Capacitor
C3, C6, C12, C15	330 pF, Chip Capacitor
C4, C5, C13, C14, C19, C20, C32, C33	47 pF, Chip Capacitor
C9, C18	250 μF, 50 V, Electrolytic Capacitor
C21, C22	12 pF, Chip Capacitor
C23, C30	0.6 – 4.5 pF, Variable Capacitor, Johanson Gigatrim
C24, C25, C26	5.1 pF, Chip Capacitor
C27, C28	3.9 pF, Chip Capacitor
C31	0.8 – 8.0 pF, Variable Capacitor, Johanson Gigatrim
L1, L2	3 Turns, #20 AWG, IDIA 0.126″, 24.7 nH
N1, N2	Type N Connectors
R1, R6	1 kΩ, 1/4 W, Carbon Resistor
R2, R5	1.2 kΩ, 0.1 W, Chip Resistor
R3, R4	75 Ω, 0.1 W, Chip Resistor
Z1 – Z22	Microstrip (See Component Placement)
Balun1, Balun2, Coax1, Coax2	2.20″ 50 Ω, 0.086″ OD Semi–Rigid Coax
Board	1/32″ Glass Teflon®, ε_r = 2.55

Figure 1. 930 – 960 MHz Test Circuit Schematic

TYPICAL CHARACTERISTICS

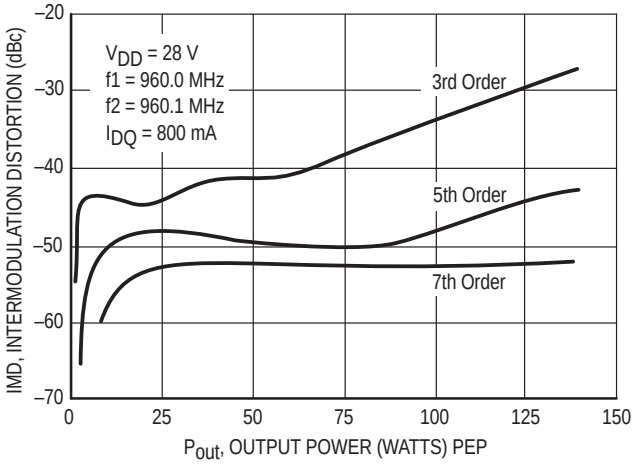


Figure 2. Intermodulation Distortion Products versus Output Power

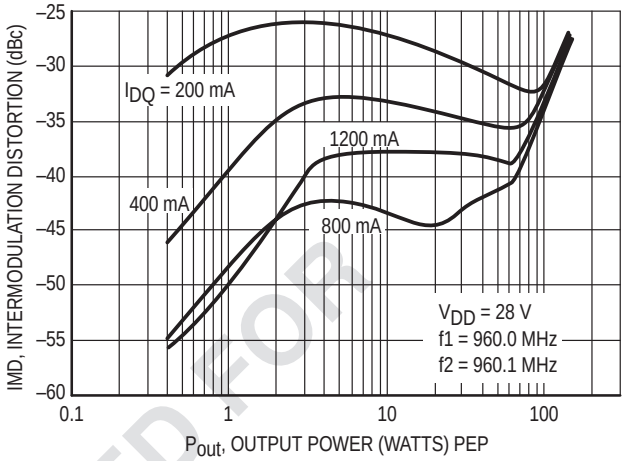


Figure 3. Intermodulation Distortion versus Output Power

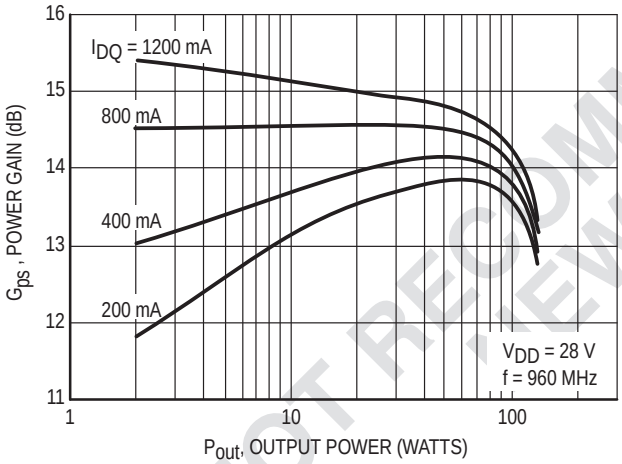


Figure 4. Power Gain versus Output Power

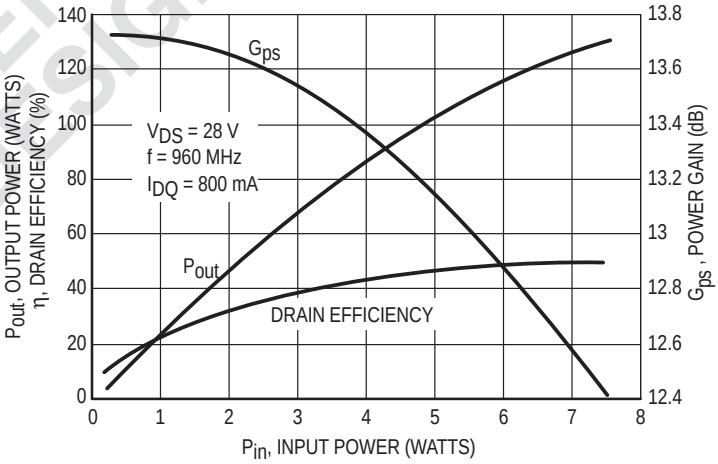


Figure 5. Output Power versus Input Power

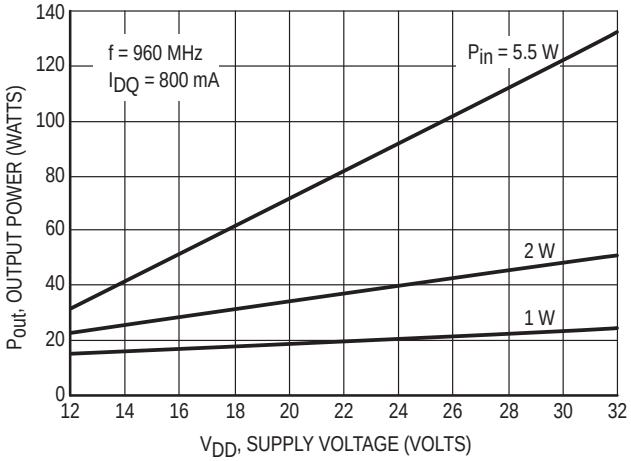


Figure 6. Output Power versus Supply Voltage

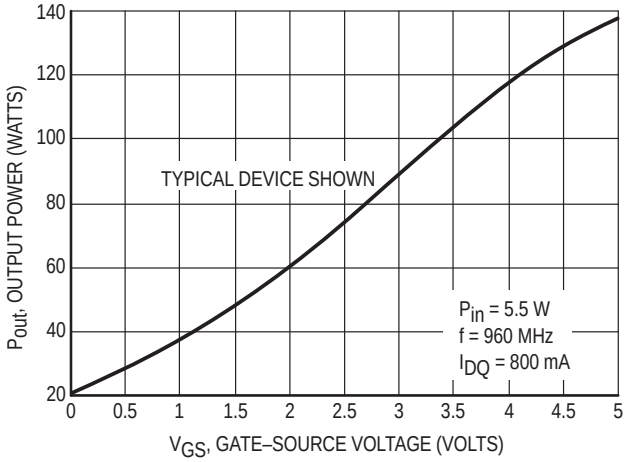


Figure 7. Output Power versus Gate Voltage

NOT RECOMMENDED FOR NEW DESIGN

TYPICAL CHARACTERISTICS

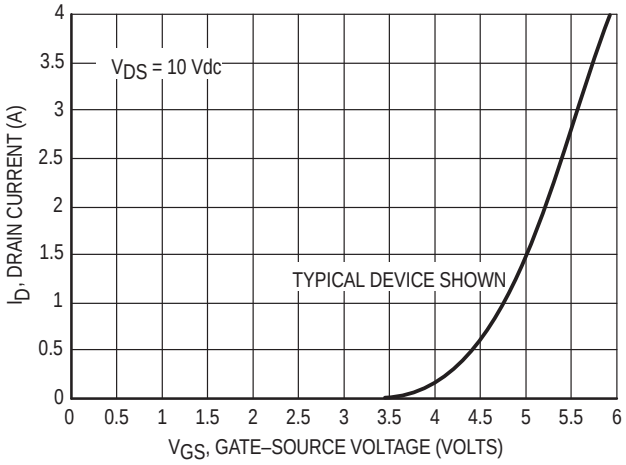


Figure 8. Drain Current versus Gate Voltage

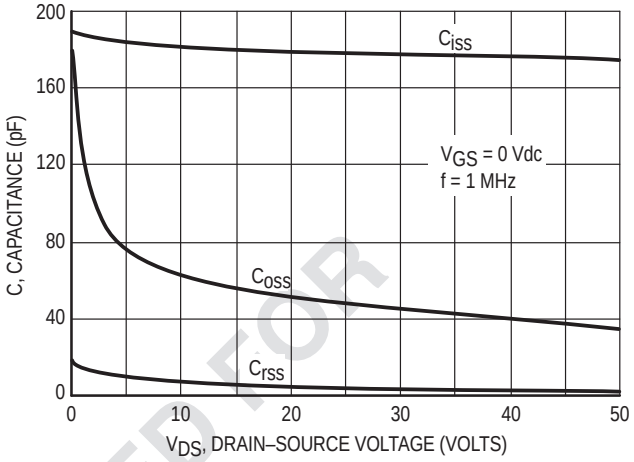


Figure 9. Capacitance versus Voltage

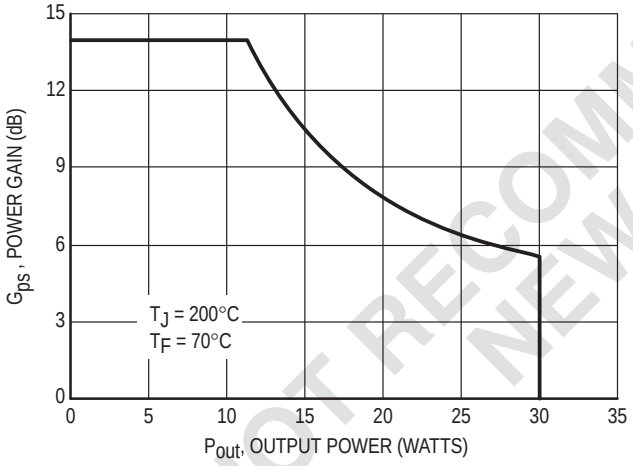


Figure 10. DC Safe Operating Area

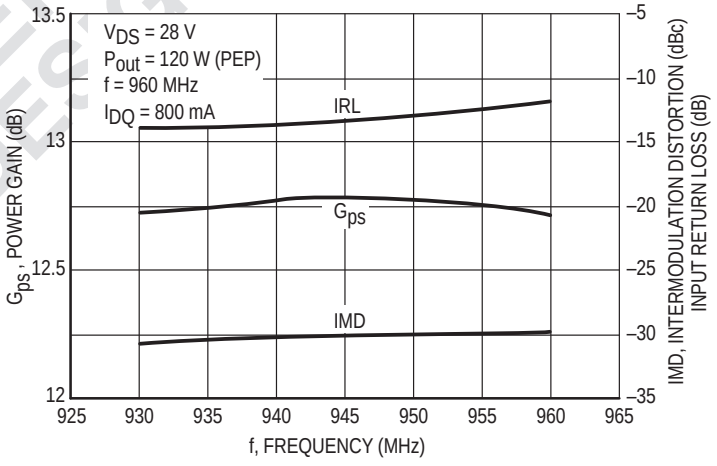
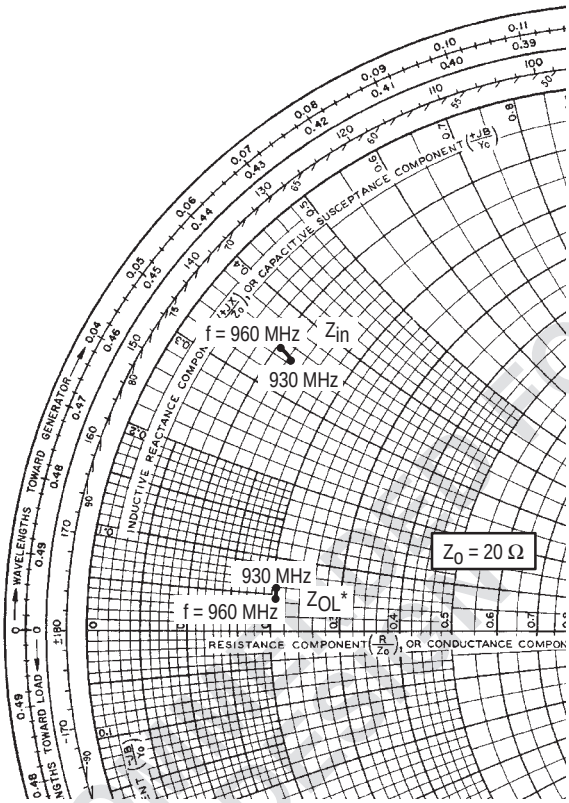


Figure 11. Broadband Circuit Performance

NOT RECOMMENDED FOR NEW DESIGN



V_{CC} = 28 V, I_{DQ} = 2 × 400 mA, P_{out} = 120 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
930	2.5 + j6.9	4.3 + j1.2
945	2.5 + j7.0	4.3 + j1.0
960	2.2 + j7.1	4.3 + j0.9

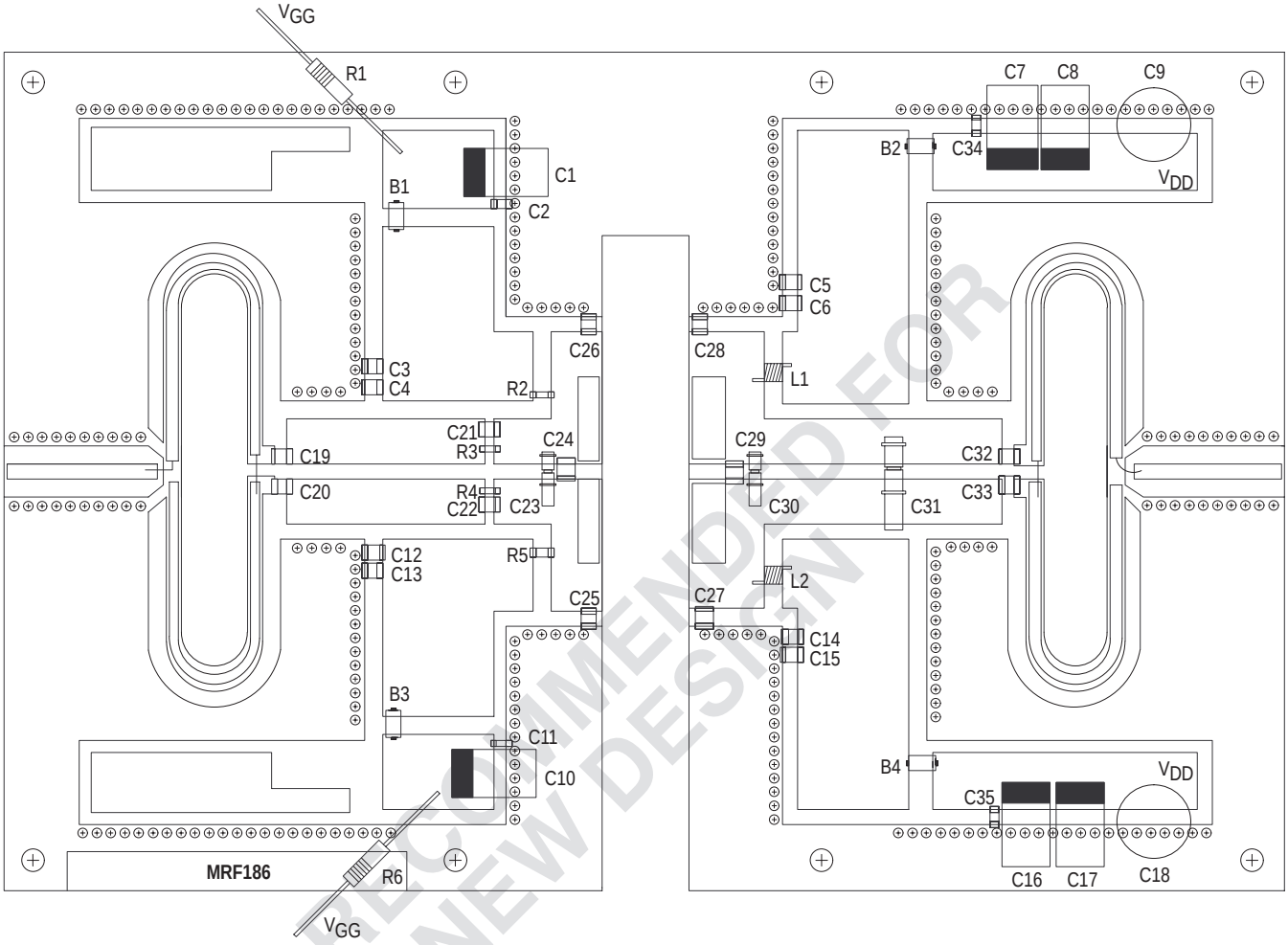
Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current, efficiency and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation performance. Impedances shown represent a single channel (1/2 of MRF186) impedance measurement.

Figure 12. Series Equivalent Input and Output Impedance

NOT RECOMMENDED FOR NEW DESIGN



NOT RECOMMENDED FOR NEW DESIGN

Figure 13. Component Placement Diagram of 930 – 960 MHz Broadband Test Fixture

Product Is Not Recommended for New Design.
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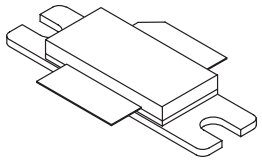
MRF187
MRF187S

The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

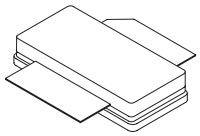
85 W, 1.0 GHz, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

Designed for broadband commercial and industrial applications at frequencies up to 1.0 GHz. The high gain and broadband performance of these devices makes them ideal for large–signal, common source amplifier applications in 26 volt base station equipment.

- Guaranteed Performance @ 880 MHz, 26 Volts
  Output Power — 85 Watts (PEP)
  Power Gain — 12 dB
  Efficiency — 30%
  Intermodulation Distortion — –28 dBc
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 26 Vdc, 880 MHz, 85 Watts CW
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 465–04, STYLE 1
(MRF187)



CASE 465A–04, STYLE 1
(MRF187S)

NOT RECOMMENDED FOR NEW DESIGN

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	15	Adc
Total Device Dissipation @ $T_C \geq 25°C$ Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

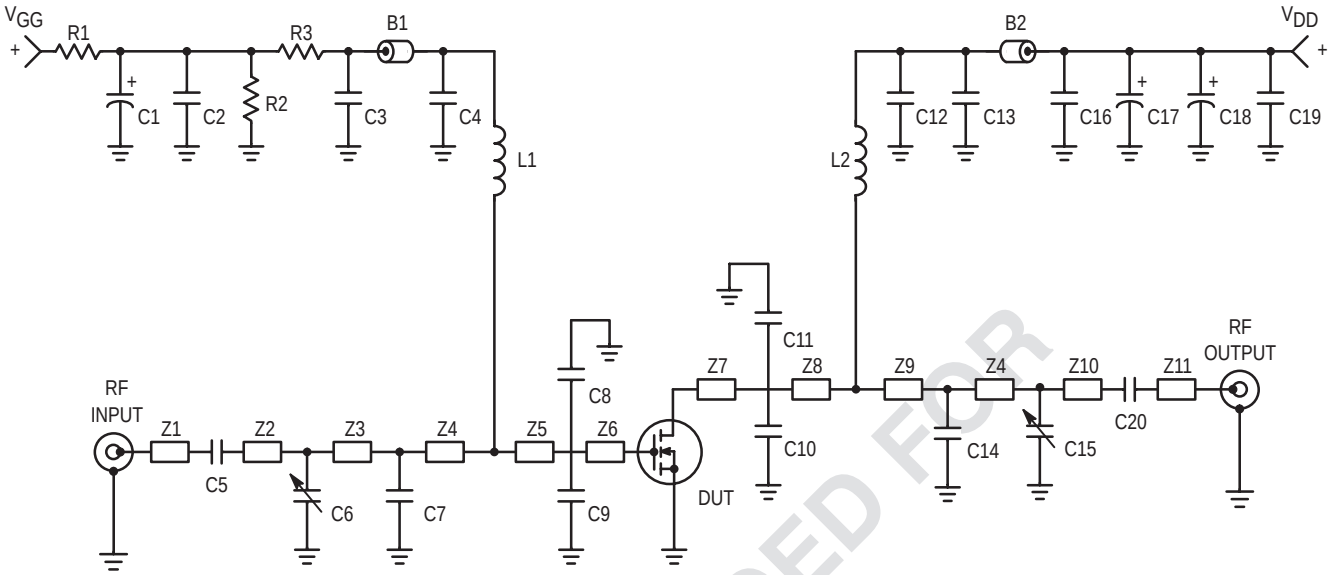
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 50 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 550 mAdc)	$V_{GS(Q)}$	3	—	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 3 Adc)	$V_{DS(on)}$	—	0.40	0.55	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 5 Adc)	g_{fs}	—	2	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Includes Internal Input MOScap) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	295	—	pF
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	85	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	10	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	G_{ps}	12	13	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	η_D	30	33	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	IRL	9	15	—	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 865.0 MHz, f2 = 865.1 MHz and f1 = 895.0 MHz, f2 = 895.1 MHz)	G_{ps}	—	13	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 865.0 MHz, f2 = 865.1 MHz and f1 = 895.0 MHz, f2 = 895.1 MHz)	η_D	—	33	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 865.0 MHz, f2 = 865.1 MHz and f1 = 895.0 MHz, f2 = 895.1 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 865.0 MHz, f2 = 865.1 MHz and f1 = 895.0 MHz, f2 = 895.1 MHz)	IRL	—	12	—	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 85 W CW, I_{DQ} = 550 mA, f = 880 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

NOT RECOMMENDED FOR NEW DESIGN



B1 – B2	Ferrite Bead, Fair Rite, 2743019447	L1, L2	5 Turns, #24 AWG, 0.059″ OD
C1	10 μF, 50 V, Electrolytic Capacitor, ECEV1HV100R Panasonic	R1	12 Ω, 1/4 Watt Carbon
C2, C16	0.10 μF, B Case Chip Capacitors, CDR33BX104AKWS, Kemet	R2	4.7 MΩ, 1/4 Watt Carbon
C3	20000 pF, B Case Chip Capacitor, 200B203MCA50X, ATC	R3	16 kΩ, 1/4 Watt Carbon
C4, C13	100 pF, B Case Chip Capacitors, 100B101JCA500X, ATC	Z1, Z11	0.150″ x 0.220″ Microstrip
C5, C20	47 pF, B Case Chip Capacitors, 100B470JCA500X, ATC	Z2, Z10	0.410″ x 0.220″ Microstrip
C6, C15	0.8 – 8.0 pF, Variable Capacitors, Johanson Gigatrim	Z3	0.160″ x 0.630″ Microstrip
C7	4.7 pF, B Case Chip Capacitor, 100B4R7JCA500X, ATC	Z4	0.160″ x 0.630″ Microstrip
C8, C9	10 pF, B Case Chip Capacitors, 100B100JCA500X, ATC	Z5	0.098″ x 0.630″ Microstrip
C10, C11	16 pF, B Case Chip Capacitors, 100B160JCA500X, ATC	Z6	0.098″ x 0.630″ Microstrip
C12	43 pF, B Case Chip Capacitor, 100B430JCA500X, ATC	Z7	0.210″ x 0.220″ Microstrip
C14	7.5 pF, B Case Chip Capacitor, 100B7R5JCA500X, ATC	Z8	0.050″ x 0.220″ Microstrip
C17, C18, C19	10 μF, 35 V, Electrolytic Capacitors, SMT, Kemet		

Figure 1. MRF187 Schematic

NOT RECOMMENDED FOR NEW DESIGN

TYPICAL CHARACTERISTICS

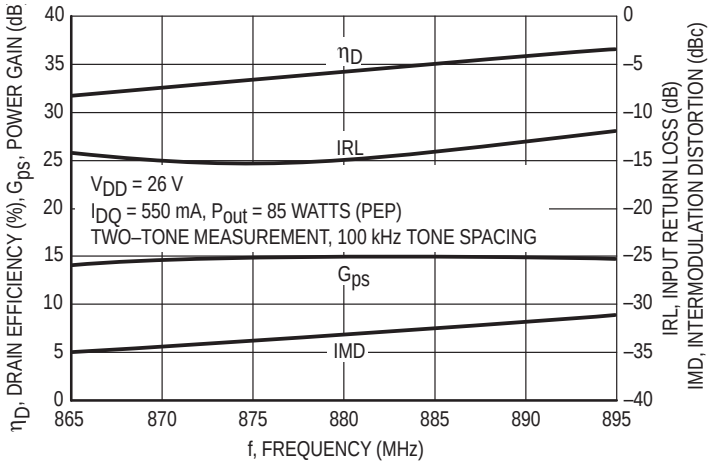


Figure 2. Class AB Broadband Circuit Performance

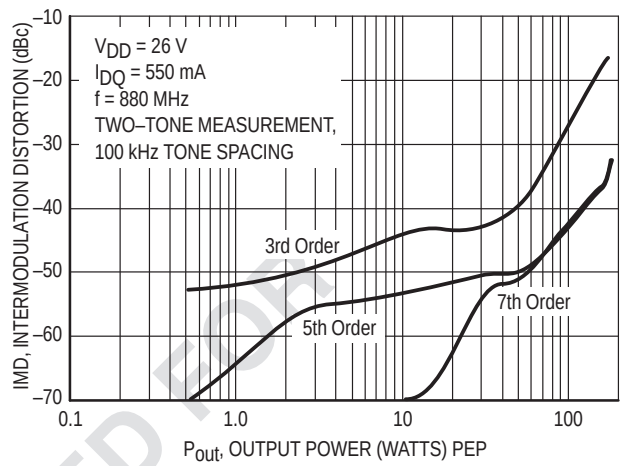


Figure 3. Intermodulation Distortion Products versus Output Power

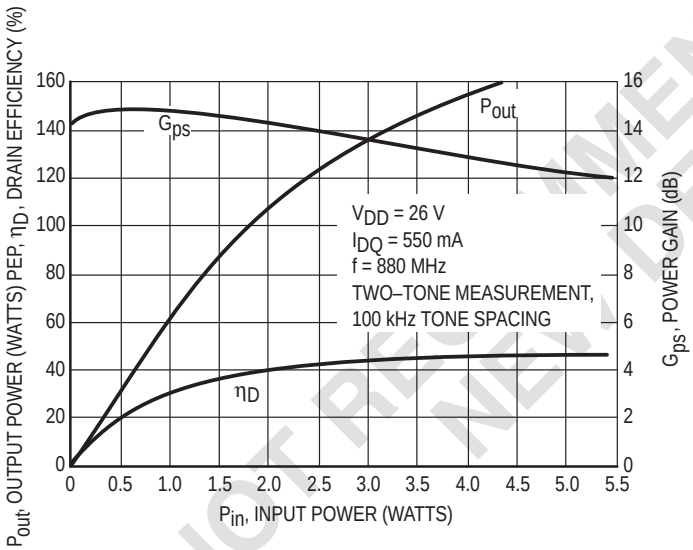


Figure 4. Class AB Parameters versus Input Power

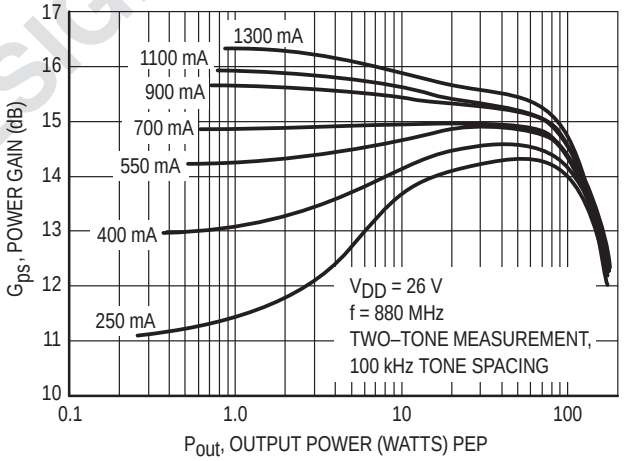


Figure 5. Power Gain versus Output Power

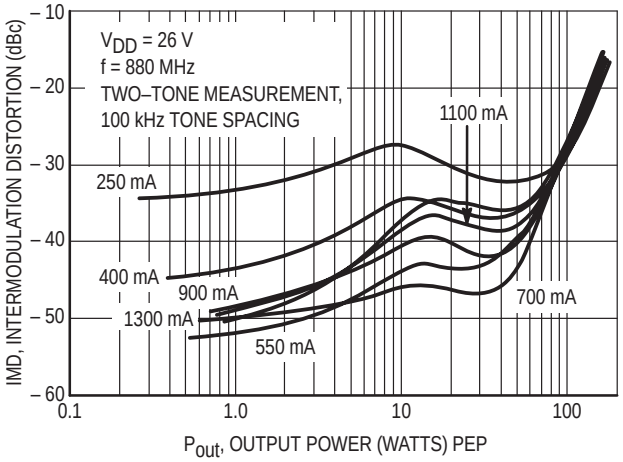
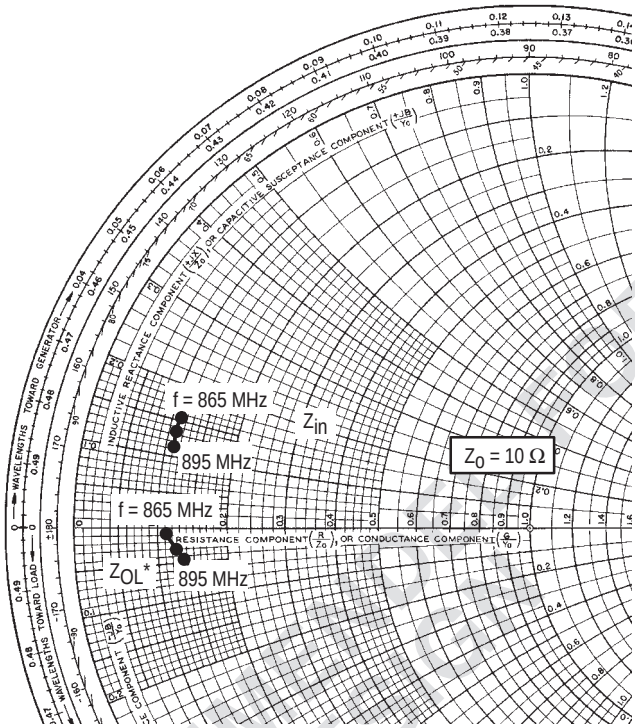


Figure 6. Intermodulation Distortion versus Output Power

NOT RECOMMENDED FOR NEW DESIGN



V_{CC} = 26 V, I_{DQ} = 550 mA, P_{out} = 85 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
865	1.04 + j1.51	1.13 – j0.091
880	1.03 + j1.39	1.20 – j0.176
895	1.03 + j1.29	1.28 – j0.242

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

Figure 7. Series Equivalent Input and Output Impedance

NOT RECOMMENDED FOR NEW DESIGN

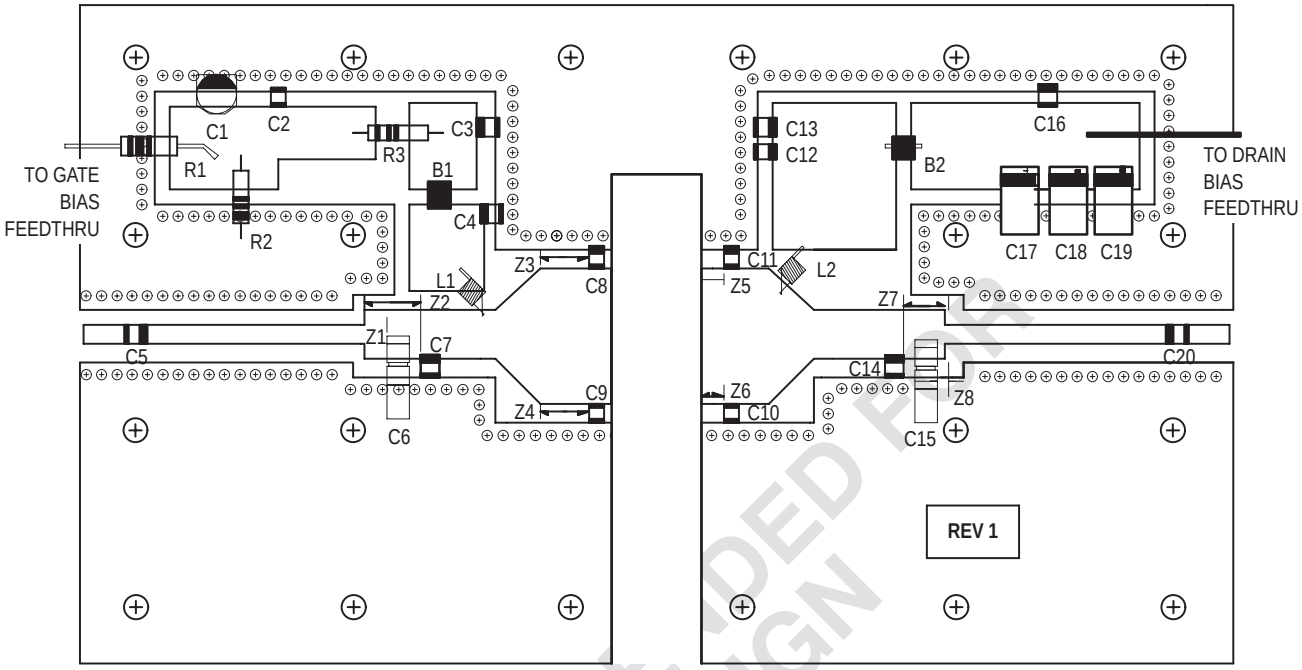


Figure 8. MRF187 Populated PC Board Layout Diagram

NOT RECOMMENDED FOR NEW DESIGN

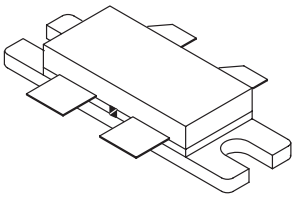
The RF MOSFET Line
Power Field-Effect Transistor
N–Channel Enhancement–Mode

MRF275G

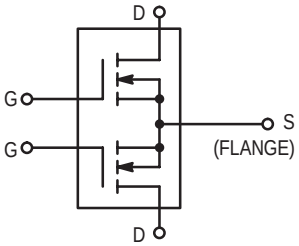
150 W, 28 V, 500 MHz
N–CHANNEL MOS
BROADBAND
100 – 500 MHz
RF POWER FET

Designed primarily for wideband large–signal output and driver stages from 100 – 500 MHz.

- Guaranteed Performance @ 500 MHz, 28 Vdc
  Output Power — 150 Watts
  Power Gain — 10 dB (Min)
  Efficiency — 50% (Min)
  100% Tested for Load Mismatch at all Phase Angles with VSWR 30:1
- Overall Lower Capacitance @ 28 V
  C_{iss} — 135 pF
  C_{oss} — 140 pF
  C_{rss} — 17 pF
- Simplified AVC, ALC and Modulation



CASE 375–04, STYLE 2



Typical data for power amplifiers in industrial and commercial applications:

- Typical Performance @ 400 MHz, 28 Vdc
  Output Power — 150 Watts
  Power Gain — 12.5 dB
  Efficiency — 60%
- Typical Performance @ 225 MHz, 28 Vdc
  Output Power — 200 Watts
  Power Gain — 15 dB
  Efficiency — 65%
- S–Parameters Available for Download into Frequency Domain Simulators.
  See http://motorola.com/sps/rf/designtds/

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Adc
Drain Current — Continuous	I_D	26	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	400 2.27	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

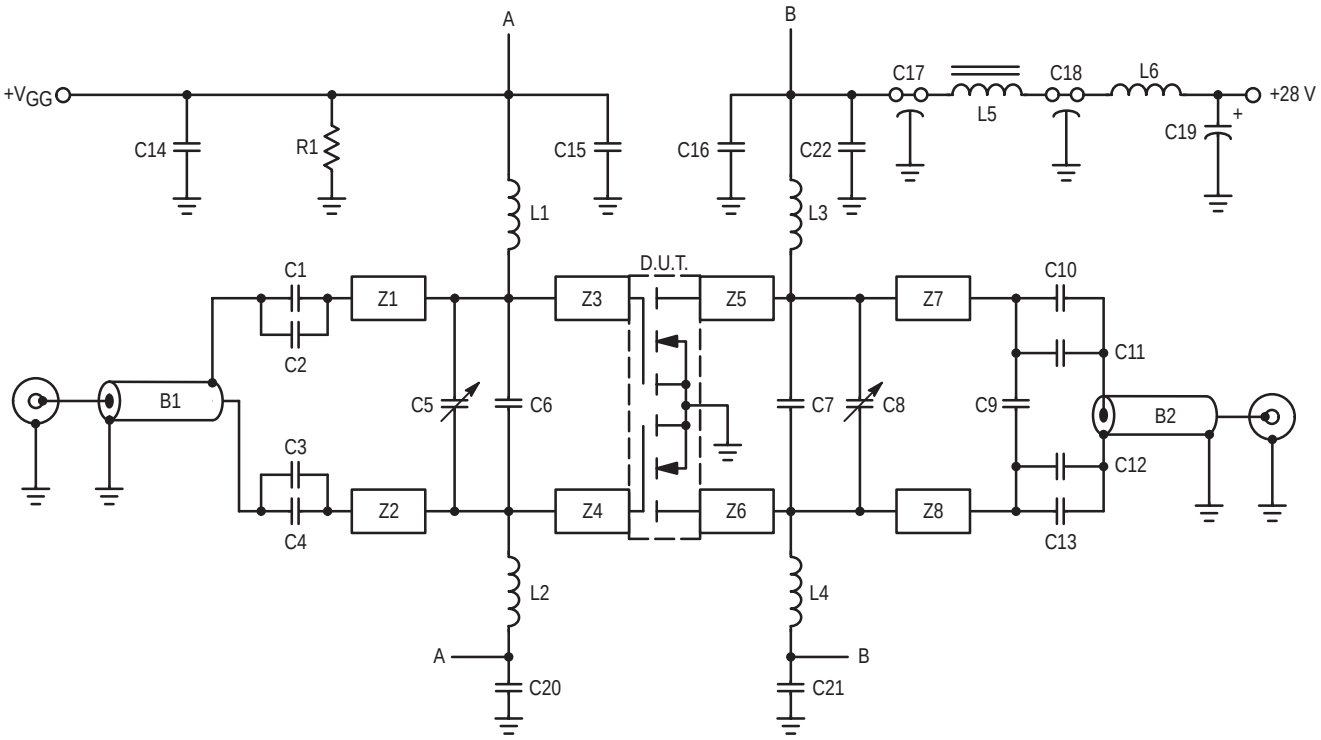
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.44	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	1	mA
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1	μA
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.5	2.5	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 5 A)	$V_{DS(on)}$	0.5	0.9	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	3	3.75	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	135	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	140	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	17	—	pF
FUNCTIONAL CHARACTERISTICS (2) (Figure 1)					
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 150 W, f = 500 MHz, I_{DQ} = 2 x 100 mA)	G_{ps}	10	11.2	—	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 150 W, f = 500 MHz, I_{DQ} = 2 x 100 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 28 V, P_{out} = 150 W, f = 500 MHz, I_{DQ} = 2 x 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

1. Each side of device measured separately.
2. Measured in push–pull configuration.



B1	Balun, 50 Ω, 0.086″ O.D. 2″ Long, Semi Rigid Coax
B2	Balun, 50 Ω, Coax 0.141″ O.D. 2″ Long, Semi Rigid
C1, C2, C3, C4, C10, C11, C12, C13	270 pF, ATC Chip Capacitor
C5, C8	1.0–20 pF, Trimmer Capacitor, Johanson
C6	22 pF, Mini–Unelco Capacitor
C7	15 pF, Unelco Capacitor
C9	2.1 pF, ATC Chip Capacitor
C14, C15, C16, C20, C21, C22	0.1 μF, Ceramic Capacitor
C17, C18	680 pF, Feedthru Capacitor
C19	10 μF, 50 V, Electrolytic Capacitor, Tantalum
L1, L2	10 Turns AWG #24, 0.145″ O.D., 106 nH Taylor–Spring Inductor
L3, L4	10 Turns AWG #18, 0.340″ I.D., Enameled Wire
L5	Ferroxcube VK200 20/4B
L6	4 Turns #16, 0.340″ I.D., Enameled Wire
R1	1.0 kΩ,1/4 W Resistor
W1 – W4	20 x 200 x 250 mils, Wear Pads, Beryllium–Copper, (See Component Location Diagram)
Z1, Z2	1.10″ x 0.245″, Microstrip Line
Z3, Z4, Z5, Z6	0.300″ x 0.245″, Microstrip Line
Z7, Z8	1.00″ x 0.245″, Microstrip Line
Board material	0.060″ Teflon–fiberglass, ε_r = 2.55, copper clad both sides, 2 oz. copper.

Points A are connected together on PCB.
Points B are connected together on PCB.

Figure 1. 500 MHz Test Circuit

TYPICAL CHARACTERISTICS

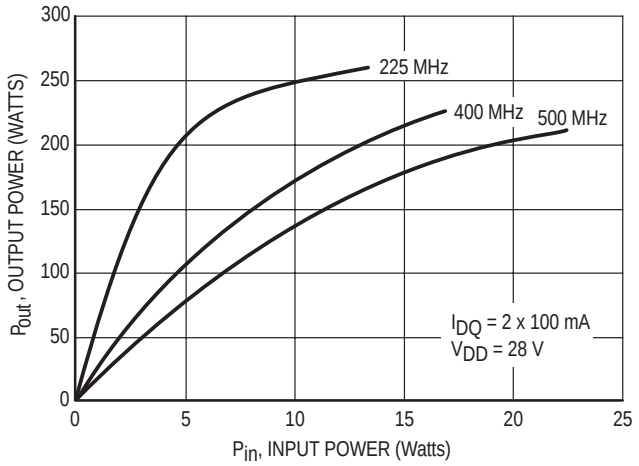


Figure 2. Output Power versus Input Power

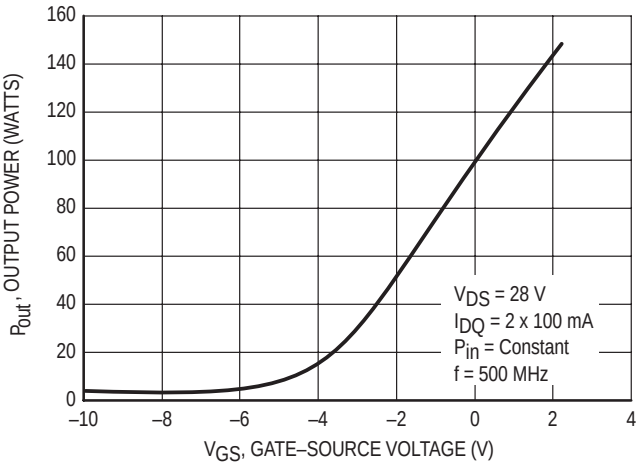


Figure 3. Output Power versus Gate Voltage

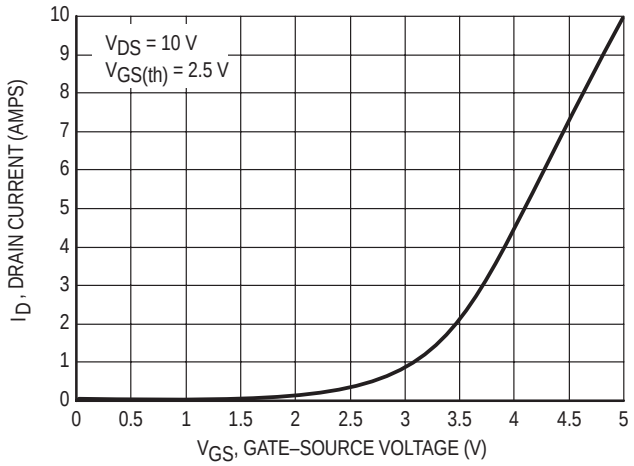


Figure 4. Drain Current versus Gate Voltage (Transfer Characteristics)

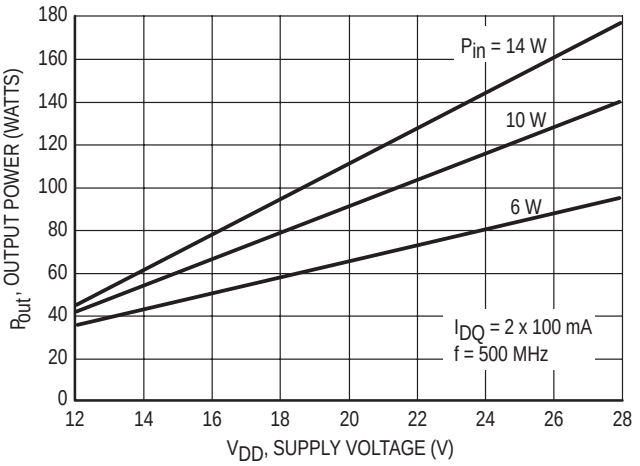


Figure 5. Output Power versus Supply Voltage

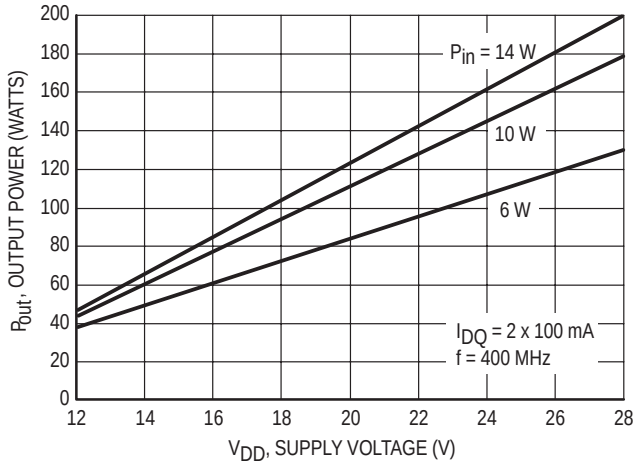


Figure 6. Output Power versus Supply Voltage

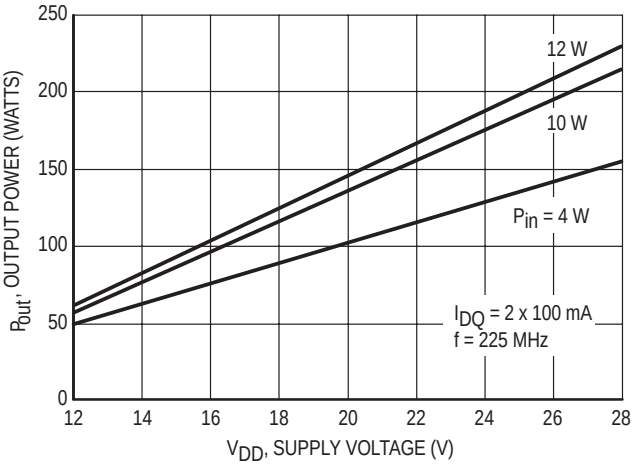


Figure 7. Output Power versus Supply Voltage

TYPICAL CHARACTERISTICS

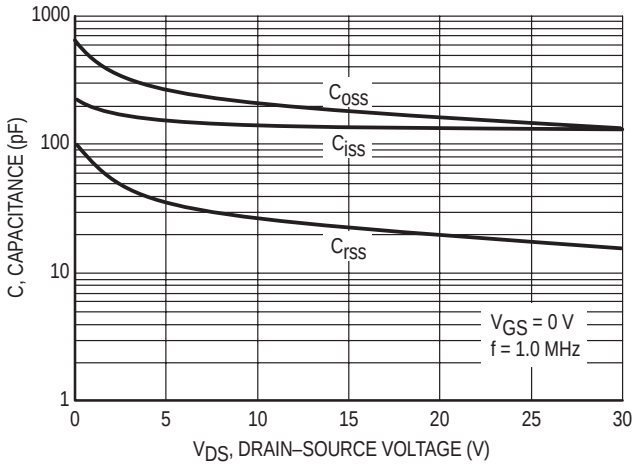


Figure 8. Capacitance versus Drain–Source Voltage*
*Data shown applies only to one half of device, MRF275G

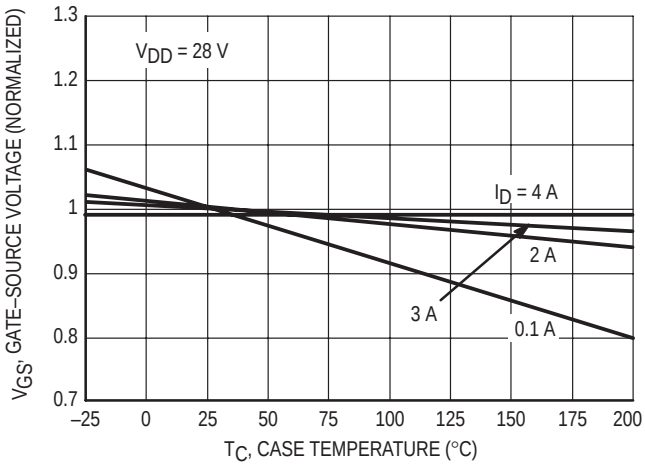


Figure 9. Gate–Source Voltage versus Case Temperature

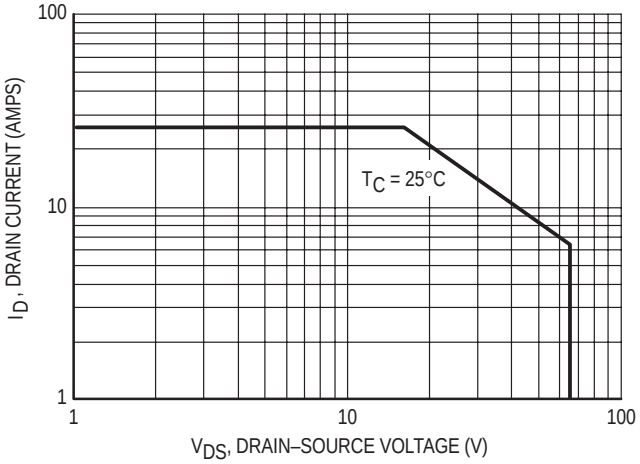
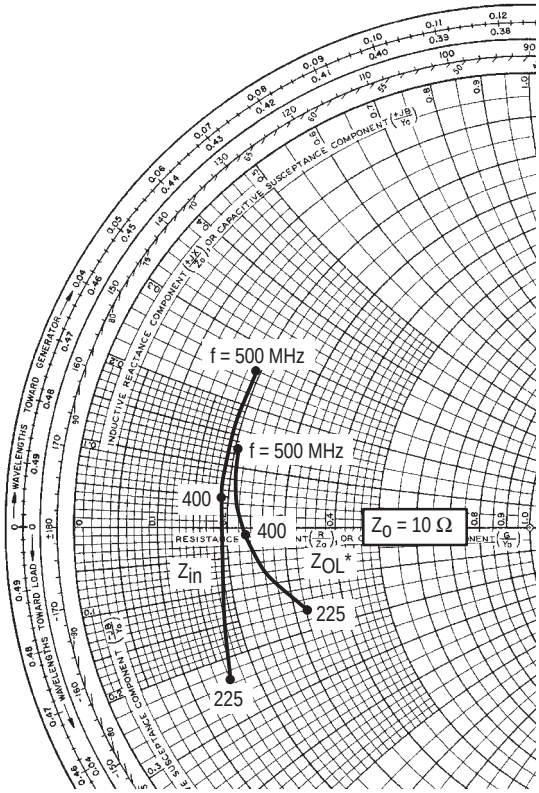


Figure 10. DC Safe Operating Area



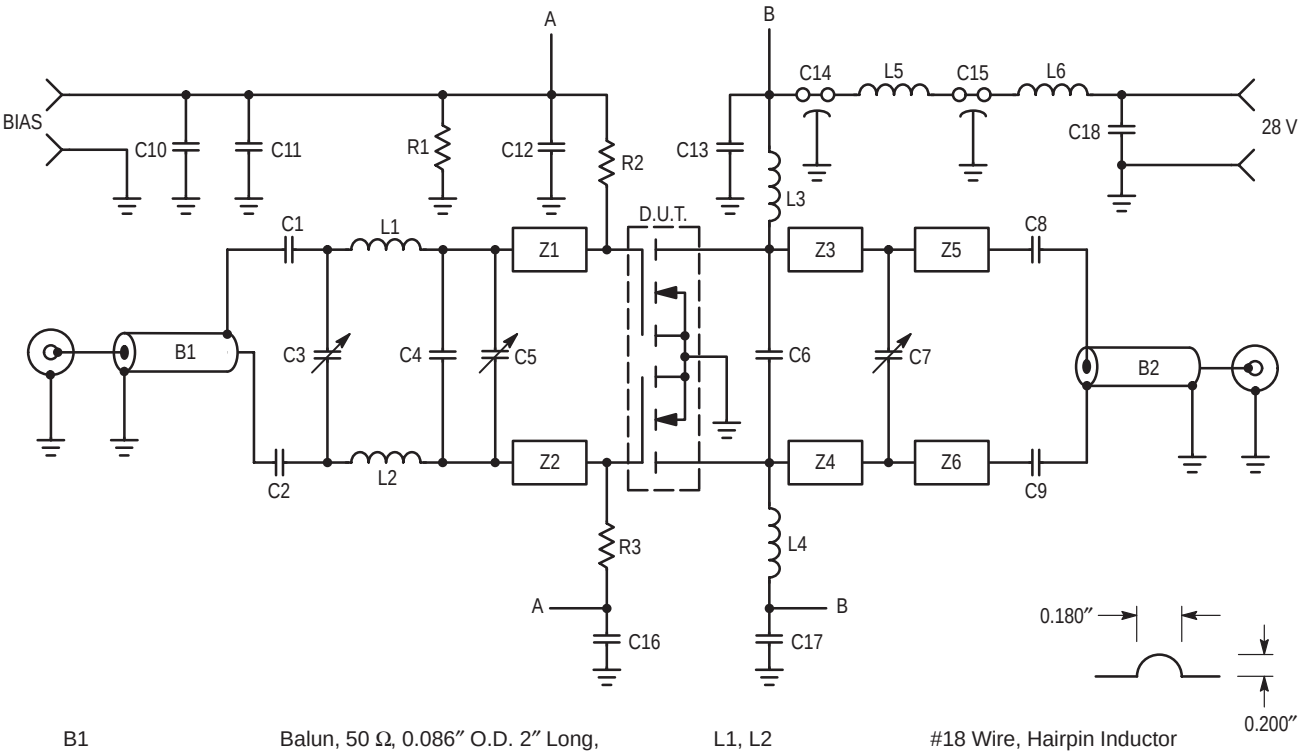
V_{DD} = 28 V, I_{DQ} = 2 x 100 mA, P_{out} = 150 W

f (MHz)	Z_{in} Ohms	Z_{OL}* Ohms
225	1.6 – j2.30	3.2 – j1.50
400	1.9 + j0.48	2.3 – j0.19
500	1.9 + j2.60	2.0 + j1.30

Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

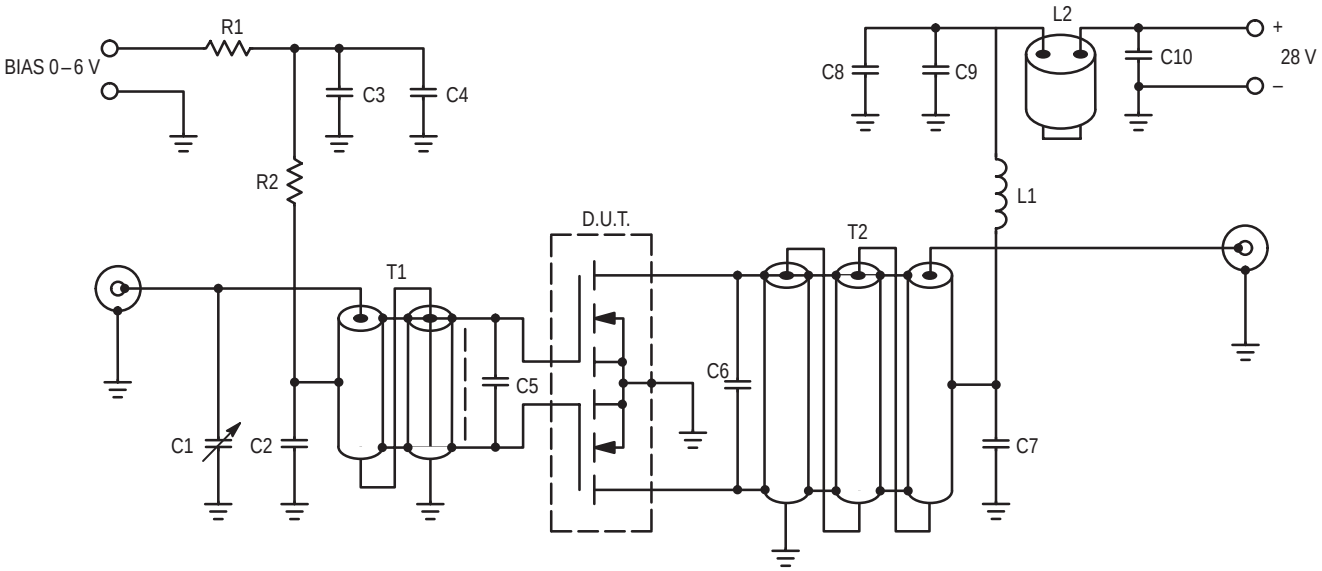
Note: Input and output impedance values given are measured from gate to gate and drain to drain respectively.

Figure 11. Series Equivalent Input/Output Impedance



B1	Balun, 50 Ω, 0.086″ O.D. 2″ Long, Semi Rigid Coax	L1, L2	#18 Wire, Hairpin Inductor
B2	Balun, 50 Ω, 0.141″ O.D. 2″ Long, Semi Rigid Coax	L3, L4	12 Turns #18, 0.340″ I.D., Enameled Wire
C1, C2, C8, C9	270 pF, ATC Chip Capacitor	L5	Ferroxcube VK200 20/4B
C3, C5, C7	1.0–20 pF, Trimmer Capacitor	L6	3 Turns #16, 0.340″ I.D., Enameled Wire
C4	15 pF, ATC Chip Capacitor	R1	1.0 kΩ, 1/4 W Resistor
C6	33 pF, ATC Chip Capacitor	R2, R3	10 kΩ, 1/4 W Resistor
C10, C12, C13, C16, C17	0.01 μF, Ceramic Capacitor	Z1, Z2	0.400″ x 0.250″, Microstrip Line
C11	1.0 μF, 50 V, Tantalum	Z3, Z4	0.870″ x 0.250″, Microstrip Line
C14, C15	680 pF, Feedthru Capacitor	Z5, Z6	0.500″ x 0.250″, Microstrip Line
C18	20 μF, 50 V, Tantalum	Board material	0.060″ Teflon–fiberglass, ε_r = 2.55, copper clad both sides, 2 oz. copper.

Figure 12. 400 MHz Test Circuit



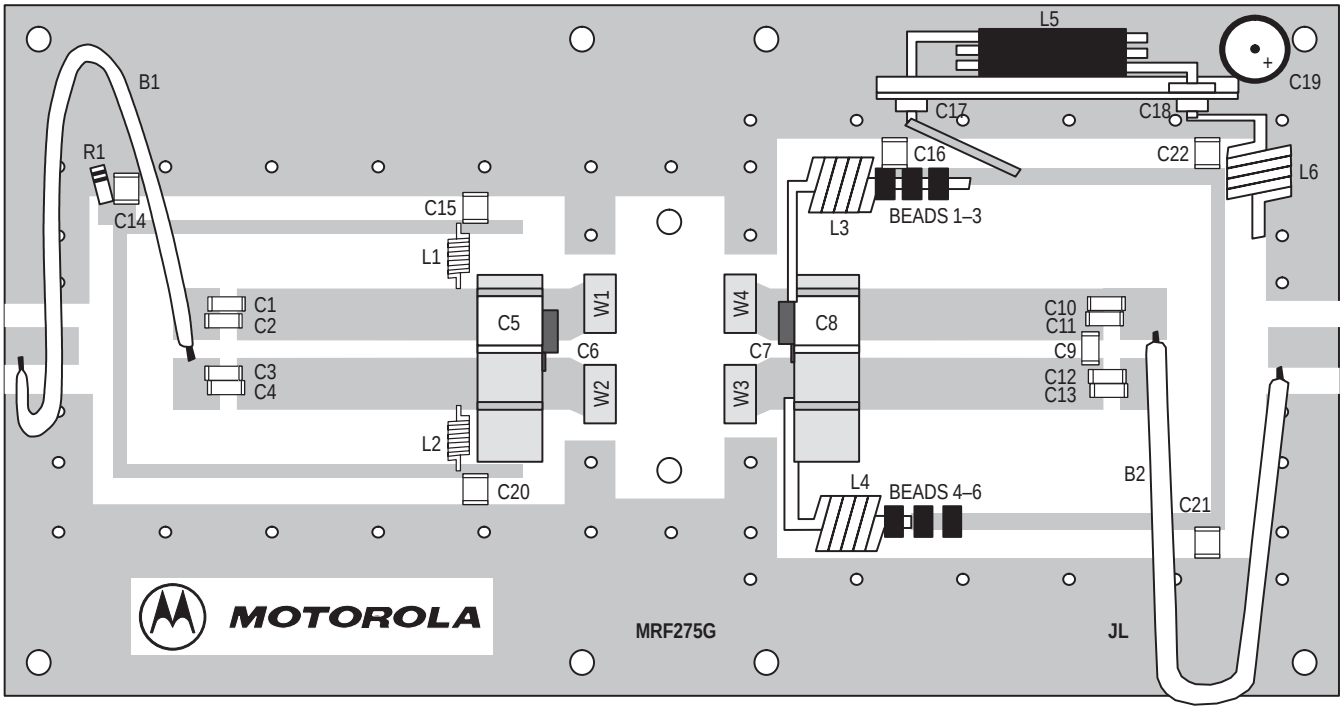
C1	8.0–60 pF, Arco 404
C2, C3, C7, C8	1000 pF, Chip Capacitor
C4, C9	0.1 μF, Chip Capacitor
C5	180 pF, Chip Capacitor
C6	100 pF and 130 pF, Chips in Parallel
C10	0.47 μF, Chip Capacitor, 1215 or Equivalent, Kemet
L1	10 Turns AWG #16, 1/4″ I.D., Enamel Wire, Close Wound
L2	Ferrite Beads of Suitable Material for 1.5–2.0 μH Total Inductance
Board material	062″ fiberglass (G10), $\varepsilon_r \cong 5$, Two sided, 1 oz. Copper.

Unless otherwise noted, all chip capacitors are ATC Type 100 or Equivalent.

R1	100 Ω, 1/2 W
R2	1.0 k Ω, 1/2 W
T1	4:1 Impedance Ratio, RF Transformer Can Be Made of 25 Ω, Semi Rigid Coax, 47–52 Mils O.D.
T2	1:9 Impedance Ratio, RF Transformer. Can Be Made of 15–18 Ω, Semi Rigid Coax, 62–90 Mils O.D.

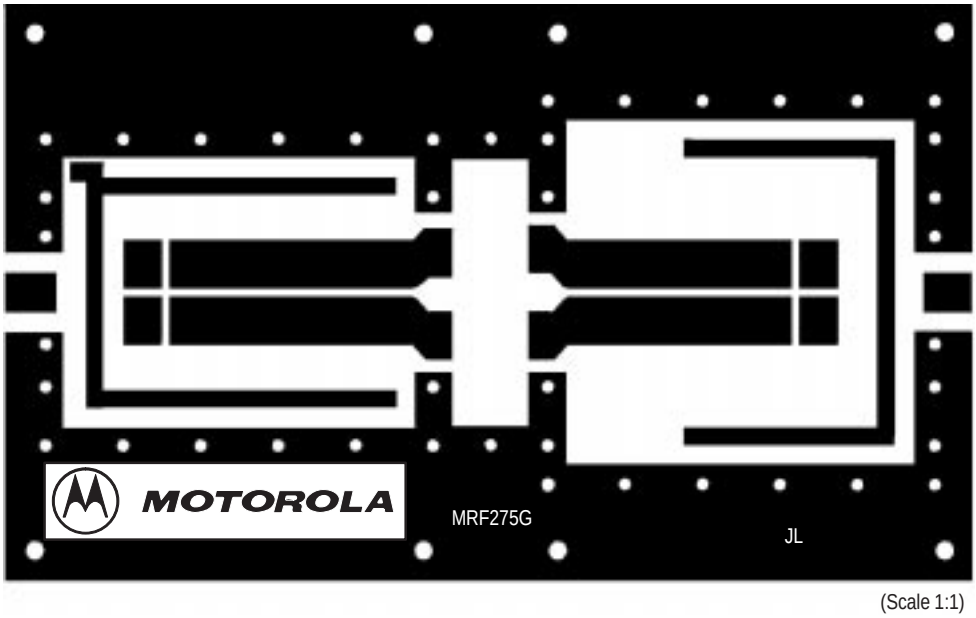
NOTE: For stability, the input transformer T1 should be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

Figure 13. 225 MHz Test Circuit



(Not to Scale)

Figure 14. MRF275G Component Location (500 MHz)



(Scale 1:1)

Figure 15. MRF275G Circuit Board Photo Master (500 MHz)
(Reduced 25% in printed data book, DL110/D)

NOTE: S–Parameter data represents measurements taken from one chip only.

Table 1. Common Source S–Parameters (V_{DS} = 12 V, I_D = 4.5 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.822	–172	6.34	91	0.027	3	0.946	–173
40	0.846	–173	4.32	81	0.027	–6	0.859	–172
50	0.842	–174	3.62	79	0.027	–8	0.863	–175
60	0.838	–175	3.03	79	0.027	–5	0.923	–177
70	0.836	–175	2.76	80	0.028	–3	1.010	–178
80	0.841	–176	2.43	78	0.029	–4	1.080	–178
90	0.849	–176	2.19	74	0.029	–7	1.150	–176
100	0.857	–176	1.89	68	0.028	–13	1.110	–176
110	0.864	–176	1.66	63	0.026	–19	1.050	–177
120	0.868	–176	1.43	60	0.024	–19	0.958	–175
130	0.871	–176	1.25	59	0.023	–19	0.905	–176
140	0.874	–176	1.15	59	0.023	–17	0.914	–177
150	0.876	–176	1.11	59	0.023	–16	0.969	–178
160	0.880	–176	1.06	59	0.023	–17	1.060	–178
170	0.885	–177	1.01	55	0.023	–18	1.130	–177
180	0.891	–177	0.96	51	0.023	–23	1.190	–178
190	0.896	–177	0.87	45	0.022	–26	1.140	–179
200	0.900	–177	0.77	43	0.020	–26	1.050	–177
210	0.904	–177	0.69	42	0.018	–25	0.958	–176
220	0.907	–177	0.63	43	0.017	–23	0.924	–175
230	0.909	–177	0.60	43	0.018	–23	0.981	–178
240	0.912	–178	0.58	44	0.017	–22	0.981	–180
250	0.915	–178	0.58	42	0.017	–20	1.040	–179
260	0.918	–178	0.56	40	0.016	–20	1.150	–180
270	0.922	–178	0.54	34	0.015	–24	1.170	179
280	0.925	–179	0.49	32	0.014	–27	1.130	–180
290	0.927	–179	0.43	28	0.013	–27	1.010	–178
300	0.930	–179	0.41	30	0.013	–23	0.964	–178
310	0.932	–179	0.40	32	0.013	–14	0.936	–178
320	0.934	–180	0.39	31	0.012	–9	0.948	180
330	0.936	–180	0.35	32	0.011	–9	1.000	180
340	0.938	180	0.38	31	0.011	–12	1.070	178
350	0.941	180	0.35	28	0.011	–12	1.100	180
360	0.943	179	0.33	23	0.011	–10	1.120	–180
370	0.944	179	0.30	21	0.011	–4	1.080	180
380	0.945	179	0.29	21	0.009	1	1.020	180
390	0.947	179	0.28	22	0.008	3	0.966	–180
400	0.948	179	0.26	25	0.008	4	0.936	–179
410	0.949	178	0.26	24	0.010	5	1.010	179
420	0.951	178	0.25	25	0.010	11	1.040	178

Table 1. Common Source S–Parameters (V_{DS} = 12 V, I_D = 4.5 A) continued

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
430	0.952	178	0.25	22	0.010	19	1.080	177
440	0.953	177	0.24	19	0.009	22	1.100	178
450	0.955	177	0.24	16	0.008	21	1.100	179
460	0.956	177	0.21	15	0.008	11	1.080	177
470	0.956	177	0.20	16	0.009	16	0.992	178
480	0.957	176	0.19	18	0.010	27	0.975	179
490	0.958	176	0.19	18	0.010	40	0.974	178
500	0.960	176	0.19	19	0.010	46	1.010	177
600	0.956	175	0.18	12	0.007	49	0.940	175
700	0.958	172	0.11	14	0.018	61	0.989	173
800	0.962	170	0.10	12	0.029	51	0.967	172
900	0.965	168	0.08	16	0.021	72	0.973	170
1000	0.964	165	0.07	12	0.021	57	1.010	168

Table 2. Common Source S–Parameters (V_{DS} = 24 V, I_D = 0.35 mA)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.829	–170	9.20	92	0.023	4	0.915	–171
40	0.858	–172	6.30	83	0.022	–4	0.834	–170
50	0.852	–173	5.28	80	0.023	–6	0.836	–174
60	0.846	–174	4.42	80	0.023	–3	0.892	–175
70	0.843	–175	4.01	81	0.024	–1	0.978	–177
80	0.847	–175	3.53	80	0.024	–2	1.050	–177
90	0.855	–175	3.18	76	0.024	–5	1.110	–176
100	0.865	–176	2.75	70	0.023	–10	1.080	–175
110	0.872	–176	2.43	65	0.022	–16	1.020	–176
120	0.874	–176	2.10	62	0.020	–16	0.932	–174
130	0.876	–176	1.84	61	0.019	–15	0.882	–175
140	0.878	–176	1.70	61	0.019	–14	0.889	–176
150	0.880	–176	1.63	61	0.019	–13	0.943	–177
160	0.883	–176	1.56	61	0.019	–13	1.030	–177
170	0.888	–177	1.49	58	0.019	–14	1.100	–176
180	0.894	–177	1.42	53	0.019	–18	1.160	–176
190	0.899	–177	1.29	47	0.018	–22	1.120	–177
200	0.902	–177	1.14	45	0.017	–24	1.030	–176
210	0.905	–177	1.02	44	0.015	–23	0.941	–175
220	0.907	–177	0.94	46	0.015	–19	0.903	–174
230	0.909	–178	0.89	45	0.015	–16	0.957	–177
240	0.912	–178	0.87	46	0.014	–15	0.961	–179
250	0.915	–178	0.86	44	0.014	–15	1.020	–178
260	0.918	–178	0.83	42	0.014	–17	1.120	–178
270	0.922	–178	0.80	36	0.013	–19	1.140	–180

Table 2. Common Source S–Parameters (V_{DS} = 24 V, I_D = 0.35 mA) continued

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
280	0.925	–179	0.73	34	0.013	–20	1.110	–179
290	0.927	–179	0.65	32	0.011	–18	0.994	–177
300	0.929	–179	0.62	32	0.011	–15	0.948	–177
310	0.931	–179	0.60	34	0.010	–9	0.916	–177
320	0.932	–180	0.57	33	0.010	–6	0.934	–180
330	0.934	–180	0.53	34	0.010	–4	0.985	–180
340	0.937	180	0.56	33	0.010	–2	1.050	179
350	0.939	180	0.53	30	0.010	0	1.090	–179
360	0.941	179	0.50	25	0.010	0	1.110	–178
370	0.943	179	0.46	23	0.009	0	1.080	–179
380	0.944	179	0.44	22	0.009	2	1.010	–179
390	0.945	179	0.41	24	0.008	8	0.956	–179
400	0.946	178	0.40	27	0.008	16	0.926	–178
410	0.947	178	0.38	26	0.009	20	1.000	–180
420	0.949	178	0.38	26	0.009	22	1.040	179
430	0.950	178	0.37	23	0.009	25	1.070	179
440	0.952	177	0.36	21	0.009	26	1.090	180
450	0.953	177	0.36	18	0.009	28	1.090	–180
460	0.954	177	0.31	17	0.009	24	1.070	178
470	0.955	177	0.30	17	0.009	29	0.990	179
480	0.956	176	0.29	19	0.009	36	0.963	–179
490	0.957	176	0.29	20	0.010	45	0.959	180
500	0.958	176	0.28	20	0.010	50	0.996	178
600	0.956	175	0.24	12	0.006	90	0.924	176
700	0.959	172	0.16	13	0.019	63	0.986	174
800	0.963	170	0.14	10	0.023	63	0.963	173
900	0.968	168	0.12	11	0.026	84	0.967	171
1000	0.969	165	0.09	7	0.025	70	1.000	169

Table 3. Common Source S–Parameters (V_{DS} = 28 V, I_D = 0.39 mA)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.834	–169	10.08	93	0.021	4	0.807	–171
40	0.863	–172	6.91	83	0.021	–4	0.828	–170
50	0.857	–173	5.79	81	0.021	–5	0.830	–173
60	0.851	–174	4.86	81	0.022	–3	0.883	–175
70	0.848	–175	4.41	82	0.022	–1	0.970	–177
80	0.852	–175	3.87	80	0.022	–1	1.040	–177
90	0.860	–175	3.49	77	0.023	–5	1.100	–176
100	0.869	–176	3.03	71	0.022	–9	1.070	–175
110	0.876	–176	2.68	66	0.021	–14	1.010	–176
120	0.878	–176	2.31	63	0.019	–14	0.923	–174
130	0.879	–176	2.03	62	0.018	–15	0.876	–175

Table 3. Common Source S–Parameters (V_{DS} = 28 V, I_D = 0.39 mA) continued

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
140	0.881	–176	1.87	62	0.018	–13	0.884	–176
150	0.883	–176	1.79	62	0.018	–11	0.934	–177
160	0.886	–177	1.72	62	0.018	–11	1.020	–177
170	0.890	–177	1.64	58	0.018	–12	1.090	–176
180	0.896	–177	1.56	54	0.018	–16	1.150	–176
190	0.901	–177	1.42	48	0.018	–21	1.110	–177
200	0.904	–177	1.26	46	0.017	–19	1.030	–176
210	0.907	–177	1.13	45	0.015	–14	0.938	–175
220	0.908	–177	1.03	47	0.013	–13	0.897	–174
230	0.910	–178	0.99	46	0.014	–15	0.948	–176
240	0.912	–178	0.96	47	0.014	–13	0.956	–179
250	0.916	–178	0.95	45	0.014	–10	1.020	–178
260	0.919	–178	0.93	42	0.013	–12	1.120	–178
270	0.922	–179	0.89	37	0.012	–15	1.140	–179
280	0.925	–179	0.81	35	0.012	–16	1.110	–178
290	0.927	–179	0.72	33	0.011	–16	0.988	–176
300	0.929	–179	0.69	33	0.011	–10	0.944	–177
310	0.931	–179	0.66	35	0.012	5	0.920	–177
320	0.933	–180	0.63	34	0.011	16	0.936	–180
330	0.934	–180	0.59	35	0.009	14	0.989	–180
340	0.937	180	0.62	34	0.009	3	1.050	180
350	0.939	180	0.59	31	0.010	4	1.080	–179
360	0.941	179	0.55	26	0.010	8	1.110	–178
370	0.943	179	0.51	24	0.009	11	1.070	–179
380	0.944	179	0.49	23	0.008	17	1.010	–178
390	0.945	179	0.46	25	0.008	24	0.949	–178
400	0.946	178	0.44	27	0.007	20	0.922	–178
410	0.947	178	0.43	26	0.010	19	0.995	–180
420	0.949	178	0.42	27	0.012	29	1.030	179
430	0.950	178	0.41	24	0.010	41	1.060	179
440	0.951	177	0.40	21	0.008	40	1.090	180
450	0.953	177	0.39	19	0.008	34	1.090	–180
460	0.953	177	0.35	17	0.009	26	1.070	178
470	0.954	177	0.33	18	0.010	30	0.983	179
480	0.955	176	0.32	19	0.012	43	0.964	–180
490	0.956	176	0.32	20	0.012	60	0.956	179
500	0.957	176	0.31	21	0.010	65	0.993	178
600	0.955	174	0.26	13	0.012	67	0.926	176
700	0.958	172	0.18	12	0.018	64	0.984	174
800	0.963	170	0.15	9	0.020	89	0.961	173
900	0.966	168	0.13	9	0.028	81	0.967	171
1000	0.968	165	0.10	6	0.033	73	0.997	169

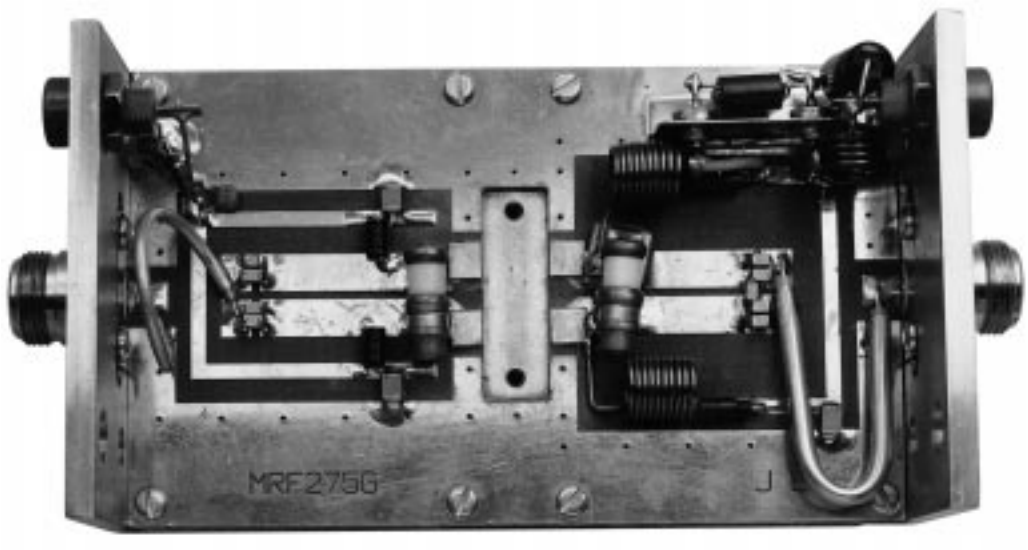


Figure 16. MRF275G Test Fixture

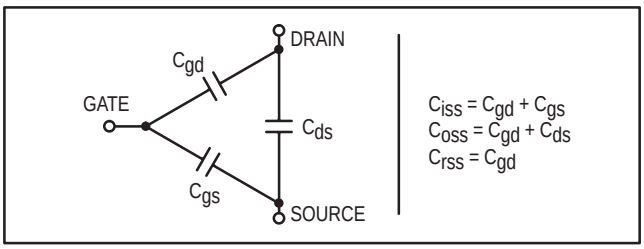
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



The C_{iss} given in the electrical characteristics table was measured using method 2 above. It should be noted that C_{iss}, C_{oss}, C_{rss} are measured at zero drain current and are provided for general information about the device. They are not RF design parameters and no attempt should be made to use them as such.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating (or any of the maximum ratings on the front page). Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of this device are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate

may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with grounded equipment.

DESIGN CONSIDERATIONS

The MRF275G is a RF power N–channel enhancement mode field–effect transistor (FETs) designed for HF, VHF and UHF power amplifier applications. Motorola RF MOSFETs feature a vertical structure with a planar design.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

The MRF275G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF275G was characterized at I_{DQ} = 100 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF275G may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

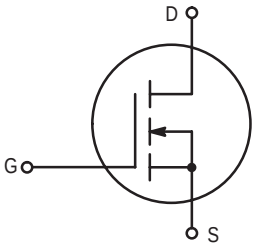
The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode

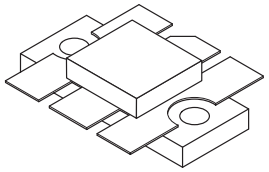
MRF275L

100 W, 28 V, 500 MHz
N–CHANNEL
BROADBAND
RF POWER FET

Designed for broadband commercial and military applications using single ended circuits at frequencies to 500 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance @ 500 MHz, 28 Vdc
  Output Power — 100 Watts
  Power Gain — 8.8 dB Typ
  Efficiency — 55% Typ
- 100% Ruggedness Tested At Rated Output Power
- Low Thermal Resistance
- Low C_{rss} — 17 pF Typ @ V_{DS} = 28 Volts
- S–Parameters Available for Download into Frequency Domain Simulators.
  See http://mot–sps.com/rf/designtds/





CASE 333–04, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	13	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

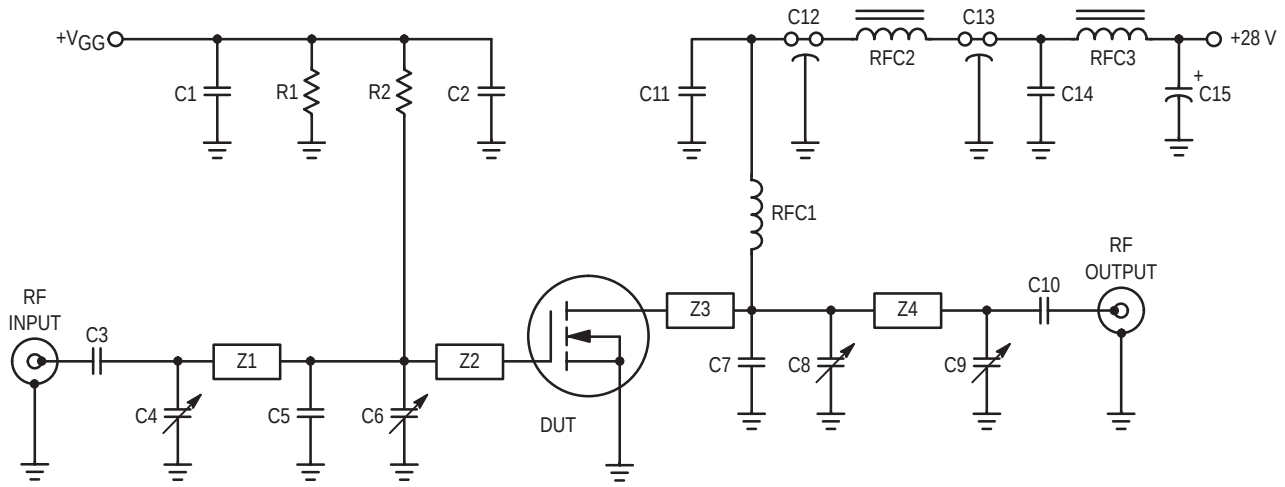
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	2.5	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.5	2.5	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 5.0 A)	$V_{DS(on)}$	0.5	0.9	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	3.0	3.75	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	135	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	140	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	17	—	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 500 MHz, I_{DQ} = 100 mA)	G_{ps}	7.5	8.8	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 500 MHz, I_{DQ} = 100 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 500 MHz, I_{DQ} = 100 mA, VSWR 10:1 at all Phase Angles)	ψ	No Degradation in Output Power			



C1, C11, C14	0.1 μF, Ceramic Capacitor
C2	240 pF, ATC Type Chip Capacitor
C3, C10	270 pF, ATC Type Chip Capacitor
C4, C6, C8, C9	1–20 pF, Trimmer Capacitor, Johansen
C5	24 pF, Mini–Unelco Type Capacitor
C7	24 pF, Mini–Unelco Type Capacitor
C12, C13	680 pF, Feedthru Capacitors
C15	10 μF, 50 V, Electrolytic Capacitor
RFC1	8 Turns AWG #18, 0.25″ I.D., Enameled
RFC2, RFC3	Ferroxcube VK200 19/4B
Z1,	0.250″ x 0.800″, Microstrip Line
Z2, Z3	0.250″ x 0.400″, Microstrip Line
Z4	0.250″ x 1.25″, Microstrip Line
Board Material	0.062″ Glass Teflon®, 2 oz. Copper, Double Clad Copper Board, ε_r = 2.55

Figure 1. 500 MHz Test Circuit

TYPICAL CHARACTERISTICS

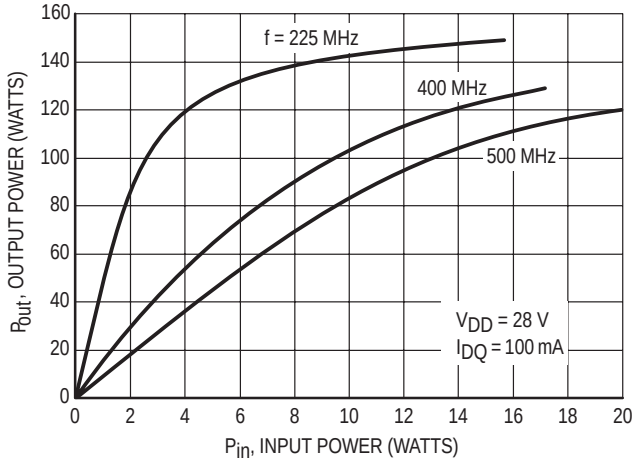


Figure 2. Output Power versus Input Power

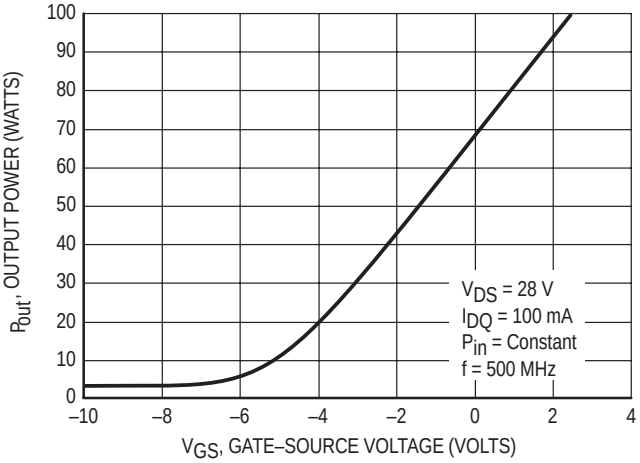


Figure 3. Output Power versus Gate Voltage

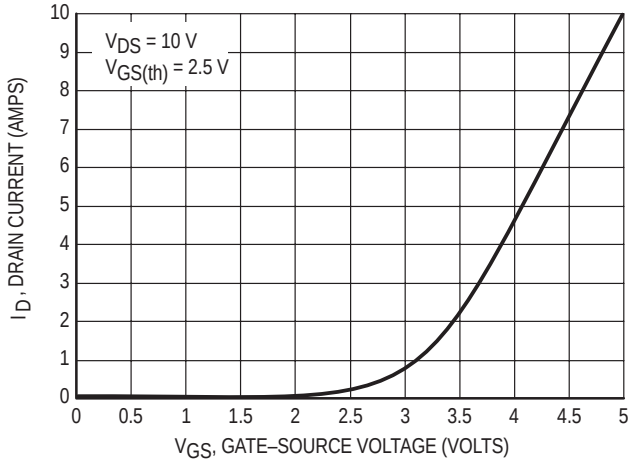


Figure 4. Drain Current versus Gate Voltage (Transfer Characteristics)

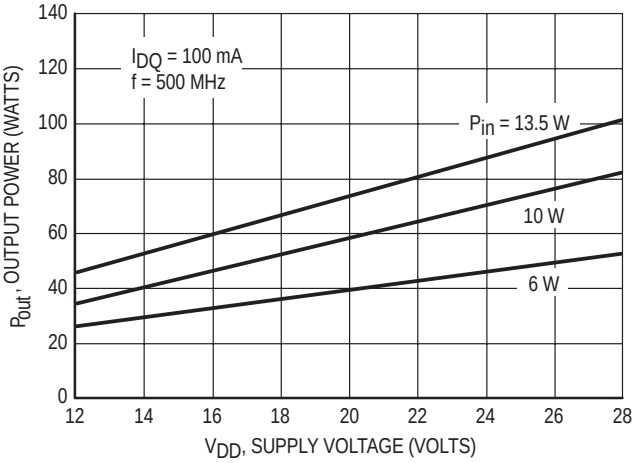


Figure 5. Output Power versus Supply Voltage

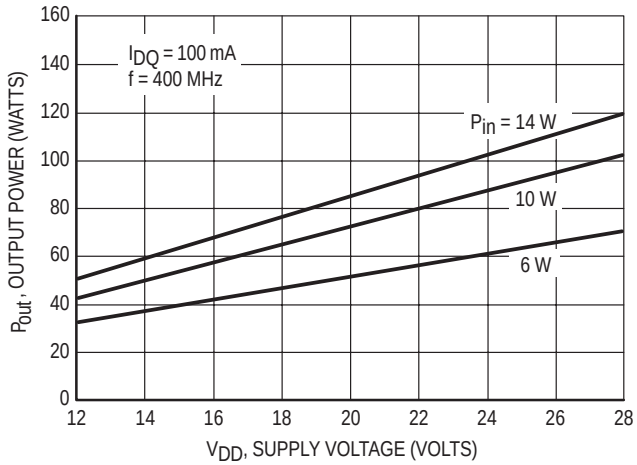


Figure 6. Output Power versus Supply Voltage

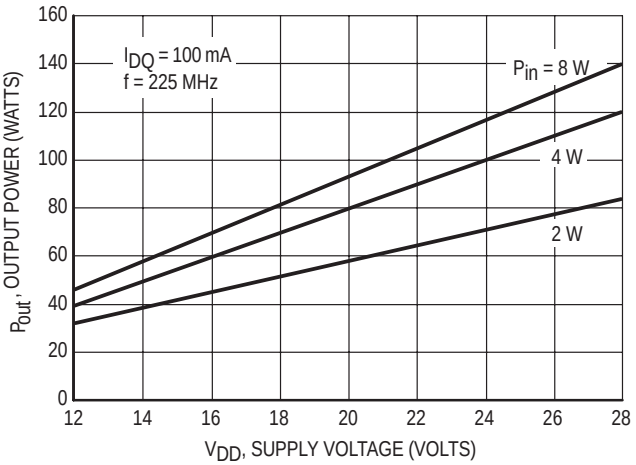


Figure 7. Output Power versus Supply Voltage

TYPICAL CHARACTERISTICS

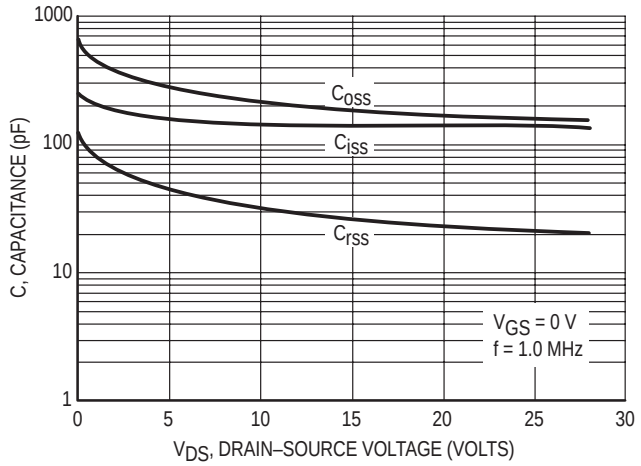


Figure 8. Capacitance versus Drain–Source Voltage

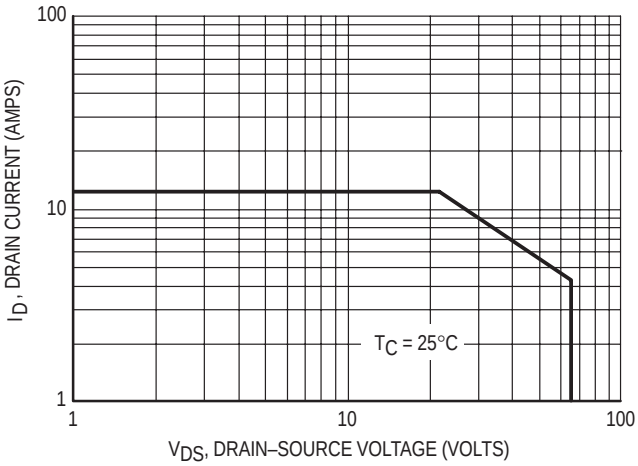
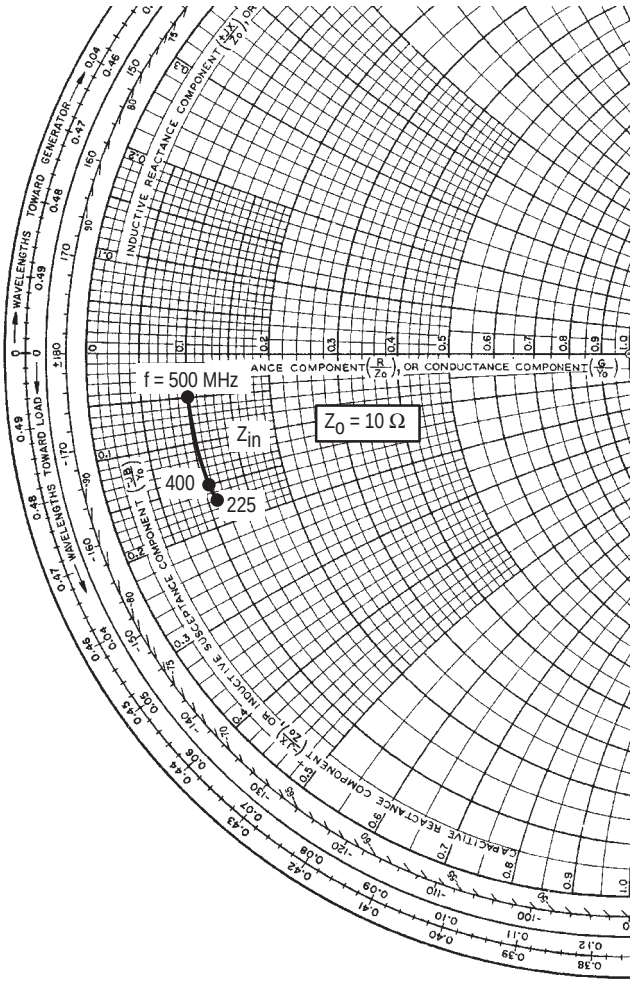
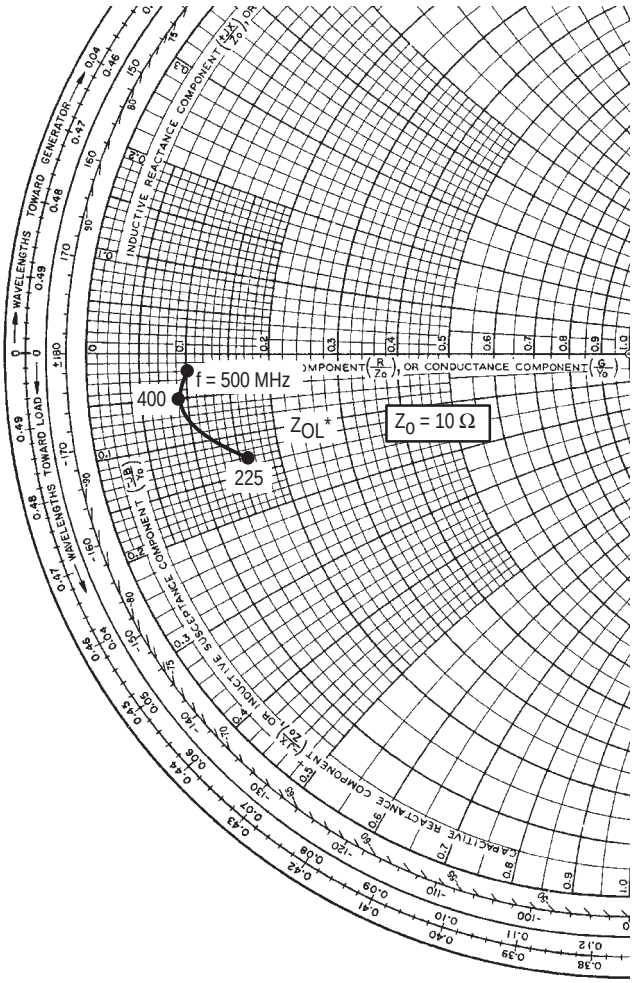


Figure 9. DC Safe Operating Area





V_{DD} = 28 V, I_{DQ} = 100 mA, P_{out} = 100 W

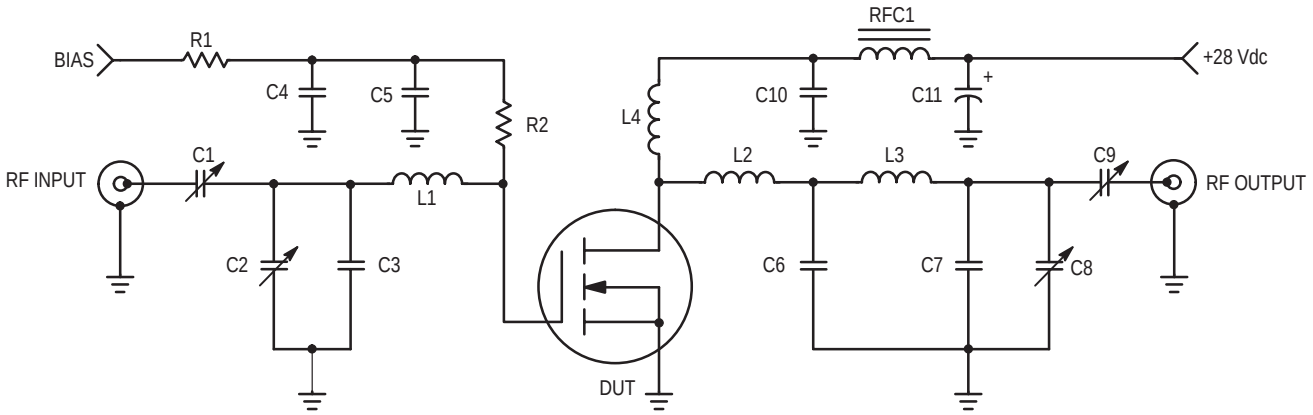
f (MHz)	Z_{in} Ohms
225	1.1 – j1.7
400	1.08 – j1.5
500	1.0 – j0.5

V_{DD} = 28 V, I_{DQ} = 100 mA, P_{out} = 100 W

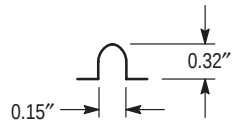
f (MHz)	Z_{OL}* Ohms
225	1.6 – j1.3
400	0.9 – j0.5
500	1.0 – j0.2

Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

Figure 10. Series Equivalent Input/Output Impedance



C1, C2, C8	Arco 463 or Equivalent	L1	Hairpin Inductor #18 Wire	L3	Hairpin Inductor #16 Wire
C3, C7	25 pF, Unelco Capacitor				
C4	1000 pF, Chip Capacitor				
C5	0.01 μF, Chip Capacitor				
C6	250 pF, Unelco Capacitor				
C9	Arco 462 or Equivalent				
C10	1000 pF, ATC Chip Capacitor				
C11	10 μF, 100 V, Electrolytic Capacitor	L2	Stripline Inductor 0.200″ x 0.500″	L4	2 Turns #16 Wire, 5/16″ ID
				RFC1	VK200–4B
				R1	1.0 k, 1/4 W Resistor
				R2	100 Ω Resistor



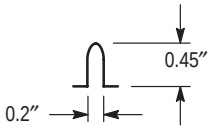
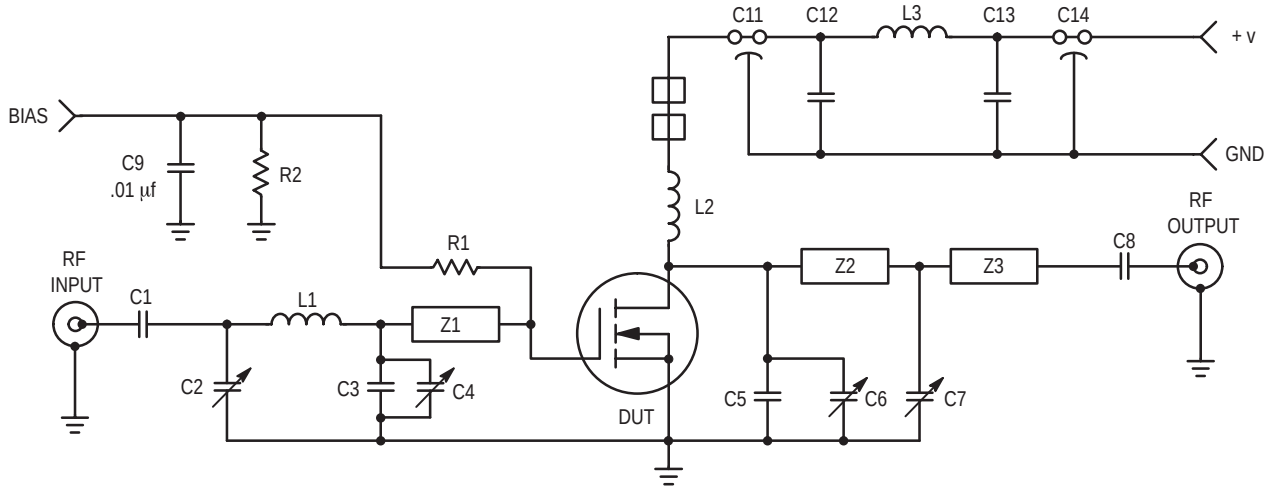


Figure 11. 225 MHz Test Circuit



C1, C8	270 pF, ATC Chip Capacitor	L1	Hairpin Inductor #18 Wire	R1	10 k, 1/4 W Resistor
C2, C4, C6, C7	1.0–20 pF, Trimmer Capacitor			R2	1 k, 1/4 W Resistor
C3	15 pF, Mini Unelco Capacitor			R3	1.5 k, 1/4 W Resistor
C5	47 pF, Mini Unelco Capacitor			Z1	0.950″ x 0.250″, Microstrip Line
C9, C12	0.1 μF, Ceramic Capacitor			Z2	1.25″ x 0.250″, Microstrip Line
C11, C14	680 pF, Feed Thru Capacitor			Z3	0.300″ x 0.250″, Microstrip Line
C13	50 μF, Tantalum Capacitor	L2	12 Turns #18 Wire, 0.450″ ID	Board Material	0.062″ Teflon®, Fiberglass, 1 oz. Copper, Clad Both Sides, ε_r = 2.56
		L3	Ferroxcube VK200 20/4B		

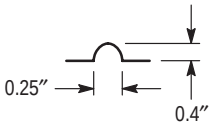
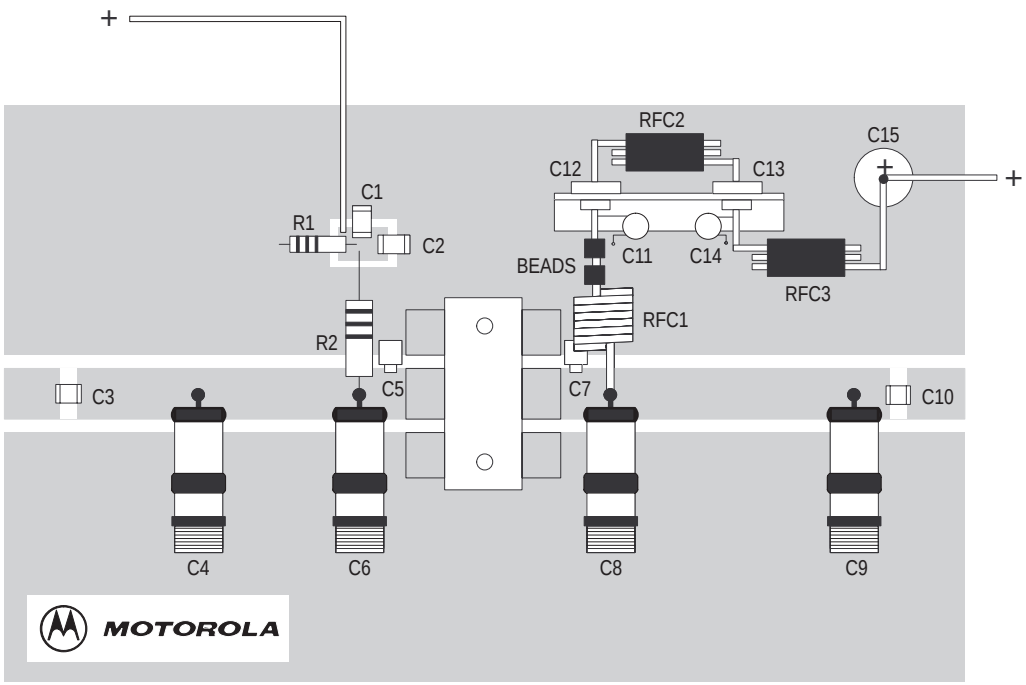
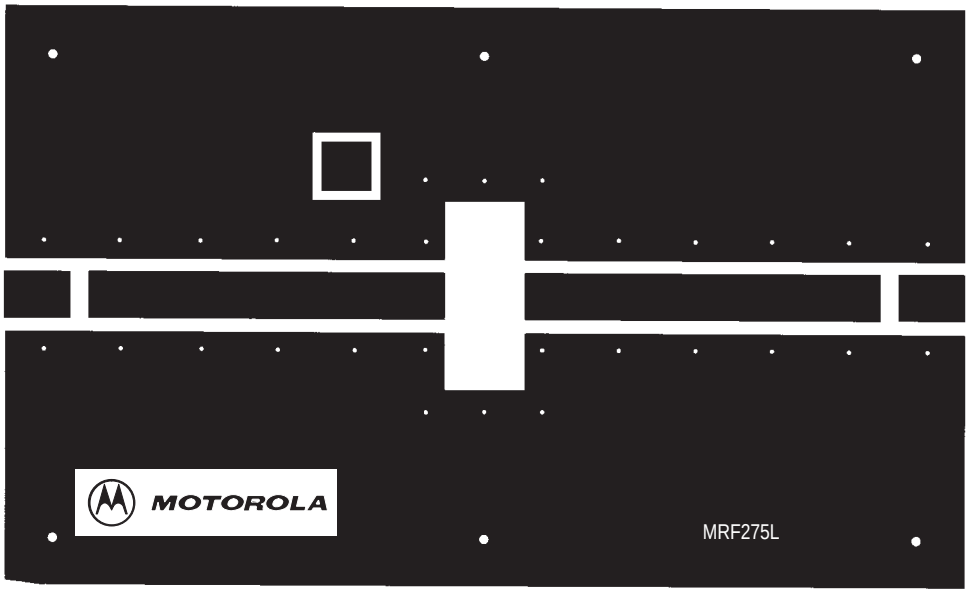


Figure 12. 400 MHz Test Circuit



(Not to Scale)

Figure 13. MRF275L Component Location (500 MHz)



(Scale 1:1)

Figure 14. MRF275L Test Circuit Photomaster
(Reduced 18% in printed data book, DL110/D)

Table 1. Common Source S–Parameters (V_{DS} = 12.5 V, I_D = 4.5 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.936	–176	6.22	87	0.010	21	0.944	–179
40	0.938	–178	4.28	87	0.010	24	0.930	–177
50	0.937	–178	3.65	83	0.010	29	0.922	179
60	0.937	–179	2.99	83	0.011	34	0.920	179
70	0.938	–179	2.54	81	0.011	39	0.917	179
80	0.938	–179	2.18	80	0.012	42	0.913	179
90	0.939	–180	1.94	78	0.012	44	0.909	180
100	0.939	–180	1.77	77	0.013	47	0.913	–180
110	0.939	180	1.57	77	0.015	50	0.916	–179
120	0.940	180	1.45	74	0.015	54	0.914	179
130	0.940	179	1.34	75	0.016	57	0.935	180
140	0.940	179	1.26	72	0.016	58	0.943	180
150	0.940	179	1.19	71	0.017	57	0.951	178
160	0.941	179	1.09	70	0.019	58	0.943	179
170	0.941	179	1.01	69	0.019	62	0.940	180
180	0.941	179	0.956	68	0.021	64	0.948	179
190	0.941	178	0.912	67	0.022	65	0.957	180
200	0.942	178	0.860	65	0.022	65	0.941	178
210	0.942	178	0.816	64	0.023	65	0.931	178
220	0.943	178	0.779	63	0.025	66	0.922	178
230	0.943	177	0.717	60	0.027	67	0.965	177
240	0.943	177	0.709	61	0.026	68	0.927	176
250	0.944	177	0.674	60	0.026	70	0.924	178
260	0.944	177	0.645	58	0.028	69	0.930	179
270	0.944	177	0.627	57	0.030	70	0.933	178
280	0.945	176	0.608	58	0.032	70	0.940	177
290	0.946	176	0.580	54	0.031	71	0.941	175
300	0.946	176	0.569	56	0.033	71	0.945	176
310	0.946	176	0.539	55	0.033	72	0.953	178
320	0.947	175	0.512	54	0.035	71	0.952	177
330	0.948	175	0.483	51	0.037	72	0.927	176
340	0.947	175	0.477	52	0.038	72	0.921	176
350	0.947	175	0.466	51	0.039	75	0.929	178
360	0.947	175	0.459	51	0.040	73	0.963	177
370	0.948	174	0.441	50	0.043	71	0.968	175
380	0.949	174	0.428	49	0.044	72	0.937	175
390	0.949	174	0.417	49	0.045	74	0.907	176
400	0.949	174	0.409	47	0.044	77	0.912	177
410	0.950	173	0.390	46	0.046	74	0.962	175
420	0.950	173	0.377	45	0.047	71	0.971	174
430	0.950	173	0.369	45	0.050	72	0.948	176
440	0.951	173	0.368	47	0.052	74	0.953	176

Table 1. Common Source S–Parameters (V_{DS} = 12.5 V, I_D = 4.5 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
450	0.951	172	0.371	42	0.053	76	0.943	175
460	0.952	172	0.347	44	0.053	72	0.965	172
470	0.952	172	0.331	43	0.053	71	0.933	173
480	0.953	172	0.323	43	0.056	71	0.936	173
490	0.953	171	0.317	41	0.059	72	0.965	173
500	0.954	171	0.306	41	0.061	74	0.963	173
600	0.957	168	0.267	35	0.069	77	0.941	171
700	0.965	165	0.224	35	0.090	70	0.958	169
800	0.967	160	0.219	32	0.099	67	0.937	164
900	0.980	156	0.214	33	0.114	69	0.943	164
1000	0.986	151	0.218	34	0.146	67	0.955	162

Table 2. Common Source S–Parameters (V_{DS} = 24 V, I_D = 4.5 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.914	–174	9.08	87	0.011	19	0.882	–178
40	0.918	–176	6.29	86	0.011	22	0.876	–176
50	0.918	–177	5.31	82	0.011	26	0.871	180
60	0.917	–177	4.35	82	0.012	29	0.871	–179
70	0.919	–178	3.70	79	0.012	32	0.865	–179
80	0.919	–178	3.16	77	0.013	37	0.857	–179
90	0.920	–179	2.81	75	0.013	42	0.851	–180
100	0.921	–179	2.55	74	0.014	46	0.863	–179
110	0.922	–179	2.27	73	0.014	47	0.876	–178
120	0.923	–179	2.08	70	0.015	49	0.867	–179
130	0.923	–180	1.92	70	0.016	51	0.880	–178
140	0.924	–180	1.78	67	0.017	55	0.880	–179
150	0.925	–180	1.68	65	0.018	58	0.904	179
160	0.926	180	1.53	64	0.018	60	0.901	–180
170	0.927	180	1.42	62	0.018	61	0.900	–179
180	0.928	180	1.34	62	0.020	61	0.901	–179
190	0.929	179	1.28	60	0.021	63	0.906	–179
200	0.930	179	1.19	58	0.022	65	0.892	179
210	0.931	179	1.12	56	0.022	67	0.902	178
220	0.932	179	1.06	55	0.023	68	0.903	179
230	0.933	179	0.988	53	0.024	67	0.931	179
240	0.934	178	0.960	53	0.025	69	0.889	179
250	0.934	178	0.910	52	0.026	73	0.877	180
260	0.935	178	0.866	50	0.026	74	0.895	180
270	0.936	178	0.838	49	0.027	74	0.908	180
280	0.937	177	0.803	49	0.029	71	0.923	179
290	0.939	177	0.766	46	0.030	72	0.915	177

Table 2. Common Source S–Parameters (V_{DS} = 24 V, I_D = 4.5 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
300	0.939	177	0.744	46	0.032	76	0.907	178
310	0.939	177	0.702	46	0.032	81	0.908	180
320	0.940	176	0.660	45	0.031	81	0.913	178
330	0.941	176	0.623	41	0.031	75	0.909	177
340	0.942	176	0.613	42	0.035	71	0.910	178
350	0.943	176	0.599	41	0.039	78	0.905	–180
360	0.943	175	0.585	41	0.040	83	0.913	179
370	0.943	175	0.556	39	0.037	85	0.924	176
380	0.944	175	0.534	38	0.035	80	0.922	175
390	0.944	175	0.512	38	0.037	73	0.907	176
400	0.946	174	0.503	37	0.043	76	0.906	179
410	0.948	174	0.482	36	0.049	81	0.944	177
420	0.948	174	0.464	35	0.047	87	0.940	176
430	0.947	174	0.450	36	0.040	88	0.912	176
440	0.947	173	0.440	36	0.039	79	0.947	176
450	0.948	173	0.445	32	0.047	73	0.944	177
460	0.951	173	0.414	32	0.057	75	0.959	174
470	0.952	173	0.397	32	0.057	86	0.913	176
480	0.951	172	0.387	33	0.050	95	0.908	175
490	0.950	172	0.376	31	0.042	90	0.941	174
500	0.950	172	0.361	31	0.044	74	0.963	175
600	0.957	168	0.287	24	0.073	75	0.932	172
700	0.965	164	0.231	24	0.091	70	0.952	169
800	0.966	160	0.216	23	0.091	67	0.928	163
900	0.979	156	0.205	27	0.112	69	0.930	164
1000	0.981	150	0.206	29	0.146	58	0.947	162

Table 3. Common Source S–Parameters (V_{DS} = 28 V, I_D = 4.5 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.910	–173	9.76	87	0.011	17	0.872	–177
40	0.913	–175	6.73	86	0.011	17	0.860	–174
50	0.913	–176	5.69	81	0.011	21	0.849	–179
60	0.913	–177	4.66	81	0.012	26	0.846	–178
70	0.915	–177	3.97	78	0.012	31	0.853	–179
80	0.916	–178	3.39	76	0.012	33	0.858	–178
90	0.916	–178	3.01	74	0.012	34	0.853	–178
100	0.917	–178	2.73	73	0.013	36	0.851	–177
110	0.918	–179	2.42	72	0.014	41	0.849	–177
120	0.919	–179	2.22	68	0.014	48	0.853	–178
130	0.920	–179	2.05	68	0.014	52	0.879	–178
140	0.921	–179	1.90	66	0.014	52	0.894	–178
150	0.922	–180	1.79	64	0.015	51	0.898	–178

Table 3. Common Source S–Parameters (V_{DS} = 28 V, I_D = 4.5 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
160	0.923	–180	1.63	63	0.016	53	0.880	–177
170	0.924	–180	1.50	61	0.017	58	0.890	–178
180	0.925	180	1.42	60	0.019	62	0.904	–178
190	0.926	180	1.35	58	0.019	64	0.922	–179
200	0.928	179	1.26	56	0.019	63	0.914	–179
210	0.929	179	1.19	54	0.020	62	0.897	–179
220	0.930	179	1.12	53	0.022	64	0.881	–179
230	0.932	179	1.04	51	0.024	67	0.907	180
240	0.932	179	1.01	51	0.024	69	0.892	179
250	0.933	178	0.955	49	0.024	70	0.910	–180
260	0.934	178	0.912	47	0.025	70	0.912	–178
270	0.936	178	0.882	46	0.027	71	0.904	–178
280	0.936	178	0.842	46	0.029	72	0.901	–180
290	0.938	177	0.798	43	0.028	71	0.920	177
300	0.939	177	0.770	44	0.030	71	0.930	178
310	0.939	177	0.731	43	0.032	72	0.934	–179
320	0.941	177	0.690	42	0.035	74	0.939	–180
330	0.942	176	0.655	39	0.036	76	0.895	180
340	0.942	176	0.639	40	0.035	75	0.892	179
350	0.942	176	0.613	39	0.036	75	0.906	–180
360	0.943	175	0.601	38	0.040	71	0.945	179
370	0.945	175	0.577	36	0.045	71	0.960	178
380	0.946	175	0.555	35	0.047	74	0.928	178
390	0.947	175	0.531	35	0.045	79	0.893	178
400	0.946	174	0.518	34	0.042	80	0.892	179
410	0.947	174	0.492	33	0.044	72	0.948	176
420	0.948	174	0.472	32	0.049	67	0.960	176
430	0.950	173	0.462	32	0.056	71	0.936	179
440	0.951	173	0.455	32	0.058	78	0.945	179
450	0.951	173	0.460	30	0.054	82	0.920	177
460	0.950	173	0.424	30	0.050	73	0.951	173
470	0.950	172	0.400	29	0.053	65	0.937	174
480	0.952	172	0.389	29	0.063	65	0.941	175
490	0.954	172	0.382	27	0.071	72	0.960	175
500	0.955	172	0.367	27	0.069	80	0.954	176
600	0.958	168	0.284	22	0.071	80	0.935	172
700	0.967	164	0.226	22	0.088	71	0.950	169
800	0.967	160	0.211	22	0.096	67	0.929	164
900	0.979	156	0.197	26	0.116	69	0.929	165
1000	0.978	150	0.200	29	0.139	67	0.944	163

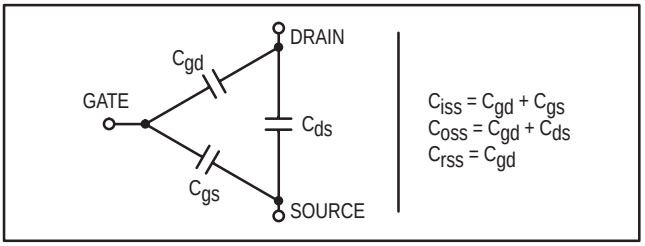
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the FET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the FET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

DESIGN CONSIDERATIONS

The MRF275L is a RF power N–channel enhancement mode field–effect transistor (FETs) designed for HF, VHF and UHF power amplifier applications. Motorola FETs feature a vertical structure with a planar design.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

The MRF275L is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF275L was characterized at I_{DQ} = 100 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF275L may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

N–Channel Enhancement–Mode Lateral MOSFETs

MRF282SR1*
MRF282ZR1*

*To be introduced 1Q00.

10 W, 2000 MHz, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

Designed for class A and class AB PCN and PCS base station applications at frequencies up to 2600 MHz. Suitable for FM, TDMA, CDMA, and multicarrier amplifier applications.

- Specified Two–Tone Performance @ 2000 MHz, 26 Volts
  Output Power = 10 Watts (PEP)
  Power Gain = 11 dB
  Efficiency = 30%
  Intermodulation Distortion = –28 dBc
- Specified Single–Tone Performance @ 2000 MHz, 26 Volts
  Output Power = 10 Watts (CW)
  Power Gain = 11 dB
  Efficiency = 40%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 2000 MHz, 10 Watts (CW) Output Power
- Gold Metallization for Improved Reliability
- Available in Tape and Reel. R1 Suffix = 500 Units per 12 mm, 7 inch Reel.
- LDMOS Models and Circuit Board Artwork Available at: http://motorola.com/sps/rf/designtds/



CASE 458–05, STYLE 1
(MRF282SR1)



CASE 458A–02, STYLE 1
(MRF282ZR1)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 0.34	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.9	°C/W

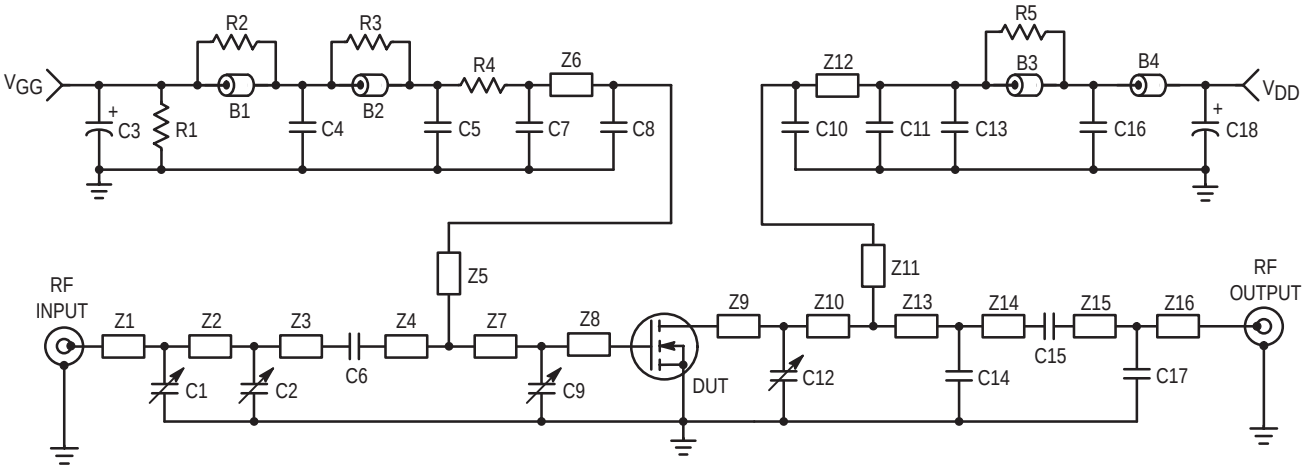
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1.0	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 50 μAdc)	$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 0.5 Adc)	$V_{DS(on)}$	—	0.4	0.6	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 0.5 Adc)	g_{fs}	—	0.7	—	S
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 75 mAdc)	$V_{GS(q)}$	3.0	4.0	5.0	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	15	—	pF
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	8.0	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	0.45	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	G_{ps}	11	12.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	η	30	34	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	IMD	—	–32.5	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	IRL	10	14	—	dB
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	G_{ps}	11	12.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	η	—	30	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IMD	—	–32.5	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IRL	10	14	—	dB
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 10 W CW, I_{DQ} = 75 mA, f = 2000.0 MHz)	G_{ps}	11	12.3	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 10 W CW, I_{DQ} = 75 mA, f = 2000.0 MHz)	η	40	45	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 10 W CW, I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz, Load VSWR = 10:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation In Output Power			



Z1	0.491″ x 0.080″ Microstrip	Z11	0.636″ x 0.055″ Microstrip
Z2	0.253″ x 0.080″ Microstrip	Z12	0.303″ x 0.055″ Microstrip
Z3	0.632″ x 0.080″ Microstrip	Z13	0.463″ x 0.080″ Microstrip
Z4	0.567″ x 0.080″ Microstrip	Z14	0.105″ x 0.080″ Microstrip
Z5	1.139″ x 0.055″ Microstrip	Z15	0.452″ ± 0.085″ x 0.080″ Microstrip
Z6	0.236″ x 0.055″ Microstrip	Z16	0.910″ ± 0.085″ x 0.080″ Microstrip
Z7	0.180″ x 0.325″ Microstrip	Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55
Z8	0.301″ x 0.325″ Microstrip		
Z9	0.439″ x 0.325″ Microstrip		
Z10	0.055″ x 0.325″ Microstrip		

Figure 1. 1.93 – 2.0 GHz Broadband Test Circuit Schematic

Table 1. 1.93 – 2.0 GHz Broadband Component Designations and Values

Designators	Description
B1, B4	0.120″ x 0.333″ x 0.100″, Surface Mount Ferrite Beads, Fair Rite # 2743019446
B2, B3	0.120″ x 0.170″ x 0.100″, Surface Mount Ferrite Beads, Fair Rite # 2743029446
C1, C2, C9	0.8–8.0 pF Gigatrim Variable Capacitors, Johanson # 27291SL
C3	10 μF, 35 V Tantalum Surface Mount Chip Capacitor, Kemet # T495X106K035AS4394
C4, C5, C13, C16	0.1 μF Chip Capacitor, Kemet # CDR33BX104AKWS
C6	200 pF, B Case RF Chip Capacitors, ATC # 100B201JCA500X
C7	18 pF, B Case RF Chip Capacitors, ATC # 100B180KP500X
C8	39 pF, B Case RF Chip Capacitors, ATC # 100B390JCA500X
C10	27 pF, B Case RF Chip Capacitors, ATC # 100B270JCA500X
C11	1.2 pF, B Case RF Chip Capacitors, ATC # 100B1R2CCA500X
C12	0.6–4.5 pF, Gigatrim Variable Capacitor, Johanson # 27271SL
C14	0.5 pF, B Case RF Chip Capacitors, ATC # 100B0R5BCA500X
C15	15 pF, B Case RF Chip Capacitors, ATC # 100B150JCA500X
C17	0.1 pF, B Case RF Chip Capacitors, ATC # 100B0R1BCA500X
C18	22 μF, 35 V Tantalum Surface Mount Chip Capacitor, Kemet # T491X226K035AS4394
R1	560 kΩ, 1/4 W Chip Resistor 0.08″ x 0.13″
R2, R5	12 Ω, 1/4 W Chip Resistor 0.08″ x 0.13″, Garrett Instruments # RM73B2B120JT
R3, R4	91 Ω, 1/4 W Chip Resistor 0.08″ x 0.13″, Garrett Instruments # RM73B2B910JT
WS1, WS2	Berrylium Copper Wear Blocks 0.010″ x 0.235″ x 0.135″ NOM
	Brass Banana Jack and Nut
	Red Banana Jack and Nut
	Green Banana Jack and Nut
	Type “N” Jack Connectors, Omni–Spectra # 3052–1648–10
	4–40 Ph Head Screws, 0.125″ Long
	4–40 Ph Head Screws, 0.188″ Long
	4–40 Ph Head Screws, 0.312″ Long
	4–40 Ph Rec. Hd. Screws, 0.438″ Long
RF Circuit Board	3″ x 5″ Copper Clad PCB, Glass Teflon®

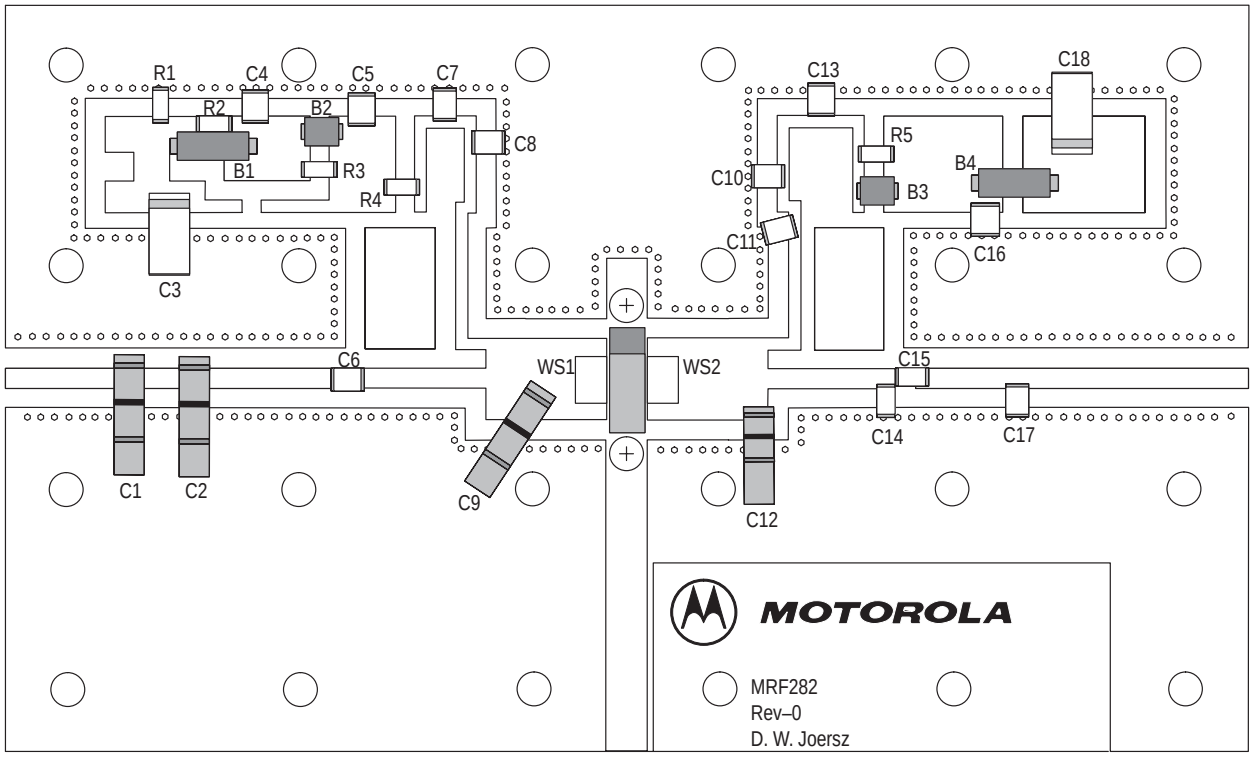
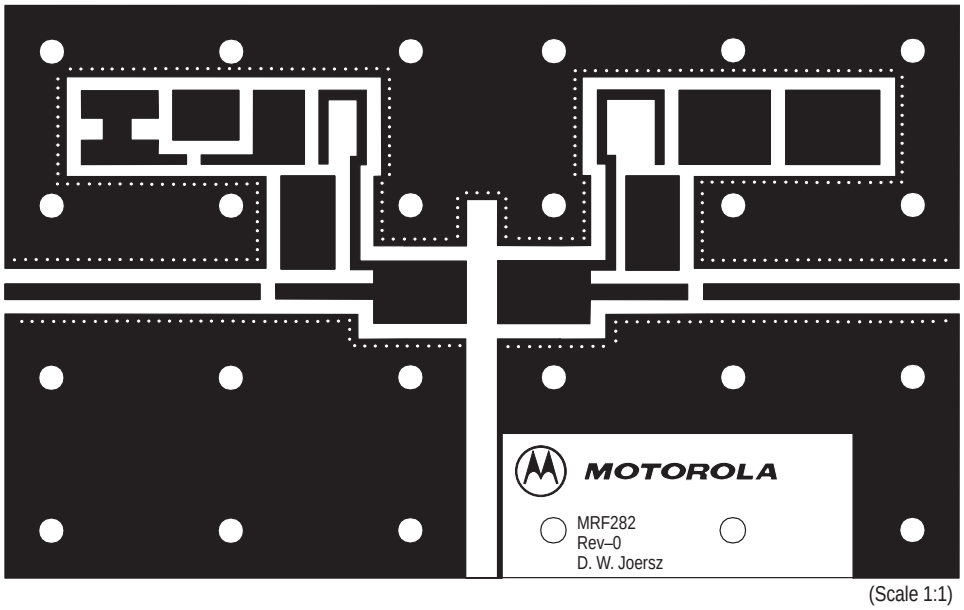
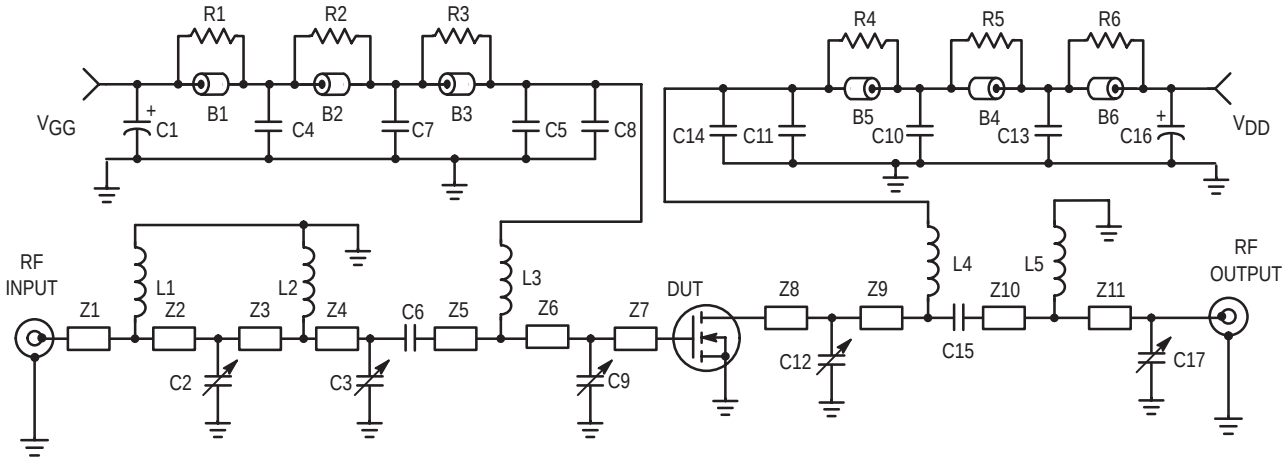


Figure 2. 1.93–2.0 GHz Broadband Test Circuit Component Layout



(Scale 1:1)

Figure 3. MRF282 Test Circuit Photomaster
(Reduced 18% in printed data book, DL110/D)

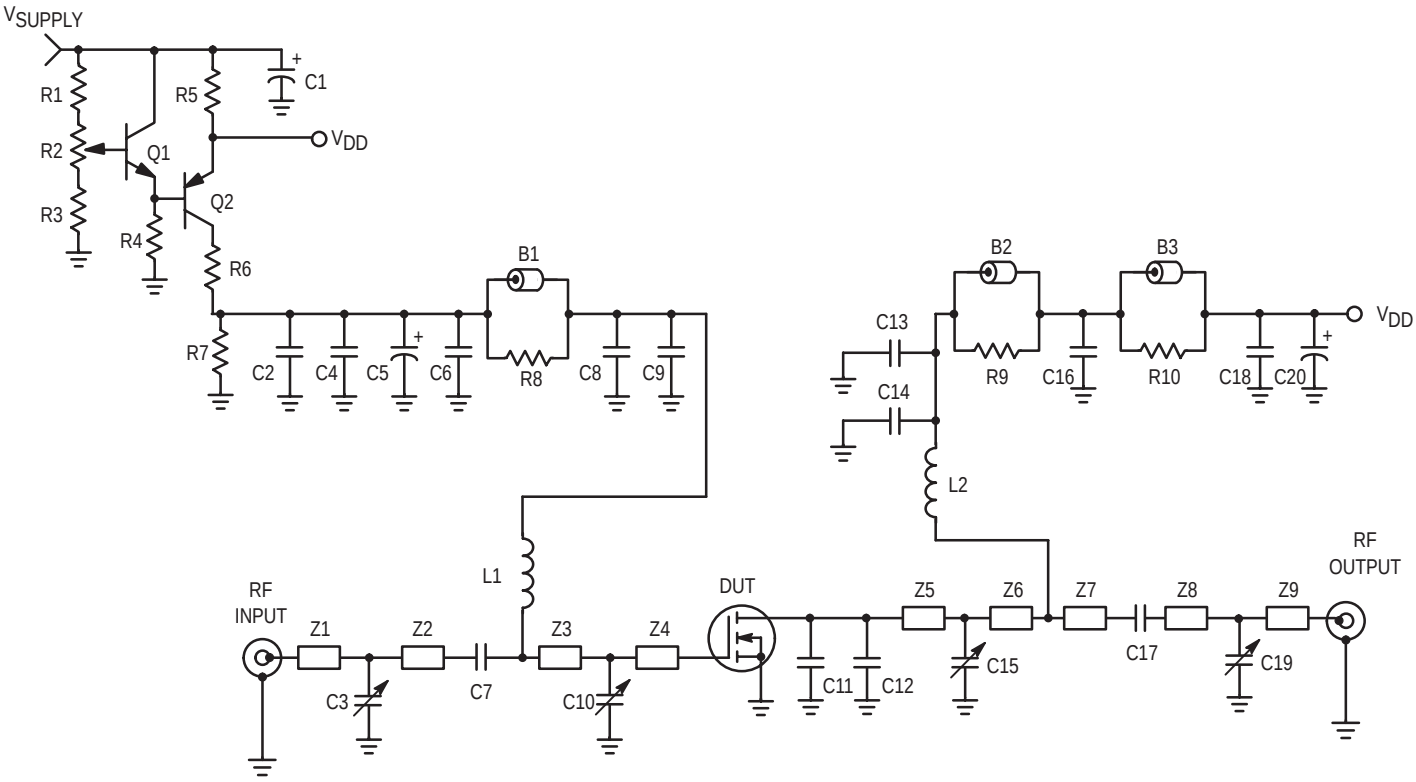


Z1	0.122″ x 0.08″ Microstrip	Z8	0.414″ x 0.330″ Microstrip
Z2	0.650″ x 0.08″ Microstrip	Z9	0.392″ x 0.08″ Microstrip
Z3	0.160″ x 0.08″ Microstrip	Z10	0.070″ x 0.08″ Microstrip
Z4	0.030″ x 0.08″ Microstrip	Z11	1.110″ x 0.08″ Microstrip
Z5	0.045″ x 0.08″ Microstrip	Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55
Z6	0.291″ x 0.08″ Microstrip		
Z7	0.483″ x 0.330″ Microstrip		

Figure 4. 1.81 – 1.88 GHz Broadband Test Circuit Schematic

Table 2. 1.81 – 1.88 GHz Broadband Component Designations and Values

Designators	Description
B1, B2, B3, B4, B5, B6	0.120″ x 0.170″ x 0.100″, Surface Mount Ferrite Beads, Fair Rite # 2743029446
C1, C16	470 μF, 63 V, Electrolytic Capacitor, Mallory # SME63UB471M12X25L
C2, C9, C12, C17	0.6–4.5 pF, Variable Capacitor, Johanson Gigatrim # 27271SL
C3	0.8–8.0 pF, Variable Capacitor, Johanson Gigatrim # 27291SL
C4, C13	0.1 μF, Chip Capacitor, Kemet # CDR33BX104AKWS
C5, C14	100 pF, B Case Chip Capacitor, ATC # 100B101JCA500X
C6, C8, C11, C15	12 pF, B Case Chip Capacitor, ATC # 100B120JCA500X
C7, C10	1000 pF, B Case Chip Capacitor, ATC # 100B102JCA50X
L1	3 Turns, 27 AWG, 0.087″ OD, 0.050″ ID, 0.053″ Long, 6.0 nH
L2	5 Turns, 27 AWG, 0.087″ OD, 0.050″ ID, 0.091″ Long, 15 nH
L3, L4	9 Turns, 26 AWG, 0.080″ OD, 0.046″ ID, 0.170″ Long, 30.8 nH
L5	4 Turns, 27 AWG, 0.087″ OD, 0.050″ ID, 0.078″ Long, 10 nH
R1, R2, R3	12 Ω, 1/8 W Fixed Film Chip Resistor. Garrett Instruments # RM73B2B120JT
R4, R5, R6	0.08″ x 0.13″. Garrett Instruments # RM73B2B120JT
W1, W2	Berrylium Copper 0.010″ x 0.110″ x 0.210″



Z1	0.624″ x 0.08″ Microstrip	Z7	0.408″ x 0.08″ Microstrip
Z2	0.725″ x 0.08″ Microstrip	Z8	0.990″ x 0.08″ Microstrip
Z3	0.455″ x 0.08″ Microstrip	Z9	0.295″ x 0.08″ Microstrip
Z4	0.530″ x 0.330″ Microstrip	Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55
Z5	0.280″ x 0.330″ Microstrip		
Z6	0.212″ x 0.330″ Microstrip		

Figure 5. Class A Test Circuit Schematic

Table 3. Class A Broadband Component Designations and Values

Designators	Description
B1, B2, B3	Ferrite Bead, Ferroxcube, 56–590–65–3B
C1, C20	470 μF, 63 V, Electrolytic Capacitor, Mallory # SME63V471M12X25L
C2	0.01 μF, B Case Chip Capacitor, ATC # 100B103JCA50X
C3, C10, C15	0.6–4.5 pF, Variable Capacitor, Johanson # 27271SL
C4, C16	0.02 μF, B Case Chip Capacitor, ATC # 100B203JCA50X
C5	100 μF, 50 V, Electrolytic Capacitor, Mallory # SME50VB101M12X256
C6, C7, C9, C14, C17	12 pF, B Case Chip Capacitor, ATC # 100B120JCA500X
C8, C13	51 pF, B Case Chip Capacitor, ATC # 100B510JCA500X
C11, C12	0.3 pF, B Case Chip Capacitor, ATC # 100B0R3CCA500X
C18	0.1 μF, Chip Capacitor, Kemet # CDR33BX104AKWS
C19	0.4–2.5 pF, Variable Capacitor, Johanson # 27285
L1	8 Turns, 0.042″ ID, 24 AWG, Enamel
L2	9 Turns, 0.046″ ID, 26 AWG, Enamel
Q1	NPN, 15 W, Bipolar Transistor, MJD310
Q2	PNP, 15 W, Bipolar Transistor, MJD320
R1	200 Ω, Axial, 1/4 W Resistor
R2	1.0 kΩ, 1/2 W Potentiometer, Bourns
R3	13 kΩ, Axial, 1/4 W Resistor
R4, R6, R7	390 Ω, 1/8 W Chip Resistor, Garrett Instruments # RM73B2B391JT
R5	1.0 Ω, 10 W 1% Resistor, DALE # RE65G1R00
R8, R9, R10	12 Ω, 1/8 W Chip Resistor, Garrett Instruments # RM73B2B120JT
Input/Output	Type N Flange Mount RF55–22, Connectors, Omni–Spectra

TYPICAL CHARACTERISTICS

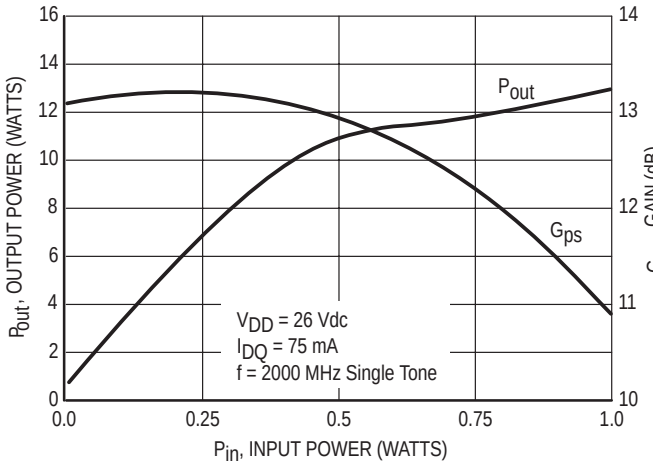


Figure 6. Output Power & Power Gain versus Input Power

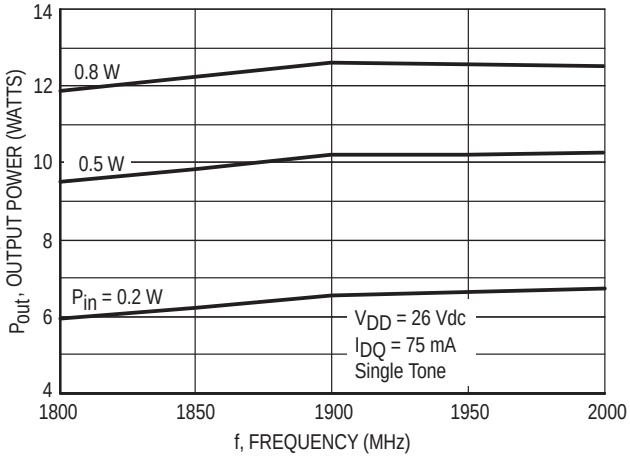


Figure 7. Output Power versus Frequency

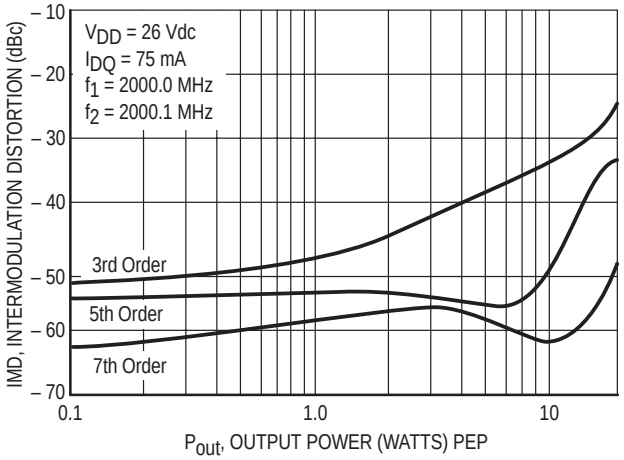


Figure 8. Intermodulation Distortion Products versus Output Power

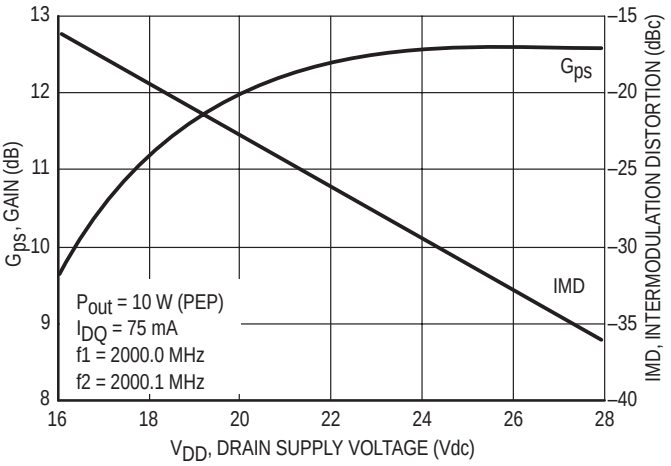


Figure 9. Power Gain and Intermodulation Distortion versus Supply Voltage

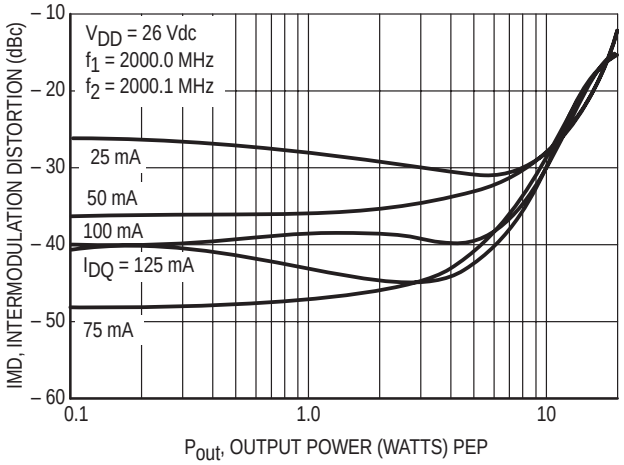


Figure 10. Intermodulation Distortion versus Output Power

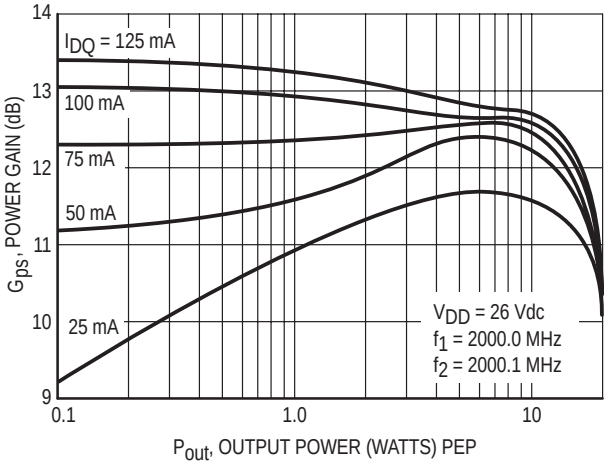


Figure 11. Power Gain versus Output Power

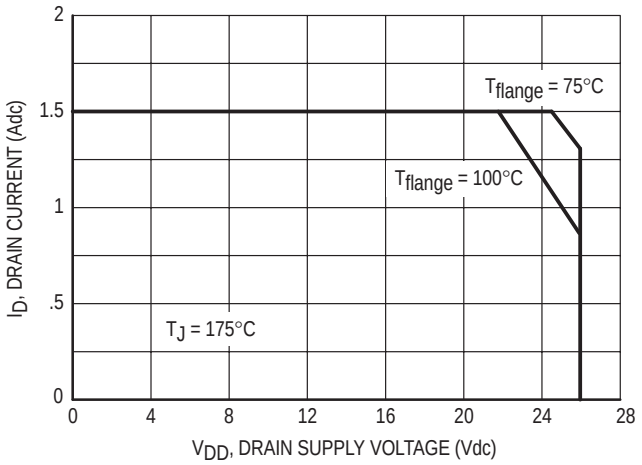


Figure 12. Class A DC Safe Operating Area

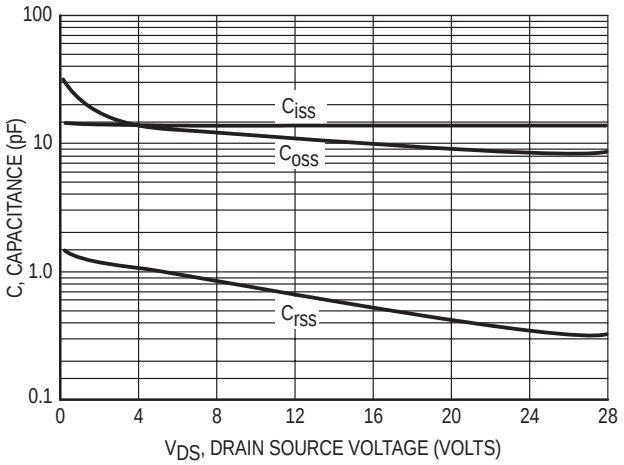


Figure 13. Capacitance versus Drain Source Voltage

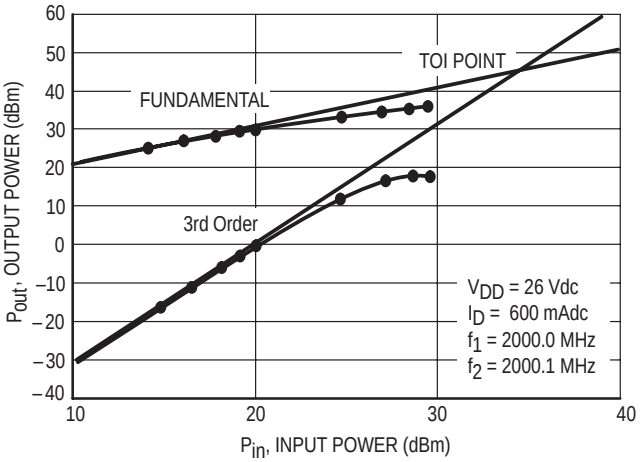


Figure 14. Class A Third Order Intercept Point

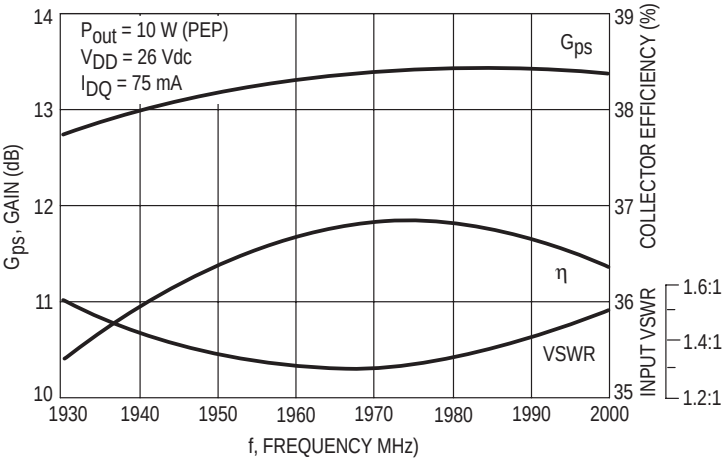
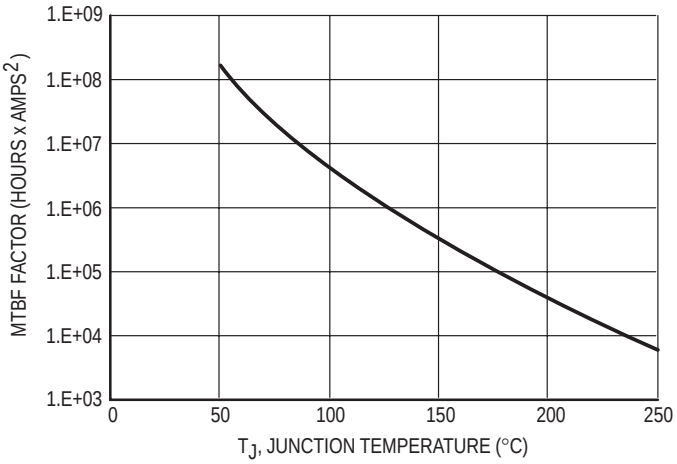
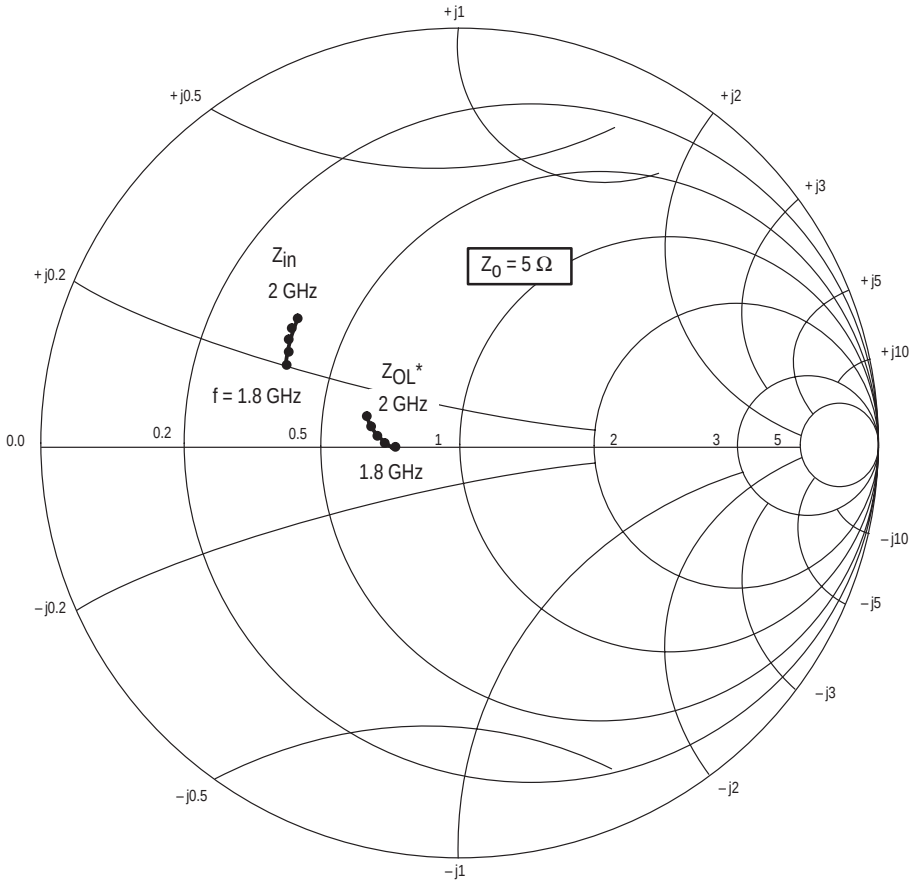


Figure 15. Performance in Broadband Circuit



This graph displays calculated MTBF in hours x ampere^2 drain current. Life tests at elevated temperature have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTBF factor by I_D^2 for MTBF in a particular application.

Figure 16. MTBF Factor versus Junction Temperature



V_{CC} = 26 V, I_{CQ} = 75 mA, P_{out} = 10 W (PEP)

f MHz	$Z_{in}(1)$ Ω	Z_{OL}^* Ω
1800	2.1 + j1.0	3.8 – j0.15
1860	2.05 + j1.15	3.77 – j0.13
1900	2.0 + j1.2	3.75 – j0.1
1960	1.9 + j1.4	3.65 + j0.1
2000	1.85 + j1.6	3.55 + j0.2

$Z_{in}(1)$ = Complex conjugate of source impedance.

Z_{OL}^* = Conjugate of the optimum load impedance at given output power, voltage, IMD, bias current and frequency.

Figure 17. Series Equivalent Input and Output Impedence

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

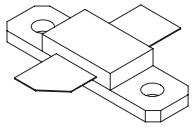
N–Channel Enhancement–Mode Lateral MOSFETs

MRF284
MRF284SR1

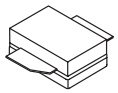
30 W, 2000 MHz, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

Designed for PCN and PCS base station applications at frequencies from 1000 to 2600 MHz. Suitable for FM, TDMA, CDMA, and multicarrier amplifier applications. To be used in class A and class AB for PCN–PCS/cellular radio and wireless local loop.

- Specified Two–Tone Performance @ 2000 MHz, 26 Volts
  Output Power = 30 Watts (PEP)
  Power Gain = 9 dB
  Efficiency = 30%
  Intermodulation Distortion = –29 dBc
- Typical Single–Tone Performance at 2000 MHz, 26 Volts
  Output Power = 30 Watts (CW)
  Power Gain = 9.5 dB
  Efficiency = 45%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 2000 MHz, 30 Watts (CW) Output Power
- MRF284SR1 Is Available in Tape and Reel. R1 Suffix = 500 Units per 12 mm, 7 inch Reel.
- LDMOS Models, Test Fixture, Reference Design and Circuit Board Artwork
  Available at: http://motorola.com/sps/rf/designtds/



CASE 360B–03, STYLE 1
(MRF284)



CASE 360C–03, STYLE 1
(MRF284SR1)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	87.5 0.5	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

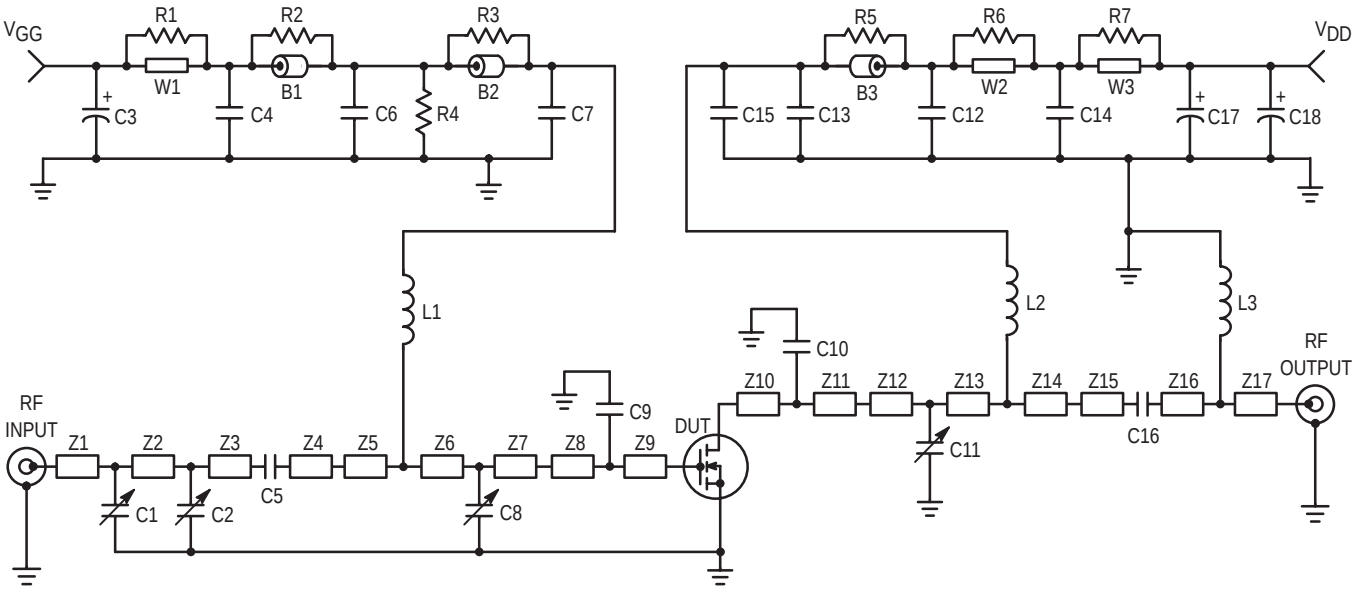
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1.0	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	10	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 150 μAdc)	$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 200 mAdc)	$V_{GS(q)}$	3.0	4.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$V_{DS(on)}$	—	0.3	0.6	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1.0 Adc)	g_{fs}	—	1.5	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	43	—	pF
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	23	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	1.4	—	pF
FUNCTIONAL TESTS (in Motorola Test Fixture)					
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W, I_{DQ} = 200 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	G_{ps}	9	10.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W, I_{DQ} = 200 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	η	30	35	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W, I_{DQ} = 200 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	IMD	—	–32	–29	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W, I_{DQ} = 200 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	IRL	9	15	—	dB
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 200 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	G_{ps}	9	10.4	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 200 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	η	—	35	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 200 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IMD	—	–34	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 200 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IRL	9	15	—	dB
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 200 mA, f1 = 2000.0 MHz)	G_{ps}	8.5	9.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 200 mA, f1 = 2000.0 MHz)	η	35	45	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 200 mA, f1 = 2000.0 MHz, VSWR = 10:1, at All Phase Angles)	Ψ	No Degradation In Output Power			



Z1	0.530″ x 0.080″ Microstrip	Z11	0.155″ x 0.515″ Microstrip
Z2	0.255″ x 0.080″ Microstrip	Z12	0.120″ x 0.325″ Microstrip
Z3	0.600″ x 0.080″ Microstrip	Z13	0.150″ x 0.325″ Microstrip
Z4	0.525″ x 0.080″ Microstrip	Z14	0.010″ x 0.325″ Microstrip
Z5	0.015″ x 0.325″ Microstrip	Z15	0.505″ x 0.080″ Microstrip
Z6	0.085″ x 0.325″ Microstrip	Z16	0.865″ x 0.080″ Microstrip
Z7	0.165″ x 0.325″ Microstrip	Z17	0.525″ x 0.080″ Microstrip
Z8	0.110″ x 0.515″ Microstrip	Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55
Z9	0.095″ x 0.515″ Microstrip		
Z10	0.050″ x 0.515″ Microstrip		

Figure 1. 1.93–2.0 GHz Broadband Test Circuit Schematic

Table 1. 1.93 – 2.0 GHz Broadband Component Designations and Values

Designators	Description
B1 – B3	Ferrite Bead, Round, Ferroxcube # 56–590–65–3B
C1, C2, C8	0.8–8.0 pF Gigatrim Variable Capacitors, Johanson # 27291SL
C3, C17	22 μF, 35 V Tantalum Surface Mount Chip Capacitor, Kemet # T491X226K035AS4394
C4, C14	0.1 μF Chip Capacitor, Kemet # CDR33BX104AKWS
C5	220 pF B Case RF Chip Capacitor, ATC # 100B221KP500X
C6, C12	1000 pF B Case RF Chip Capacitor, ATC # 100B102JCA50X
C7, C13	5.1 pF B Case RF Chip Capacitor, ATC # 100B5R1CCA500X
C9	1.2 pF B Case RF Chip Capacitor, ATC # 100B1R2CCA500X
C10	2.7 pF B Case RF Chip Capacitor, ATC # 100B2R7CCA500X
C11	0.6–4.5 pF Gigatrim Variable Capacitors, Johanson # 27271SL
C15, C16	200 pF B Case RF Chip Capacitor, ATC # 100B201KP500X
C18	10 μF, 35 V Tantalum Surface Mount Chip Capacitor, Kemet # T495X106K035AS4394
L1, L2	4 Turns, #24 AWG, 0.120″ OD, 0.140″ Long, (12.5 nH), Coilcraft # A04T–5
L3	2 Turns, #24 AWG, 0.120″ OD, 0.140″ Long, (5.0 nH), Coilcraft # A02T–5
R1, R2, R3, R5, R6, R7	12 Ω, 1/4 W Chip Resistor 0.08″ x 0.13″, Garrett Instruments # RM73B2B120JT
R4	560 kΩ, 1/4 W Chip Resistor 0.08″ x 0.13″
W1, W2, W3	Solid Copper Buss Wire, 16 AWG
WS1, WS2	Berrylium Copper Wear Blocks 0.005″ x 0.250″ x 0.250″
	Brass Banana Jack and Nut
	Red Banana Jack and Nut
	Green Banana Jack and Nut
	Type “N” Jack Connectors, Omni–Spectra # 3052–1648–10
	4–40 Ph Head Screws, 0.125″ Long
	4–40 Ph Head Screws, 0.188″ Long
	4–40 Ph Head Screws, 0.312″ Long
	4–40 Ph Rec. Hd. Screws, 0.438″ Long
RF Circuit Board	3″ x 5″ Copper Clad PCB, Glass Teflon®

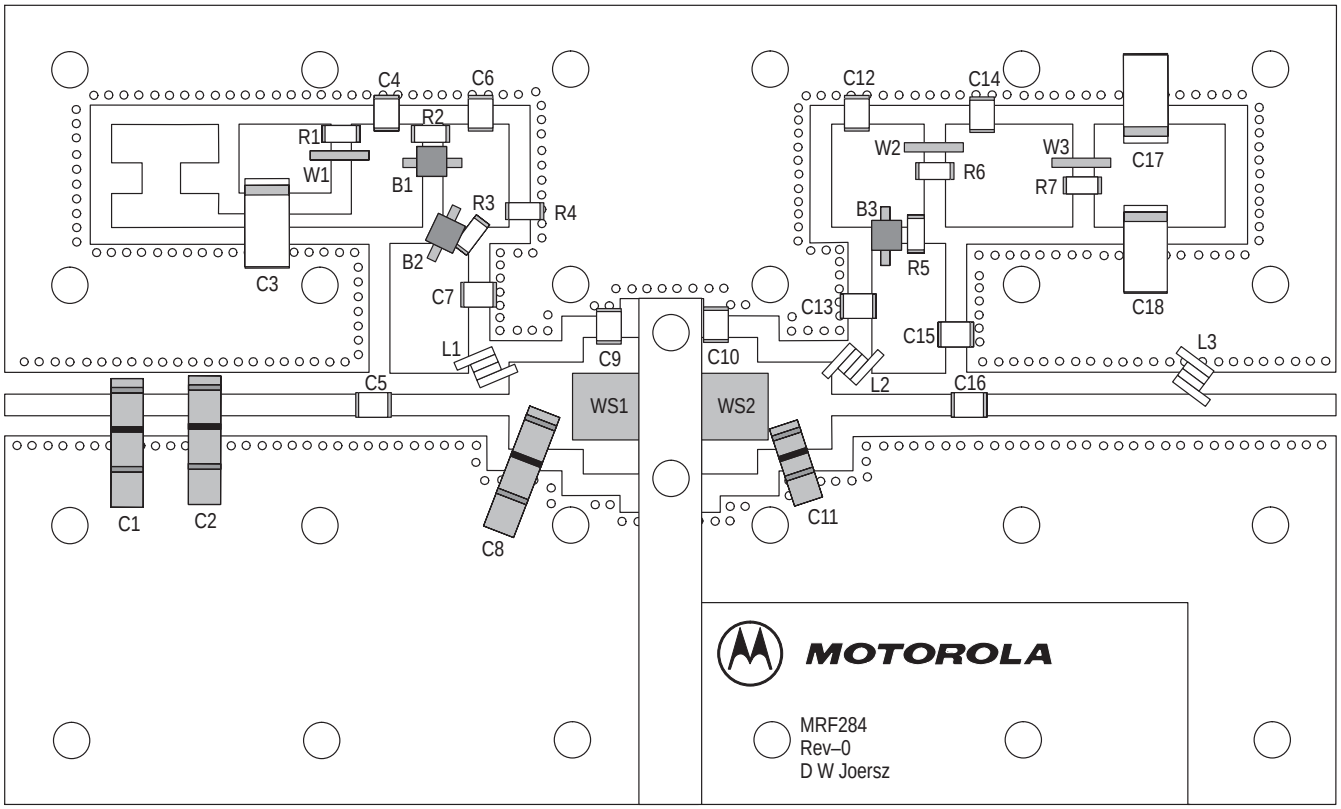
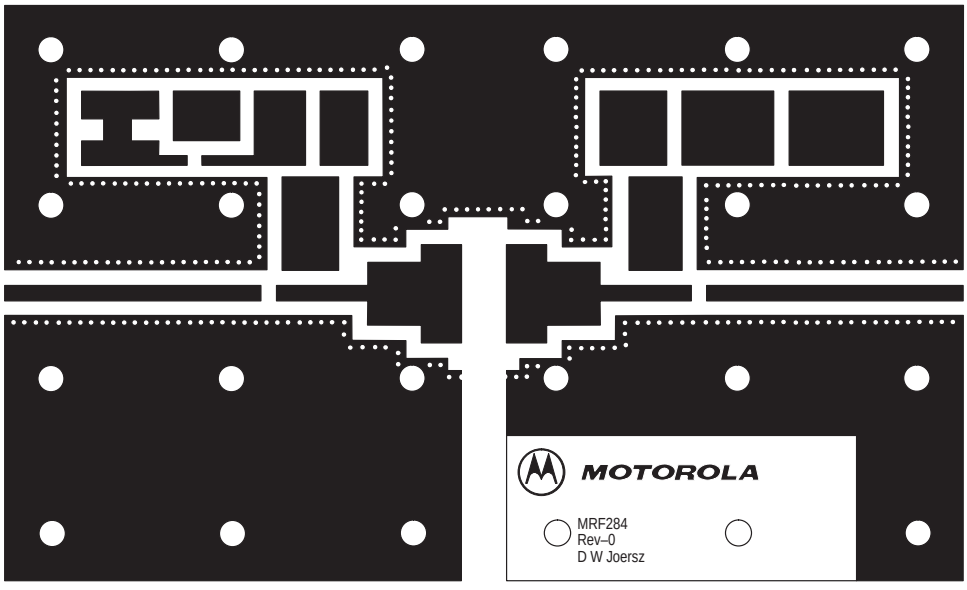
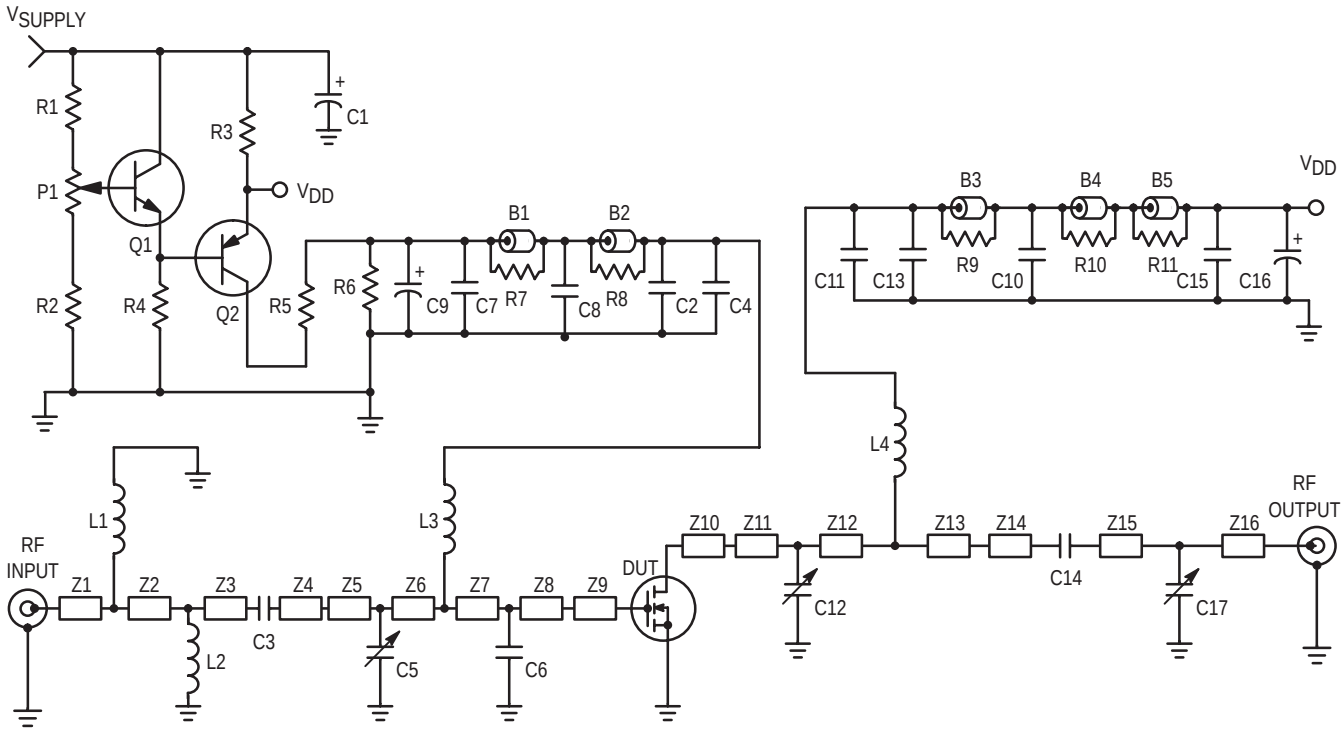


Figure 2. 1.93–2.0 GHz Broadband Test Circuit Component Layout



(Scale 1:1)

Figure 3. MRF284 Test Circuit Photomaster
(Reduced 18% in printed data book, DL110/D)



Z1	0.363″ x 0.080″ Microstrip	Z11	0.235″ x 0.325″ Microstrip
Z2	0.080″ x 0.080″ Microstrip	Z12	0.02″ x 0.325″ Microstrip
Z3	0.916″ x 0.080″ Microstrip	Z13	0.02″ x 0.325″ Microstrip
Z4	0.517″ x 0.080″ Microstrip	Z14	0.510″ x 0.080″ Microstrip
Z5	0.050″ x 0.325″ Microstrip	Z15	0.990″ x 0.080″ Microstrip
Z6	0.050″ x 0.325″ Microstrip	Z16	0.390″ x 0.080″ Microstrip
Z7	0.071″ x 0.325″ Microstrip	Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55
Z8	0.125″ x 0.325″ Microstrip		
Z9	0.210″ x 0.515″ Microstrip		
Z10	0.210″ x 0.515″ Microstrip		

Figure 4. 2.0 GHz Class A Test Circuit Schematic

Table 2. 2.0 GHz Class A Component Designations and Values

Designators	Description
B1 – B5	Ferrite Bead, Round, Ferroxcube # 56–590–65–3B
C1, C9, C16	100 μF, 50 V, Electrolytic Capacitor, Mallory # SME50VB101M12X25L
C2, C13	51 pF, ATC RF Chip Capacitors, Case “B” # 100B510JCA500x
C3, C14	10 pF, ATC RF Chip Capacitors, Case “B” # 100B100JCA500X
C4, C11	12 pF, ATC RF Chip Capacitors, Case “B” # 100B120JCA500X
C5	0.8 – 8.0 pF Variable Capacitor, Johansen Gigatrim # 27291SL
C6	4.7 pF, ATC RF Chip Capacitor, Case “B” # 100B4R7CCA500X
C7, C15	91 pF, ATC RF Chip Capacitors, Case “B” # 100B910KP500X
C8	1000 pF, ATC RF Chip Capacitor, Case “B” # 100B102JCA50X
C10	0.1 μF, Chip Capacitor, Kemet # CDR33BX104AKWS
C12, C17	0.6 – 4.5 pF, Variable Capacitors, Johansen Gigatrim # 27271SL
L1	4 Turns, #27 AWG, 0.087″ OD, 0.050″ ID, 0.069″ Long, 10 nH
L2	5 Turns, #24 AWG, 0.083″ OD, 0.040″ ID, 0.128″ Long, 12.5 nH
L3, L4	9 Turns, #26 AWG, 0.080″ OD, 0.046″ ID, 0.170″ Long, 30.8 nH
P1	1000 Ω Potentiometer, 1/2 W, 10 Turns, Bourns
Q1	Transistor, NPN, Motorola P/N: MJD31, Case 369A–10
Q2	Transistor, PNP, Motorola P/N: MJD32, Case 369A–10
R1	360 Ω, Fixed Film Chip Resistor 0.08″ x 0.13″, Garrett Instruments # RM73B2B361JT
R2	2 x 12 kΩ, Fixed Film Chip Resistor 0.08″ x 0.13″, Garrett Instruments # RM73B2B122JT
R3	1 Ω, Wirewound, 5 W, 3% Resistor, Dale # RE60G1R00
R4	4 x 6.8 kΩ, Fixed Film Chip Resistor 0.08″ x 0.13″, Garrett Instruments # RM73B2B682JT
R5	2 x 1500 Ω, Fixed Film Chip Resistor 0.08″ x 0.13″, Garrett Instruments # RM73B2B152JT
R6	270 Ω, Fixed Film Chip Resistor 0.08″ x 0.13″, Garrett Instruments # RM73B2B271JT
R7 – R11	12 Ω, Fixed Film Chip Resistor 0.08″ x 0.13″, Garrett Instruments # RM73B2B120JT

TYPICAL CHARACTERISTICS

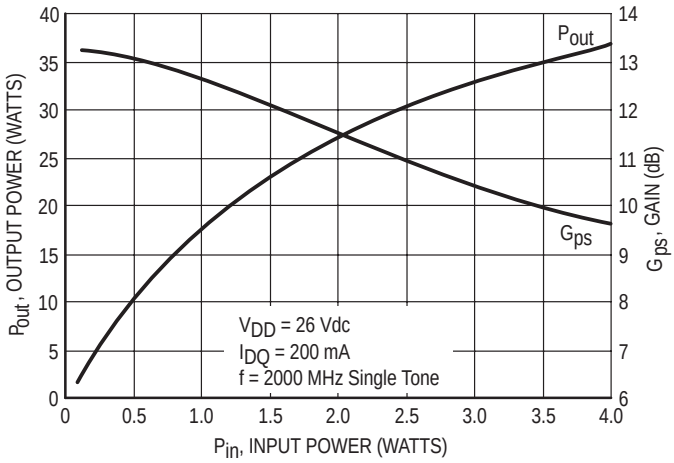


Figure 5. Output Power & Power Gain versus Input Power

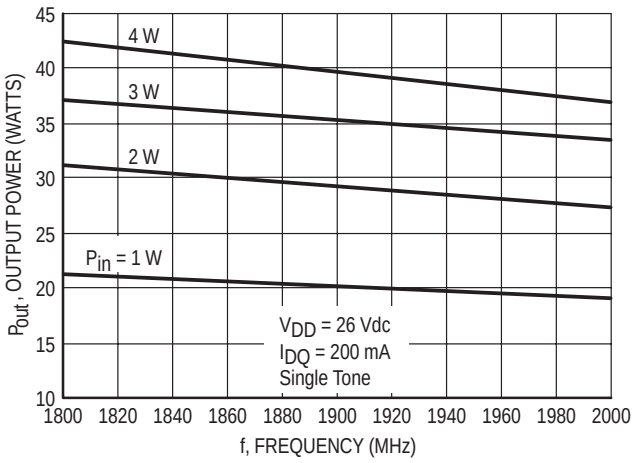


Figure 6. Output Power versus Frequency

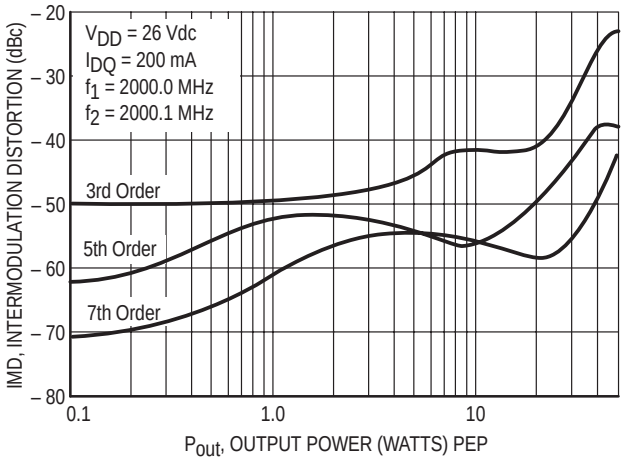


Figure 7. Intermodulation Distortion Products versus Output Power

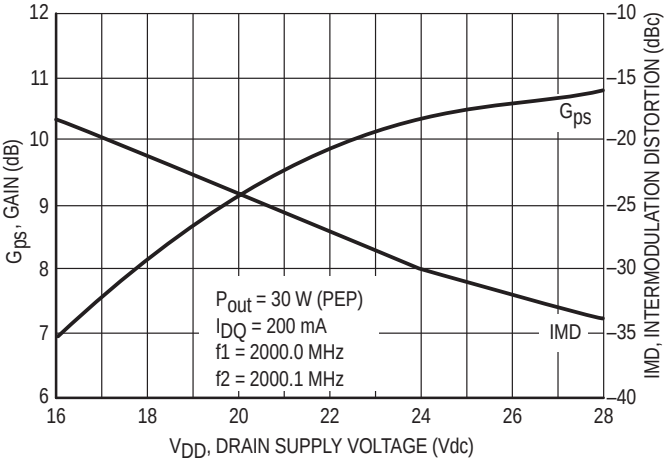


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage

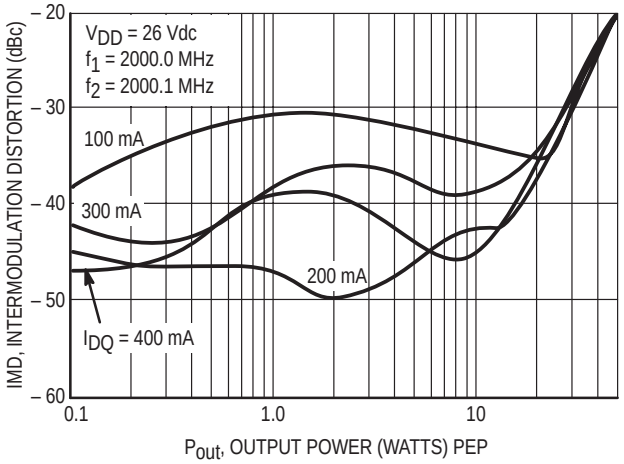


Figure 9. Intermodulation Distortion versus Output Power

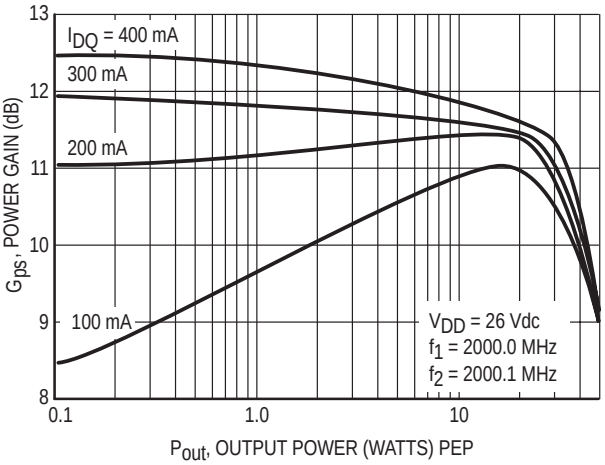


Figure 10. Power Gain versus Output Power

TYPICAL CHARACTERISTICS

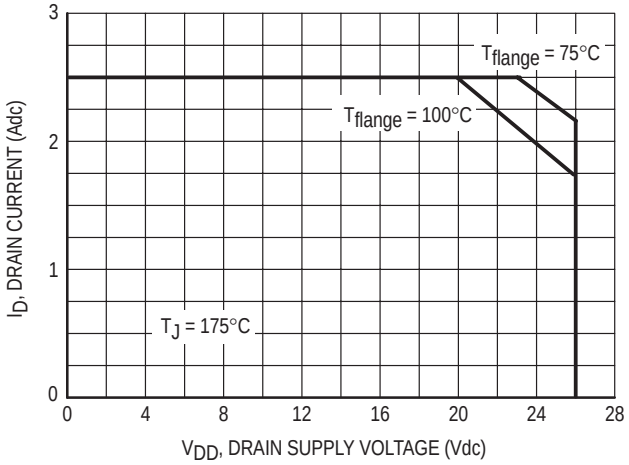


Figure 11. DC Safe Operating Area

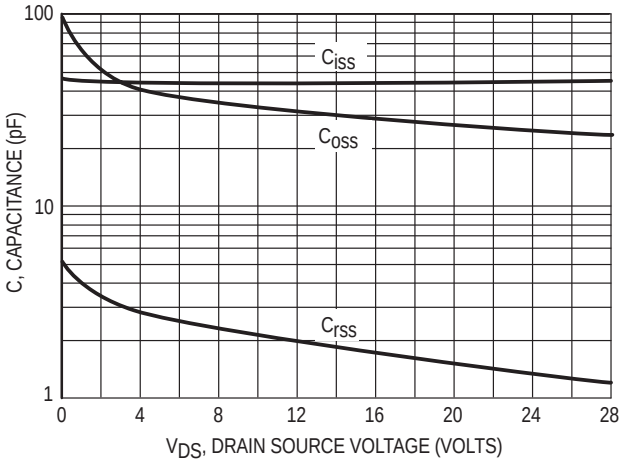


Figure 12. Capacitance versus Drain Source Voltage

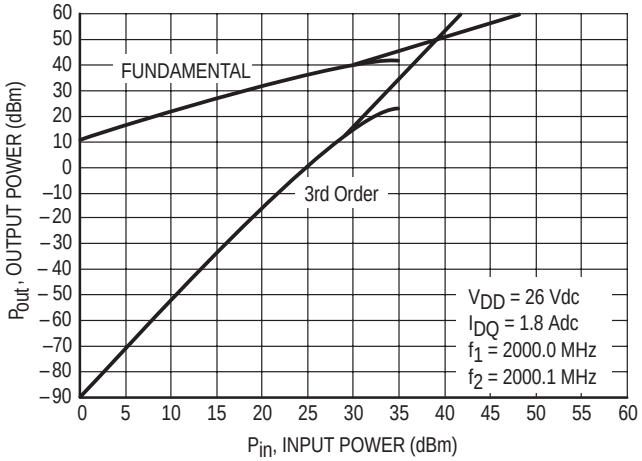


Figure 13. Class A Third Order Intercept Point

TYPICAL CHARACTERISTICS

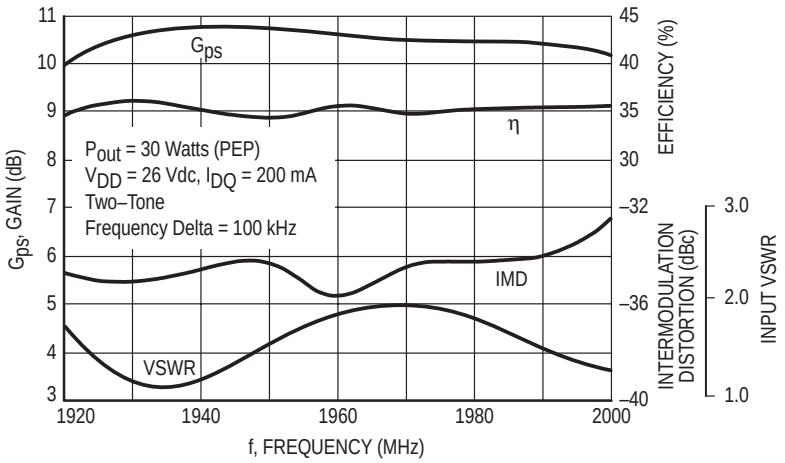
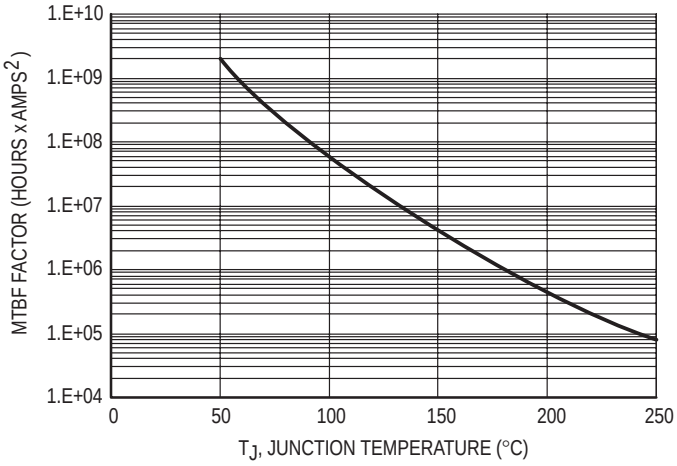
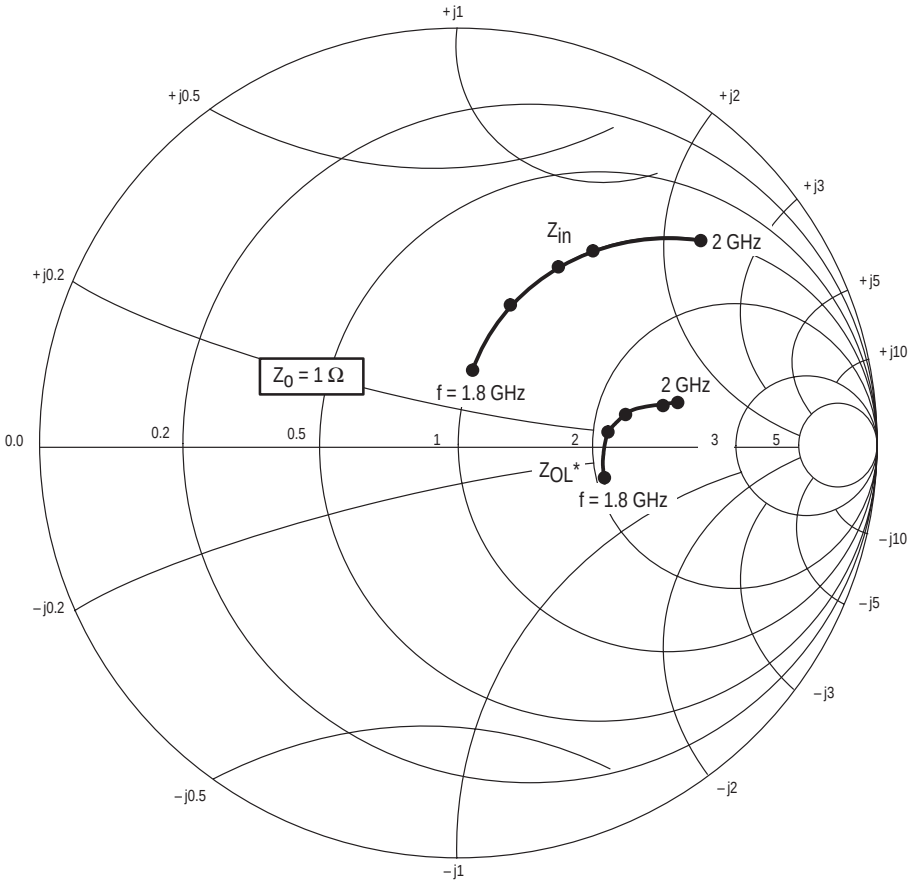


Figure 14. 1.92–2.0 GHz Broadband Circuit Performance



This graph displays calculated MTBF in hours x ampere^2 drain current. Life tests at elevated temperature have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTBF factor by I_D^2 for MTBF in a particular application.

Figure 15. MTBF Factor versus Junction Temperature



V_{CC} = 26 V, I_{CQ} = 200 mA, P_{out} = 15 W_{avg}

f MHz	$Z_{in}(1)$ Ohms	Z_{OL}* Ohms
1800	1.0 + j0.4	2.1 – j0.4
1860	1.0 + j0.8	2.2 + j0.2
1900	1.0 + j1.1	2.3 + j0.5
1960	1.0 + j1.4	2.5 + j0.9
2000	1.0 + j2.3	2.6 + j0.92

$Z_{in}(1)$ = Complex conjugate of source impedance.

Z_{OL}* = Conjugate of the optimum load impedance at given output power, voltage, bias current and frequency.

Figure 16. Series Equivalent Input and Output Impedence

Product Is Not Recommended for New Design.
The next generation of higher performance products are in development. Visit our online Selector Guides (http://mot–sps.com/rf/sg/sg.html) for scheduled introduction dates.

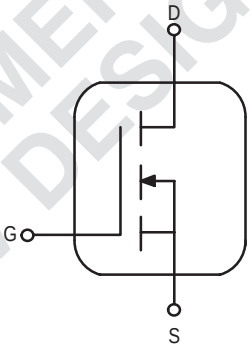
MRF373
MRF373S

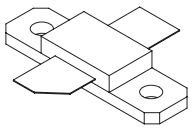
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

60 W, 470 – 860 MHz, 28 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETS

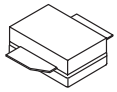
Designed for broadband commercial and industrial applications at frequencies from 470 – 860 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 28 volt transmitter equipment.

- Guaranteed CW Performance at 860 MHz, 28 Volts, Narrowband Fixture
  Output Power – 60 Watts
  Power Gain – 13 dB
  Efficiency – 50%
- Typical Performance at 860 MHz, 28 Volts, Broadband Push–Pull Fixture
  Output Power – 100 Watts (PEP)
  Power Gain – 11.2 dB
  Efficiency – 40%
  IMD – –30 dBc
- Excellent Thermal Stability
- 100% Tested for Load Mismatch Stress at All Phase Angles with 5:1 VSWR @ 28 Vdc, 860 MHz, 60 Watts CW





CASE 360B–03, STYLE 1
(MRF373)



CASE 360C–03, STYLE 1
(MRF373S)

NOT RECOMMENDED FOR NEW DESIGN

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Drain–Source Voltage		V_{DSS}	65	Vdc
Gate–Source Voltage		V_{GS}	±20	Vdc
Drain Current – Continuous		I_D	7	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	MRF373S	P_D	173 1.33	W W/°C
Storage Temperature Range		T_{stg}	– 65 to +150	°C
Operating Junction Temperature		T_J	200	°C

THERMAL CHARACTERISTICS

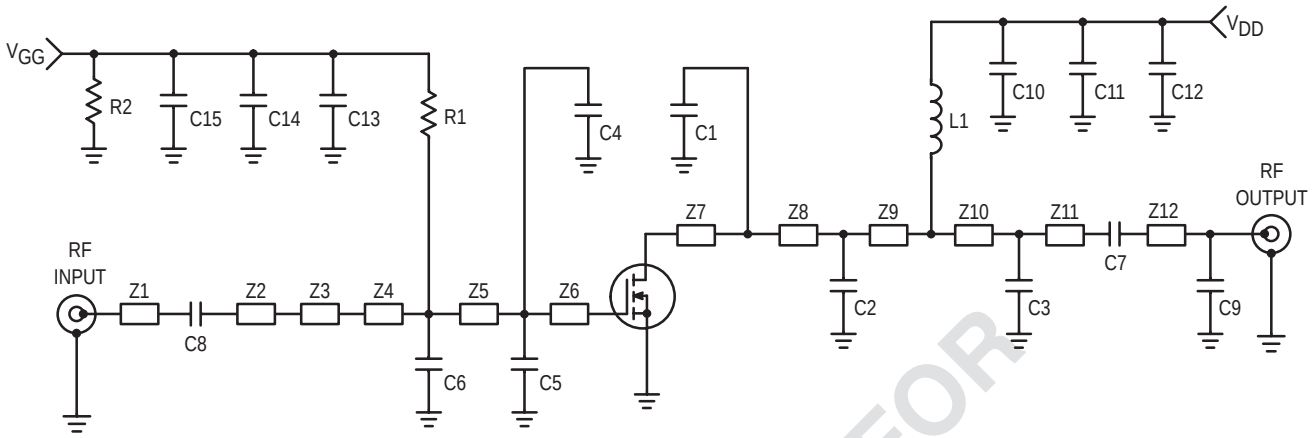
Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Case	MRF373S	$R_{\theta JC}$	0.75	°C/W
Thermal Resistance, Junction to Case	MRF373	$R_{\theta JC}$	1	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D =1 μA)	$V_{(BR)DSS}$	65	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	–	–	1	μAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	–	–	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 200 μA)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 100 mA)	$V_{GS(Q)}$	3	4	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3 A)	$V_{DS(on)}$	–	0.6	0.8	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3 A)	g_{fs}	2.2	2.9	–	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	–	79	–	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	–	46	–	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	–	4	–	pF
FUNCTIONAL CHARACTERISTICS, CW Operation					
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 60 W, I_{DQ} = 200 mA, f = 860 MHz)	G_{ps}	13	14.7	–	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 60 W, I_{DQ} = 200 mA, f = 860 MHz)	η	50	54	–	%
Load Mismatch (V_{DD} = 28 V, P_{out} = 60 W, I_{DQ} = 200 mA, f = 860 MHz, Load VSWR at 5:1 at All Phase Angles)	ψ	No Degradation in Output Power			
TYPICAL CHARACTERISTICS, 2 Tone Operation, Push Pull Configuration (MRF373S), Broadband Fixture					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 100 W PEP, I_{DQ} = 400 mA, f1 = 860.0 MHz, f2 = 866 MHz)	G_{ps}	–	11.2	–	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 100 W PEP, I_{DQ} = 400 mA, f1 = 860.0 MHz, f2 = 866 MHz)	η	–	40	–	%
Third Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 100 W PEP, I_{DQ} = 400 mA, f1 = 860.0 MHz, f2 = 866 MHz)	IMD	–	–30	–	dBc

NOT RECOMMENDED FOR NEW DESIGN



C1	4.7 pF, B Case Chip Capacitor, ATC
C2	15 pF, B Case Chip Capacitor, ATC
C3	6.8 pF, B Case Chip Capacitor, ATC
C4, C5, C6	10 pF, B Case Chip Capacitor, ATC
C7, C8	47 pF, B Case Chip Capacitor, ATC
C9	0.2 pF, B Case Chip Capacitor, ATC
C10, C13	300 pF, B Case Chip Capacitor, ATC, Side Mounted
C11	2) 2.2 μF, 50 V, Kemet P/N C1825C225
C12	22 μF, 50 V, Kemet P/N T491D226K50AS
C14	2) 1.0 μF, 50 V, Kemet P/N C1825C105
C15	10 μF, 35 V, Kemet P/N T491D106K35AS
L1	22 nH, Coilcraft P/N B07T
R1	1.2 kΩ, Vishay Dale Chip Resistor (1206)
R2	12 kΩ, Vishay Dale Chip Resistor (1206)
Connectors	N–Type (female), M/A Com P/N 3052–1648–10
PCB	MRF373 Printed Circuit Board Rev 01, CuClad 250 (GX–0300–55), height 30 mils, ε_r = 2.55
Heatsink	Motorola P/N 95–11LDMOSKPS–1 LDMOS μ250 3″ x 5″ Bedstead
Insert	Motorola P/N 95–11LDMOSKPS–2 Insert for LDMOS μ250 3″ x 5″ Bedstead
End Plates	2) Motorola P/N 93–3MB–9, End Plate for Type–N Connector
Banana Jack and Nut	2) Johnson P/N 108–0904–001
Brass Banana Jack	2) H.H. Smith P/N SM–101

Figure 1. Single–Ended Narrowband Test Circuit Schematic (MRF373)

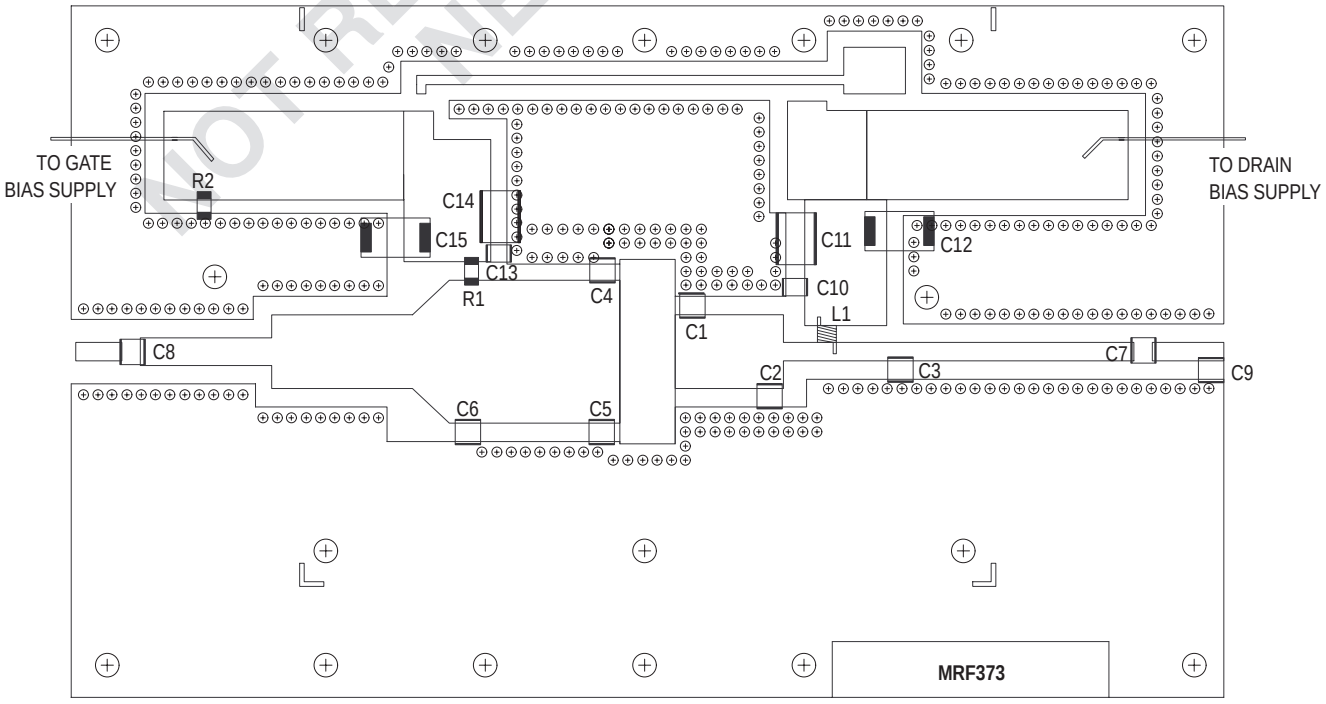


Figure 2. Single–Ended Narrowband Test Circuit Layout (Suitable for Use with MRF373)

NOT RECOMMENDED FOR NEW DESIGN

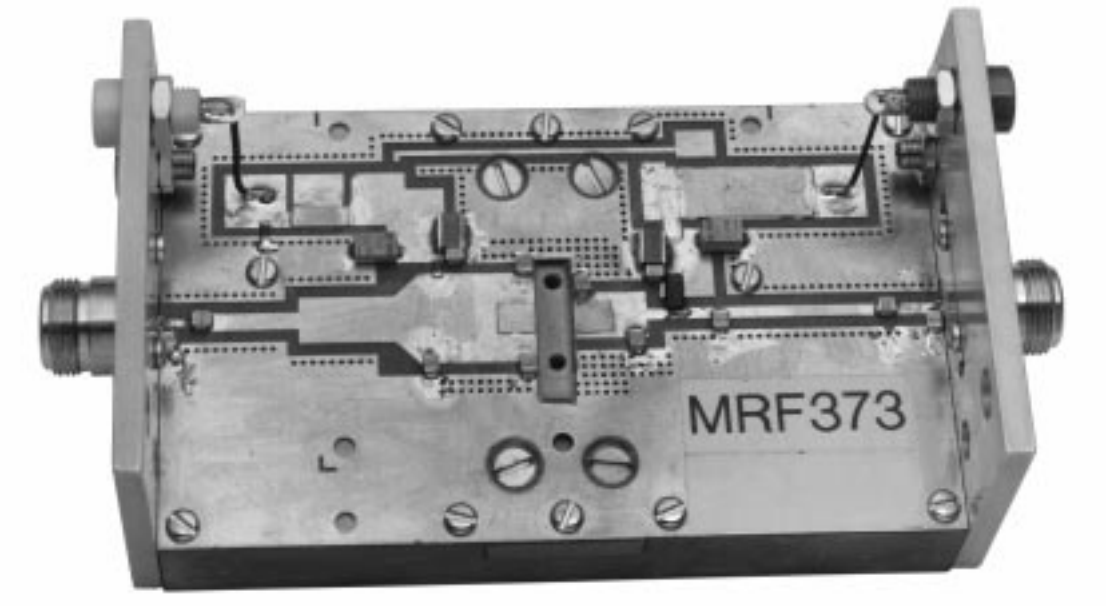
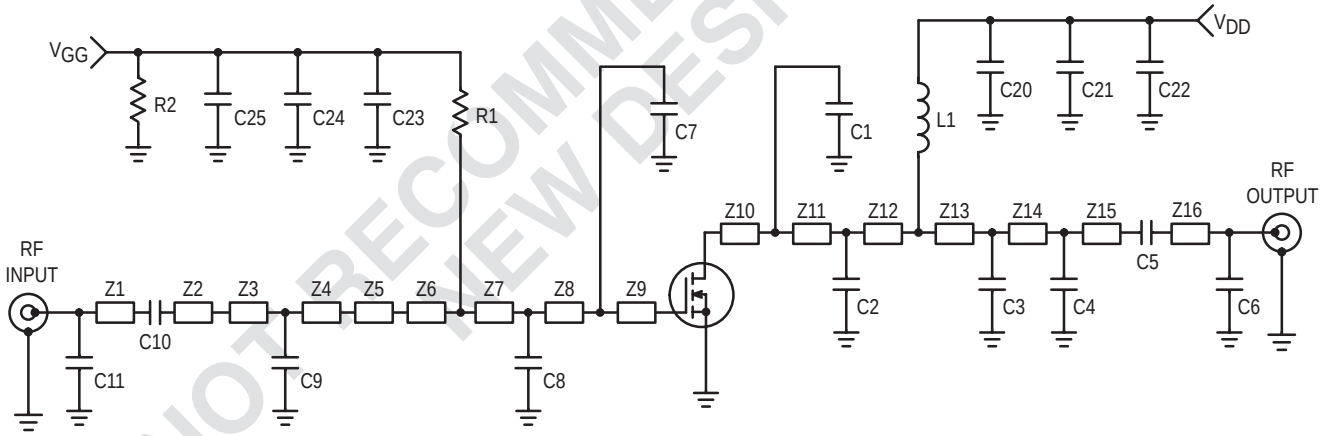


Figure 3. MRF373 Narrowband Test Fixture Photo

NOT RECOMMEND FOR NEW DESIGN



C1, C2	18 pF, B Case Chip Capacitor, ATC
C3	12 pF, B Case Chip Capacitor, ATC
C4, C11	0.8 pF, B Case Chip Capacitor, ATC
C5, C10	68 pF, B Case Chip Capacitor, ATC
C6	0.3 pF, B Case Chip Capacitor, ATC
C7	15 pF, B Case Chip Capacitor, ATC
C8	10 pF, B Case Chip Capacitor, ATC
C9	1.8 pF, B Case Chip Capacitor, ATC
C20, C23	300 pF, B Case Chip Capacitor, ATC, Side Mounted
C21	2) 2.2 μF, 100 V, Vishay P/N VJ3640Y225KXBAT
C24	2) 1.0 μF, 50 V, Kemet P/N C1825C105
C22	22 μF, 35 V, Kemet P/N T491D226K35AS
C25	10 μF, 35 V, Kemet P/N T491D106K35AS
L1	22 nH, Coilcraft P/N B07T
R1	1.2 kΩ, Vishay Dale Chip Resistor (1206)
R2	12 kΩ, Vishay Dale Chip Resistor (1206)

Connectors	N–Type (female), M/A Com P/N 3052–1648–10
PCB	MRF373 Printed Circuit Board Rev 01, CuClad 250 (GX–0300–55), height 30 mils, ε_r = 2.55 (new PCB's available from CMR)
Heatsink	Motorola P/N 95–11LDMOSKPS–1 LDMOS μ250 3″ x 5″ Bedstead
Insert	Motorola P/N 95–11LDMOSKPS–2S Insert for LDMOS μ250S 3″ x 5″ Bedstead
End Plates	2) Motorola P/N 93–3MB–9, End Plate for Type–N Connector
Banana Jack and Nut	2) Johnson P/N 108–0904–001
Brass Banana Jack	2) H.H. Smith P/N SM–101

Figure 4. Single–Ended Narrowband Test Circuit Schematic (MRF373S)

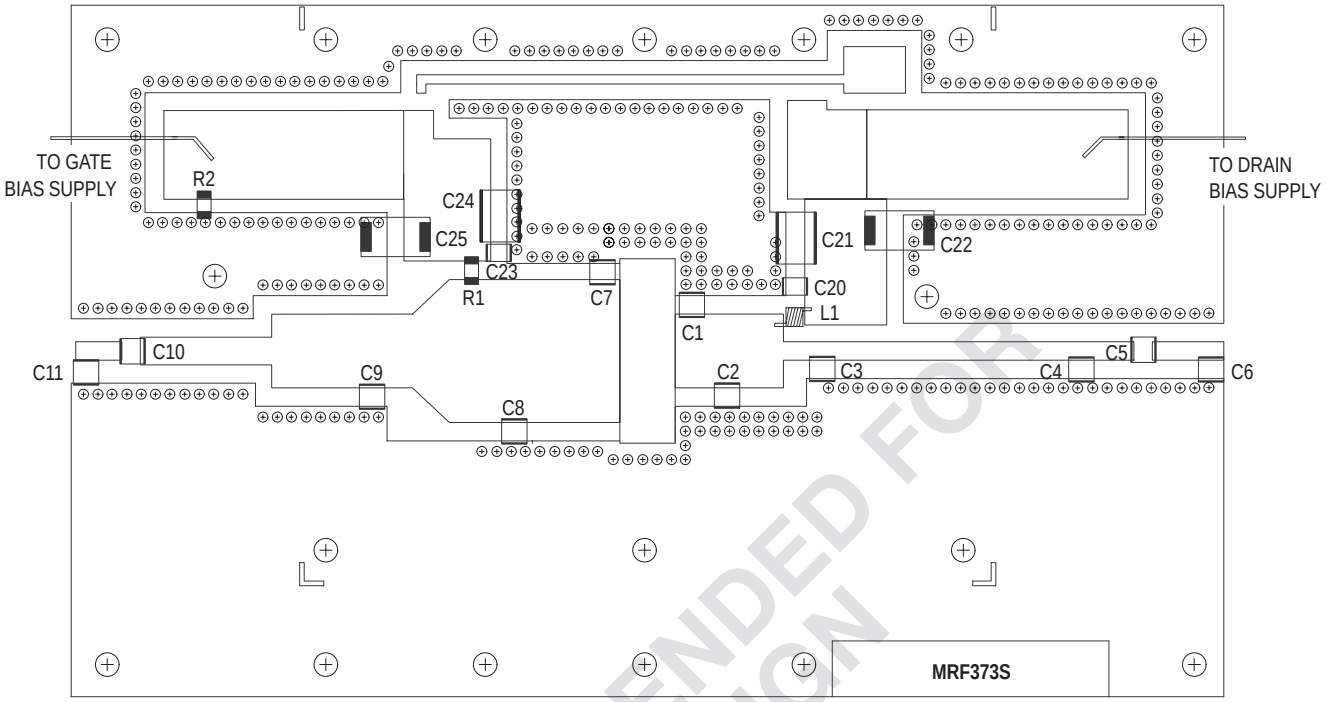


Figure 5. Single–Ended Narrowband Test Circuit Layout (Suitable for Use with MRF373S)

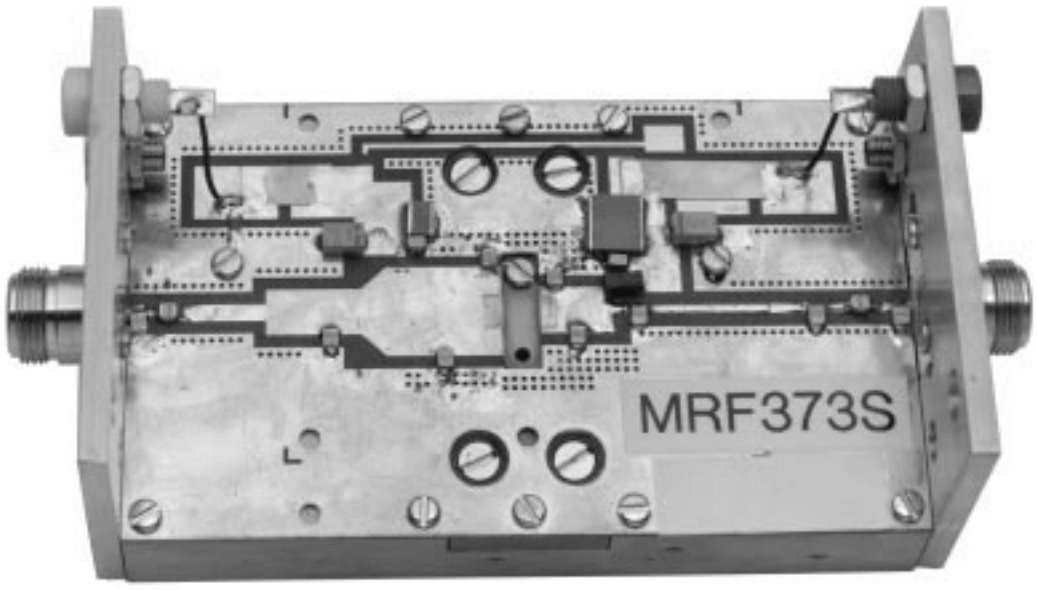


Figure 6. MRF373S Narrowband Test Circuit Photo

TYPICAL CHARACTERISTICS FOR MRF373 IN SINGLE–ENDED FIXTURE

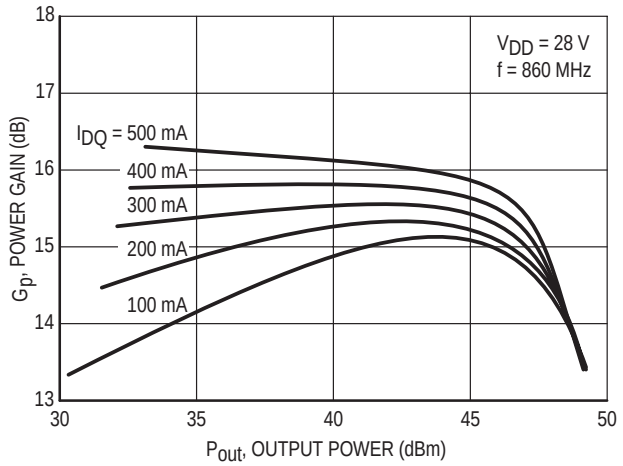


Figure 7. Power Gain versus Output Power

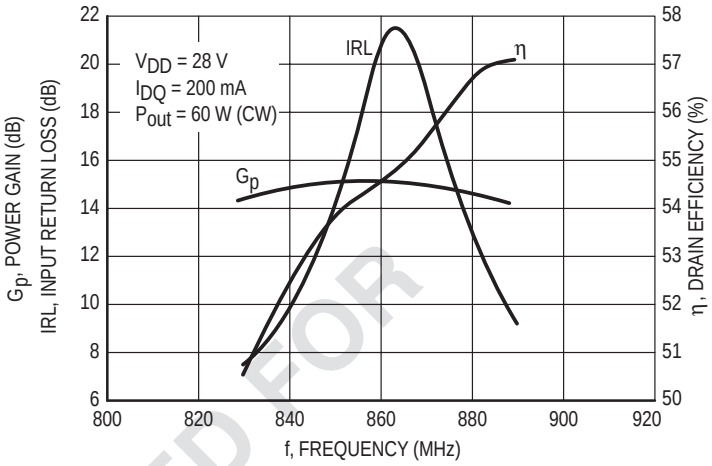


Figure 8. Performance in Narrowband Circuit

NOT RECOMMENDED FOR NEW DESIGN

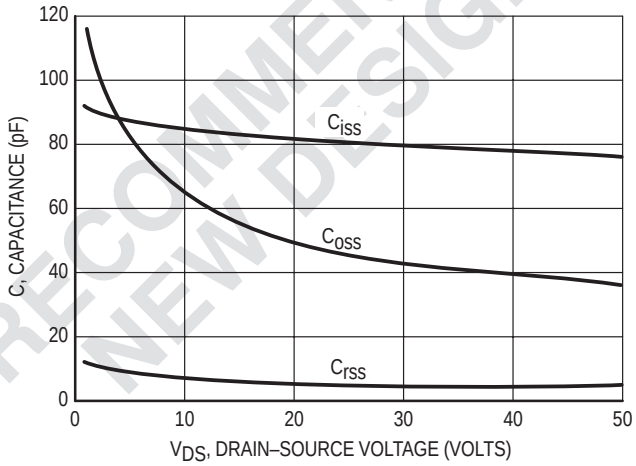
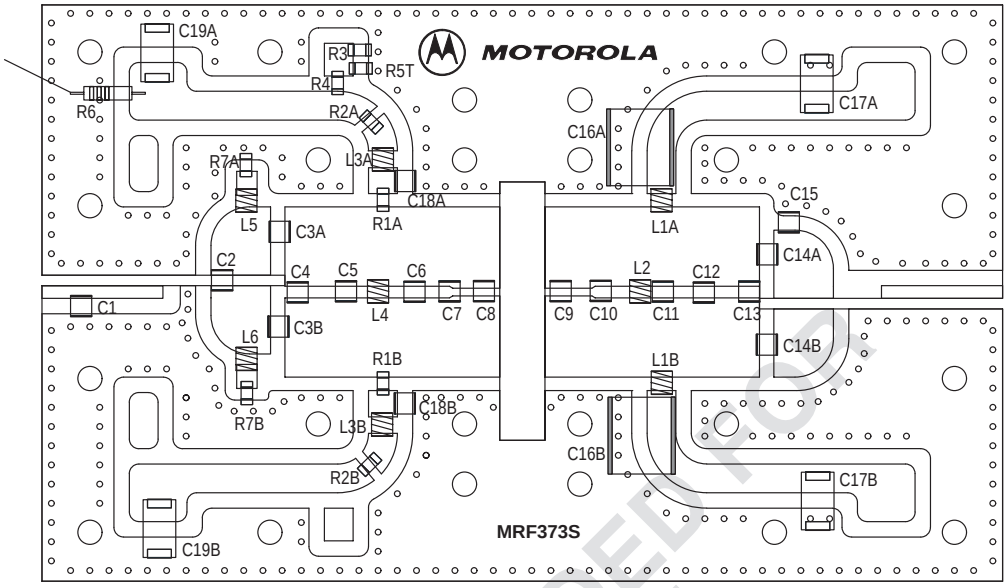


Figure 9. Capacitance versus Voltage

Table 1. Common Source S–Parameters (V_{DS} = 28 V, I_D = 2.0 A)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
400	0.921	182	2.23	52	0.009	39	0.824	184
450	0.922	181	1.95	49	0.009	53	0.832	184
500	0.924	180	1.70	46	0.010	64	0.841	184
550	0.926	179	1.49	42	0.011	72	0.851	183
600	0.929	178	1.31	38	0.013	78	0.860	183
650	0.932	177	1.16	35	0.015	81	0.870	182
700	0.936	176	1.03	31	0.017	82	0.881	182
750	0.940	176	0.93	28	0.019	82	0.892	181
800	0.945	175	0.84	26	0.021	82	0.904	180
850	0.951	174	0.78	24	0.023	80	0.917	180
900	0.957	173	0.72	24	0.025	78	0.929	179



Vertical Balun Mounting Detail

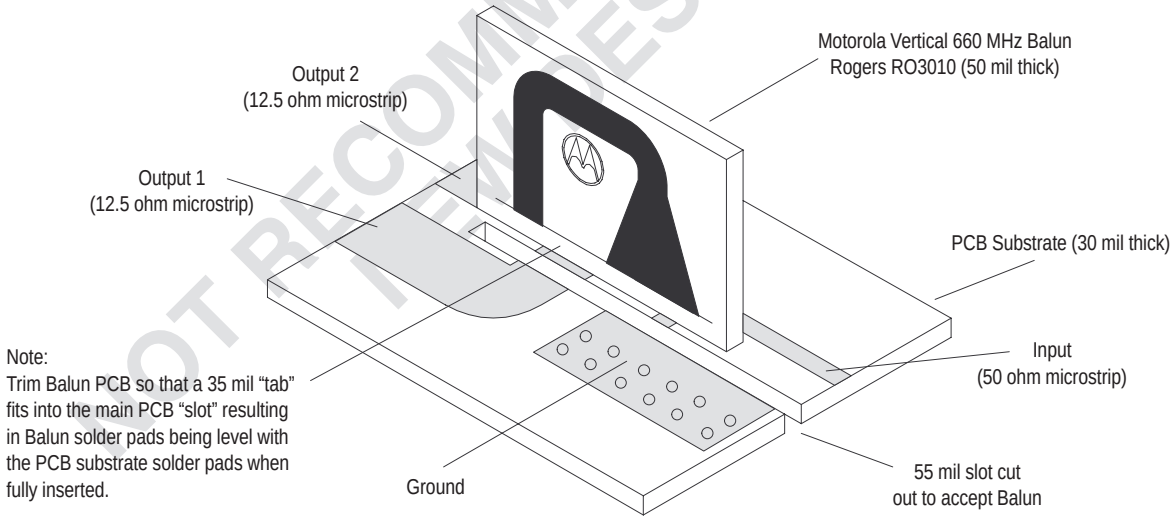


Figure 10. MRF373S Broadband Push–Pull Component Layout

NOT RECOMMENDED FOR NEW DESIGN

Table 2. MRF373S Broadband Push–Pull Application Parts List

Designation	Description
C1	1.0 pF, AVX, P12101J1R0BBT
C2, C4, C10	10 pF, AVX, P12101J100GBT
C3A, B	120 pF, 300 V, AVX, AQ149M121JAJBE
C5, C6, C9	12 pF, AVX, P12101J120GBT
C7, C8	18 pF, AVX, P12101J180GBT
C11	6.8 pF, AVX, P12101J6R8BBT
C12	4.7 pF, AVX, P12101J4R7BBT
C13, C18A, B	3.3 pF, AVX, P12101J3R3BBT
C14A, B	100 pF, 500 V, AVX, AQ147M101JAJBE
C15	2.7 pF, AVX, P12101J2R7BBT
C16A, B	3.3 μF, 100 V, Vitramon P/N VJ3640Y335KXBAT
C17A, B, C19A, B	22 μF, 35 V, Kemet P/N T491D226K35AS
L1A, B, L3A, B, L4, L5	8.0 nH, Coilcraft P/N A03T
L2, L6	12.5 nH, Coilcraft P/N A04T
R1A, B	22 Ω, Vishay Dale Chip Resistor, 1/4 W (1206)
R2A, B	10 Ω, Vishay Dale Chip Resistor, 1/4 W (1206)
R3	390 Ω, Vishay Dale Chip Resistor (1206)
R4	2.4 kΩ, Vishay Dale Chip Resistor (1206)
R5T	470 Ω Thermistor, KOA SPEER MOT P/N 0680149M01
PCB	MRF373 PP Printed Circuit Board Rev 2C, Rogers RO4350, Height 30 mils, ε_r = 3.48
Balun A, B	Vertical 660 MHz Broadband Balun, Printed Circuit Board Rev 01, Rogers RO3010, Height 50 mils, ε_r = 10.2

NOT RECOMMENDED FOR NEW DESIGN

TYPICAL TWO–TONE BROADBAND CHARACTERISTICS

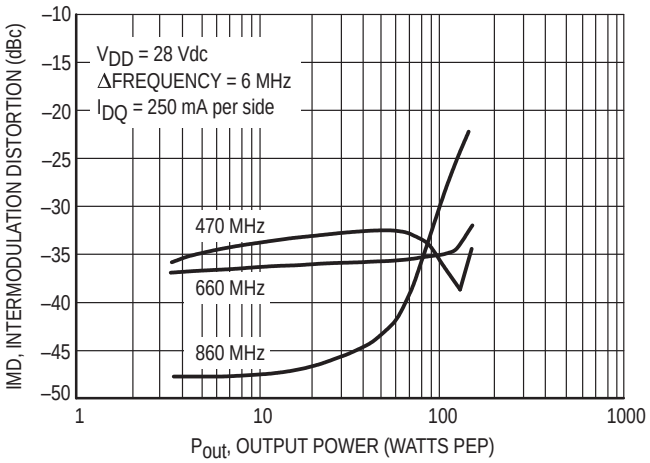


Figure 11. Intermodulation Distortion versus Output Power (MRF373S Broadband Push–Pull Fixture)

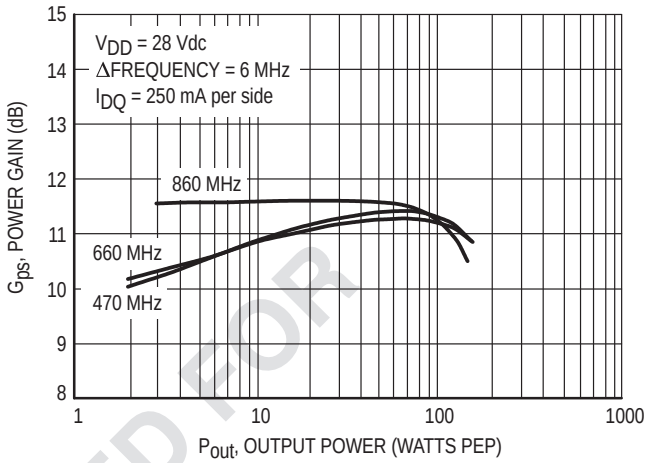


Figure 12. Broadband Power Gain versus Output Power (MRF373S Broadband Push–Pull Fixture)

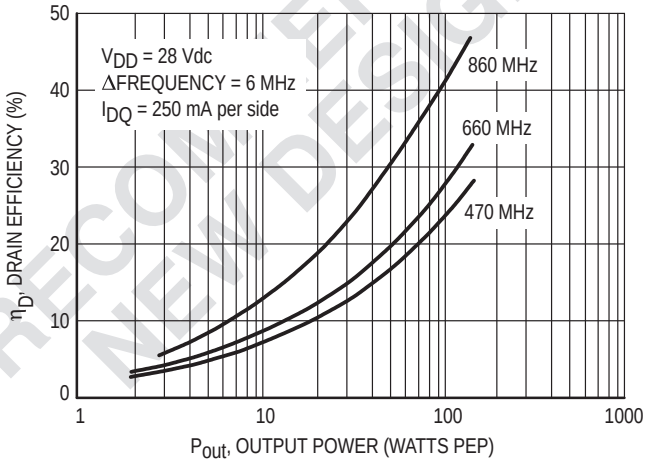


Figure 13. Efficiency versus Output Power (MRF373S Broadband Push–Pull Fixture)

NOT RECOMMENDED FOR NEW DESIGN

Product Is Not Recommended for New Design.
The next generation of higher performance products are in development. Visit our online Selector Guides (http://mot–sps.com/rf/sg/sg.html) for scheduled introduction dates.

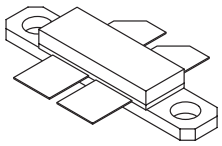
MRF374

The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode Lateral MOSFET

100 W, 470 – 860 MHz, 28 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET

Designed for broadband commercial and industrial applications at frequencies from 470 – 860 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 28 volt transmitter equipment.

- Typical Two–Tone Performance @ 860 MHz, 28 Volts, Narrow-band Fixture
  Output Power – 100 Watts PEP
  Power Gain – 13.5 dB
  Efficiency – 36%
  IMD – –31 dBc
- Typical Performance at 860 MHz, 28 Volts, Broadband Fixture
  Output Power – 100 Watts PEP
  Power Gain – 12 dB
  Efficiency – 36%
  IMD – –34 dBc
- 100% Tested for Load Mismatch Stress at All Phase Angles with
  5:1 VSWR @ 28 Vdc, 860 MHz, 100 Watts CW
- Excellent Thermal Stability
- Characterized with Differential Large–Signal Impedance Parameters



CASE 375F–02, STYLE 1

NOT RECOMMENDED FOR NEW DESIGN

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current – Continuous (per Side)	I_D	7	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	350 1.25	W W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

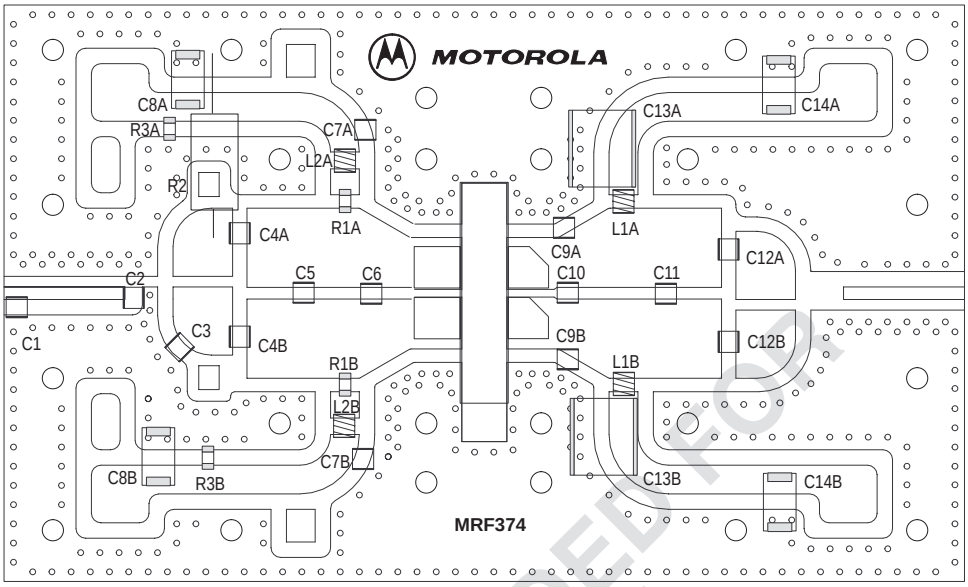
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (per Side) (V_{GS} = 0 V, I_D =1 μA per Side)	$V_{(BR)DSS}$	65	–	–	Vdc
Zero Gate Voltage Drain Current (per Side) (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	–	–	1	μAdc
Gate–Source Leakage Current (per Side) (V_{GS} = 20 V, V_{DS} = 0 V)	I_{GSS}	–	–	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (per Side) (V_{DS} = 10 V, I_D = 200 μA per Side)	$V_{GS(th)}$	2	3.5	4	Vdc
Gate Quiescent Voltage (per Side) (V_{DS} = 28 V, I_D = 100 mA per Side)	$V_{GS(Q)}$	3	4.2	5	Vdc
Drain–Source On–Voltage (per Side) (V_{GS} = 10 V, I_D = 3 A per Side)	$V_{DS(on)}$	–	0.56	0.8	Vdc
Forward Transconductance (per Side) (V_{DS} = 10 V, I_D = 3 A per Side)	g_{fs}	2.2	2.8	–	S
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (per Side) (V_{DS} = 28 V, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	–	80	–	pF
Output Capacitance (per Side) (V_{DS} = 28 V, V_{GS} = 0 V, f = 1 MHz)	C_{oss}	–	45	–	pF
Reverse Transfer Capacitance (per Side) (V_{DS} = 28 V, V_{GS} = 0 V, f = 1 MHz)	C_{rss}	–	3.5	–	pF
FUNCTIONAL CHARACTERISTICS, TWO–TONE TESTING (2)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 100 W PEP, I_{DQ} = 400 mA, f1 = 857 MHz, f2 = 863 MHz)	G_{ps}	12.5	13.5	–	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 100 W PEP, I_{DQ} = 400 mA, f1 = 857 MHz, f2 = 863 MHz)	η	30	36	–	%
Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 100 W PEP, I_{DQ} = 400 mA, f1 = 857 MHz, f2 = 863 MHz)	IMD	–28	–31	–	dB
Load Mismatch (V_{DD} = 28 Vdc, P_{out} = 100 W CW, I_{DQ} = 400 mA, f = 860 MHz, VSWR 5:1 at All Phase Angles of Test)		No Degradation in Output Power			
TYPICAL TWO–TONE BROADBAND					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 100 W PEP, I_{DQ} = 500 mA, f1 = 857 MHz, f2 = 863 MHz)	G_{ps}	–	12	–	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 100 W PEP, I_{DQ} = 500 mA, f1 = 857 MHz, f2 = 863 MHz)	η	–	36	–	%
Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 100 W PEP, I_{DQ} = 500 mA, f1 = 857 MHz, f2 = 863 MHz)	IMD	–	– 34	–	dB

(1) Each side of device measured separately.
(2) Measured in push–pull configuration.

NOT RECOMMENDED FOR NEW DESIGN



Vertical Balun Mounting Detail

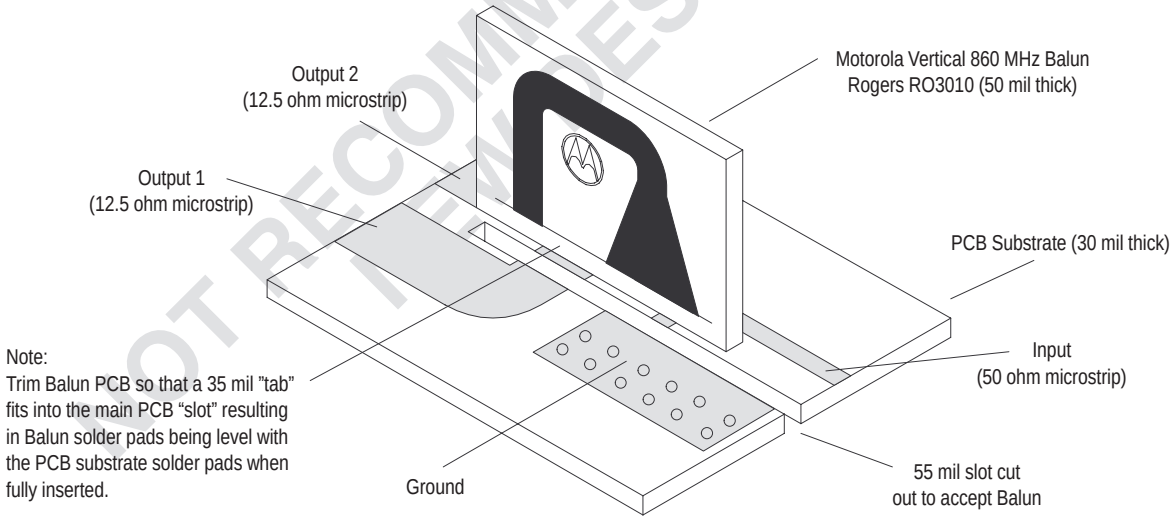


Figure 1. Narrowband Component Layout

NOT RECOMMENDED FOR NEW DESIGN

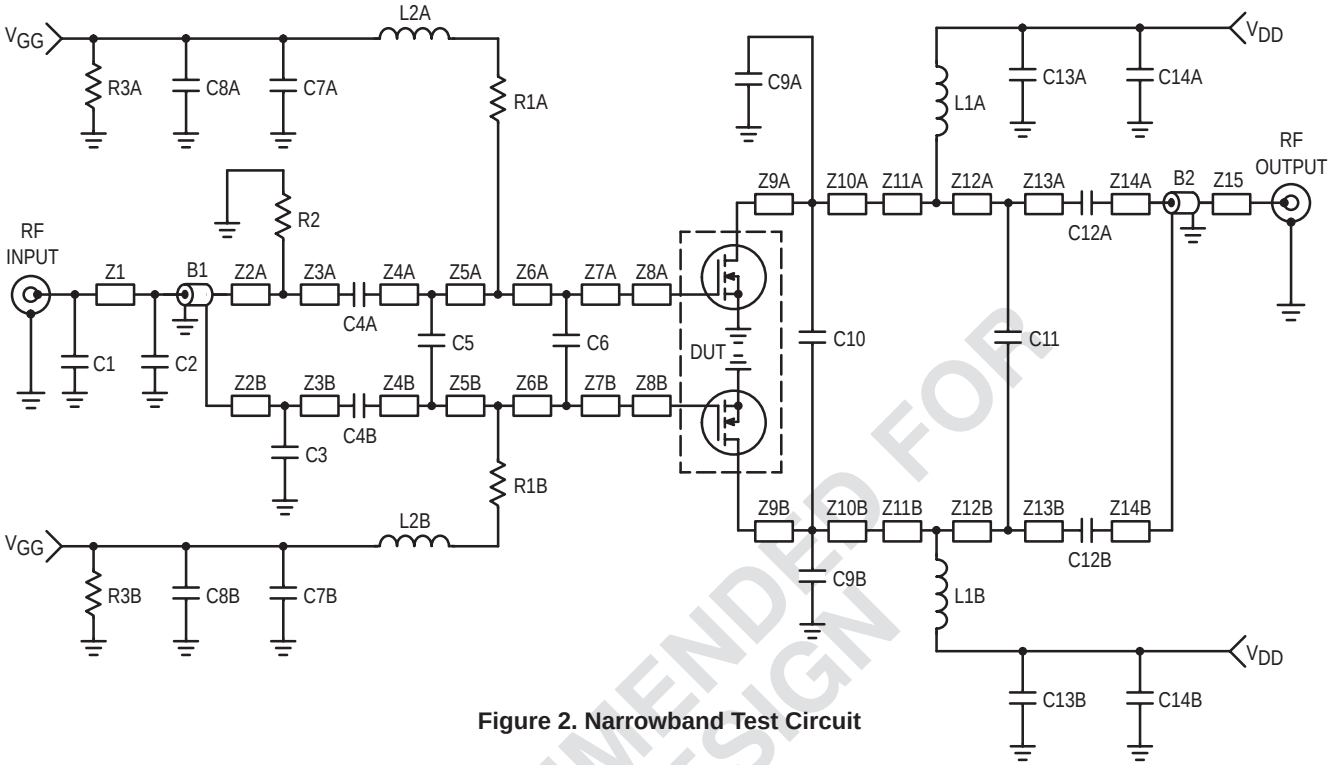


Figure 2. Narrowband Test Circuit

Table 1. Narrowband Component Designations and Values

Designation	Description
C1	0.3 pF, ATC, Case B
C2	3.0 pF, ATC, Case B
C3, C5	1.8 pF, ATC, Case B
C4A, B, C12A, B	47 pF, ATC, Case B
C6	10 pF, ATC, Case B
C7A, B	68 pF, ATC, Case B
C8A, B	10 μF, 35 V Kemet P/N T491D106K35AS
C9A, B	15 pF, ATC, Case B
C10	5.6 pF, ATC, Case B
C11	5.1 pF, ATC, Case B
C12	3.0 pF, ATC, Case B
C13A, B	2.2 μF, 100 V, Vishay P/N VJ3640Y225KXBAT
C14A, B	22 μF, 35 V Kemet P/N T491D226K35AS
L1A, B	5.0 nH, Coilcraft P/N A02T
L2A, B	8.0 nH, Coilcraft P/N A03T
R1A, B	180 Ω, Vishay Dale Chip Resistor, 1/4 W (1210)
R2	10 Ω, Dale Axial Carbon Resistor, 1 W
R3A, B	3.3 kΩ, Vishay Dale Chip Resistor (1206)
PCB	MRF374 Printed Circuit Board Rev 03, Rogers RO4350, Height 30 mils, ε_r = 3.48
Balun B1A, B	860 MHz Vertical Balun, 4:1 Impedance Translation (i.e., 12.5 Ω : 50 Ω), Printed Circuit Board Rev 01, Rogers RO3010, Height 50 mils, ε_r = 10.2
Connectors	N–Type (female), M/A–Com P/N 3052–1648–10
Heatsink	Motorola P/N 99–1RH–2C 3″ X 5″ Bedstead
Insert	Motorola P/N 99–7RI–1D Insert for LDMOS μ650 in 3″ X 5″ Bedstead
Protective Cover	Motorola P/N 99–2PC–2B
End Plates	2) Motorola P/N 94–7GB–1EPL, End Plate for Type–N Connector
Banana Jack and Nut	2) Johnson P/N 108–0904–001
Brass Banana Jack	2) H.H. Smith P/N SM–101

NOT RECOMMENDED FOR NEW DESIGN

TYPICAL TWO–TONE NARROWBAND CHARACTERISTICS

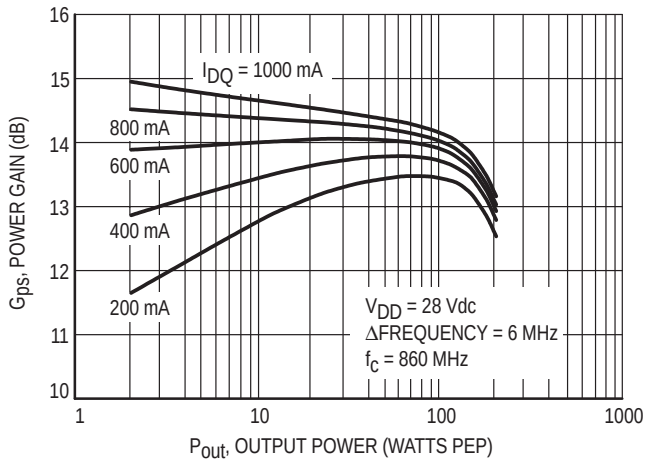


Figure 3. Power Gain versus Peak Output Power

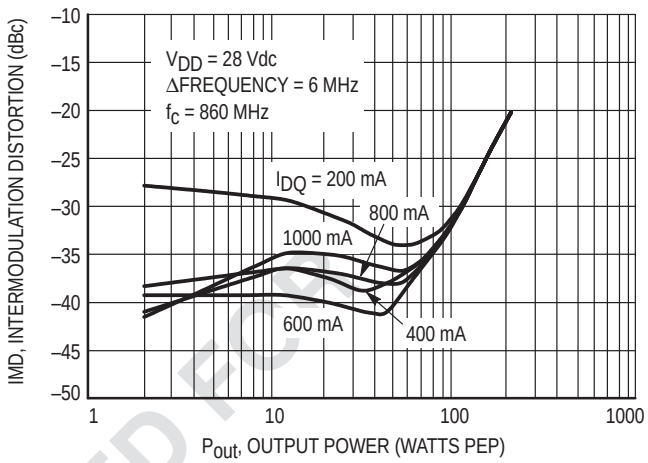


Figure 4. Intermodulation Distortion versus Peak Output Power

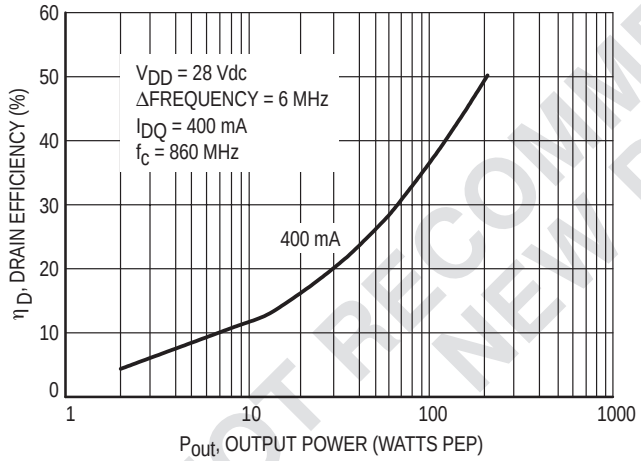


Figure 5. Drain Efficiency versus Peak Output Power

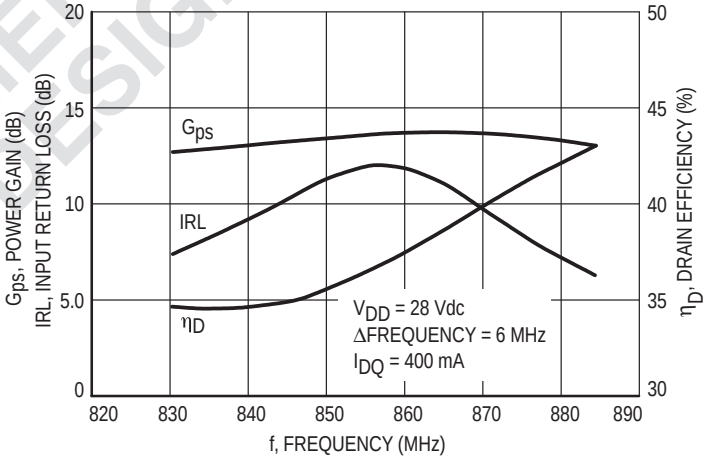


Figure 6. Performance in Narrowband Test Circuit

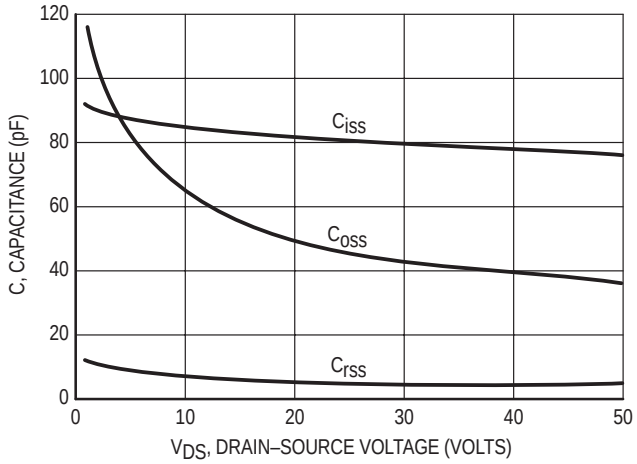
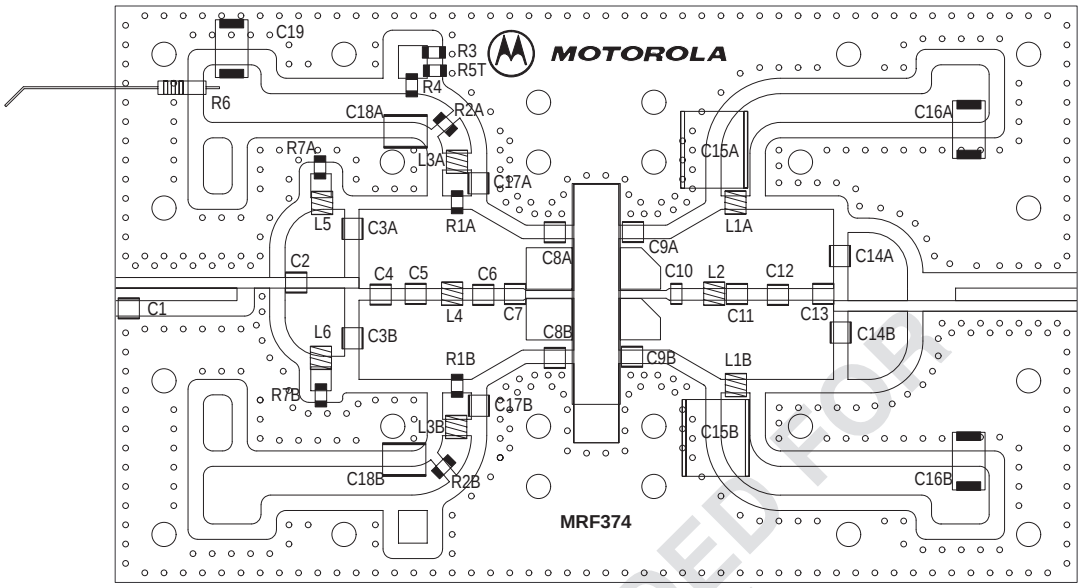


Figure 7. Capacitance versus Voltage

NOT RECOMMENDED FOR NEW DESIGN



Vertical Balun Mounting Detail

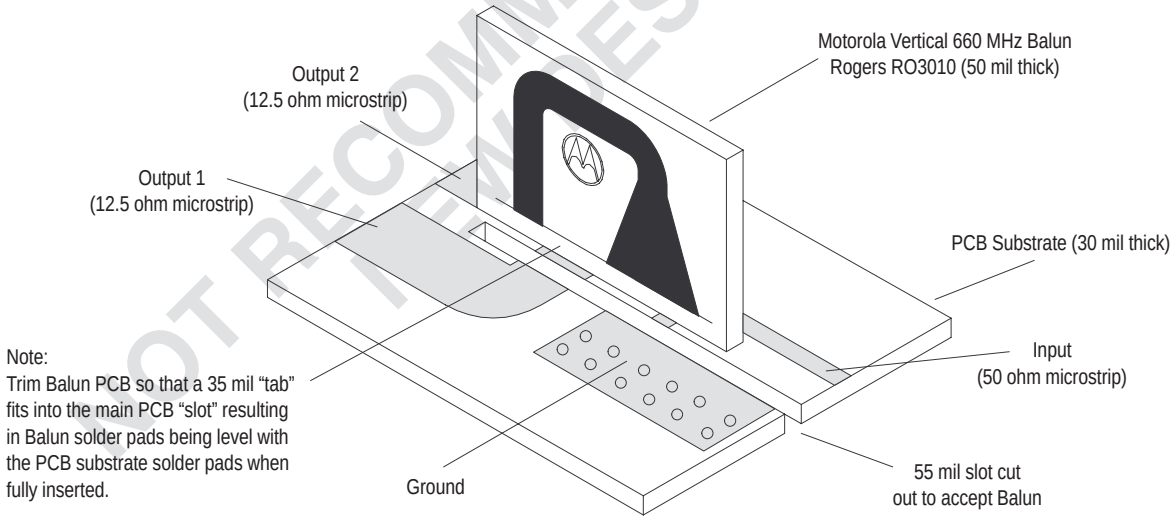


Figure 8. Broadband Component Layout

NOT RECOMMENDED FOR NEW DESIGN

Table 2. Broadband Component Designations and Values

Designation	Description
C1	0.8 pF, ATC, Case B
C2	8.2 pF, ATC, Case B
C3A, B, C14A, B	100 pF, ATC, Case B
C4	7.5 pF, ATC, Case B
C5	3.0 pF, ATC, Case B
C6	9.1 pF, ATC, Case B
C7	15 pF, ATC, Case B
C8A, B	12 pF, ATC, Case B
C9A, B	4.7 pF, ATC, Case B
C10	10 pF, ATC, Case B
C11	3.6 pF, ATC, Case B
C12	3.0 pF, ATC, Case B
C13	2.7 pF, ATC, Case B
C15A, B	3.3 μF, 100 V, Vitramon P/N VJ3640Y335KXBAT
C16A, B	22 μF, 35 V, Kemet P/N T491D226K035AS
C17A, B	3.9 pF, ATC, Case B
C18A, B	2.2 μF, 50 V, Vitramon P/N VJ2225Y225KXAAT
C19	10 μF, 35 V, Kemet P/N T491D106K035AS
L1A, B, L3A, B, L4, L5	8.0 nH, Coilcraft P/N A03T
L2, L6	12.5 nH, Coilcraft P/N A04T
R1A, B	22 Ω, Vishay Dale Chip Resistor, 1/4 W (1206)
R2A, B, R7A, B	10 Ω, Vishay Dale Chip Resistor, 1/4 W (1206)
R3	390 Ω, Vishay Dale Chip Resistor (1206)
R4	2.4 kΩ, Vishay Dale Chip Resistor (1206)
R5T	470 Ω Thermistor, KOA SPEER MOT P/N 0680149M01
R6	6.8 kΩ, Vishay Dale Resistor, 1/2 W (Axial Lead)
PCB	MRF374 Printed Circuit Board Rev 03, Rogers RO4350, Height 30 mils, ε_r = 3.48
Balun B1, B2	Vertical 660 MHz Broadband Balun, Printed Circuit Board Rev 01, Rogers RO3010, Height 50 mils, ε_r = 10.2

NOT RECOMMENDED FOR NEW DESIGN

f MHz	Z_{in} Ω	Z_{OL}* Ω
470	5.79 – j0.97	4.54 + j2.82
660	4.52 + j0.50	4.21 + j3.04
860	3.16 + j3.73	3.86 + j3.44

Z_{in} = Input impedance from the transistor.

Z_{OL}* = Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

Note: Z_{in} and Z_{OL} are measured impedances taken from gate–to–gate and drain–to–drain, respectively.

Table 3. Broadband Push–Pull Balanced Fixture Impedances

TYPICAL TWO–TONE BROADBAND CHARACTERISTICS

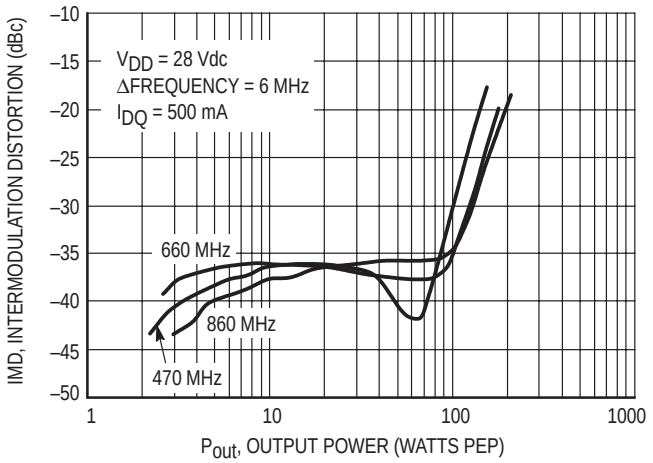


Figure 9. Broadband Intermodulation Distortion versus Output Power

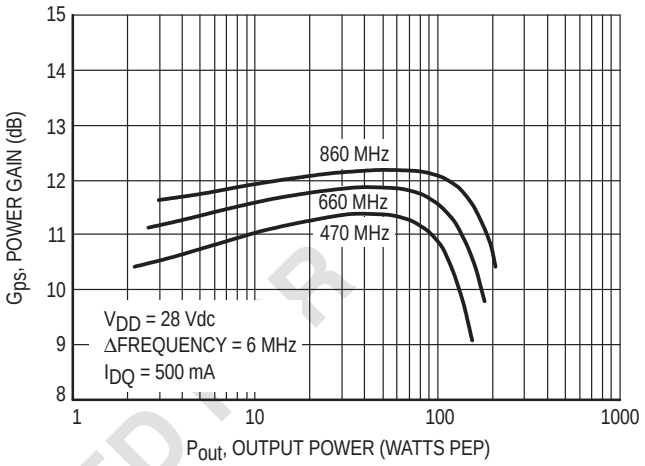


Figure 10. Broadband Power Gain versus Output Power

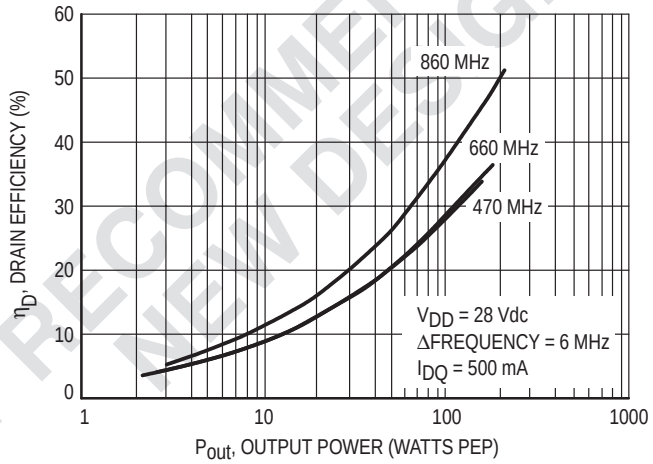


Figure 11. Broadband Efficiency versus Output Power

NOT RECOMMENDED FOR NEW DESIGN

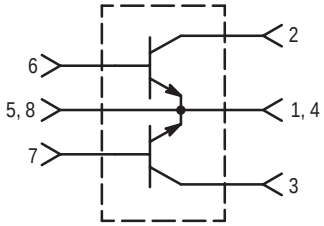
The RF Line
NPN Silicon Push-Pull RF Power Transistor

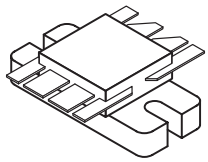
MRF392

125 W, 30 to 500 MHz
CONTROLLED "Q"
BROADBAND PUSH–PULL
RF POWER TRANSISTOR
NPN SILICON

Designed primarily for wideband large–signal output and driver amplifier stages in the 30 to 500 MHz frequency range.

- Specified 28 Volt, 400 MHz Characteristics —
  Output Power = 125 W
  Typical Gain = 10 dB
  Efficiency = 55% (Typ)
- Built–In Input Impedance Matching Networks for Broadband Operation
- Push–Pull Configuration Reduces Even Numbered Harmonics
- Gold Metallization System for High Reliability
- 100% Tested for Load Mismatch
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.





CASE 744A–01, STYLE 1

The MRF392 is two transistors in a single package with separate base and collector leads and emitters common. This arrangement provides the designer with a space saving device capable of operation in a push–pull configuration.

PUSH–PULL TRANSISTORS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	16	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

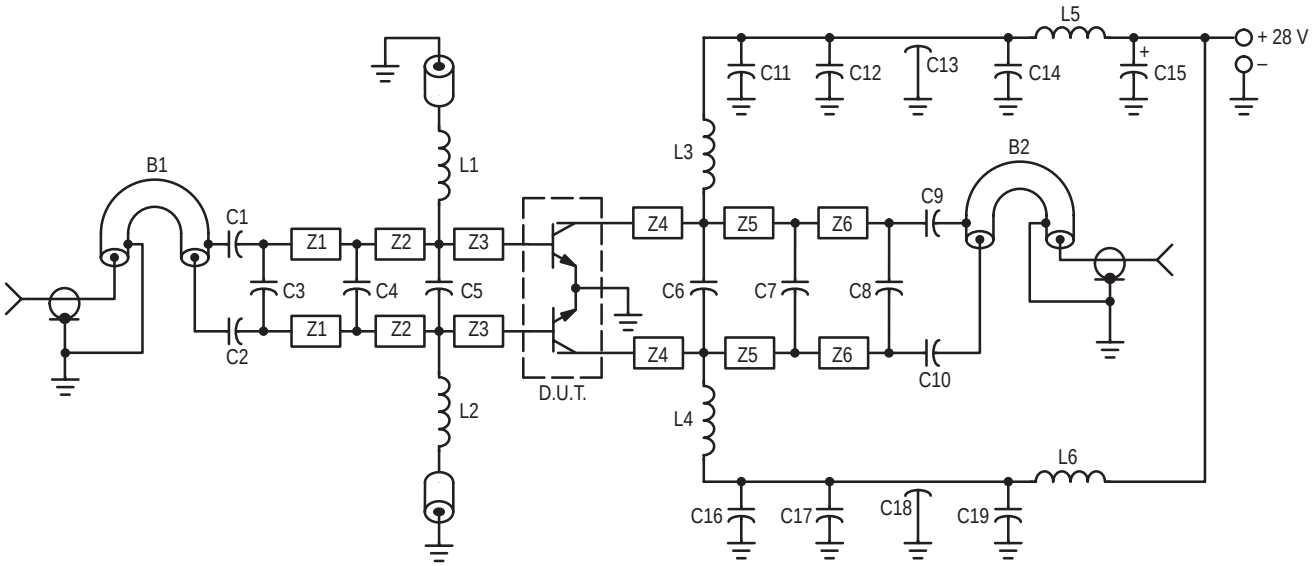
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

NOTE:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF push–pull amplifier.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	5.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40	60	100	—
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	75	95	pF
FUNCTIONAL TESTS (2) **— See Figure 1**					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 125 W, f = 400 MHz)	G_{pe}	8.0	10	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 125 W, f = 400 MHz)	η	50	55	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 125 W, f = 400 MHz, VSWR = 30:1, all phase angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each transistor chip measured separately.
2. Both transistor chips operating in push–pull amplifier.



C1, C2 — 240 pF, 100 Mil Chip Cap (ATC) or Equivalent
C3 — 3.6 pF, 100 Mil Chip Cap (ATC) or Equivalent
C4, C8 — 8.2 pF, 100 Mil Chip Cap (ATC) or Equivalent
C5, C6 — 20 pF, 100 Mil Chip Cap (ATC) or Equivalent
C7 — 18 pF, Mini Unelco or Equivalent
C9, C10 — 270 pF, 100 Mil Chip Cap (ATC) or Equivalent
C11, C12, C16, C17 — 470 pF 100 Mil Chip Cap (ATC) or Equivalent
C13, C18 — 680 pF Feedthru
C14, C19 — 0.1 μF Erie Redcap or Equivalent
C15 — 20 μF, 50 V

L1, L2 — 0.15 μH Molded Choke With Ferrite Bead
L3, L4 — 2–1/2 Turns #20 AWG, 0.200 ID
L5, L6 — 3–1/2 Turns #18 AWG, 0.200 ID

B1 — Balun, 50 Ω Semi–Rigid Coaxial Cable 86 Mil OD, 2″ L
B2 — Balun, 50 Ω Semi–Rigid Coaxial Cable 86 Mil OD, 2″ L

Z1 — Microstrip Line 270 Mil L x 125 Mil W
Z2 — Microstrip Line 375 Mil L x 125 Mil W
Z3 — Microstrip Line 280 Mil L x 125 Mil W
Z4 — Microstrip Line 300 Mil L x 125 Mil W
Z5 — Microstrip Line 350 Mil L x 125 Mil W
Z6 — Microstrip Line 365 Mil L x 125 Mil W

Board Material — 0.0625″ Teflon Fiberglass ε_r = 2.5 ± 0.05 1 oz. Cu. CLAD, Double Sided

Figure 1. 400 MHz Test Fixture

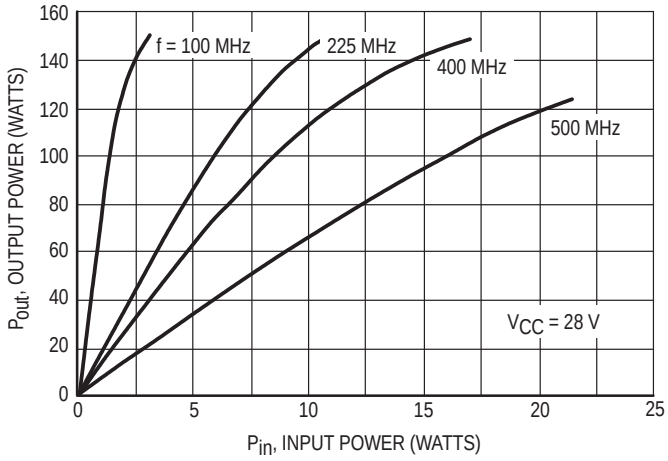


Figure 2. Output Power versus Input Power

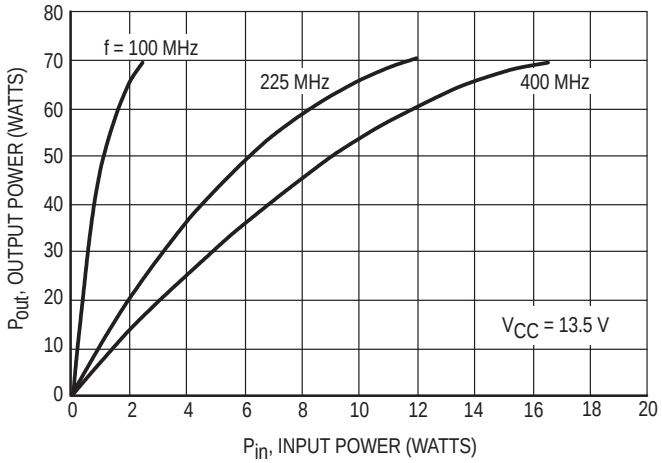


Figure 3. Output Power versus Input Power

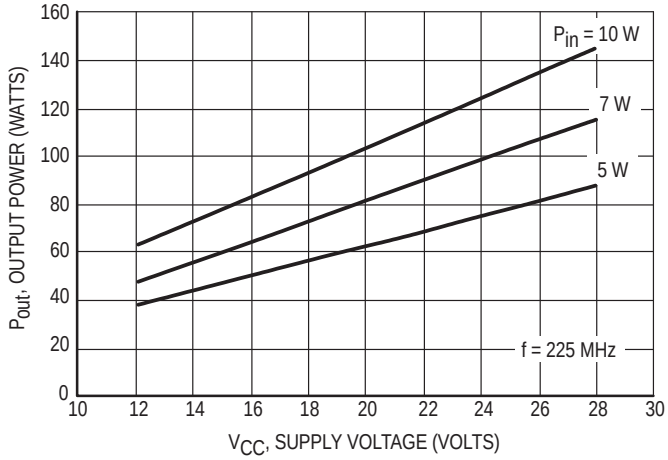


Figure 4. Output Power versus Supply Voltage

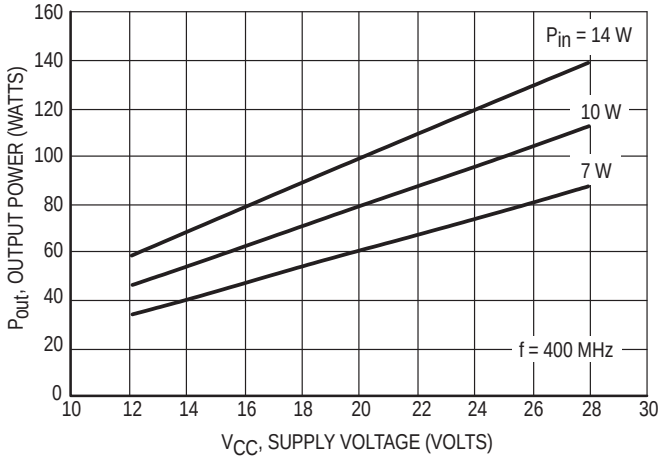
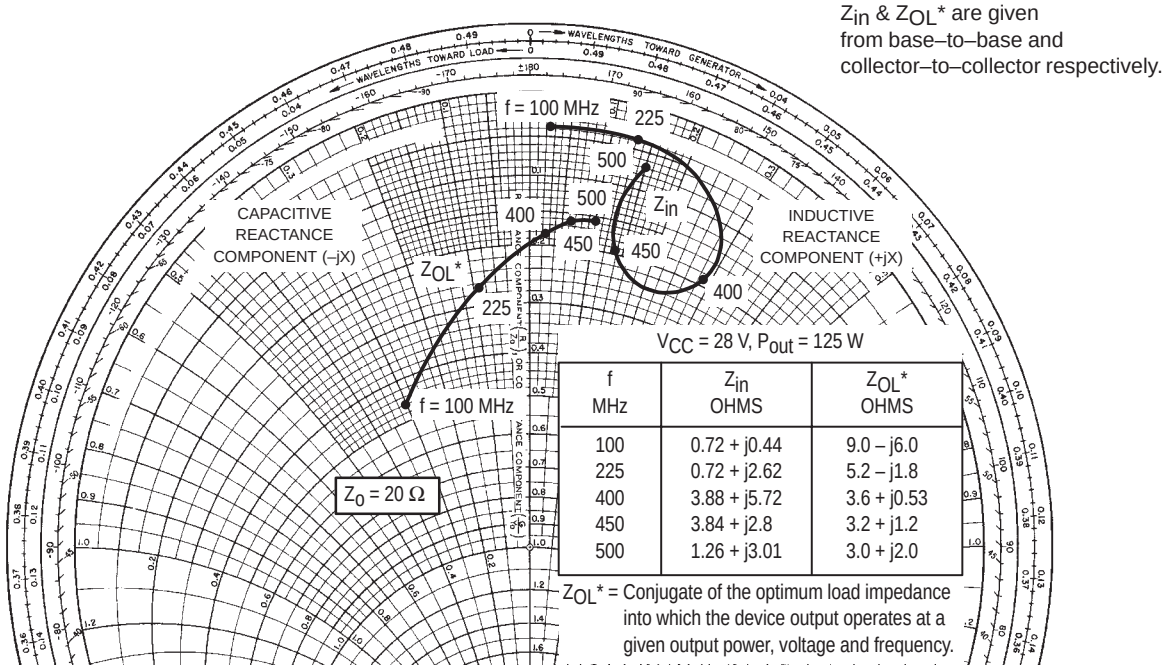


Figure 5. Output Power versus Supply Voltage



f MHz	Z_{in} OHMS	Z_{OL}* OHMS
100	0.72 + j0.44	9.0 – j6.0
225	0.72 + j2.62	5.2 – j1.8
400	3.88 + j5.72	3.6 + j0.53
450	3.84 + j2.8	3.2 + j1.2
500	1.26 + j3.01	3.0 + j2.0

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

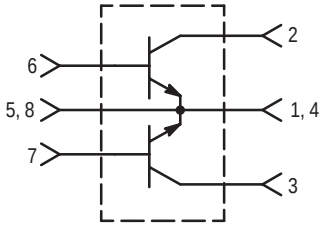
Figure 6. Series Equivalent Input/Output Impedance

The RF Line

NPN Silicon Push-Pull RF Power Transistor

. . . designed primarily for wideband large–signal output and driver amplifier stages in the 30 to 500 MHz frequency range.

- Specified 28 Volt, 500 MHz Characteristics —
  Output Power = 100 W
  Typical Gain = 9.5 dB (Class AB); 8.5 dB (Class C)
  Efficiency = 55% (Typ)
- Built–In Input Impedance Matching Networks for Broadband Operation
- Push–Pull Configuration Reduces Even Numbered Harmonics
- Gold Metallization System for High Reliability
- 100% Tested for Load Mismatch
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

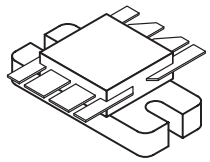


The MRF393 is two transistors in a single package with separate base and collector leads and emitters common. This arrangement provides the designer with a space saving device capable of operation in a push–pull configuration.

PUSH–PULL TRANSISTORS

MRF393

100 W, 30 to 500 MHz
CONTROLLED "Q"
BROADBAND PUSH–PULL
RF POWER TRANSISTOR
NPN SILICON



CASE 744A–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	16	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

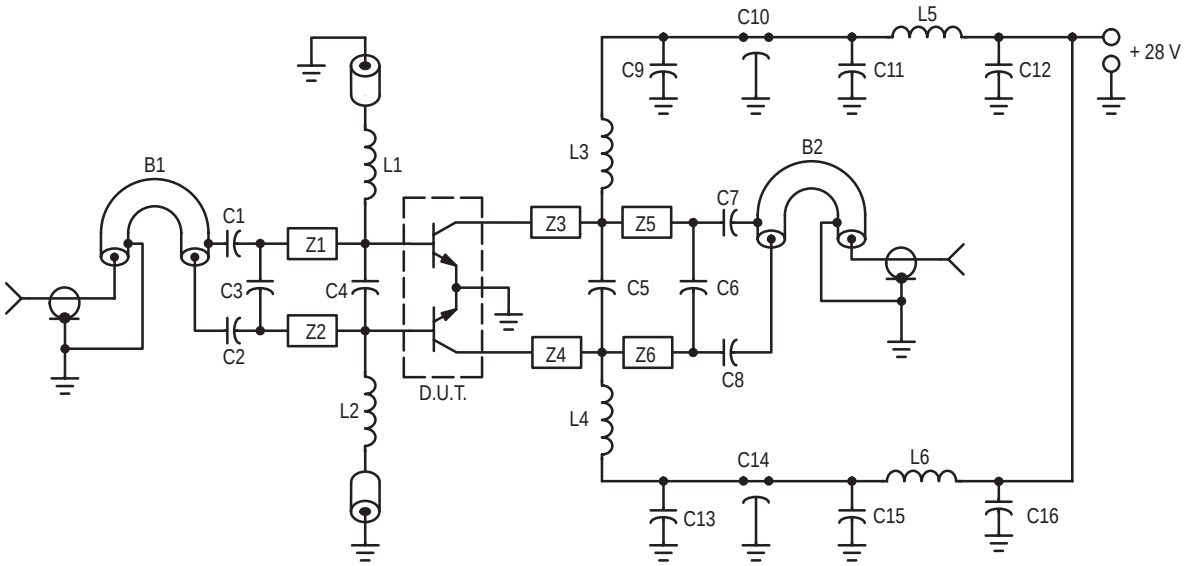
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

NOTE:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF push–pull amplifier.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	5.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	100	—
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	40	75	95	pF
FUNCTIONAL TESTS (2) **— See Figure 1**					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 500 MHz)	G_{pe}	7.5	8.5	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 500 MHz)	η	50	55	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 500 MHz, VSWR = 30:1, all phase angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each transistor chip measured separately.
2. Both transistor chips operating in push–pull amplifier.



C1, C2, C7, C8 — 240 pF 100 mil Chip Cap
C3 — 15 pF 100 mil Chip Cap
C4 — 24 pF 100 mil Chip Cap
C5 — 33 pF 100 mil Chip Cap
C6 — 12 pF 100 mil Chip Cap
C9, C13 — 1000 pF 100 mil Chip Cap
C10, C14 — 680 pF Feedthru Cap
C11, C15 — 0.1 μF Ceramic Disc Cap
C12, C16 — 50 μF 50 V

L1, L2 — 0.15 μH Molded Choke with Ferrite Bead
L3, L4 — 2–1/2 Turns #20 AWG 0.200″ ID
L5, L6 — 3–1/2 Turns #18 AWG 0.200″ ID
B1, B2 — Balun 50 Ω Semi Rigid Coax, 86 mil OD, 4″ Long
Z1, Z2 — 850 mil Long x 125 mil W. Microstrip
Z3, Z4 — 200 mil Long x 125 mil W. Microstrip
Z5, Z6 — 800 mil Long x 125 mil W. Microstrip
Board Material — 0.0325″ Teflon–Fiberglass, ε_r = 2.56, 1 oz. Copper Clad both sides.

Figure 1. 500 MHz Test Fixture

CLASS C

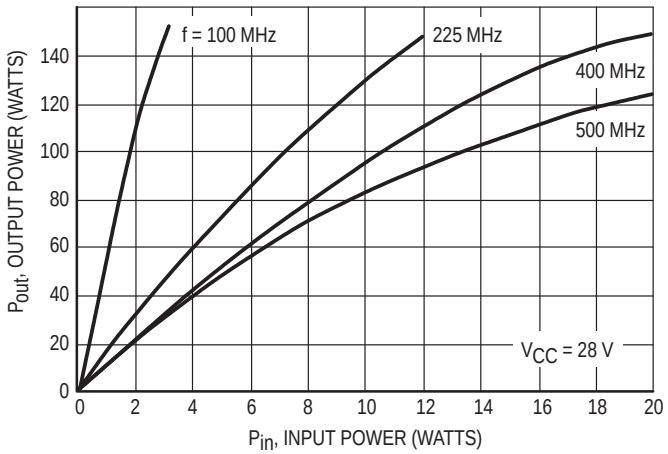


Figure 2. Output Power versus Input Power

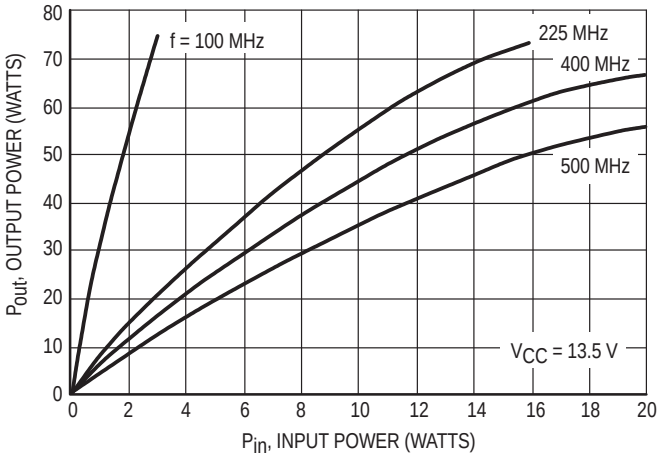


Figure 3. Output Power versus Input Power

CLASS C

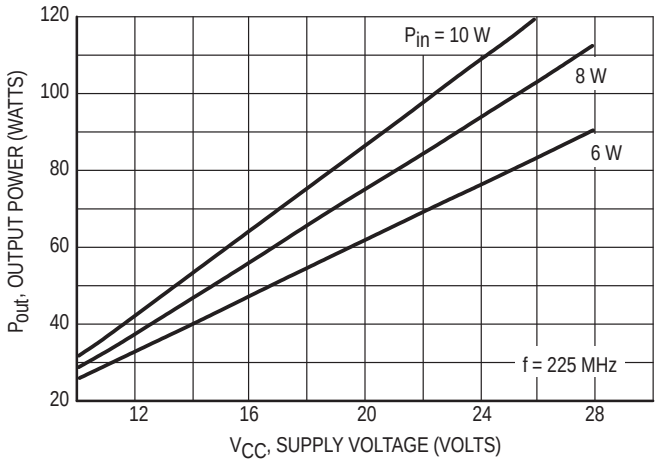


Figure 4. Output Power versus Supply Voltage

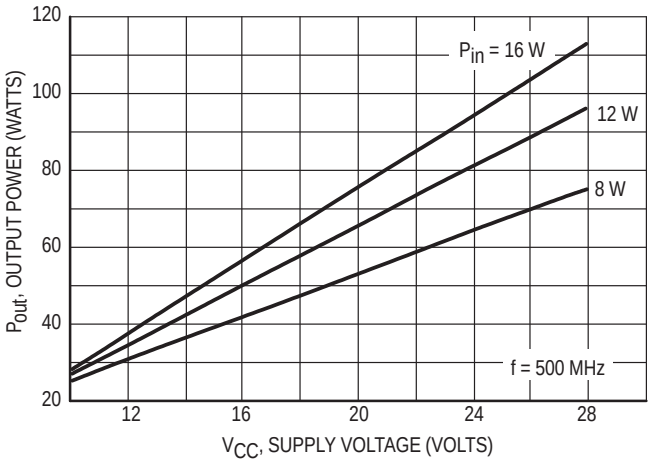
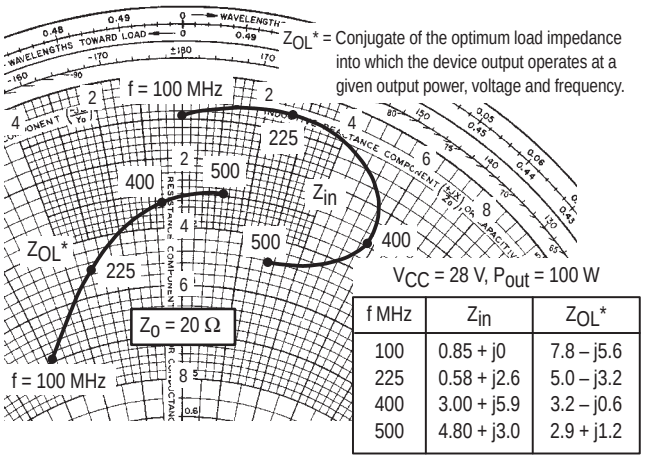


Figure 5. Output Power versus Supply Voltage



ZOL* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

f MHz	Zin	ZOL*
100	0.85 + j0	7.8 – j5.6
225	0.58 + j2.6	5.0 – j3.2
400	3.00 + j5.9	3.2 – j0.6
500	4.80 + j3.0	2.9 + j1.2

NOTE: Z_{in} & Z_{OL}* are given from base–to–base and collector–to–collector respectively.

Figure 6. Series Equivalent Input/Output Impedance

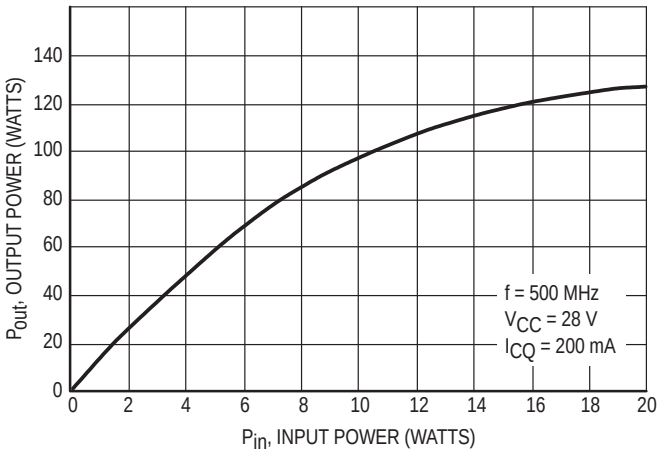


Figure 7. Class AB Output Power versus Input Power

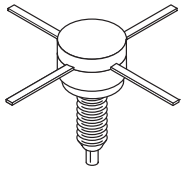
The RF Line
NPN Silicon High-Frequency Transistor

MRF587

. . . designed for use in high–gain, low–noise, ultra–linear, tuned and wideband amplifiers. Ideal for use in CATV, MATV, and instrumentation applications.

- Low Noise Figure —
  NF = 3.0 dB (Typ) @ f = 500 MHz, I_C = 90 mA
- High Power Gain —
  $G_{U(max)}$ = 16.5 dB (Typ) @ f = 500 MHz
- Ion Implanted
- All Gold Metal System
- High f_T — 5.5 GHz
- Low Intermodulation Distortion:
  TB_3 = –70 dB
  DIN = 125 dB μV
- Nichrome Emitter Ballast Resistors

NF = 3.0 dB @ 0.5 GHz
HIGH–FREQUENCY TRANSISTOR
NPN SILICON



CASE 244A–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	17	Vdc
Collector–Base Voltage	V_{CBO}	34	Vdc
Emitter–Base Voltage	V_{EBO}	2.5	Vdc
Collector Current — Continuous	I_C	200	mAdc
Total Device Dissipation @ T_C = 50°C Derate above T_C = 50°C	P_D	5.0 33	Watts mW/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Junction Temperature	T_J	200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	17	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 1.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	34	—	—	Vdc
Emitter–Base Breakdown Voltage (I_C = 0, I_E = 0.1 mAdc)	$V_{(BR)EBO}$	2.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	—	—	50	μAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	50	—	200	—

NOTE:
1. 300 μs pulse on Tektronix 576 or equivalent.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 90 mAdc, V_{CE} = 15 Vdc, f = 0.5 GHz)	f_T	—	5.5	—	GHz
Collector–Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	—	1.7	2.2	pF
FUNCTIONAL TESTS					
Narrowband — Figure 15 (I_C = 90 mA, V_{CC} = 15 V, f = 0.5 GHz) Noise Figure Power Gain at Optimum Noise Figure	 NF G_{NF}	 — 11	 3.0 13	 4.0 —	dB
Broadband — Figure 16 (I_C = 90 mA, V_{CC} = 15 V, f = 0.3 GHz) Noise Figure Power Gain at Optimum Noise Figure	 NF G_{NF}	 — —	 6.3 11	 — —	dB
Triple Beat Distortion (I_C = 50 mA, V_{CC} = 15 V, P_{Ref} = 50 dBmV) (I_C = 90 mA, V_{CC} = 15 V, P_{Ref} = 50 dBmV)	TB_3	—	–70	—	dB
DIN 45004 (I_C = 90 mA, V_{CC} = 15 V) (I_C = 90 mA, V_{CC} = 15 V)	DIN	—	125	—	dBμV
Maximum Available Power Gain (3) (I_C = 90 mA, V_{CE} = 15 Vdc, f = 0.5 GHz)	G_{Umax}	—	16.5	—	dB

NOTES:

2. Characterized on HP8542 Automatic Network Analyzer

3. $G_{Umax} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$

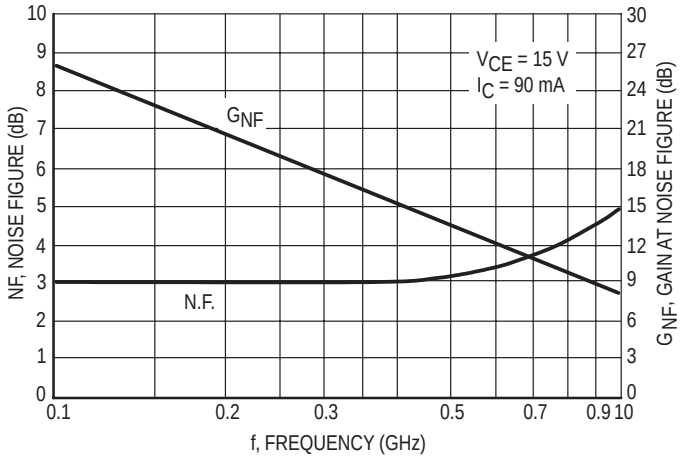


Figure 1. Typical Noise Figure and Associated Gain versus Frequency

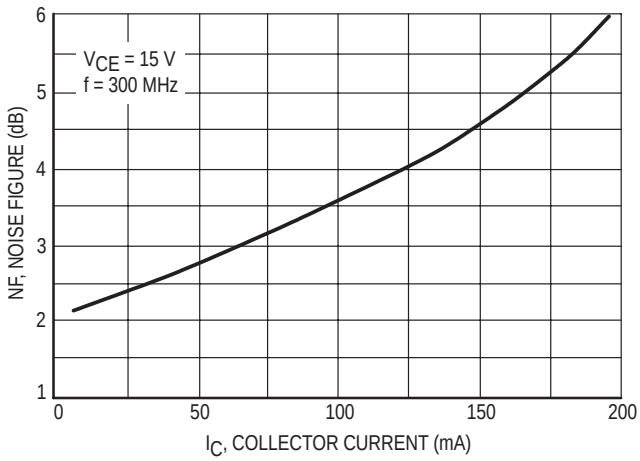


Figure 2. Noise Figure versus Collector Current

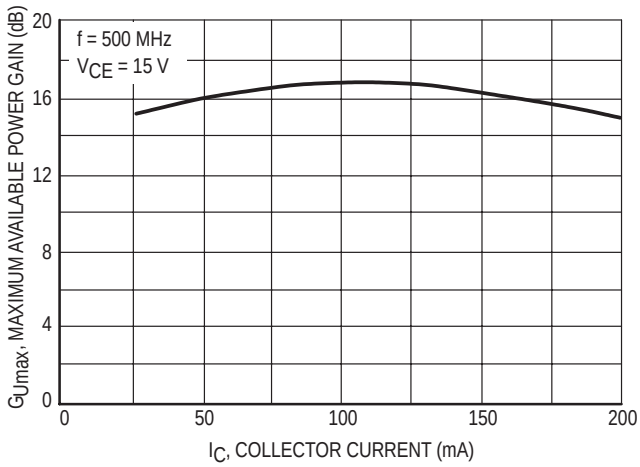


Figure 3. G_{Umax} versus Collector Current

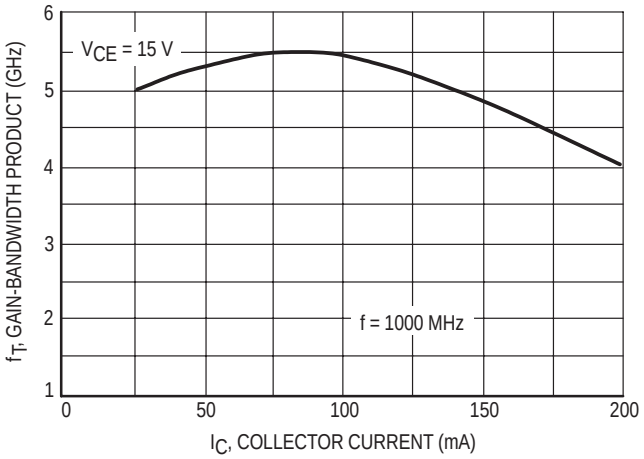


Figure 4. Gain–Bandwidth Product versus Collector Current

TYPICAL PERFORMANCE

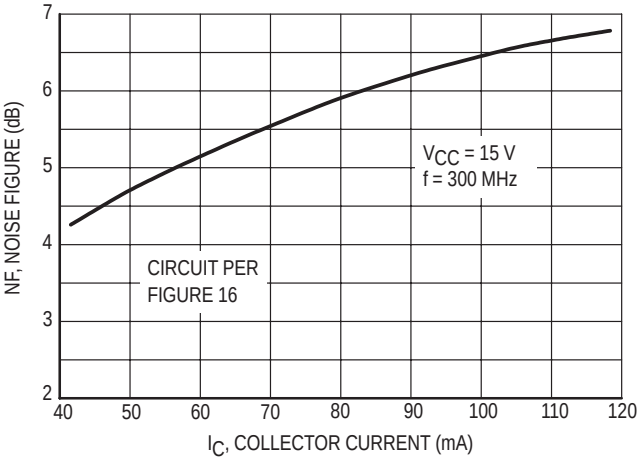


Figure 5. Broadband Noise Figure

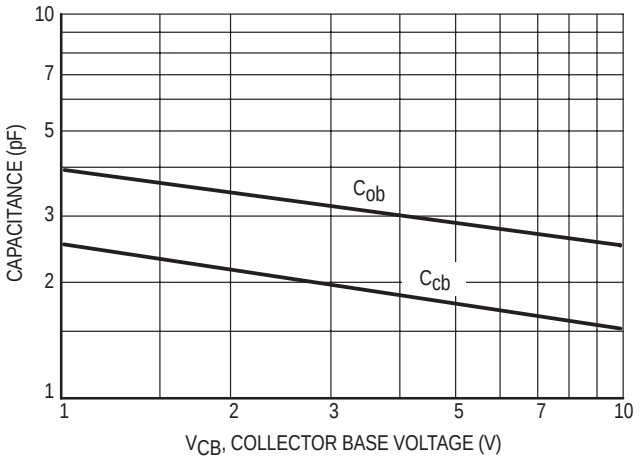


Figure 6. Junction Capacitance versus Voltage

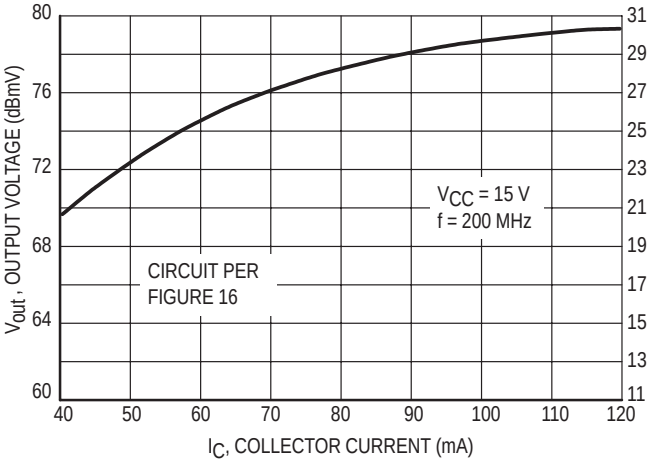


Figure 7. 1.0 dB Compression Point versus Collector Current

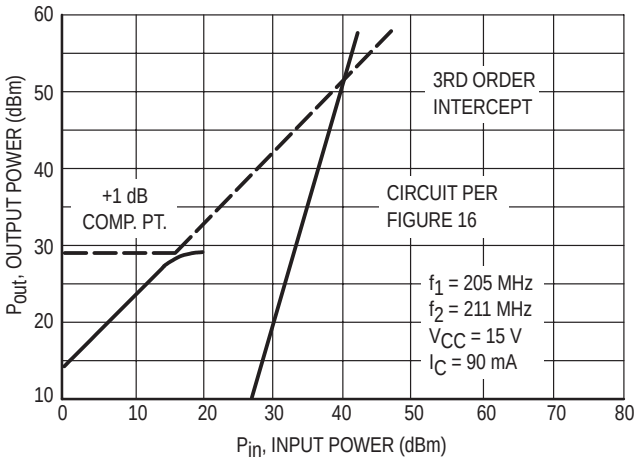


Figure 8. Third Order Intercept Point

TYPICAL PERFORMANCE (continued)

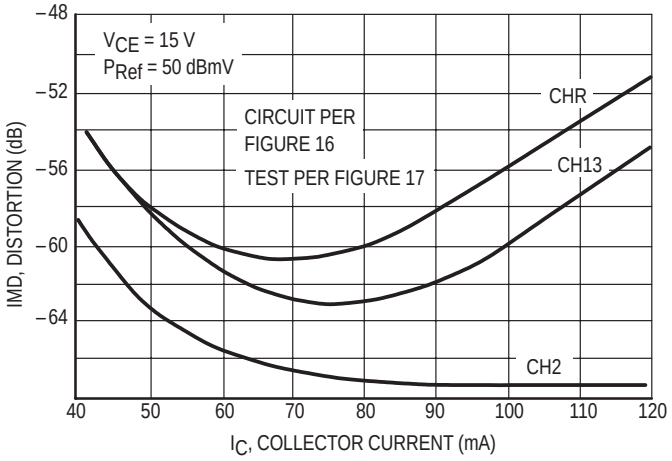


Figure 9. Second Order Distortion versus Collector Current

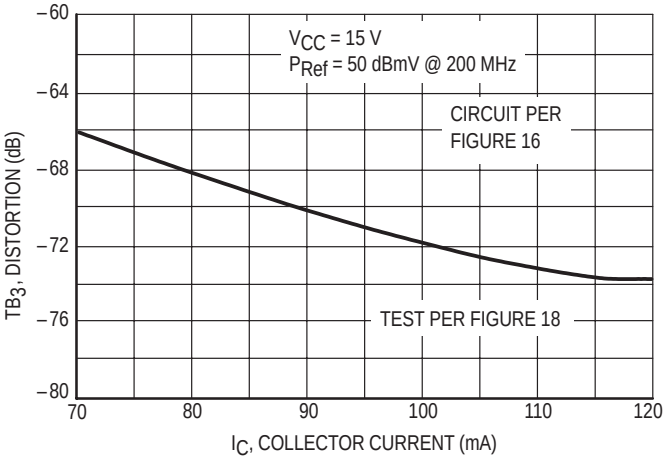


Figure 10. Triple Beat Distortion versus Collector Current

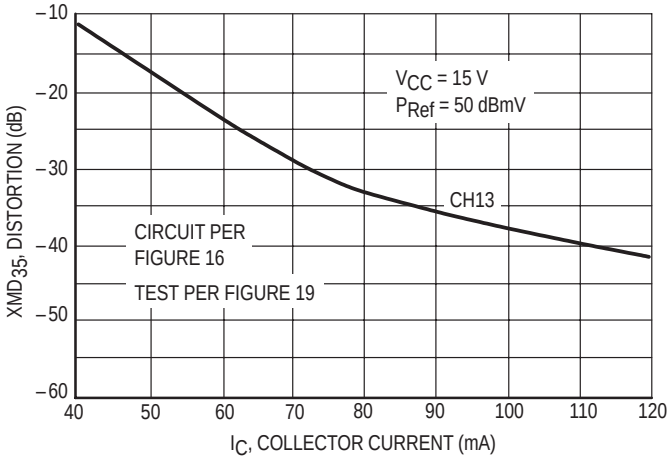


Figure 11. 35–Channel X–Modulation Distortion versus Collector Current

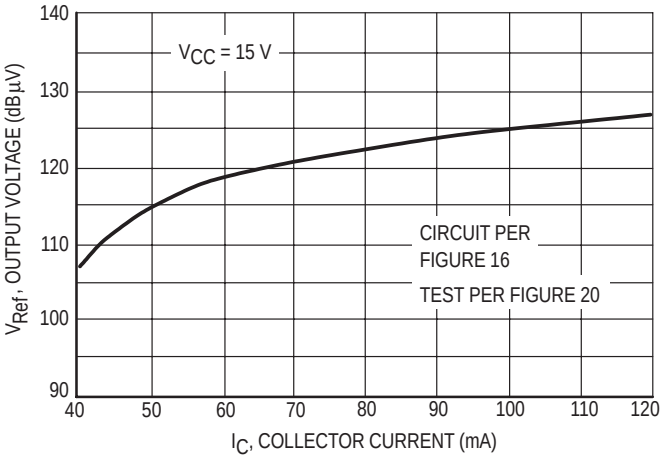


Figure 12. DIN 45004B versus Collector Current

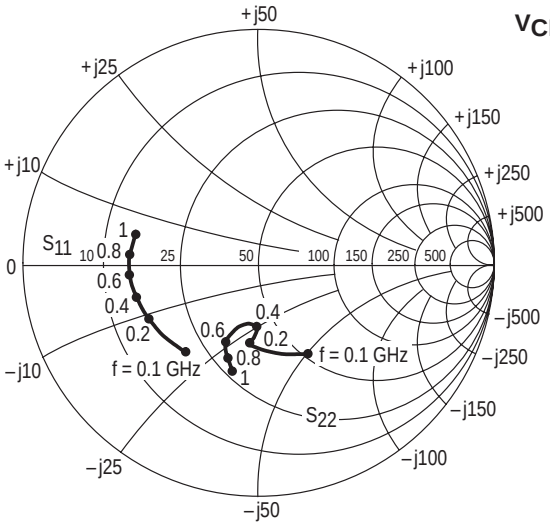


Figure 13. Input/Output Reflection Coefficient versus Frequency (GHz)

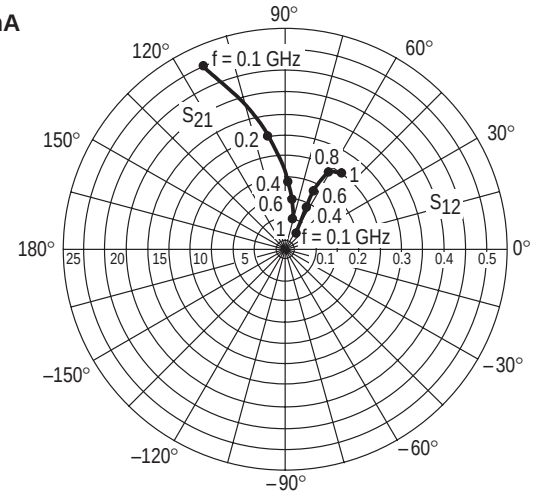


Figure 14. Forward/Reverse Transmission Coefficients versus Frequency (GHz)

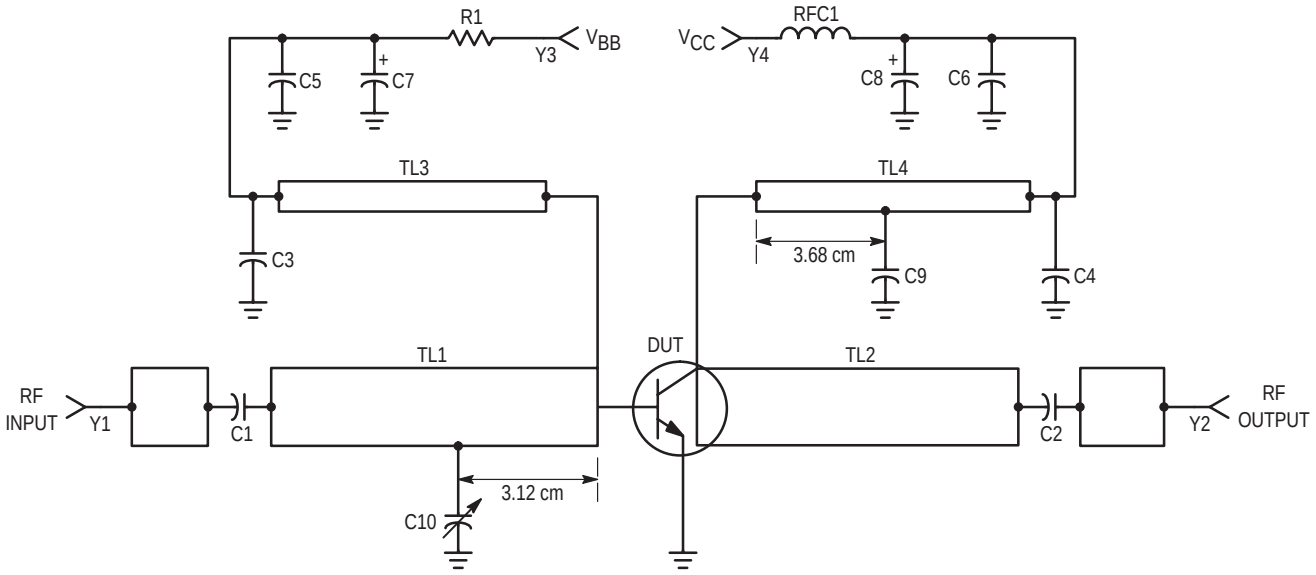
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
5.0	30	100	0.56	–131	16.45	113	0.04	45	0.49	–91
		200	0.58	–159	9.42	98	0.06	49	0.38	–116
		400	0.60	–178	5.00	86	0.08	55	0.35	–132
		600	0.64	170	3.61	76	0.11	56	0.38	–138
		800	0.67	162	2.92	67	0.14	55	0.41	–144
		1000	0.70	155	2.55	58	0.17	54	0.44	–152
	60	100	0.53	–141	17.89	110	0.04	50	0.47	–102
		200	0.56	–164	10.05	97	0.05	55	0.39	–126
		400	0.59	178	5.31	85	0.09	60	0.38	–141
		600	0.63	169	3.82	76	0.12	59	0.40	–146
		800	0.66	161	3.09	67	0.15	57	0.44	–153
		1000	0.69	155	2.67	58	0.18	55	0.47	–160
	90	100	0.52	–145	18.26	109	0.04	52	0.47	–106
		200	0.56	–166	10.20	96	0.05	57	0.39	–130
		400	0.59	177	5.38	85	0.09	62	0.39	–144
		600	0.63	168	3.86	76	0.12	60	0.41	–149
		800	0.66	161	3.12	67	0.15	58	0.45	–155
		1000	0.69	155	2.70	58	0.19	55	0.48	–162
10	30	100	0.53	–122	18.36	115	0.04	48	0.50	–75
		200	0.53	–153	10.63	100	0.05	51	0.36	–96
		400	0.55	175	5.71	87	0.08	57	0.33	–112
		600	0.59	173	4.16	78	0.10	58	0.35	–119
		800	0.62	165	3.37	68	0.13	57	0.39	–127
		1000	0.65	158	2.95	59	0.15	55	0.42	–136
	60	100	0.49	–132	20.19	112	0.03	51	0.46	–85
		200	0.51	–158	11.54	99	0.05	57	0.35	–107
		400	0.53	–178	6.12	87	0.08	61	0.33	–123
		600	0.58	171	4.43	78	0.11	60	0.36	–129
		800	0.60	164	3.58	68	0.14	59	0.40	–136
		1000	0.63	157	3.12	60	0.16	57	0.44	–144
	90	100	0.48	–135	20.82	111	0.03	53	0.45	–88
		200	0.50	–160	11.77	98	0.05	59	0.34	–111
		400	0.53	–179	6.22	86	0.08	63	0.33	–126
		600	0.57	171	4.50	78	0.11	62	0.36	–131
		800	0.60	164	3.64	68	0.14	59	0.41	–139
		1000	0.63	157	3.18	60	0.17	57	0.44	–147

(continued)

Table 1. Common–Emitter S–Parameters

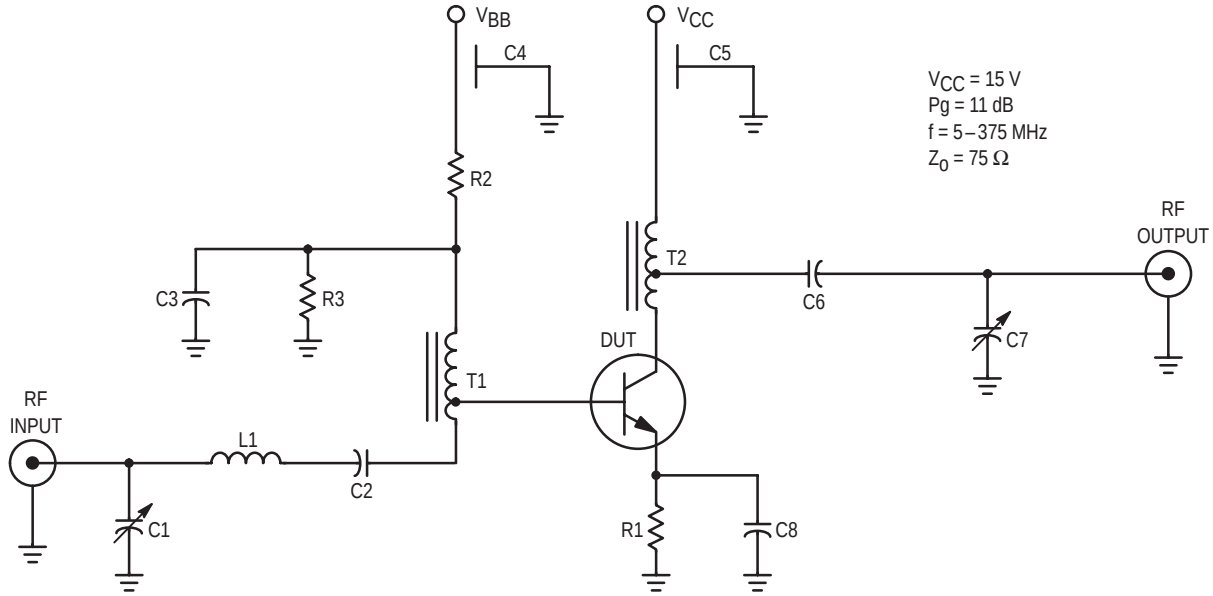
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
15	30	100	0.49	−112	20.34	118	0.04	54	0.51	−52
		200	0.52	−145	11.51	101	0.05	56	0.36	−77
		400	0.48	−164	6.12	87	0.09	63	0.32	−74
		600	0.52	−174	4.19	75	0.12	62	0.32	−90
		800	0.53	177	3.29	68	0.16	61	0.38	−90
		1000	0.53	168	2.76	61	0.20	56	0.47	−90
	60	100	0.45	−122	22.14	115	0.03	56	0.45	−60
		200	0.49	−150	12.24	99	0.05	60	0.33	−86
		400	0.45	−166	6.45	86	0.09	65	0.30	−83
		600	0.50	−175	4.42	75	0.13	63	0.32	−99
		800	0.51	177	3.47	68	0.16	61	0.38	−98
		1000	0.51	168	2.91	62	0.20	55	0.46	−96
	90	100	0.44	−127	22.76	114	0.03	58	0.43	−62
		200	0.48	−152	12.44	98	0.05	62	0.32	−89
		400	0.44	−167	6.55	85	0.09	66	0.29	−85
		600	0.50	−176	4.47	75	0.13	64	0.32	−102
		800	0.51	176	3.51	69	0.17	61	0.38	−100
		1000	0.51	168	2.95	62	0.20	55	0.46	−98

Table 1. Common–Emitter S–Parameters (continued)



C1, C2 — 470 pF Chip (Ceramic)
C3, C4 — 0.018 μF Chip Capacitor
C5, C6 — 0.1 μF Mylar
C7, C8 — 1.0 μF, 25 Vdc Electrolytic
C9 — 91 pF Mini–Unelco (C9 Taped 3.68 cm from Collector Connection on TL4 as shown)
C10 — 35–45 pF Johanson Ceramic Capacitor, JMC 5801 or Equivalent (C10 Taped 3.12 cm from Base Connection on TL1)
R1 — 2.7 kΩ, 1–1/2 W
RFC1 — 0.15 μH Molded Choke
TL1, TL2 — Z_O = 26 Ω, 0.0625 TFG as shown in Photomaster
TL3, TL4 — λ/4 Microstrip, Z_O = 100 Ω
Y1, Y2 — N–Type Connection (Female)
Y3, Y4 — BNC–Type Connector (Female)
Board Material — 0.0625″ Thick Glass Teflon ε_r = 2.5

Figure 15. Narrowband Test Fixture Schematic
500 MHz



C1, C7 — 0.5–10 pF
C2, C6 — 0.001 μF
C3 — 0.01 μF
C4, C5 — 0.01 μF Feedthru
C8 — 12 pF

R1 — 12 Ω 1.0 W (2.0–24 Ω on each emitter port)
R2 — 1.8 k 1/8 W
R3 — 2.2 k 1/8 W
L1 — 1 Turn 0.012 dia #22 AWG
T1(1) — 5 Turns Tapped at 2 Turns, #30 AWG
T2(1) — 8 Turns Tapped at 3 Turns, #30 AWG

(1) Ferroxcube 135 CT050 3D3 Material

Figure 16. Broadband Test Circuit Schematic

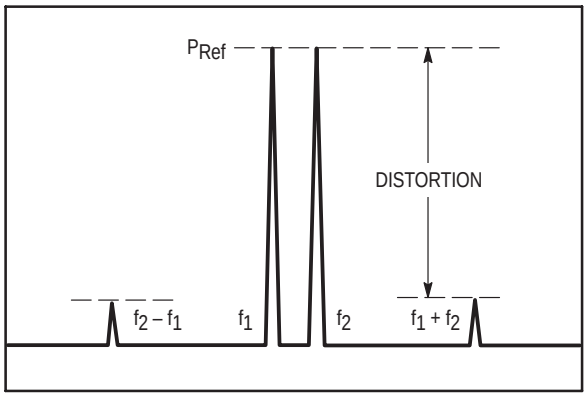


Figure 17. Second Order Distortion Test

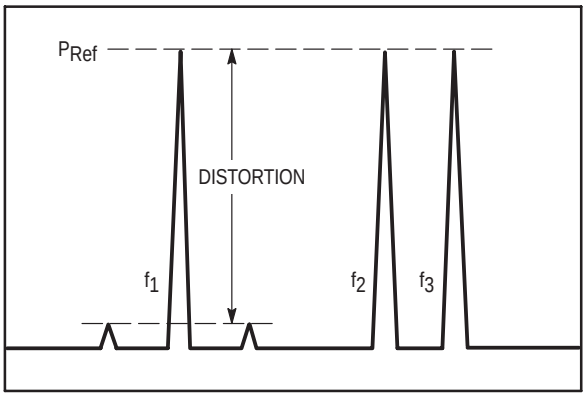


Figure 18. Triple Beat Distortion Test

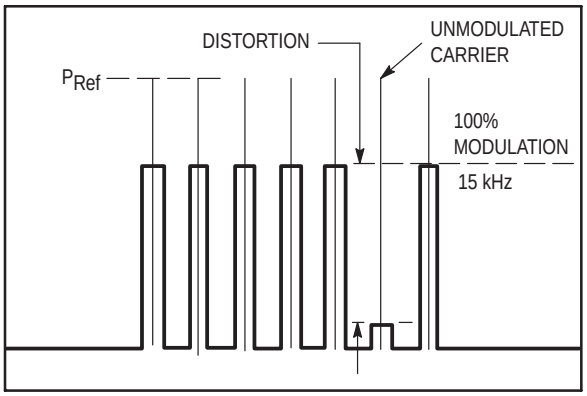


Figure 19. Cross Modulation Distortion Test

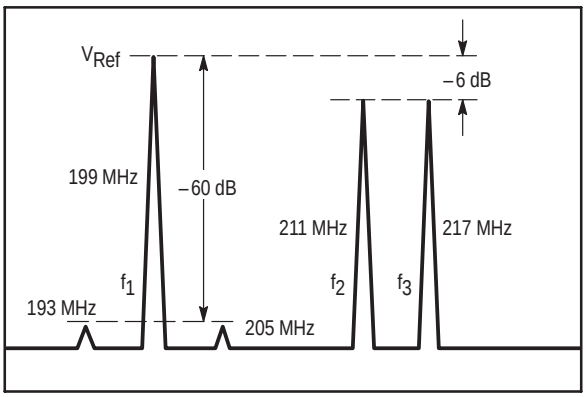
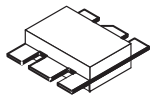


Figure 20. DIN 45004B Intermodulation Test

The RF Line
NPN Silicon RF Power Transistor

MRF858S

CLASS A
800–960 MHz
3.6 W (CW), 24 V
NPN SILICON
RF POWER TRANSISTOR



CASE 319A–02, STYLE 2

Designed for 24 Volt UHF large–signal, common emitter, class A linear amplifier applications in industrial and commercial equipment operating in the range of 800–960 MHz.

- Specified for V_{CE} = 24 Vdc, I_C = 0.5 Adc Characteristics
  - Output Power = 3.6 Watts CW
  - Minimum Power Gain = 11 dB
  - Minimum ITO = +44.5 dBm
  - Typical Noise Figure = 6 dB
- Characterized with Small–Signal S–Parameters and Series Equivalent Large–Signal Parameters from 800–960 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at All Phase Angles with 30:1 VSWR @ 24 Vdc, I_C = 0.5 Adc and Rated Output Power
- Will Withstand RF Input Overdrive of 0.85 W CW
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	55	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Total Device Dissipation @ T_C = 50°C Derate above 50°C	P_D	20 0.138	Watts W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance (T_J = 150°C, T_C = 50°C)	$R_{\theta JC}$	6.9	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mA, I_B = 0)	$V_{(BR)CEO}$	28	35	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mA, V_{BE} = 0)	$V_{(BR)CES}$	55	85	—	Vdc
Collector–Base Breakdown Voltage (I_C = 20 mA, I_E = 0)	$V_{(BR)CBO}$	55	85	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 1 mA, I_C = 0)	$V_{(BR)EBO}$	4	5	—	Vdc
Collector Cutoff Current (V_{CB} = 24 V, I_E = 0)	I_{CES}	—	—	1	mA

ELECTRICAL CHARACTERISTICS — continued

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.1 A, V_{CE} = 5 V)	h_{FE}	30	60	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 V, f = 1 MHz)	C_{ob}	—	6.5	8	pF
FUNCTIONAL CHARACTERISTICS					
Common–Emitter Power Gain (V_{CE} = 24 V, I_C = 0.5 A, f = 840–900 MHz, Power Output = 3.6 W)	P_g	11	12	—	dB
Load Mismatch (P_o = 3.6 W) (V_{CE} = 24 V, I_C = 0.5 A, f = 840 MHz, Load VSWR = 30:1, All Phase Angles)	ψ	No Degradation in Output Power			
RF Input Overdrive (V_{CE} = 24 V, I_C = 0.5 A, f = 840 MHz) No degradation	$P_{in(over)}$	—	—	0.85	W
Third Order Intercept Point (V_{CE} = 24 V, I_C = 0.5 A) (f1 = 900 MHz, f2 = 900.1 MHz, Meas. @ IMD 3rd Order = –40 dBc)	ITO	+44.5	+45.5	—	dBm
Noise Figure (V_{CE} = 24 V, I_C = 0.5 A, f = 900 MHz)	NF	—	6	—	dB
Input Return Loss (V_{CE} = 24 V, I_C = 0.5 A, f = 840–900 MHz, Power Output = 3.6 W)	IRL	—	–12	–9	dB

Table 1. Common Emitter S–Parameters

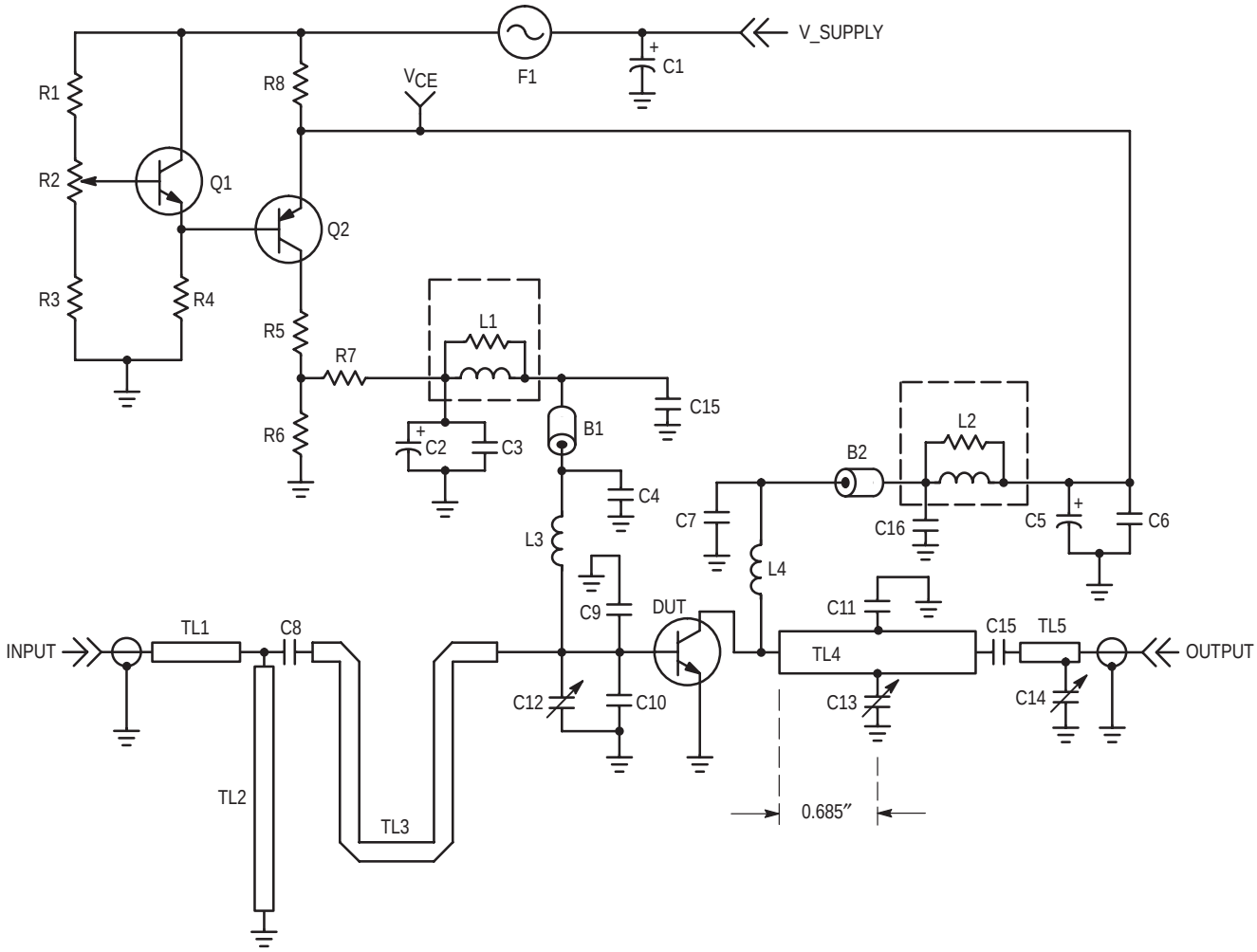
V_{CE} (V)	I_C (A)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
24	0.5	800	0.942	167	1.493	50	0.027	58	0.538	–165
		820	0.942	166	1.453	50	0.027	58	0.541	–164
		840	0.941	166	1.415	49	0.028	59	0.545	–165
		860	0.940	166	1.379	48	0.028	59	0.550	–165
		880	0.941	165	1.351	47	0.029	59	0.553	–165
		900	0.940	165	1.320	46	0.030	59	0.557	–165
		920	0.940	165	1.289	45	0.030	59	0.562	–165
		940	0.940	164	1.252	44	0.031	59	0.566	–165
		960	0.940	164	1.222	43	0.031	59	0.570	–165

Table 2. Z_{in} and Z_{OL}* versus Frequency

f (MHz)	Z_{in} (Ohms)		Z_{OL}* (Ohms)	
840	1.1	2.9	9.9	–14.4
870	1.1	3.5	9.5	–14.6
900	1.2	3.5	9	–14.5

V_{CE} = 24 V, I_C = 0.5 A, P_o = 3.6 W

Z_{OL}* = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.



B1, B2	Short Ferrite Bead, Fair Rite (2743021447)
C1	250 μF, 50 Vdc Electrolytic Capacitor
C2, C5	10 μF, 50 Vdc Electrolytic Capacitor
C3, C6	0.1 μF, Chip Capacitor
C4, C7	100 pF, Chip Capacitor
C8, C15	43 pF, 100 Mil Chip Capacitor
C9, C10	10 pF, Mini–Unelco
C11	5 pF, Mini–Unelco
C12, C13, C14	0.8–8.0 pF, Johanson Gigatrim
C15, C16	1000 pF, Chip Capacitor
F1	1 A Micro–Fuse
L1, L2	10 Turns, 20 AWG, 0.150″ ID (10 Ω 1/2 W Resistor)
L3	4 Turns, 16 AWG, 0.101″ ID
L4	0.5″ 18 AWG Wire
Q1	MMBT2222ALT1, NPN Transistor
Q2	BD136, PNP Transistor

R1	390 Ω, 1/4 W
R2	500 Ω Potentiometer, 1/4 W
R3	7.5K Ω, 1/4 W
R4	2 x 4.7K Ω, 1/4 W
R5	56 Ω, 2 W
R6	75 Ω, 1/4 W
R7	4.7 Ω, 1/4 W
R8	4 Ω, 10 W
TL1, TL5	50 Ω, Microstrip Transmission Line
TL2	Microstrip Transmission Line
TL3	Microstrip Transmission Line
TL4	Microstrip Transmission Line
V_Supply	+26 Vdc ±0.5 Vdc Due to Resistor Tolerance
V_{CE}	+24 Vdc @ 0.5 A
Board	0.030″ Glass–Teflon® 2 oz. Cu, ε_r = 2.55

Figure 1. MRF858S Class A RF Test Fixture Schematic

TYPICAL CHARACTERISTICS

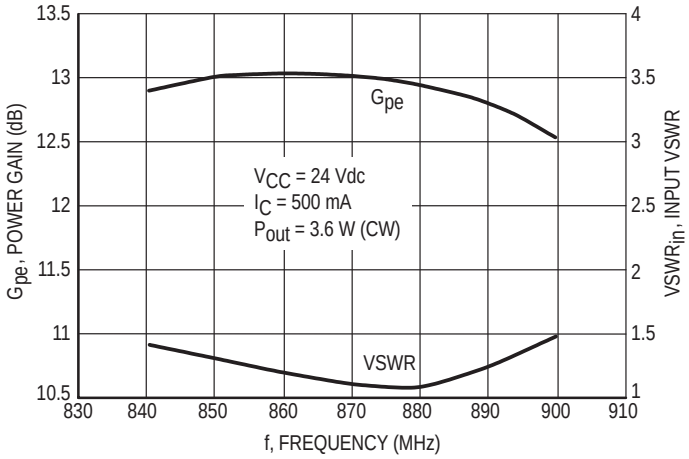


Figure 2. Performance in Broadband Circuit

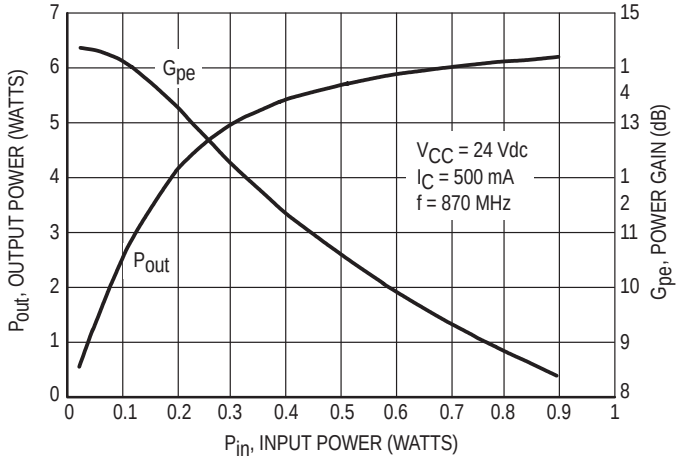


Figure 3. Output Power & Power Gain versus Input Power

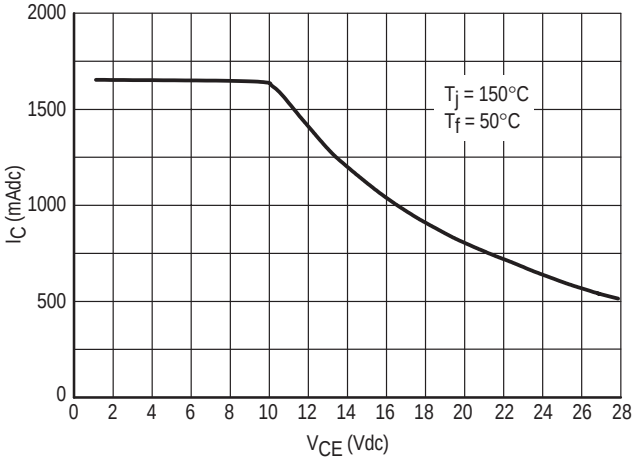


Figure 4. DC SOA

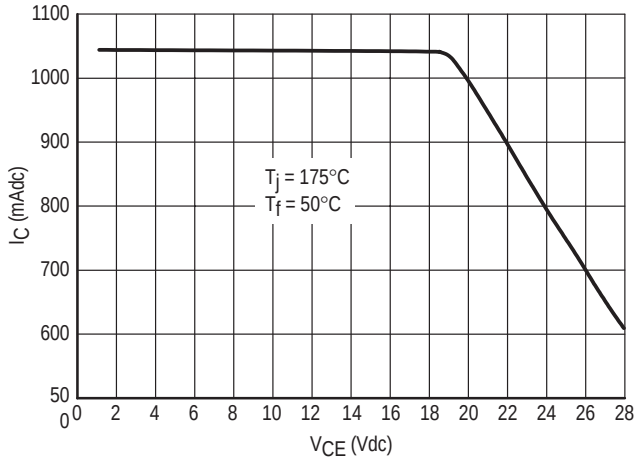


Figure 5. DC SOA
(This device is MTBF limited for V_{CE} < 20 Vdc.)

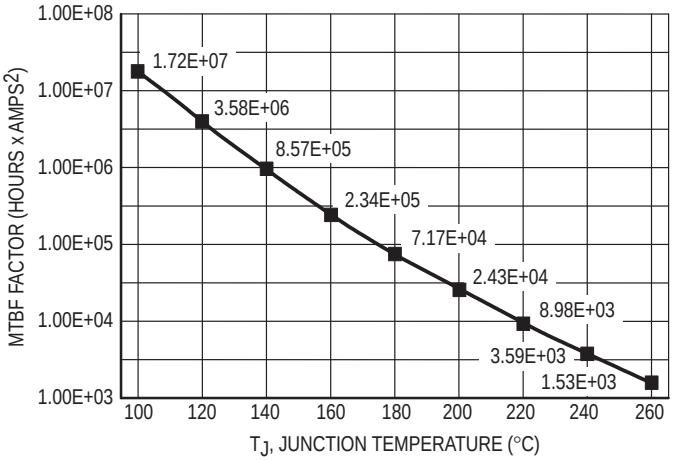


Figure 6. MTBF Factor versus Junction Temperature

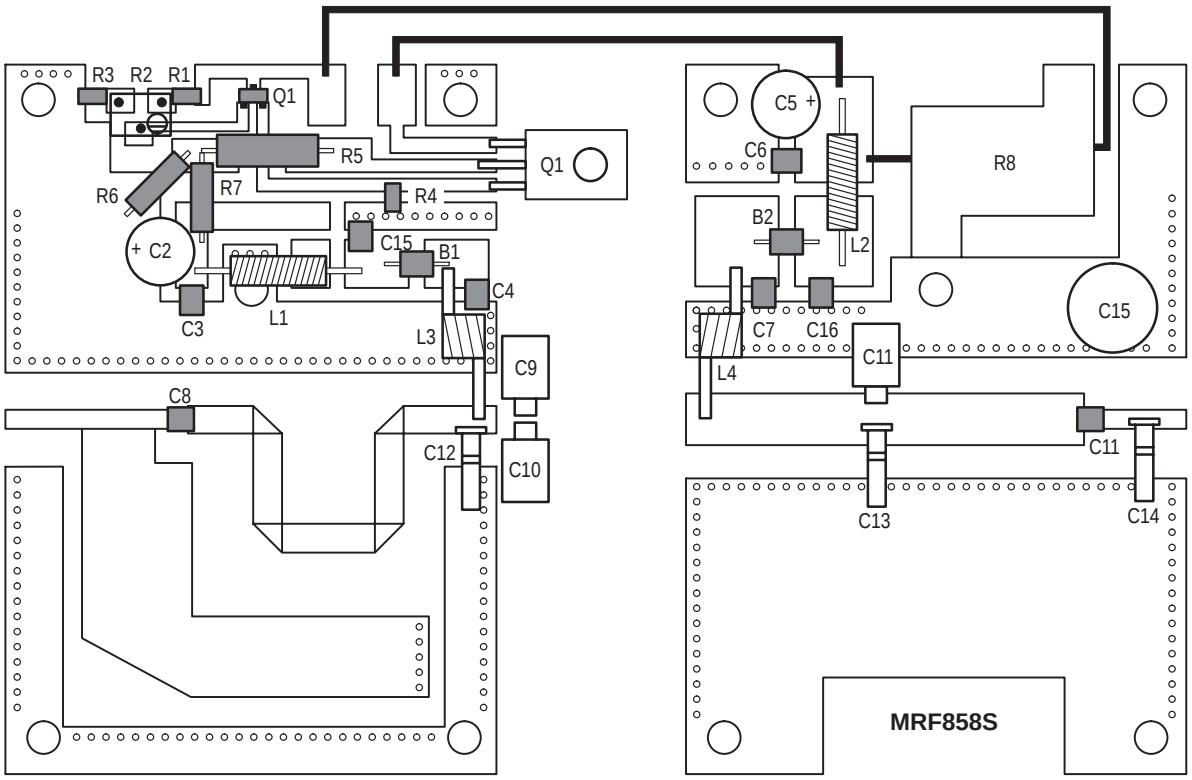


Figure 7. MRF858S Test Fixture Component Layout

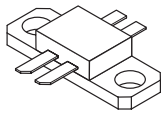
The RF Line
NPN Silicon RF Power Transistor

MRF897

30 W, 900 MHz
RF POWER
TRANSISTOR
NPN SILICON

Designed for 24 Volt UHF large–signal, common emitter, class–AB linear amplifier applications in industrial and commercial FM/AM equipment operating in the range 800–970 MHz.

- Specified 24 Volt, 900 MHz Characteristics
  - Output Power = 30 Watts
  - Minimum Gain = 10 dB @ 900 MHz, class–AB
  - Minimum Efficiency = 30% @ 900 MHz, 30 Watts (PEP)
  - Maximum Intermodulation Distortion –30 dBc @ 30 Watts (PEP)
- Characterized with Series Equivalent Large–Signal Parameters from 800 to 960 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 26 Vdc, and Rated Output Power
- Gold Metalized, Emitter Ballasted for Long Life and Resistance to Metal–Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



CASE 395B–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector–Current — Continuous	I_C	4.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	105 0.60	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W

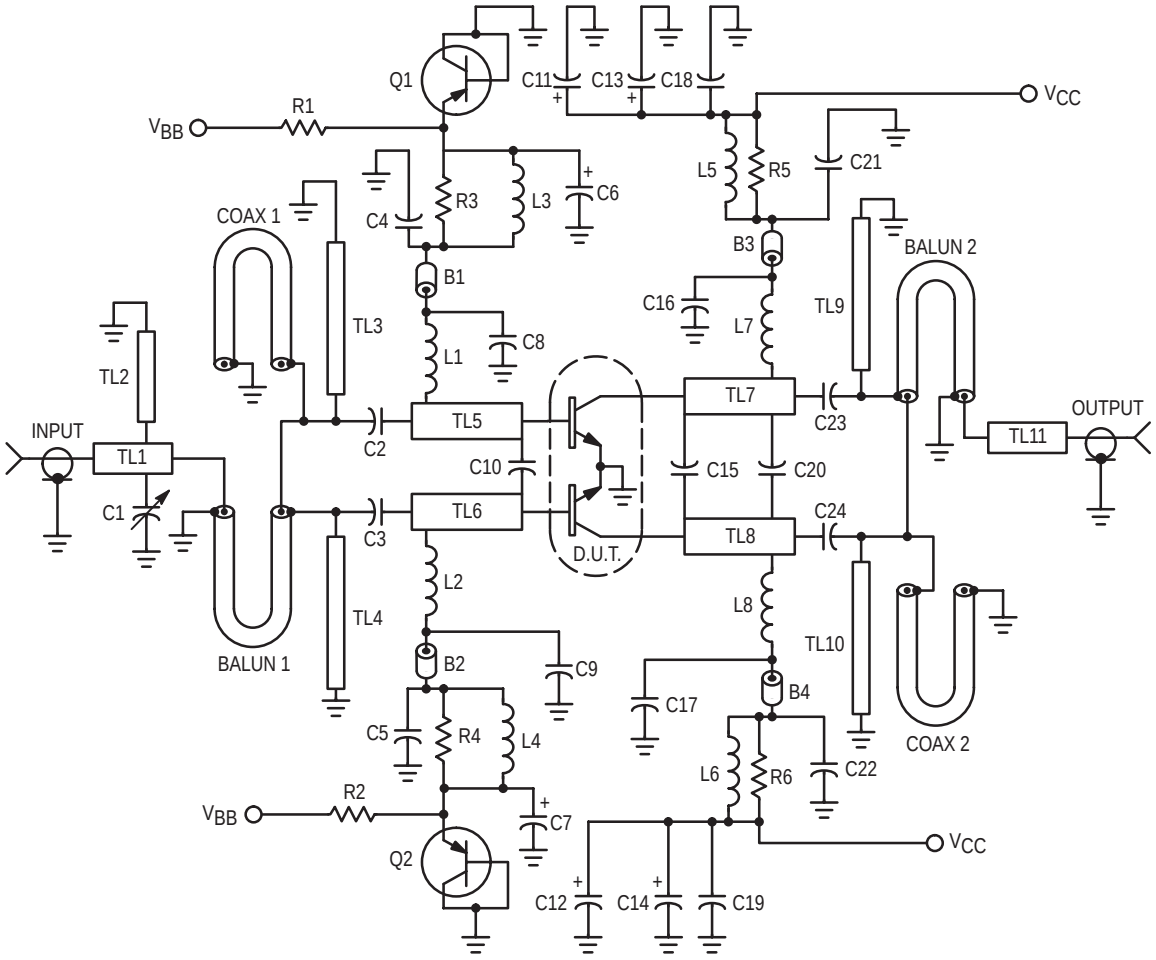
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	33	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	80	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	4.7	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	10.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1.0 Adc, V_{CE} = 5 Vdc)	h_{FE}	30	80	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	14	21	28	pF

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL CHARACTERISTICS					
Common–Emitter Amplifier Power Gain (V_{CC} = 24 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	G_{pe}	10.0	12.0	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	η	35	38	—	%
Intermodulation Distortion (V_{CC} = 24 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	IMD	—	–37	–30	dBc
Output Mismatch Stress (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz, Load VSWR = 5:1 (all phase angles))	ψ	No Degradation in Output Power Before and After Test			



B1, B2, B3, B4 — Ferrite Bead, Fair Rite #2743019447
C1 — 0.8–8.0 pF Trimmer Capacitor, Johanson
C2, C3, C23, C24 — 43 pF, 100 mil, ATC Chip Capacitor
C4, C5, C18, C19, C21, C22 — 820 pF, 100 mil, Chip Capacitor, Kemet
C6, C7, C11, C12 — 10 μF, Lytic Capacitor, Panasonic
C8, C9, C16, C17 — 100 pF, 100 mil, Chip Capacitor, Murata Erie
C10 — 13 pF, 50 mil, ATC Chip Capacitor
C13, C14 — 250 μF Lytic Capacitor, Mallory
C15 — 1.1 pF, 50 mil, ATC Chip Capacitor
C20 — 6.8 pF, 100 mil, ATC Chip Capacitor
L1, L2, L3, L4, L5, L6 — 5 Turns 20 AWG, IDIA 0.126″ choke
N1, N2 — Type N Flange Mount, Omni Spectra 3052–1648–10
Q1 — Bias Transistor BD136 PNP
R1, R12 — 39 Ohm, 2.0 W
R3, R4, R5, R6 — 4.0 x 39 Ohm, 1/8 W, Chips in Parallel, Rohm 390–J
TL1–TL11 — See Photomaster
Balun1, Balun2, Coax 1, Coax 2 — 2.20″ 50 Ohm, 0.088″ o.d. semi–rigid coax, Micro Coax UT–85–M17
Board — 1/32″ Glass Teflon, Arlon GX–0300–55–22, ε_r = 2.55

Figure 1. MRF897 Broadband Test Circuit

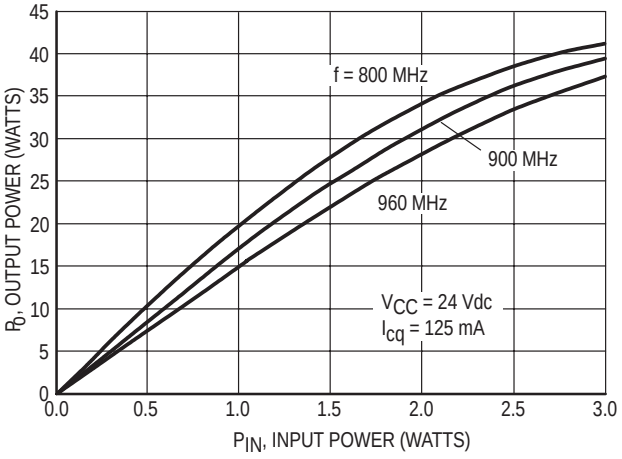


Figure 2. Output Power versus Input Power

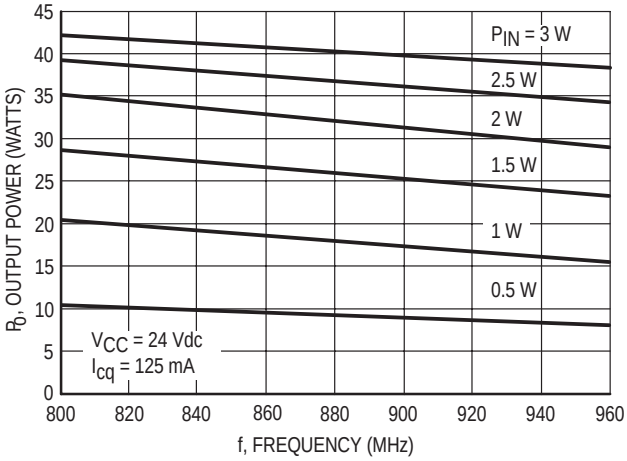


Figure 3. Output Power versus Frequency

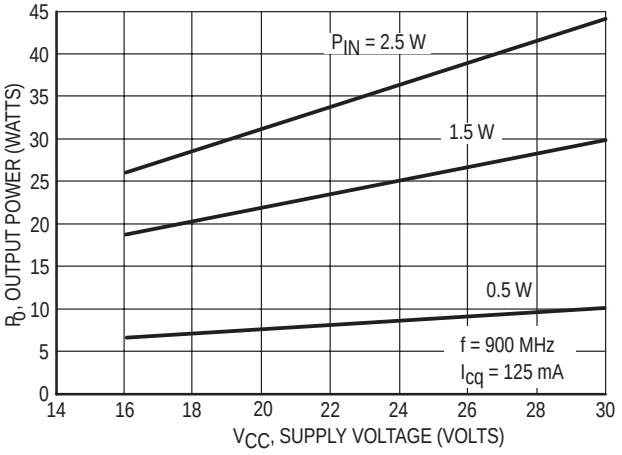


Figure 4. Output Power versus Supply Voltage

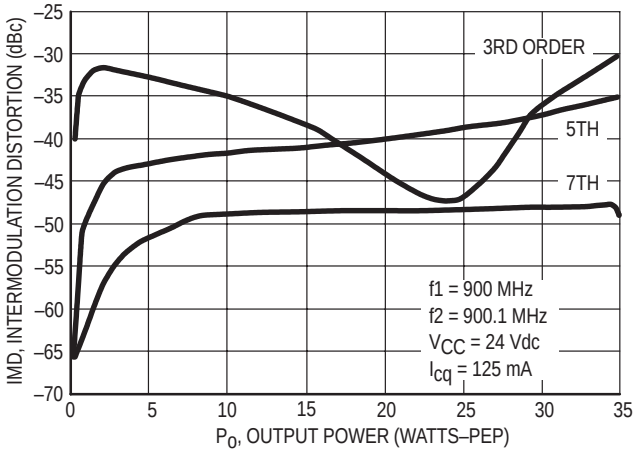


Figure 5. Intermodulation versus Output Power

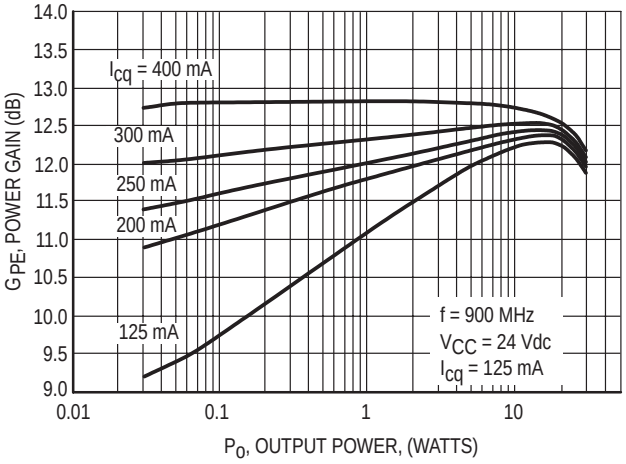


Figure 6. Power Gain versus Output Power

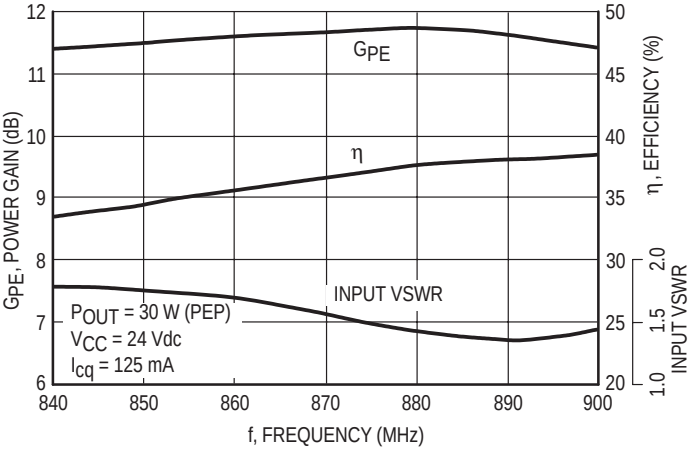
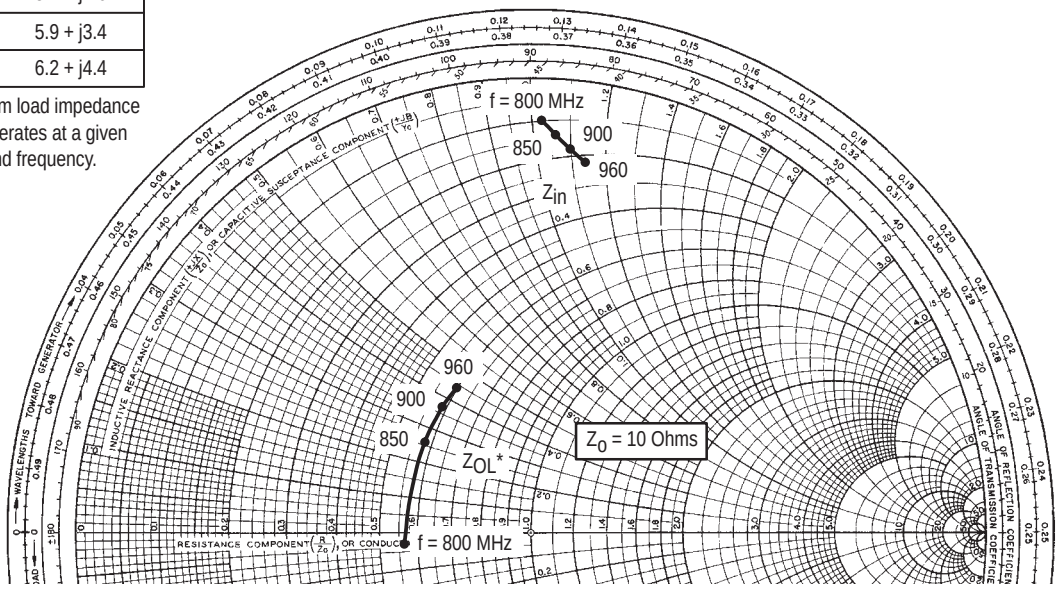


Figure 7. Broadband Test Fixture Performance

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	1.0 + j10.3	5.9 – j0.4
850	1.5 + j10.5	5.7 + j2.6
900	1.8 + j11.0	5.9 + j3.4
960	2.2 + j11.4	6.2 + j4.4

Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.



NOTE: Z_{in} & Z_{OL}* are given from base–to–base and collector–to–collector respectively.

P_0 = 300 W (PEP), V_{CC} = 24 V

Figure 8. Series Equivalent Input/Output Impedances

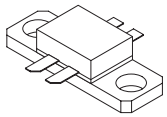
The RF Line
NPN Silicon RF Power Transistor

MRF897R

Designed for 24 Volt UHF large–signal, common emitter, class–AB linear amplifier applications in industrial and commercial FM/AM equipment operating in the range 800–970 MHz.

- Specified 24 Volt, 900 MHz Characteristics
  - Output Power = 30 Watts
  - Minimum Gain = 10.5 dB @ 900 MHz, class–AB
  - Minimum Efficiency = 30% @ 900 MHz, 30 Watts (PEP)
  - Maximum Intermodulation Distortion –30 dBc @ 30 Watts (PEP)
- Characterized with Series Equivalent Large–Signal Parameters from 800 to 960 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 26 Vdc, and Rated Output Power
- Gold Metalized, Emitter Ballasted for Long Life and Resistance to Metal–Migration

30 W, 900 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 395E–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector–Current — Continuous	I_C	4.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	105 0.60	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W

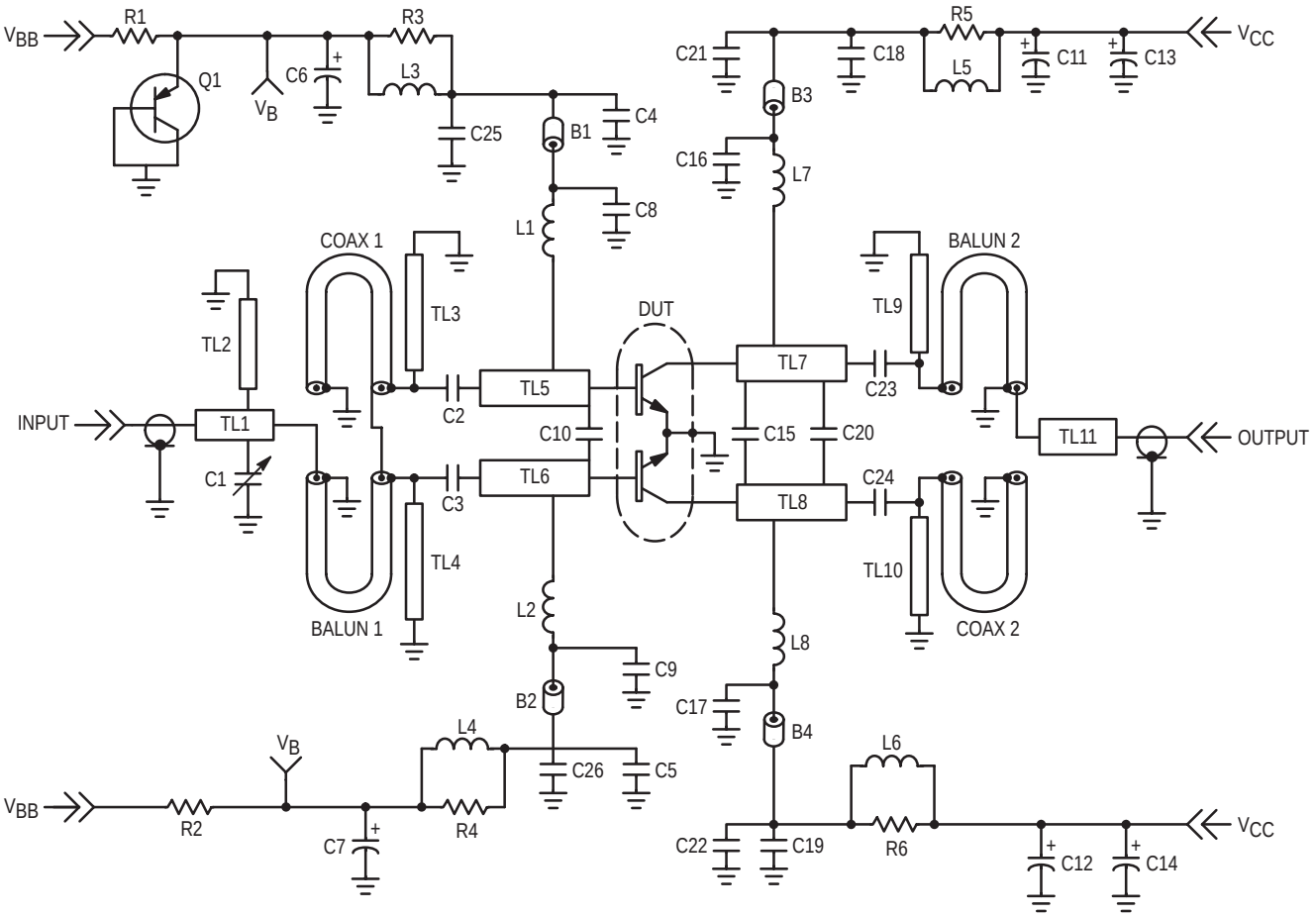
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	33	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	80	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	4.7	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	10.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1.0 Adc, V_{CE} = 5 Vdc)	h_{FE}	30	80	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	14	21	28	pF

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL CHARACTERISTICS					
Common–Emitter Amplifier Power Gain (V_{CC} = 24 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	G_{pe}	10.5	12.0	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	η	30	38	—	%
Intermodulation Distortion (V_{CC} = 24 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	IMD	—	–37	–30	dBc
Output Mismatch Stress (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz, Load VSWR = 5:1 (all phase angles))	ψ	No Degradation in Output Power			



B1, B2, B3, B4 — Short Ferrite Bead, Fair Rite #2743019447
C1 — 0.8–8.0 pF Var Capacitor, Johansen Gigatrim
C2, C3, C23, C24 — 43 pF, 100 mil, ATC Chip Capacitor
C4, C5, C21, C22 — 1000 pF, 100 mil, ATC Chip Capacitor
C6, C7, C11, C12 — 10 μF, Electrolytic Capacitor, Panasonic
C8, C9, C16, C17 — 100 pF, 100 mil, ATC Chip Capacitor
C10 — 9.1 pF, 50 mil, ATC Chip Capacitor
C13 — 250 μF Electrolytic Capacitor, Mallory
C14, C18, C19, C25 — 0.1 μF, Chip Capacitor, Kemet
C15 — 1.1 pF, 50 mil, ATC Chip Capacitor
C20 — 6.8 pF, 100 mil, ATC Chip Capacitor
L1, L2, L3, L4, L5, L6, L7, L8 — 5 Turns 20 AWG, IDIA 0.126″ Choke, Taylor Spring 46 nH
N1, N2 — Type N Flange Mount, Omni Spectra 3052–1648–10
Q1 — Bias Transistor BD136 PNP
R1, R12 — 27 Ohm, 2.0 W
R3, R4, R5, R6 — 4.0 x 39 Ohm, 1/8 W, Chips Resistors in Parallel, Rohm 390–J
SB1 — 0.15″ x 0.3″ x 0.03″ Cu
TL1–TL11 — Microstrip Line, See Photomaster
Balun1, Balun2, Coax 1, Coax 2 — 2.20″ 50 Ohm, 0.086″ o.d. semi–rigid coax, Micro Coax UT–85–M17
Circuit Board — 1/32″ Glass Teflon, Arlon GX–0300–55–22, ε_r = 2.55

Figure 1. 840–900 MHz Test Circuit Schematic

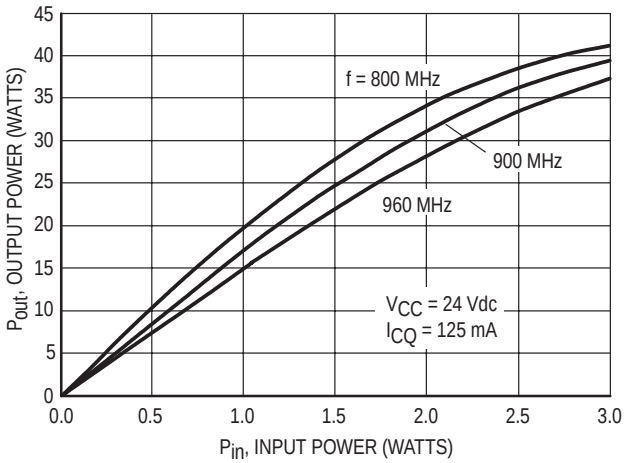


Figure 2. Output Power versus Input Power

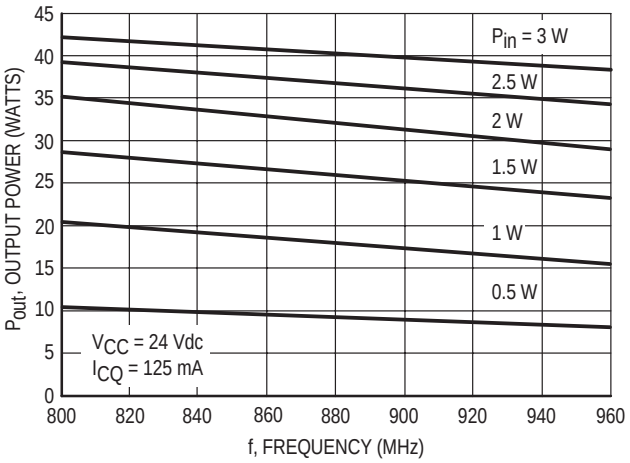


Figure 3. Output Power versus Frequency

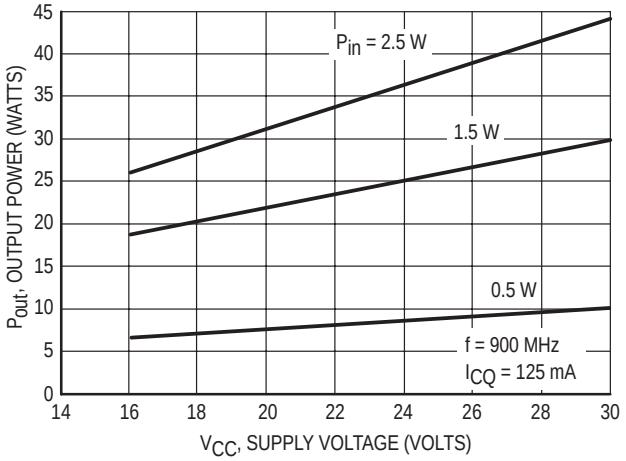


Figure 4. Output Power versus Supply Voltage

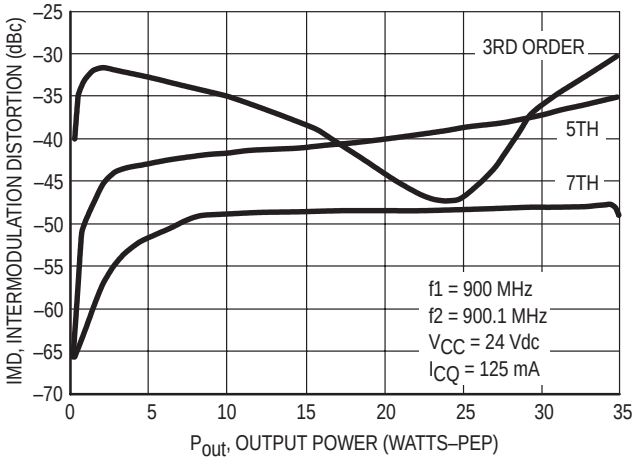


Figure 5. Intermodulation versus Output Power

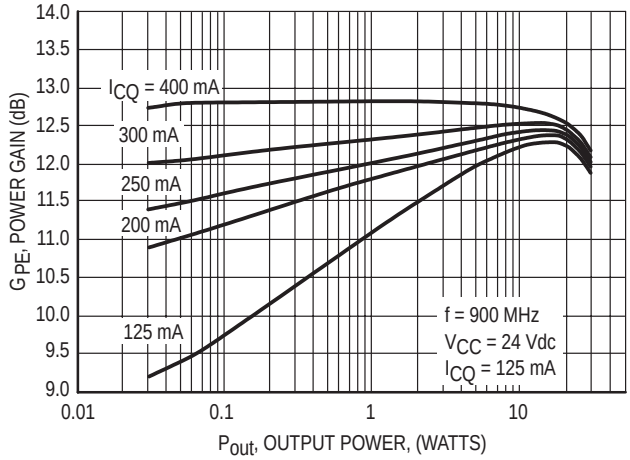


Figure 6. Power Gain versus Output Power

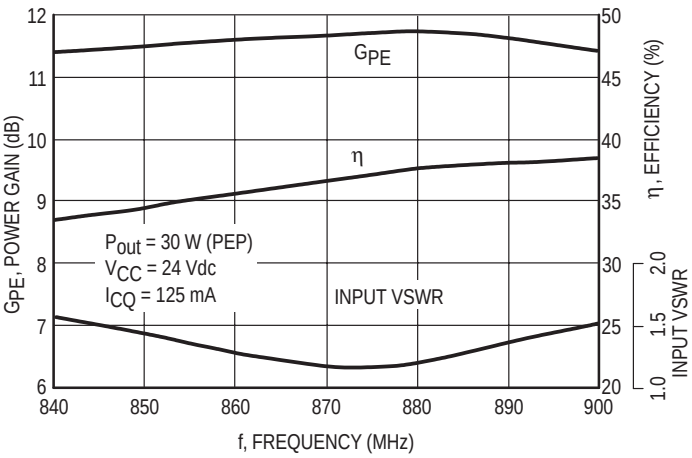
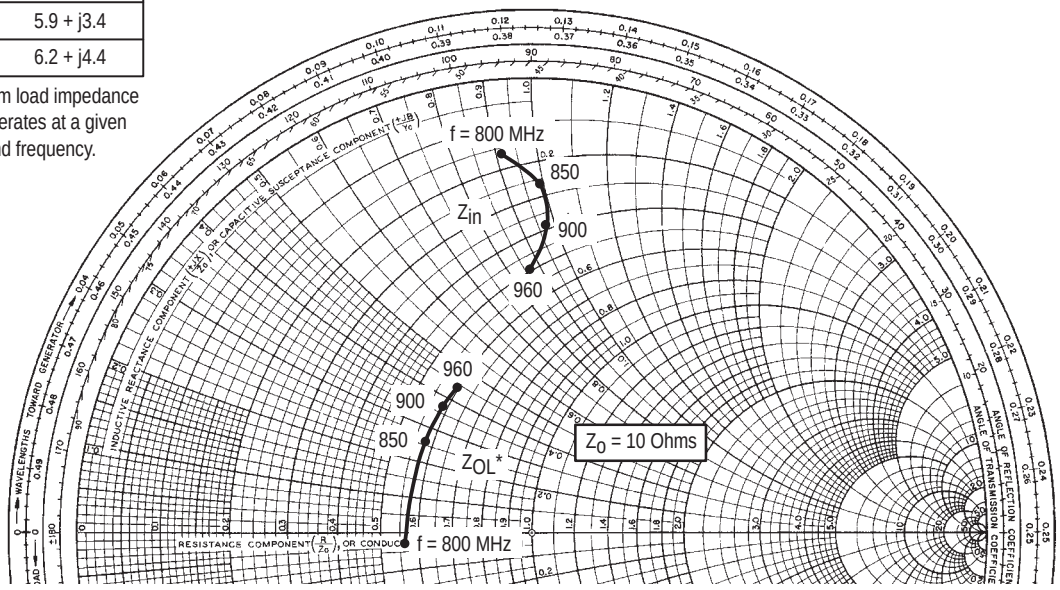


Figure 7. Broadband Test Fixture Performance

P_{out} = 30 W (PEP), V_{CC} = 24 V

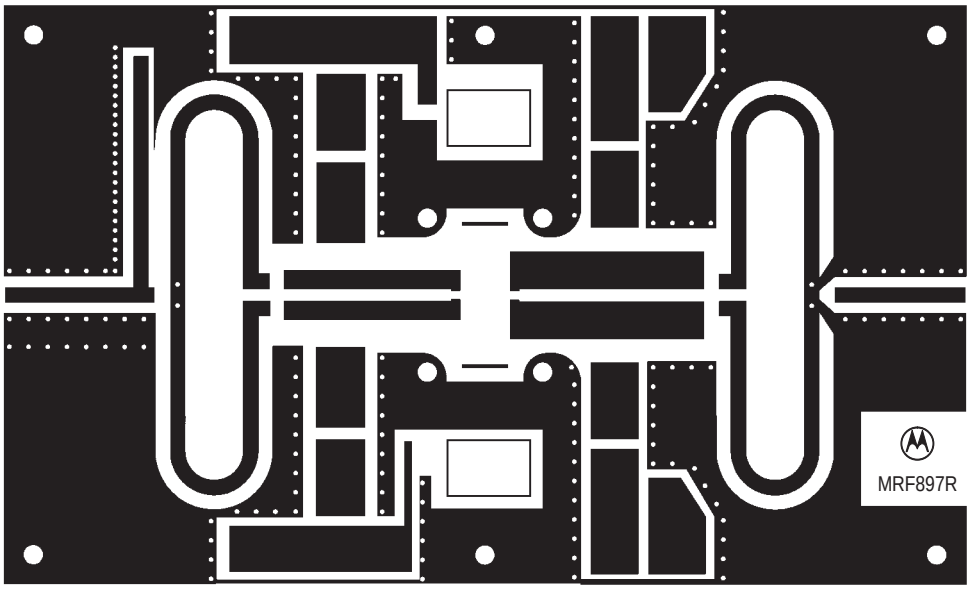
f MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	1.7 + j9.2	5.9 – j0.4
850	2.6 + j10	5.7 + j2.6
900	4 + j9.9	5.9 + j3.4
950	5 + j8.8	6.2 + j4.4

Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.



NOTE: Z_{in} & Z_{OL}* are given from base–to–base and collector–to–collector respectively.

Figure 8. Series Equivalent Input/Output Impedances



(SCALE: 1:1)

Figure 9. MRF897R Photomaster
(Reduced 25% in printed data book, DL110/D)

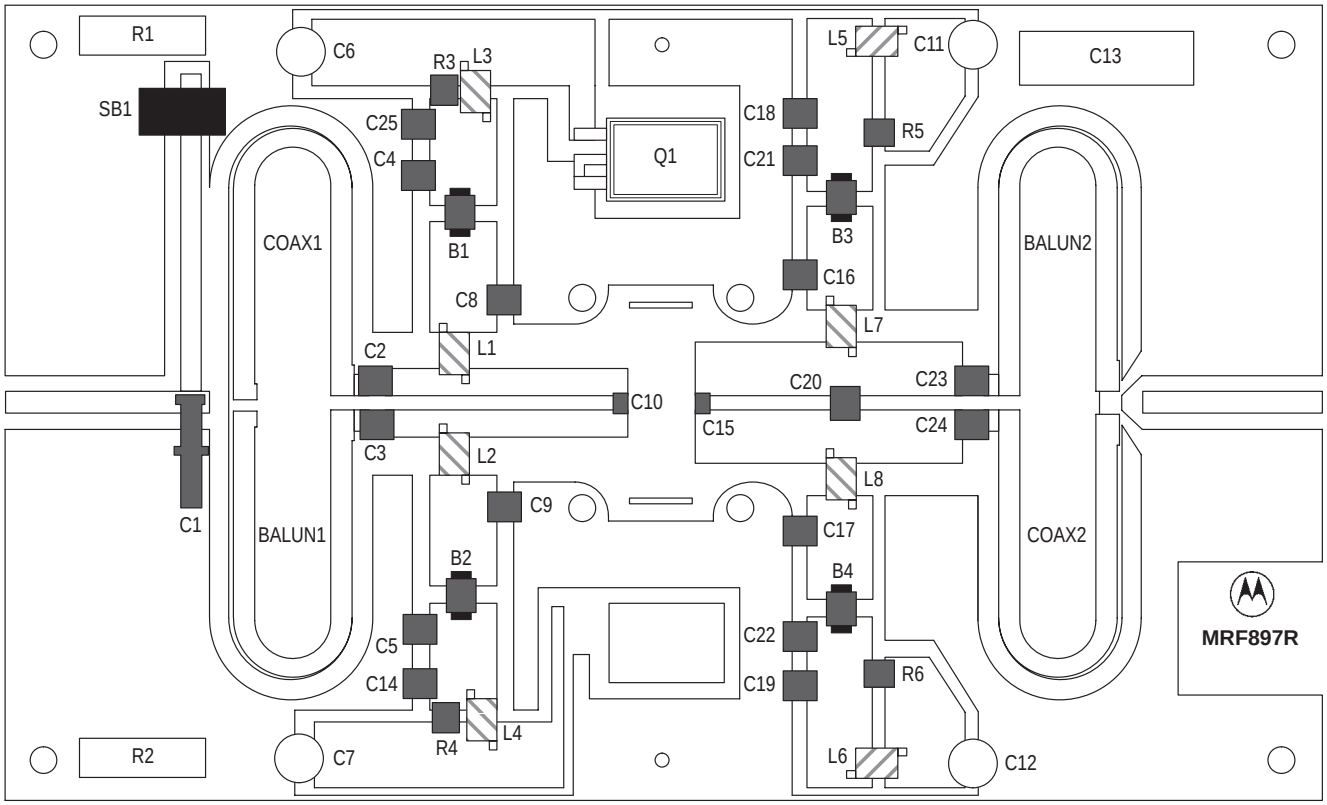


Figure 10. 840 – 900 MHz Test Circuit Component Layout

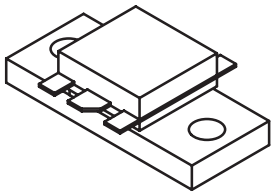
The RF Line
NPN Silicon RF Power Transistor

. . . designed for 24 Volt UHF large–signal, common base amplifier applications in industrial and commercial FM equipment operating in the range of 850–960 MHz.

- Motorola Advanced Amplifier Concept Package
- Specified 24 Volt, 900 MHz Characteristics
  Output Power = 60 Watts
  Power Gain = 7.0 dB Min
  Efficiency = 60% Min
- Double Input/Output Matched for Wideband Performance and Simplified External Matching
- Series Equivalent Large–Signal Characterization
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

MRF898

60 W, 850–960 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 333A–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	55	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	10	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	175 1.0	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

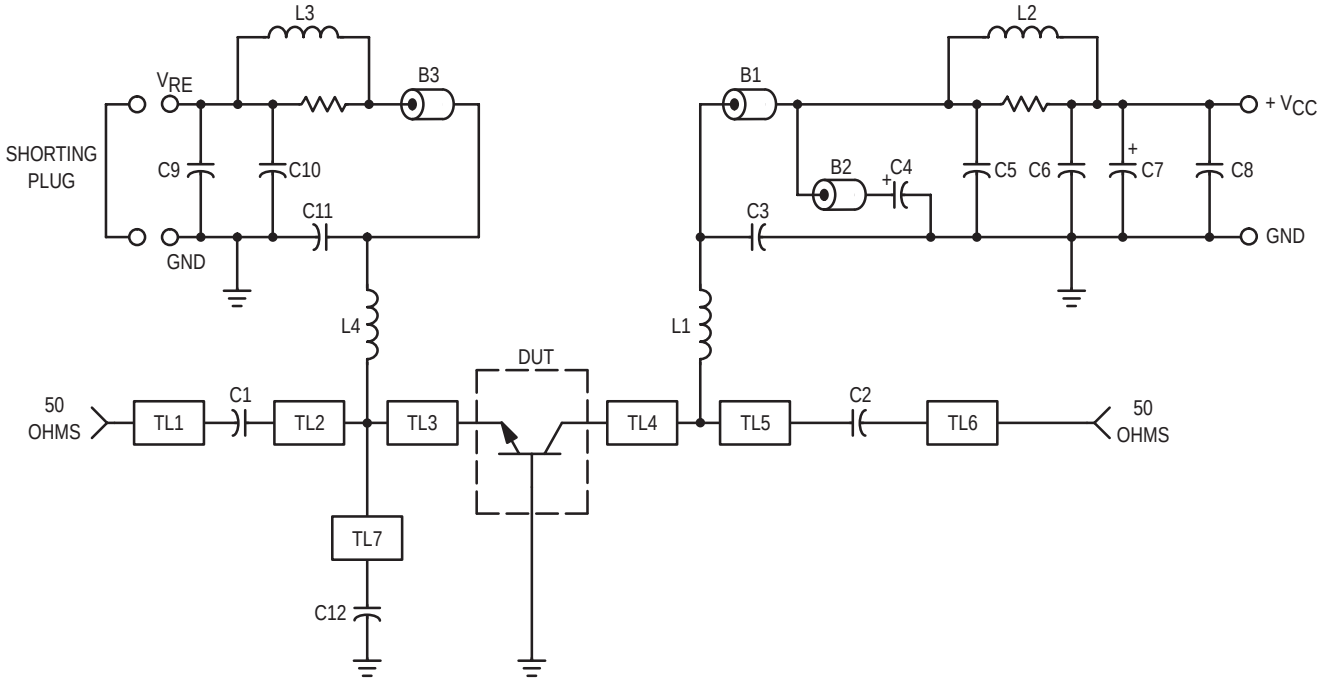
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	10	mAdc

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	50	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (1) (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	60	—	pF
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CC} = 24 Vdc, P_{out} = 60 W, f = 900 MHz)	G_{pb}	7.0	7.9	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 60 W, f = 900 MHz)	η	60	65	—	%
Output Mismatch Stress (V_{CC} = 24 Vdc, P_{out} = 60 W, f = 900 MHz, VSWR = 5:1, all phase angles)	ψ	No Degradation in Output Power			

NOTE:
1. Value of "C_{ob}" is that of die only. It is not measurable in MRF898 because of internal matching network.



B1, B2, B3 — Bead, Ferroxcube 56–390–65/3B
C1, C2, C12 — 39 pF, 100 Mil Chip Capacitor
C3, C11 — 91 pF, Mini Underwood or Equivalent
C4, C7, C9 — 10 μF, 35 V Electrolytic
C5 — 4000 pF, 1.0 kV Ceramic
C6, C10 — 1000 pF, 350 V Unelco or Equivalent
C8 — 47 pF, 100 Mil Chip Capacitor
L1, L4 — 4 Turns #18 AWG Choke
L2 — 11 Turns #20 AWG Choke on 10 Ohm, 1.0 Watt Resistor
L3 — 3 Turns #18 AWG Choke on 10 Ohm, 1.0 Watt Resistor

TL1, TL6 — 50 Ohm Microstrip
TL2 — 400 x 950 Mils
TL3, TL4 — 140 x 200 Mils
TL5 — 320 x 690 Mils
TL7 — 260 x 230 Mils
Board — 3M Epsilam–10, 50 Mil
Bias Boards — 1/32″ G10 or Equivalent

Figure 1. 850 – 960 MHz Broadband Test Circuit

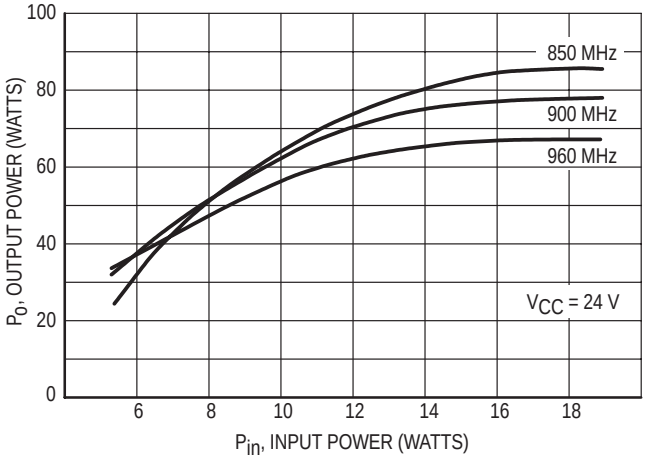


Figure 2. Output Power versus Input Power

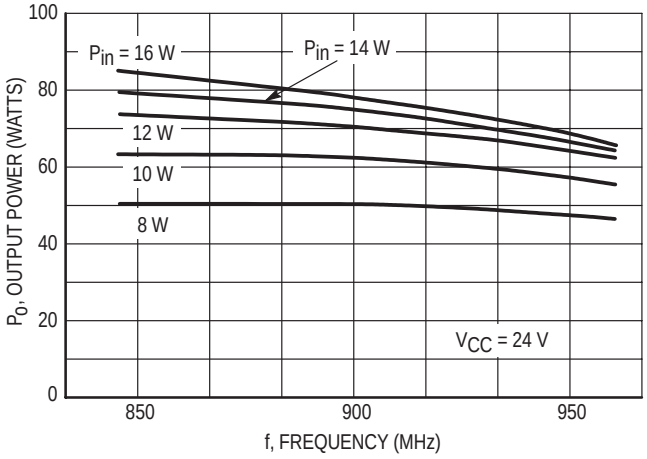


Figure 3. Output Power versus Frequency

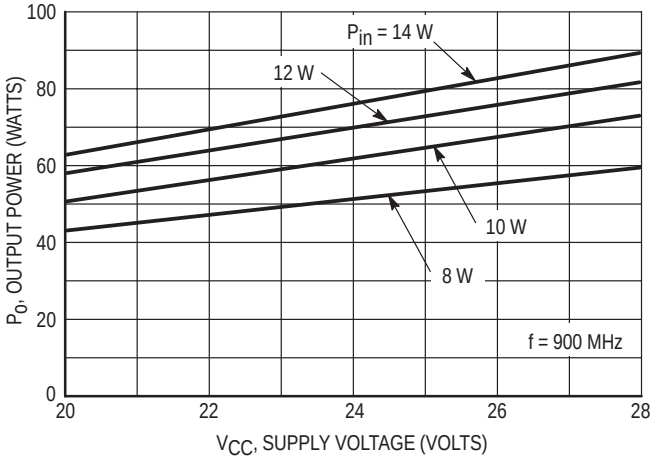


Figure 4. Output Power versus Supply Voltage

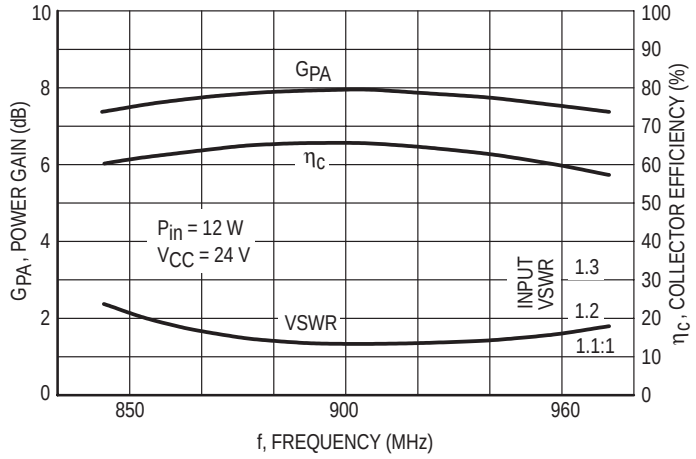
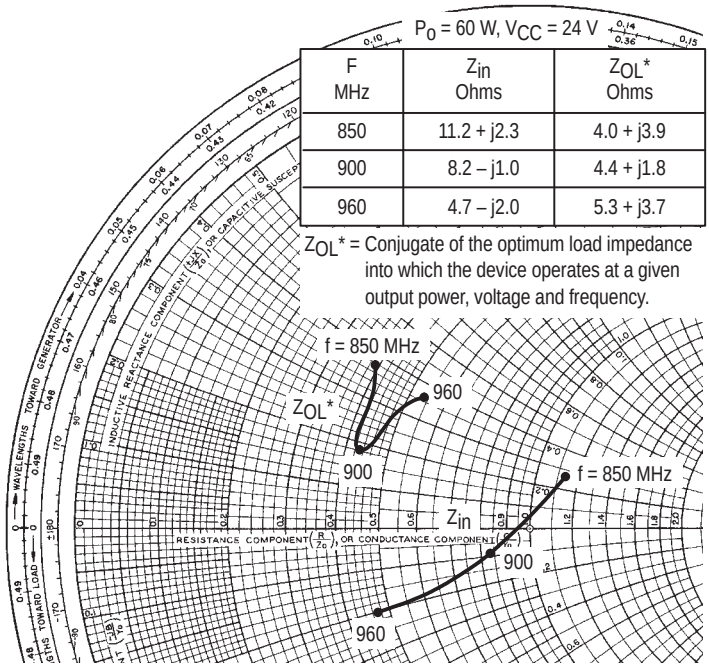


Figure 5. Typical Broadband Circuit Performance



F MHz	Z_{in} Ohms	Z_{OL}* Ohms
850	11.2 + j2.3	4.0 + j3.9
900	8.2 – j1.0	4.4 + j1.8
960	4.7 – j2.0	5.3 + j3.7

Figure 6. Input/Output Impedance versus Frequency

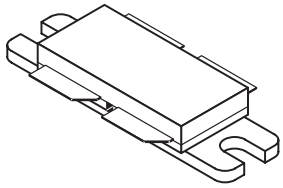
The RF Line
NPN Silicon RF Power Transistor

MRF899

Designed for 26 Volt UHF large–signal, common emitter, Class AB linear amplifier applications in industrial and commercial FM / AM equipment operating in the range 800 – 960 MHz.

- Specified 26 Volt, 900 MHz Characteristics
  - Output Power = 150 Watts (PEP)
  - Minimum Gain = 8.0 dB @ 900 MHz, Class AB
  - Minimum Efficiency = 35% @ 900 MHz, 150 Watts (PEP)
  - Maximum Intermodulation Distortion – 28 dBc @ 150 Watts (PEP)
- Characterized with Series Equivalent Large–Signal Parameters from 800 to 960 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 26 Vdc, and Rated Output Power
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

150 W, 900 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 375A–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	28	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector–Current — Continuous	I_C	25	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	230 1.33	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

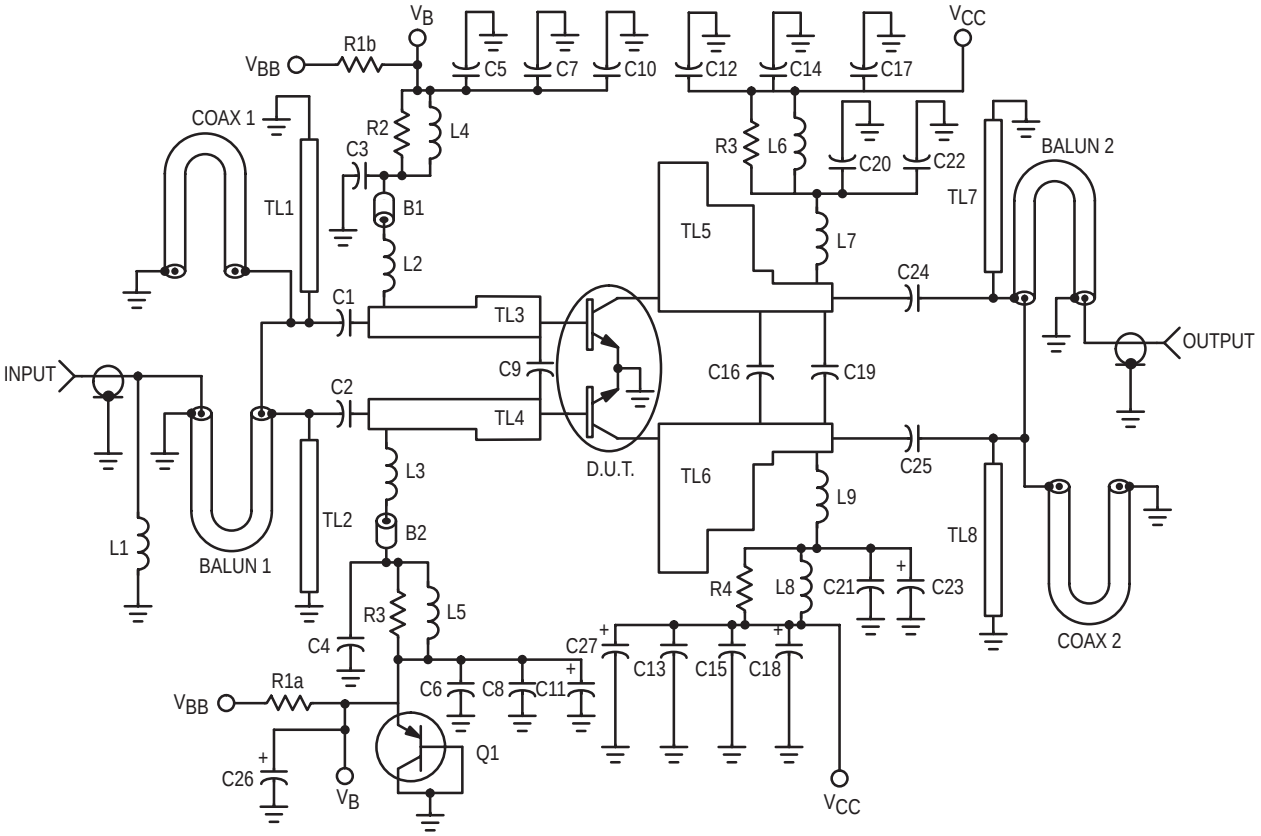
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	28	37	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	85	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	4.9	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	30	75	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 Vdc, I_E = 0, f = 1.0 MHz) (1)	C_{ob}	—	75	—	pF

(1) For information only. This part is collector matched.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL CHARACTERISTICS					
Common–Emitter Amplifier Power Gain V_{CC} = 26 Vdc, P_{out} = 150 Watts (PEP), I_{cq} = 300 mA, f_1 = 900 MHz, f_2 = 900.1 MHz	G_{pe}	8.0	9.0	—	dB
Collector Efficiency V_{CC} = 26 Vdc, P_{out} = 150 Watts (PEP), I_{cq} = 300 mA, f_1 = 900 MHz, f_2 = 900.1 MHz	η	30	40	—	%
3rd Order Intermodulation Distortion V_{CC} = 26 Vdc, P_{out} = 150 Watts (PEP), I_{cq} = 300 mA, f_1 = 900 MHz, f_2 = 900.1 MHz	IMD	—	–32	–28	dBc
Output Mismatch Stress V_{CC} = 26 Vdc, P_{out} = 150 Watts (PEP), I_{cq} = 300 mA, f_1 = 900 MHz, f_2 = 900.1 MHz, VSWR = 5:1 (all phase angles)	ψ	No Degradation in Output Power Before and After Test			



B1, B2 — Ferrite Bead, Ferroxcube #56–590–65–3B
C1, C2, C24, C25 — 43 pF, B Case, ATC Chip Capacitor
C3, C4, C20, C21 — 100 pF, B Case, ATC Chip Capacitor
C5, C6, C12, C13 — 1000 pF, B Case, ATC Chip Capacitor
C7, C8, C14, C15 — 1800 pF, AVX Chip Capacitor
C9 — 9.1 pF, A Case, ATC Chip Capacitor
C10, C11, C17, C18, C22, C23 — 10 μF, Electrolytic Capacitor Panasonic
C16 — 3.9 pF, B Case, ATC Chip Capacitor
C19 — 0.8 pF, B Case, ATC Chip Capacitor
C26 — 200 μF, Electrolytic Capacitor Mallory Sprague
C27 — 500 μF Electrolytic Capacitor
L1 — 5 Turns 24 AWG IDIA 0.059″ Choke, 19.8 nH
L2, L3, L7, L9 — 4 Turns 20 AWG IDIA 0.163″ Choke
L4, L5, L6, L8 — 12 Turns 22 AWG IDIA 0.140″ Choke
N1, N2 — Type N Flange Mount, Omni Spectra
Q1 — Bias Transistor BD136 PNP
R2, R3, R4, R5 — 4.0 x 39 Ohm 1/8 W Chips in Parallel
R1a, R1b — 56 Ohm 1.0 W
TL1–TL8 — See Photomaster
Balun1, Balun2, Coax 1, Coax 2 — 2.20″ 50 Ohm 0.088″ o.d. Semi–rigid Coax, Micro Coax
Board — 1/32″ Glass Teflon, ε_r = 2.55″ Arlon (GX–0300–55–22)

Figure 1. 900 MHz Power Gain Test Circuit

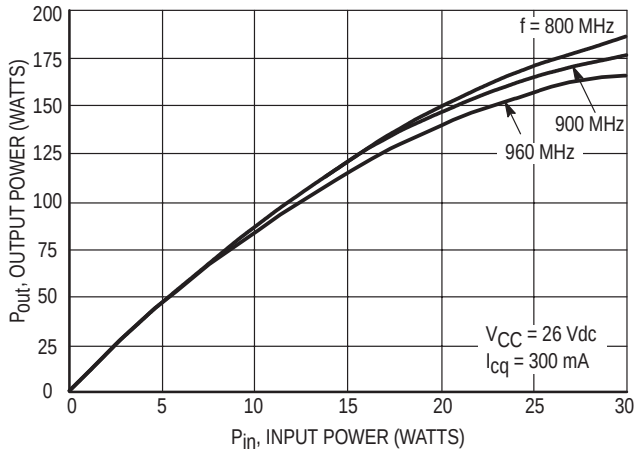


Figure 2. Output Power versus Input Power

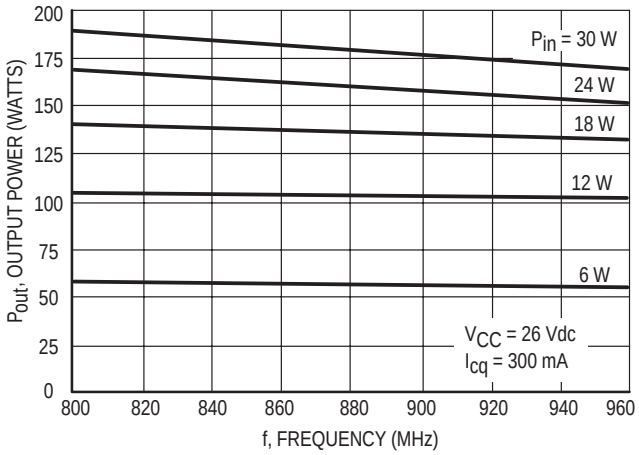


Figure 3. Output Power versus Frequency

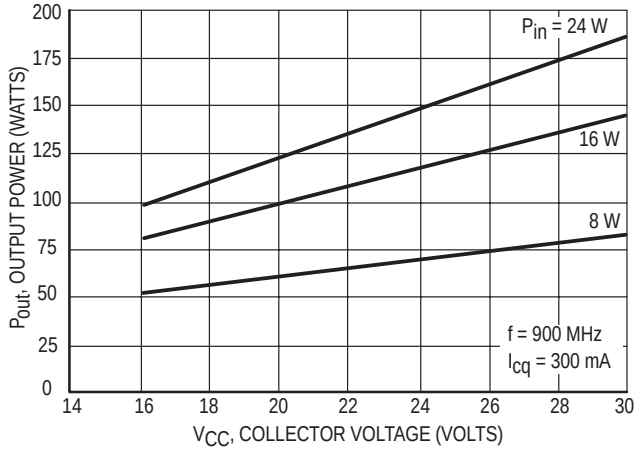


Figure 4. Output Power versus Supply Voltage

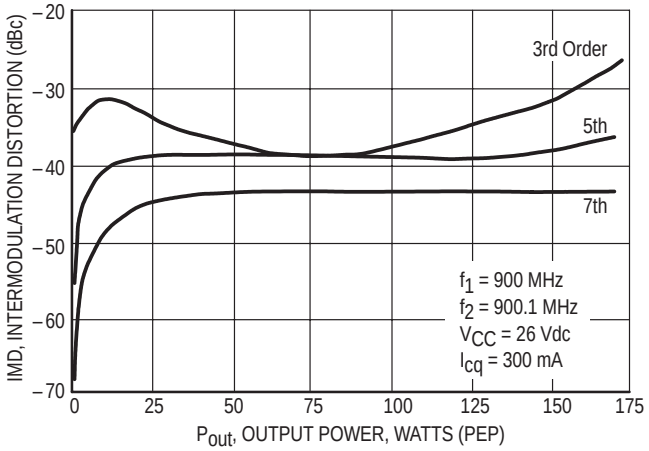


Figure 5. Intermodulation versus Output Power

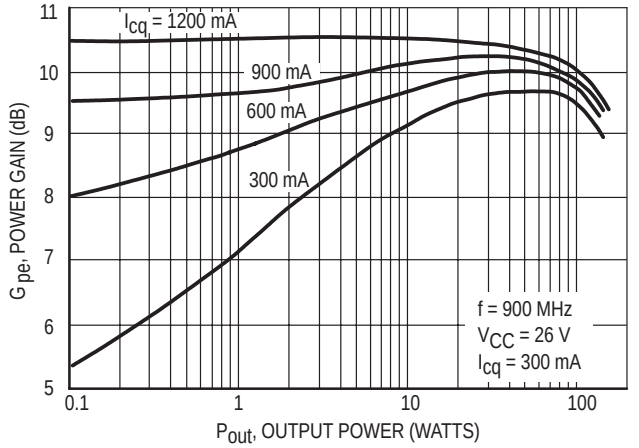


Figure 6. Power Gain versus Output Power

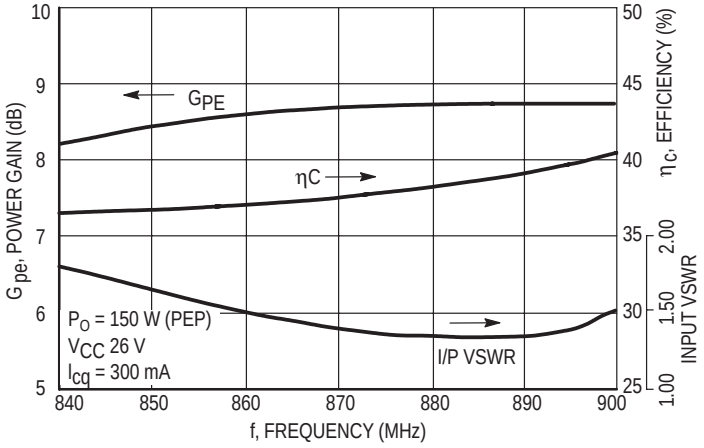
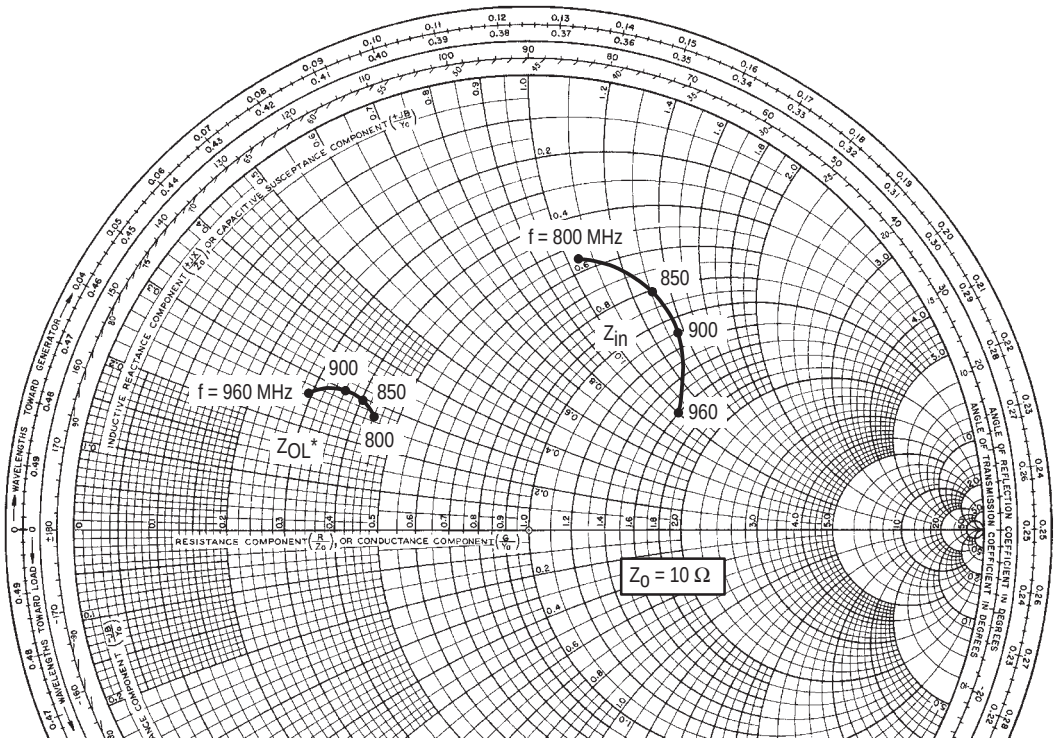


Figure 7. Broadband Test Fixture Performance



f MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	5.51 + j10.6	4.52 + j2.64
850	8.17 + j13.2	4.21 + j2.98
900	11.2 + j13.8	3.68 + j2.97
960	16.8 + j10.1	2.98 + j2.71

Z_{OL}* = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.

NOTE: Z_{in} & Z_{OL}* are given from base–to–base and collector–to–collector respectively

Figure 8. Input and Output Impedances with Circuit Tuned for Maximum Gain @ P_o = 150 W (PEP), V_{CC} = 26 V

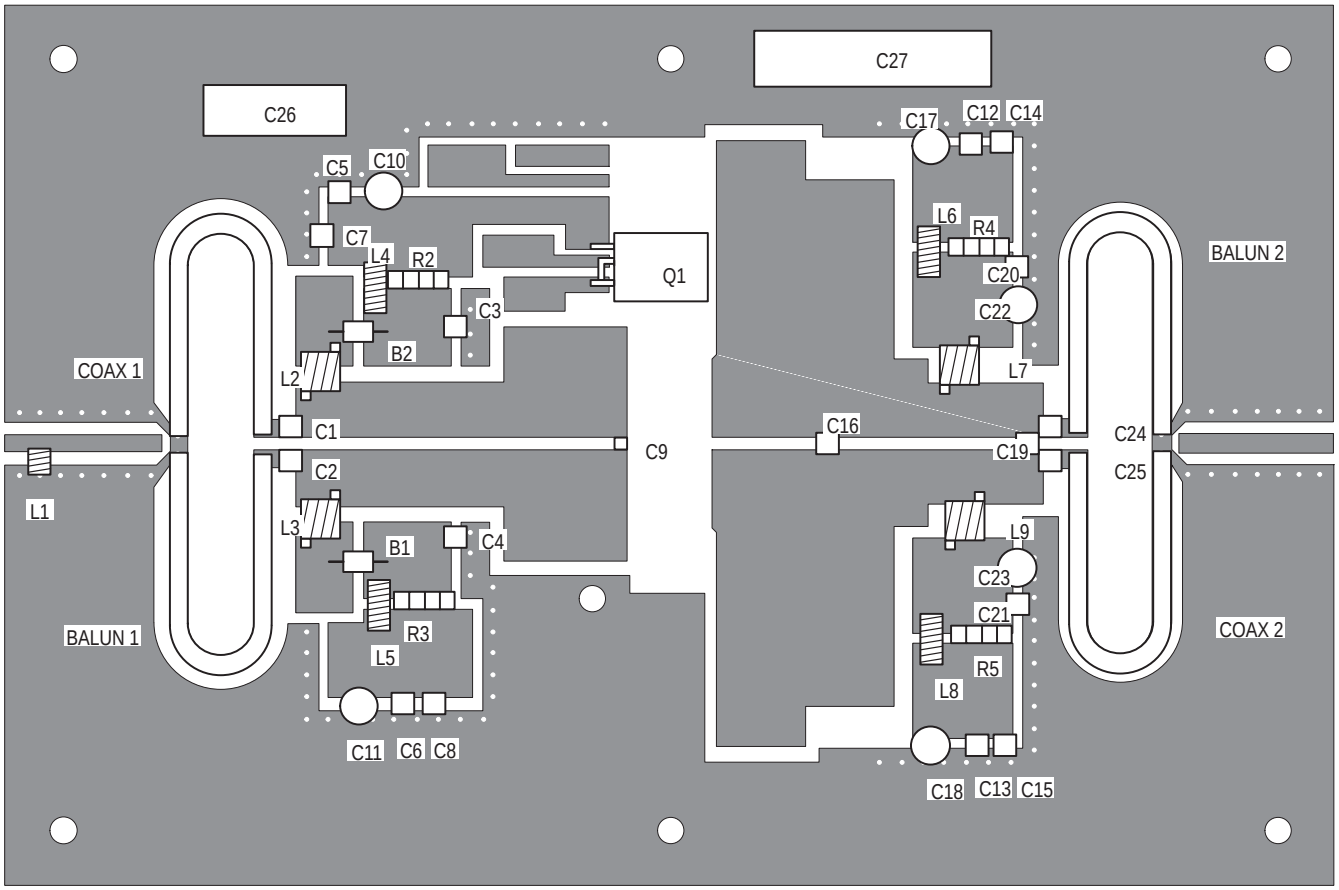


Figure 9. MRF899 Test Fixture Component Layout

MOTOROLA

MRF949T1

NPN Silicon Low Noise Transistors

Motorola's MRF949 is a high performance NPN transistor designed for use in high gain, low noise small–signal amplifiers. The MRF949 is well suited for low voltage wireless applications. This device features a 9.0 GHz DC current gain–bandwidth product with excellent linearity.

- Low Noise Figure, NF_{min} = 1.4 dB (Typ) @ 1.0 GHz, 8.0 V, 3.0 mA
- High Current Gain–Bandwidth Product, f_τ = 9.0 GHz, 6.0 V, 15 mA
- Maximum Stable Gain, 19 dB @ 1.0 GHz, 6.0 V, 10 mA
- Output Third Order Intercept, Output IP_3 = 29 dBm @ 1.0 GHz, 6.0 V, 10 mA
- Fully Ion–Implanted with Gold Metallization and Nitride Passivation

LOW NOISE TRANSISTORS

f_τ = 9.0 GHz

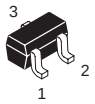
NF_{min} = 1.4 dB

I_{CMAX} = 50 mA

V_{CEO} = 10 V

SEMICONDUCTOR TECHNICAL DATA

Pin 1. Base
2. Emitter
3. Collector



PLASTIC PACKAGE
CASE 463
(SC–90/SC–75, Tape & Reel Only)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	10	Vdc
Collector–Base Voltage	V_{CBO}	20	Vdc
Emitter–Base Voltage	V_{EBO}	1.5	Vdc
Power Dissipation @ T_C = 75°C Derate linearly above T_C = 75°C at	$P_{D(max)}$	0.144 1.92	W mW/°C
Collector Current – Continuous [Note 3]	I_C	50	mA
Storage Temperature	T_{stg}	–55 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$	150	°C

NOTES: 1. Meets Human Body Model (HBM) ≤300 V and Machine Model (MM) ≤75 V.
2. ESD data available upon request.
3. For MTBF >10 years.

THERMAL CHARACTERISTIC

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	520	°C/W

NOTE: To calculate the junction temperature use $T_J = (P_D \times R_{\theta JC}) + T_C$. The case temperature measured on collector lead adjacent to the package body.

ORDERING INFORMATION

Device	Marking	Package
MRF949T1	JL	SC–90/SC75 Tape & Reel*

*3,000 Units per 8 mm, 7 inch reel.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS [Note 1]					
Collector–Emitter Breakdown Voltage (I_C = 0.1 mA, I_B = 0)	$V_{(BR)CEO}$	10	12	–	Vdc
Collector–Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)	$V_{(BR)CBO}$	20	23	–	Vdc
Emitter Cutoff Current (V_{EB} = 1.0 V, I_C = 0)	I_{EBO}	–	–	0.1	μA
Collector Cutoff Current (V_{CB} = 10 V, I_E = 0)	I_{CBO}	–	–	0.1	μA
ON CHARACTERISTICS [Note 1]					
DC Current Gain (V_{CE} = 6.0 V, I_C = 5.0 mA)	h_{FE}	50	–	–	–
DYNAMIC CHARACTERISTICS					
Collector–Base Capacitance	C_{cb}				pF
(V_{CB} = 1.0 V, I_E = 0, f = 1.0 MHz)		–	0.4	–	
(V_{CB} = 5.0 V, I_E = 0, f = 1.0 MHz)		–	0.3	–	
Current–Gain Bandwidth Product (V_{CE} = 6.0 V, I_C = 30 mA, f = 1.0 GHz)	f_τ	–	9.0	–	GHz
PERFORMANCE CHARACTERISTICS					
Insertion Gain	$\|S_{21}\|^2$				dB
(V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz)		–	7.0	–	
(V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)		–	15	–	
Maximum Unilateral Gain [Note 2]	G_{Umax}				dB
(V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz)		–	13	–	
(V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)		–	17	–	
Maximum Stable Gain and/or Maximum Available Gain [Note 3]					dB
(V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz)	MSG	–	12	–	
(V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)	MAG	–	18	–	
Noise Figure – Minimum	NF_{min}				dB
(V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz)		–	1.6	–	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)		–	1.4	–	
Noise Resistance	R_N				Ω
(V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz)		–	24	–	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)		–	19	–	
Associated Gain at Minimum NF	G_{NF}				dB
(V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz)		–	10	–	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)		–	15	–	
Output Power at 1.0 dB Gain Compression [Note 4] (V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)	P_{1dB}	–	13	–	dBm
Output Third Order Intercept [Note 4] (V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)	OIP_3	–	28	–	dBm

NOTES: 1. Pulse width ≤300 μs, duty cycle ≤2% pulsed.

2. Maximum unilateral gain is:

$$G_{Umax} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$$

3. Maximum Available Gain and Maximum Stable Gain are defined by the K factor as follows:

$$MAG = \left|\frac{S_{21}}{S_{12}}\left(K \pm \sqrt{K^2-1}\right)\right|, \text{ if } K > 1, \; MSG = \left|\frac{S_{21}}{S_{12}}\right|, \text{ if } K < 1$$

4. Z_{in} = 50 Ω and Z_{out} matched for optimum IP_3.

TYPICAL CHARACTERISTICS

Figure 1. Capacitance versus Voltage

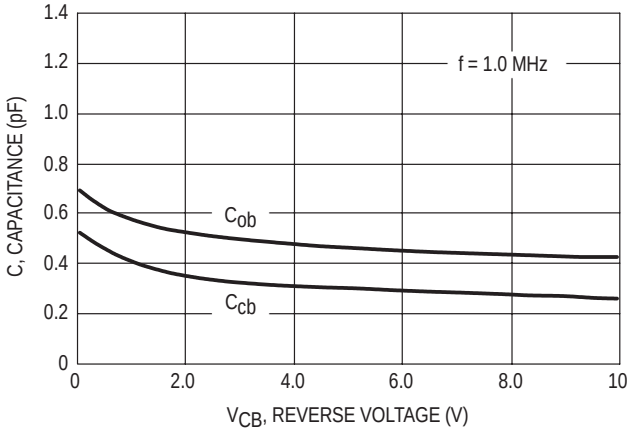


Figure 2. Input Capacitance versus Voltage

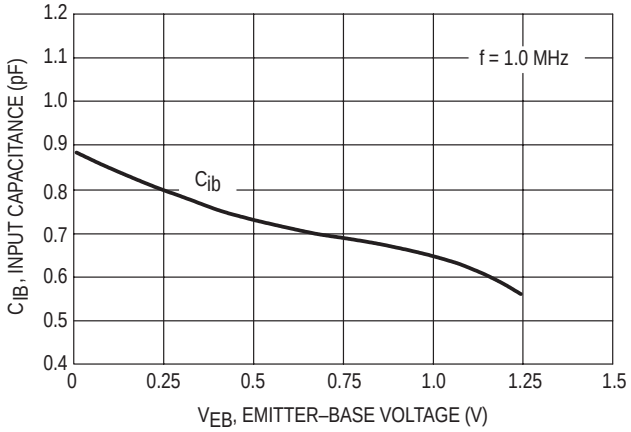


Figure 3. DC Current Gain versus Collector Current

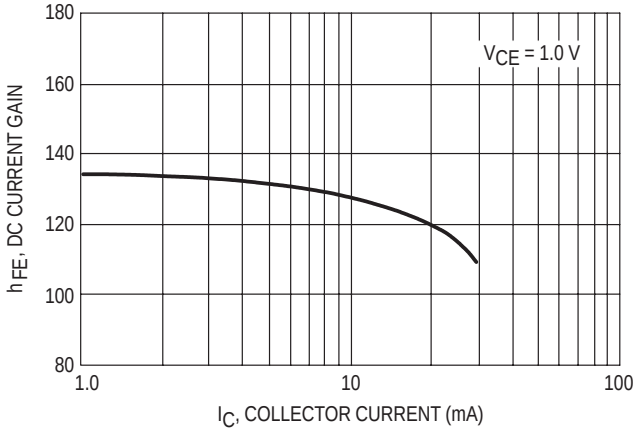


Figure 4. Gain–Bandwidth Product versus Collector Current

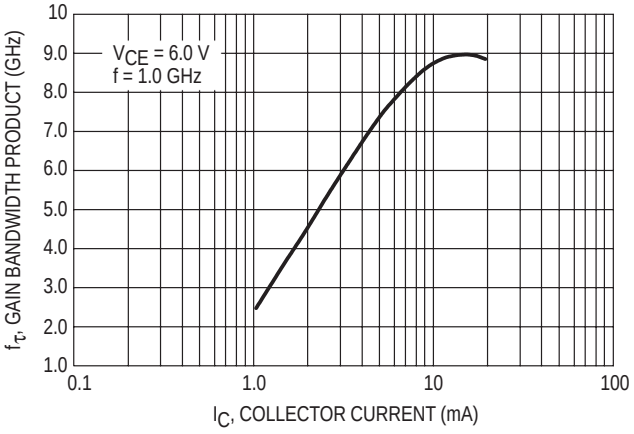
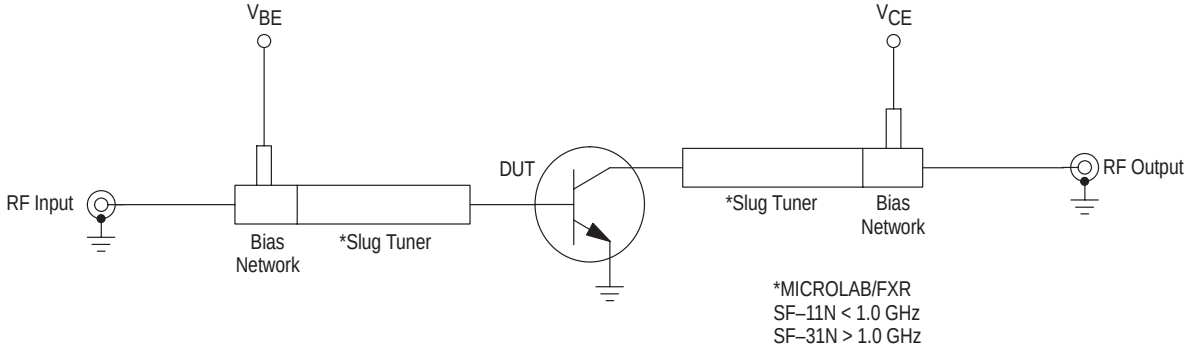


Figure 5. Functional Circuit Schematic



TYPICAL CHARACTERISTICS

Figure 6. Maximum Stable/Available Gain versus Frequency

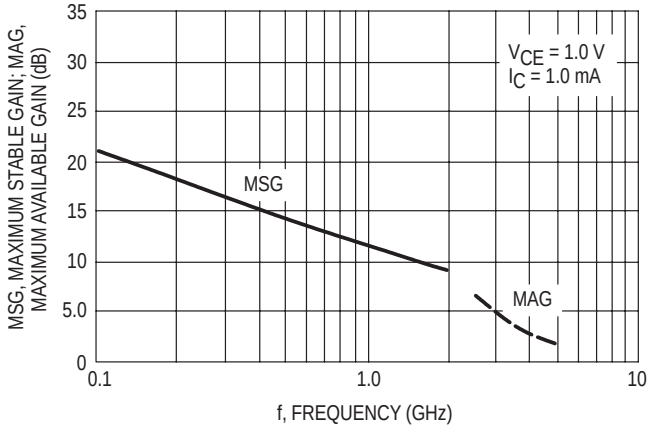


Figure 7. Maximum Stable/Available Gain versus Frequency

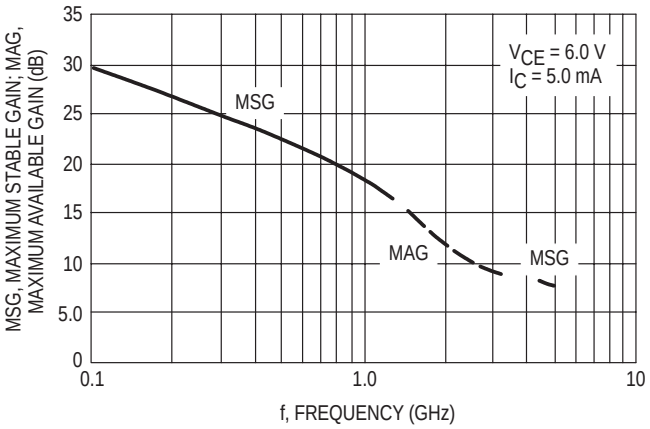


Figure 8. Maximum Unilateral Gain and Forward Insertion Gain versus Frequency

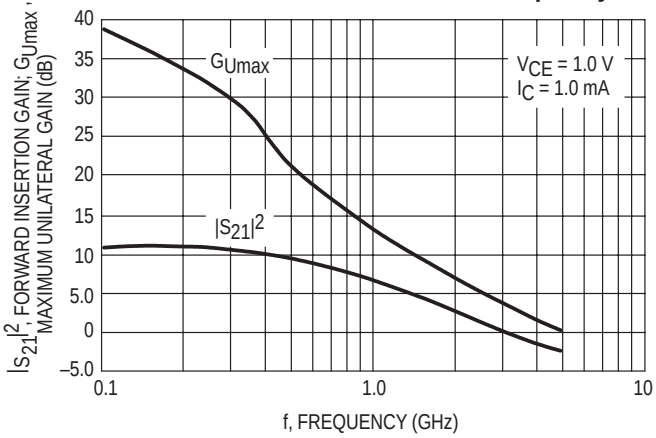


Figure 9. Maximum Unilateral Gain and Forward Insertion Gain versus Frequency

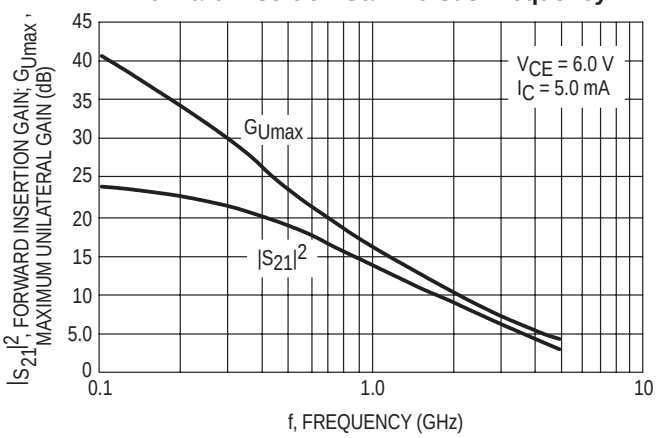


Figure 10. Maximum Unilateral Gain and Forward Insertion Gain versus Collector Current

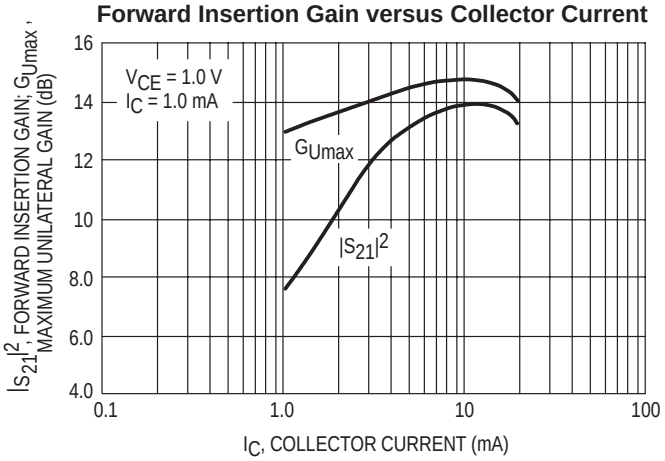
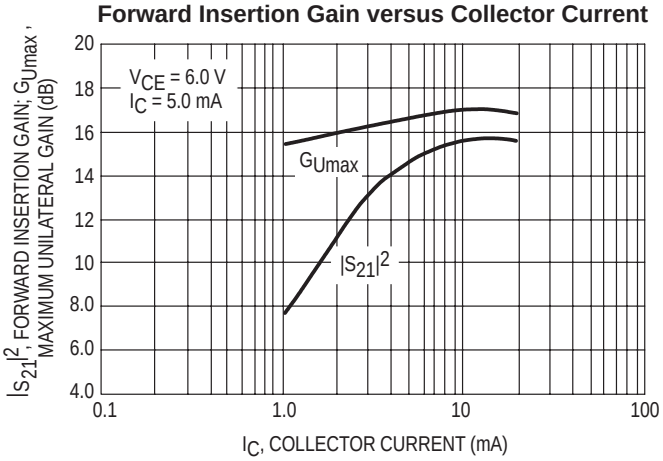


Figure 11. Maximum Unilateral Gain and Forward Insertion Gain versus Collector Current



TYPICAL CHARACTERISTICS

Figure 12. Maximum Stable/Available Gain versus Collector Current

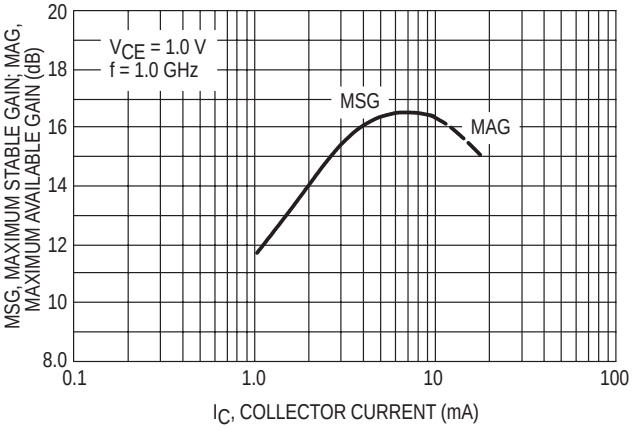


Figure 13. Maximum Stable/Available Gain versus Collector Current

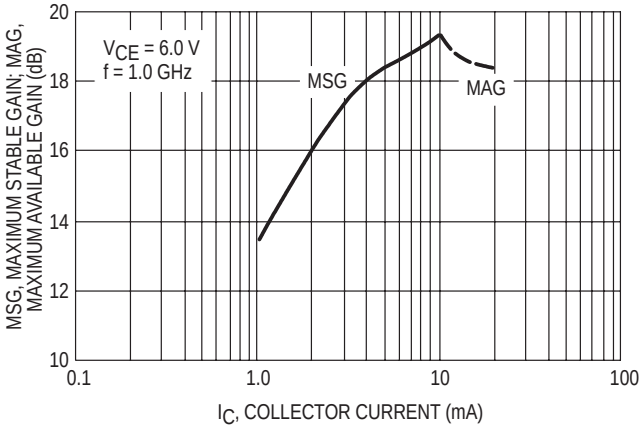


Figure 14. Minimum Noise Figure and Associated Gain versus Frequency

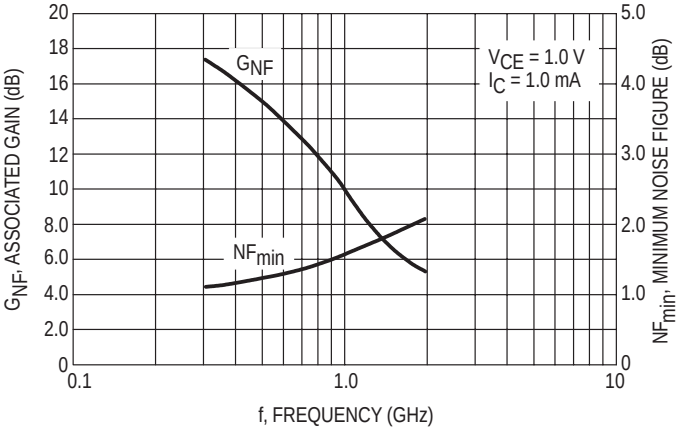


Figure 15. Minimum Noise Figure and Associated Gain versus Frequency

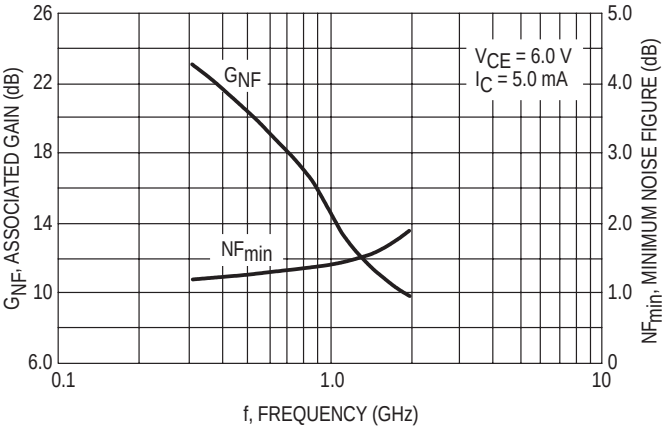


Figure 16. Minimum Noise Figure and Associated Gain versus Collector Current

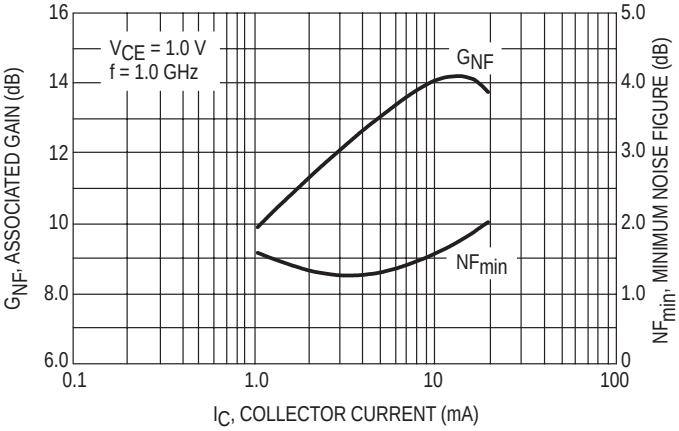
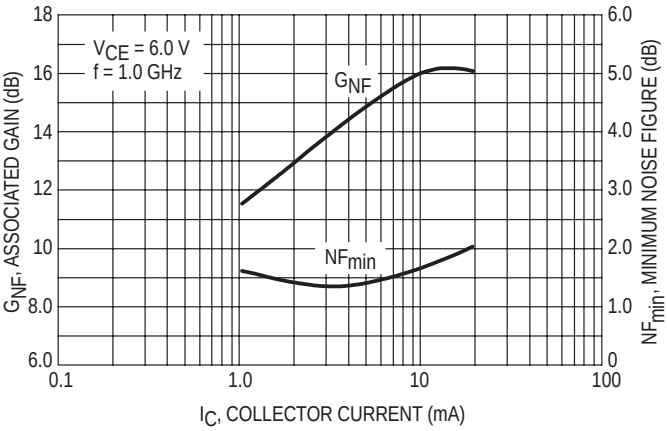


Figure 17. Minimum Noise Figure and Associated Gain versus Collector Current



TYPICAL CHARACTERISTICS

Figure 18. Output Third Order Intercept and Output Power at 1.0 dB Gain Compression versus Collector Current

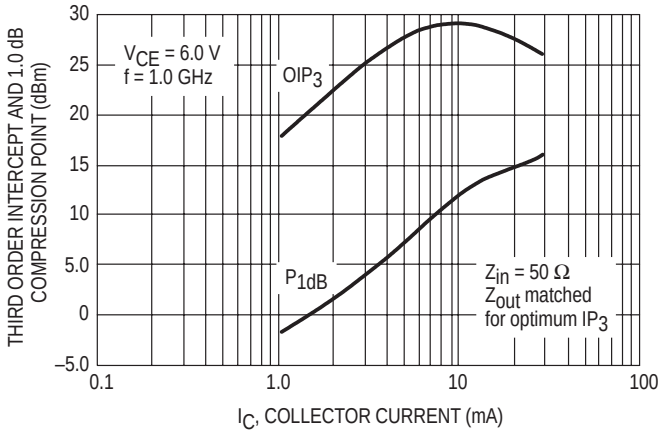


Table 1. Common Emitter S–Parameters

V_{CE} (Vdc)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
1.0	1.0	0.1	0.964	–12	3.62	171	0.028	82	0.989	–6
		0.3	0.926	–36	3.41	152	0.078	69	0.950	–17
		0.5	0.872	–55	2.98	135	0.115	56	0.878	–24
		0.7	0.773	–73	2.67	121	0.140	47	0.811	–31
		0.9	0.701	–89	2.40	110	0.157	40	0.751	–37
		1.0	0.672	–96	2.27	105	0.163	37	0.725	–39
		1.3	0.605	–116	1.95	90	0.172	31	0.660	–44
		1.5	0.579	–127	1.77	83	0.176	27	0.631	–48
		2.0	0.537	–152	1.43	66	0.173	24	0.584	–56
		2.5	0.521	–173	1.22	52	0.168	25	0.555	–65
		3.0	0.520	171	1.06	41	0.168	31	0.542	–74
		3.5	0.529	157	0.94	31	0.179	38	0.543	–84
		4.0	0.543	145	0.84	24	0.205	45	0.541	–95
		4.5	0.552	133	0.79	17	0.248	48	0.525	–106
		5.0	0.571	123	0.72	13	0.296	48	0.527	–117
	3.0	0.1	0.896	–20	9.79	165	0.027	79	0.960	–12
		0.3	0.780	–57	8.17	138	0.068	61	0.826	–29
		0.5	0.653	–80	6.36	120	0.089	51	0.680	–38
		0.7	0.551	–101	5.11	107	0.103	46	0.578	–43
		0.9	0.488	–117	4.23	97	0.113	43	0.510	–47
		1.0	0.468	–125	3.89	93	0.117	43	0.484	–48
		1.3	0.431	–143	3.14	82	0.128	43	0.425	–51
		1.5	0.420	–153	2.78	77	0.137	43	0.401	–54
		2.0	0.410	–174	2.16	63	0.157	44	0.364	–60
		2.5	0.415	169	1.80	52	0.179	45	0.343	–68
		3.0	0.426	157	1.55	43	0.205	46	0.332	–76
		3.5	0.439	146	1.37	34	0.234	46	0.332	–85
		4.0	0.454	137	1.24	26	0.265	45	0.329	–95
		4.5	0.470	128	1.13	19	0.302	44	0.323	–105
		5.0	0.492	119	1.05	12	0.339	41	0.324	–116
	5.0	0.1	0.831	–27	14.66	160	0.026	75	0.929	–16
		0.3	0.668	–72	10.92	129	0.059	57	0.719	–37
		0.5	0.530	–97	7.88	112	0.075	51	0.556	–44
		0.7	0.450	–118	6.06	100	0.087	49	0.458	–48
		0.9	0.409	–133	4.89	92	0.098	49	0.400	–50
		1.0	0.397	–140	4.47	88	0.103	50	0.379	–51
		1.3	0.378	–157	3.55	79	0.119	51	0.331	–53
		1.5	0.376	–166	3.12	74	0.131	51	0.312	–56
		2.0	0.378	177	2.41	62	0.159	52	0.283	–62
		2.5	0.392	162	1.99	52	0.190	51	0.266	–70
		3.0	0.402	151	1.71	43	0.221	50	0.258	–78
		3.5	0.417	141	1.51	35	0.253	48	0.257	–87
		4.0	0.433	133	1.36	27	0.286	46	0.254	–97
		4.5	0.451	125	1.25	20	0.321	43	0.250	–107
		5.0	0.469	117	1.16	13	0.356	40	0.251	–118

Table 1. Common Emitter S–Parameters (continued)

V_{CE} (Vdc)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
3.0	3.0	0.1	0.909	–17	9.75	166	0.019	80	0.972	–9
		0.3	0.805	–48	8.43	142	0.051	65	0.874	–22
		0.5	0.680	–70	6.76	124	0.070	55	0.756	–29
		0.7	0.567	–89	5.55	111	0.082	51	0.669	–33
		0.9	0.490	–104	4.65	102	0.091	48	0.608	–36
		1.0	0.464	–111	4.30	98	0.095	48	0.587	–37
		1.3	0.408	–130	3.49	86	0.105	48	0.534	–39
		1.5	0.391	–141	3.10	81	0.113	48	0.513	–41
		2.0	0.366	–163	2.42	68	0.131	50	0.479	–46
		2.5	0.365	178	2.01	56	0.151	52	0.459	–52
		3.0	0.371	164	1.73	47	0.175	53	0.448	–59
		3.5	0.385	152	1.52	38	0.202	54	0.446	–67
		4.0	0.404	142	1.37	30	0.232	54	0.443	–75
		4.5	0.420	132	1.26	23	0.268	53	0.436	–83
		5.0	0.443	124	1.16	16	0.307	51	0.434	–92
	5.0	0.1	0.853	–22	14.73	162	0.019	78	0.950	–12
		0.3	0.697	–60	11.59	134	0.045	62	0.791	–27
		0.5	0.547	–82	8.62	116	0.060	56	0.652	–32
		0.7	0.447	–102	6.75	104	0.070	54	0.565	–35
		0.9	0.386	–117	5.50	96	0.080	54	0.513	–37
		1.0	0.368	–124	5.03	92	0.085	54	0.494	–37
		1.3	0.332	–142	4.02	83	0.099	55	0.453	–39
		1.5	0.323	–152	3.54	78	0.109	56	0.436	–40
		2.0	0.315	–173	2.74	66	0.134	57	0.408	–45
		2.5	0.323	170	2.26	56	0.161	57	0.392	–51
		3.0	0.334	158	1.93	47	0.189	56	0.384	–58
		3.5	0.348	147	1.70	38	0.218	55	0.380	–65
		4.0	0.369	138	1.53	31	0.249	53	0.376	–73
		4.5	0.387	130	1.40	24	0.283	51	0.371	–81
		5.0	0.410	122	1.30	17	0.319	49	0.367	–89
	10.0	0.1	0.730	–33	23.83	154	0.017	74	0.896	–17
		0.3	0.518	–80	15.52	122	0.037	61	0.647	–33
		0.5	0.382	–103	10.52	106	0.049	60	0.517	–34
		0.7	0.319	–122	7.89	96	0.060	61	0.450	–35
		0.9	0.287	–137	6.28	89	0.072	62	0.414	–35
		1.0	0.279	–144	5.71	86	0.078	63	0.402	–35
		1.3	0.268	–159	4.49	79	0.096	64	0.374	–36
		1.5	0.269	–168	3.94	74	0.108	64	0.362	–38
		2.0	0.278	176	3.02	64	0.139	63	0.343	–42
		2.5	0.294	161	2.48	55	0.171	61	0.331	–49
		3.0	0.311	151	2.12	47	0.202	59	0.323	–56
		3.5	0.329	142	1.86	39	0.233	56	0.319	–63
		4.0	0.347	134	1.68	31	0.265	53	0.314	–71
		4.5	0.367	127	1.53	24	0.298	51	0.309	–79
		5.0	0.390	120	1.42	18	0.332	47	0.305	–87
6.0	5.0	0.1	0.870	–20	14.57	163	0.016	79	0.958	–10
		0.3	0.719	–55	11.68	136	0.040	64	0.822	–23
		0.5	0.566	–76	8.81	118	0.053	58	0.697	–28
		0.7	0.457	–94	6.96	106	0.063	56	0.619	–30
		0.9	0.387	–109	5.69	98	0.072	56	0.571	–31
		1.0	0.365	–115	5.22	94	0.076	56	0.554	–32
		1.3	0.320	–133	4.18	84	0.089	57	0.516	–33
		1.5	0.306	–143	3.69	79	0.098	58	0.501	–35
		2.0	0.291	–164	2.86	67	0.121	59	0.476	–39
		2.5	0.293	178	2.35	57	0.146	60	0.462	–45
		3.0	0.304	165	2.02	48	0.171	59	0.454	–51
		3.5	0.319	154	1.78	40	0.198	59	0.452	–58
		4.0	0.339	145	1.60	32	0.228	58	0.449	–65
		4.5	0.359	136	1.46	25	0.261	56	0.445	–72
		5.0	0.384	128	1.35	18	0.297	54	0.442	–80

Table 1. Common Emitter S–Parameters (continued)

V_{CE} (Vdc)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
6.0	15.0	0.1	0.698	–37	28.78	150	0.014	74	0.877	–17
		0.3	0.465	–84	17.38	118	0.030	63	0.627	–29
		0.5	0.331	–105	11.47	103	0.041	64	0.525	–28
		0.7	0.274	–123	8.50	95	0.052	66	0.478	–27
		0.9	0.248	–137	6.74	88	0.063	67	0.453	–27
		1.0	0.241	–143	6.12	85	0.069	67	0.443	–27
		1.3	0.232	–158	4.80	78	0.086	68	0.425	–28
		1.5	0.235	–165	4.20	74	0.098	68	0.415	–30
		2.0	0.247	179	3.22	64	0.127	66	0.400	–34
		2.5	0.264	165	2.64	55	0.156	64	0.390	–41
		3.0	0.279	156	2.25	48	0.185	62	0.385	–47
		3.5	0.297	148	1.98	40	0.214	60	0.381	–54
		4.0	0.317	141	1.78	33	0.245	57	0.376	–61
		4.5	0.338	134	1.62	26	0.276	55	0.371	–69
		5.0	0.361	127	1.50	19	0.310	52	0.366	–76
	30.0	0.1	0.550	–54	35.24	141	0.012	70	0.801	–20
		0.3	0.351	–107	17.63	109	0.024	66	0.562	–25
		0.5	0.267	–130	11.12	97	0.035	70	0.506	–21
		0.7	0.246	–147	8.12	90	0.047	72	0.481	–21
		0.9	0.239	–158	6.39	84	0.058	72	0.467	–22
		1.0	0.239	–163	5.79	82	0.064	73	0.462	–22
		1.3	0.245	–174	4.52	75	0.082	72	0.450	–24
		1.5	0.253	–180	3.96	71	0.094	72	0.444	–26
		2.0	0.272	168	3.04	62	0.123	70	0.433	–32
		2.5	0.296	156	2.48	53	0.152	68	0.425	–39
		3.0	0.315	148	2.12	45	0.182	66	0.421	–46
		3.5	0.339	140	1.86	38	0.213	64	0.417	–54
		4.0	0.358	134	1.67	31	0.245	62	0.414	–61
		4.5	0.381	127	1.52	24	0.279	59	0.410	–69
		5.0	0.406	120	1.40	18	0.317	56	0.406	–77

Table 2. Common Emitter Noise Parameters

V_{CE} (Vdc)	I_C (mA)	f (GHz)	NF_{min} (dB)	Γ_o		R_N (Ω)	r_n	G_{NF} (dB)
				Magnitude	Angle			
1.0	1.0	0.3	1.14	0.67	16	29	0.58	17.3
		0.5	1.24	0.63	28	28	0.56	14.8
		0.7	1.35	0.60	40	27	0.53	12.5
		0.9	1.50	0.57	52	25	0.51	10.6
		1.0	1.57	0.56	58	24	0.49	9.7
		1.5	1.86	0.51	89	19	0.39	6.5
		2.0	2.08	0.50	120	13	0.26	5.2
3.0	3.0	0.3	1.04	0.57	12	21	0.42	21.5
		0.5	1.12	0.53	21	20	0.41	18.8
		0.7	1.21	0.50	31	19	0.39	16.4
		0.9	1.30	0.47	42	19	0.38	14.3
		1.0	1.34	0.45	47	18	0.37	13.4
		1.5	1.57	0.41	77	15	0.31	9.9
		2.0	1.80	0.40	110	12	0.24	8.4
6.0	5.0	0.3	1.22	0.54	11	22	0.44	23.1
		0.5	1.27	0.51	19	21	0.42	20.3
		0.7	1.32	0.48	28	20	0.41	17.8
		0.9	1.38	0.45	38	20	0.39	15.7
		1.0	1.41	0.44	43	19	0.38	14.7
		1.5	1.61	0.40	71	17	0.33	11.2
		2.0	1.86	0.38	103	13	0.26	9.5

Table 3. Spice Parameters (MRF949 Die Gummel–Poon Parameters)

Name	Value	Name	Value	Name	Value
IS	4.598E–16	IRB	8.00E–05	TF	1.00E–11
BF	175	RBM	3.0	XTF	50
NF	0.9904	RE	0.45	VTF	1.2
VAF	22	RC	6.0	ITF	0.32
IKF	0.08	XTB	0	PTF	32
ISE	1.548E–14	EG	1.11	TR	1.00E–09
NE	1.703	XTI	3.0	FC	0.9
BR	76.1	CJE	8.70E–13		
NR	0.9952	VJE	0.905		
VAR	2.1	MJE	0.389		
IKR	0.02059	CJC	3.60E–13		
ISC	3.395E–16	VJC	0.4907		
NC	1.13	MJC	0.2198		
RB	8.0	XCJC	0.43		

Figure 19. MRF949 SC–90/SC–75 Package Equivalent Circuit

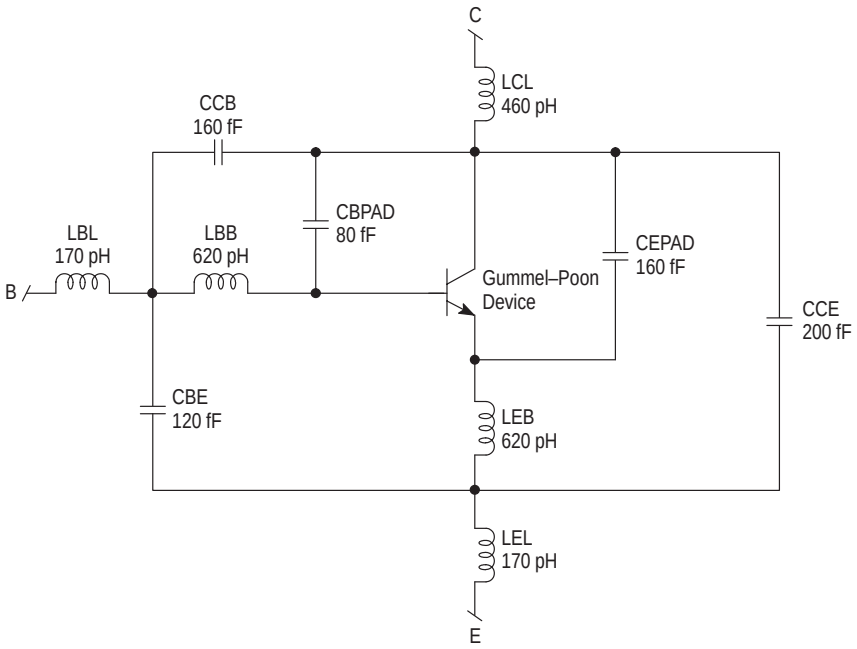
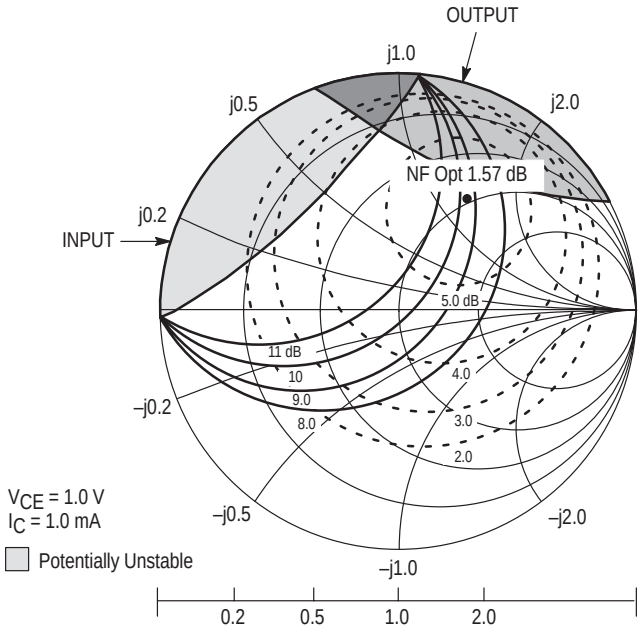
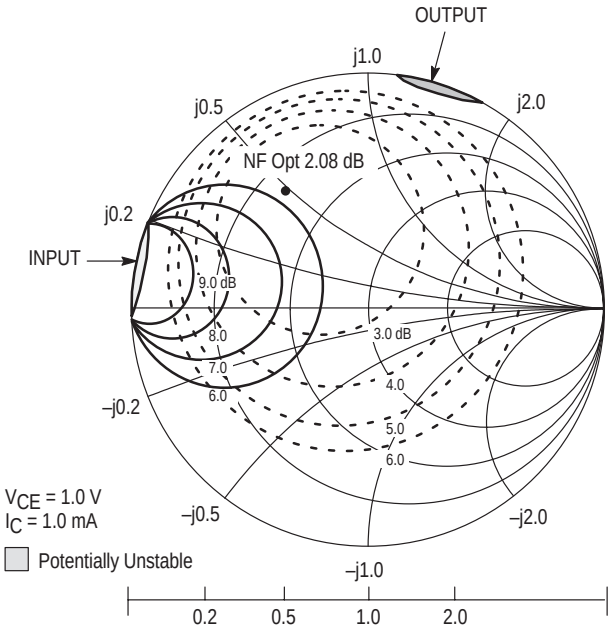


Figure 20. Constant Gain and Noise Figure Contours (f = 1.0 GHz)



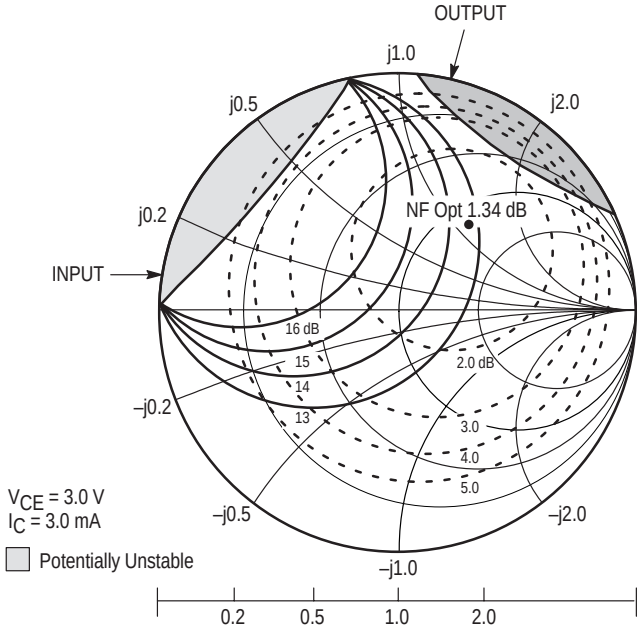
f (GHz)	NF Opt (dB)	Γ_o	Rn	K
1.0	1.57	0.56 ∠ 57.7°	24.2	0.48

Figure 21. Constant Gain and Noise Figure Contours (f = 2.0 GHz)



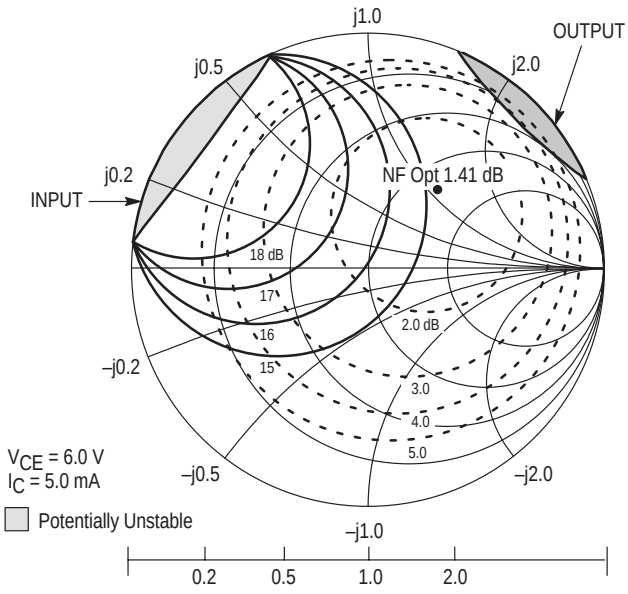
f (GHz)	NF Opt (dB)	Γ_o	Rn	K
2.0	2.08	0.50 ∠ 119.8°	13	0.93

Figure 22. Constant Gain and Noise Figure Contours (f = 1.0 GHz)



f (GHz)	NF Opt (dB)	Γ_o	Rn	K
1.0	1.34	0.45 ∠ 47.3°	18.2	0.73

Figure 23. Constant Gain and Noise Figure Contours (f = 1.0 GHz)



f (GHz)	NF Opt (dB)	Γ_o	Rn	K
1.0	1.41	0.44 ∠ 42.9°	19	0.86

MOTOROLA

MRF959T1

NPN Silicon Low Noise Transistors

Motorola's MRF959 is a high performance NPN transistor designed for use in high gain, low noise small–signal amplifiers. The MRF959 is well suited for low voltage applications. This device features a 9.0 GHz DC current gain–bandwidth product with excellent linearity.

- Low Noise Figure, NF_{min} = 1.3 dB (Typ) @ 1.0 GHz, 6.0 V, 5.0 mA
- High Current Gain–Bandwidth Product, f_τ = 9.0 GHz, 6.0 V, 30 mA
- Maximum Stable Gain, 17 dB @ 1.0 GHz, 6.0 V, 10 mA
- Output Third Order Intercept, Output IP_3 = 30 dBm @ 1.0 GHz, 6.0 V, 30 mA
- Fully Ion–Implanted with Gold Metallization and Nitride Passivation

LOW NOISE TRANSISTORS

f_τ = 9.0 GHz

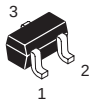
NF_{min} = 1.3 dB

I_{CMAX} = 100 mA

V_{CEO} = 10 V

SEMICONDUCTOR TECHNICAL DATA

Pin 1. Base
2. Emitter
3. Collector



PLASTIC PACKAGE
CASE 463
(SC–90/SC–75, Tape & Reel Only)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	10	Vdc
Collector–Base Voltage	V_{CBO}	20	Vdc
Emitter–Base Voltage	V_{EBO}	1.5	Vdc
Power Dissipation @ T_C = 75°C Derate linearly above T_C = 75°C at	$P_{D(max)}$	0.15 2.0	W mW/°C
Collector Current – Continuous [Note 3]	I_C	100	mA
Storage Temperature	T_{stg}	–55 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$	150	°C

NOTES: 1. Meets Human Body Model (HBM) ≤300 V and Machine Model (MM) ≤75 V.
2. ESD data available upon request.
3. For MTBF >10 years.

THERMAL CHARACTERISTIC

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	500	°C/W

NOTE: To calculate the junction temperature use $T_J = (P_D \times R_{\theta JC}) + T_C$. The case temperature measured on collector lead adjacent to the package body.

ORDERING INFORMATION

Device	Marking	Package
MRF959T1	V1	SC–90/SC–75 Tape & Reel*

*3,000 Units per 8 mm, 7 inch reel.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS [Note 1]					
Collector–Emitter Breakdown Voltage (I_C = 0.1 mA, I_B = 0)	$V_{(BR)CEO}$	10	13	–	Vdc
Collector–Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)	$V_{(BR)CBO}$	20	25	–	Vdc
Emitter Cutoff Current (V_{EB} = 1.0 V, I_C = 0)	I_{EBO}	–	–	0.1	μA
Collector Cutoff Current (V_{CB} = 10 V, I_E = 0)	I_{CBO}	–	–	0.1	μA
ON CHARACTERISTICS [Note 1]					
DC Current Gain (V_{CE} = 6.0 V, I_C = 5.0 mA)	h_{FE}	75	–	150	–
DYNAMIC CHARACTERISTICS					
Collector–Base Capacitance	C_{cb}				pF
(V_{CB} = 1.0 V, I_E = 0, f = 1.0 MHz)		–	0.63	–	
(V_{CB} = 5.0 V, I_E = 0, f = 1.0 MHz)		–	0.44	–	
Current Gain – Bandwidth Product (V_{CE} = 6.0 V, I_C = 30 mA, f = 1.0 GHz)	f_τ	–	9.0	–	GHz
PERFORMANCE CHARACTERISTICS					
Insertion Gain	$\|S_{21}\|^2$				dB
(V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz)		–	4.0	–	
(V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)		–	14	–	
Maximum Unilateral Gain [Note 2]	G_{Umax}				dB
(V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz)		–	9.0	–	
(V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)		–	15	–	
Maximum Stable Gain and/or Maximum Available Gain [Note 3]					dB
(V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz)	MSG	–	10	–	
(V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)	MAG	–	17	–	
Noise Figure – Minimum	NF_{min}				dB
(V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz)		–	1.6	–	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)		–	1.3	–	
Noise Resistance	R_N				Ω
(V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz)		–	14	–	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)		–	9.0	–	
Associated Gain at Minimum NF	G_{NF}				dB
(V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz)		–	8.0	–	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)		–	13	–	
Output Power at 1.0 dB Gain Compression [Note 4] (V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)	P_{1dB}	–	12	–	dBm
Output Third Order Intercept [Note 4] (V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)	OIP_3	–	26	–	dBm

NOTES: 1. Pulse width ≤300 μs, duty cycle ≤2% pulsed.

2. Maximum unilateral gain is:

$$G_{Umax} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$$

3. Maximum Available Gain and Maximum Stable Gain are defined by the K factor as follows:

$$MAG = \left|\frac{S_{21}}{S_{12}}\left(K \pm \sqrt{K^2-1}\right)\right|, \text{ if } K > 1, \quad MSG = \left|\frac{S_{21}}{S_{12}}\right|, \text{ if } K < 1$$

4. Z_{in} = 50 Ω and Z_{out} matched for small signal maximum gain.

TYPICAL CHARACTERISTICS

Figure 1. Capacitance versus Voltage

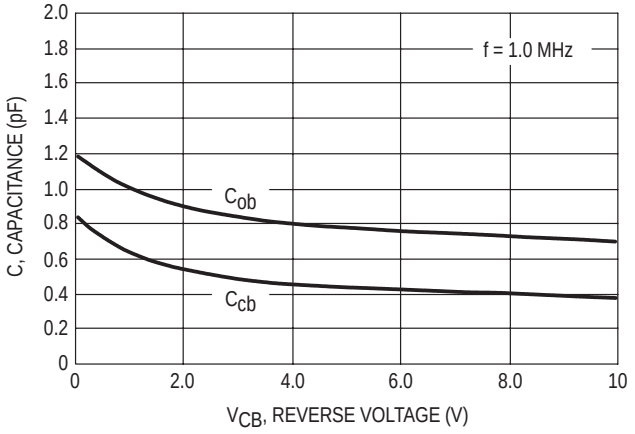


Figure 2. Input Capacitance versus Voltage

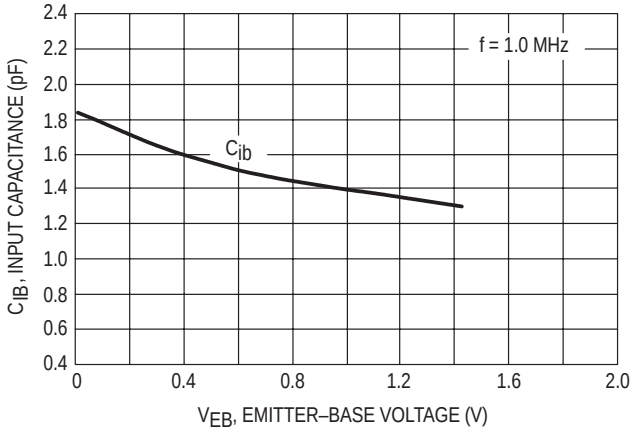


Figure 3. DC Current Gain versus Collector Current

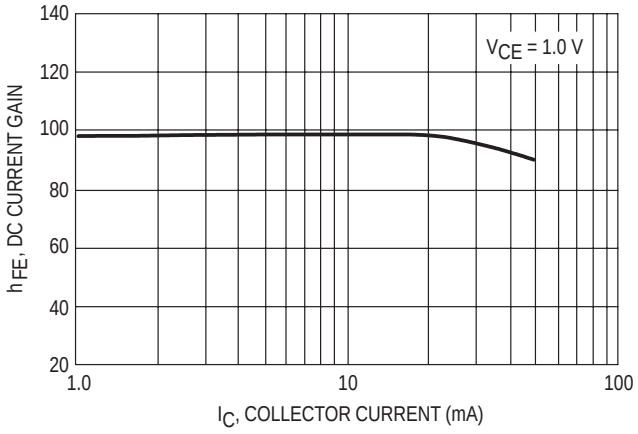


Figure 4. Gain–Bandwidth Product versus Collector Current

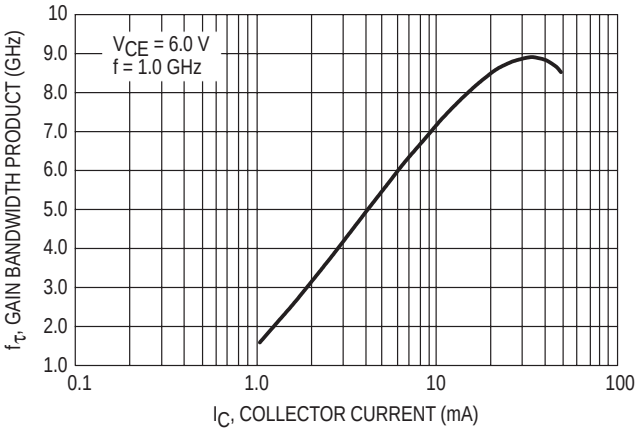
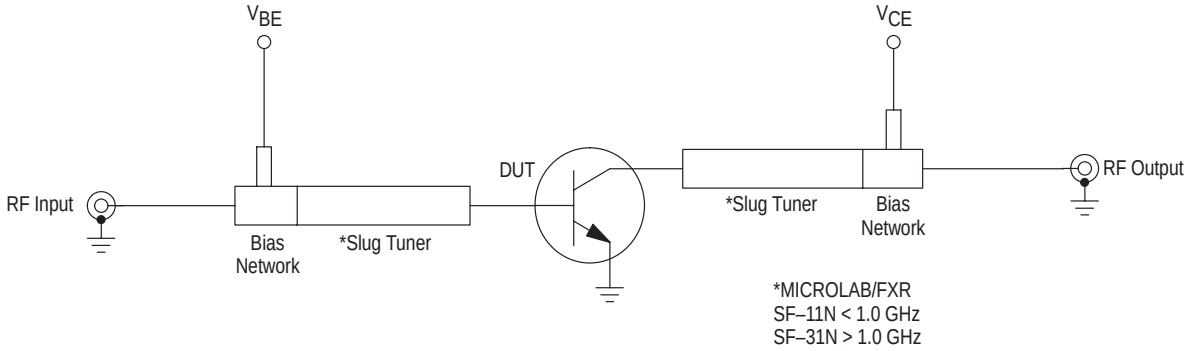


Figure 5. Functional Circuit Schematic



TYPICAL CHARACTERISTICS

Figure 6. Maximum Stable/Available Gain versus Frequency

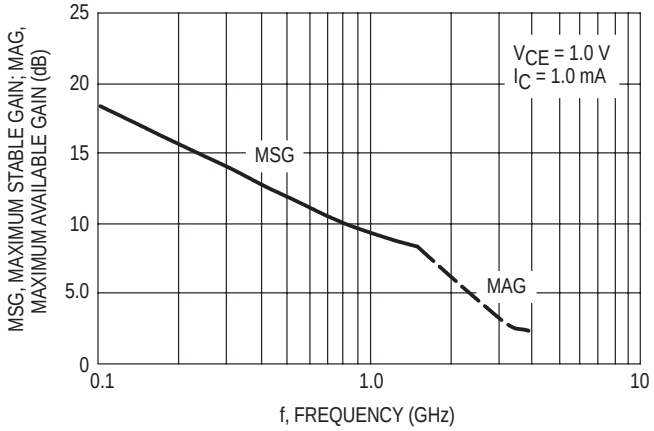


Figure 7. Maximum Stable/Available Gain versus Frequency

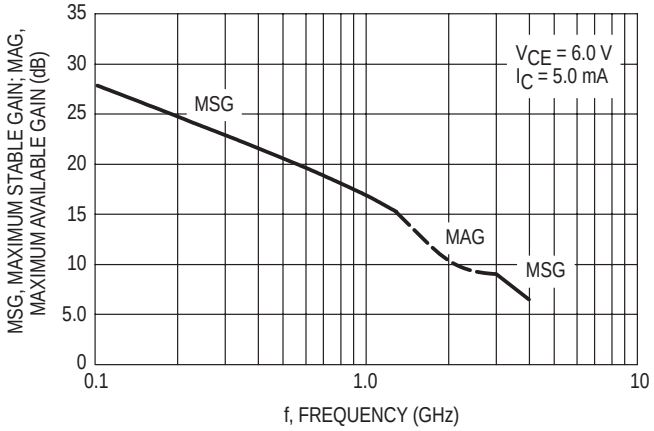


Figure 8. Maximum Unilateral Gain and Forward Insertion Gain versus Frequency

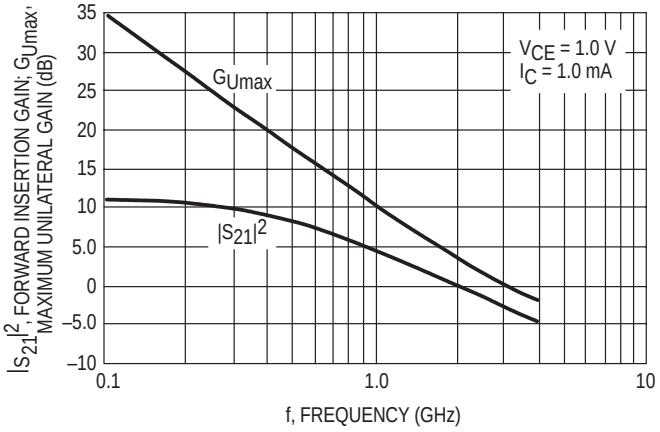


Figure 9. Maximum Unilateral Gain and Forward Insertion Gain versus Frequency

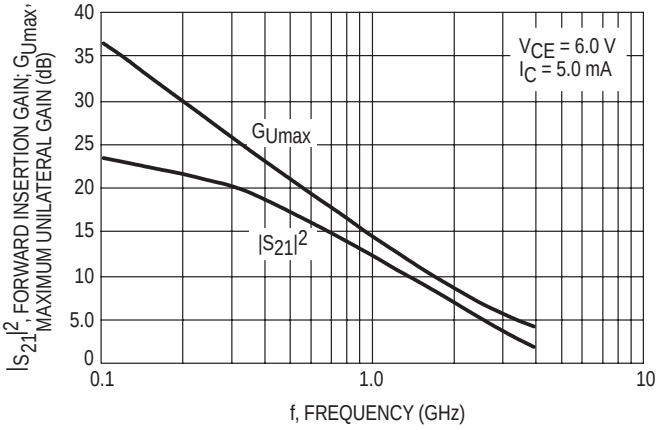


Figure 10. Maximum Unilateral Gain and Forward Insertion Gain versus Collector Current

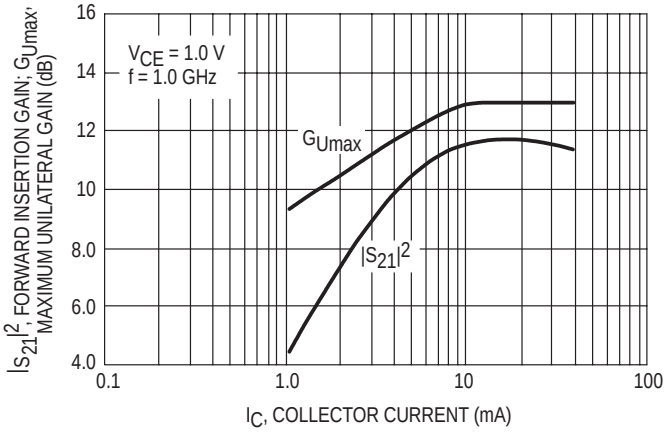
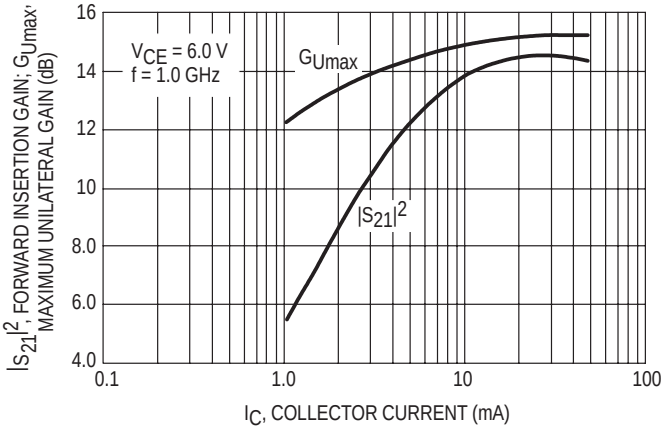


Figure 11. Maximum Unilateral Gain and Forward Insertion Gain versus Collector Current



TYPICAL CHARACTERISTICS

Figure 12. Maximum Stable/Available Gain versus Collector Current

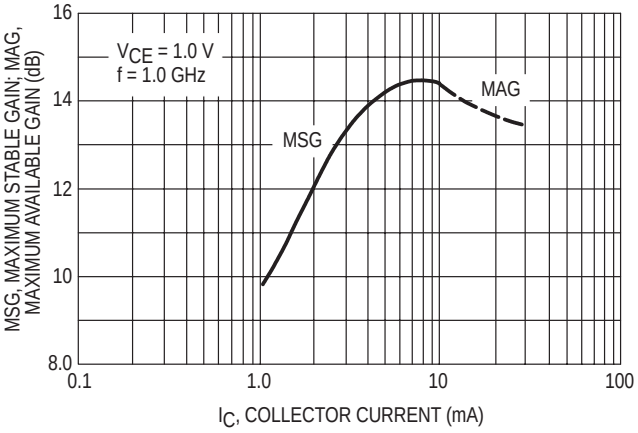


Figure 13. Maximum Stable/Available Gain versus Collector Current

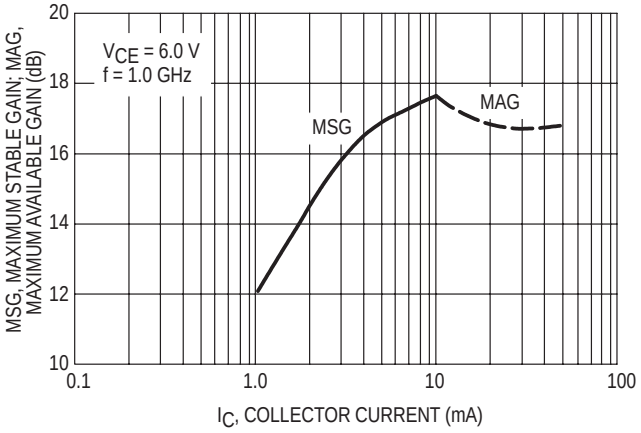


Figure 14. Minimum Noise Figure and Associated Gain versus Frequency

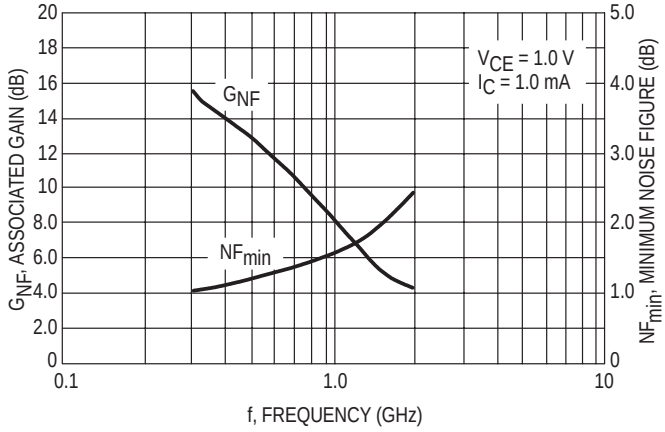


Figure 15. Minimum Noise Figure and Associated Gain versus Frequency

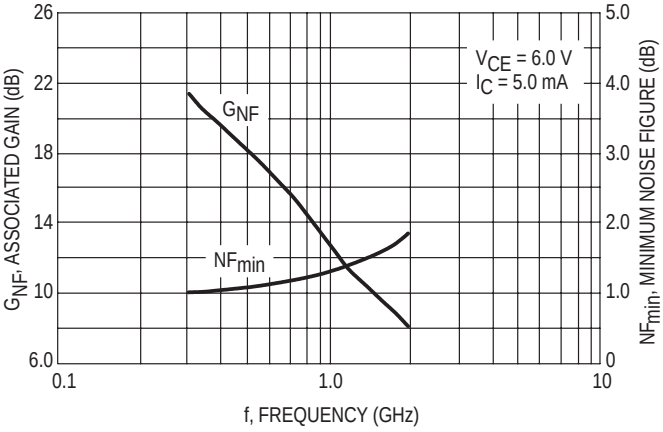


Figure 16. Minimum Noise Figure and Associated Gain versus Collector Current

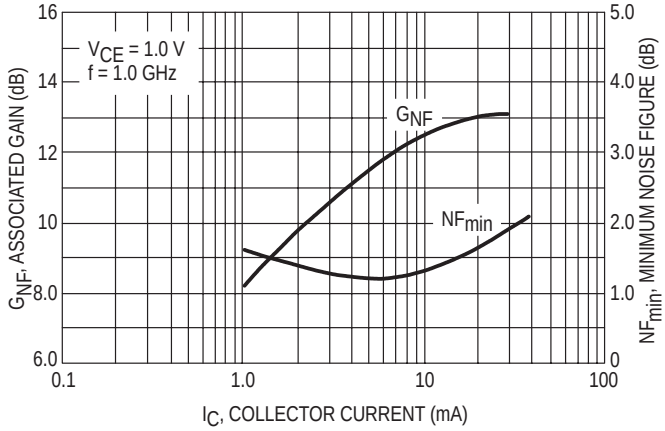
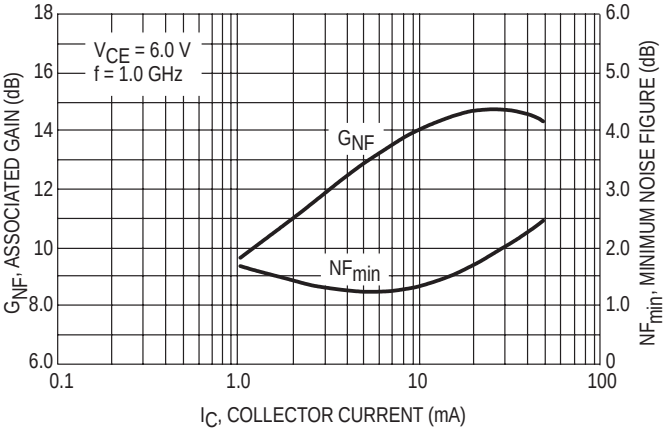


Figure 17. Minimum Noise Figure and Associated Gain versus Collector Current



TYPICAL CHARACTERISTICS

Figure 18. Output Third Order Intercept and Output Power at 1.0 dB Gain Compression versus Collector Current

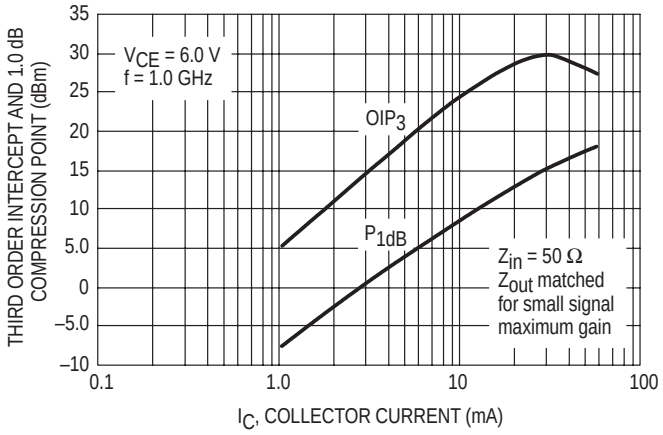


Table 1. Common Emitter S–Parameters

V_{CE} (Vdc)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
1.0	1.0	0.1	0.946	–21	3.53	165	0.047	78	0.980	–9
		0.3	0.888	–60	3.08	139	0.122	56	0.889	–24
		0.5	0.801	–89	2.49	118	0.160	41	0.778	–32
		0.7	0.748	–111	2.06	102	0.177	30	0.698	–39
		0.9	0.711	–128	1.74	90	0.183	24	0.646	–45
		1.0	0.700	–135	1.62	85	0.182	21	0.629	–47
		1.3	0.688	–153	1.33	72	0.174	17	0.591	–54
		1.5	0.682	–163	1.18	64	0.166	15	0.579	–59
		2.0	0.680	179	0.94	49	0.141	21	0.571	–73
		2.5	0.702	163	0.77	37	0.135	39	0.568	–90
		3.0	0.713	152	0.67	30	0.172	56	0.582	–104
		3.5	0.712	138	0.59	26	0.235	62	0.596	–118
		4.0	0.727	127	0.55	25	0.312	60	0.603	–132
		4.5	0.710	117	0.54	24	0.393	55	0.602	–145
		5.0	0.705	108	0.55	23	0.463	48	0.598	–160
	3.0	0.1	0.850	–34	9.36	158	0.044	72	0.934	–18
		0.3	0.736	–86	6.84	126	0.096	49	0.707	–42
		0.5	0.640	–117	4.86	107	0.115	39	0.532	–51
		0.7	0.606	–137	3.74	95	0.123	35	0.436	–56
		0.9	0.584	–151	3.01	86	0.129	35	0.385	–61
		1.0	0.578	–156	2.76	82	0.132	35	0.370	–63
		1.3	0.581	–170	2.20	72	0.140	37	0.331	–68
		1.5	0.580	–178	1.93	66	0.146	39	0.321	–73
		2.0	0.581	168	1.51	53	0.167	45	0.315	–85
		2.5	0.611	156	1.25	42	0.195	50	0.316	–101
		3.0	0.619	147	1.09	33	0.237	53	0.336	–113
		3.5	0.621	135	0.96	26	0.285	53	0.358	–124
		4.0	0.645	127	0.87	20	0.338	51	0.381	–136
		4.5	0.638	118	0.81	16	0.397	47	0.400	–147
		5.0	0.65	110	0.758	12	0.45	43	0.415	–160
	5.0	0.1	0.650	–53	23.10	147	0.025	68	0.844	–27
		0.3	0.535	–114	13.19	114	0.048	53	0.513	–50
		0.5	0.474	–140	8.59	100	0.060	54	0.359	–52
		0.7	0.465	–156	6.34	91	0.072	57	0.290	–53
		0.9	0.459	–166	5.01	84	0.084	59	0.256	–55
		1.0	0.456	–170	4.55	81	0.091	60	0.247	–56
		1.3	0.467	180	3.56	74	0.112	62	0.220	–58
		1.5	0.469	174	3.11	69	0.126	62	0.212	–61
		2.0	0.473	163	2.40	59	0.162	62	0.203	–71
		2.5	0.509	152	1.96	49	0.198	61	0.189	–86
		3.0	0.514	146	1.69	41	0.237	58	0.202	–95
		3.5	0.518	135	1.49	33	0.276	56	0.214	–105
		4.0	0.544	129	1.35	26	0.316	53	0.230	–115
		4.5	0.543	122	1.24	20	0.358	49	0.247	–123
		5.0	0.568	114	1.14	14	0.398	45	0.255	–136
3.0	3.0	0.1	0.866	–28	9.71	161	0.031	75	0.954	–13
		0.3	0.760	–76	7.57	131	0.072	54	0.782	–31
		0.5	0.653	–106	5.59	113	0.089	43	0.630	–37
		0.7	0.607	–127	4.37	100	0.097	39	0.541	–40
		0.9	0.578	–142	3.55	91	0.102	38	0.491	–43
		1.0	0.569	–148	3.26	87	0.105	38	0.475	–45
		1.3	0.566	–163	2.60	77	0.111	41	0.437	–48
		1.5	0.562	–172	2.28	71	0.116	43	0.425	–51

Table 1. Common Emitter S–Parameters (continued)

V_{CE} (Vdc)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
3.0	3.0	2.0	0.561	173	1.77	58	0.131	50	0.411	–61
		2.5	0.588	160	1.45	47	0.155	56	0.396	–73
		3.0	0.598	151	1.26	38	0.190	60	0.406	–84
		3.5	0.603	139	1.10	30	0.233	61	0.419	–95
		4.0	0.629	130	0.98	23	0.282	60	0.433	–106
		4.5	0.626	122	0.90	18	0.338	57	0.447	–117
		5.0	0.644	113	0.83	13	0.394	53	0.452	–130
	5.0	0.1	0.792	–36	14.53	156	0.029	72	0.921	–18
		0.3	0.663	–90	10.09	124	0.062	52	0.676	–39
		0.5	0.566	–120	7.01	107	0.074	46	0.510	–43
		0.7	0.535	–139	5.32	96	0.083	45	0.425	–46
		0.9	0.517	–153	4.25	88	0.091	47	0.380	–48
		1.0	0.510	–158	3.89	84	0.096	48	0.367	–49
		1.3	0.515	–171	3.06	75	0.109	51	0.333	–52
		1.5	0.515	–178	2.69	70	0.118	53	0.322	–55
		2.0	0.516	169	2.08	58	0.146	56	0.310	–64
		2.5	0.548	156	1.70	48	0.176	58	0.294	–77
		3.0	0.556	149	1.47	39	0.213	59	0.306	–87
		3.5	0.559	137	1.29	31	0.253	58	0.319	–97
		4.0	0.587	130	1.16	24	0.296	56	0.334	–108
		4.5	0.586	122	1.06	18	0.345	53	0.351	–117
		5.0	0.608	114	0.98	12	0.393	49	0.358	–130
	10.0	0.1	0.823	–24	14.80	161	0.018	77	0.952	–13
		0.3	0.666	–63	11.47	131	0.045	60	0.790	–29
		0.5	0.514	–87	8.47	113	0.058	53	0.653	–34
		0.7	0.425	–108	6.60	100	0.069	51	0.577	–38
		0.9	0.366	–124	5.37	91	0.078	50	0.532	–40
		1.0	0.347	–132	4.91	86	0.083	50	0.512	–42
		1.3	0.309	–152	3.91	75	0.098	50	0.479	–44
		1.5	0.295	–163	3.44	70	0.108	49	0.465	–48
		2.0	0.284	172	2.65	55	0.134	48	0.449	–55
		2.5	0.277	151	2.18	43	0.161	45	0.442	–63
		3.0	0.291	134	1.87	31	0.190	42	0.440	–71
		3.5	0.298	118	1.63	20	0.221	37	0.441	–82
		4.0	0.299	108	1.46	11	0.245	32	0.431	–92
		4.5	0.343	96	1.35	1	0.278	29	0.430	–102
		5.0	0.373	82	1.24	–8	0.313	23	0.436	–113
6.0	5.0	0.1	0.809	–32	14.52	158	0.024	74	0.934	–15
		0.3	0.665	–83	10.44	126	0.053	55	0.721	–32
		0.5	0.550	–112	7.37	109	0.065	49	0.572	–35
		0.7	0.507	–132	5.63	98	0.074	49	0.493	–37
		0.9	0.482	–146	4.52	90	0.082	50	0.452	–38
		1.0	0.472	–152	4.12	86	0.086	51	0.440	–39
		1.3	0.471	–166	3.27	77	0.098	55	0.409	–41
		1.5	0.469	–174	2.87	72	0.108	57	0.398	–44
		2.0	0.469	172	2.22	60	0.135	61	0.385	–52
		2.5	0.502	160	1.82	50	0.166	63	0.364	–62
		3.0	0.512	151	1.57	41	0.203	64	0.372	–72
		3.5	0.514	140	1.38	33	0.244	63	0.381	–81
		4.0	0.548	132	1.24	25	0.289	61	0.391	–92
		4.5	0.545	124	1.13	19	0.341	58	0.404	–102
		5.0	0.571	117	1.04	13	0.394	54	0.403	–114

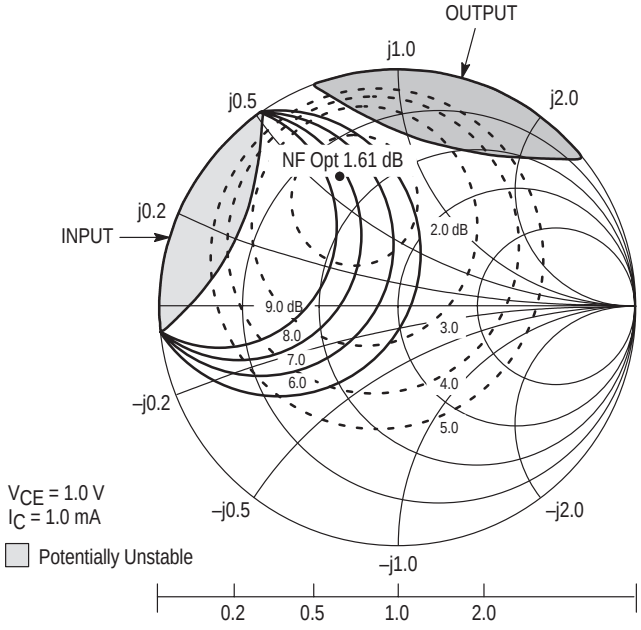
Table 1. Common Emitter S–Parameters (continued)

V_{CE} (Vdc)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
6.0	15.0	0.1	0.598	–56	28.57	144	0.020	68	0.814	–26
		0.3	0.458	–115	15.28	111	0.038	59	0.491	–43
		0.5	0.396	–141	9.78	98	0.050	62	0.367	–40
		0.7	0.387	–156	7.18	90	0.063	64	0.315	–39
		0.9	0.381	–166	5.67	84	0.077	66	0.290	–39
		1.0	0.377	–170	5.12	81	0.084	67	0.284	–40
		1.3	0.389	–179	4.01	74	0.106	68	0.264	–41
		1.5	0.394	174	3.51	70	0.120	68	0.257	–44
		2.0	0.397	164	2.71	60	0.157	66	0.247	–52
		2.5	0.436	154	2.21	51	0.194	65	0.224	–64
		3.0	0.443	148	1.91	43	0.233	62	0.233	–73
		3.5	0.448	138	1.68	35	0.272	59	0.240	–82
		4.0	0.479	131	1.52	28	0.311	56	0.250	–92
		4.5	0.474	125	1.39	21	0.353	53	0.265	–101
		5.0	0.506	118	1.29	15	0.395	49	0.263	–113
	30.0	0.1	0.476	–76	36.18	135	0.017	66	0.706	–33
		0.3	0.396	–134	16.55	104	0.032	65	0.387	–44
		0.5	0.364	–156	10.31	94	0.046	69	0.296	–38
		0.7	0.365	–167	7.50	87	0.061	71	0.261	–36
		0.9	0.364	–175	5.88	81	0.077	72	0.245	–36
		1.0	0.360	–178	5.23	79	0.085	72	0.242	–37
		1.3	0.376	175	4.16	73	0.108	71	0.228	–39
		1.5	0.382	170	3.63	69	0.124	71	0.222	–41
		2.0	0.387	161	2.79	59	0.163	68	0.215	–50
		2.5	0.428	152	2.28	51	0.200	65	0.193	–63
		3.0	0.436	146	1.96	43	0.240	62	0.202	–72
		3.5	0.440	136	1.73	35	0.279	59	0.210	–82
		4.0	0.473	130	1.56	28	0.317	55	0.219	–92
		4.5	0.470	124	1.43	21	0.359	52	0.234	–101
		5.0	0.499	118	1.32	15	0.400	48	0.233	–113

Table 2. Common Emitter Noise Parameters

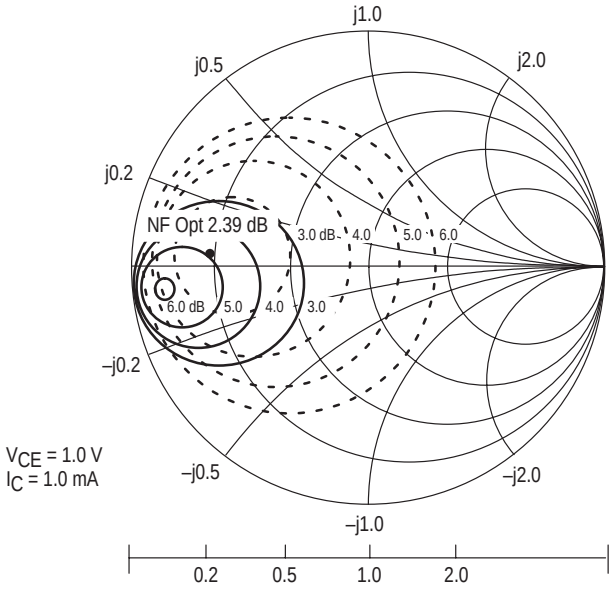
V_{CE} (Vdc)	I_C (mA)	f (GHz)	NF_{min} (dB)	Γ_o		R_N (Ω)	r_n	G_{NF} (dB)
				Magnitude	Angle			
1.0	1.0	0.3	0.97	0.58	38	18	0.35	15.6
		0.5	1.16	0.56	62	18	0.36	13.1
		0.7	1.35	0.54	83	17	0.34	10.9
		0.9	1.52	0.53	102	15	0.30	9.0
		1.0	1.61	0.53	111	14	0.28	8.2
		1.5	2.02	0.56	149	8	0.16	5.2
		2.0	2.39	0.64	175	4	0.08	4.5
3.0	3.0	0.3	0.93	0.37	37	10	0.20	19.8
		0.5	1.03	0.36	59	10	0.20	17.0
		0.7	1.13	0.36	80	10	0.20	14.6
		0.9	1.24	0.37	99	9	0.18	12.4
		1.0	1.29	0.37	108	9	0.18	11.4
		1.5	1.59	0.43	146	7	0.13	8.6
		2.0	1.92	0.53	172	4	0.08	6.8
6.0	5.0	0.3	0.98	0.29	34	10	0.19	21.4
		0.5	1.05	0.29	56	10	0.19	18.5
		0.7	1.12	0.29	76	9	0.19	16.0
		0.9	1.20	0.30	95	9	0.18	13.9
		1.0	1.28	0.31	104	9	0.17	13.0
		1.5	1.51	0.37	142	7	0.13	10.1
		2.0	1.84	0.47	170	5	0.10	8.2

Figure 19. Constant Gain and Noise Figure Contours (f = 1.0 GHz)



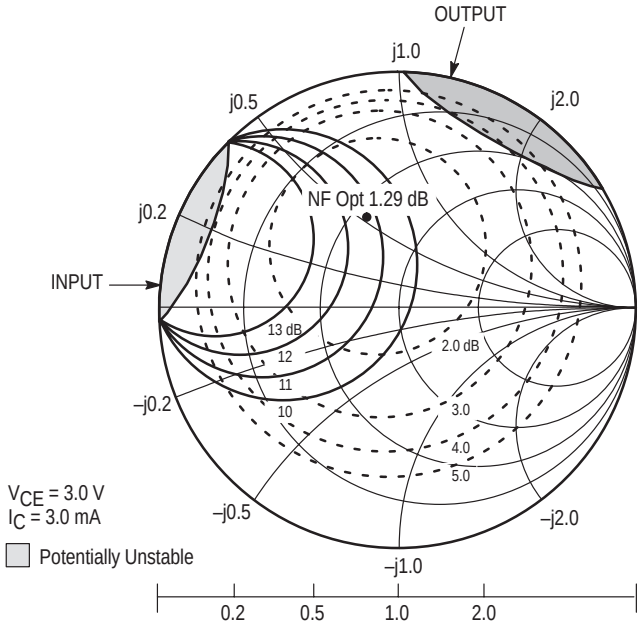
f (GHz)	NF Opt (dB)	Γ_o	Rn	K
1.0	1.61	0.53 ∠ 111.4°	14	0.53

Figure 20. Constant Gain and Noise Figure Contours (f = 2.0 GHz)



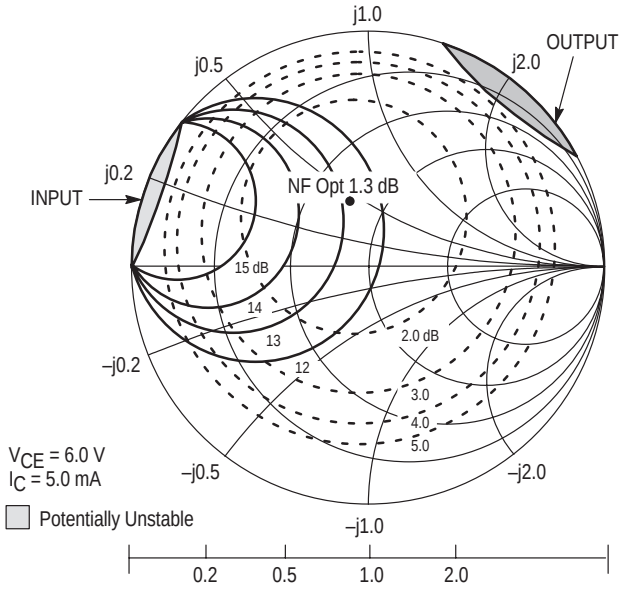
f (GHz)	NF Opt (dB)	Γ_o	Rn	K
2.0	2.39	0.64 ∠ 174.6°	4.0	1.12

Figure 21. Constant Gain and Noise Figure Contours (f = 1.0 GHz)



f (GHz)	NF Opt (dB)	Γ_o	Rn	K
1.0	1.29	0.37 ∠ 108°	9.0	0.73

Figure 22. Constant Gain and Noise Figure Contours (f = 1.0 GHz)



f (GHz)	NF Opt (dB)	Γ_o	Rn	K
1.0	1.3	0.31 ∠ 104°	8.5	0.88

MOTOROLA

MRF1047T1

Advance Information

NPN Silicon Low Noise Transistor

RF NPN SILICON TRANSISTOR

f_τ = 12 GHz

NF_{min} = 1.0 dB

I_{CMAX} = 45 mA

V_{CEO} = 5.0 V

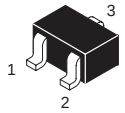
SEMICONDUCTOR TECHNICAL DATA

The MRF1047T1 is fabricated utilizing Motorola's latest 12 GHz f_τ discrete bipolar silicon process. The minimum noise figure is 1.0 dB at V_{CE} = 3.0 V and I_C = 3.0 mA. The noise performance of the MRF1047T1 at low bias makes this device the ideal choice in high gain, low noise applications. This device is well suited for low–voltage, low–current, front–end applications, for use in pagers, cellular and cordless phones, and other portable wireless systems.

The MRF1047T1 has 16 emitter fingers, with self–aligned and enhanced processing, resulting in a high f_τ, low operating current transistor with reduced parasitics. The MRF1047T1 is fully–ion implanted with gold metallization and nitride passivation for maximum device r
eliability, performance and uniformity.

- Low Noise Figure, NF_{min} = 1.0 dB (Typ) @1.0 GHz, 3.0 V and 3.0 mA
- High Current Gain–Bandwidth Product, f_τ = 12 GHz, 3.0 V @ 15 mA
- Maximum Stable Gain, 17 dB @ 1.0 GHz, 3.0 V and 10 mA
- Output Third Order Intercept, OIP_3 = 26 dBm @ 1.0 GHz 3.0 V and 15 mA
- Fully Ion–Implanted with Gold Metallization and Nitride Passivation

Pin 1. Base
2. Emitter
3. Collector



PLASTIC PACKAGE
CASE 419
(SC–70, Tape & Reel Only)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	5.0	Vdc
Collector–Base Voltage	V_{CBO}	12	Vdc
Emitter–Base Voltage	V_{EBO}	2.5	Vdc
Collector Current – Continuous [Note 3]	I_C	45	mAdc
Power Dissipation @ T_C = 75°C Derate Linearly above T_C = 75°C at	$P_{D(max)}$	0.172 2.3	W mW/°C
Storage Temperature Range	T_{stg}	–55 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$	150	°C

NOTES: 1. Meets Human Body Model (HBM) ≤300 V and Machine Model (MM) ≤75 V.
2. ESD data available upon request.
3. For MTBF >10 years.

THERMAL CHARACTERISTIC

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	435	°C/W

NOTE: To calculate the junction temperature use $T_J = (P_D \times R_{\theta JC}) + T_C$. The case temperature measured on collector lead adjacent to the package body.

ORDERING INFORMATION

Device	Marking	Package
MRF1047T1	WB	SC–70 Tape & Reel*

*3,000 Units per 8 mm, 7 inch reel.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS [Note 1]					
Collector–Emitter Breakdown Voltage (I_C = 0.1 mA, I_B = 0)	$V_{(BR)CEO}$	5.0	–	–	Vdc
Collector–Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)	$V_{(BR)CBO}$	12	–	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.1 mA, I_C = 0)	$V_{(BR)CBO}$	2.5	–	–	Vdc
Collector Cutoff Current (V_{CB} =1.0 V, I_E = 0)	I_{CBO}	–	–	0.2	μA
Emitter Cutoff Current (V_{EB} = 1.0 V, I_C = 0)	I_{EBO}	–	–	0.1	μA
ON CHARACTERISTICS [Note 1]					
DC Current Gain (V_{CE} = 3.0 V, I_C = 3.0 mA)	h_{FE}	100	–	200	–
DYNAMIC CHARACTERISTICS					
Collector–Base Capacitance (V_{CB} = 1.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	0.4	–	pF
Current–Gain Bandwidth Product (V_{CE} = 3.0 Vdc, I_C = 15 mA, f = 1.0 GHz)	f_τ	–	12	–	GHz
PERFORMANCE CHARACTERISTICS					
Insertion Gain	$\|S_{21}\|^2$				dB
V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz		–	8.0	–	
V_{CE} = 3.0 V, I_C = 3.0 mA, f = 1.0 GHz		–	13	–	
Maximum Stable Gain and/or Maximum Available Gain [Note 2]	MSG, MAG				dB
V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz		–	11	–	
V_{CE} = 3.0 V, I_C = 3.0 mA, f = 1.0 GHz		–	16	–	
Minimum Noise Figure	NF_{min}				dB
V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz		–	1.2	–	
V_{CE} = 3.0 V, I_C = 3.0 mA, f = 1.0 GHz		–	1.0	–	
Associated Gain at Minimum NF	G_{NF}				dB
V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 GHz		–	10	–	
V_{CE} = 3.0 V, I_C = 3.0 mA, f = 1.0 GHz		–	13	–	
Output Power at 1.0 dB Gain Compression [Note 3] (V_{CE} = 3.0 V, I_C = 3.0 mA, f = 1.0 GHz)	P_{1dB}	–	0.5	–	dBm
Output Third Order Intercept [Note 3] (V_{CE} = 3.0 V, I_C = 3.0 mA, f = 1.0 GHz)	OIP_3	–	22	–	dBm

NOTES: 1. Pulse width ≤300 μs, duty cycle ≤2% pulsed.

2. Maximum Available Gain and Maximum Stable Gain are defined by the K factor as follows:

$$MAG = \left|\frac{S_{21}}{S_{12}}\left(K \pm \sqrt{K^2 - 1}\right)\right|, \text{ if } K > 1, \; MSG = \left|\frac{S_{21}}{S_{12}}\right|, \text{ if } K < 1$$

3. Z_{in} = 50 Ω and Z_{out} matched for optimum IP3.

Figure 1. Capacitance versus Voltage

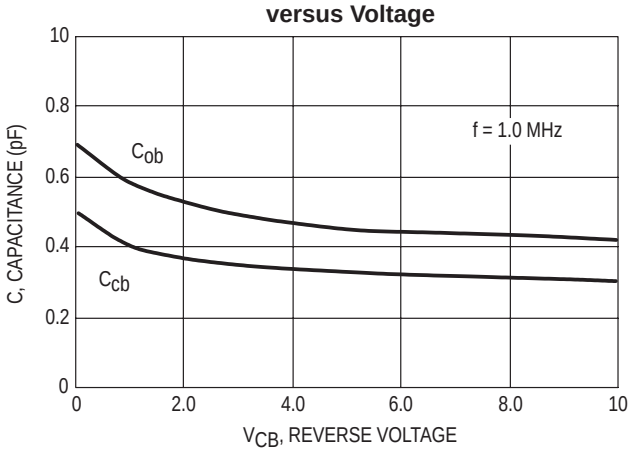


Figure 2. Input Capacitance versus Voltage

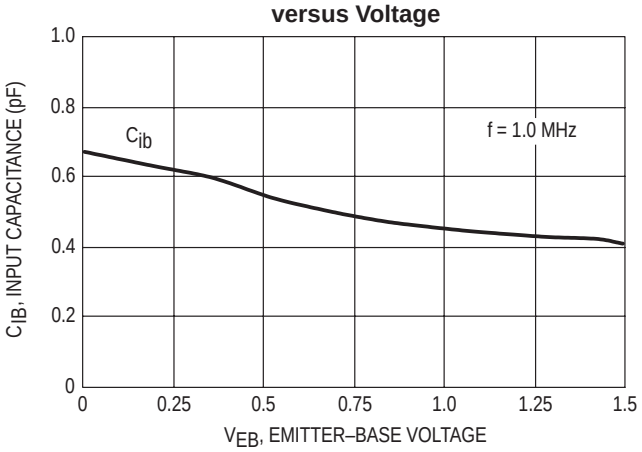


Figure 3. DC Current Gain versus Collector Current

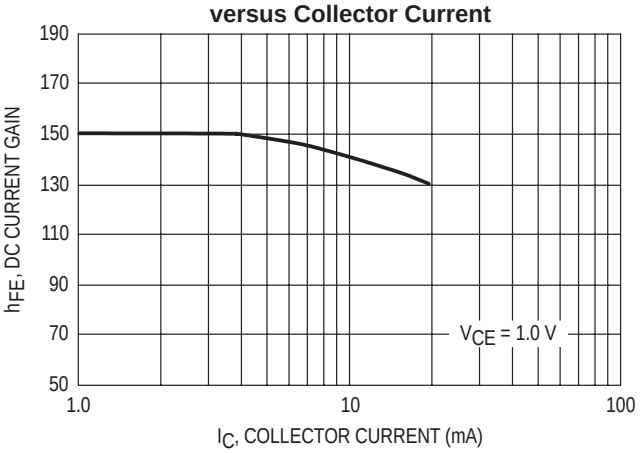


Figure 4. Gain–Bandwidth Product versus Collector Current

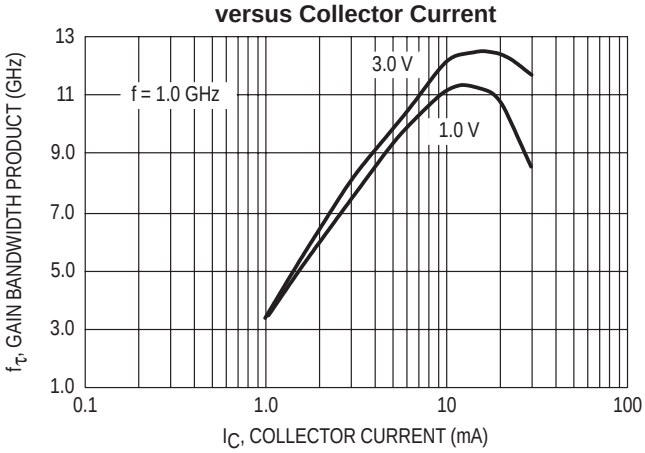


Figure 5. Functional Circuit Schematic

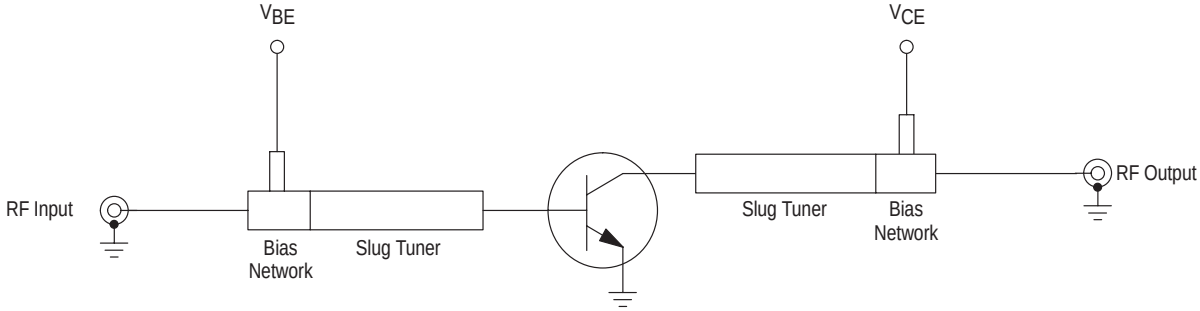


Figure 6. Maximum Stable/Available Gain and Forward Insertion Gain versus Frequency

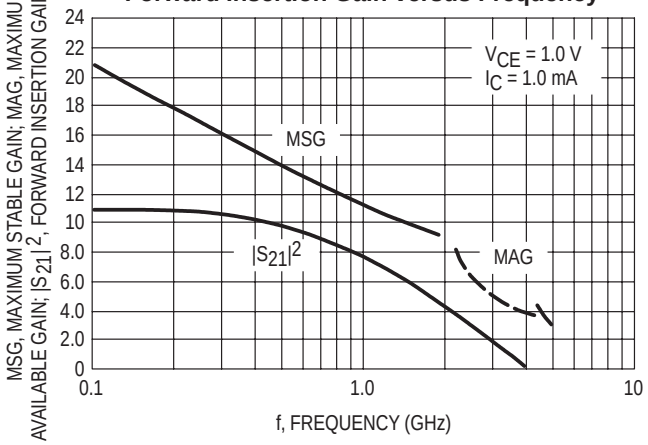


Figure 7. Maximum Stable/Available Gain and Forward Insertion Gain versus Frequency

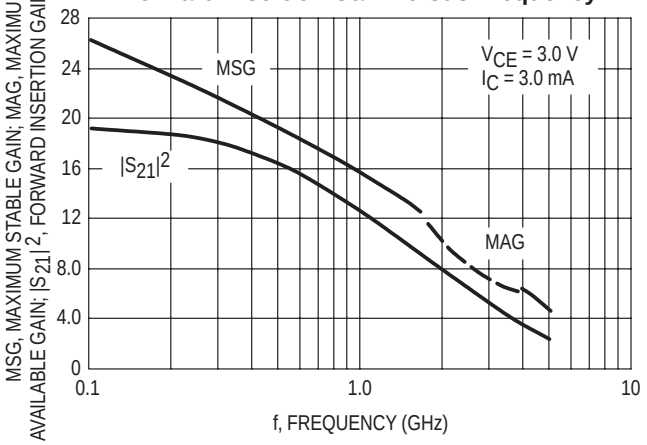


Figure 8. Maximum Stable/Available Gain and Forward Insertion Gain versus Collector Current

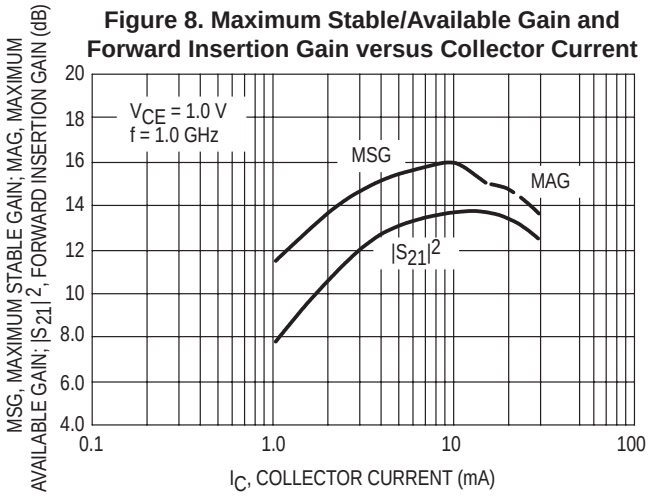


Figure 9. Maximum Stable/Available Gain and Forward Insertion Gain versus Collector Current

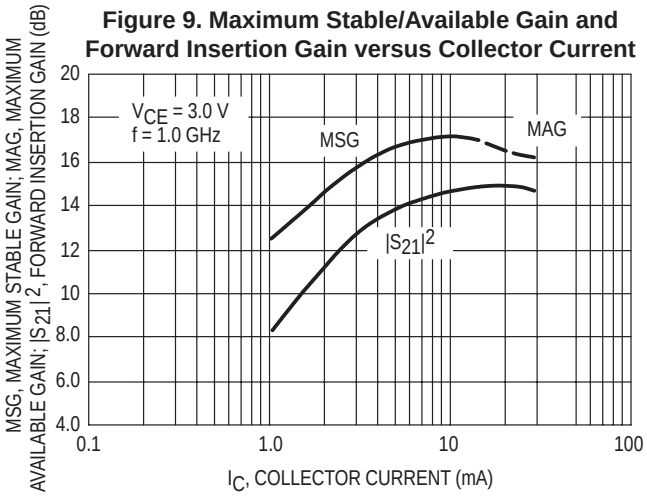


Figure 10. Minimum Noise Figure and Associated Gain versus Frequency

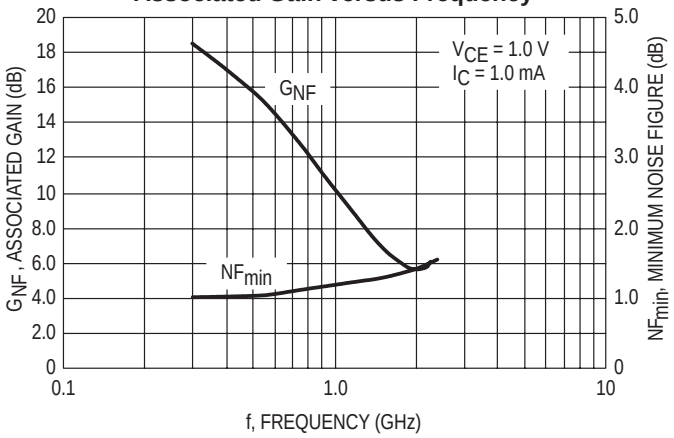


Figure 11. Minimum Noise Figure and Associated Gain versus Frequency

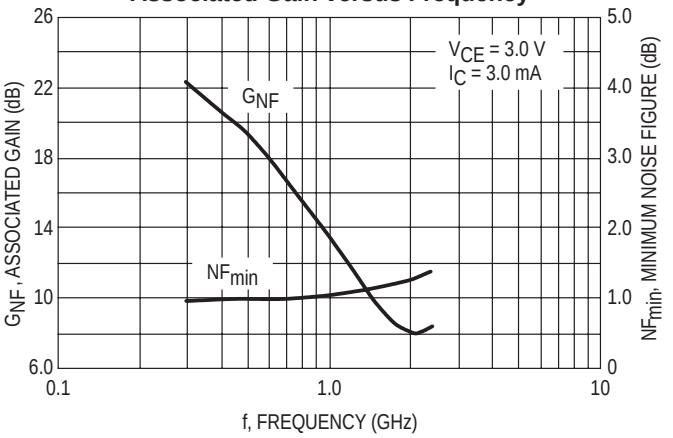


Figure 12. Minimum Noise Figure and Associated Gain versus Collector Current

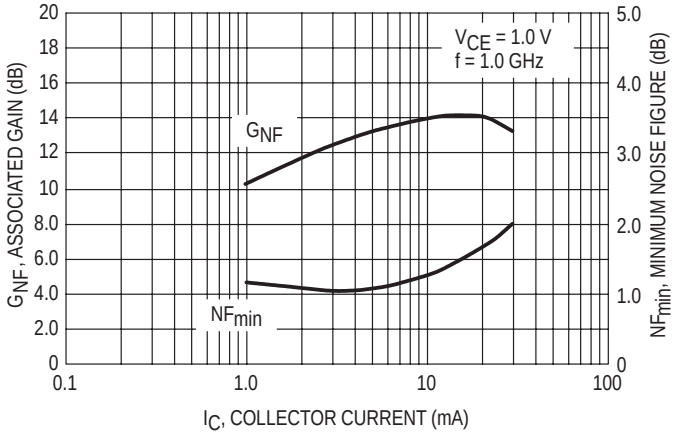


Figure 13. Minimum Noise Figure and Associated Gain versus Collector Current

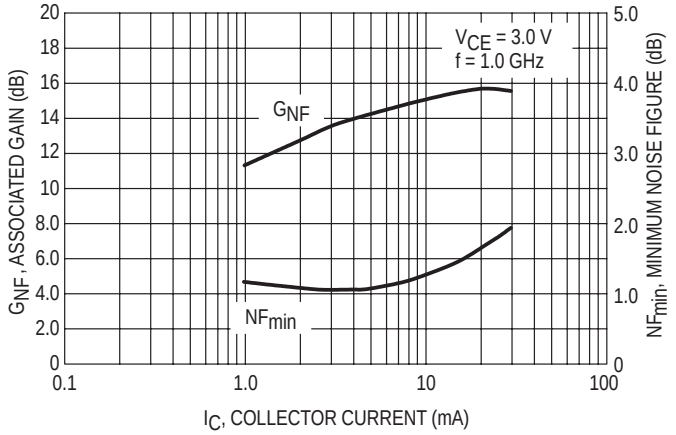


Figure 14. Output Third Order Intercept and Output Power at 1.0 dB Gain Compression versus Collector Current

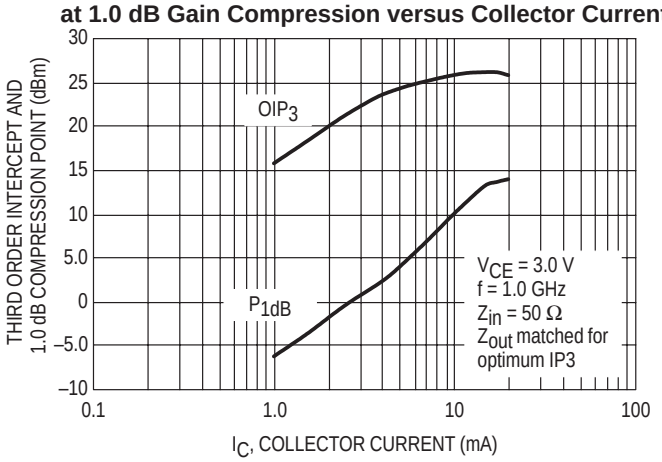


Table 1. Common Emitter S–Parameters

V_{CE} (Vdc)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}		K
			$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ	
1.0	1.0	0.1	0.973	–10	3.49	171	0.029	84	0.987	–6	0.04
		0.3	0.938	–30	3.35	154	0.082	72	0.952	–17	0.12
		0.5	0.875	–48	3.03	137	0.124	60	0.877	–25	0.27
		0.7	0.770	–64	2.75	124	0.153	51	0.812	–33	0.36
		0.9	0.685	–79	2.51	112	0.174	45	0.745	–39	0.45
		1.0	0.649	–85	2.40	107	0.181	42	0.717	–42	0.49
		1.3	0.555	–105	2.09	92	0.195	36	0.639	–48	0.64
		1.5	0.509	–117	1.92	84	0.202	33	0.601	–53	0.72
		1.8	0.454	–136	1.72	72	0.204	30	0.553	–58	0.85
		2.0	0.434	–148	1.59	66	0.205	30	0.531	–62	0.92
		2.5	0.417	–175	1.38	50	0.208	32	0.477	–73	1.09
		3.0	0.403	164	1.23	39	0.227	37	0.457	–83	1.14
		3.5	0.416	142	1.10	28	0.259	41	0.454	–93	1.12
		4.0	0.442	125	1.00	20	0.310	43	0.448	–105	1.05
		4.5	0.454	109	0.95	12	0.378	41	0.433	–118	0.99
		5.0	0.478	96	0.89	6	0.445	37	0.437	–133	0.95
	3.0	0.1	0.917	–17	9.30	165	0.028	80	0.955	–11	0.10
		0.3	0.792	–48	7.94	140	0.072	65	0.831	–29	0.26
		0.5	0.630	–69	6.31	121	0.098	56	0.674	–39	0.47
		0.7	0.505	–87	5.11	107	0.116	51	0.571	–45	0.62
		0.9	0.418	–103	4.26	97	0.131	50	0.498	–49	0.74
		1.0	0.388	–110	3.93	93	0.138	49	0.471	–50	0.78
		1.3	0.317	–129	3.20	82	0.158	49	0.406	–54	0.91
		1.5	0.289	–142	2.84	76	0.172	48	0.380	–58	0.96
		1.8	0.265	–161	2.45	67	0.192	48	0.346	–62	1.02
		2.0	0.260	–173	2.24	61	0.206	48	0.329	–65	1.05
		2.5	0.282	164	1.88	49	0.244	47	0.284	–76	1.07
		3.0	0.283	147	1.65	39	0.287	45	0.271	–85	1.07
		3.5	0.306	128	1.47	30	0.330	42	0.269	–95	1.04
		4.0	0.334	115	1.34	21	0.374	38	0.262	–107	1.02
		4.5	0.354	103	1.25	13	0.423	34	0.256	–119	0.99
		5.0	0.382	93	1.176	6	0.470	29	0.260	–133	0.97
	5.0	0.1	0.861	–23	13.74	160	0.027	78	0.923	–15	0.15
		0.3	0.671	–59	10.50	130	0.064	63	0.727	–36	0.38
		0.5	0.489	–81	7.68	112	0.085	57	0.552	–44	0.62
		0.7	0.379	–100	5.95	100	0.103	56	0.455	–48	0.77
		0.9	0.311	–115	4.82	92	0.119	55	0.393	–50	0.87
		1.0	0.289	–122	4.41	88	0.128	55	0.372	–51	0.90
		1.3	0.241	–143	3.53	78	0.153	55	0.323	–54	0.98
		1.5	0.223	–155	3.11	72	0.171	55	0.303	–57	1.01
		1.8	0.214	–175	2.66	65	0.197	54	0.277	–62	1.04
		2.0	0.217	174	2.43	60	0.215	53	0.263	–65	1.05
		2.5	0.251	154	2.03	49	0.260	50	0.222	–77	1.06
		3.0	0.256	138	1.77	39	0.306	46	0.213	–86	1.05
		3.5	0.282	122	1.58	30	0.351	42	0.212	–97	1.03
		4.0	0.310	110	1.44	22	0.395	37	0.205	–111	1.01
		4.5	0.330	100	1.34	14	0.440	32	0.202	–123	1.00
		5.0	0.360	91	1.26	7	0.483	27	0.206	–138	0.98
3.0	3.0	0.1	0.926	–13	9.03	167	0.021	82	0.967	–8	0.10
		0.3	0.820	–37	7.99	145	0.056	70	0.877	–22	0.26
		0.5	0.673	–55	6.60	126	0.079	61	0.750	–30	0.48
		0.7	0.541	–69	5.47	113	0.096	57	0.663	–34	0.62
		0.9	0.441	–80	4.63	103	0.110	56	0.595	–38	0.73
		1.0	0.402	–85	4.30	99	0.117	55	0.571	–39	0.78
		1.3	0.308	–100	3.53	87	0.136	55	0.512	–42	0.90
		1.5	0.262	–109	3.16	81	0.149	54	0.485	–45	0.95
		1.8	0.208	–126	2.73	72	0.169	54	0.453	–48	1.01
		2.0	0.185	–139	2.50	67	0.183	54	0.436	–51	1.03
		2.5	0.176	–172	2.11	55	0.219	52	0.389	–59	1.06
		3.0	0.160	165	1.85	45	0.259	51	0.379	–66	1.05

Table 1. Common Emitter S–Parameters (continued)

V_{CE} (Vdc)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}		K
			$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ	
		3.5	0.177	137	1.65	35	0.301	48	0.374	–74	1.03
		4.0	0.208	120	1.50	27	0.346	45	0.363	–84	1.00
		4.5	0.228	106	1.40	19	0.395	41	0.354	–93	0.97
		5.0	0.261	96	1.32	11	0.444	37	0.353	–105	0.94
	5.0	0.1	0.884	–19	13.66	162	0.020	80	0.941	–12	0.14
		0.3	0.713	–49	10.92	135	0.052	67	0.786	–28	0.37
		0.5	0.529	–68	8.25	116	0.071	61	0.632	–34	0.61
		0.7	0.406	–83	6.48	104	0.086	59	0.546	–37	0.75
		0.9	0.324	–95	5.31	95	0.101	59	0.489	–38	0.85
		1.0	0.293	–101	4.87	92	0.108	59	0.470	–39	0.89
		1.3	0.223	–118	3.90	82	0.131	59	0.426	–41	0.97
		1.5	0.192	–129	3.45	76	0.146	59	0.406	–44	1.00
		1.8	0.163	–149	2.96	68	0.169	58	0.383	–47	1.03
		2.0	0.155	–163	2.70	64	0.185	57	0.369	–49	1.04
		2.5	0.176	168	2.25	53	0.226	55	0.327	–58	1.05
		3.0	0.174	149	1.96	43	0.269	52	0.321	–65	1.03
		3.5	0.198	128	1.74	34	0.311	48	0.317	–74	1.01
		4.0	0.229	115	1.59	26	0.355	44	0.306	–84	0.99
		4.5	0.249	104	1.47	18	0.400	40	0.299	–93	0.97
		5.0	0.279	95	1.38	11	0.446	35	0.297	–105	0.94
	10.0	0.1	0.781	–27	21.48	155	0.019	77	0.886	–17	0.25
		0.3	0.530	–62	14.32	123	0.045	66	0.648	–33	0.56
		0.5	0.350	–79	9.81	106	0.062	65	0.504	–35	0.80
		0.7	0.257	–92	7.38	96	0.078	66	0.439	–35	0.91
		0.9	0.198	–105	5.90	89	0.096	66	0.401	–35	0.96
		1.0	0.179	–110	5.37	86	0.105	66	0.389	–36	0.98
		1.3	0.133	–128	4.24	78	0.131	65	0.362	–37	1.02
		1.5	0.114	–142	3.73	73	0.149	64	0.348	–40	1.03
		1.8	0.104	–166	3.18	66	0.176	62	0.331	–43	1.03
		2.0	0.106	178	2.90	62	0.194	61	0.320	–46	1.04
		2.5	0.144	154	2.41	52	0.239	57	0.280	–55	1.03
		3.0	0.149	137	2.09	43	0.284	53	0.276	–62	1.02
		3.5	0.176	118	1.85	35	0.327	48	0.273	–72	1.00
		4.0	0.208	108	1.69	27	0.370	43	0.260	–82	0.99
		4.5	0.228	99	1.56	19	0.414	39	0.253	–92	0.97
		5.0	0.257	91	1.47	12	0.457	34	0.250	–104	0.95

Table 2. Common–Emitter Noise Parameters

V_{CE} (Vdc)	I_C (mA)	f (GHz)	NF_{min} (dB)	Γ_O		R_N Ω	r_n	G_{NF} (dB)	K
				Magnitude	Angle				
1.0	1.0	0.3	1.00	0.67	15	28	0.55	18.6	0.12
		0.5	1.04	0.64	25	26	0.52	15.8	0.27
		0.7	1.08	0.61	35	25	0.49	13.3	0.36
		0.9	1.13	0.59	46	23	0.46	11.2	0.45
		1.0	1.16	0.57	51	22	0.44	10.2	0.49
		1.5	1.28	0.52	81	16	0.33	6.8	0.72
		2.0	1.41	0.48	116	10	0.20	5.5	0.92
		2.4	1.52	0.47	146	6.0	0.12	6.0	1.07
	3.0	0.3	0.83	0.56	14	17	0.34	20.9	0.26
		0.5	0.88	0.52	23	16	0.32	18.0	0.47
		0.7	0.94	0.48	32	15	0.30	15.5	0.62
		0.9	0.99	0.45	42	14	0.29	13.3	0.74
		1.0	1.02	0.43	47	14	0.28	12.4	0.78
		1.5	1.16	0.38	79	11	0.22	8.7	0.96
		2.0	1.31	0.35	117	8.0	0.15	7.1	1.05
		2.4	1.44	0.35	152	5.0	0.10	7.3	1.07
	5.0	0.3	0.90	0.48	13	15	0.29	21.6	0.38
		0.5	0.94	0.44	21	14	0.28	18.8	0.62
		0.7	0.98	0.40	31	13	0.26	16.3	0.77
		0.9	1.03	0.36	42	12	0.25	14.1	0.87
		1.0	1.06	0.35	48	12	0.24	13.1	0.90
		1.5	1.20	0.30	82	10	0.19	9.4	1.01
		2.0	1.37	0.28	123	7.0	0.14	7.7	1.05
		2.4	1.53	0.30	161	5.0	0.11	7.7	1.06
3.0	1.0	0.3	1.11	0.67	14	31	0.62	19.7	0.11
		0.5	1.12	0.65	22	30	0.59	16.8	0.26
		0.7	1.13	0.64	31	28	0.56	14.3	0.35
		0.9	1.16	0.62	41	26	0.52	12.2	0.44
		1.0	1.17	0.60	46	25	0.50	11.2	0.48
		1.5	1.26	0.56	74	19	0.38	7.7	0.70
		2.0	1.39	0.51	106	12	0.24	6.5	0.91
		2.4	1.51	0.47	135	7.0	0.15	7.0	1.05
	3.0	0.3	0.94	0.60	13	21	0.41	22.3	0.26
		0.5	0.96	0.57	19	20	0.40	19.3	0.48
		0.7	0.98	0.54	25	19	0.39	16.7	0.62
		0.9	1.01	0.51	33	18	0.36	14.5	0.73
		1.0	1.03	0.50	37	18	0.35	13.5	0.78
		1.5	1.13	0.44	61	15	0.29	9.7	0.95
		2.0	1.26	0.37	92	11	0.21	8.1	1.03
		2.4	1.39	0.32	121	8.0	0.15	8.3	1.06
	5.0	0.3	0.92	0.53	13	17	0.34	22.8	0.37
		0.5	0.95	0.49	20	16	0.32	19.9	0.61
		0.7	0.99	0.46	28	16	0.31	17.4	0.75
		0.9	1.03	0.43	37	15	0.29	15.2	0.85
		1.0	1.06	0.42	42	14	0.28	14.2	0.89
		1.5	1.20	0.36	72	12	0.23	10.4	1.00
		2.0	1.36	0.32	109	8.0	0.17	8.7	1.04
		2.4	1.53	0.30	144	6.0	0.12	8.8	1.05
	10.0	0.3	1.17	0.39	13	15	0.29	23.8	0.56
		0.5	1.18	0.35	21	14	0.28	20.9	0.80
		0.7	1.21	0.32	31	13	0.26	18.3	0.91
		0.9	1.24	0.29	42	13	0.25	16.1	0.96
		1.0	1.26	0.28	48	12	0.25	15.1	0.98
		1.5	1.40	0.24	83	10	0.21	11.2	1.03
		2.0	1.59	0.23	128	8.0	0.16	9.3	1.04
		2.4	1.79	0.24	170	7.0	0.13	9.3	1.03

Table 3. Spice Parameters (MRF1047 Die Gummel–Poon Parameters)

Name	Value	Name	Value	Name	Value
IS	5.8 E–16	IRB	7.50E–03	TF	1.50E–11
BF	180	RBM	4.0	XTF	8.0
NF	0.99	RE	1.0	VTF	4.2355
VAF	40	RC	7.0	ITF	0.2
IKF	0.18	XTB	0	PTF	60
ISE	3.140E–14	EG	1.11	TR	1.00E–09
NE	1.78	XTI	3.0	FC	0.95
BR	26.8	CJE	5.70E–13		
NR	0.9974	VJE	0.98		
VAR	2.0	MJE	0.5		
IKR	7.50E–03	CJC	4.00E–13		
ISC	2.200E–14	VJC	0.59		
NC	1.48	MJC	0.314		
RB	6.924	XCJC	0.6		

Figure 15. MRF1047 SC–70 Package Equivalent Circuit

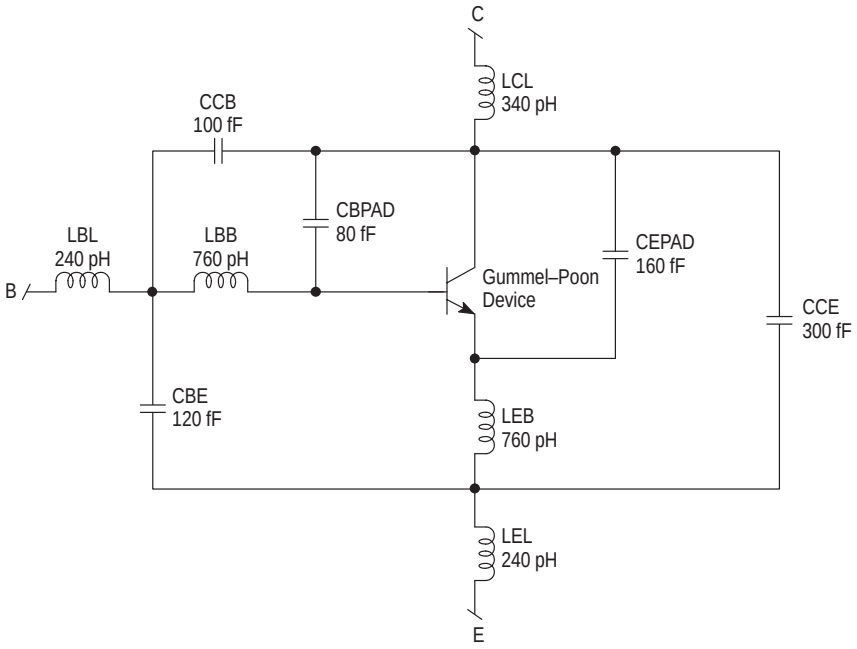
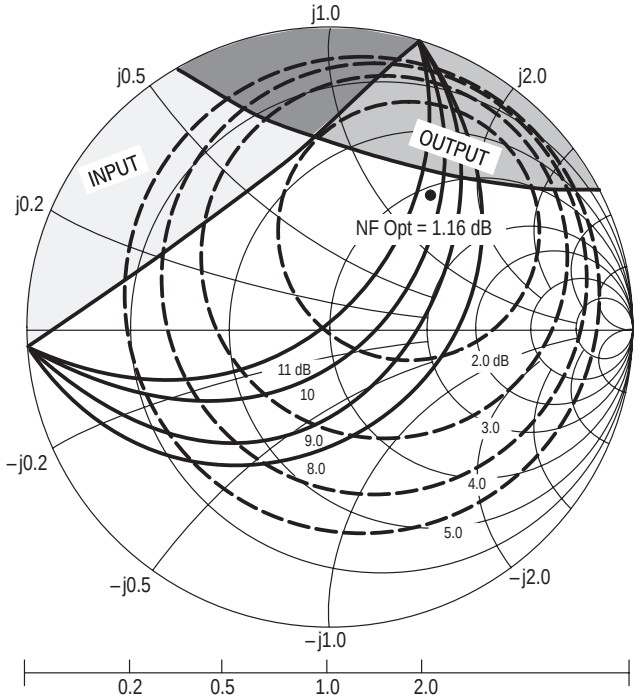


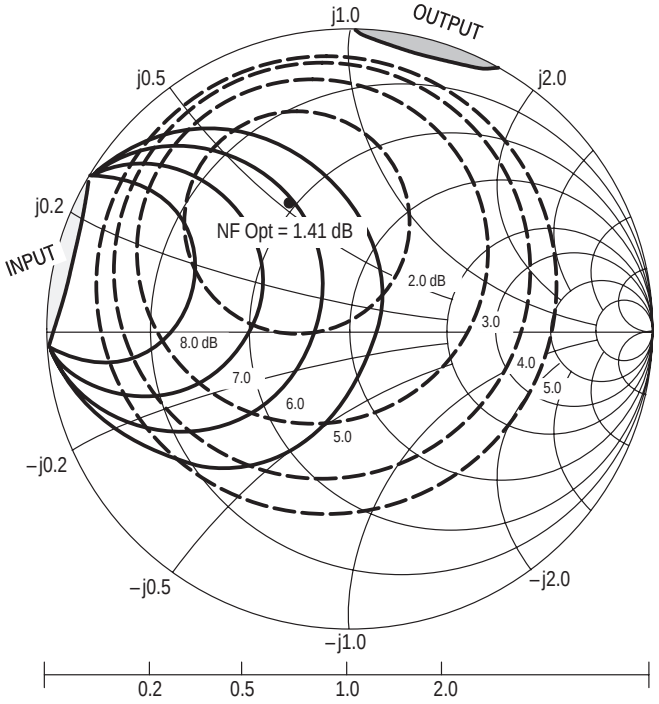
Figure 16. Constant Gain and Noise Figure Contours
(f = 1.0 GHz)



V_{CE} = 1.0 V
I_C = 1.0 mA
— Potentially Unstable

f (GHz)	NF Opt (dB)	Γ_O	Rn	K
1.0	1.16	0.57 ∠ 51.3°	21.8	0.49

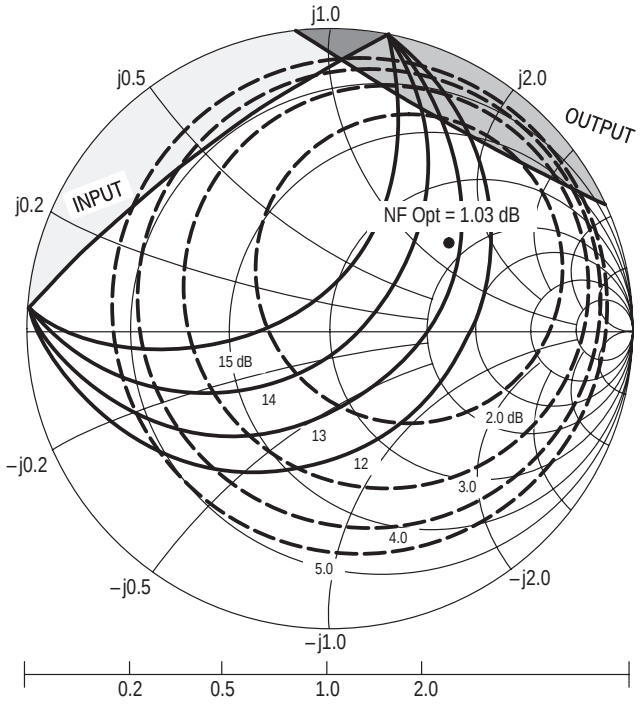
Figure 17. Constant Gain and Noise Figure Contours
(f = 2.0 GHz)



V_{CE} = 1.0 V
I_C = 1.0 mA
— Potentially Unstable

f (GHz)	NF Opt (dB)	Γ_O	Rn	K
2.0	1.41	0.48 ∠ 115.6°	9.8	0.92

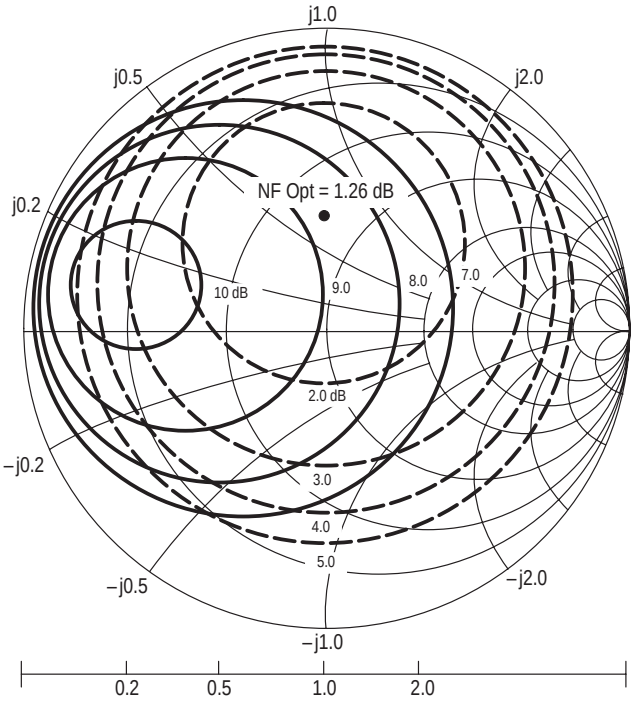
Figure 18. Constant Gain and Noise Figure Contours
(f = 1.0 GHz)



V_{CE} = 3.0 V
I_C = 3.0 mA
— Potentially Unstable

f (GHz)	NF Opt (dB)	Γ_o	Rn	K
1.0	1.03	0.50 ∠ 37.1°	17.6	0.78

Figure 19. Constant Gain and Noise Figure Contours
(f = 2.0 GHz)



V_{CE} = 3.0 V
I_C = 3.0 mA
— Potentially Unstable

f (GHz)	NF Opt (dB)	Γ_o	Rn	K
2.0	1.26	0.37 ∠ 91.7°	10.7	1.03

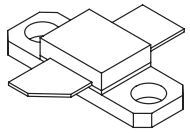
The RF Line
NPN Silicon RF Power Transistor

MRF6404

30 W, 1.88 GHz
RF POWER TRANSISTOR
NPN SILICON

The MRF6404 is designed for 26 volts microwave large signal, common emitter, class AB linear amplifier applications operating in the range 1.8 to 2.0 GHz.

- Specified 26 Volts, 1.88 GHz Characteristics
  Output Power — 30 Watts
  Gain — 7.5 dB Min @ 30 Watts
  Efficiency — 38% Min @ 30 Watts
- Characterized with Series Equivalent Large–Signal Parameters from 1.8 to 2.0 GHz
- To be used in Class AB for DCS1800 and PCS1900/Cellular Radio
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration



CASE 395C–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	24	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Collector–Current — Continuous	I_C	10	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.71	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1)	$R_{\theta JC}$	1.4	°C/W

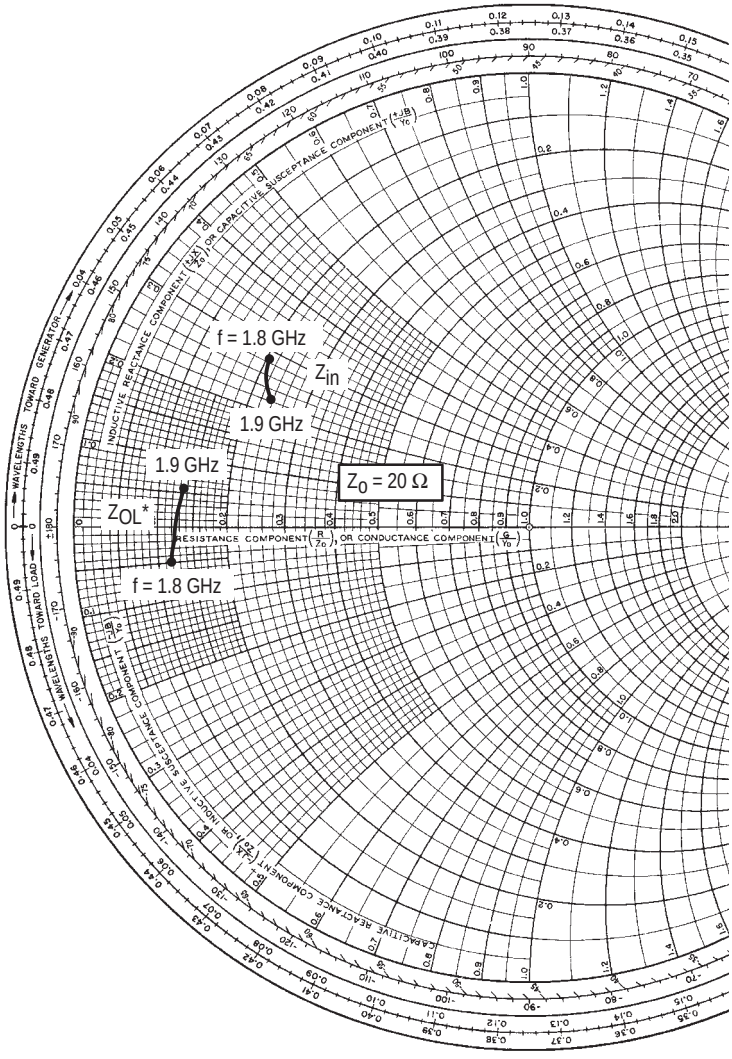
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mA, I_B = 0)	$V_{(BR)CEO}$	24	29	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc)	$V_{(BR)EBO}$	4	5	—	Vdc
Collector–Base Breakdown Voltage (I_C = 50 mAdc)	$V_{(BR)CES}$	60	68	—	Vdc
Collector–Base Breakdown Voltage (I_C = 50 mAdc, R_{BE} = 75 Ω)	$V_{(BR)CER}$	40	56	—	Vdc
Collector Cutoff Current (V_{CE} = 30 V, V_{BE} = 0)	I_{CES}	—	—	10	mA
ON CHARACTERISTICS					
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	50	120	—

(1) Thermal resistance is determined under specified RF operating condition.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 V, I_E = 0, f = 1 MHz) For information only. This part is collector matched.	C_{ob}	30	38	—	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 V, P_{out} = 30 W, I_{CQ} = 150 mA, f = 1.88 GHz)	G_{pe}	7.5	8.5	—	dB
Common–Emitter Amplifier Power Gain (V_{CC} = 26 V, P_{out} = 28 W, I_{CQ} = 150 mA) (f = 1.99 GHz)	G_{pe}	7	8	—	dB
Collector Efficiency (V_{CC} = 26 V, P_{out} = 30 W, f = 1.88 GHz) (V_{CC} = 26 V, P_{out} = 28 W, f = 1.99 GHz)	η	 38 35	 43 40	 — —	%
Output Power at 1 dBc (V_{CC} = 26 V, f = 1.88 GHz) (V_{CC} = 26 V, f = 1.99 GHz)	P_{1dBc}	 30 28	 35 33	 — —	Watts
Output Mismatch Stress: VSWR = 3:1 (all phase angles) (V_{CC} = 26 Vdc, P_{out} = 25 W, I_{CQ} = 150 mA, f = 1.88 GHz)	Ψ	No Degradation in Output Power			



DCS EVALUATION

f (GHz)	Z_{in} (Ω)	Z_{OL}* (Ω)
1.8	4.3 + j6.1	2.7 – j1.0
1.85	4.6 + j5.3	2.9 + j0.3
1.9	4.8 + j5.0	3.0 + j1.2

Z_{OL}*: Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

Figure 1. Input and Output Impedances with Circuit Tuned for Maximum Gain @ V_{CC} = 26 V, I_{CQ} = 150 mA, P_{out} = 30 W

TYPICAL CHARACTERISTICS

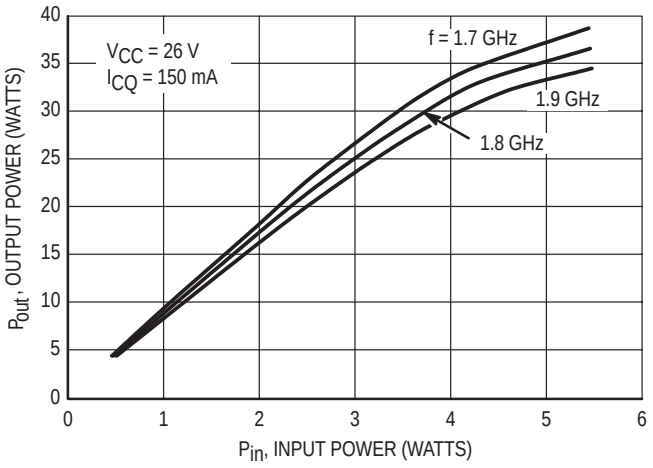


Figure 2. Output Power versus Input Power

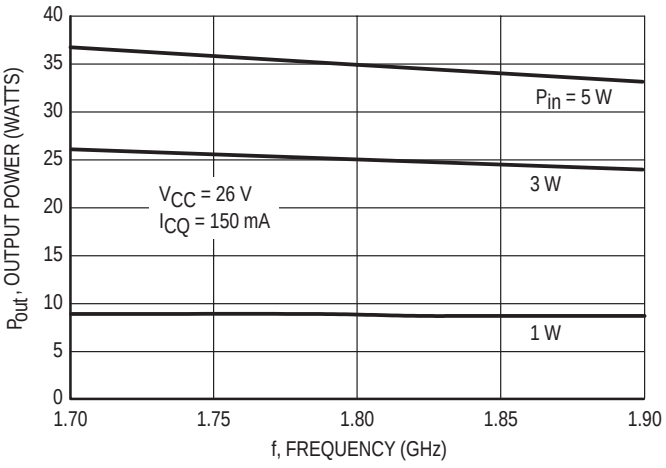


Figure 3. Output Power versus Frequency

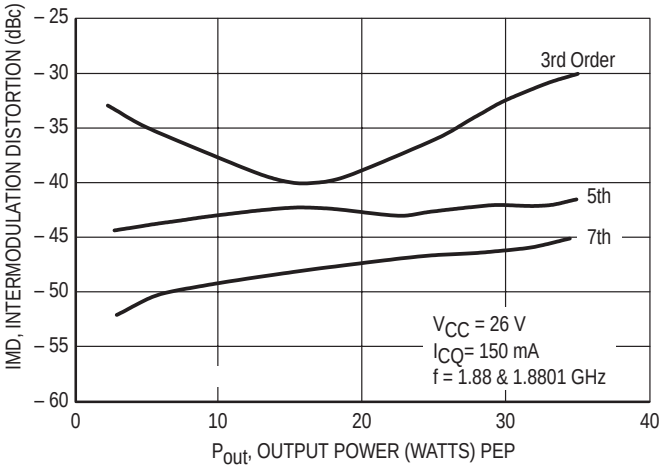


Figure 4. Intermodulation versus Output Power

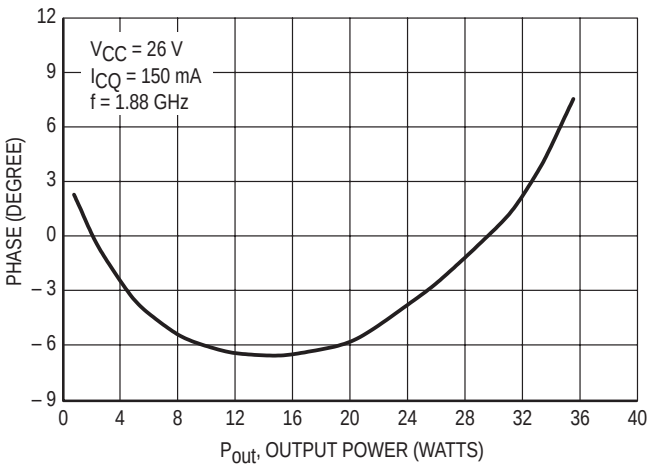
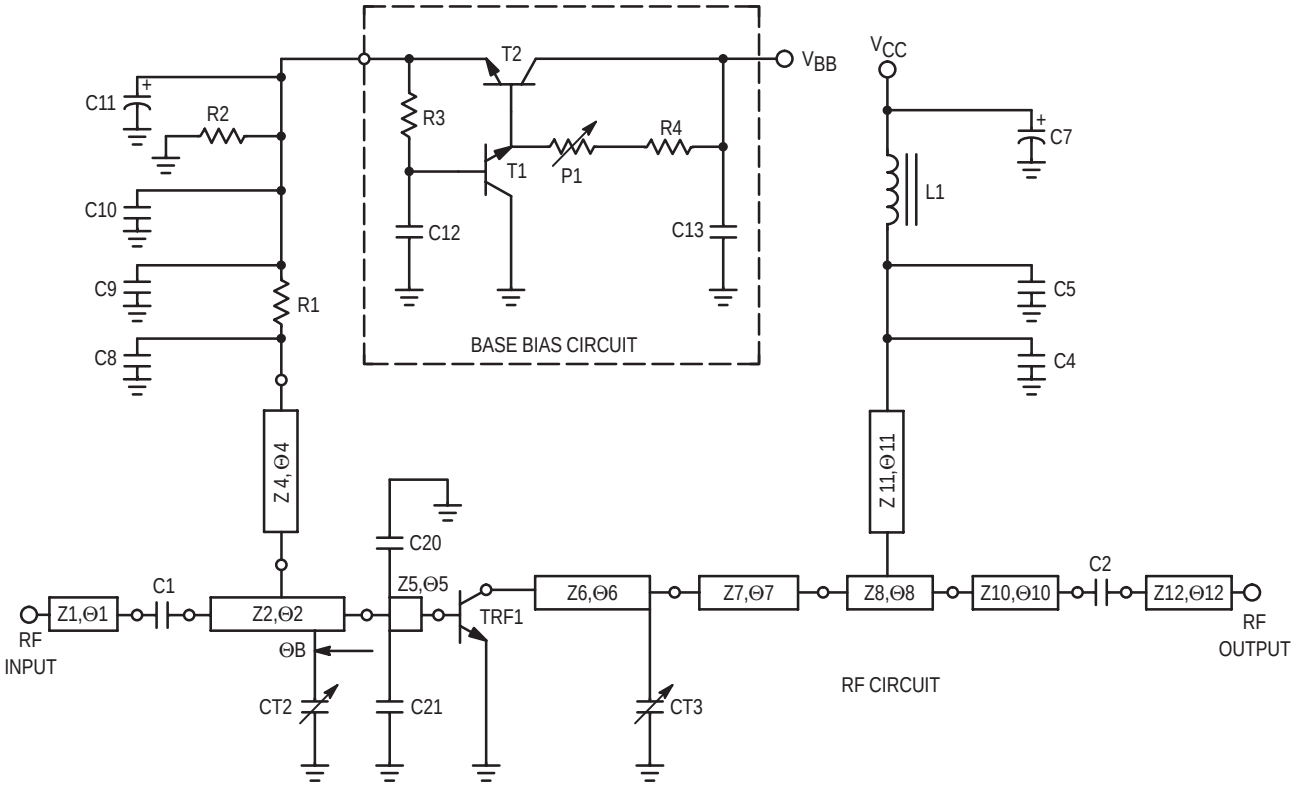


Figure 5. AM/PM Conversion



Base Bias Circuit

C12, C13	15 nF, Chip Capacitor, Vitramon (0805 A153 JXB)
P1	1 KΩ, Trimmer
R3	47 Ω, Chip Resistor, 0805
R4	330 Ω, Chip Resistor, 0805
T1,T2	Motorola MJD 31C

Decoupling Base Bias Circuit

C4	68 pF, Chip Capacitor, ATC 100A
C5, C9	330 pF, Chip Capacitor, Vitramon (0805 A331 JXB)
C7, C11	4.7 μF, 63 V, Electrolytic Capacitor
C8	68 pF, Chip Capacitor, ATC 100A
C10	15 nF, Chip Capacitor, Vitramon (0805 A153 JXB)
R1	1.5 Ω, Chip Resistor, 0805
R2	56 Ω, Chip Resistor, 1206

RF Circuit

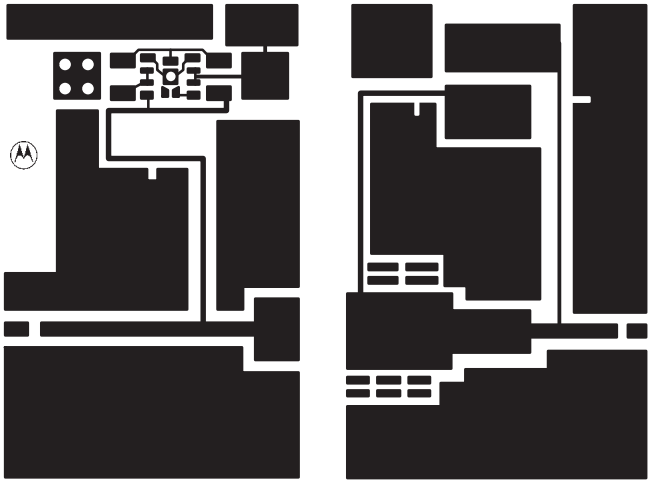
C1, C2	68 pF, Chip Capacitor, ATC 100A
C20, C21	1.3 pF, Chip Capacitor, ATC 100A
CT2	Trimmer Capacitor, Gigatrim, Ref 37281
CT3	Trimmer Capacitor, Gigatrim, Ref 37291
TRF1	MRF6404

PC Board Material:
ε_r = 2.55, H = 0.508 mm, T = 0.035 mm

All Electrical Lengths Are Referenced from λg @ f = 1.9 GHz

Z1 : 50 Ω	Θ1 : 10°
Z2 : 50 Ω	Θ2 : 74.5° ΘB : 16.5°
Z4 : 74 Ω	Θ4 : 68°
Z5 : 12.8 Ω	Θ5 : 21°
Z6 : 10.4 Ω	Θ6 : 49.5°
Z7 : 18 Ω	Θ7 : 36.5°
Z8 : 45 Ω	Θ8 : 20°
Z10 : 50 Ω	Θ10 : 10°
Z11 : 74 Ω	Θ11 : 74.5°
Z12 : 50 Ω	Θ12 : 10°

Figure 6. 1.80 – 1.88 GHz Test Circuit Electrical Schematic and Components List



(Not to Scale)

Teflon® Glass 0.5 mm – Double Side 35 µm Cu.

Figure 7. 1.80 – 1.88 GHz PCN Test Circuit Photomaster

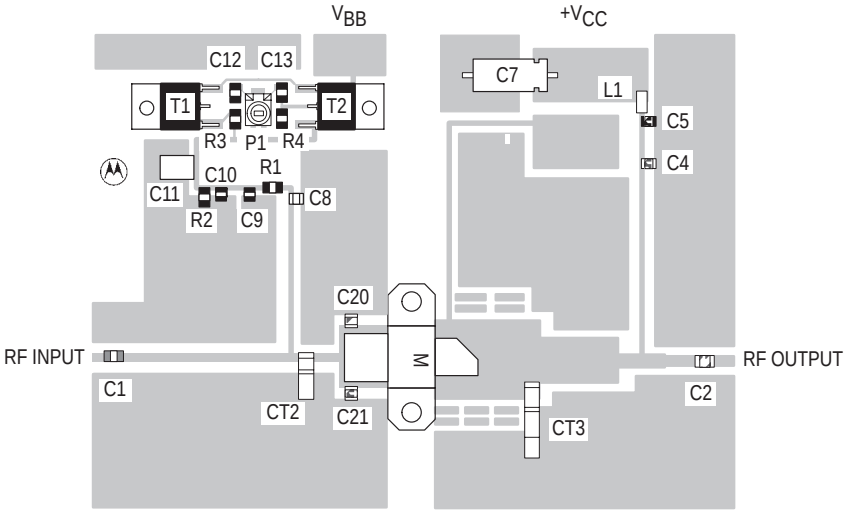
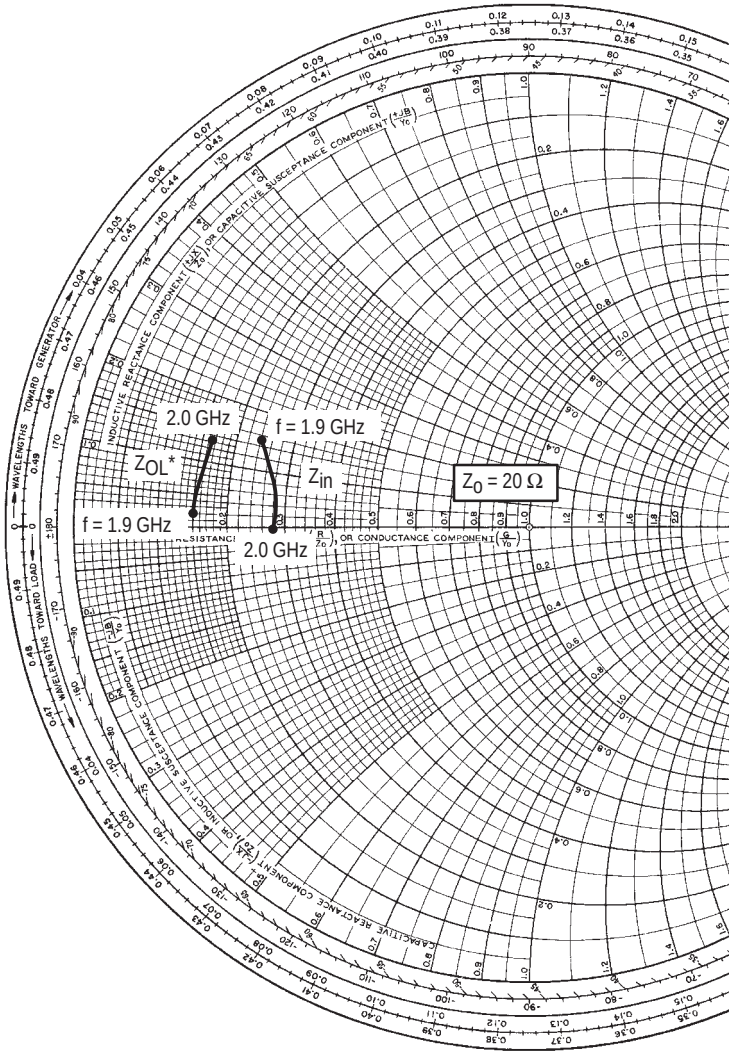


Figure 8. 1.80 – 1.88 GHz PCN Test Circuit Components Layout



PCS EVALUATION

f (GHz)	Z_{in} (Ω)	Z_{OL}* (Ω)
1.90	4.9 + j3.0	3.2 + j0.5
1.93	5.4 + j2.5	3.3 + j1.2
1.97	5.6 + j1.4	3.4 + j1.5
2.00	5.4 – j0.2	3.6 + j2.5

Z_{OL}*: Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

Figure 9. Input and Output Impedances with Circuit Tuned for Maximum Gain @ V_{CC} = 26 V, I_{CQ} = 150 mA, P_{out} = 28 W

TYPICAL CHARACTERISTICS

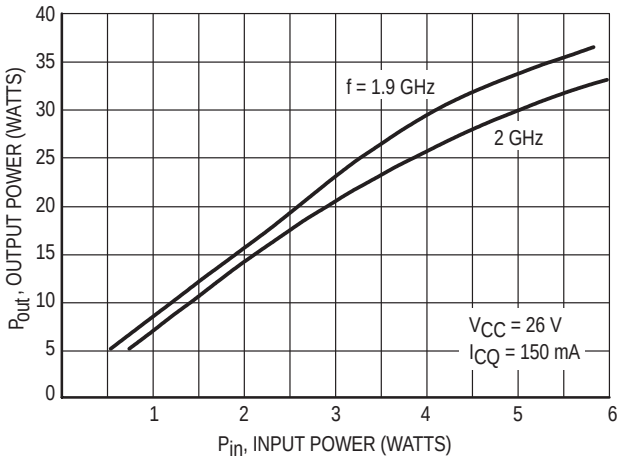


Figure 10. Output Power versus Input Power

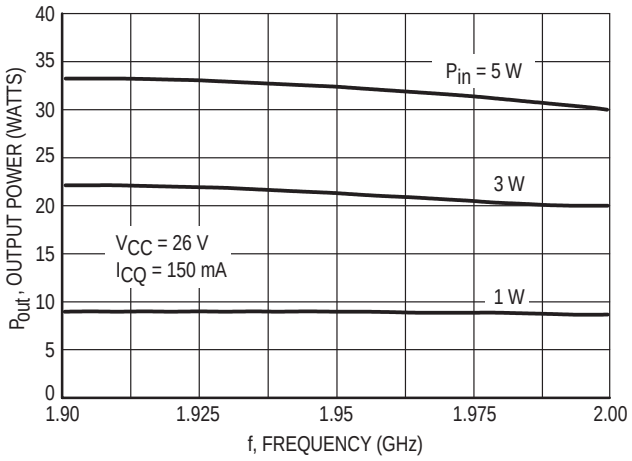


Figure 11. Output Power versus Frequency

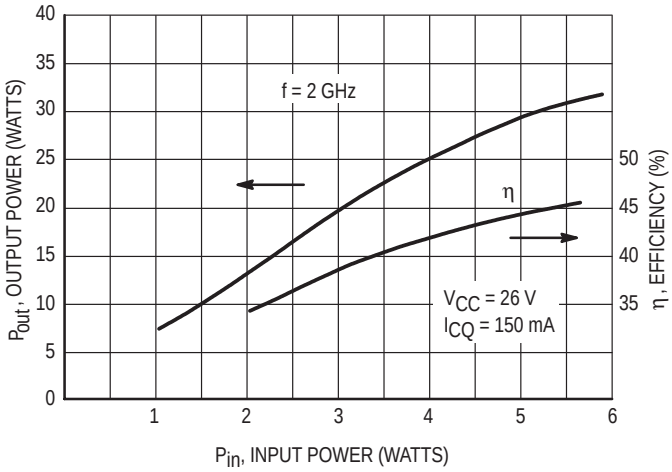


Figure 12. Output Power and Efficiency versus Input Power

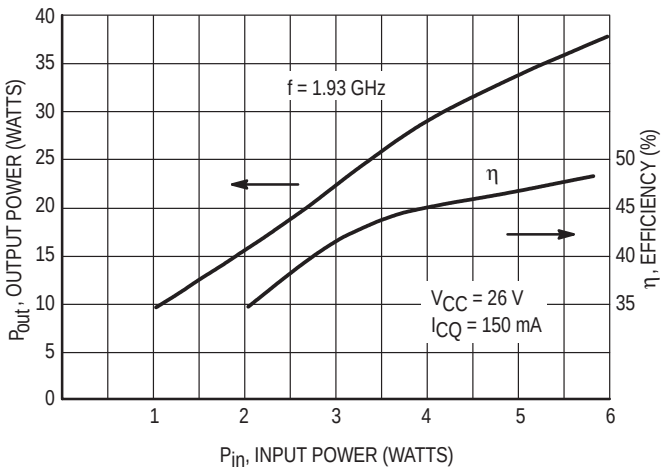


Figure 13. Output Power and Efficiency versus Input Power

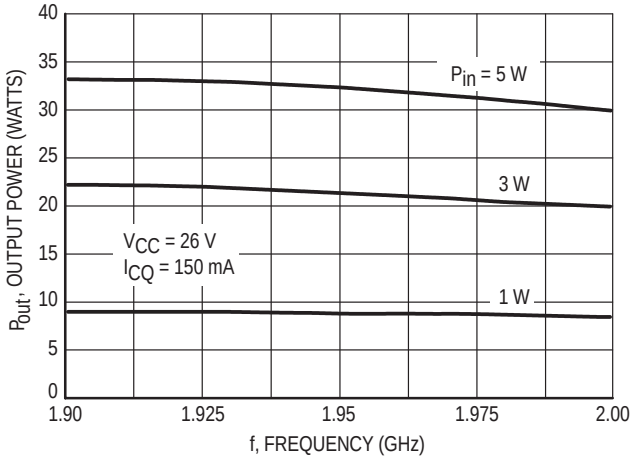
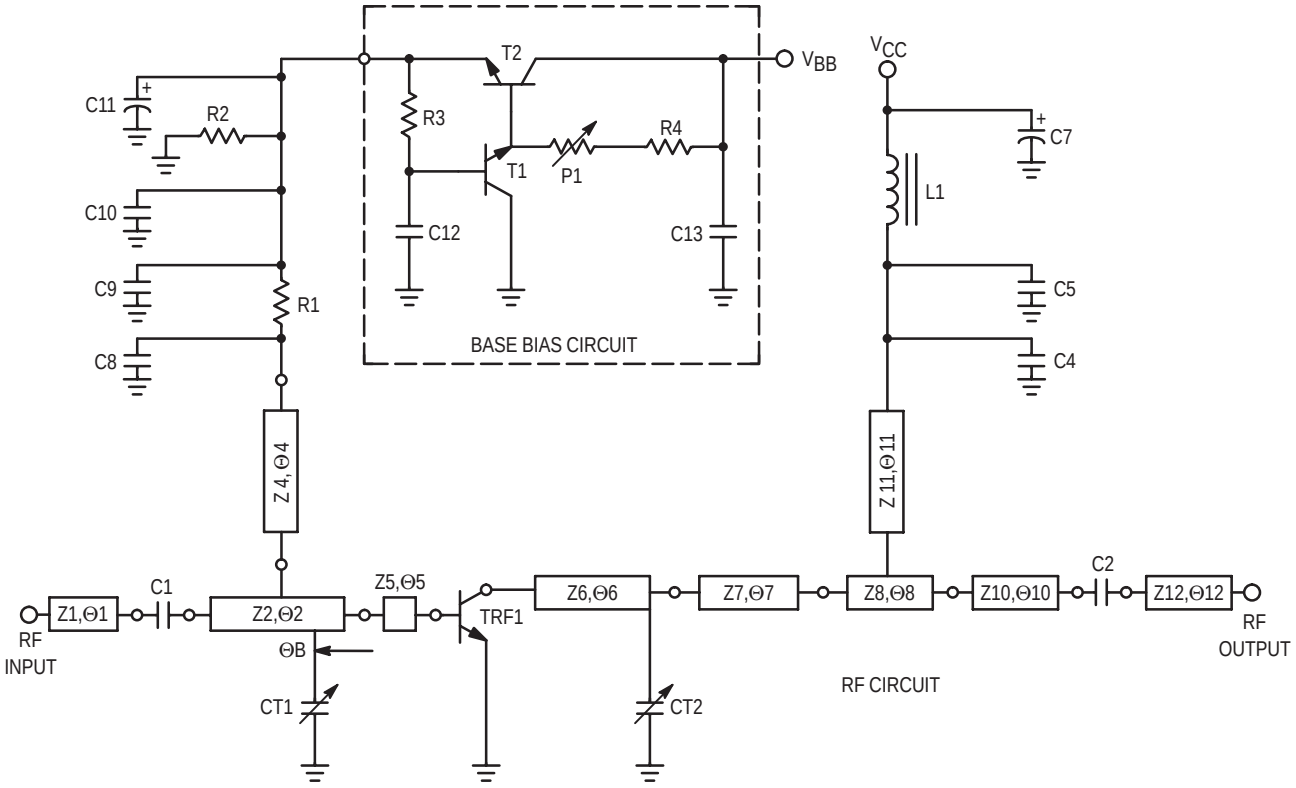


Figure 14. Output Power versus Frequency



Base Bias Circuit

C12, C13	15 nF, Chip Capacitor, Vitramon (0805 A153 JXB)
P1	1 KΩ, Trimmer
R3	47 Ω, Chip Resistor, 0805
R4	330 Ω, Chip Resistor, 0805
T1,T2	Motorola MJD 31C

Decoupling Base Bias Circuit

C4	68 pF, Chip Capacitor, ATC 100A
C5, C9	330 pF, Chip Capacitor, Vitramon (0805 A331 JXB)
C7, C11	4.7 μF, 63 V, Electrolytic Capacitor
C8	68 pF, Chip Capacitor, ATC 100A
C10	15 nF, Chip Capacitor, Vitramon (0805 A153 JXB)
R1	1.2 Ω, Chip Resistor, 0805
R2	56 Ω, Chip Resistor, 1206

RF Circuit

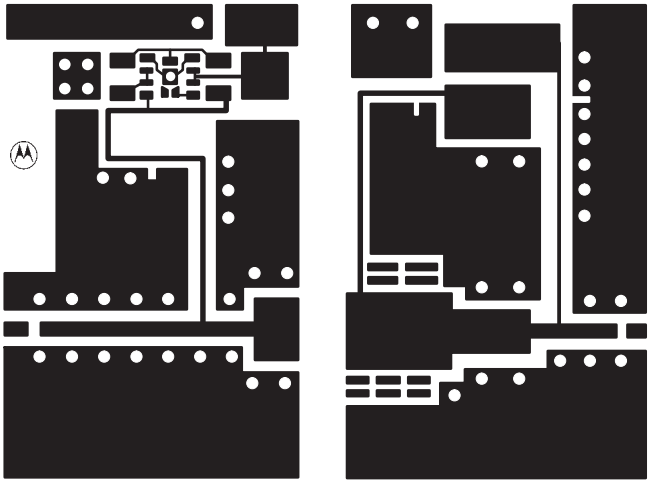
C1, C2	68 pF, Chip Capacitor, ATC 100A
C20, C21	1.3 pF, Chip Capacitor, ATC 100A
CT1, CT2	Trimmer Capacitor, Gigatrim, Ref 37271
TRF1	MRF6404

PC Board Material:
ε_r = 2.55, H = 0.508 mm, T = 0.035 mm

All Electrical Lengths Are Referenced from λg @ f = 1.9 GHz

Z1 : 50 Ω	Θ1 : 10°	
Z2 : 50 Ω	Θ2 : 74.5°	ΘB : 16.5°
Z4 : 74 Ω	Θ4 : 68°	
Z5 : 12.8 Ω	Θ5 : 21°	
Z6 : 10.4 Ω	Θ6 : 49.5°	
Z7 : 18 Ω	Θ7 : 36.5°	
Z8 : 45 Ω	Θ8 : 20°	
Z10 : 50 Ω	Θ10 : 10°	
Z11 : 74 Ω	Θ11 : 60°	
Z12 : 50 Ω	Θ12 : 10°	

Figure 15. 1.9 – 2.0 GHz Test Circuit Electrical Schematic and Components List



(Not to Scale)

Teflon® Glass 0.5 mm – Double Side 35 µm Cu.

Figure 16. 1.9 – 2.0 GHz Test Circuit Photomaster

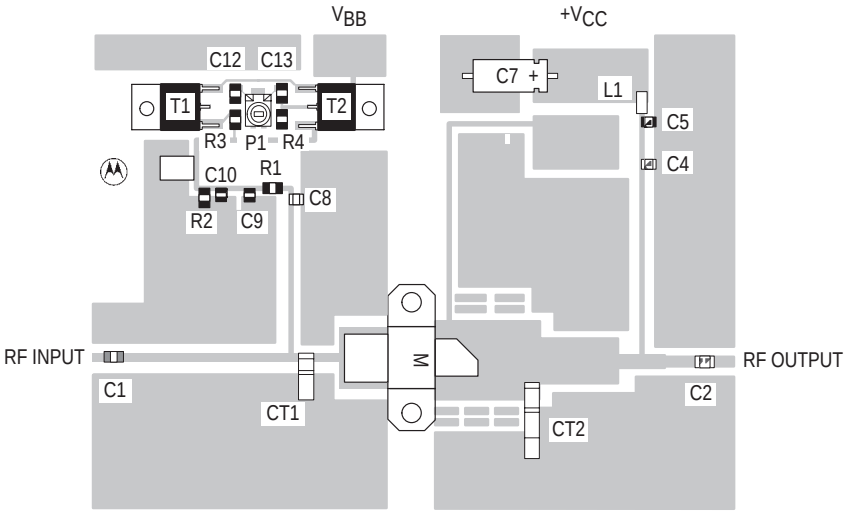


Figure 17. 1.9 – 2.0 GHz Test Circuit Components Layout

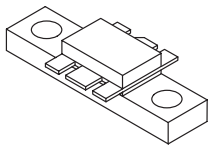
The RF Line
NPN Silicon RF Power Transistor

MRF6409

The MRF6409 is designed for GSM base stations applications. It incorporates high value emitter ballast resistors, gold metallizations and offers a high degree of reliability and ruggedness.

- To be used in Class AB
- Specified 26 Volts, 960 MHz Characteristics
  Output Power — 20 Watts CW
  Gain — 11 dB Typ
  Efficiency — 60% Typ

20 W, 960 MHz
RF POWER TRANSISTOR
NPN SILICON



CASE 319–07, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	24	Vdc
Collector–Emitter Voltage	V_{CES}	55	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector–Current — Continuous	I_C	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	45 0.26	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1)	$R_{\theta JC}$	3.8	°C/W

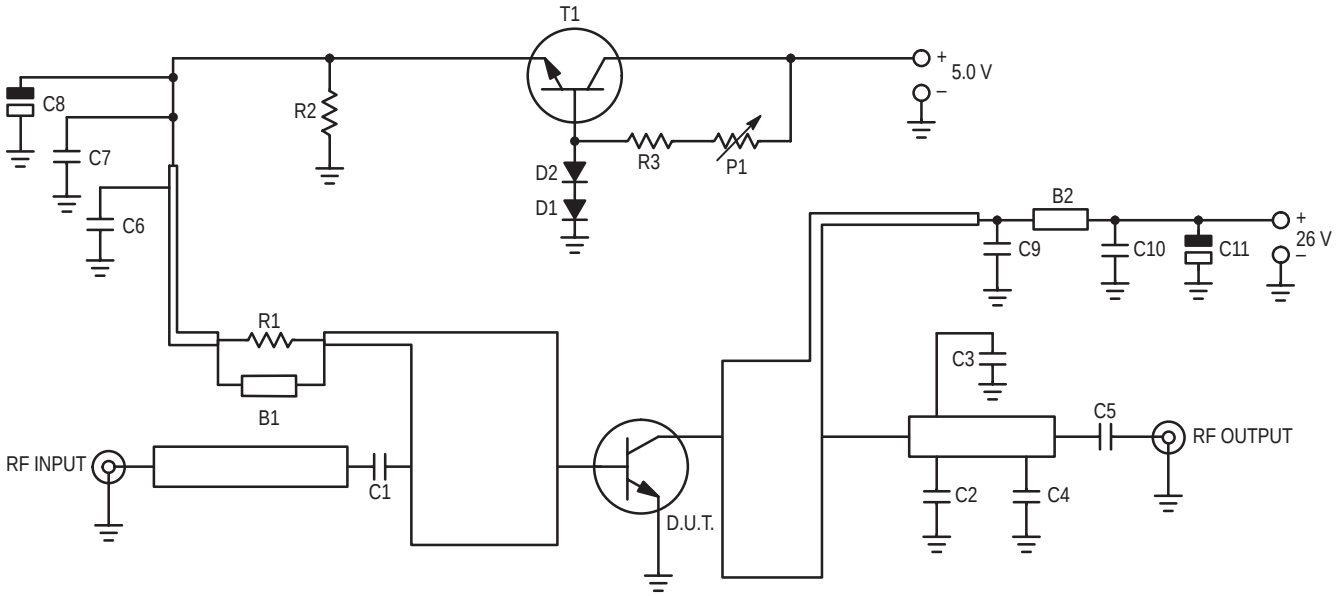
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	24	30	—	Vdc
Emitter–Base Breakdown Voltage (I_B = 5.0 mAdc, I_C =0)	$V_{(BR)EBO}$	4.0	5.0	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	60	—	Vdc
Collector–Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	6.0	mA

(1) Thermal resistance is determined under specified RF operating condition.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	35	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	18	—	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 20 W (CW), I_{CQ} = 50 mA, f = 960 MHz)	G_{pe}	10	11	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 20 W (CW), I_{CQ} = 50 mA, f = 960 MHz)	η	50	60	—	%
Load Mismatch (V_{CC} = 26 Vdc, P_{out} = 15 W (CW), I_{CQ} = 50 mA, f = 960 MHz, Load VSWR = 3:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation in Output Power			



B1, B2	Ferrite Bead
C1	3.3 pF, Chip Capacitor, High Q
C2, C3	4.7 pF, Chip Capacitor, High Q
C4	2.2 pF, Chip Capacitor, High Q
C5	82 pF, Chip Capacitor, High Q
C6, C9	330 pF, Chip Capacitor, High Q
C7, C10	0.1 μF, Chip Capacitor
C8	22 μF, 16 V, Tantalum Capacitor
C11	4.7 μF, 50 V, Tantalum Capacitor
D1, D2	Diode BAS16 Type or Equivalent
P1	1.0 kΩ, Trimmer
R1	3.3 Ω, Chip Resistor
R2	68 Ω, Chip Resistor
R3	2.2 kΩ, Resistor
T1	NPN Transistor
Board	Glass Teflon®, ε_r = 2.55, H = 1/50 inch

Figure 1. Test Circuit Electrical Schematic

TYPICAL CHARACTERISTICS

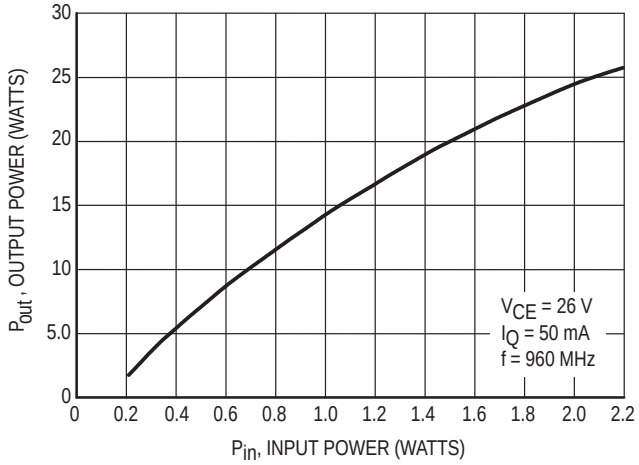


Figure 2. Output Power versus Input Power (CW)

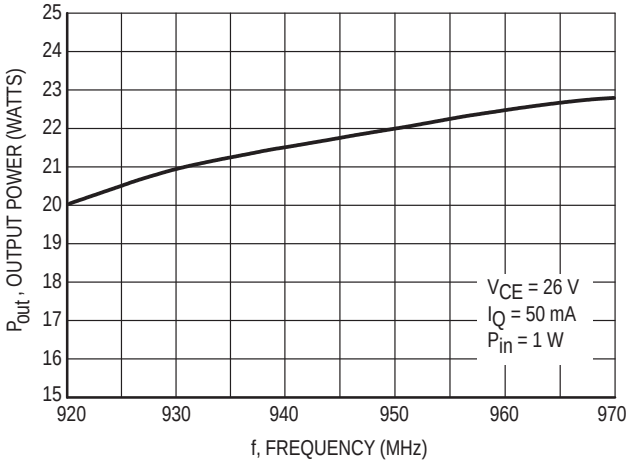


Figure 3. Output Power versus Frequency (CW)

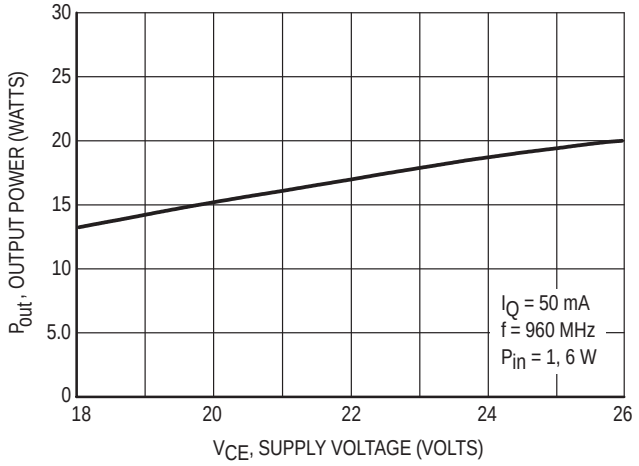


Figure 4. Output Power versus Supply Voltage (CW)

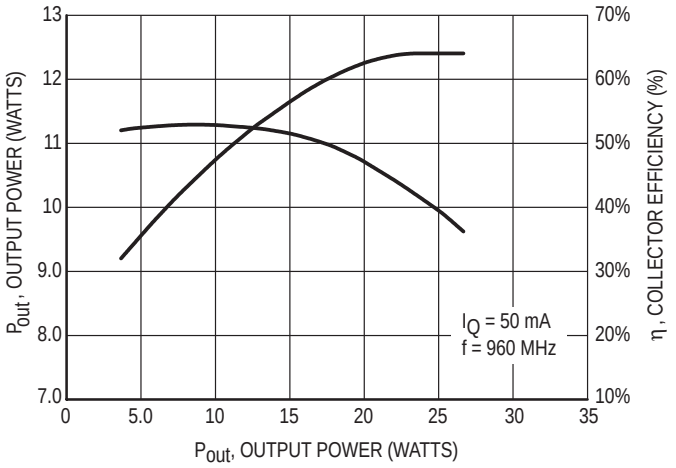


Figure 5. Power Gain and Efficiency versus Output Power

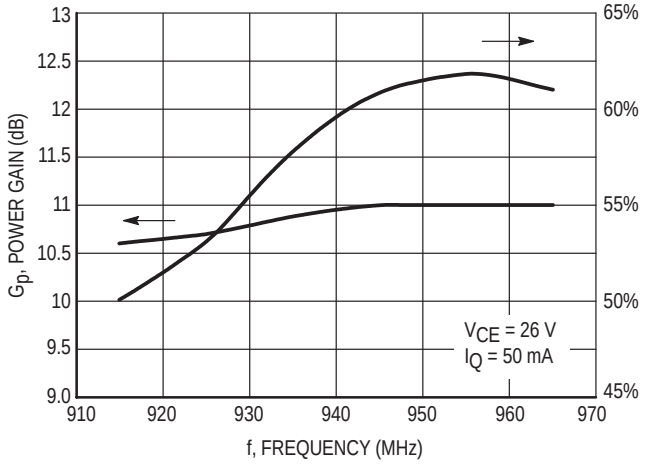


Figure 6. Typical Broadband Performances

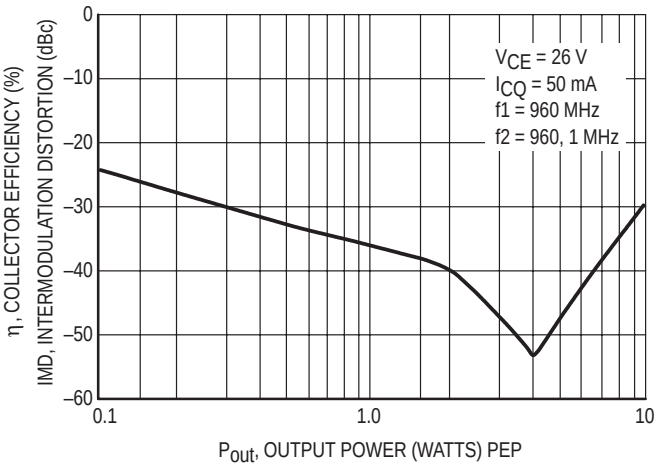
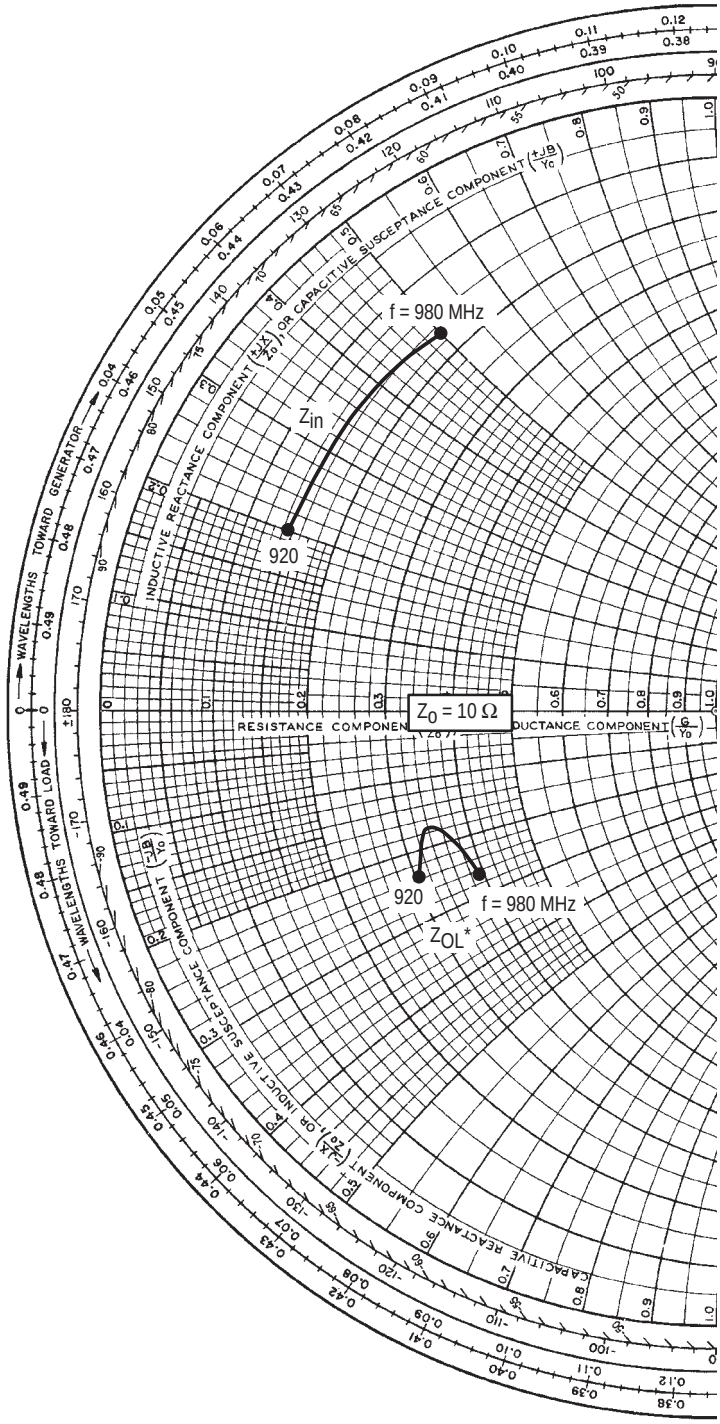


Figure 7. Intermodulation Distortion versus Output Power



f (MHz)	Z_{in} (Ω)	Z_{OL}* (Ω)
920	1.4 + j3.0	3.2 – j2.5
940	1.5 + j3.9	3.5 – j1.88
960	1.5 + j4.2	3.9 – j2.5
980	1.6 + j4.4	4.0 – j2.8

Z_{OL}*: Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

Figure 8. Input and Output Impedances with Circuit Tuned for Maximum Gain @ V_{CC} = 26 V, I_{CQ} = 50 mA, P_{out} = 20 W (CW)

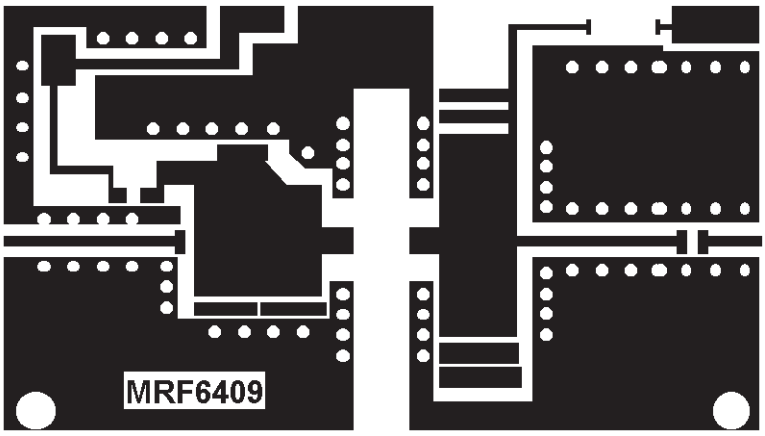


Figure 9. 960 MHz Test Circuit RF, Photomaster Scale 1:1
(Reduced 25% in printed data book, DL110/D)

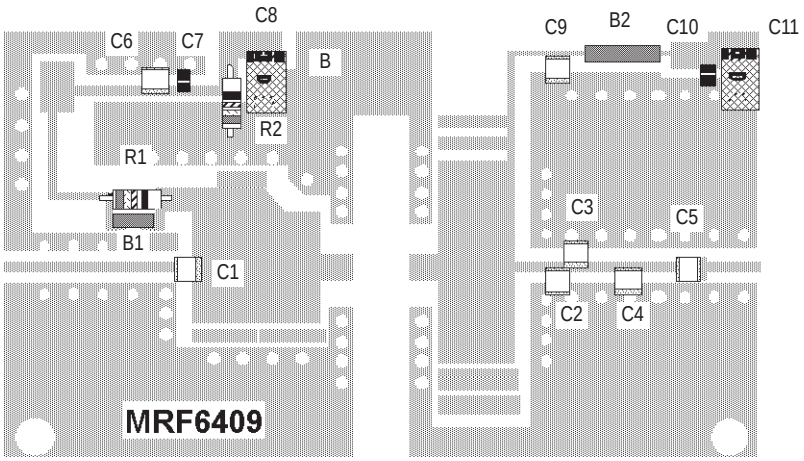


Figure 10. 960 MHz Test Circuit RF, Photomaster Scale 1:1
and Components Location
(Reduced 25% in printed data book, DL110/D)

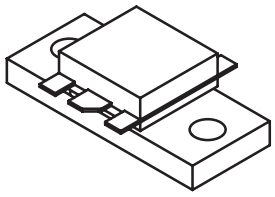
The RF Line
NPN Silicon RF Power Transistor

MRF6414

The MRF6414 is designed for 26 volt UHF large signal, common emitter, class AB linear amplifier applications.

- Specified 26 Volt, 960 MHz Characteristics
  Output Power = 50 Watts
  Minimum Gain = 8.5 dB @ 960 MHz, Class AB
  Minimum Efficiency = 50% @ 960 MHz, 50 Watts
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration

50 W, 960 MHz
RF POWER TRANSISTOR
NPN SILICON



CASE 333A–02, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	28	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Collector–Current — Continuous	I_C	6	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	134 0.77	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.3	°C/W

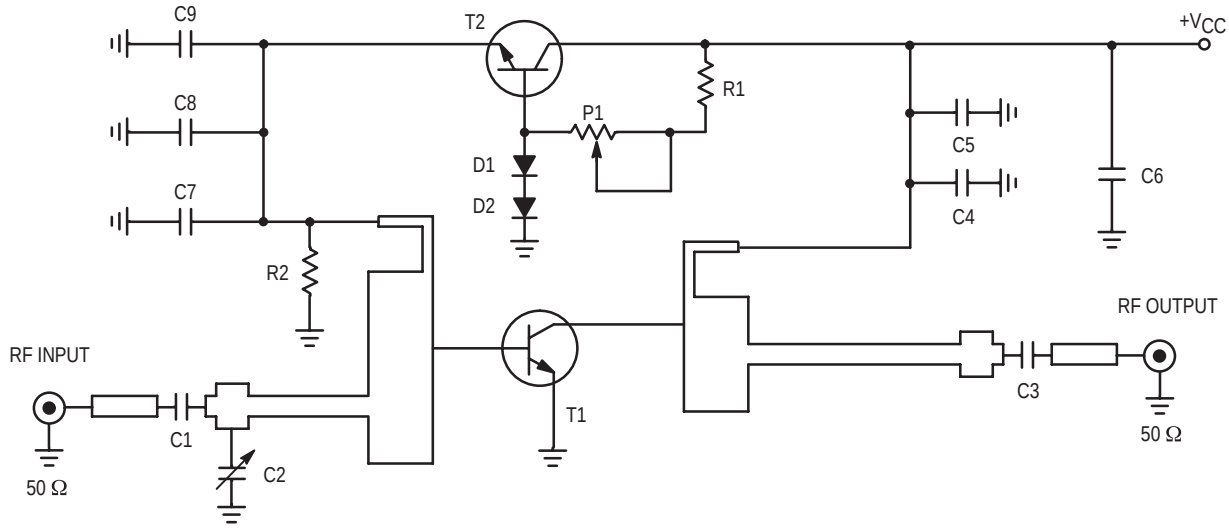
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	28	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 20 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector–Emitter Leakage Current (V_{CE} = 30 Vdc, R_{BE} = 75 Ω)	I_{CER}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	30	—	120	—

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 Vdc, I_E = 0, f = 1 MHz) (1)	C_{ob}	—	45	—	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 50 W, I_{CQ} = 200 mA, f = 960 MHz)	G_{pe}	8.5	—	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 50 W, I_{CQ} = 200 mA, f = 960 MHz)	η	50	55	—	%
Output Mismatch Stress (V_{CC} = 26 Vdc, P_{out} = 50 W, I_{CQ} = 200 mA, f = 960 MHz) VSWR = 3:1; all phase angles at frequency of test	Ψ	No Degradation in Output Power			

(1) For information only. It is not measurable in MRF6414 because of internal matching network.



C1, C3	100 pF, Chip Capacitor, Hight Q	P1	1 kΩ, Trimmer
C2, C7	330 pF, Chip Capacitor, 0805	R1	1 kΩ, Resistor
C5, C8	10 nF, Chip Capacitor, 0805	R2	58 Ω, Resistor, 0805
C6	15 μF, Capacitor, 63 V	T1	MRF6414
C9	100 μF, Capacitor, 16 V	T2	Transistor NPN Type BD135
D1, D2	Diode 1N4007		

Figure 1. 960 MHz Test Circuit Schematic

TYPICAL CHARACTERISTICS

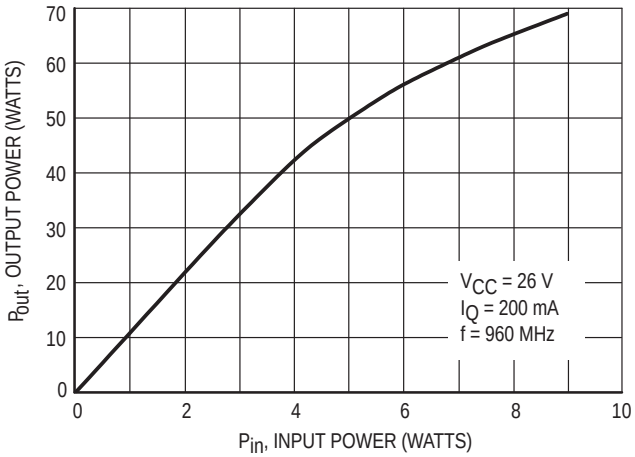


Figure 2. Output Power versus Input Power (Typical)

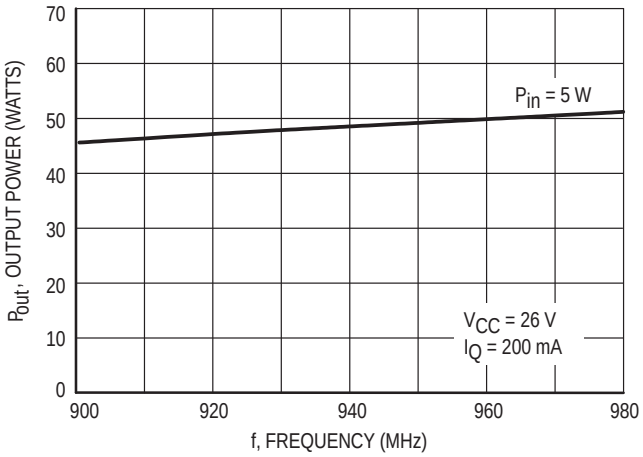


Figure 3. Output Power versus Frequency

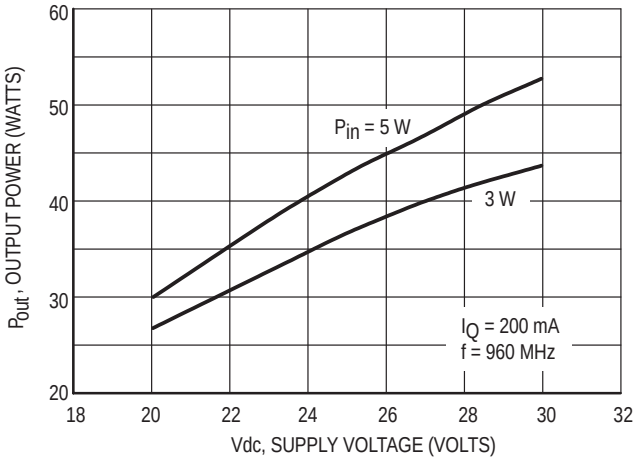


Figure 4. Output Power versus Supply Voltage

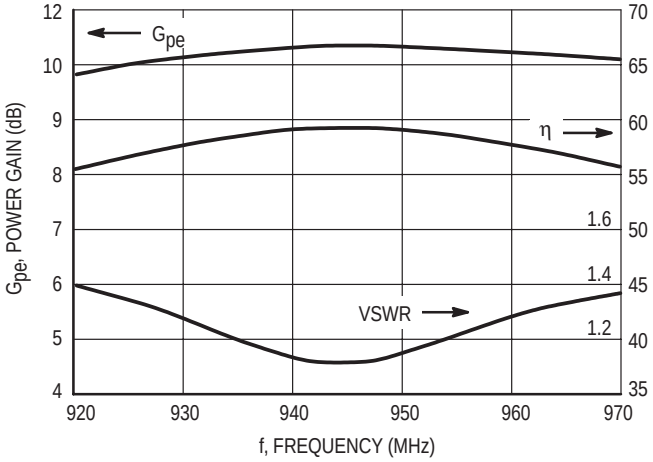
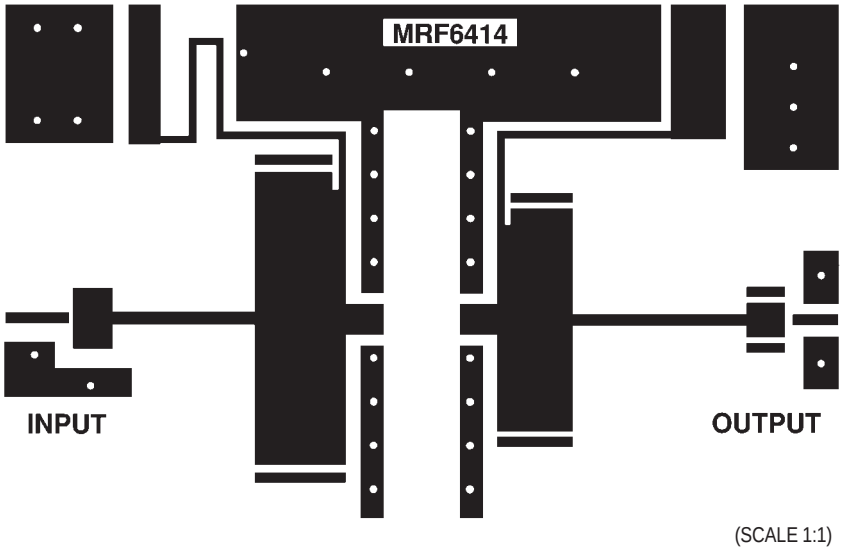


Figure 5. Typical Broadband Amplifier



TEST CIRCUIT @ f = 960 MHz
TEFLON® GLASS 1/50 INCH Er = 2.55

Figure 6. MRF6414 Photomaster
(Reduced 25% in printed data book, DL110/D)

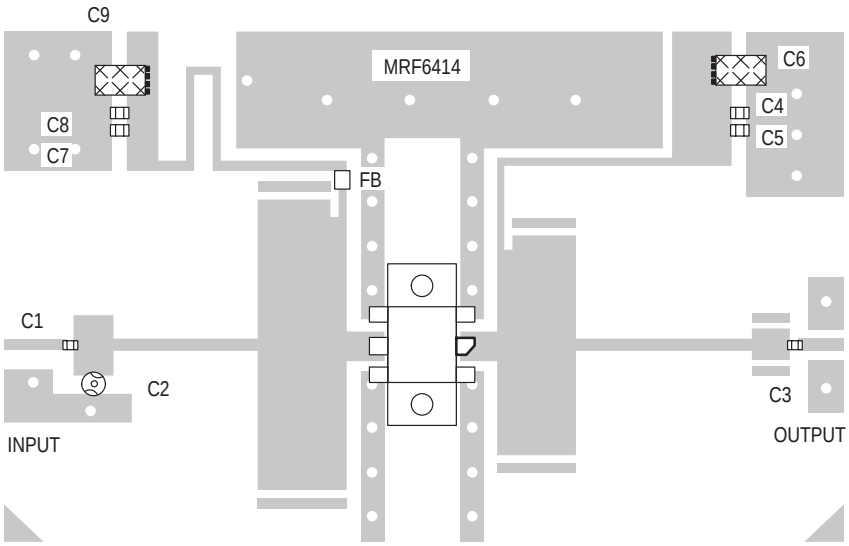
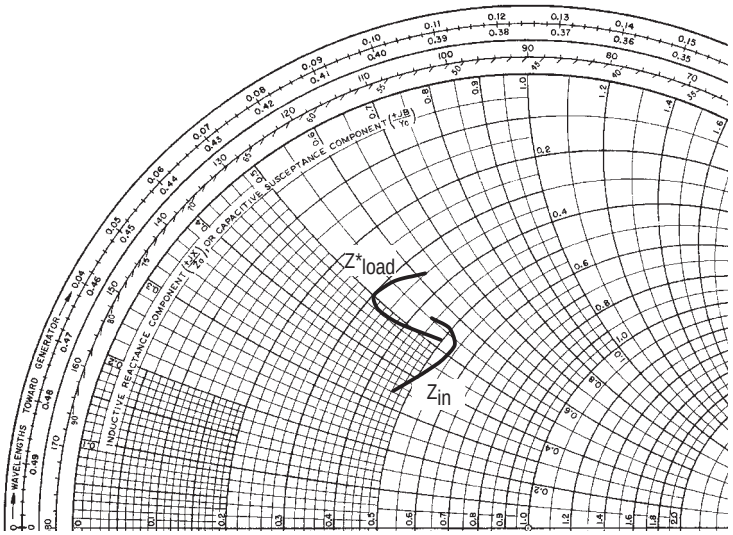


Figure 7. 960 MHz Test Circuit Components Layout



Normalized to 10 Ω

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
900	4.4 + j4.6	4.7 + j4.7
935	5.1 + j4.8	4.0 + j3.9
960	5.4 + j3.6	3.7 + j4.5
980	4.7 + j2.5	3.4 + j4.7

Z_{OL}*: Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

Figure 8. Input and Output Impedances with Circuit Tuned for Maximum Gain @ V_{CC} = 26 V, I_Q = 200 mA, P_{out} = 50 W

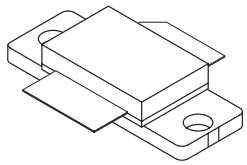
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF6522-70
MRF6522-70R3

Designed for GSM 900 frequency band, the high gain and broadband performances of this device makes it ideal for large–signal, common source amplifier applications in 26 volt base station equipment.

- Specified Performance @ Full GSM Band, 921–960 MHz, 26 Volts
  Output Power, P1dB — 80 Watts (Typ)
  Power Gain @ P1dB — 16 dB (Typ)
  Efficiency @ P1dB — 58% (Typ)
- MRF6522–70 Available in Tape and Reel by Adding R3 Suffix to Part
  Number. MRF6522–70R3 = 250 Units per 32 mm, 13 inch Reel.

70 W, 921 – 960 MHz, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET



CASE 465D–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	7	Adc
Total Device Dissipation @ $T_C \geq 25°C$ Derate above 25°C	P_D	159 0.9	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.1	°C/W

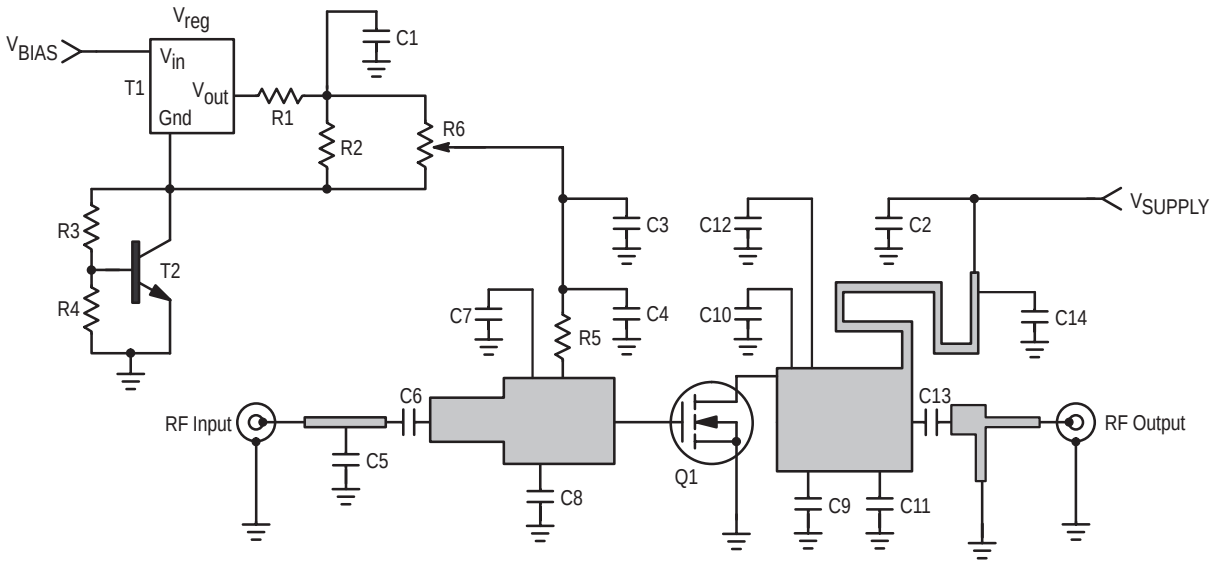
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 20 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 400 mAdc)	$V_{GS(Q)}$	3	4	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.15	0.6	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	2	3	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	130	—	pF
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	41	47	52	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	2.4	3	3.4	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Output Power (2) (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	P1dB	73	80	—	W
Common–Source Amplifier Power Gain @ P1dB (Min) (2) (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	G_{ps}	14	16	18	dB
Drain Efficiency @ P_{out} = 50 W (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	η_1	47	51	—	%
Drain Efficiency @ P1dB (2) (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	η_2	—	58	—	%
Input Return Loss @ P_{out} = 50 W (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = 921 MHz and 960 MHz f = 940 MHz)	IRL	 10 15	 — —	 — —	dB
Output Mismatch Stress (2) (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz, VSWR = 5:1, All Phase Angles)	Ψ	No Degradation In Output Power Before and After Test			

(1) Value excludes the input matching.

(2) To meet application requirements, Motorola test fixtures have been designed to cover full GSM 900 band ensuring batch–to–batch consistency.



C1	1.0 μF, Chip Capacitor 0805	R3	1.2 kΩ, Chip Resistor 0805
C2	10 μF, 35 Vdc Tantalum Capacitor	R4	2.2 kΩ, Chip Resistor 0805
C3	100 nF, Chip Capacitor	R5	220 Ω, Chip Resistor 0805
C4, C6, C14	22 pF, ACCU–P Chip Capacitor 0805	R6	5.0 kΩ SMD Potentiometer
C5	2.7 pF, ACCU–P Chip Capacitor 0805		
C7, C8, C13	4.7 pF, ACCU–P Chip Capacitor 0805	T1	LP2951 Micro–8
C9, C10	8.2 pF, ACCU–P Chip Capacitor 0805	T2	BC847 SOT–23
C11, C12	2.2 pF, ACCU–P Chip Capacitor 0805		
R1	10 Ω, Chip Resistor 0805	SUBSTRATE	GI180 0.8 mm
R2	1.0 kΩ, Chip Resistor 0805		

Figure 1. MRF6522–70 Test Circuit Schematic

TYPICAL CHARACTERISTICS

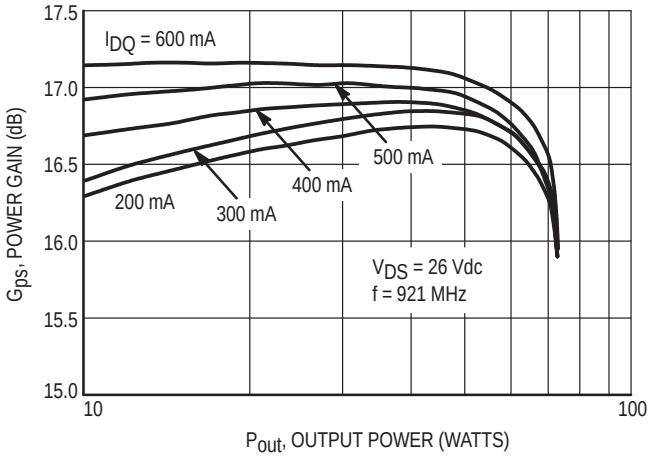


Figure 2. Power Gain versus Output Power

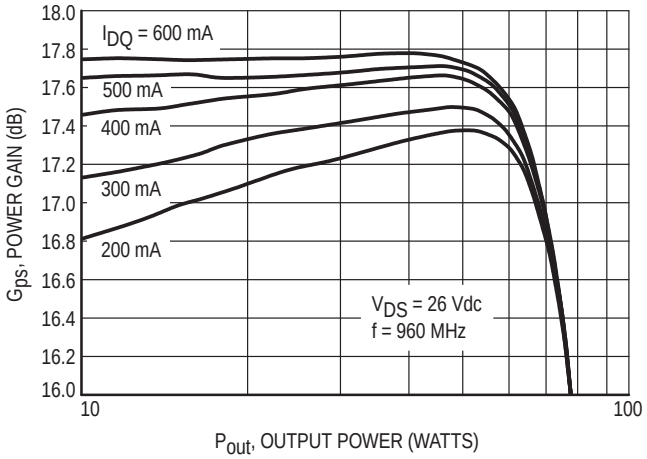


Figure 3. Power Gain versus Output Power

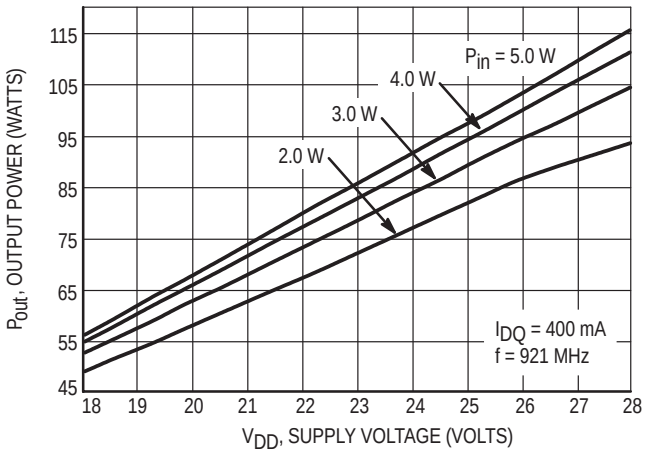


Figure 4. Output Power versus Supply Voltage

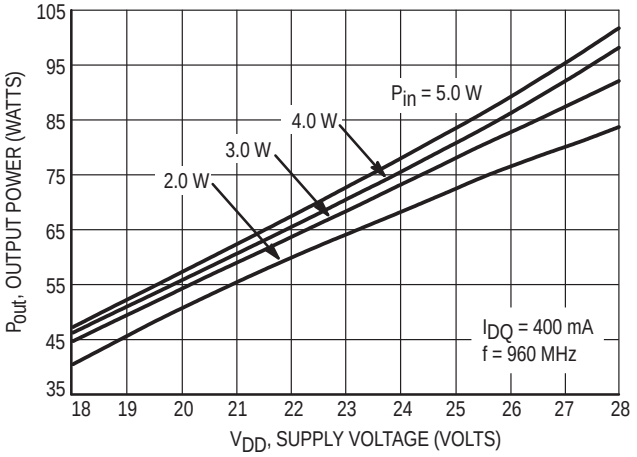


Figure 5. Output Power versus Supply Voltage

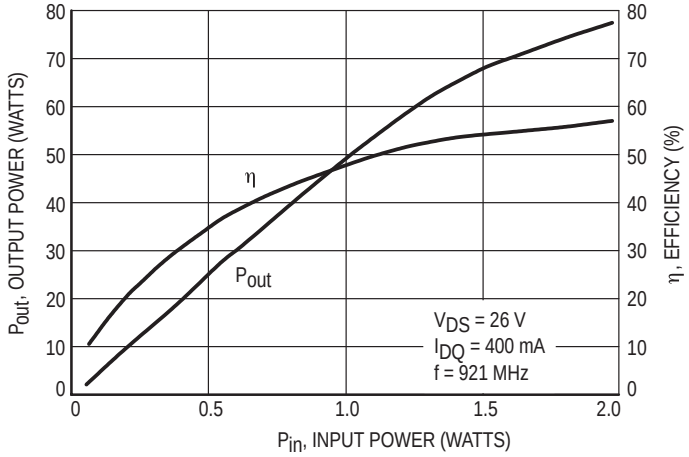


Figure 6. Efficiency and Output Power versus Input Power

TYPICAL CHARACTERISTICS

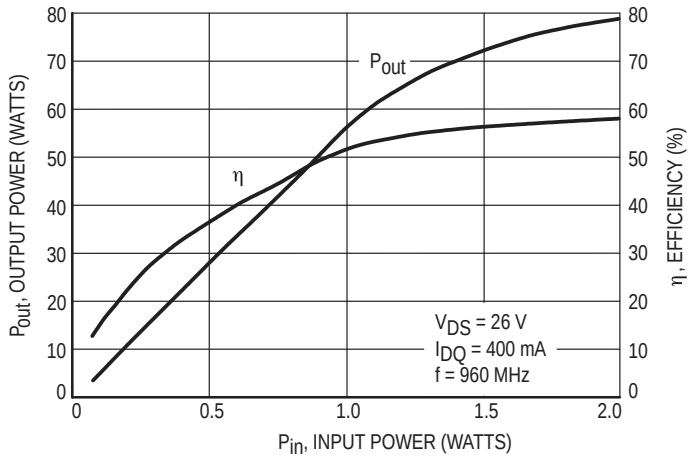


Figure 7. Efficiency and Output Power versus Input Power

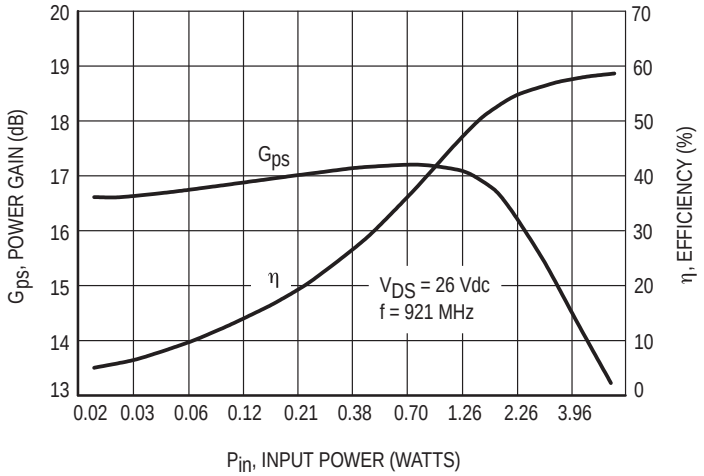


Figure 8. Power Gain and Efficiency versus Input Power

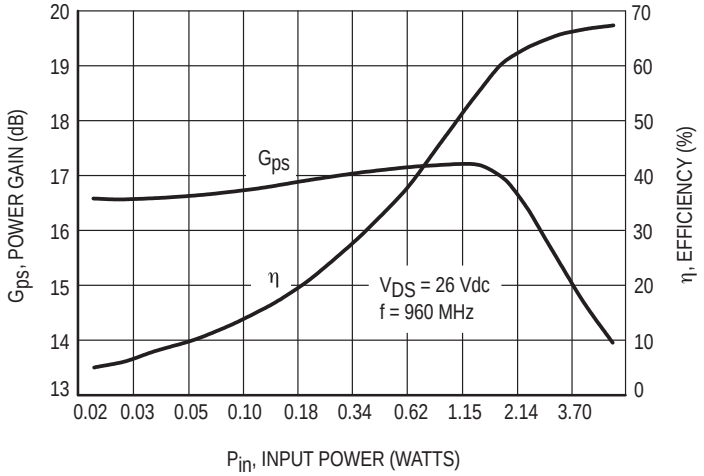


Figure 9. Power Gain and Efficiency versus Input Power

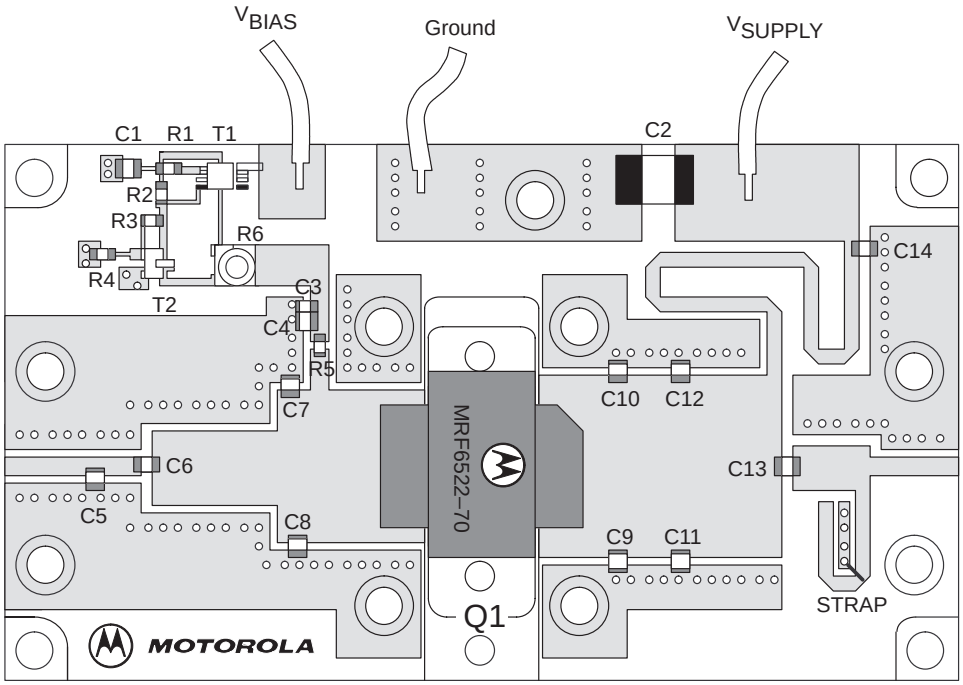


Figure 10. Component Parts Layout

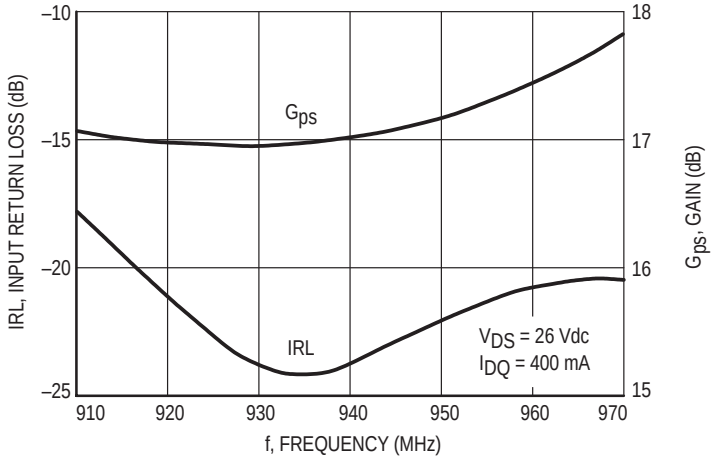
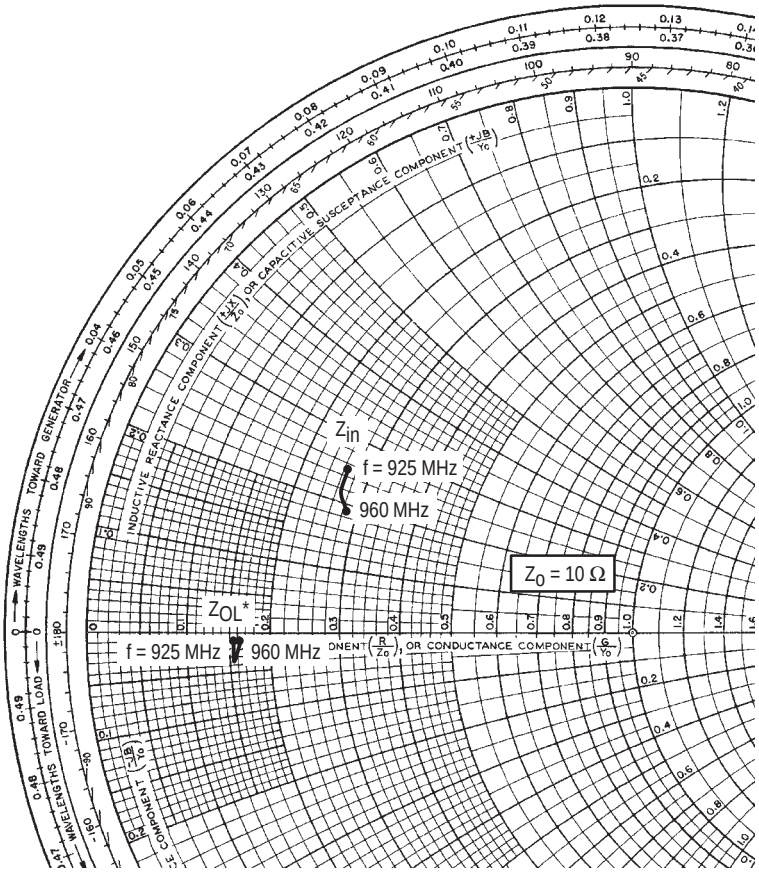


Figure 11. Performance in Broadband Circuit (at Small Signal)



V_{SUPPLY} = 26 Vdc, I_{BIAS} = 400 mA, CW = Room Temperature

f MHz	Z_{in} Ω	Z_{OL}* Ω
925	2.65 + j2.53	1.62 – j0.2
940	2.67 + j2.14	1.56 – j0.34
960	2.85 + j1.87	1.55 – j0.2

Z_{in} = Conjugate of fixture gate terminal impedance.

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Note: Output tuning was chosen based on tradeoffs between P1dB, gain and drain efficiency for GSM application (P1dB = 80 W, gain = 16 dB, efficiency = 56%).

Figure 12. Series Equivalent Input and Output Impedance

MOTOROLA

MRF9382T1

Product Preview

Silicon Lateral FET, N-Channel Enhancement-Mode MOSFET

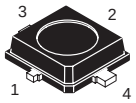
Designed for use in low voltage, moderate power amplifiers such as portable analog and digital cellular radios and PC RF modems.

- Performance Specifications at 900 MHz:
  Output Power = 36.5 dBm Typ
  Power Gain = 10.5 dB Typ
  Efficiency = 65% Typ
- Guaranteed Ruggedness at Load VSWR = 10:1
- New Plastic Surface Mount Package

HIGH FREQUENCY POWER TRANSISTOR LDMOS FET 36.5 dBm, 900 MHz

SEMICONDUCTOR TECHNICAL DATA

Pin 1. Drain
2. Gate
3. Source
4. Source



PLASTIC PACKAGE
CASE 449
(PLD–1, Tape & Reel Only)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	28	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGO}	28	Vdc
Gate–Source Voltage	V_{GS}	±12	Vdc
Drain Current – Continuous	I_D	2.2	Adc
Total Device Dissipation @ T_C = 50°C Derate above 50°C	P_D	12.5 125	W mW/°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Operating Junction Temperature	T_J	150	°C

NOTE: ESD data available upon request.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	8.0	°C/W

ORDERING INFORMATION

Device	Marking	Package
MRF9382T1	9382	PLD–1 Tape & Reel*

*1,000 Units per 12 mm, 7 inch reel.

MOTOROLA

MRF9482T1

Product Preview

Silicon Lateral FET, N-Channel Enhancement-Mode MOSFET

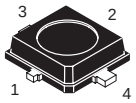
Designed for use in low voltage, moderate power amplifiers such as portable analog and digital cellular radios and PC RF modems.

- Performance Specifications at 900 MHz, 4.8 V
  - Output Power = 36 dBm Typ
  - Power Gain = 10 dB Typ
  - Efficiency = 65% Typ
- Guaranteed Ruggedness at Load VSWR = 10:1
- New Plastic Surface Mount Package

HIGH FREQUENCY POWER TRANSISTOR LDMOS FET 36 dBm, 900 MHz

SEMICONDUCTOR TECHNICAL DATA

Pin 1. Drain
2. Gate
3. Source
4. Source



PLASTIC PACKAGE
CASE 449
(PLD–1, Tape & Reel Only)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	20	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGO}	20	Vdc
Gate–Source Voltage	V_{GS}	±7.0	Vdc
Drain Current – Continuous	I_D	1.1	Adc
Total Device Dissipation @ T_C = 50°C Derate above 50°C	P_D	12.5 125	W mW/°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Operating Junction Temperature	T_J	150	°C

NOTE: ESD data available upon request.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	8.0	°C/W

ORDERING INFORMATION

Device	Marking	Package
MRF9482T1	9482	PLD–1 Tape & Reel*

*1,000 Units per 12 mm, 7 inch reel.

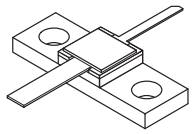
The RF Line
Microwave Power Transistor

. . . designed for CW and long pulsed common base amplifier applications, such as JTIDS and Mode S, in the 0.96 to 1.215 GHz frequency range at high overall duty cycles.

- Guaranteed Performance @ 1.215 GHz, 28 Vdc
  Output Power = 5.0 Watts CW
  Minimum Gain = 8.5 dB, 10.3 dB (Typ)
- RF Performance Curves given for 28 Vdc and 36 Vdc Operation
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Industry Standard Package
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input Matching for Broadband Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

MRF10005

5.0 W, 960 – 1215 MHz
MICROWAVE POWER
TRANSISTOR
NPN SILICON



CASE 336E–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	55	Vdc
Collector–Base Voltage	V_{CBO}	55	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Continuous (1)	I_C	1.25	mAdc
Total Device Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	25 143	Watt mW/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Junction Temperature	T_J	200	°C

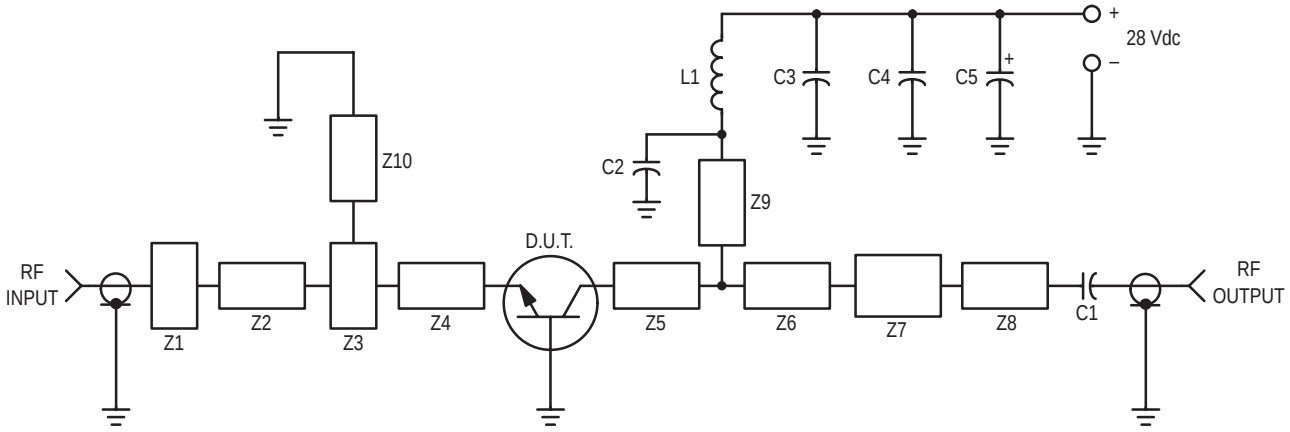
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	7.0	°C/W

NOTES:
1. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
2. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 25 mAdc, I_E = 0)	$V_{(BR)CBO}$	55	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.5 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 28 Vdc, I_E = 0)	I_{CBO}	—	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	7.0	10	pF
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 5.0 W, f = 1215 MHz)	G_{PB}	8.5	10.3	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 5.0 W, f = 1215 MHz)	η	45	55	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 5.0 W, f = 1215 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1, C2, C3 — 220 pF 100 mil Chip Capacitor
C4 — 0.1 μF
C5 — 47 μF/50 V Electrolytic
L1 — 3 turn #18 AWG, 1/8″ ID, 0.18″ Long

Z1–Z10 — Microstrip, see details below
Board Material — 0.030″ Glass Teflon,
2.0 oz. Copper, ε_r = 2.55

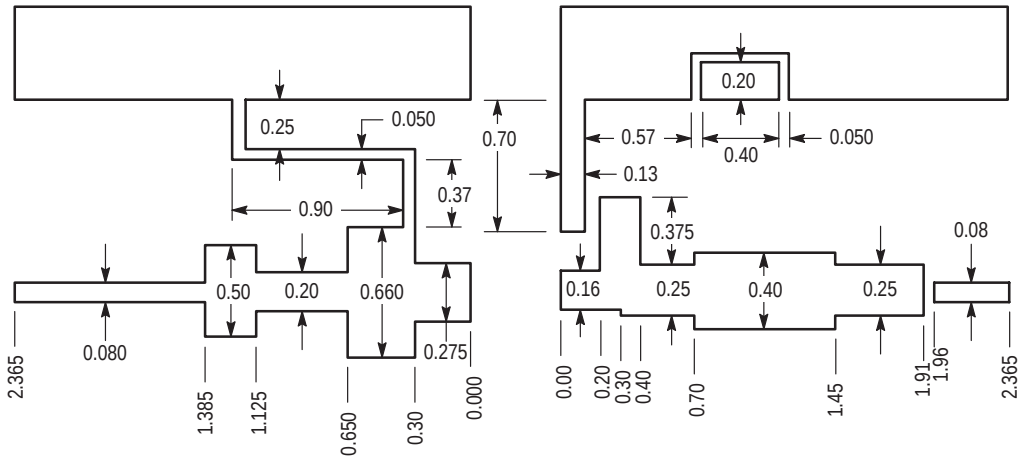


Figure 1. Test Circuit

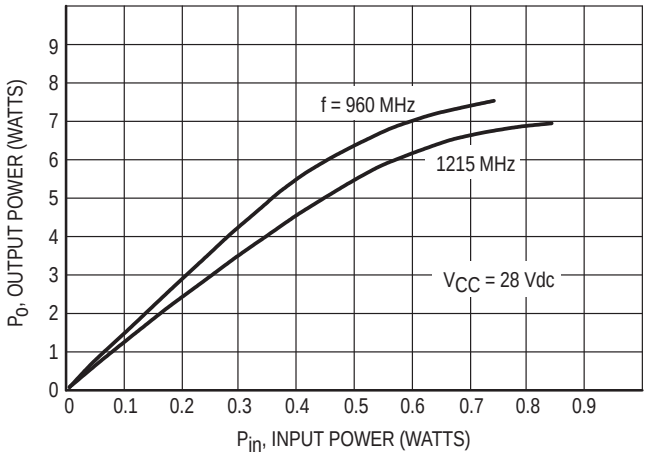


Figure 2. Output Power versus Input Power

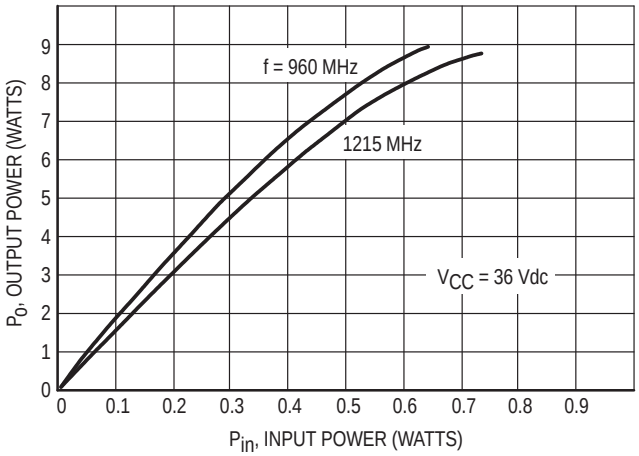
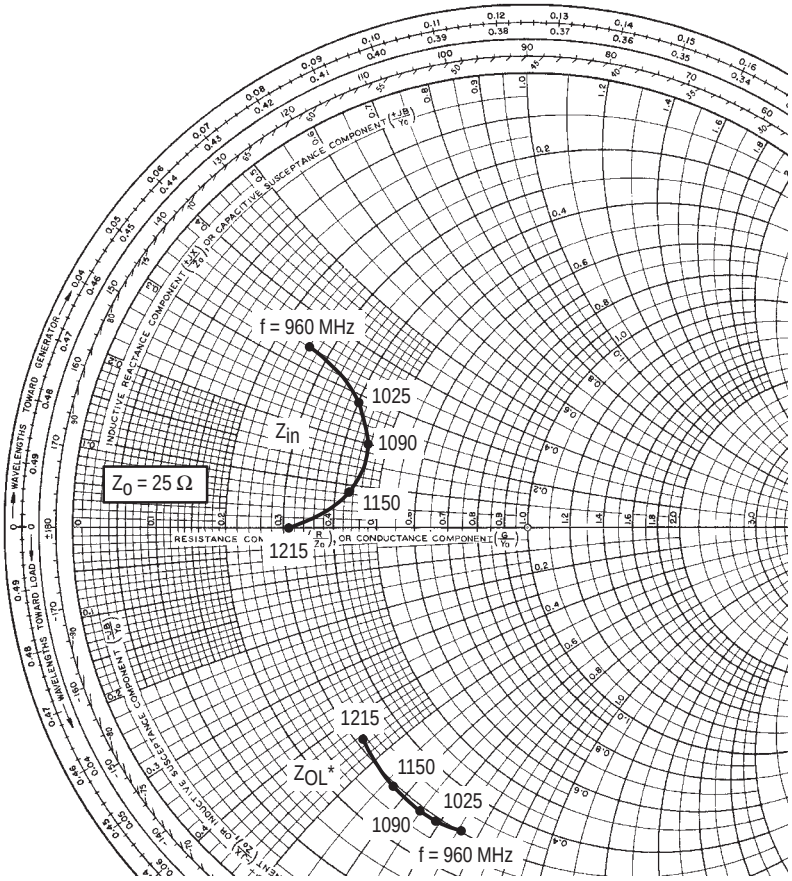


Figure 3. Output Power versus Input Power



P_{out} = 5 W, V_{CC} = 28 V

f MHz	Z_{in} OHMS	Z_{OL}* OHMS
960	6.5 + j8.5	7.4 – j18.9
1025	10.0 + j7.0	7.2 – j17.4
1090	11.2 + j4.9	7.1 – j16.3
1150	10.8 + j2.0	7.15 – j14.3
1215	7.8 + j0.0	7.8 – j11.2

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 4. Series Equivalent Input/Output Impedances

The RF Line

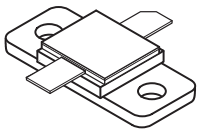
Microwave Long Pulse Power Transistor

MRF10031

Designed for 960–1215 MHz long or short pulse common base amplifier applications such as JTIDS and Mode–S transmitters.

- Guaranteed Performance @ 960 MHz, 36 Vdc
  Output Power = 30 Watts Peak
  Minimum Gain = 9.0 dB Min (9.5 dB Typ)
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Industry Standard Package
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input Matching for Broadband Operation

30 W (PEAK)
960 – 1215 MHz
MICROWAVE POWER
TRANSISTOR
NPN SILICON



CASE 376B–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	55	Vdc
Collector–Base Voltage (1)	V_{CBO}	55	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Continuous (1)	I_C	3.0	Adc
Total Device Dissipation @ T_C = 25°C (1), (2) Derate above 25°C	P_D	110 0.625	Watts mW/°C
Storage Temperature Range	T_{stg}	– 65 to + 200	°C
Junction Temperature	T_J	200	°C

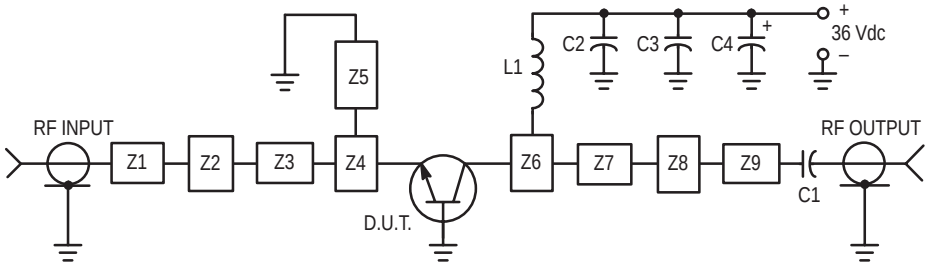
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	1.6	°C/W

NOTES:
1. Under pulse RF operating conditions.
2. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as pulsed RF amplifiers.
3. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques. (Worst case θ_{JC} value measured @ 23% duty cycle)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 25 mAdc, I_E = 0)	$V_{(BR)CBO}$	55	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 36 Vdc, I_E = 0)	I_{CBO}	—	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	—	—
FUNCTIONAL TESTS (10 μs Pulses @ 50% duty cycle for 3.5 ms; overall duty cycle – 25%)					
Common–Base Amplifier Power Gain (V_{CC} = 36 Vdc, P_{out} = 30 W Peak, f = 960 MHz)	G_{PB}	9.0	9.5	—	dB
Collector Efficiency (V_{CC} = 36 Vdc, P_{out} = 30 W Peak, f = 960 MHz)	η	40	45	—	%
Load Mismatch (V_{CC} = 36 Vdc, P_{out} = 30 W Peak, f = 960 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1 — 75 pF 100 Mil Chip Capacitor
C2 — 39 pF 100 Mil Chip Capacitor
C3 — 0.1 μF
C4 — 1000 μF, 50 Vdc, Electrolytic
L1 — 3 Turns #18 AWG, 1/8″ ID, 0.18 Long

Z1–Z9 — Microstrip, See Details
Board Material — Teflon, Glass Laminate
Dielectric Thickness = 0.030″
ε_r = 2.55, 2 Oz. Copper

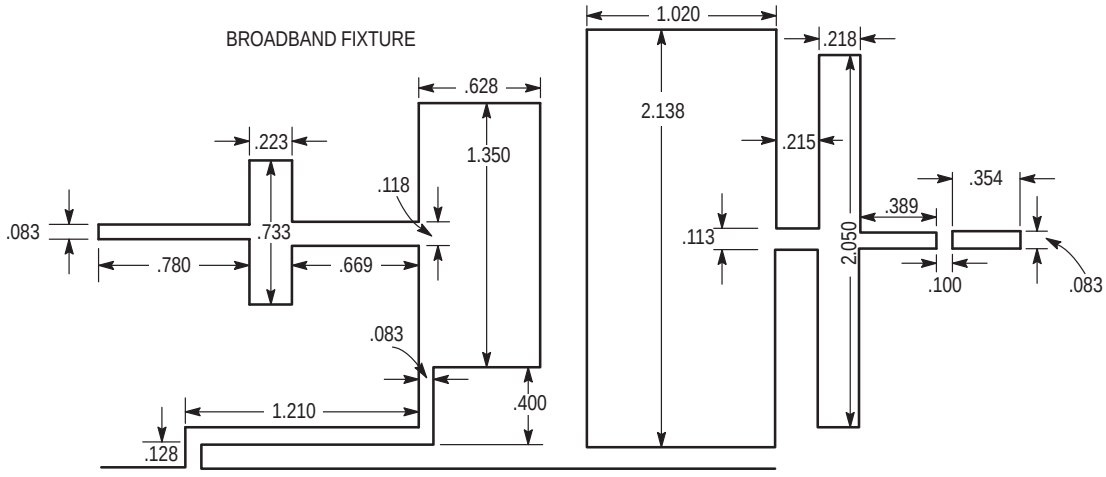


Figure 1. Test Circuit

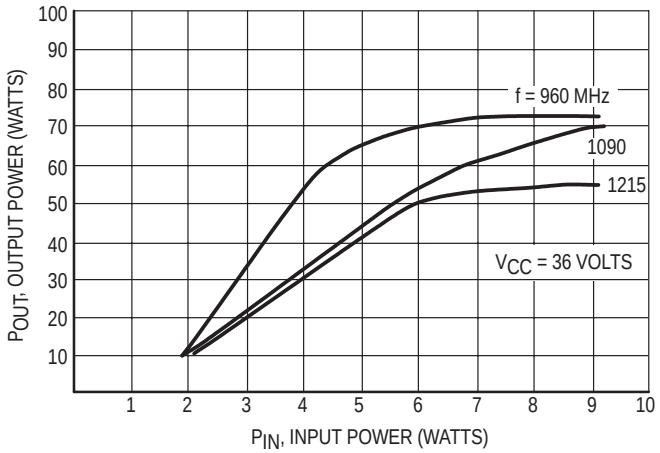
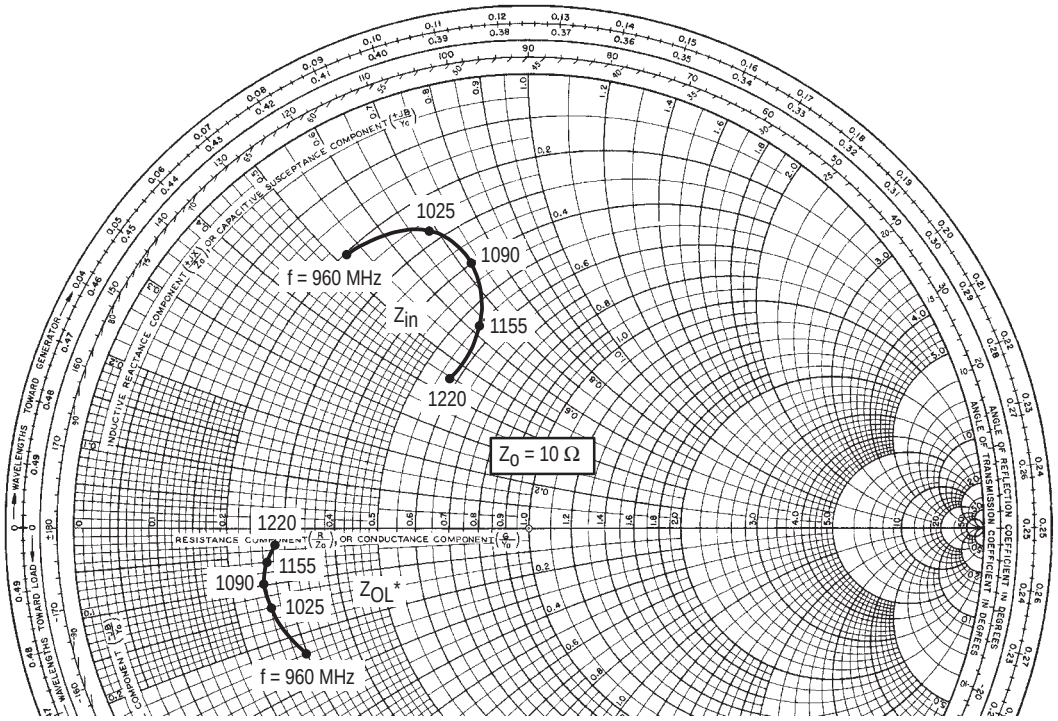


Figure 2. Output Power versus Input Power



P_{out} = 30 W Pk V_{CC} = 36 V

f MHz	Zin Ohms	Z_{OL}* Ohms
960	2.05 + j5.2	2.9 – j2.35
1025	2.67 + j6.34	2.55 – j1.3
1090	4.0 + j7.1	2.52 – j0.9
1155	5.5 + j6.2	2.6 – j0.6
1220	5.7 + j4.3	2.8 – j0.3

Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

Figure 3. Series Equivalent Input/Output Impedances

The RF Line

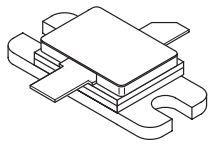
Microwave Long Pulse Power Transistor

MRF10120

Designed for 960–1215 MHz long pulse common base amplifier applications such as JTIDS and Mode S transmitters.

- Guaranteed Performance @ 1.215 GHz, 36 Vdc
  Output Power = 120 Watts Peak
  Gain = 8.0 dB Min., 9.2 dB (Typ)
- 100% Tested for Load Mismatch at All Phase Angles with 3:1 VSWR
- Hermetically Sealed Industry Standard Package
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input and Output Matching for Broadband Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

120 W (PEAK), 960–1215 MHz
MICROWAVE POWER
TRANSISTOR
NPN SILICON



CASE 355C–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	55	Vdc
Collector–Base Voltage	V_{CBO}	55	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Peak (1)	I_C	15	Adc
Total Device Dissipation @ T_C = 25°C (1), (2) Derate above 25°C	P_D	380 2.17	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Junction Temperature	T_J	200	

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	0.46	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

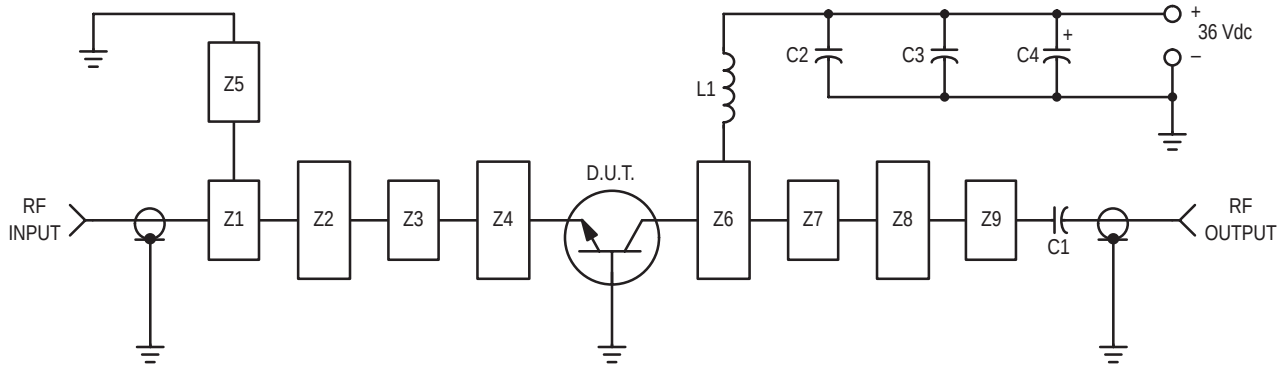
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 60 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 60 mAdc, I_E = 0)	$V_{(BR)CBO}$	55	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 36 Vdc, I_E = 0)	I_{CBO}	—	—	25	mAdc

NOTES: (continued)

1. Under pulse RF operating conditions.
2. These devices are designed for RF operation. The total device dissipation rating applies only when the device is operated as RF amplifiers.
3. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	—	—
FUNCTIONAL TESTS (7.0 μs Pulses @ 54% duty cycle for 3.4 ms; then off for 4.5 ms; overall duty cycle = 23%)					
Common–Base Amplifier Power Gain (V_{CC} = 36 Vdc, P_{out} = 120 W Peak, f = 1215 MHz)	G_{PB}	8.0	9.2	—	dB
Collector Efficiency (V_{CC} = 36 Vdc, P_{out} = 120 W Peak, f = 1215 MHz)	η	50	55	—	%
Load Mismatch (V_{CC} = 36 Vdc, P_{out} = 120 W Peak, f = 1215 MHz, VSWR = 3:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1 — 270 pF 100 Mil Chip Capacitor
C2 — 220 pF 100 Mil Chip Capacitor
C3 — 0.1 μF
C4 — 47 μF 50 V Electrolytic
L1 — 3 Turns #18 AWG, 1/8″ ID, 0.18 Long

Z1–Z9 — Microstrip, See Details
Board Material — Teflon®/Glass Laminate,
Dielectric Thickness = 0.030″,
ε_r = 2.55, 2 Oz. Copper

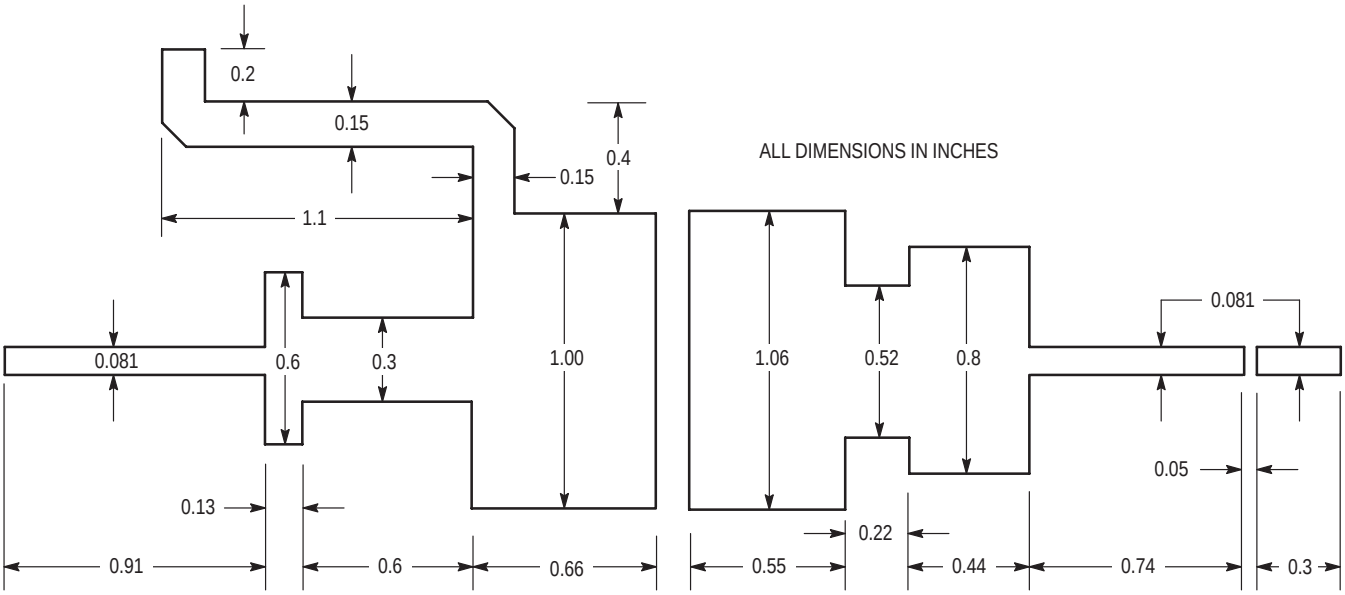


Figure 1. Test Circuit

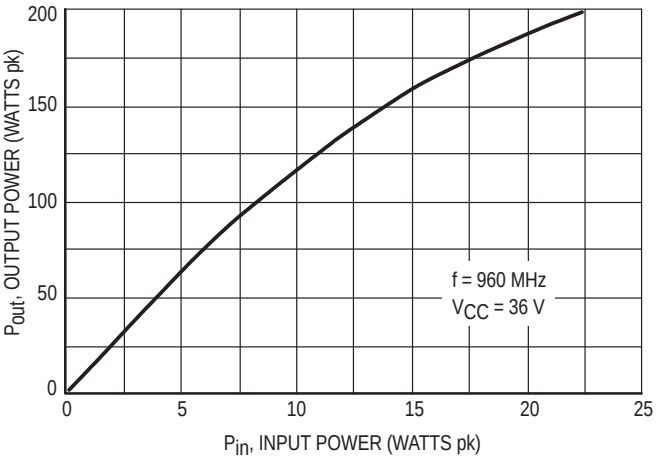


Figure 2. Output Power versus Input Power

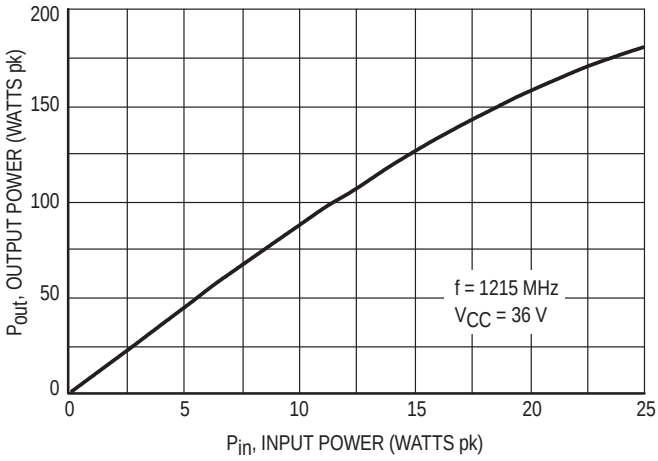
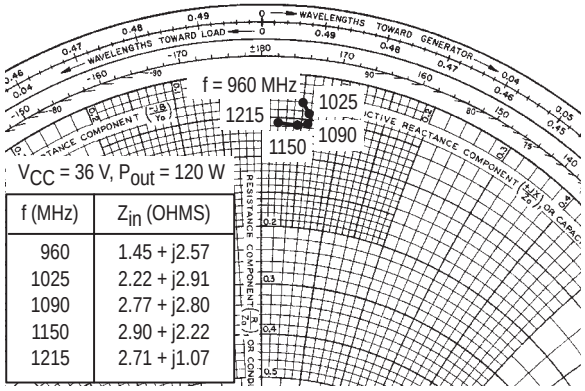
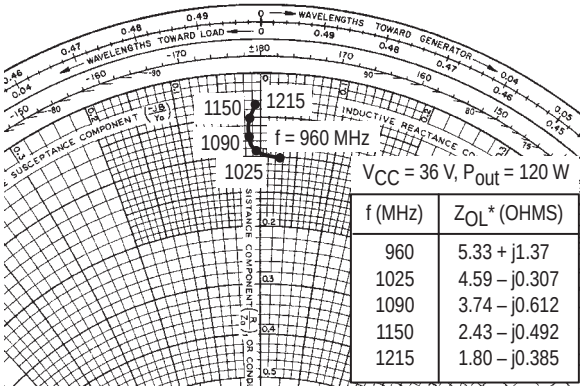


Figure 3. Output Power versus Input Power



f (MHz)	Z_{in} (OHMS)
960	1.45 + j2.57
1025	2.22 + j2.91
1090	2.77 + j2.80
1150	2.90 + j2.22
1215	2.71 + j1.07

Figure 4. Series Equivalent Input Impedances



f (MHz)	Z_{OL}* (OHMS)
960	5.33 + j1.37
1025	4.59 – j0.307
1090	3.74 – j0.612
1150	2.43 – j0.492
1215	1.80 – j0.385

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 5. Series Equivalent Output Impedance

The RF Line

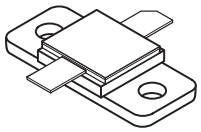
Microwave Pulse Power Transistor

. . . designed for 1025–1150 MHz pulse common base amplifier applications such as TCAS, TACAN and Mode–S transmitters.

- Guaranteed Performance @ 1090 MHz
  Output Power = 150 Watts Peak
  Gain = 9.5 dB Min, 10.0 dB (Typ)
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Package
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input and Output Matching
- Characterized with 10 μs, 10% Duty Cycle Pulses
- Recommended Driver for a Pair of MRF10500 Transistors

MRF10150

150 W (PEAK)
1025–1150 MHz
MICROWAVE POWER
TRANSISTOR
NPN SILICON



CASE 376B–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	65	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Peak (1)	I_C	14	Adc
Total Device Dissipation @ T_C = 25°C (1), (2) Derate above 25°C	P_D	700 4.0	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Junction Temperature	T_J	200	°C

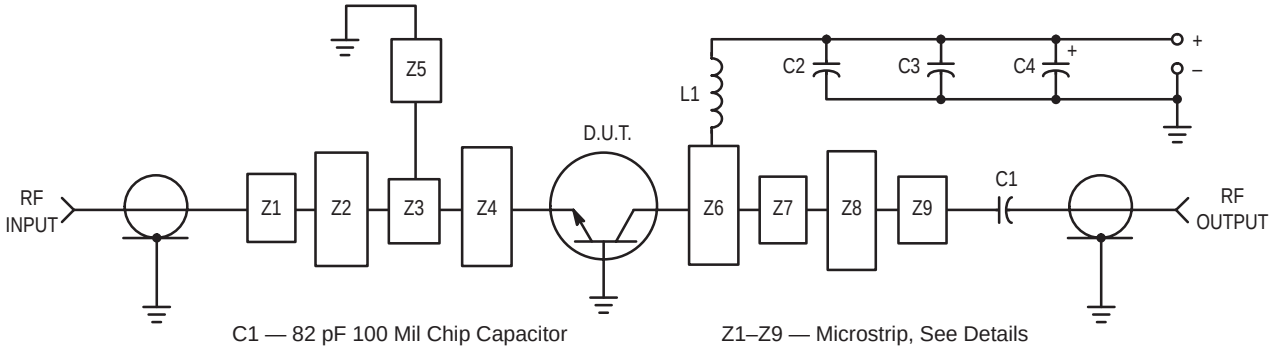
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	0.25	°C/W

NOTES:
1. Under pulse RF operating conditions.
2. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as pulsed RF amplifiers.
3. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques. (Worst case θ_{JC} value measured @ 10 μs, 10%.)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 60 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 60 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 36 Vdc, I_E = 0)	I_{CBO}	—	—	25	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	—	—
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 150 W Peak, f = 1090 MHz)	G_{PB}	9.5	10	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 150 W Peak, f = 1090 MHz)	η	40	—	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 150 W Peak, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1 — 82 pF 100 Mil Chip Capacitor
C2 — 39 pF 100 Mil Chip Capacitor
C3 — 0.1 μF
C4 — 100 μF, 100 Vdc, Electrolytic
L1 — 3 Turns #18 AWG, 1/8″ ID, 0.18 Long

Z1–Z9 — Microstrip, See Details
Board Material — Teflon Glass Laminate
Dielectric Thickness = 0.030″
ε_r = 2.55, 2 Oz. Copper

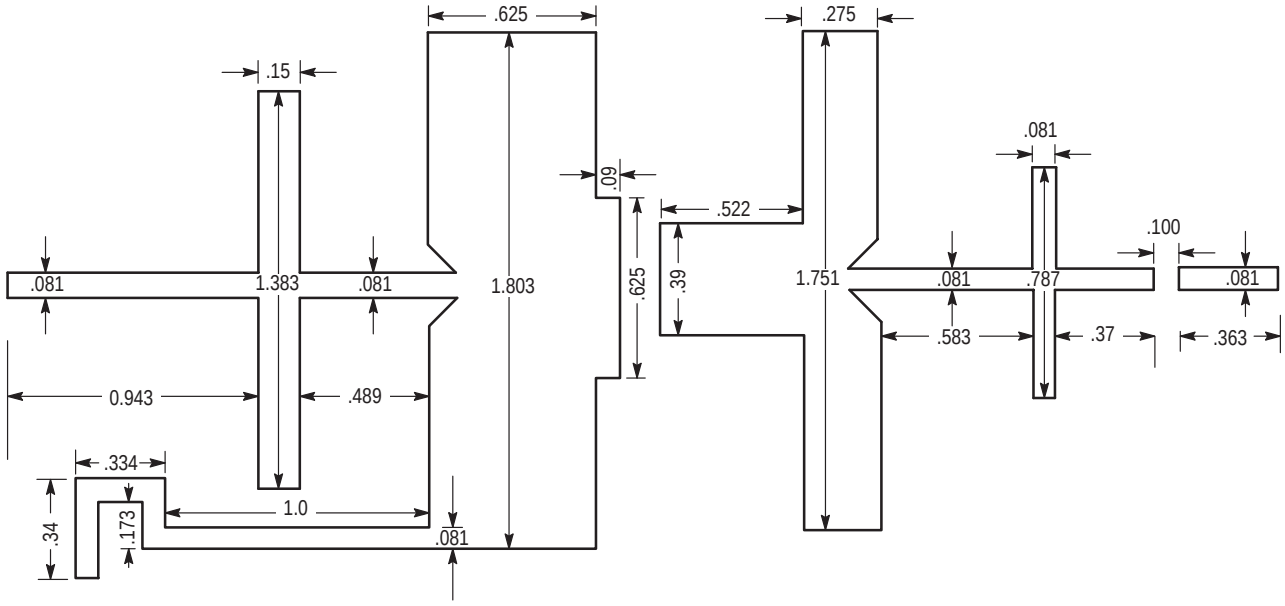


Figure 1. Test Circuit

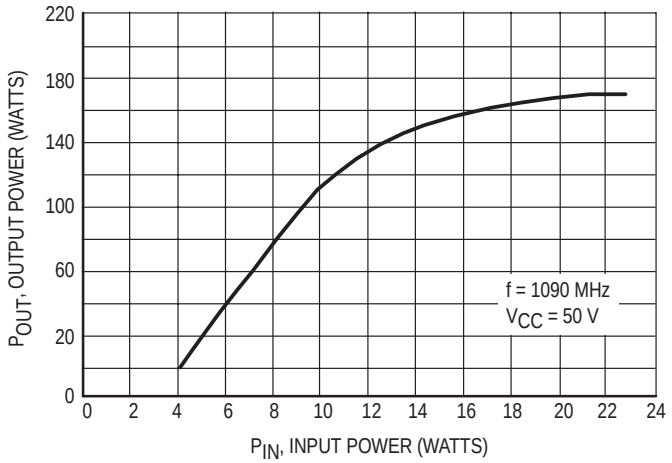
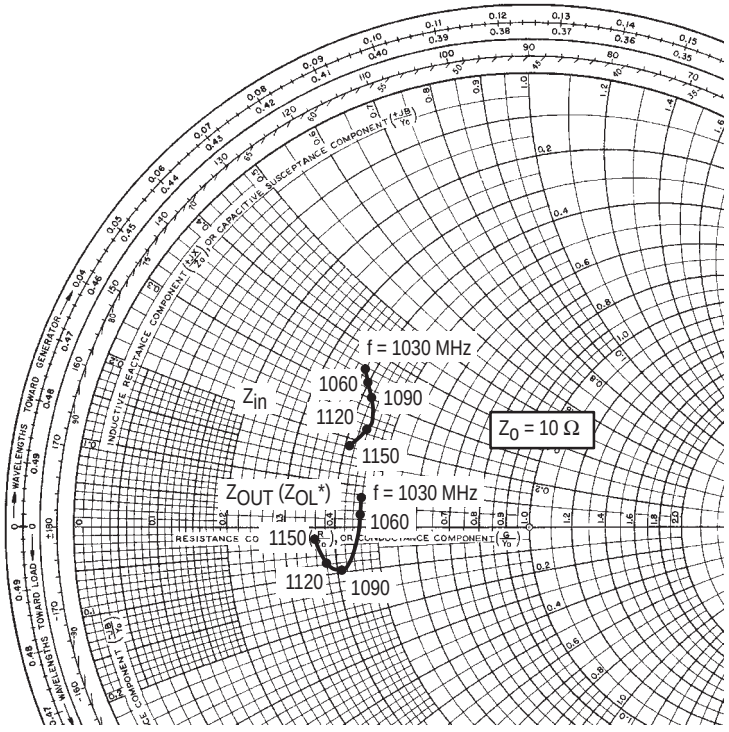


Figure 2. Output Power versus Input Power



P_{OUT} = 150 W Pk V_{CC} = 50 V

f MHz	Z_{in} OHMS	Z_{OL}* (Z_{OUT}) OHMS
1030	3.8 + j3.5	4.6 + j0.7
1060	4.0 + j3.3	4.6 + j0.3
1090	4.2 + j3.0	4.1 – j1.0
1120	4.4 + j2.3	3.8 – j0.8
1150	4.1 + j1.8	3.6 – j0.3

Z_{OL}* is the conjugate of the optimum load impedance into which the device operates at a given output power voltage and frequency.

Figure 3. Series Equivalent Input/Output Impedances

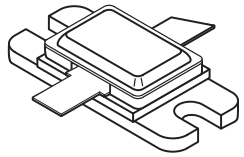
The RF Line
Microwave Pulse Power Transistor

MRF10350

Designed for 1025–1150 MHz pulse common base amplifier applications such as TCAS, TACAN and Mode–S transmitters.

- Guaranteed Performance @ 1090 MHz
  Output Power = 350 Watts Peak
  Gain = 8.5 dB Min, 9.0 dB (Typ)
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Package
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input and Output Matching
- Characterized using Mode–S Pulse Format

350 W (PEAK)
1025–1150 MHz
MICROWAVE POWER TRANSISTOR
NPN SILICON



CASE 355E–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	65	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Peak (1)	I_C	31	Adc
Total Device Dissipation @ T_C = 25°C (1), (2) Derate above 25°C	P_D	1590 9.1	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Junction Temperature	T_J	200	°C

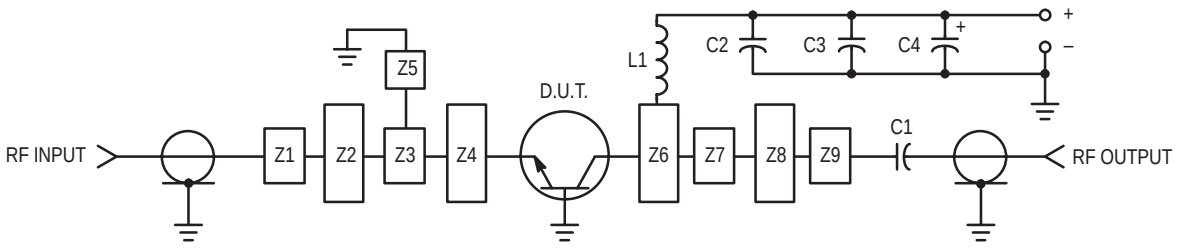
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	0.11	°C/W

NOTES:
1. Under pulse RF operating conditions.
2. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as pulsed RF amplifiers.
3. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques. (Worst Case θ_{JC} measured using Mode–S pulse train, 128 μs burst 0.5 μs on, 0.5 μs off repeating at 6.4 ms interval.)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 60 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 60 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 36 Vdc, I_E = 0)	I_{CBO}	—	—	25	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	—	—
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 350 W Peak, f = 1090 MHz)	G_{PB}	8.5	9.0	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 350 W Peak, f = 1090 MHz)	η	40	—	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 350 W Peak, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1 — 75 pF 100 Mil Chip Capacitor
C2 — 39 pF 100 Mil Chip Capacitor
C3 — 0.1 μF
C4 — 100 μF, 100 Vdc, Electrolytic
L1 — 3 Turns #18 AWG, 1/8″ ID, 0.18 Long

Z1–Z9 — Microstrip, See Details
Board Material — Teflon, Glass Laminate
Dielectric Thickness = 0.030″
ε_r = 2.55, 2 Oz. Copper

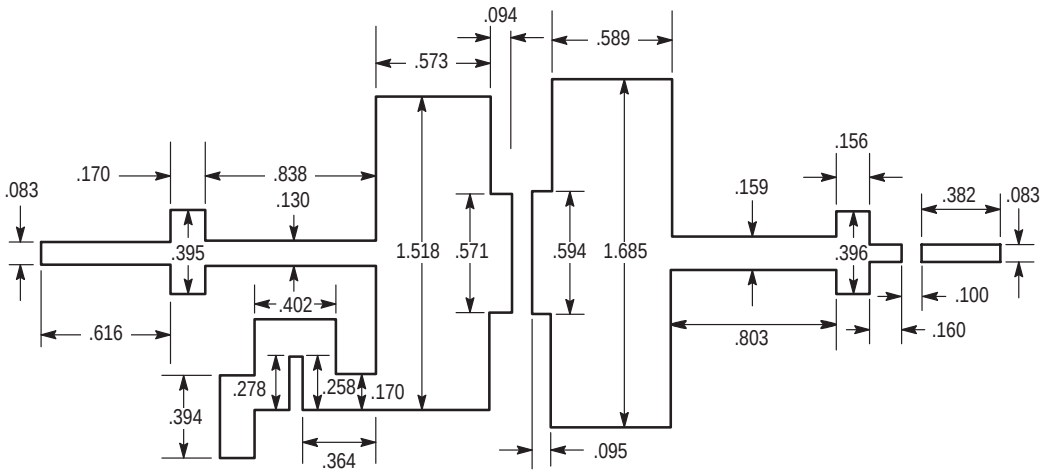
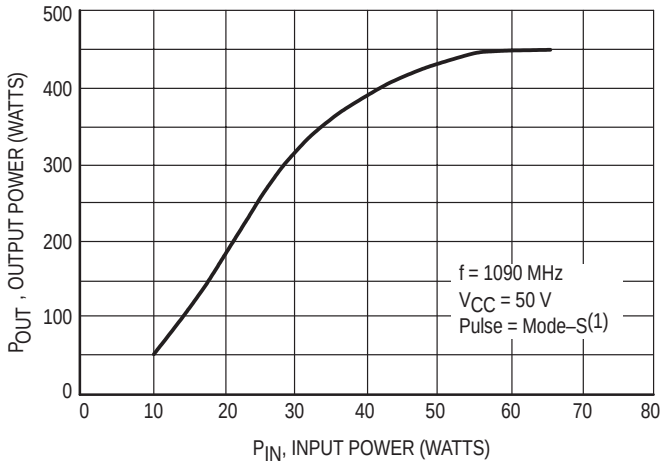
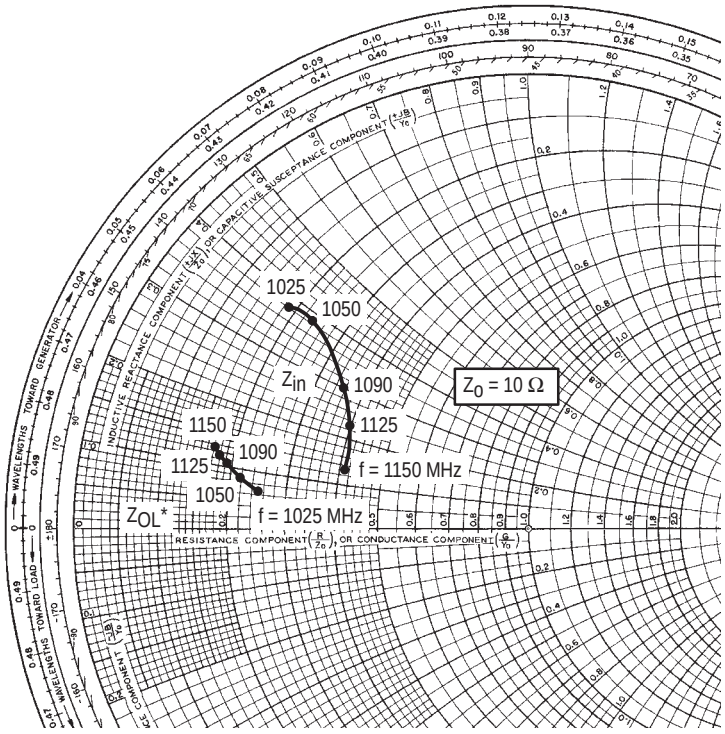


Figure 1. Test Circuit



(1) 128 μs burst 0.5 μs on, 0.5 μs off repeating at 6.4 ms interval.

Figure 2. Output Power versus Input Power



P_{OUT} = 350 W Pk V_{CC} = 50 V

f MHz	Z_{in} OHMS	Z_{OL}* (1) OHMS
1025	1.92 + j3.80	2.52 + j0.70
1050	2.44 + j3.92	2.18 + j0.85
1090	3.55 + j3.02	1.94 + j1.13
1125	4.11 + j2.27	1.80 + j1.22
1150	4.13 + j1.35	1.71 + j1.31

Z_{OL}* is the conjugate of the optimum load impedance into which the device operates at a given output power voltage and frequency.

Figure 3. Series Equivalent Input/Output Impedances

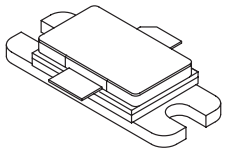
The RF Line
Microwave Pulse Power Transistor

MRF10502

500 W (PEAK)
1025–1150 MHz
MICROWAVE POWER
TRANSISTOR
NPN SILICON

Designed for 1025–1150 MHz pulse common base amplifier applications such as TCAS, TACAN and Mode–S transmitters.

- Guaranteed Performance @ 1090 MHz
  Output Power = 500 Watts Peak
  Gain = 8.5 dB Min, 9.0 dB (Typ)
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Industry Package
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input and Output Matching
- Characterized with 10 μs, 1% Duty Cycle Pulses



CASE 355J–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	65	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Peak (1)	I_C	29	Adc
Total Device Dissipation @ T_C = 25°C (1), (2) Derate above 25°C	P_D	1460 8.3	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Junction Temperature	T_J	200	°C

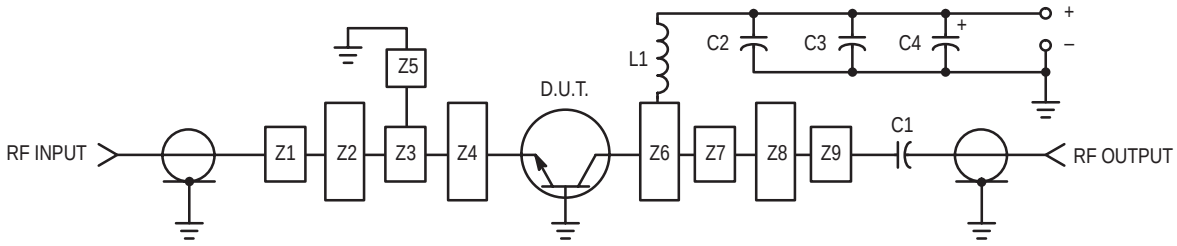
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	0.12	°C/W

NOTES:
1. Under pulse RF operating conditions.
2. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as pulsed RF amplifiers.
3. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques. (Worst case θ_{JC} value measured @ 32 μs, 2%.)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 60 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 60 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 36 Vdc, I_E = 0)	I_{CBO}	—	—	25	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	—	—
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 500 W Peak, f = 1090 MHz)	G_{PB}	8.5	9.0	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 500 W Peak, f = 1090 MHz)	η	40	45	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 500 W Peak, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1 — 82 pF 100 Mil Chip Capacitor
C2 — 39 pF 100 Mil Chip Capacitor
C3 — 0.1 μF
C4 — 100 μF, 100 Vdc, Electrolytic
L1 — 3 Turns #18 AWG, 1/8″ ID, 0.18 Long

Z1–Z9 — Microstrip, See Details
Board Material — Teflon, Glass Laminate
Dielectric Thickness = 0.030″
ε_r = 2.55, 2 Oz. Copper

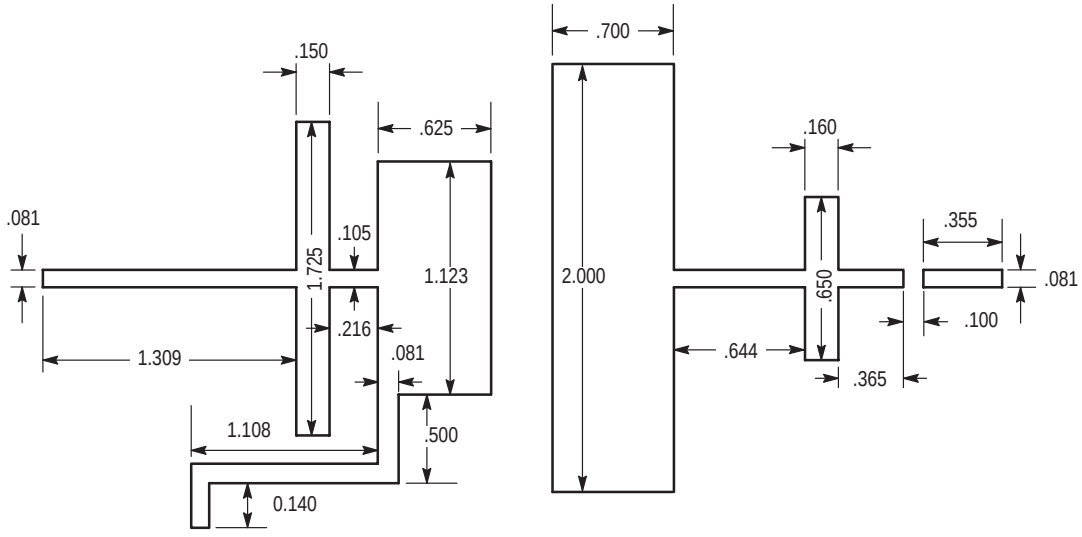


Figure 1. Test Circuit

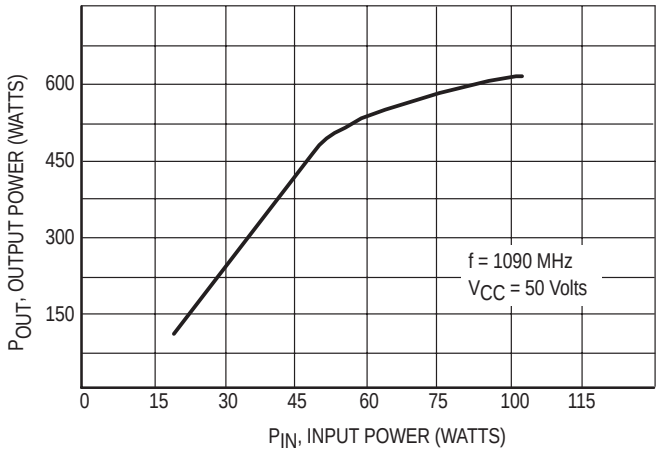
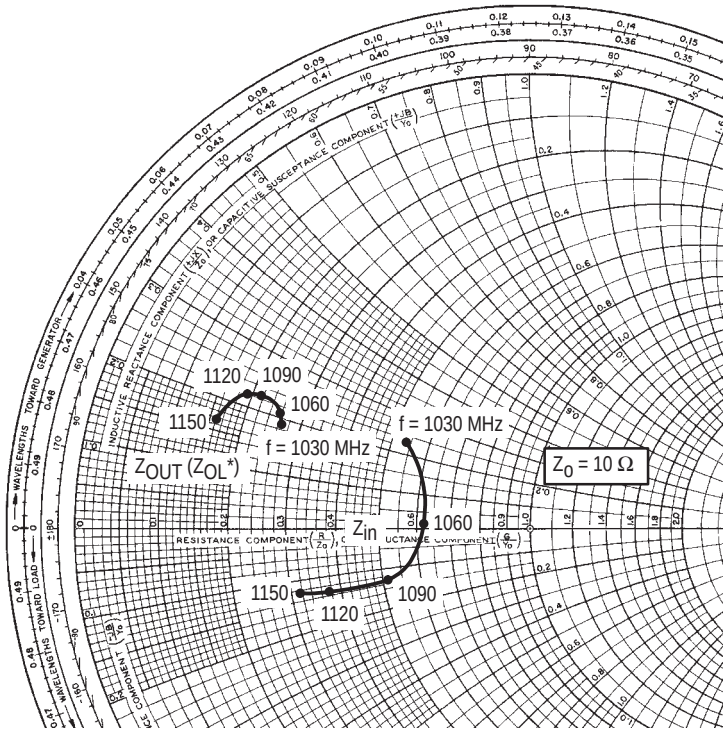


Figure 2. Output Power versus Input Power



P_{OUT} = 500 W Pk V_{CC} = 50 V

f MHz	Z_{in} OHMS	Z_{OL}* (Z_{OUT}) OHMS
1030	5.3 + j2.25	2.6 + j1.89
1060	6.2 + j0.2	2.56 + j2.0
1090	5.2 – j1.4	2.12 + j2.2
1120	3.7 – j1.35	1.9 + j2.15
1150	3.15 – j1.3	1.6 + j1.62

Z_{OL}* is the conjugate of the optimum load impedance into which the device operates at a given output power voltage and frequency.

Figure 3. Series Equivalent Input/Output Impedances

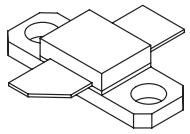
The RF Line
NPN Silicon
RF Power Transistor

MRF16006

6.0 WATTS, 1.6 GHz
RF POWER TRANSISTOR
NPN SILICON

Designed for 28 Volt microwave large–signal, common base, Class–C CW amplifier applications in the range 1600 – 1640 MHz.

- Specified 28 Volt, 1.6 GHz Class–C Characteristics
  Output Power = 6 Watts
  Minimum Gain = 7.4 dB, @ 6 Watts
  Minimum Efficiency = 40% @ 6 Watts
- Characterized with Series Equivalent Large–Signal Parameters from 1500 MHz to 1700 MHz
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



CASE 395C–01, STYLE 2

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector–Current	I_C	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	26 0.15	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

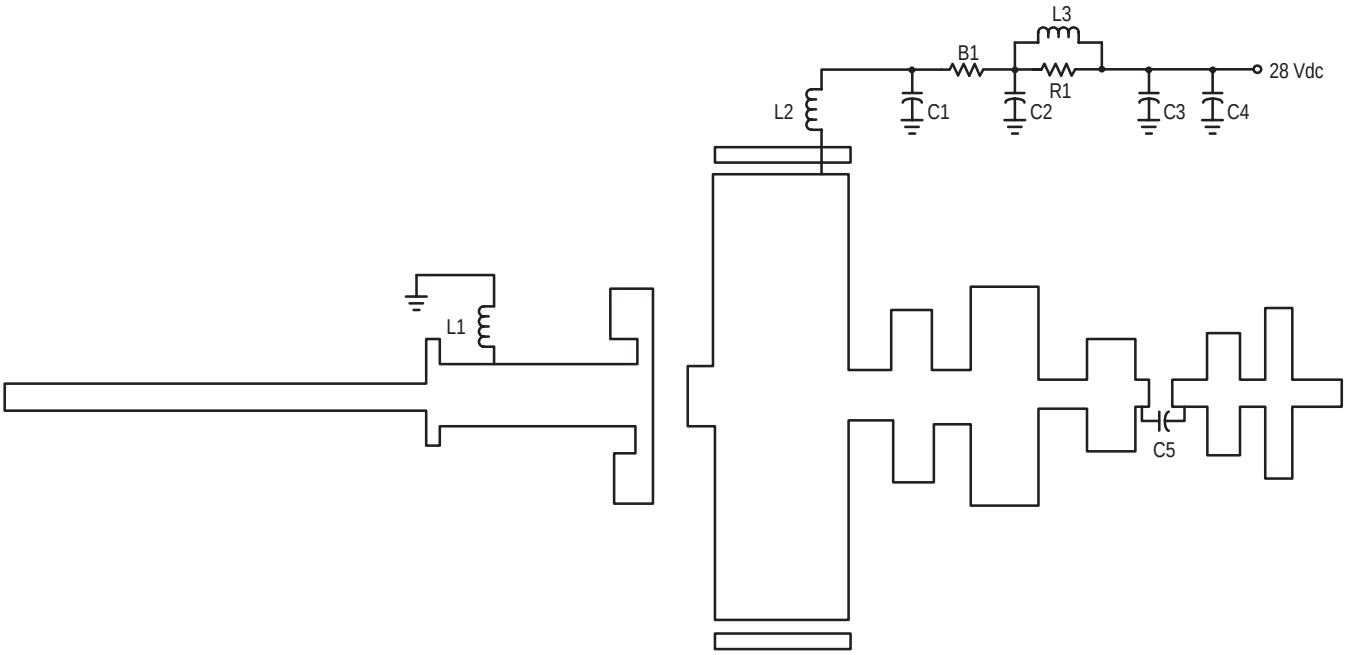
THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case (1) (2)	$R_{\theta JC}$	6.8	°C/W

(1) Thermal measurement performed using CW RF operating condition.
(2) Thermal resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

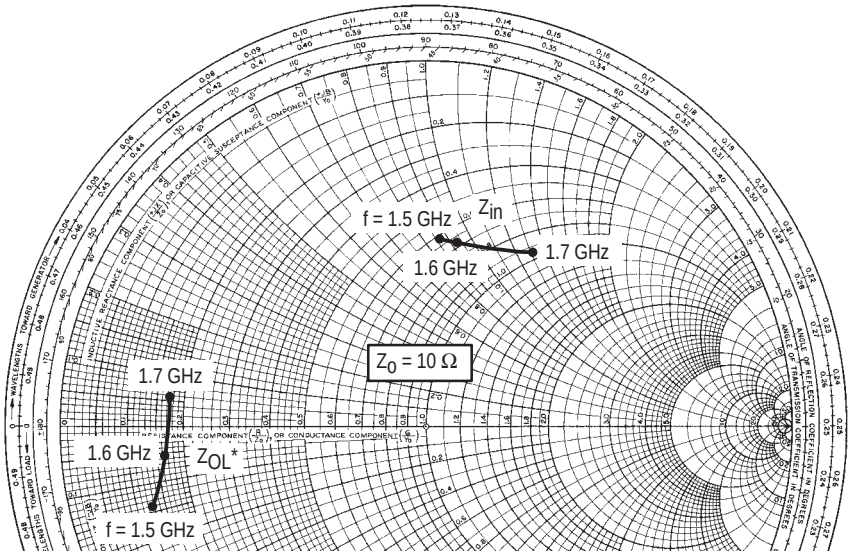
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 40 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 40 mAdc, I_E = 0)	$V_{(BR)CBO}$	55	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 2.5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (VCE = 28 Vdc, V_{BE} = 0)	I_{CES}	—	—	2.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 0.2 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB}= 28 Vdc, f = 1.0 MHz)	C_{ob}	11	—	—	pf
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 6 Watts, f = 1600/1640 MHz)	G_{pe}	7.4	—	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 6 Watts, f = 1600/1640 MHz)	η	40	45	—	%
Return Loss (V_{CC} = 28 Vdc, P_{out} = 6 Watts, f = 1600/1640 MHz)	I_{RL}	—	8.0	—	dB
Output Mismatch Stress (V_{CC} = 28 Vdc, P_{out} = 6 Watts, f = 1600 MHz, Load VSWR = 3:1 all phase angles at frequency of test)	ψ	No Degradation in Output Power			



Board Material – Teflon® Glass Laminate Dielectric
Thickness – 0.30″, ε_r = 2.55″, 2.0 oz. Copper

B1	Fair Rite Bead on #24 Wire	C4	47 µF, 50 V, Electrolytic Cap
C1, C5	100 pF, B Case, ATC Chip Cap	L1, L2	3 Turns, #18, 0.133″ ID, 0.15″ Long
C2	0.1 µF, Dipped Mica Cap	L3	9 Turns, #24 Enamel
C3	0.1 µF, Chip Cap	R1	82 Ω, 1.0 W, Carbon Resistor

Figure 1. MRF16006 Test Fixture Schematic



V_{CC} = 28 Vdc, P_{out} = 6 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
1500	6.28 + j 8.53	1.22 – j 1.37
1600	7.04 + j 9.00	1.58 – j 0.53
1700	9.55 + j 12.86	1.71 + j 0.39

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 2. Series Equivalent Input/Output Impedance

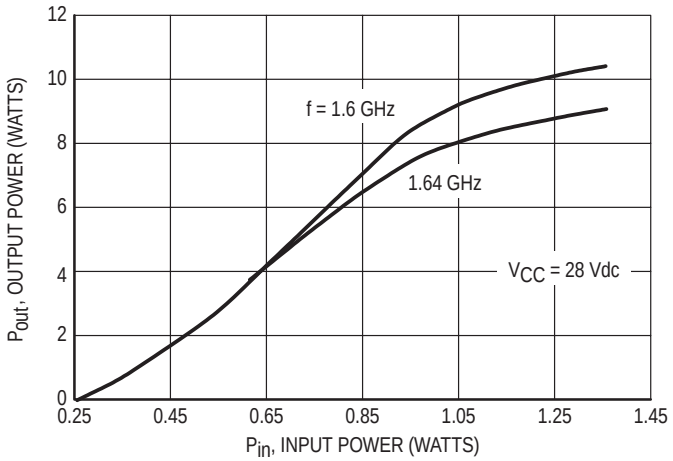


Figure 3. Output Power versus Input Power

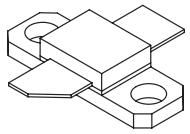
The RF Line
NPN Silicon
RF Power Transistor

MRF16030

30 WATTS, 1.6 GHz
RF POWER TRANSISTOR
NPN SILICON

Designed for 28 Volt microwave large–signal, common base, Class–C CW amplifier applications in the range 1600 – 1640 MHz.

- Specified 28 Volt, 1.6 GHz Class–C Characteristics
  Output Power = 30 Watts
  Minimum Gain = 7.5 dB, @ 30 Watts
  Minimum Efficiency = 40% @ 30 Watts
- Characterized with Series Equivalent Large–Signal Parameters from 1500 MHz to 1700 MHz
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



CASE 395C–01, STYLE 2

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector–Current	I_C	4.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	103 0.58	Watts °C/W
Storage Temperature Range	T_{stg}	–65 to +150	°C

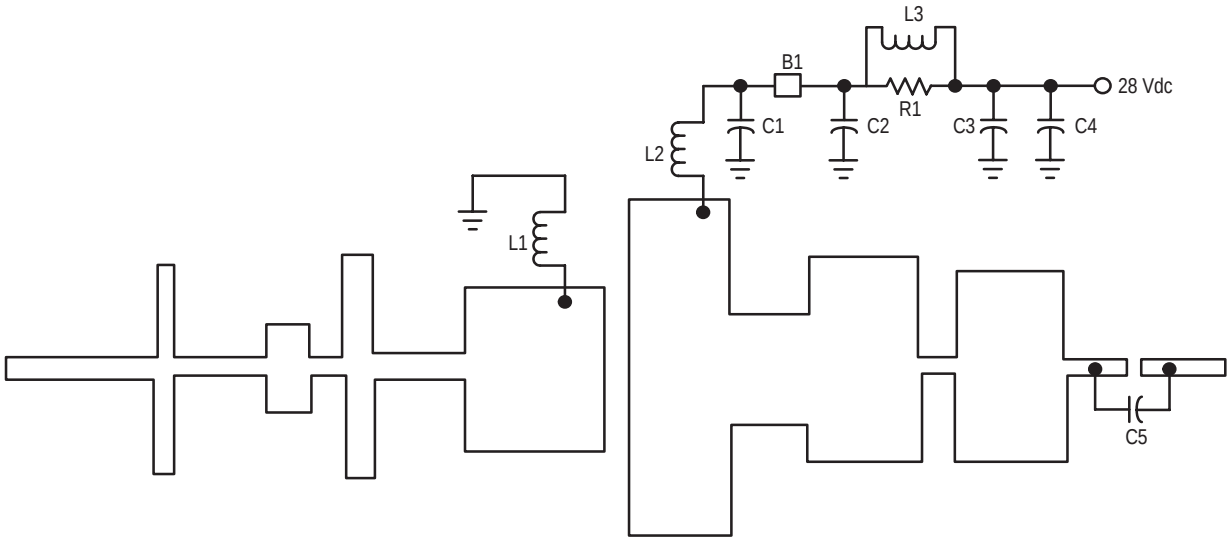
THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case (1) (2)	$R_{\theta JC}$	1.7	°C/W

(1) Thermal measurement performed using CW RF operating condition.
(2) Thermal resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

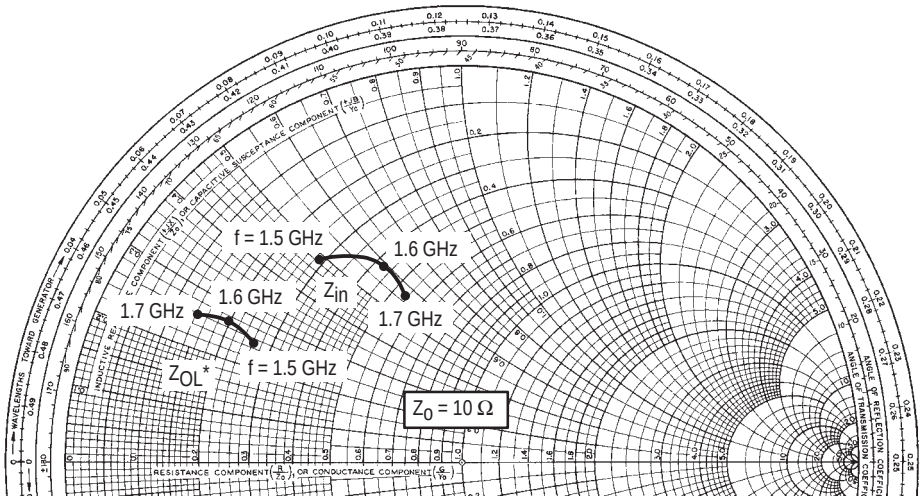
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	55	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, V_{BE} = 0)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	35	80	—
FUNCTIONAL TESTS					
Collector–Base Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 30 Watts, f = 1600/1640 MHz)	G_{pe}	7.5	7.7	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 30 Watts, f = 1600/1640 MHz)	η	40	45	—	%
Input Return Loss (V_{CC} = 28 Vdc, P_{out} = 30 Watts, f = 1600/1640 MHz)	I_{RL}	8.0	—	—	dB
Output Mismatch Stress V_{CC} = 28 Vdc, P_{out} = 30 Watts, f = 1600 MHz, Load VSWR = 3:1, All phase angles at frequency of test	Ψ	No Degradation in Output Power			



Board Material – Teflon® Glass Laminate Dielectric
Thickness = 0.30″, ε_r = 2.55″, 2.0 oz. Copper

B1	Fair Rite Bead on #24 Wire	C4	47 µF, 50 V, Electrolytic
C1, C5	100 pF, B Case, ATC Chip Cap	L1, L2	3 Turns, #18, 0.133″ ID, 0.15″ Long
C2	0.1 µF, Dipped Mica Cap	L3	9 Turns, #24 Enamel
C3	0.1 µF, Chip Cap	R1	82 Ω, 1.0 W, Carbon

Figure 1. MRF16030 Test Fixture Schematic



V_{CC} = 28 Vdc, P_{out} = 30 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
1500	3.05 + j 4.88	2.66 + j 2.53
1600	4.32 + j 6.00	1.79 + j 2.80
1700	5.62 + j 5.79	1.51 + j 2.64

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 2. Series Equivalent Input/Output Impedance

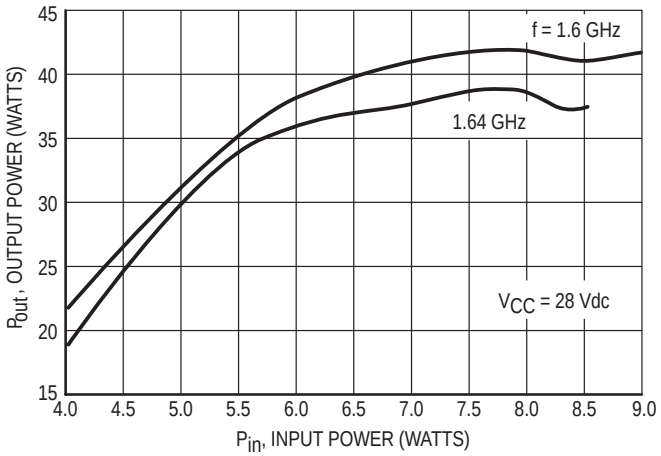


Figure 3. Output Power versus Input Power

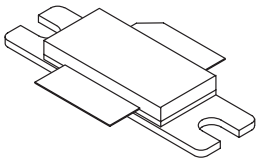
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF18060A
MRF18060AS

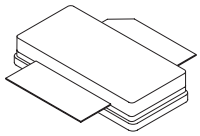
60 W, 1.80 – 1.88 GHz, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

Designed for PCN and PCS base station applications from frequencies up to 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in class AB for PCN–PCS/cellular radio and WLL applications. Specified for GSM1805 – 1880 MHz.

- Typical GSM Performance, Full Frequency Band (1805 – 1880 MHz)
  Power Gain — 13 dB (Typ) @ 60 Watts
  Efficiency — 45% (Typ) @ 60 Watts
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection: Class 2 Human Body Model, Class M3
  Machine Model
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 60 Watts (CW) Output Power
- Excellent Thermal Stability



CASE 465–04, STYLE 1
(MRF18060A)



CASE 465A–04, STYLE 1
(MRF18060AS)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ $T_C \geq 25°C$ Derate above 25°C	P_D	180 1.03	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	°C/W

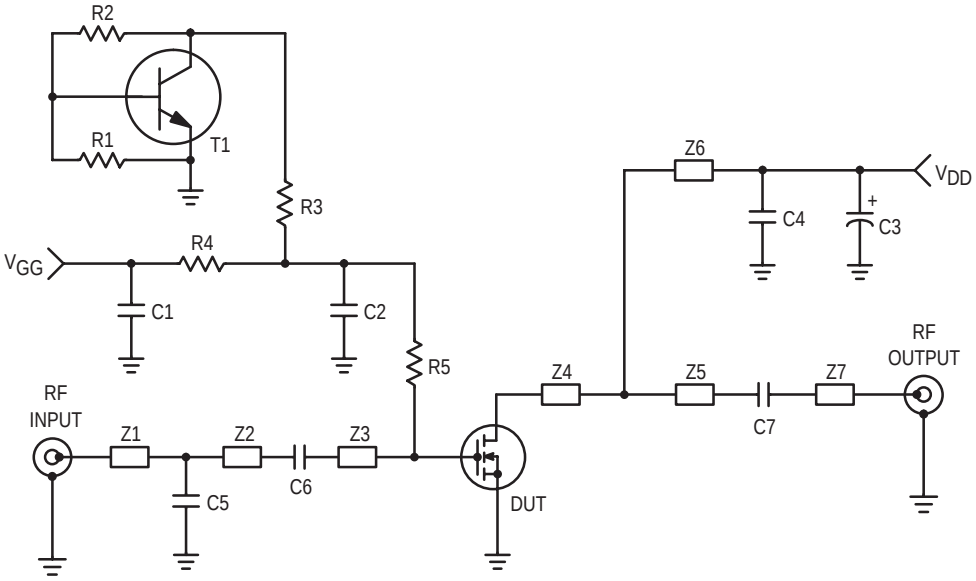
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0)	I_{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.27	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	4.7	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Including Input Matching Capacitor in Package) (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	160	—	pF
Output Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	740	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain @ 60 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 500 mA, f = 1805 – 1880 MHz)	G_{ps}	11.5	13	—	dB
Drain Efficiency @ 60 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 500 mA, f = 1805 – 1880 MHz)	η	43	45	—	%
Input Return Loss (2) (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA, f = 1805 – 1880 MHz)	IRL	10	—	—	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

(2) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1800 band, ensuring batch–to–batch consistency.



C1	100 nF, Chip Capacitor 1203	R1, R3	2.2 kΩ, Chip Resistor 0805
C2, C4, C7	10 pF, Chip Capacitor	R2, R4	2.7 kΩ, Chip Resistor 0805
C3	10 μF, 35 V Electrolytic Tantalum Capacitor	R5	1.1 kΩ, Chip Resistor 0805
C5	1.2 pF, Chip Capacitor	T1	BC847 Transistor SOT–23
C6	1.0 pF, Chip Capacitor	Z1 to Z7	Microstrip Transmission Lines

Figure 1. 1805 – 1880 MHz Test Fixture Schematic

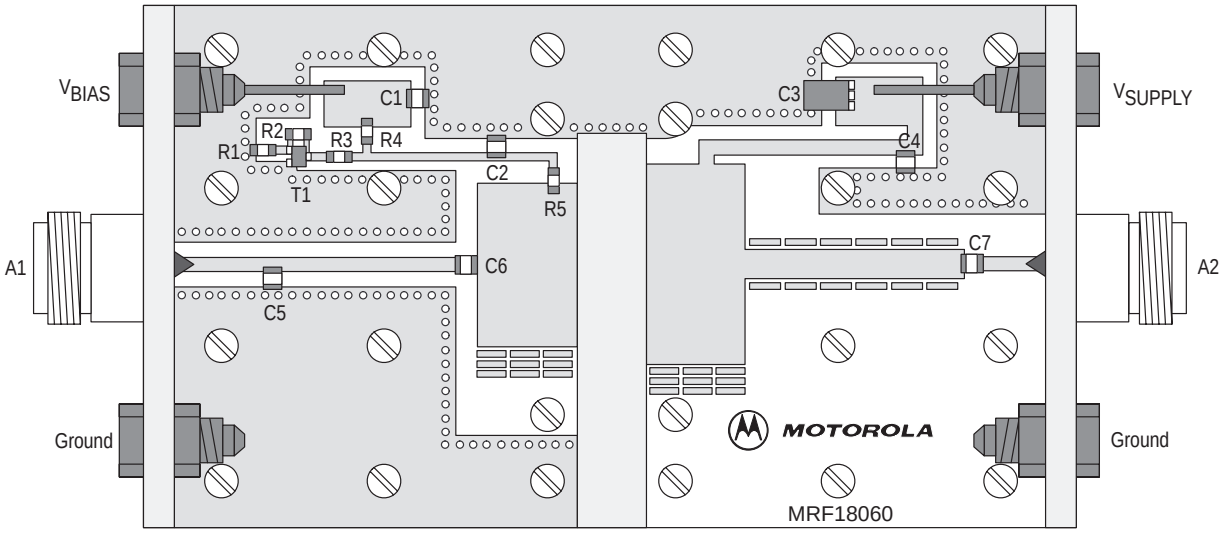
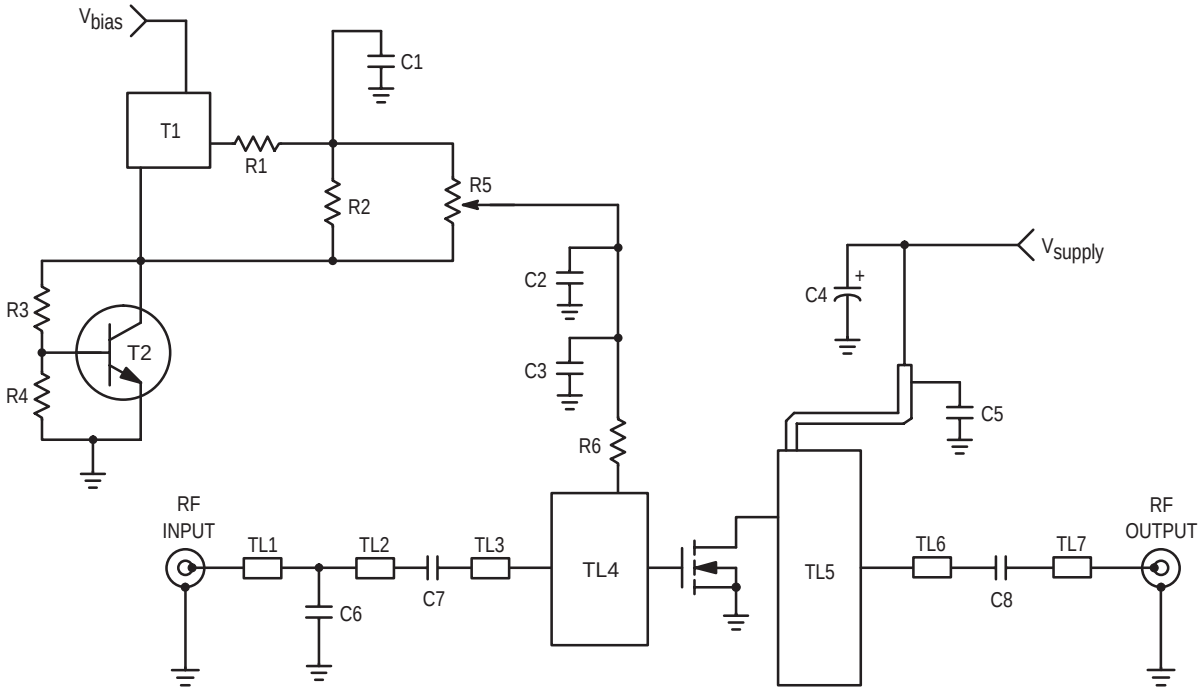


Figure 2. 1805 – 1880 MHz Test Fixture Component Layout



C1	1 μF, Chip Capacitor 0805	R1	10 Ω, Chip Resistor 0805
C2	100 nF, Chip Capacitor 0805	R2, R6	1 kΩ, Chip Resistor 0805
C3, C5, C8	10 pF, ACCU–P Chip Capacitor 0805	R3	1.2 kΩ, Chip Resistor 0805
C4	10 μF, 35 V Tantalum Electrolytic Capacitor	R4	2.2 kΩ, Chip Resistor 0805
C6	1.8 pF, ACCU–P Chip Capacitor 0805	R5	5 kΩ, SMD Potentiometer
C7	1 pF, ACCU–P Chip Capacitor 0805	T1	LP2951 Micro–8 Voltage Regulator
		T2	BC847 SOT–23 NPN Transistor

Substrate = 0.5 mm Teflon® Glass, ε_r = 2.55

Figure 3. 1800 – 2000 MHz Demo Board Schematic

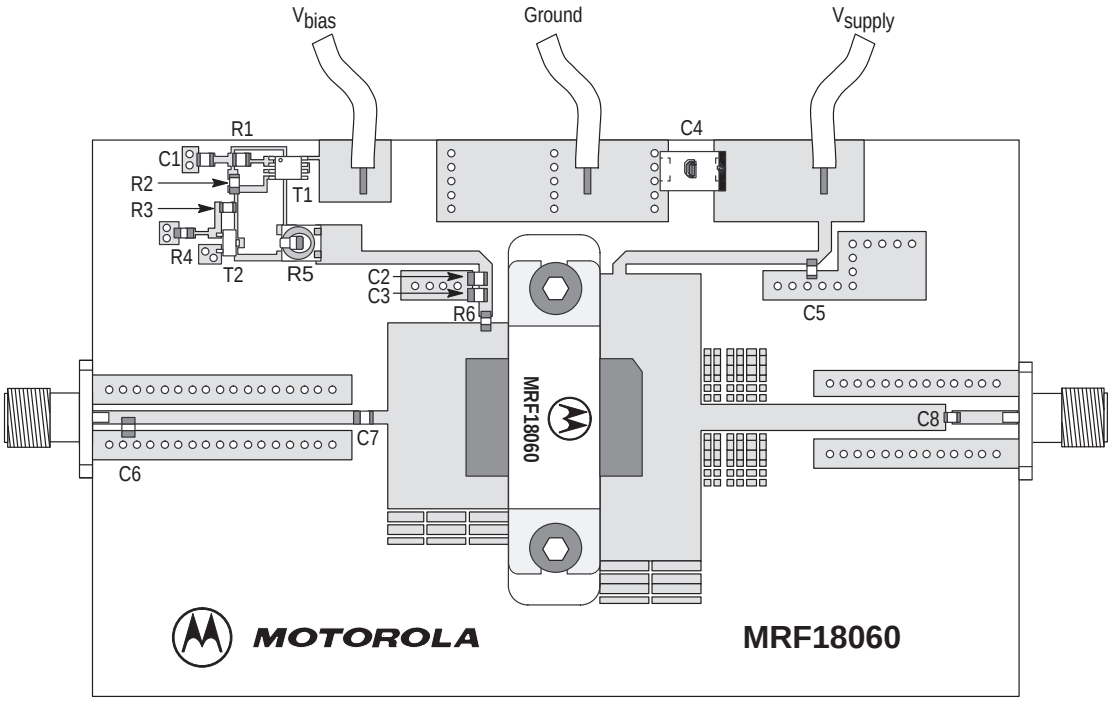


Figure 4. 1800 – 2000 MHz Demo Board Component Layout

V_{DD} = 26 V, I_{DQ} = 500 mA, P_{out} = 60 Watts (CW)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1700	0.60 + j2.53	2.27 + j3.44
1800	0.80 + j3.20	2.05 + j3.05
1900	0.92 + j3.42	1.90 + j2.90
2000	1.07 + j3.59	1.64 + j2.88
2100	1.31 + j4.00	1.29 + j2.99

Z_{in} = Complex conjugate of source impedance.

Z_{OL}*= Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

Table 1. Series Equivalent Input and Output Impedance

TYPICAL CHARACTERISTICS (DATA TAKEN USING WIDEBAND DEMONSTRATION BOARD)

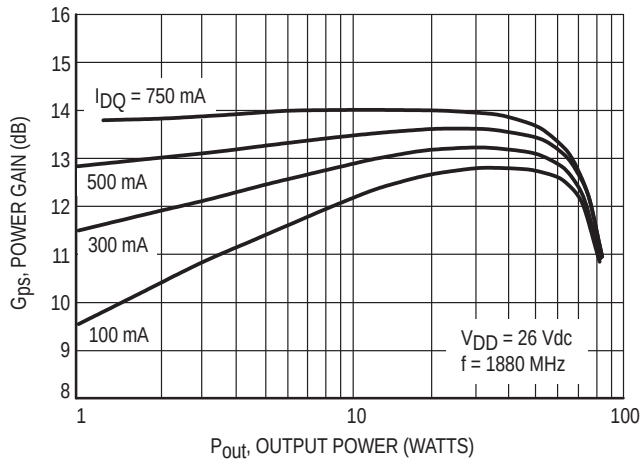


Figure 5. Power Gain versus Output Power

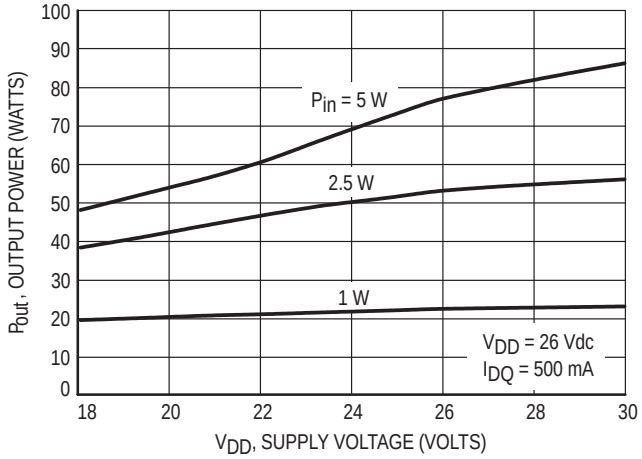


Figure 6. Output Power versus Supply Voltage

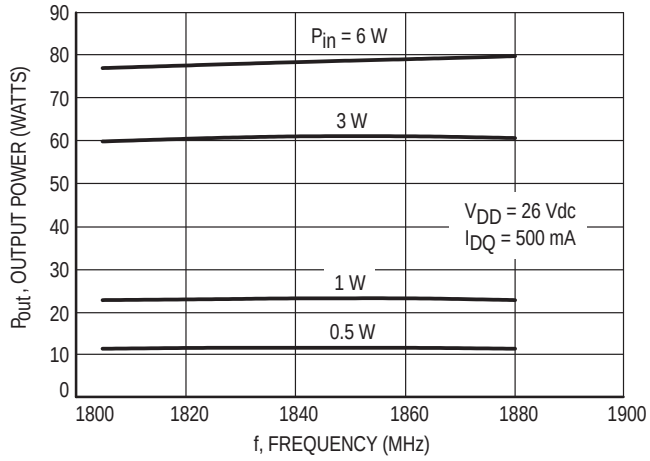


Figure 7. Output Power versus Frequency

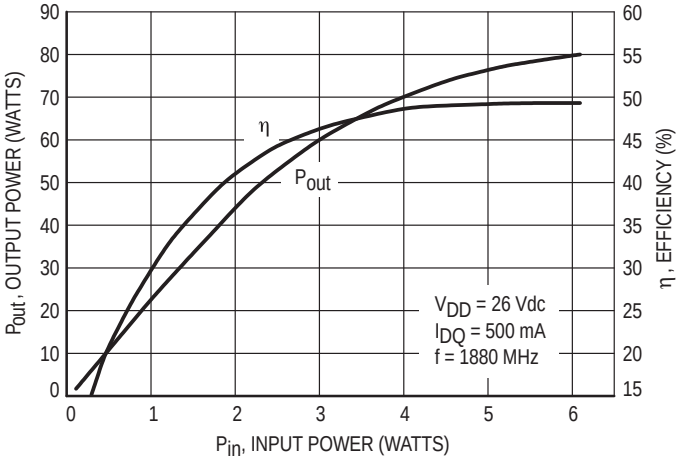


Figure 8. Output Power and Efficiency versus Input Power

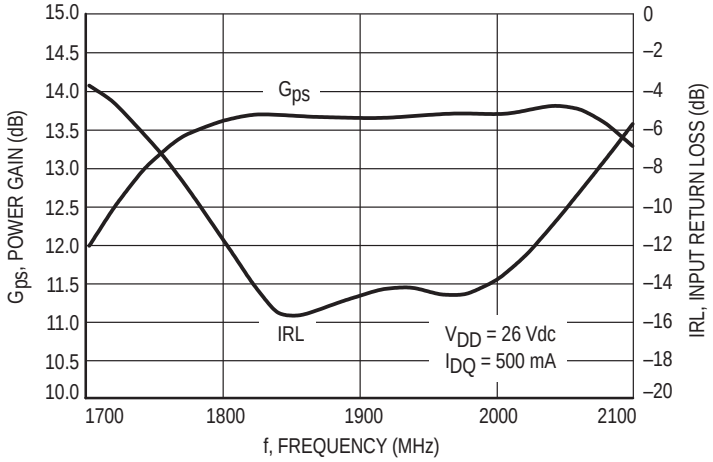


Figure 9. Wideband Gain and IRL (at Small Signal)

The RF MOSFET Line

RF Power Field Effect Transistors

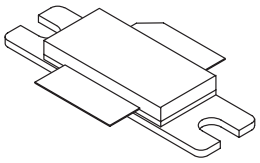
N–Channel Enhancement–Mode Lateral MOSFETs

MRF18060B
MRF18060BS

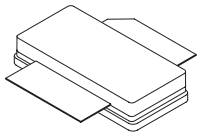
60 W, 1.90 – 1.99 GHz, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

Designed for PCN and PCS base station applications from frequencies up to 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in class AB for PCN–PCS/cellular radio and WLL applications. Specified for GSM1930 – 1990 MHz.

- GSM Performance, Full Frequency Band (1930 – 1990 MHz)
  Power Gain — 13 dB (Typ) @ 60 Watts (CW)
  Efficiency — 45% (Typ) @ 60 Watts (CW)
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection: Class 2 Human Body Model, Class M3
  Machine Model
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 60 Watts (CW) Output Power
- Excellent Thermal Stability



CASE 465–04, STYLE 1
(MRF18060B)



CASE 465A–04, STYLE 1
(MRF18060BS)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C > = 25°C Derate above 25°C	P_D	180 1.03	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	°C/W

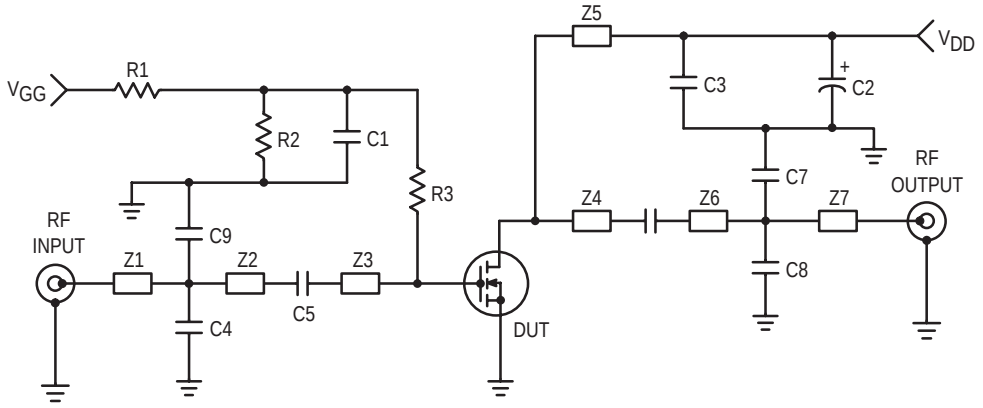
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0)	I_{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.27	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	4.7	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Including Input Matching Capacitor in Package) (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	160	—	pF
Output Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	740	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain @ 60 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 500 mA, f = 1930 – 1990 MHz)	G_{ps}	11.5	13	—	dB
Drain Efficiency @ 60 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 500 mA, f = 1930 – 1990 MHz)	η	40	45	—	%
Input Return Loss (2) (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA, f = 1930 – 1990 MHz)	IRL	10	—	—	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

(2) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1900 band, ensuring batch–to–batch consistency.



C1, C3	10 pF, 100B Chip Capacitor	C7, C9	0.3 pF, 100B Chip Capacitor
C2	10 μF, 35 V Electrolytic Tantalum Capacitor	R1, R2	10 kΩ, Chip Resistor 0805
C4, C8	1.2 pF, 100B Chip Capacitor	R3	1.0 kΩ, Chip Resistor 0805
C5	1.0 pF, 100B Chip Capacitor		
C6	2.2 pF, 100B Chip Capacitor	PCB	Teflon® Glass

Figure 1. 1930 – 1990 MHz Test Fixture Schematic

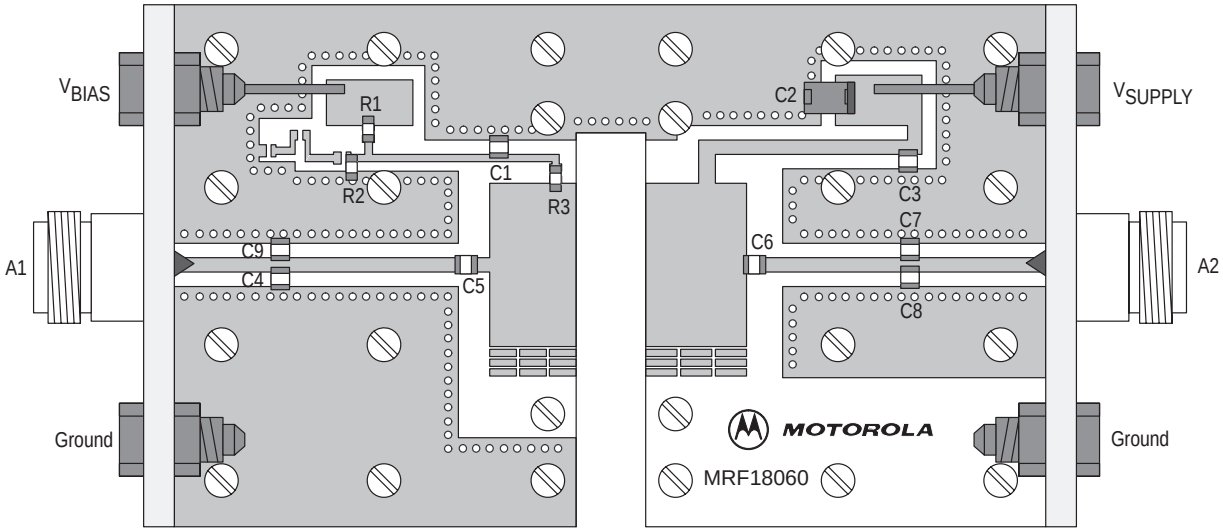
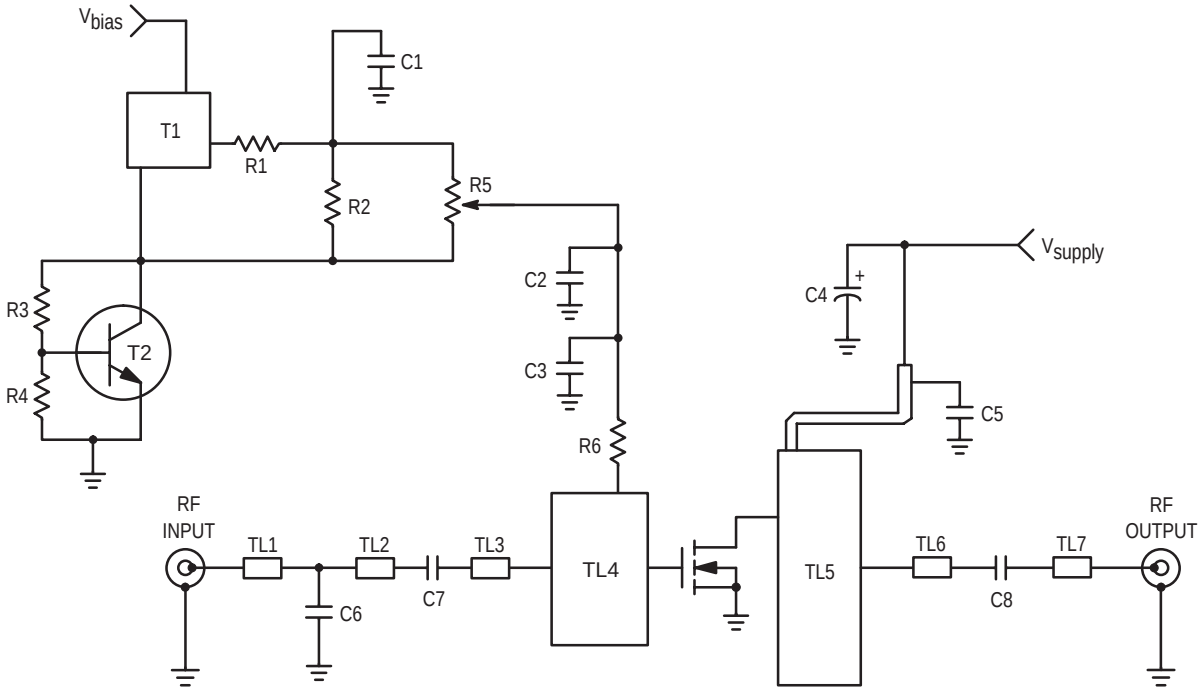


Figure 2. 1930 – 1990 MHz Test Fixture Component Layout



C1	1 μF, Chip Capacitor 0805	R1	10 Ω, Chip Resistor 0805
C2	100 nF, Chip Capacitor 0805	R2, R6	1 kΩ, Chip Resistor 0805
C3, C5, C8	10 pF, ACCU–P Chip Capacitor 0805	R3	1.2 kΩ, Chip Resistor 0805
C4	10 μF, 35 V Tantalum Electrolytic Capacitor	R4	2.2 kΩ, Chip Resistor 0805
C6	1.8 pF, ACCU–P Chip Capacitor 0805	R5	5 kΩ, SMD Potentiometer
C7	1 pF, ACCU–P Chip Capacitor 0805	T1	LP2951 Micro–8 Voltage Regulator
		T2	BC847 SOT–23 NPN Transistor

Substrate = 0.5 mm Teflon® Glass, ε_r = 2.55

Figure 3. 1800 – 2000 MHz Demo Board Schematic

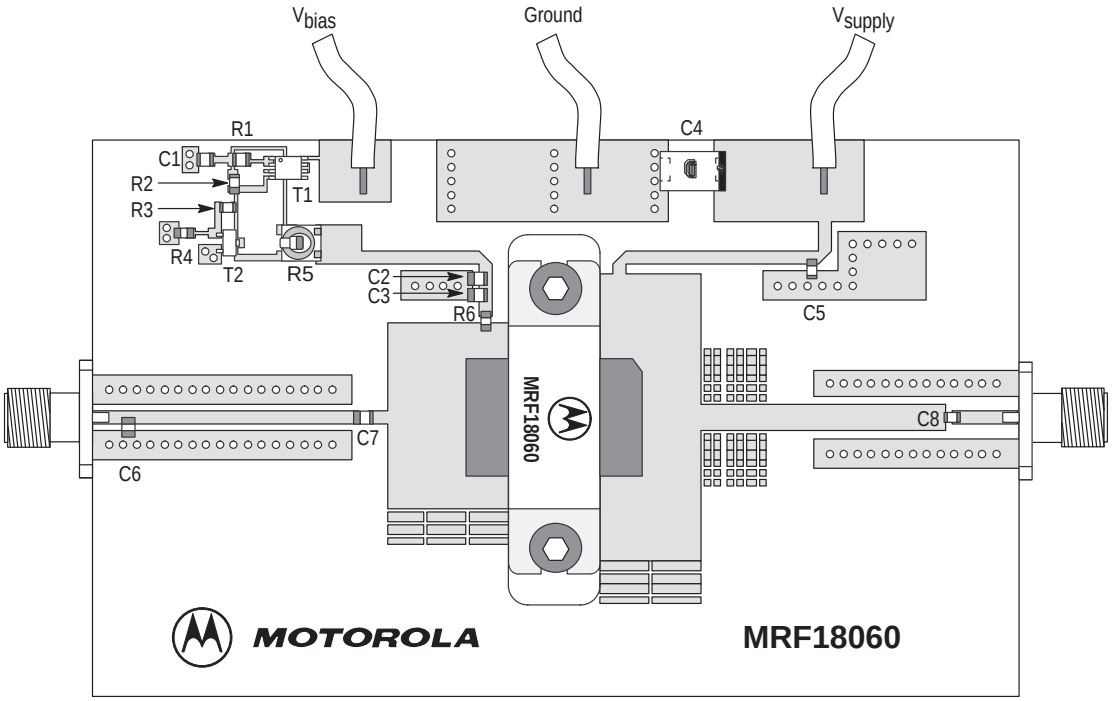


Figure 4. 1800 – 2000 MHz Demo Board Component Layout

TYPICAL CHARACTERISTICS (DATA TAKEN USING WIDEBAND DEMONSTRATION BOARD)

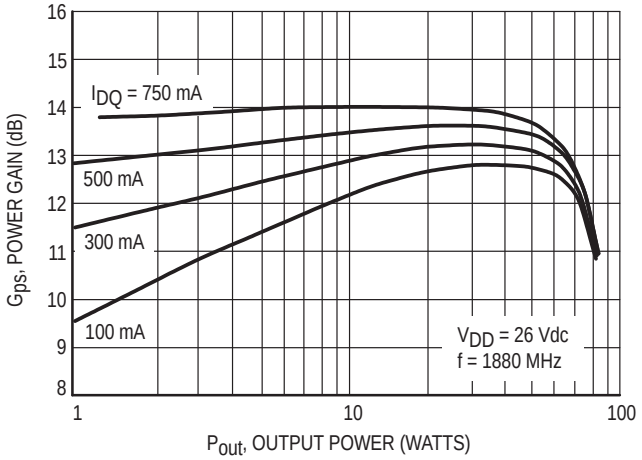


Figure 5. Power Gain versus Output Power

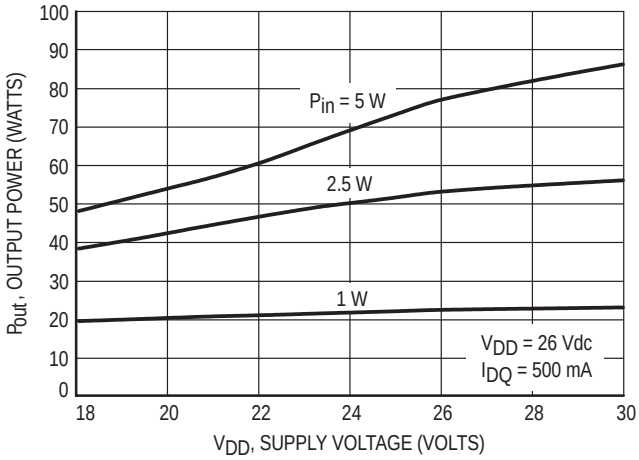


Figure 6. Output Power versus Supply Voltage

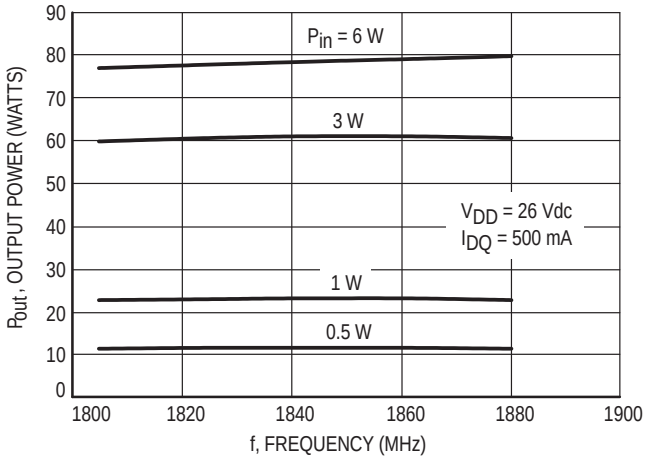


Figure 7. Output Power versus Frequency

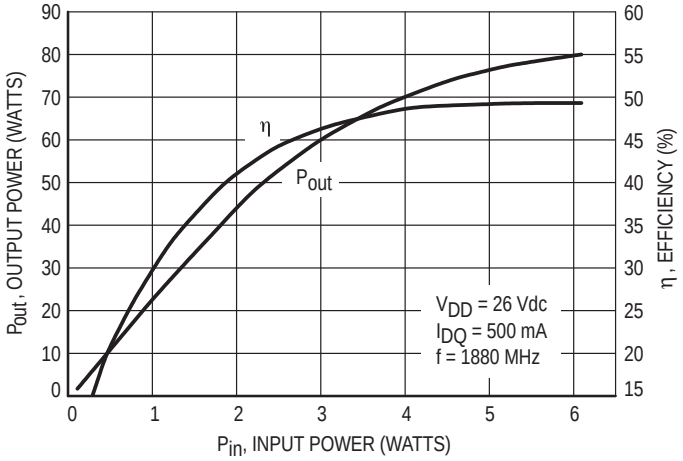


Figure 8. Output Power and Efficiency versus Input Power

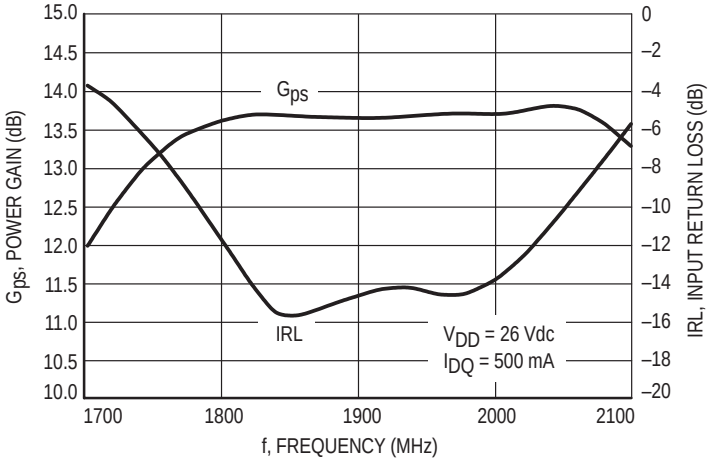


Figure 9. Wideband Gain and IRL (at Small Signal)

V_{DD} = 26 V, I_{DQ} = 500 mA, P_{out} = 60 Watts (CW)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1700	0.60 + j2.53	2.27 + j3.44
1800	0.80 + j3.20	2.05 + j3.05
1900	0.92 + j3.42	1.90 + j2.90
2000	1.07 + j3.59	1.64 + j2.88
2100	1.31 + j4.00	1.29 + j2.99

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

Table 1. Series Equivalent Input and Output Impedance

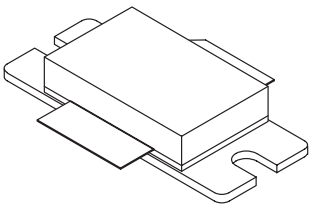
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF18090A
MRF18090AS

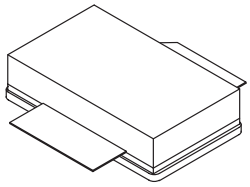
90 W, 1.80 – 1.88 GHz, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETS

Designed for GSM and EDGE base station applications from frequencies up to 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in class AB for GSM and EDGE cellular radio applications.

- GSM and EDGE Performances, Full Frequency Band
  Power Gain — 13.5 dB (Typ) @ 90 Watts (CW)
  Efficiency — 52% (Typ) @ 90 Watts (CW)
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection: Class 2 Human Body Model, Class M3
  Machine Model
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 90 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 465B–02, STYLE 1



CASE 465C–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

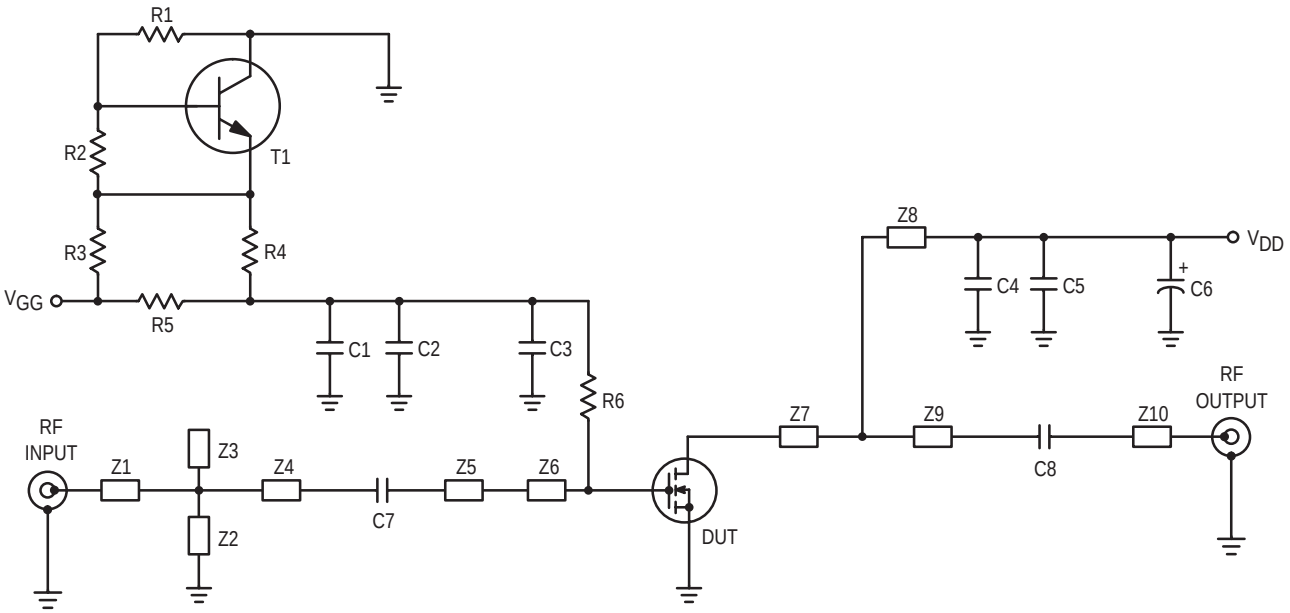
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 750 mAdc)	$V_{GS(Q)}$	2.5	3.7	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.1	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	7.2	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	4.2	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain @ 90 W (1) (V_{DD} = 26 Vdc, I_{DQ} = 750 mA, f = 1805 – 1880 MHz)	G_{ps}	12.0	13.5	—	dB
Drain Efficiency @ 90 W (1) (V_{DD} = 26 Vdc, I_{DQ} = 750 mA, f = 1805 – 1880 MHz)	η	47	52	—	%
Input Return Loss (1) (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA, f = 1805 – 1880 MHz)	IRL	10	—	—	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1800 band, ensuring batch–to–batch consistency.



R1	2.2 kΩ, Chip Resistor 0805	C4, C5	6.8 pF, 100B Chip Capacitor ATC
R2, R3, R6	1.0 kΩ, Chip Resistor 0805	C6	220 μF, 50 V Electrolytic Capacitor
R4	10 kΩ, Chip Resistor 0805	C7, C8	12 pF, 100B Chip Capacitor ATC
R5	6.8 kΩ, Chip Resistor 0805	T1	BC847 SOT–23
C1, C3	1.0 μF, Chip Capacitor 0805	Z1 – Z10	Printed Microstrip Line
C2	1.0 nF, Chip Capacitor 0805	PCB	Teflon® Glass

Figure 1. 1.80 – 1.88 GHz Test Fixture Schematic

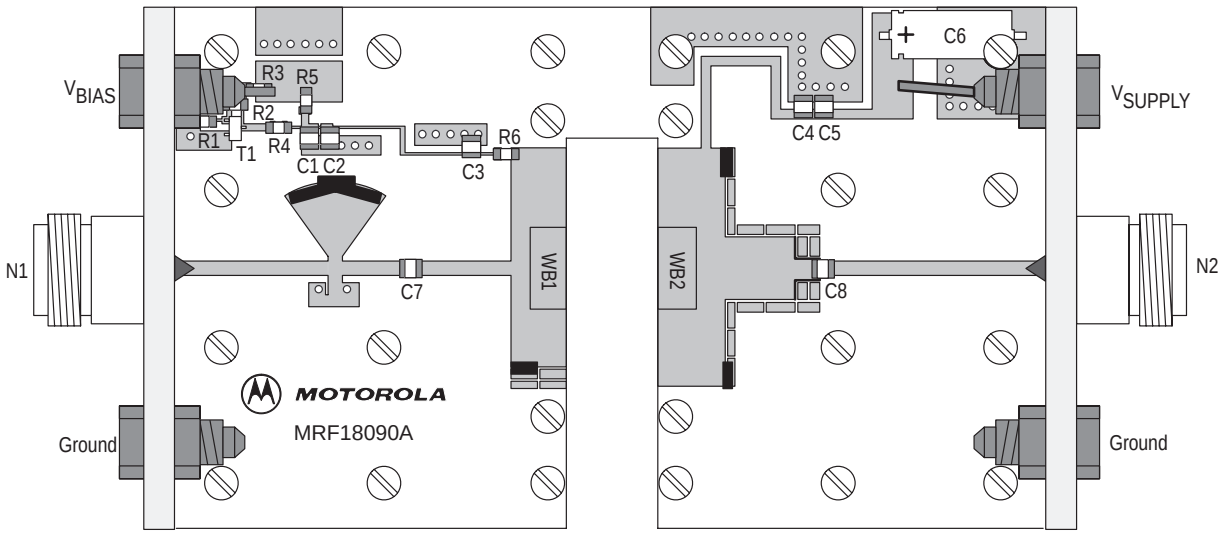
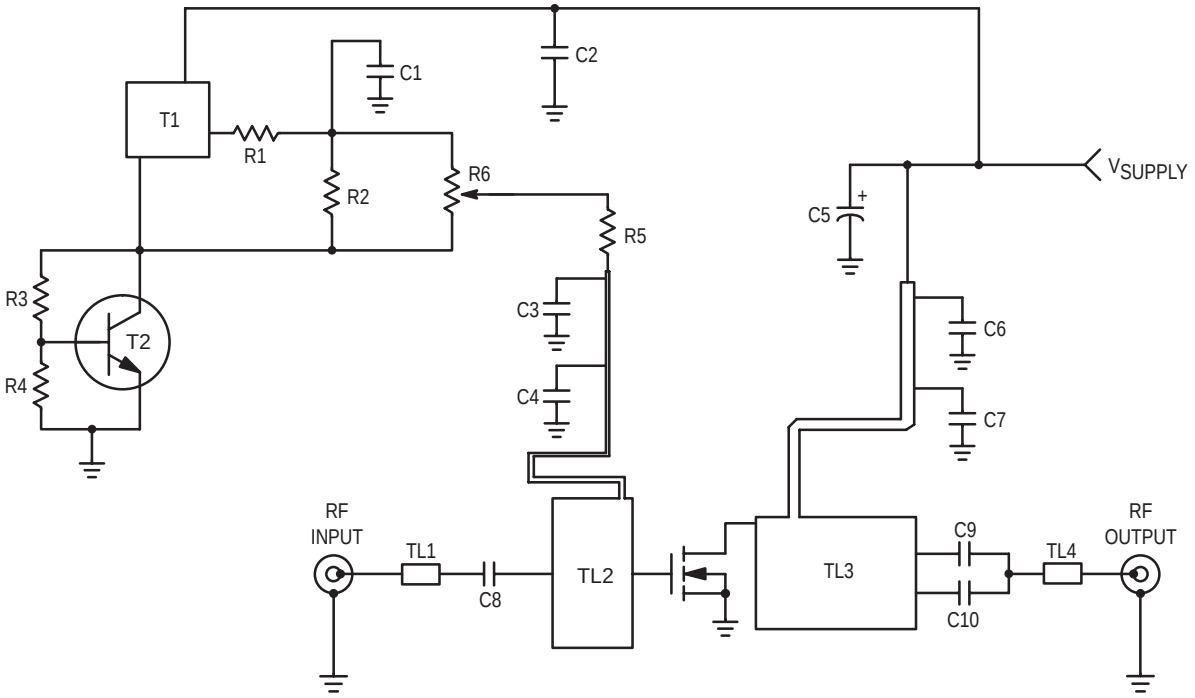


Figure 2. 1.80 – 1.88 GHz Test Fixture Component Layout



C1, C3	1 μF, Chip Capacitor 0805
C2	0.1 μF, Chip Capacitor 0805
C4	1 nF, Chip Capacitor 0805
C5	220 μF, 50 V Electrolytic Capacitor
C6, C7	8.2 pF, 100A Chip Capacitor
C8, C9, C10	22 pF, 100A Chip Capacitor

R1	10 Ω, Chip Resistor 0805
R2, R3	1 kΩ, Chip Resistor 0805
R4	2.2 kΩ, Chip Resistor 0805
R5	10 kΩ, Chip Resistor 0603
R6	5 kΩ, SMD Potentiometer
T1	LP2951 Micro–8 Voltage Regulator
T2	BC847 SOT–23 NPN Transistor
TL1 – TL4	Printed Transmission Lines

Substrate = 0.5 mm Teflon® Glass

Figure 3. 1.80 – 1.88 GHz Demo Board Schematic

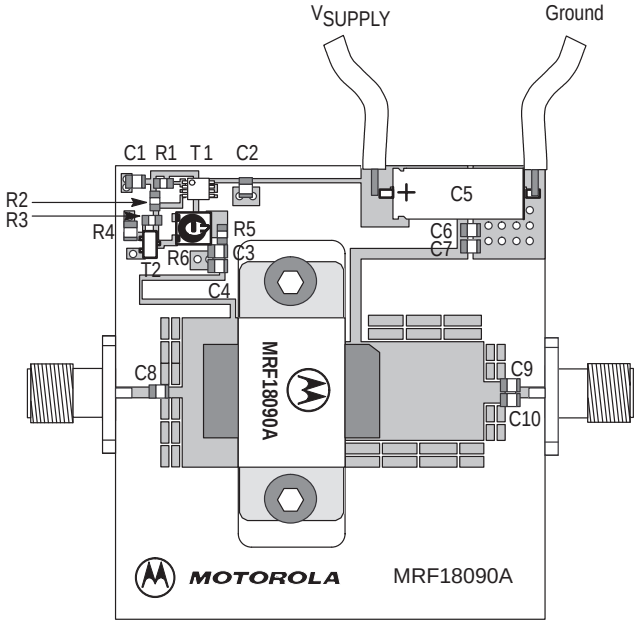


Figure 4. 1.80 – 1.88 GHz Demo Board Component Layout

TYPICAL CHARACTERISTICS

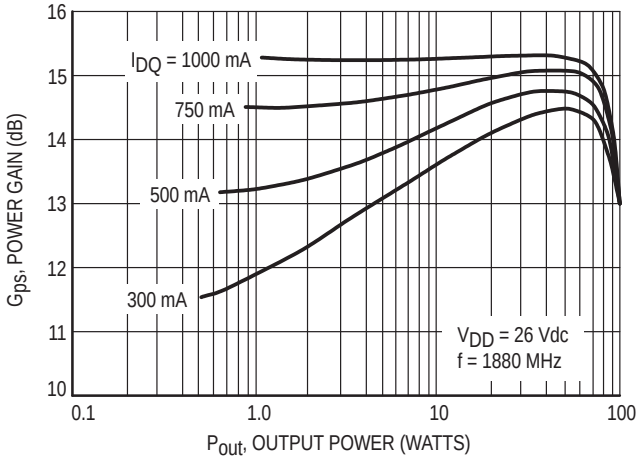


Figure 5. Power Gain versus Output Power

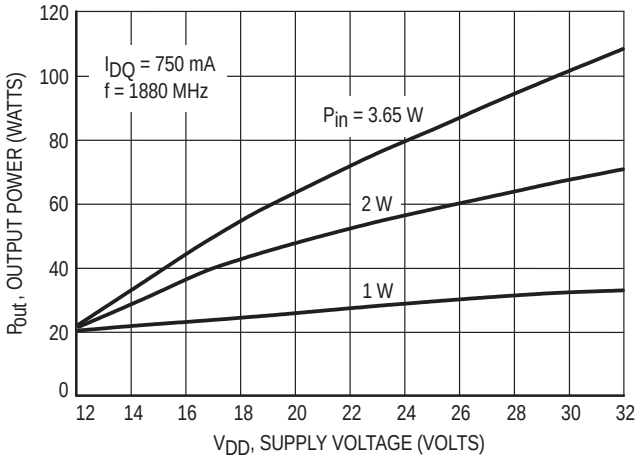


Figure 6. Output Power versus Supply Voltage

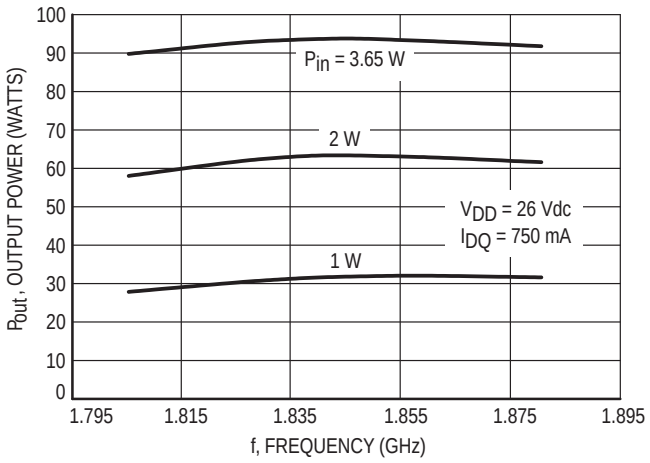


Figure 7. Output Power versus Frequency

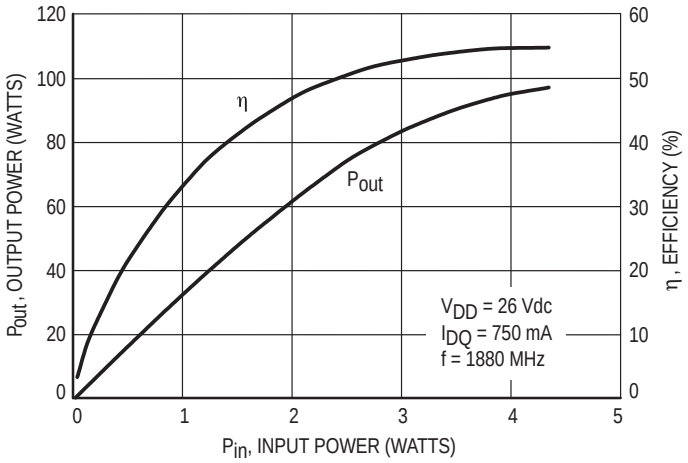


Figure 8. Output Power and Efficiency versus Input Power

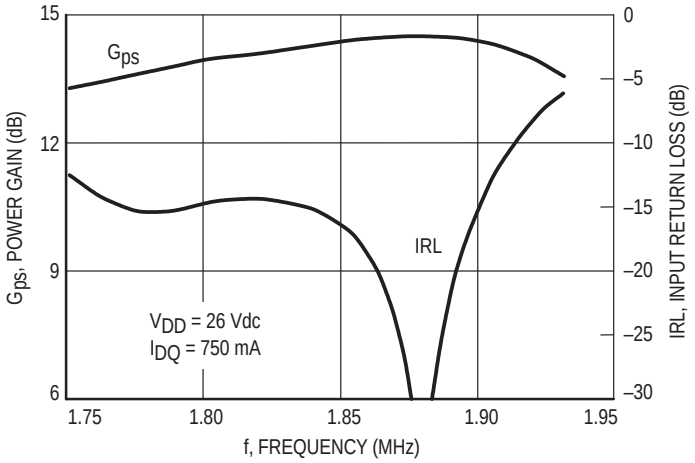


Figure 9. Wideband Gain and IRL (at Small Signal)

V_{DD} = 26 V, I_{DQ} = 750 mA, P_{out} = 90 Watts (CW)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1805	1.1 + j5.85	1.15 + j2.16
1880	1.56 + j6.75	1.13 + j2.6
1930	2.05 + j8.0	1.30 + j2.23
1990	2.3 + j7.3	0.82 + j2.90

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

Table 1. Large Signal Input and Output Impedance

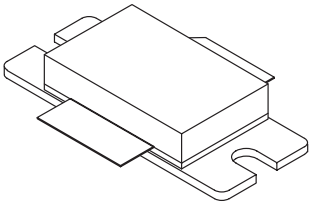
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF18090B
MRF18090BS

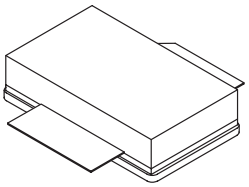
90 W, 1.90 – 1.99 GHz, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETS

Designed for GSM and EDGE base station applications from frequencies up to 1.9 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in class AB for GSM and EDGE cellular radio applications.

- GSM and EDGE Performances, Full Frequency Band
  Power Gain — 13.5 dB (Typ) @ 90 Watts (CW)
  Efficiency — 45% (Typ) @ 90 Watts (CW)
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection: Class 2 Human Body Model, Class M3
  Machine Model
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 90 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 465B–02, STYLE 1



CASE 465C–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

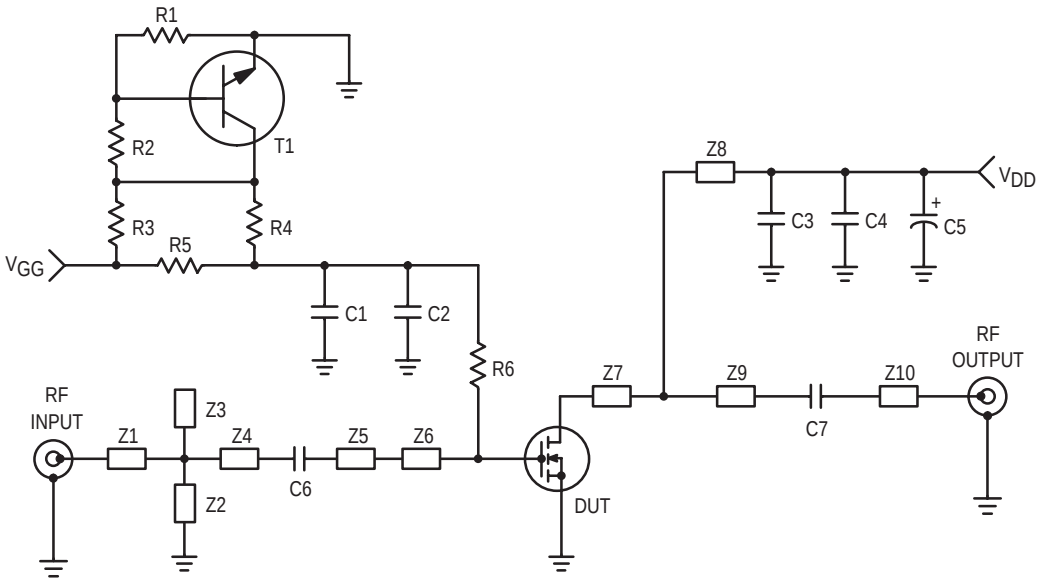
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 750 mAdc)	$V_{GS(Q)}$	2.5	3.7	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.1	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	7.2	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	4.2	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain @ 90 W (1) (V_{DD} = 26 Vdc, I_{DQ} = 750 mA, f = 1930 – 1990 MHz)	G_{ps}	12	13.5	—	dB
Drain Efficiency @ 90 W (1) (V_{DD} = 26 Vdc, I_{DQ} = 750 mA, f = 1930 – 1990 MHz)	η	40	45	—	%
Input Return Loss (1) (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA, f = 1930 – 1990 MHz)	IRL	10	—	—	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1900 band, ensuring batch–to–batch consistency.



C1	1.0 μF, Chip Capacitor 0805	R2, R3, R6	1.0 kΩ, Chip Resistor 0805
C2	1.0 nF, Chip Resistor 0805	R4	10 kΩ, Chip Resistor 0805
C3, C4	6.8 pF, 100B Chip Capacitor	R5	6.8 kΩ, Chip Resistor 0805
C5	220 μF, 50 V Electrolytic Capacitor	T1	BC847 SOT–23
C6, C7	12 pF, 100B Chip Capacitor	Z1 – Z10	Printed Microstrip Line
R1	2.2 kΩ, Chip Resistor 0805	PCB	Teflon® Glass

Figure 1. 1.93 – 1.99 MHz Test Fixture Schematic

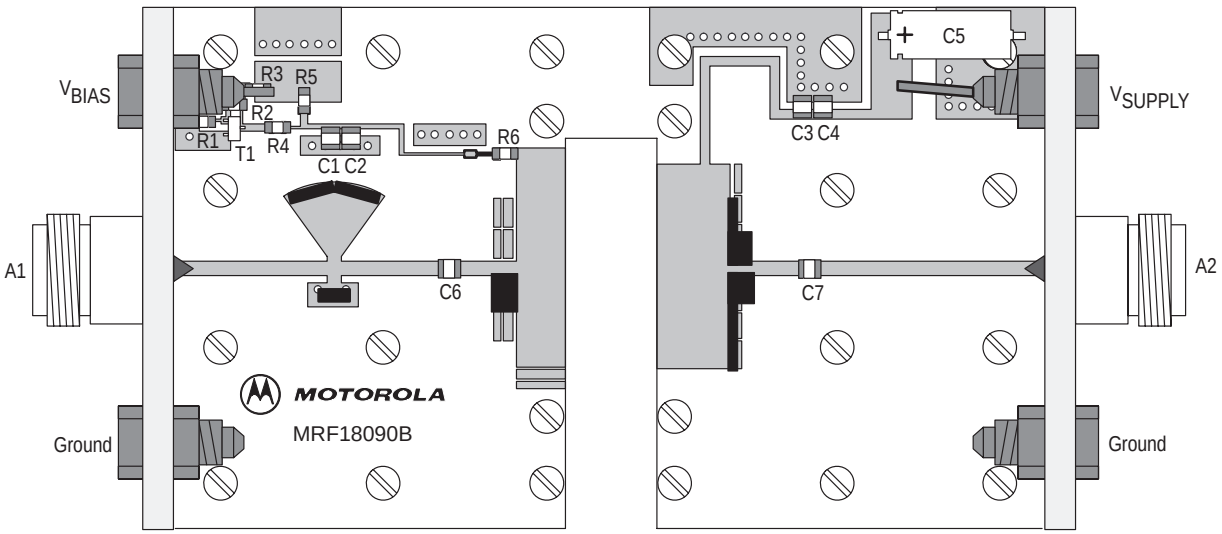
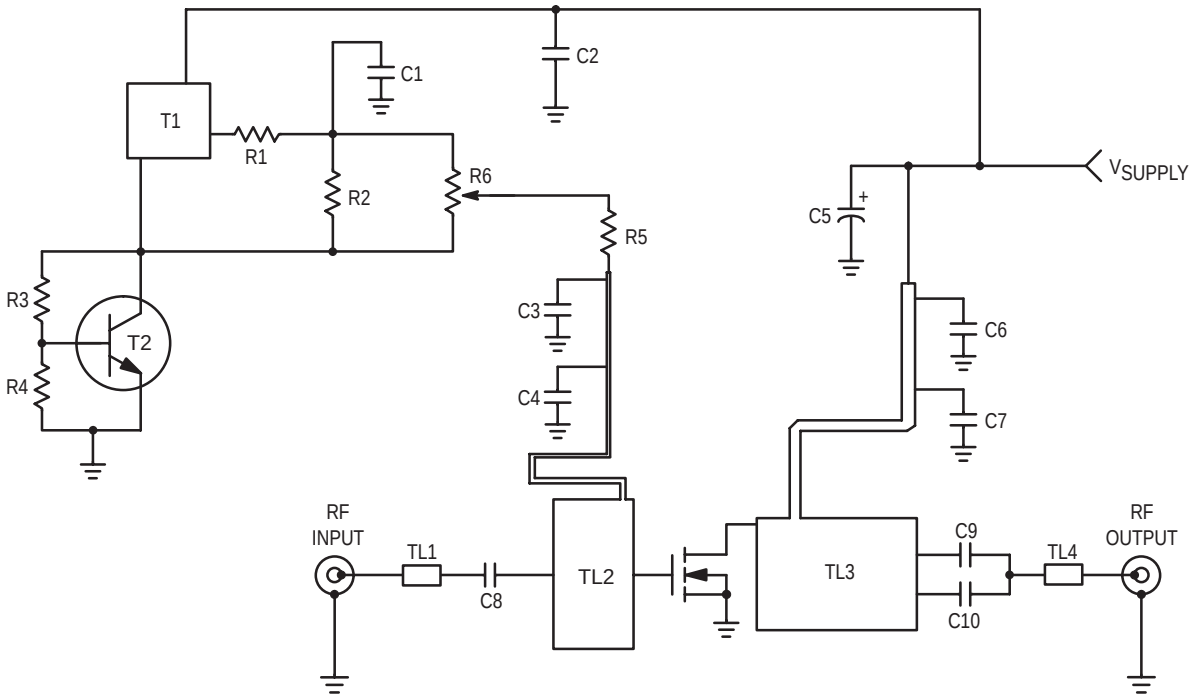


Figure 2. 1.93 – 1.99 GHz Test Fixture Component Layout



C1, C3	1 μF, Chip Capacitor 0805
C2	0.1 μF, Chip Capacitor 0805
C4	1 nF, Chip Capacitor 0805
C5	220 μF, 50 V Electrolytic Capacitor
C6, C7	8.2 pF, 100A Chip Capacitor
C8, C9, C10	22 pF, 100A Chip Capacitor

R1	10 Ω, Chip Resistor 0805
R2, R3	1 kΩ, Chip Resistor 0805
R4	2.2 kΩ, Chip Resistor 0805
R5	10 kΩ, Chip Resistor 0603
R6	5 kΩ, SMD Potentiometer
T1	LP2951 Micro–8 Voltage Regulator
T2	BC847 SOT–23 NPN Transistor
TL1 – TL4	Printed Transmission Lines

Substrate = 0.5 mm Teflon® Glass

Figure 3. 1.93 – 1.99 GHz Demo Board Schematic

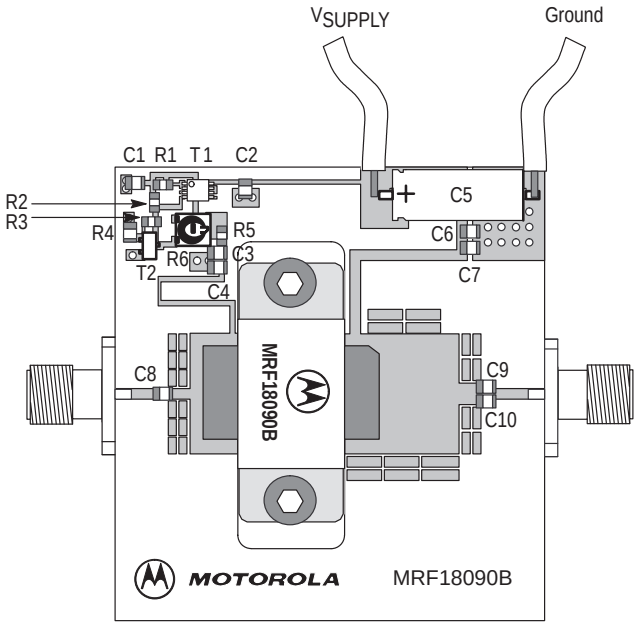


Figure 4. 1.93 – 1.99 GHz Demo Board Component Layout

TYPICAL CHARACTERISTICS

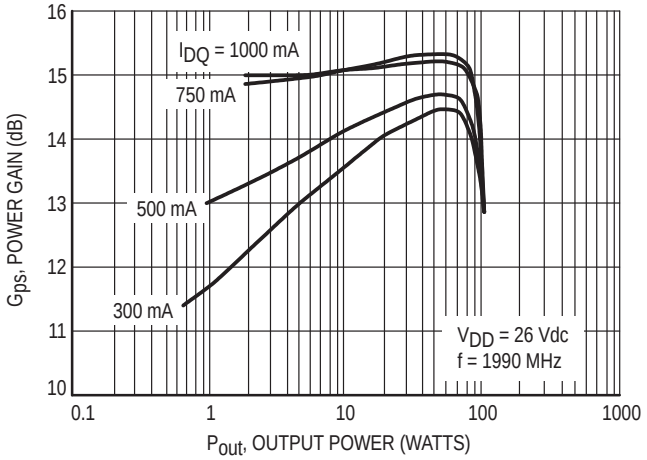


Figure 5. Power Gain versus Output Power

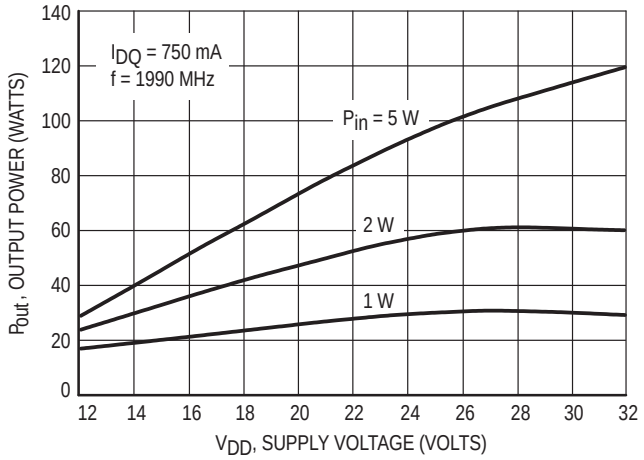


Figure 6. Output Power versus Supply Voltage

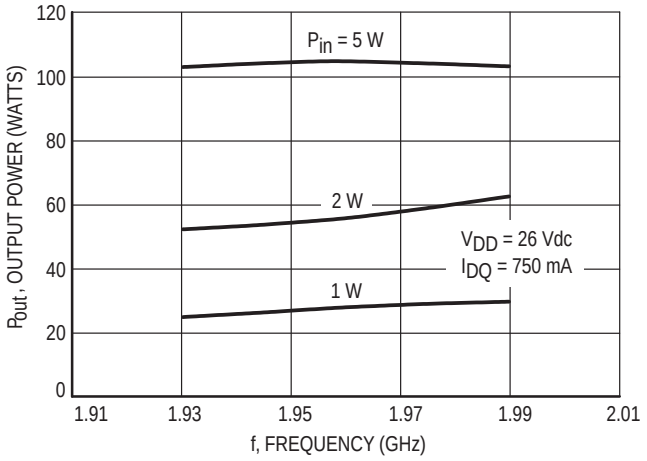


Figure 7. Output Power versus Frequency

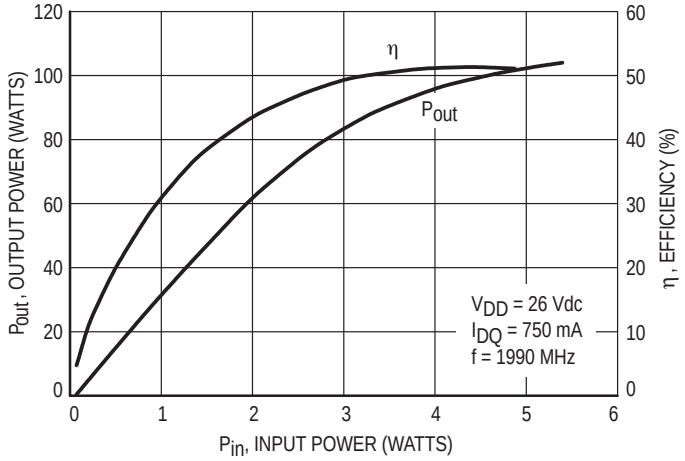


Figure 8. Output Power and Efficiency versus Input Power

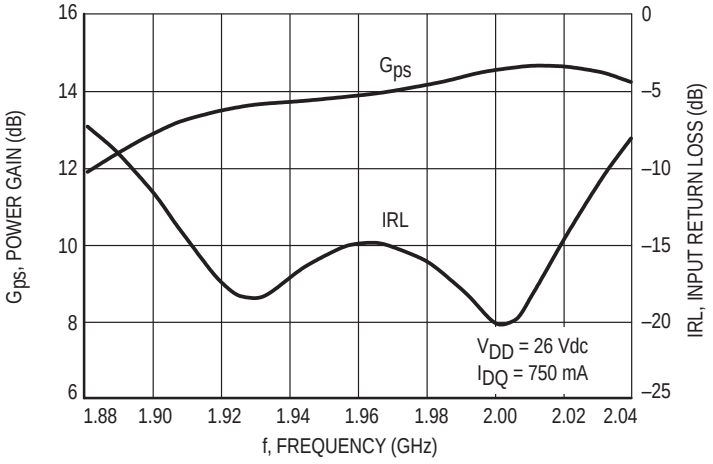


Figure 9. Wideband Gain and IRL (at Small Signal)

V_{DD} = 26 V, I_{DQ} = 750 mA, P_{out} = 90 Watts (CW)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1805	1.1 + j5.85	1.15 + j2.16
1880	1.56 + j6.75	1.13 + j2.6
1930	2.05 + j8.0	1.30 + j2.23
1990	2.3 + j7.3	0.82 + j2.90

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

Table 1. Large Signal Input and Output Impedance

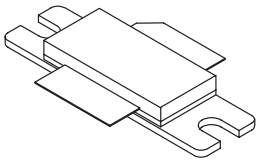
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF19060
MRF19060S

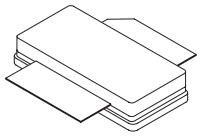
60 W, 1990 MHz, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

Designed for PCN and PCS base station applications from frequencies up to 1.9 to 2.0 GHz. Suitable for CDMA, TDMA, GSM and multicarrier amplifier applications.

- Typical CDMA Performance: 1960 MHz, 26 Volts
  IS–97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
  Output Power — 7.5 Watts
  Power Gain — 12.5 dB
  Adjacent Channel Power —
  885 kHz: –47 dBc @ 30 kHz BW
  1.25 MHz: –55 dBc @ 12.5 kHz BW
  2.25 MHz: –55 dBc @ 1 MHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection: Class 2 Human Body Model, Class M3
  Machine Model
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 60 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 465–04, STYLE 1
(MRF19060)



CASE 465A–04, STYLE 1
(MRF19060S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ $T_C \geq = 25°C$ Derate above 25°C	P_D	180 1.03	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

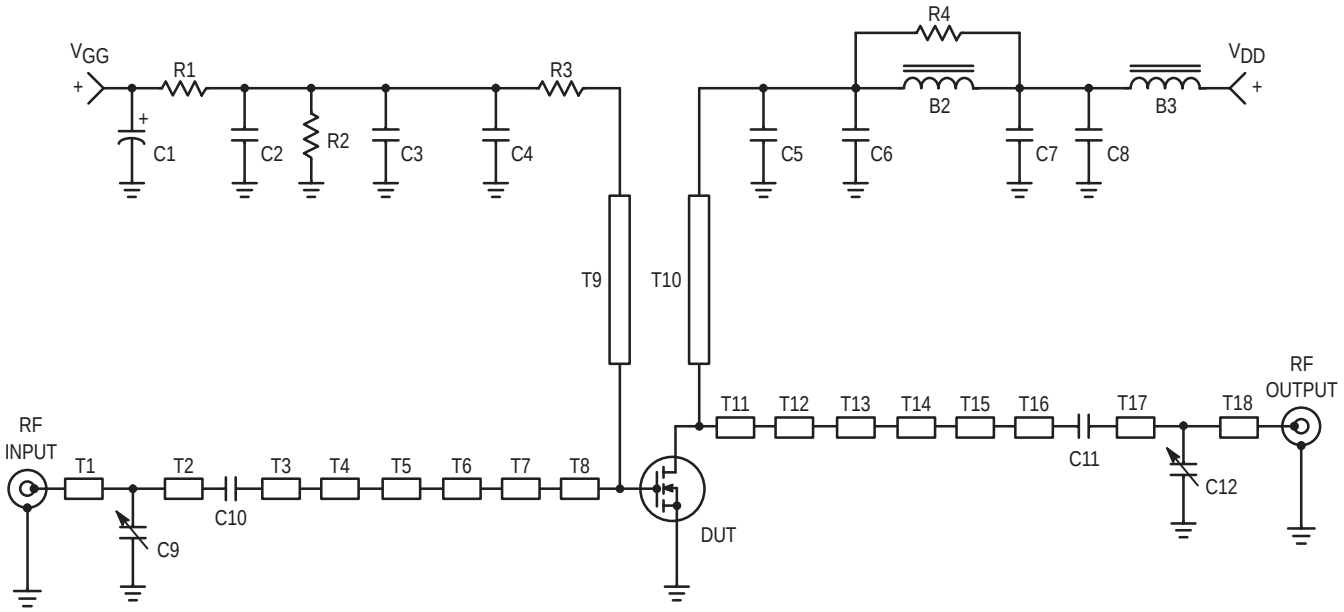
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0)	I_{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	4.7	—	S
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$VGS_{(th)}$	2	—	4	V
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	V
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.27	—	V
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	G_{ps}	11	12.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	η	33	36	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 26 Vdc, P_{out} = 60 W CW, f = 1990 MHz)	P1dB	—	60	—	W
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA, f = 1930 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B2 – B3	Ferrite Bead, Fair Rite, 2743019447	T4	0.152″ x 0.140″ Microstrip
C1	10 μF, 50 V Electrolytic, ECEV1HV100R Panasonic	T5	0.090″ x 0.102″ Microstrip
C2, C7	1000 pF, B Case Chip Capacitor, 100B102JCA500X, ATC	T6	0.245″ x 0.217″ Microstrip
C3, C8	0.10 μF, B Case Chip Capacitor, CDR33BX104AKWS, Kemet	T7	0.090″ x 0.737″ Microstrip
C4	5.1 pF, B Case Chip Capacitor, 100B5R1JCA500X, ATC	T8	0.530″ x 0.941″ Microstrip
C5	6.2 pF, B Case Chip Capacitor, 100B6R2JCA500X, ATC	T9	1.010″ x 0.050″ Microstrip
C6	22 μF, 35 V Tantalum, SMT, Sprague	T10	1.060″ x 0.050″ Microstrip
C9	0.8 pF – 8.0 pF, Variable Capacitor, Johanson Gigatrim	T11	0.446″ x 1.137″ Microstrip
C10, C11	10 pF, B Case Chip Capacitor, 100B100JCA500X, ATC	T12	0.152″ x 0.567″ Microstrip
C12	0.4 pF – 2.5 pF, Variable Capacitor, Johanson Gigatrim	T13	0.183″ x 0.220″ Microstrip
R1	1 kΩ, 1/4 W, Fixed Film Chip Resistor, 0.08″ x 0.13″	T14	0.100″ x 0.338″ Microstrip
R2	560 kΩ, 1/4 W, Fixed Film Chip Resistor, 0.08″ x 0.13″	T15	0.480″ x 0.142″ Microstrip
R3	15 Ω, 1/4 W, Fixed Film Chip Resistor, 0.08″ x 0.13″	T16	0.140″ x 0.080″ Microstrip
R4	10 Ω, 1/4 W, Fixed Film Chip Resistor, 0.08″ x 0.13″	T17	0.173″ x 0.080″ Microstrip
T1	0.580″ x 0.074″ Microstrip	T18	0.420″ x 0.080″ Microstrip
T2	0.100″ x 0.074″ Microstrip	Board	0.030″ Glass Teflon® Arlon
T3	0.384″ x 0.074″ Microstrip		GX–0300–55–22, 2 oz Cu

Figure 1. MRF19060 Schematic

TYPICAL CHARACTERISTICS

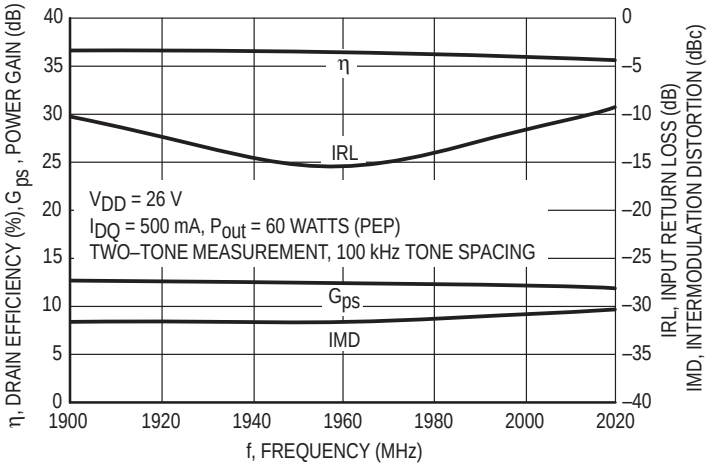


Figure 2. Class AB Broadband Circuit Performance

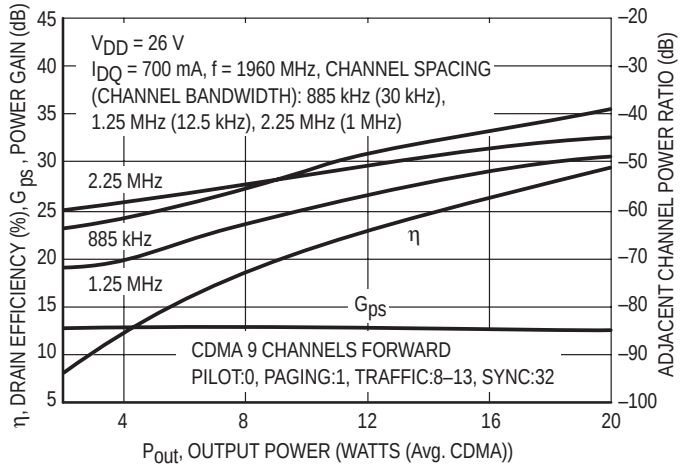


Figure 3. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

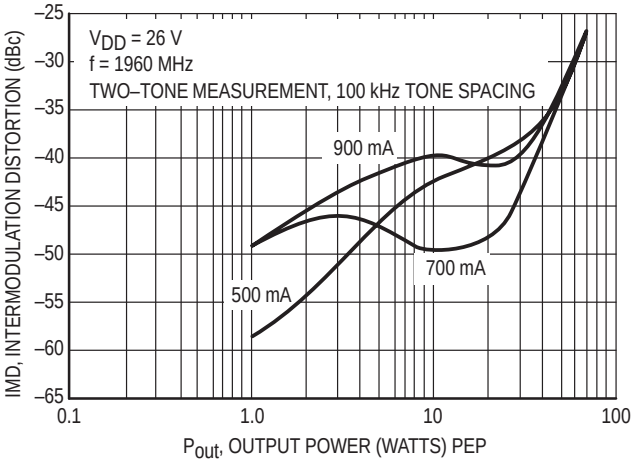


Figure 4. Intermodulation Distortion versus Output Power

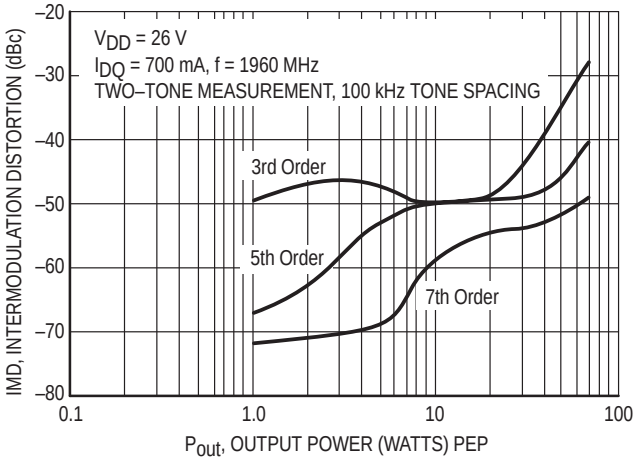


Figure 5. Intermodulation Products versus Output Power

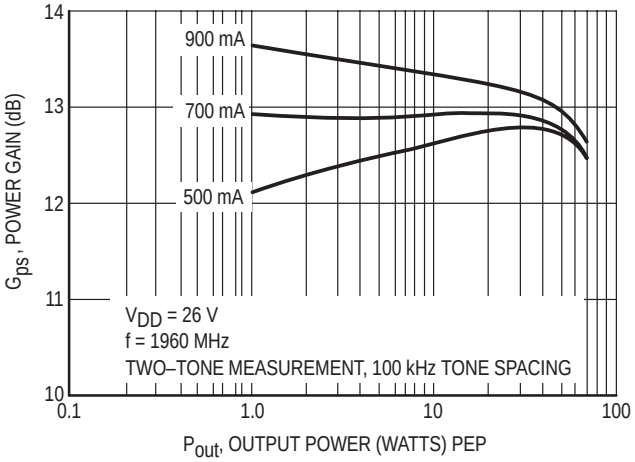


Figure 6. Power Gain versus Output Power

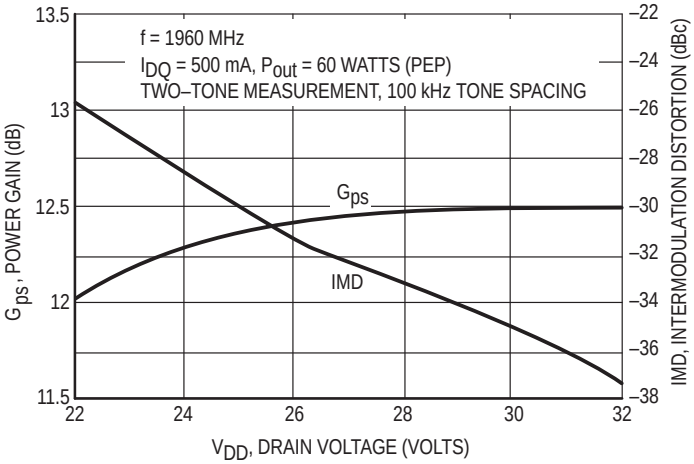
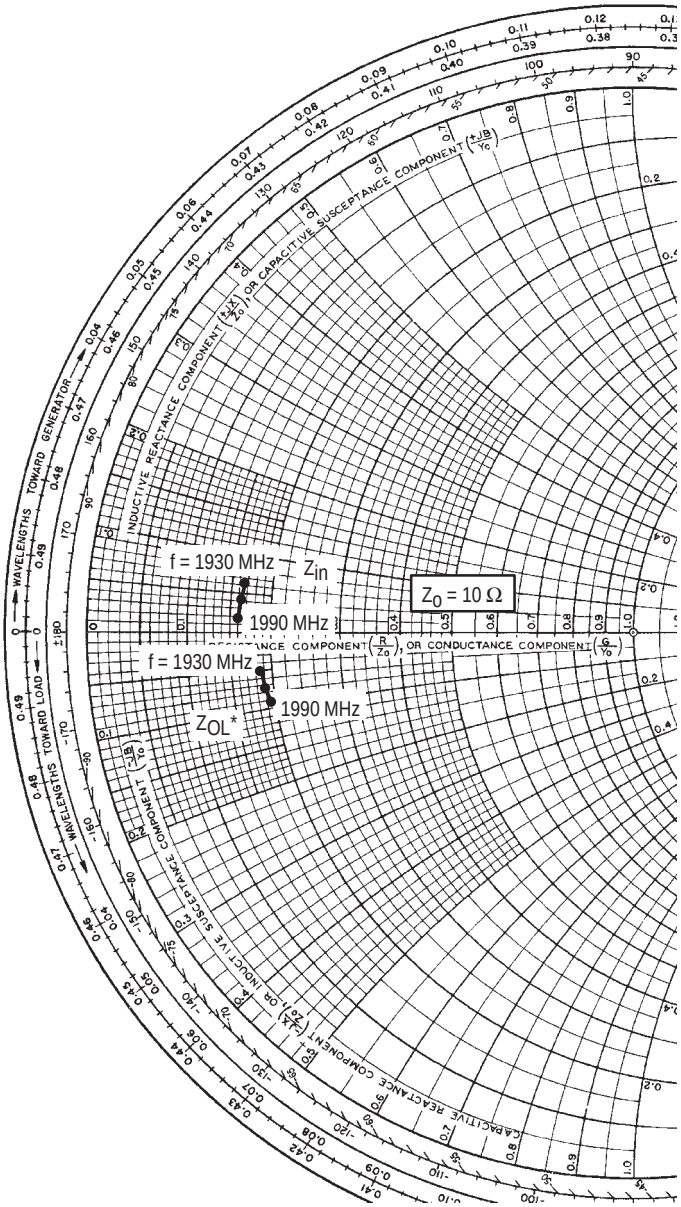


Figure 7. Power Gain and Intermodulation Distortion versus Supply Voltage



V_{DD} = 26 V, I_{DQ} = 500 mA, P_{out} = 60 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1930	1.65 + j0.67	1.85 – j0.50
1960	1.64 + j0.45	1.89 – j0.74
1990	1.60 + j0.20	1.96 – j0.94

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

Figure 8. Series Equivalent Input and Output Impedance

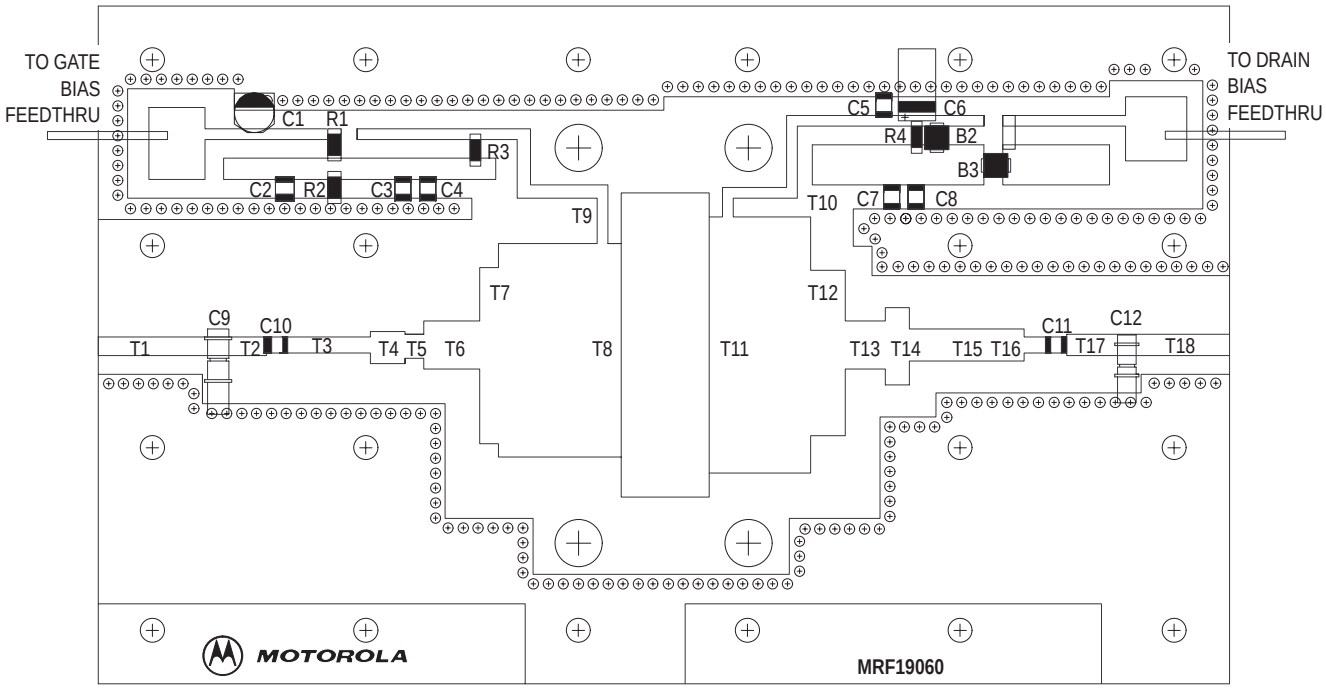


Figure 9. MRF19060 Populated PC Board Layout Diagram

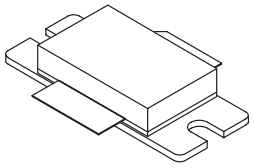
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF19090
MRF19090S

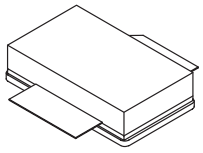
90 W, 1990 MHz
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

Designed for class AB PCN and PCS base station applications from 1.9 to 2.0 GHz. Suitable for CDMA, TDMA, GSM, and multicarrier amplifier applications.

- Typical CDMA Performance: 1990 MHz, 26 Volts
  IS–97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
  Output Power — 9 Watts
  Power Gain — 10 dB
  Adjacent Channel Power —
  885 kHz: –47 dBc @ 30 kHz BW
  1.25 MHz: –55 dBc @ 12.5 kHz BW
  2.25 MHz: –55 dBc @ 1 MHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection: Class 2 Human Body Model, Class M3
  Machine Model
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 90 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 465B–02, STYLE 1
(MRF19090)



CASE 465C–01, STYLE 1
(MRF19090S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C > = 25°C Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

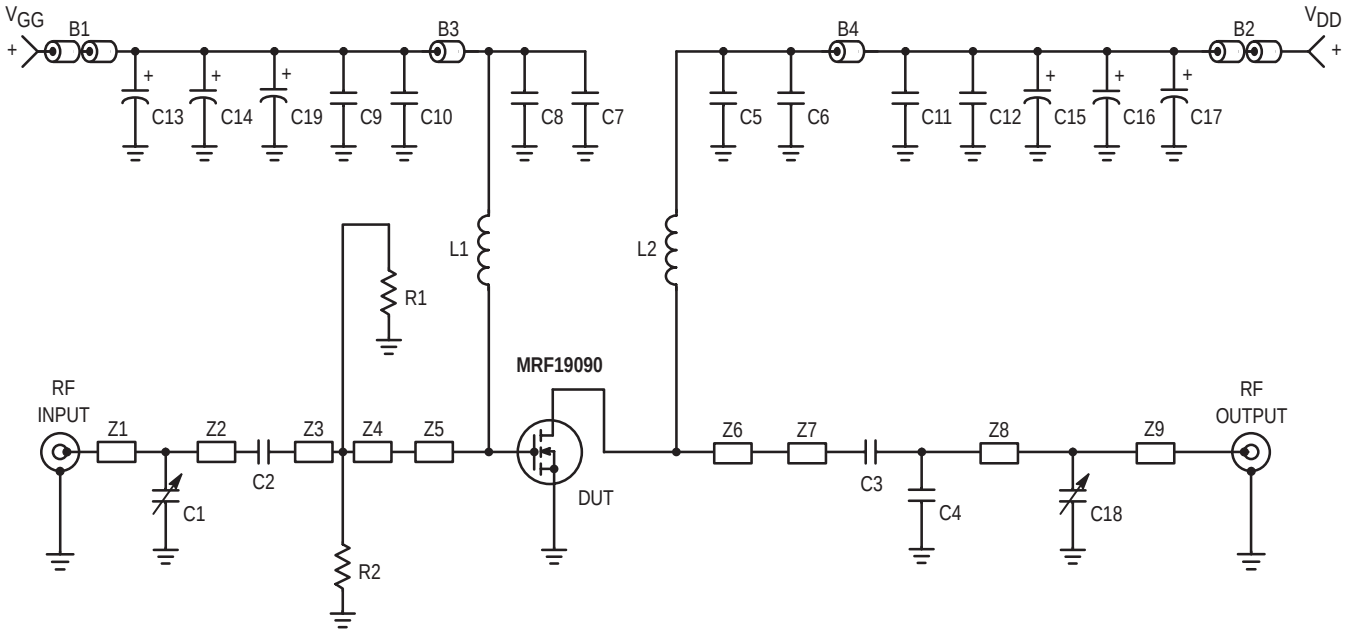
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	7.2	—	S
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$VGS_{(th)}$	2.0	—	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 750 mAdc)	$V_{GS(Q)}$	2.5	3.8	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.10	—	Vdc
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	4.2	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	G_{ps}	10	11.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	η	33	35	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IMD	—	–30	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 26 Vdc, P_{out} = 90 W CW, f = 1990 MHz)	P1dB	—	90	—	W
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA, f = 1930 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B1 – B4	2 Ferrite Beads, Round, Ferroxcube 56–590–65–3B	L1, L2	8 Turns, #26 AWG, 0.085″ OD, 0.330″ Long, Copper Wire
B2 – B3	Ferrite Bead, Surface Mount Ferrite Bead, Ferroxcube	R1, R2	270 Ω, 1/4 W Chip Resistor, Garrett Instruments RM73B2B271JT
C1, C18	0.4 – 2.5 pF, Gigatrim Variable Capacitors, Johanson 27285	Z1	ZO = 50 Ohms
C2, C5, C8	10 pF, ATC RF Chip Capacitors, Case “B”, 100B100CCA500X	Z2	ZO = 50 Ohms, Lambda = 0.123
C3	12 pF, ATC RF Chip Capacitors, Case “B”, 100B120CCA500X	Z3	ZO = 15.24 Ohms, Lambda = 0.0762
C4	0.3 pF, ATC RF Chip Capacitors, Case “B”, 100B0R3CCA500X	Z4	ZO = 10.11 Ohms, Lambda = 0.0392
C6, C7	120 pF, ATC RF Chip Capacitors, Case “B”, 100B12R1CCA500X	Z5	ZO = 6.34 Ohms, Lambda = 0.0711
C9, C12	0.1 μF, Chip Capacitor, CDR33BX104AKWS, KEMET	Z6	ZO = 5.02 Ohms, Lambda = 0.0476
C10, C11	1000 pF, ATC RF Chip Capacitors, Case “B”, 100B102JCA50X	Z7	ZO = 5.54 Ohms, Lambda = 0.0972
C13, C17	22 μF, 35 V Tantalum Surface Mount Electrolytic Chip Capacitor, T491X226K035AS4394, KEMET	Z8	ZO = 50.0 Ohms, Lambda = 0.194
C14, C16	10 μF, 35 V Tantalum Surface Mount Electrolytic Chip Capacitor, T495X106K035AS4394, KEMET	Z9	ZO = 50.0 Ohms
C15, C19	1 μF, 35 V Tantalum Surface Mount Electrolytic Chip Capacitor, T495X105K035AS4394, KEMET	Raw PCB Material	0.030″ Glass Teflon®, ε_r = 2.55, 2 oz Copper, 3″ x 5″ Dimensions

Figure 1. MRF19090 Test Circuit Schematic

TYPICAL CHARACTERISTICS

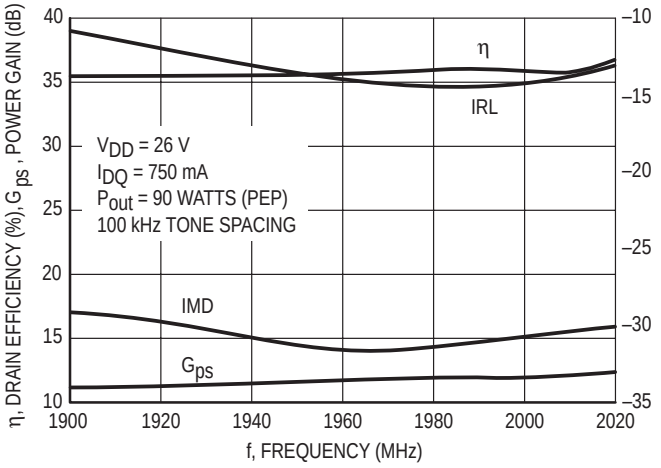


Figure 2. Class AB Performance versus Frequency

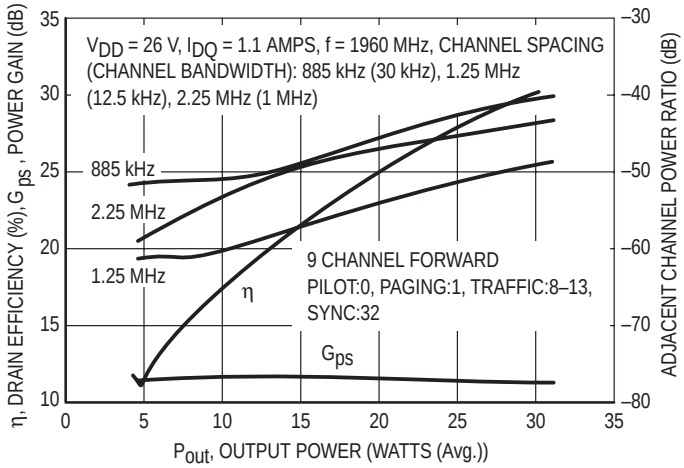


Figure 3. CDMA Performance ACPR, Gain and Drain Efficiency versus Output Power

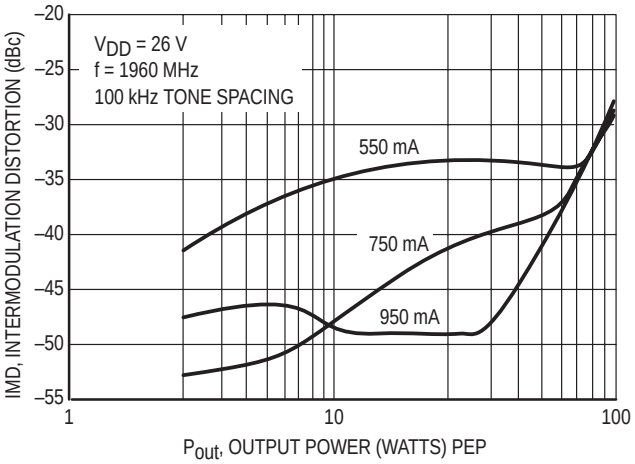


Figure 4. Third Order Intermodulation Distortion versus Output Power

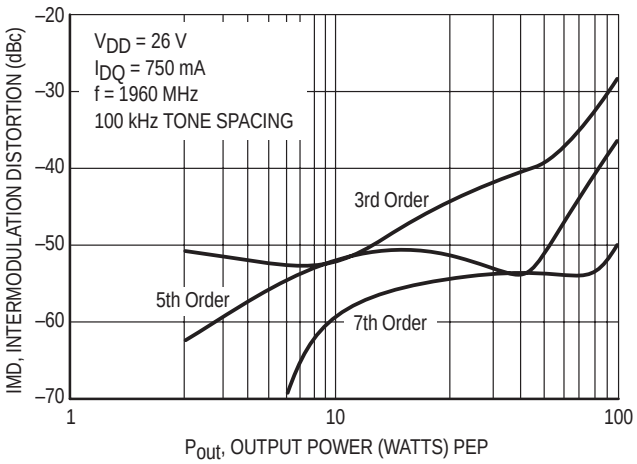


Figure 5. Intermodulation Products versus Output Power

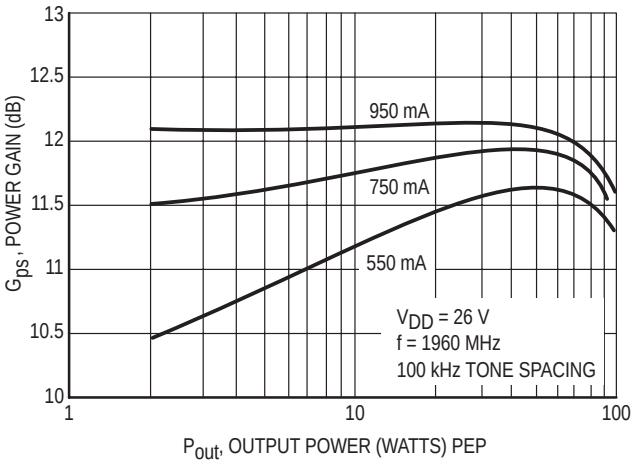


Figure 6. Power Gain versus Output Power

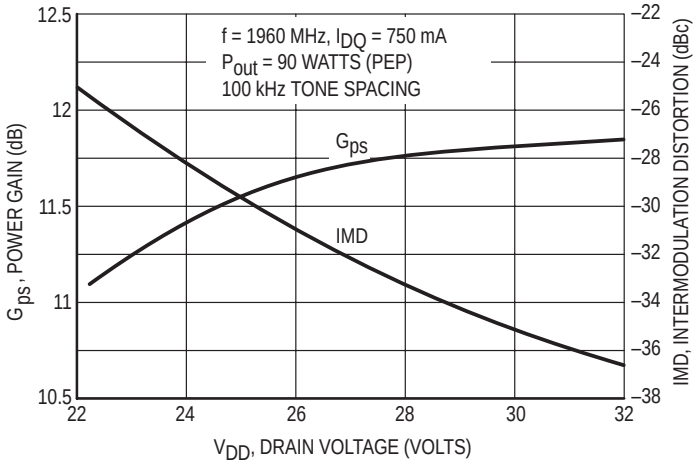
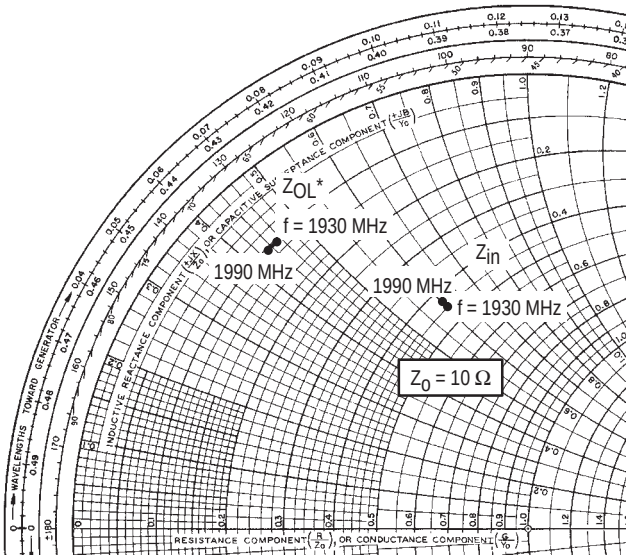


Figure 7. Third Order Intermodulation Distortion and Gain versus Supply Voltage



V_{DD} = 26 V, I_{DQ} = 750 mA, P_{out} = 90 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1930	4.5 + j6.1	1.1 + j4.5
1960	4.4 + j6.0	1.1 + j4.4
1990	4.3 + j6.1	1.1 + j4.3

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

Figure 8. Series Equivalent Input and Output Impedance

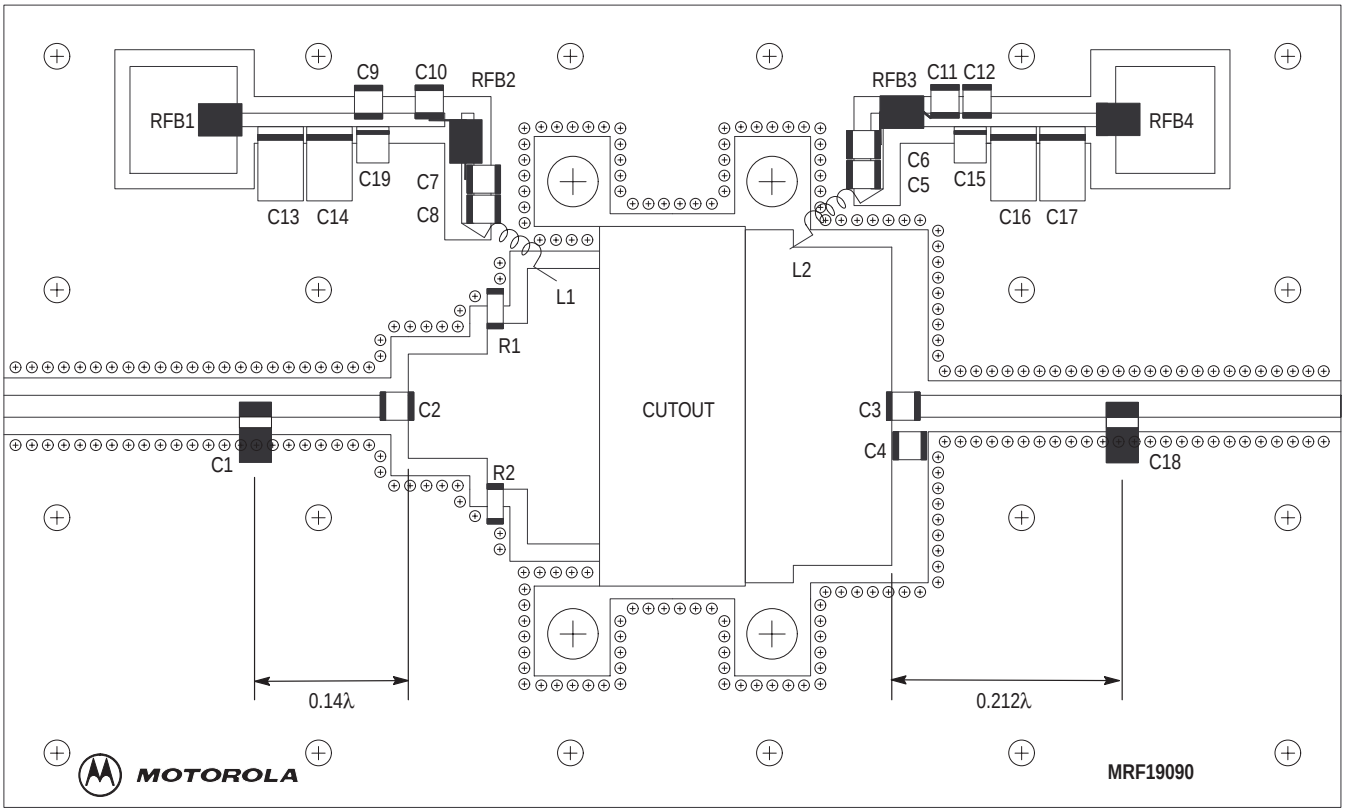


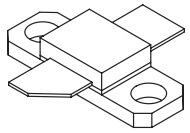
Figure 9. MRF19090 Populated PC Board Layout Diagram

The RF Sub–Micron Bipolar Line

RF Power Bipolar Transistor

MRF20030R

30 W, 2.0 GHz
NPN SILICON
BROADBAND
RF POWER TRANSISTOR



CASE 395C–01, STYLE 1

Designed for broadband commercial and industrial applications at frequencies from 1800 to 2000 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common–emitter class AB amplifier applications. Suitable for frequency modulated, amplitude modulated and multi–carrier base station RF power amplifiers.

- Specified 26 Volts, 2.0 GHz, Class AB, Two–Tones Characteristics
  Output Power — 30 Watts (PEP)
  Power Gain — 9.8 dB
  Efficiency — 34%
  Intermodulation Distortion — –28 dBc
- Typical 26 Volts, 1.88 GHz, Class AB, CW Characteristics
  Output Power — 30 Watts
  Power Gain — 11 dB
  Efficiency — 40%
  Intermodulation Distortion — –30 dBc
- Excellent Thermal Stability
- Capable of Handling 3:1 VSWR @ 26 Vdc, 2000 MHz, 30 Watts (PEP) Output Power
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Designed for FM, TDMA, CDMA, and Multi–Carrier Applications

Note: Not suitable for class A operation.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	25	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Collector–Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	30	Vdc
Emitter–Base Voltage	V_{EB}	–3	Vdc
Collector Current – Continuous	I_C	4	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.71	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1)	$R_{\theta JC}$	1.4	°C/W

(1) Thermal resistance is determined under specified RF operating condition.

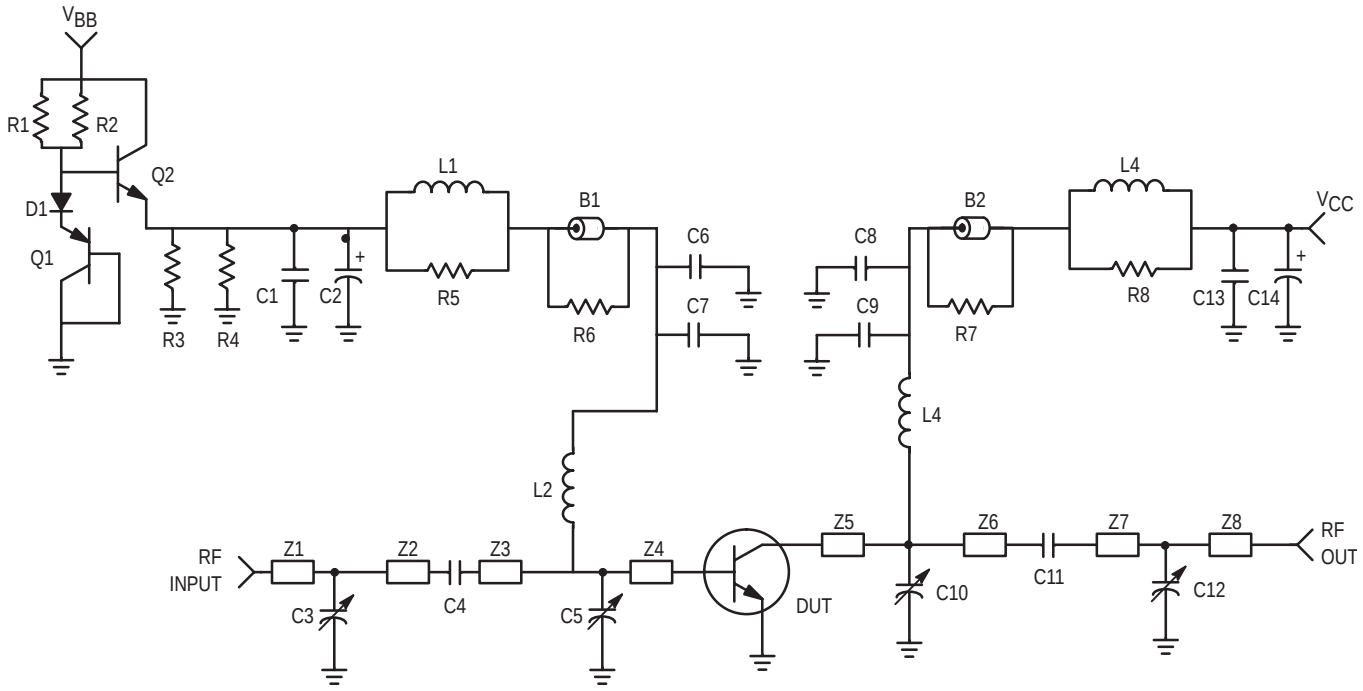
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	25	28	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	70	—	Vdc
Collector–Base Breakdown Voltage (I_C = 25 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	70	—	Vdc

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Emitter–Base Breakdown Voltage (I_B = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	3	3.8	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (V_{CE} = 5 Vdc, I_{CE} = 1 Adc)	h_{FE}	20	40	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 Vdc, I_E = 0, f = 1.0 MHz) (1)	C_{ob}	—	28	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 30 Watts, I_{CQ} = 120 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	G_{pe}	9.8	11	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 120 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	η	34	38	—	%
Intermodulation Distortion (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 120 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	IMD	—	– 30	– 28	dBc
Input Return Loss (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 125 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	IRL	10	17	—	dB
Load Mismatch (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 120 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz, Load VSWR = 3:1, All Phase Angles at Frequency of Test)	ψ	No Degradation in Output Power			
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 125 mA, f_1 = 1930.0 MHz, f_2 = 1930.1 MHz)	G_{pe}	—	11	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 125 mA, f_1 = 1930.0 MHz, f_2 = 1930.1 MHz)	η	—	34	—	%
Intermodulation Distortion (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 125 mA, f_1 = 1930.0 MHz, f_2 = 1930.1 MHz)	IMD	—	– 32	—	dBc
Input Return Loss (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 125 mA, f_1 = 1930.0 MHz, f_2 = 1930.1 MHz)	IRL	—	14	—	dB
GUARANTEED BUT NOT TESTED (In Motorola Test Fixture)					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 30 Watts, I_{CQ} = 125 mA, f = 1880 MHz)	G_{pe}	—	10.5	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 30 Watts , I_{CQ} = 125 mA, f = 1880 MHz)	η	—	40	—	%
Input Return Loss (V_{CC} = 26 Vdc, P_{out} = 30 Watts , I_{CQ} = 125 mA, f = 1880 MHz)	IRL	—	14	—	dB
Output Mismatch Stress (V_{CC} = 25 Vdc, P_{out} = 30 Watts, I_{CQ} = 125 mA, f = 1880 MHz, VSWR = 3:1, All Phase Angles at Frequency of Test)	ψ	Typically No Degradation in Output Power			

(1) For Information Only. This Part Is Collector Matched.



B1, B2	Ferrite Bead, P/N 5659065/3B, Ferroxcube	N1, N2	Type N Flange Mount RF Connector MA/COM 3052–1648–10
C1, C13	0.1 μF, Chip Capacitor, Kermet		
C2	100 μF, 50 V, Electrolytic Capacitor, Mallory	R1, R2	130 Ω, 1/8 W Chip Resistor, Rohm
C3, C5, C12	0.6–4 pF, Variable Capacitor, Johanson, Gigatrim	R3, R4	100 Ω, 1/8 W Chip Resistor, Rohm
C4, C11	10 pF, B Case Chip Capacitor, ATC	R5, R8	10 Ω, 1/2 W Resistor
C6, C8	24 pF, B Case Chip Capacitor, ATC	R6, R7	10 Ω, 1/8 W Chip Resistor, Rohm (10J)
C7, C9	75 pF, B Case Chip Capacitor, ATC	Q1	Transistor, PNP Motorola (BD136)
C10	0.4–2.5 pF, Variable Capacitor, Johanson, Gigatrim	Q2	Transistor, NPN Motorola (MJD47)
C14	470 μF, 63 V, Electrolytic Capacitor, Mallory	Board	30 Mil Glass Teflon®, Arlon GX–0300–55–22, ε_r = 2.55
D1	Diode, Motorola (MUR3160T3)		
L1, L4	12 Turns, 22 AWG, IDIA. 0.195″		
L2, L3	0.750″ 20 AWG		

Figure 1. Class AB Test Fixture Electrical Schematic

TYPICAL CHARACTERISTICS

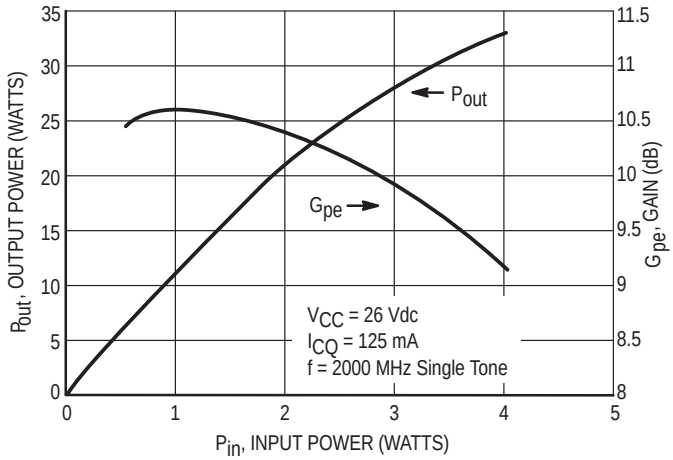


Figure 2. Output Power & Power Gain versus Input Power

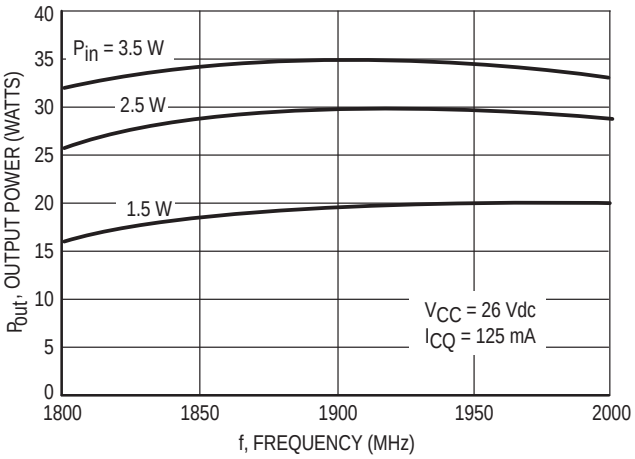


Figure 3. Output Power versus Frequency

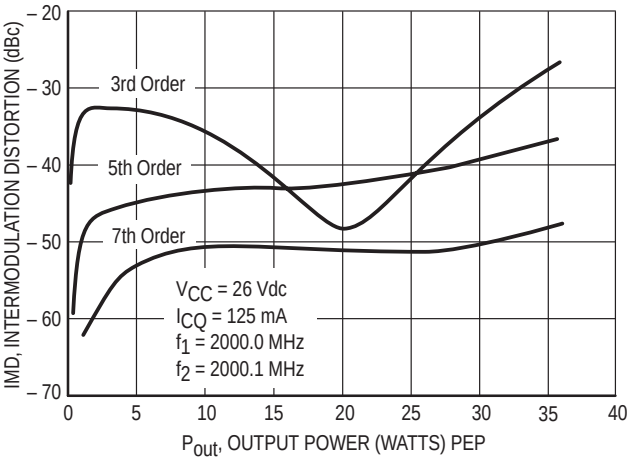


Figure 4. Intermodulation Distortion versus Output Power

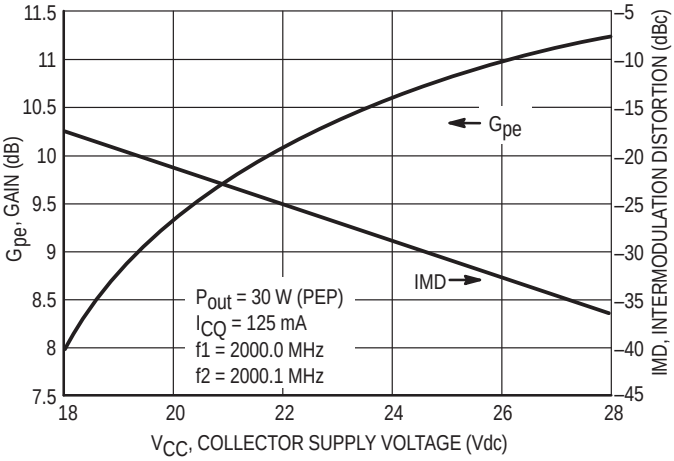


Figure 5. Power Gain and Intermodulation Distortion versus Supply Voltage

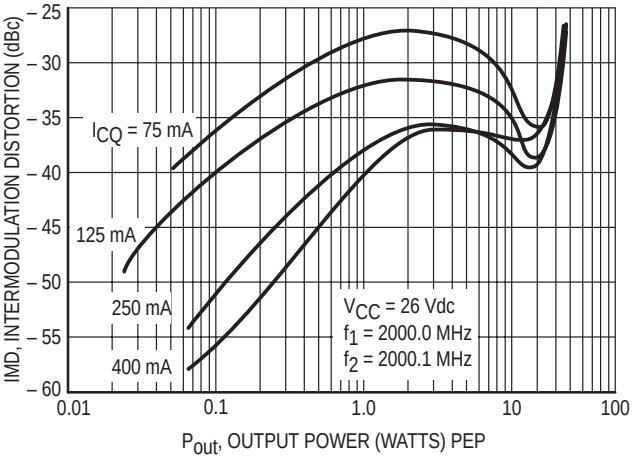


Figure 6. Intermodulation Distortion versus Output Power

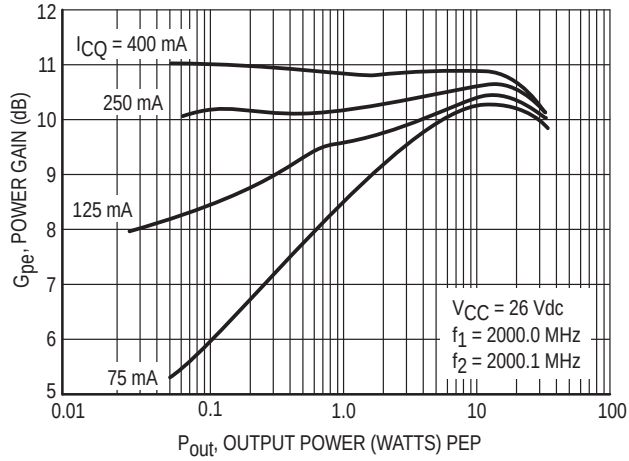


Figure 7. Power Gain versus Output Power

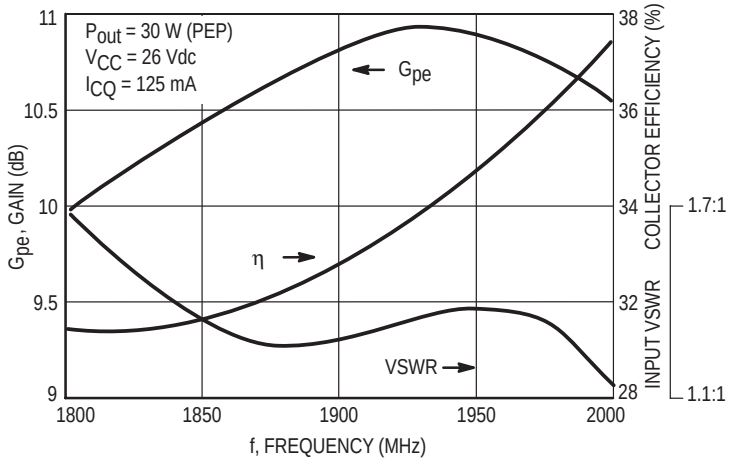
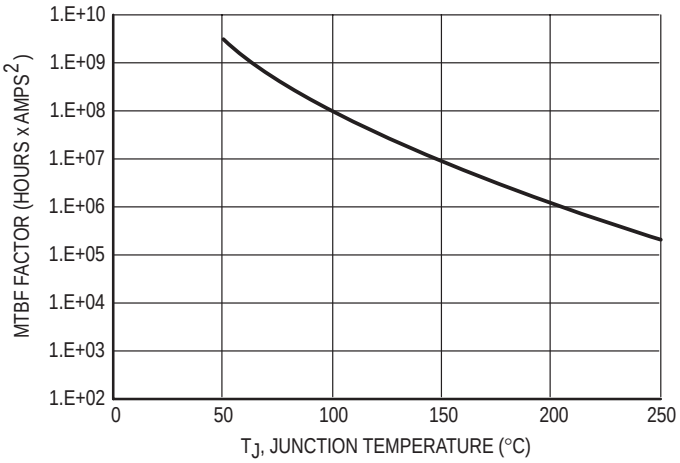
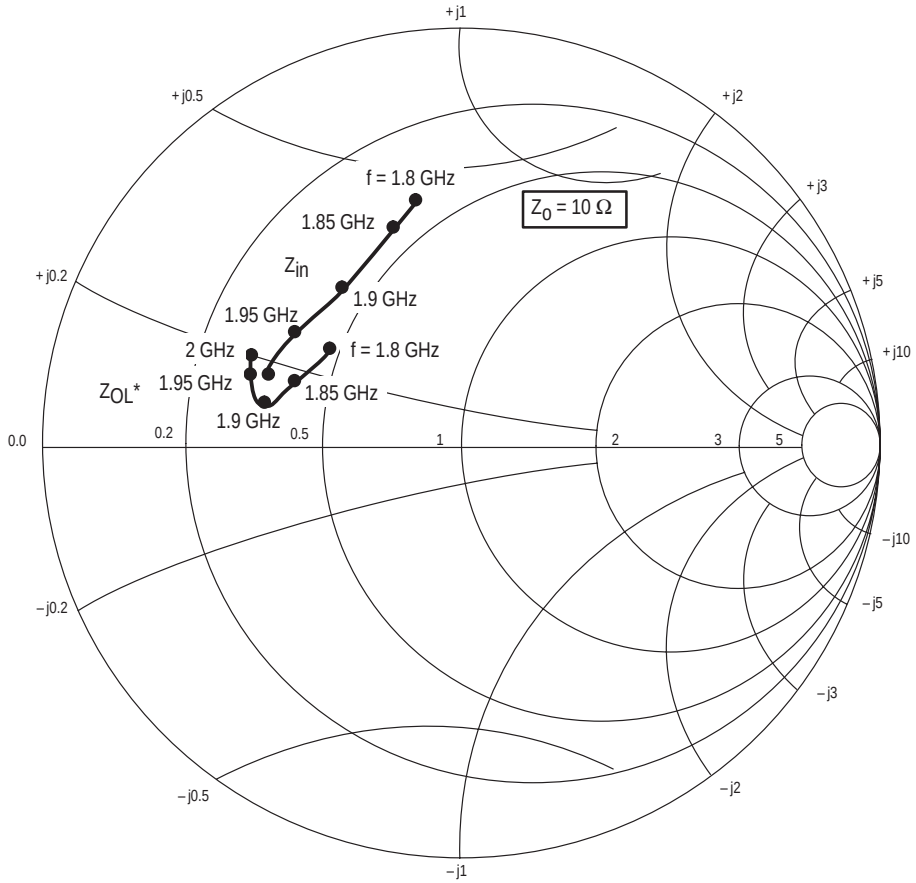


Figure 8. Performance in Broadband Circuit



This above graph displays calculated MTBF in hours x ampere^2 emitter current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTBF factor by I_C^2 for MTBF in a particular application.

Figure 9. MTBF Factor versus Junction Temperature



V_{CC} = 26 V, I_{CQ} = 125 mA, P_{out} = 30 W (PEP)

f MHz	$Z_{in}(1)$ Ω	Z_{OL}* Ω
1800	4.5 + j7.0	4.7 + j2.4
1850	4.5 + j6.0	4.4 + j1.6
1900	4.5 + j4.6	3.4 + j1.2
1950	3.7 + j2.4	3.3 + j1.6
2000	3.5 + j1.5	3.5 + j2.0

$Z_{in}(1)$ = Conjugate of fixture base impedance.

Z_{OL}* = Conjugate of the optimum load impedance at given output power, voltage, bias current and frequency.

Figure 10. Series Equivalent Input and Output Impedence

Table 1. Common Emitter S–Parameters at V_{CE} = 24 Vdc, I_C = 1.8 Adc

f GHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
1.5	.964	158	.65	74	.046	60	.859	161
1.55	.960	156	.74	68	.047	56	.841	161
1.6	.952	155	.87	60	.049	53	.815	160
1.65	.933	153	1.05	50	.048	46	.787	161
1.7	.892	149	1.32	35	.047	40	.744	163
1.75	.804	149	1.64	13	.040	29	.719	168
1.8	.727	157	1.78	–18	.026	21	.778	175
1.85	.787	163	1.50	–50	.015	54	.883	174
1.9	.873	163	1.14	–73	.020	81	.937	171
1.95	.921	160	.84	–89	.026	88	.949	168
2	.941	157	.62	–102	.031	93	.950	165
2.05	.943	155	.48	–109	.036	93	.946	164
2.1	.940	153	.38	–118	.040	92	.942	163
2.15	.928	151	.30	–127	.042	97	.939	162
2.2	.917	150	.24	–133	.049	99	.935	161
2.25	.907	150	.20	–140	.056	101	.933	160
2.3	.888	148	.17	–150	.066	100	.926	159
2.35	.861	148	.14	–159	.077	98	.916	157
2.4	.853	149	.11	–167	.087	92	.909	157
2.45	.860	146	.10	–176	.095	89	.900	155
2.5	.880	146	.10	156	.119	84	.880	155

The RF Sub–Micron Bipolar Line

RF Power Bipolar Transistors

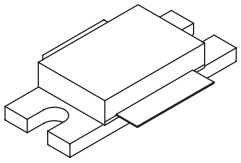
MRF20060R
MRF20060RS

60 W, 2000 MHz
RF POWER
BROADBAND
NPN BIPOLAR

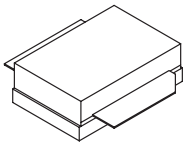
The MRF20060R and MRF20060RS are designed for class AB broadband commercial and industrial applications at frequencies from 1800 to 2000 MHz. The high gain, excellent linearity and broadband performance of these devices make them ideal for large–signal, common emitter class AB amplifier applications. These devices are suitable for frequency modulated, amplitude modulated and multi–carrier base station RF power amplifiers.

- Guaranteed Two–tone Performance at 2000 MHz, 26 Volts
  Output Power — 60 Watts (PEP)
  Power Gain — 9 dB
  Efficiency — 33%
  Intermodulation Distortion — –30 dBc
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- Capable of Handling 3:1 VSWR @ 26 Vdc, 2000 MHz, 60 Watts (PEP) Output Power
- Designed for FM, TDMA, CDMA and Multi–Carrier Applications
- Test Fixtures Available at: http://mot–sps.com/rf/designtds/

Note: Not suitable for class A operation.



CASE 451–06, STYLE 1
(MRF20060R)



CASE 451A–03, STYLE 1
(MRF20060RS)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage (I_B = 0 mA)	V_{CEO}	25	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Collector–Emitter Voltage (R_{BE} = 100 Ohm)	V_{CER}	30	Vdc
Base–Emitter Voltage	V_{EB}	– 3	Vdc
Collector Current – Continuous	I_C	8	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

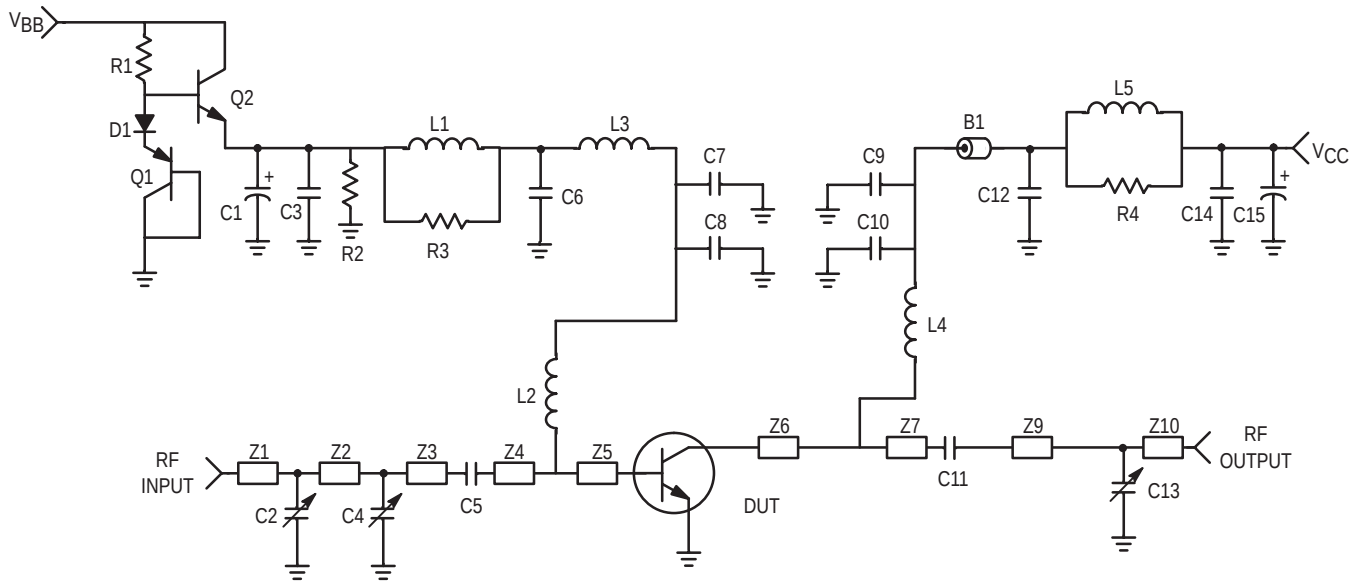
THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	25	28	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	69	—	Vdc
Collector–Base Breakdown Voltage (I_C = 50 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	69	—	Vdc
Reverse Base–Emitter Breakdown Voltage (I_B = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3	3.5	—	Vdc
Zero Base Voltage Collector Leakage Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (V_{CE} = 5 Vdc, I_C = 1 Adc)	h_{FE}	20	40	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 Vdc, I_E = 0, f = 1.0 MHz) (1)	C_{ob}	—	55	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	G_{pe}	9	9.8	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	η	33	35	—	%
Intermodulation Distortion (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	IMD	—	– 32	– 30	dB
Input Return Loss (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	IRL	12	19	—	dB
Output Mismatch Stress (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz, VSWR = 3:1, All Phase Angles at Frequency of Test)	ψ	No Degradation in Output Power			

(1) For Information Only. This Part Is Collector Matched.



B1	Ferrite Bead, P/N 5659065/3B, Ferroxcube	D1	Diode, Motorola (MURS160T3)
C1	100 μF, 50 V, Electrolytic Capacitor, Mallory	L1, L5	12 Turns, 22 AWG, 0.140″ Choke
C2, C4, C13	0.6–4.0 pF, Variable Capacitor, Gigatrim, Johanson	L2, L4	.5 inch of 20 AWG
C3, C14	0.1 μF, Chip Capacitor, Kemit	L3	12.5 nH Inductor
C5	15 pF, B Case Chip Capacitor, ATC	R1	2 x 130 Ω, 1/8 W Chip Resistor, Rohm
C6, C12	1000 pF, B Case Chip Capacitor, ATC	R2	2 x 100 Ω, 1/8 W Chip Resistor, Rohm
C7, C9	91 pF, B Case Chip Capacitor, ATC	R3, R4	10 Ω, 1/2 W, Resistor
C8, C10	24 pF, B Case Chip Capacitor, ATC	Q1	Transistor, PNP Motorola (BD136)
C11	13 pF, B Case Chip Capacitor, ATC	Q2	Transistor, NPN Motorola (MJD47)
C15	470 μF, 50 V, Electrolytic Capacitor, Mallory	Board	Glass Teflon®, Arlon GX–0300–55–22, ε_r

Figure 1. 1.93 – 2 GHz Test Fixture Electrical Schematic

TYPICAL CHARACTERISTICS

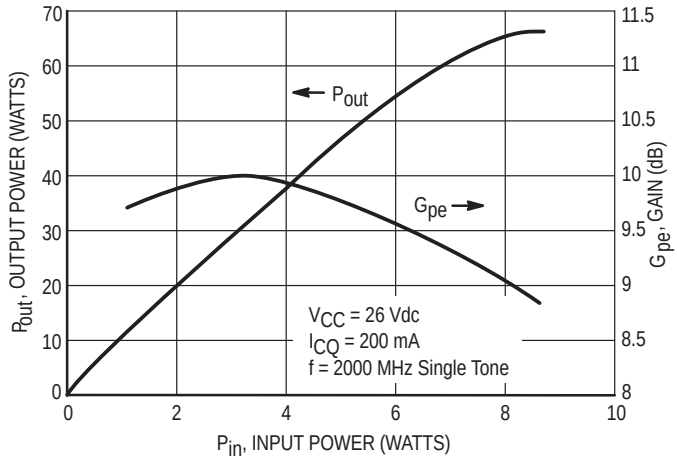


Figure 2. Output Power & Power Gain versus Input Power

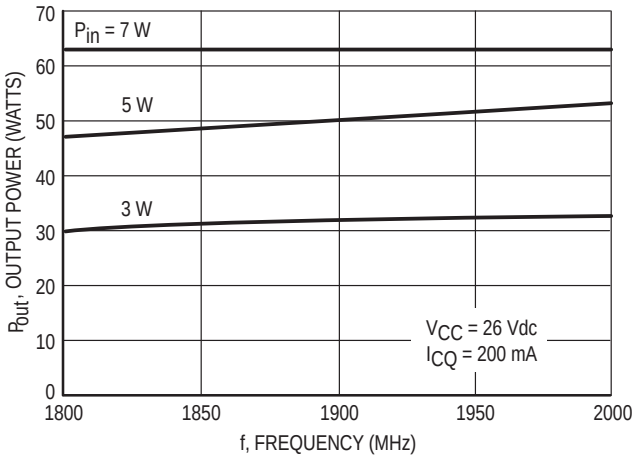


Figure 3. Output Power versus Frequency

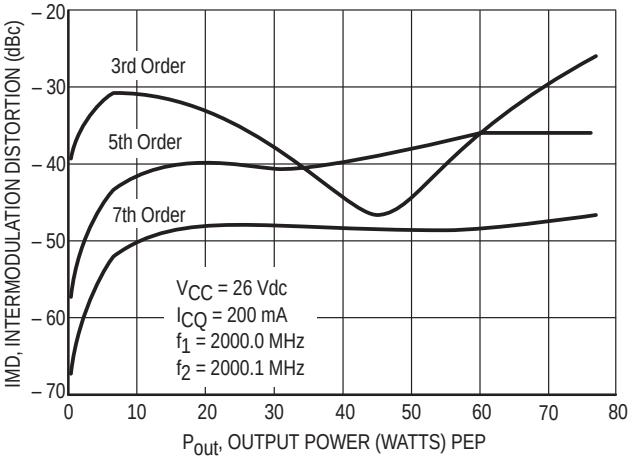


Figure 4. Intermodulation Distortion versus Output Power

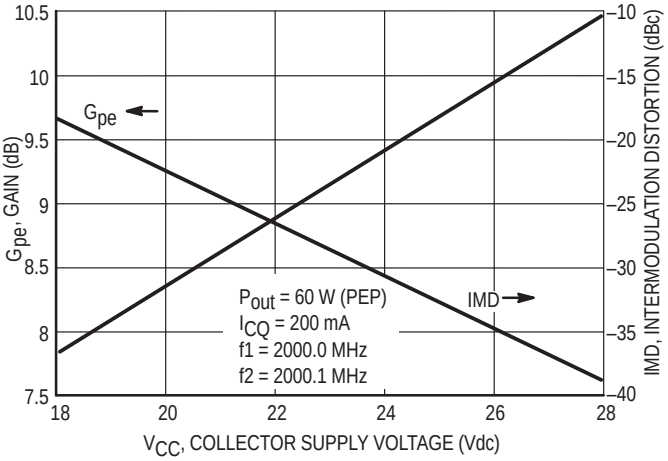


Figure 5. Power Gain and Intermodulation Distortion versus Supply Voltage

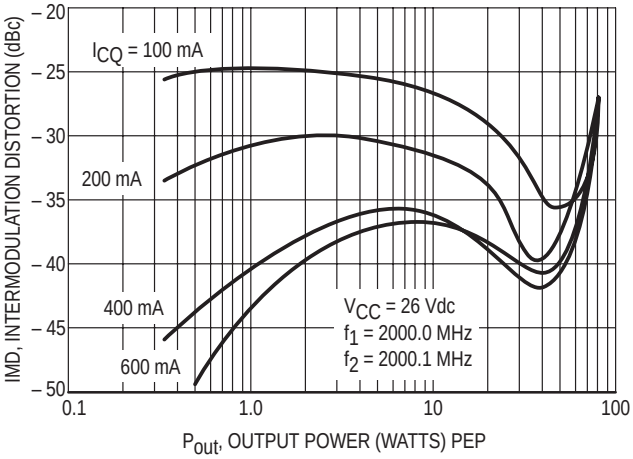


Figure 6. Intermodulation Distortion versus Output Power

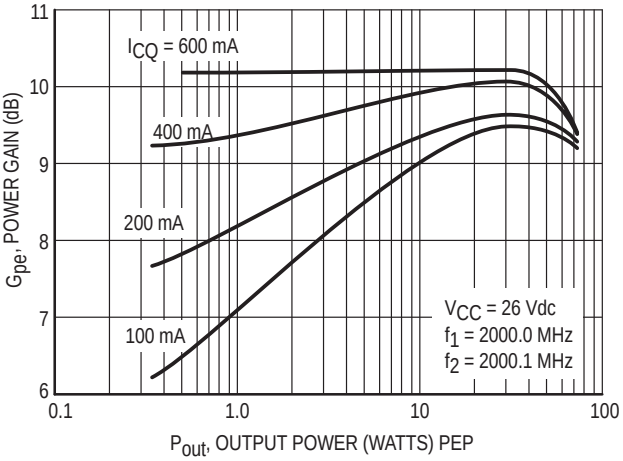


Figure 7. Power Gain versus Output Power

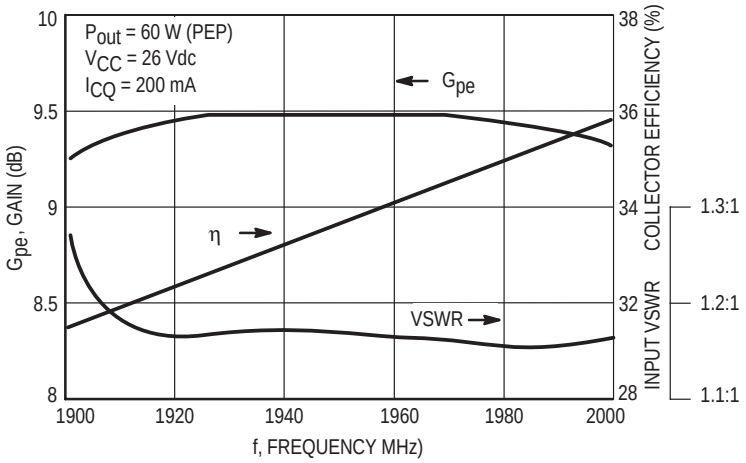
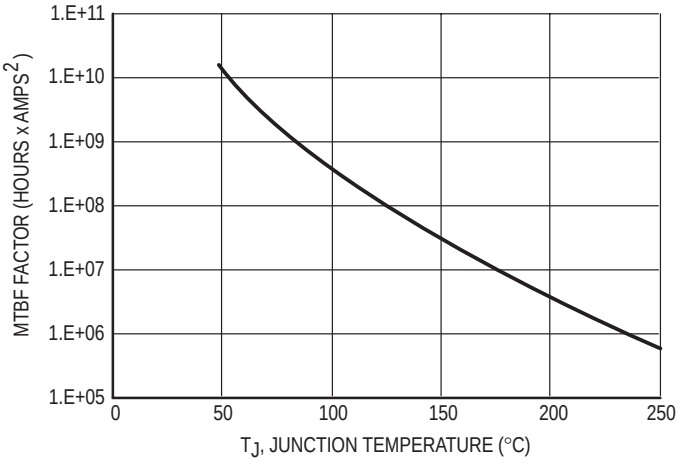
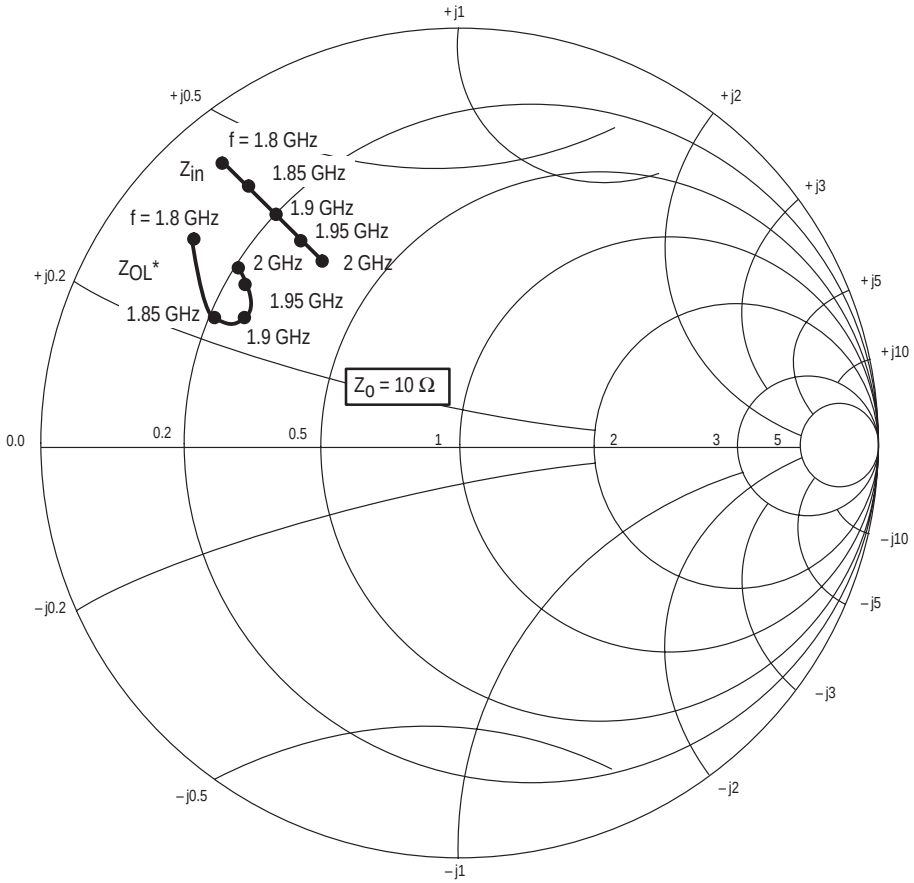


Figure 8. Performance in Broadband Circuit



This above graph displays calculated MTBF in hours x ampere^2 emitter curent. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTBF factor by I_C^2 for MTBF in a particular application.

Figure 9. MTBF Factor versus Junction Temperature



V_{CC} = 26 V, I_{CQ} = 200 mA, P_{out} = 60 W (PEP)

f MHz	$Z_{in}(1)$ Ω	Z_{OL}^* Ω
1800	1.0 + j4.8	1.7 + j3.3
1850	1.5 + j4.8	2.2 + j2.7
1900	2.0 + j4.7	2.4 + j3.0
1950	2.5 + j4.7	2.3 + j3.2
2000	3.5 + j4.7	2.0 + j3.4

$Z_{in}(1)$ = Conjugate of fixture base terminal impedance.

Z_{OL}^* = Conjugate of the optimum load impedance at given output power, voltage, bias current and frequency.

Figure 10. Series Equivalent Input and Output Impedence

Table 1. Common Emitter S–Parameters at V_{CE} = 24 Vdc, I_C = 3.5 Adc

f GHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
1.5	0.986	168	0.32	81	0.031	60	0.923	169
1.55	0.985	167	0.35	76	0.031	63	0.918	169
1.6	0.981	167	0.40	70	0.032	61	0.908	169
1.65	0.973	166	0.45	63	0.030	53	0.897	169
1.7	0.968	165	0.52	56	0.033	50	0.889	168
1.75	0.951	163	0.62	46	0.028	47	0.880	169
1.8	0.914	161	0.76	32	0.027	39	0.871	170
1.85	0.851	161	0.91	12	0.024	26	0.863	171
1.9	0.789	164	1.02	–15	0.015	5	0.888	174
1.95	0.810	170	0.94	–44	0.005	–7	0.931	174
2	0.880	172	0.75	–68	0.006	–151	0.953	172
2.05	0.934	170	0.57	–85	0.010	152	0.967	170
2.1	0.964	168	0.45	–98	0.015	158	0.965	169
2.15	0.977	165	0.36	–109	0.022	164	0.955	168
2.2	0.975	163	0.30	–118	0.033	165	0.950	167
2.25	0.961	161	0.25	–128	0.049	160	0.947	167
2.3	0.942	160	0.22	–139	0.066	149	0.938	166
2.35	0.919	157	0.19	–149	0.077	142	0.931	165
2.4	0.860	156	0.17	–163	0.100	137	0.922	165
2.45	0.821	159	0.15	177	0.128	122	0.914	165
2.5	0.781	161	0.14	157.0	0.156	108	0.907	165

The RF MOSFET Line

RF Power Field Effect Transistors

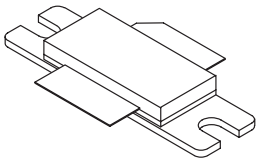
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21060
MRF21060S

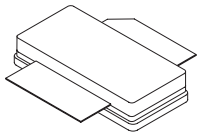
60 W, 2170 MHz, 28 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

Designed for PCN and PCS base station applications from frequencies up to 2.1 to 2.2 GHz. Suitable for W–CDMA, CDMA, TDMA, GSM and multicarrier amplifier applications.

- Typical W–CDMA Performance: 2140 MHz, 28 Volts
  5 MHz Offset @ 4.096 MHz BW, 15 DTCH
  Output Power — 6.0 Watts
  Power Gain — 12.5 dB
  Drain Efficiency — 15%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection: Class 2 Human Body Model, Class M3
  Machine Model
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2.11 GHz, 60 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 465–04, STYLE 1
(MRF21060)



CASE 465A–04, STYLE 1
(MRF21060S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ $T_C \geq = 25°C$ Derate above 25°C	P_D	180 0.98	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

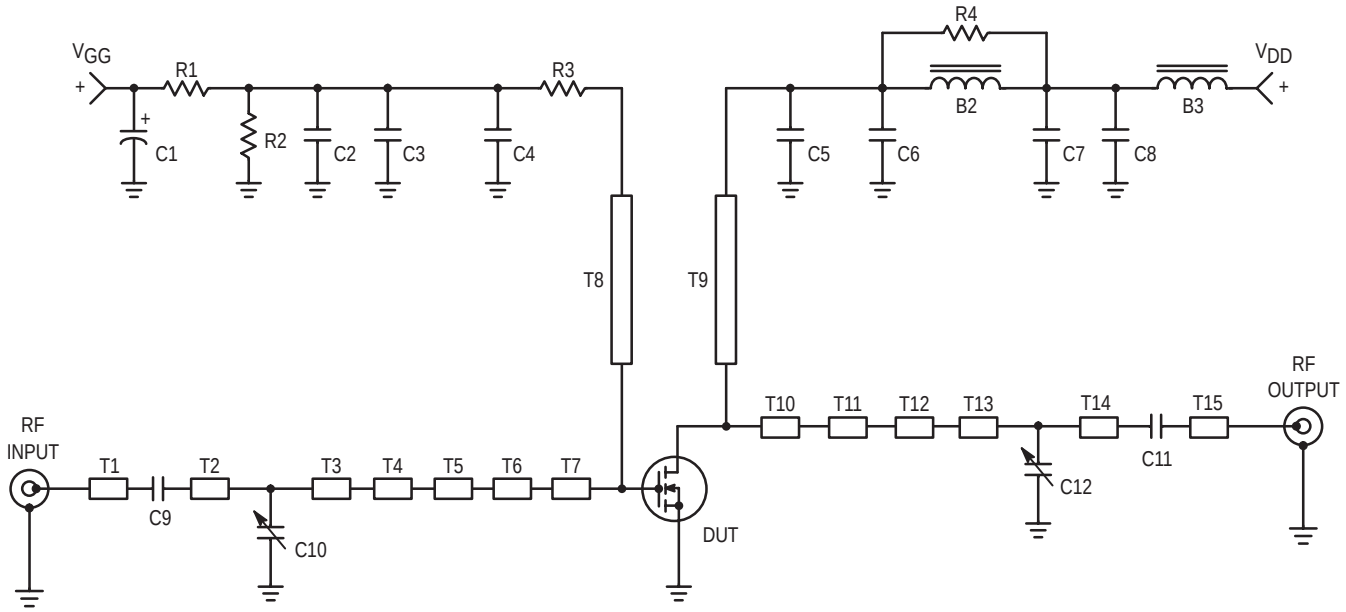
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.02	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.27	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	4.7	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	G_{ps}	11	12.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	η	31	34	—	%
3rd Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	IMD	—	–30	–28	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 28 Vdc, P_{out} = 60 W CW, f = 2170 MHz)	P1dB	—	60	—	W
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA, f = 2110 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B2 – B3	Ferrite Bead, Fair Rite, 2743019447	T3	0.180″ x 0.100″ Microstrip
C1	10 μF, 50 V Electrolytic, ECEV1HV100R Panasonic	T4	0.152″ x 0.293″ Microstrip
C2, C7	1000 pF, B Case Chip Capacitor, 100B102JCA500X, ATC	T5	0.216″ x 0.100″ Microstrip
C3, C8	0.10 μF, B Case Chip Capacitor, CDR33BX104AKWS, Kemet	T6	0.114″ x 0.410″ Microstrip
C4, C5	4.7pF, B Case Chip Capacitor, 100B4R7JCA500X, ATC	T7	0.626″ x 0.872″ Microstrip
C6	22 μF, 35 V Tantalum, SMT, Sprague	T8	1.050″ x 0.050″ Microstrip
C9, C11	9.1 pF, B Case Chip Capacitor, 100B9R1JCA500X, ATC	T9	0.830″ x 0.050″ Microstrip
C10	0.8 pF – 8.0 pF, Variable Capacitor, Johanson Gigatrim	T10	0.596″ x 1.040″ Microstrip
C12	0.4 pF – 4.5 pF, Variable Capacitor, Johanson Gigatrim	T11	0.186″ x 0.315″ Microstrip
R1	1 kΩ, 1/4 W, Fixed Film Chip Resistor, 0.08″ x 0.13″	T12	0.097″ x 0.525″ Microstrip
R2	560 kΩ, 1/4 W, Fixed Film Chip Resistor, 0.08″ x 0.13″	T13	0.353″ x 0.138″ Microstrip
R3	10 Ω, 1/4 W, Fixed Film Chip Resistor, 0.08″ x 0.13″	T14	0.112″ x 0.080″ Microstrip
R4	10 Ω, 1/4 W, Fixed Film Chip Resistor, 0.08″ x 0.13″	T15	0.722″ x 0.080″ Microstrip
T1	0.743″ x 0.080″ Microstrip	Board	0.030″ Glass Teflon®, Arlon
T2	0.070″ x 0.100″ Microstrip		GX–0300–55–22, 2 oz Cu

Figure 1. MRF21060 Schematic

TYPICAL CHARACTERISTICS

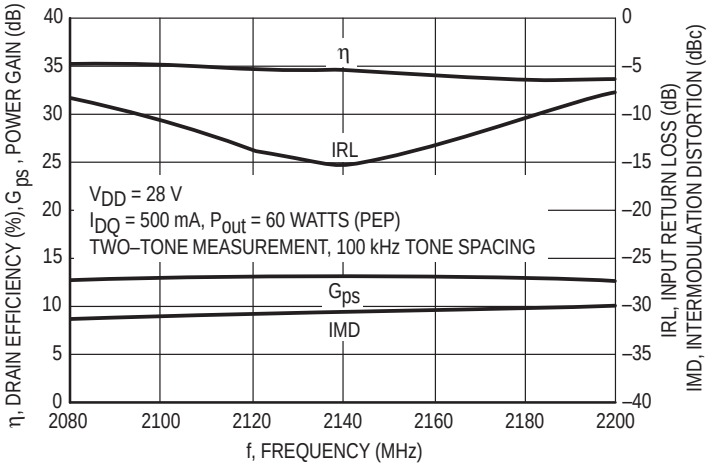


Figure 2. Class AB Broadband Circuit Performance

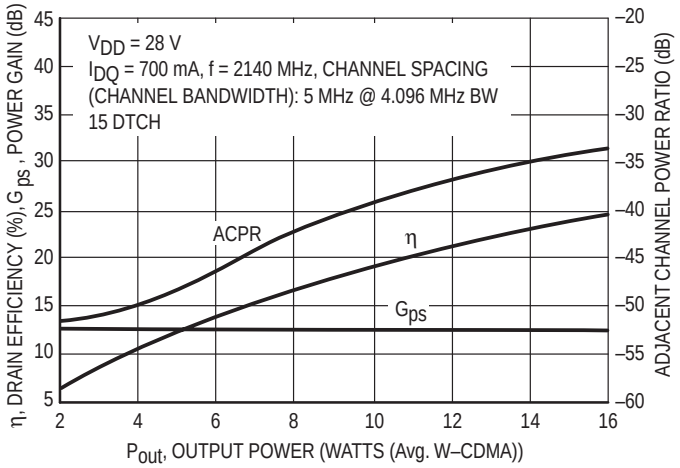


Figure 3. W–CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

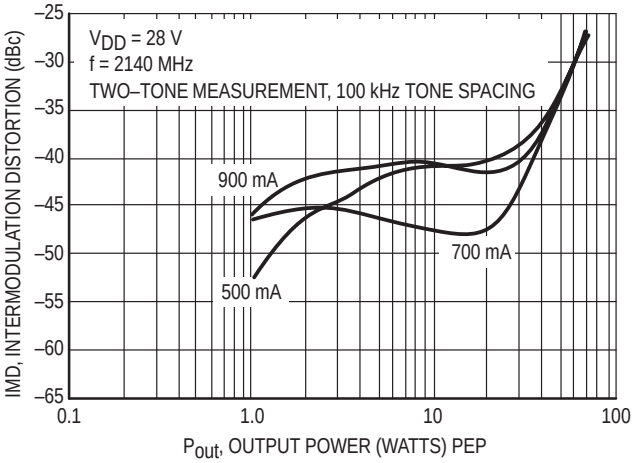


Figure 4. Intermodulation Distortion versus Output Power

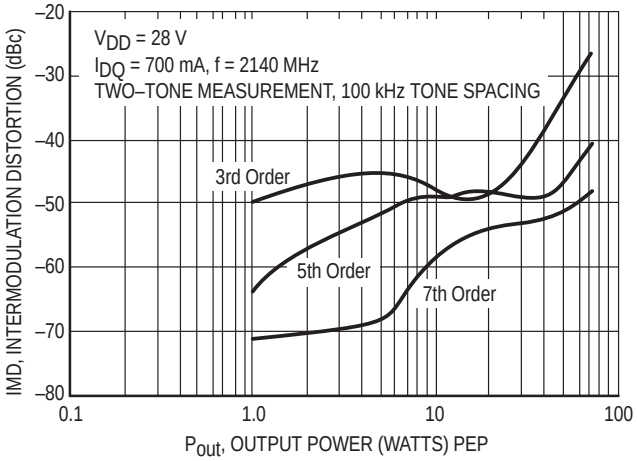


Figure 5. Intermodulation Products versus Output Power

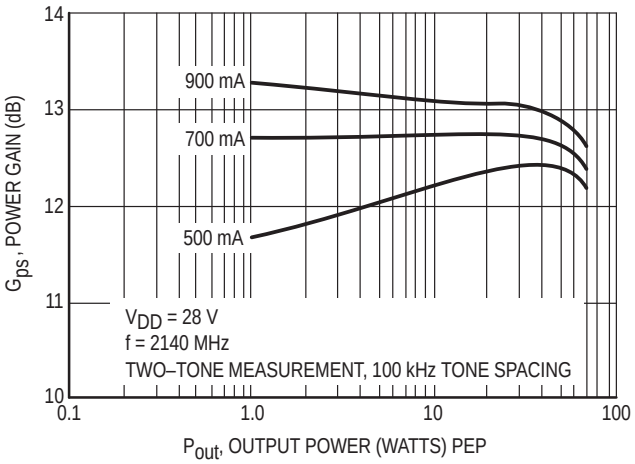


Figure 6. Power Gain versus Output Power

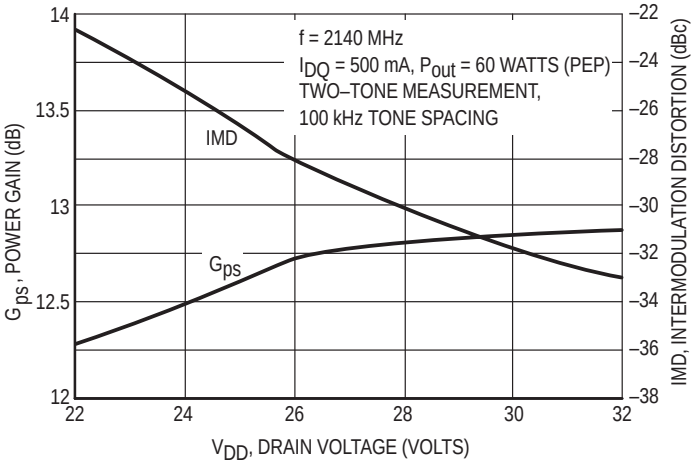
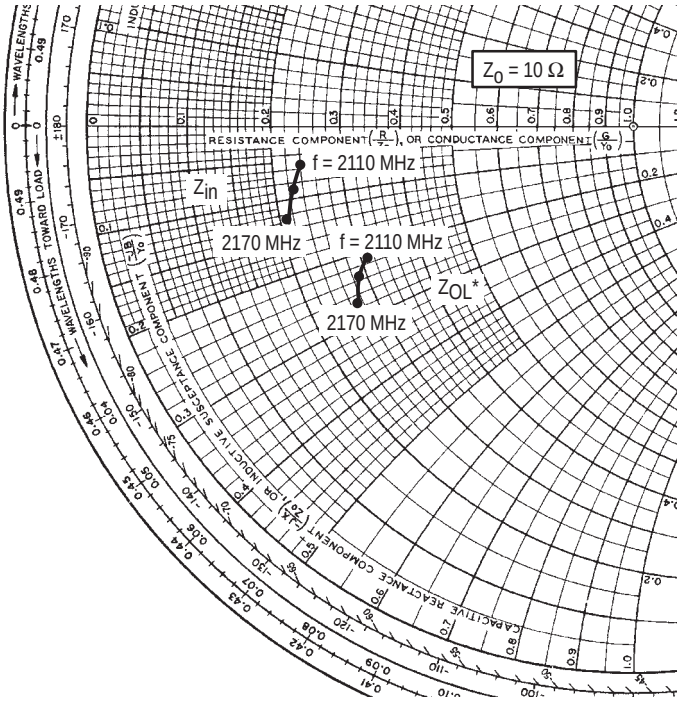


Figure 7. Power Gain and Intermodulation Distortion versus Supply Voltage



V_{DD} = 28 V, I_{DQ} = 500 mA, P_{out} = 60 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
2110	2.40 – j0.55	3.07 – j2.05
2140	2.26 – j0.87	2.89 – j2.38
2170	2.08 – j1.23	2.66 – j2.71

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

Figure 8. Series Equivalent Input and Output Impedance

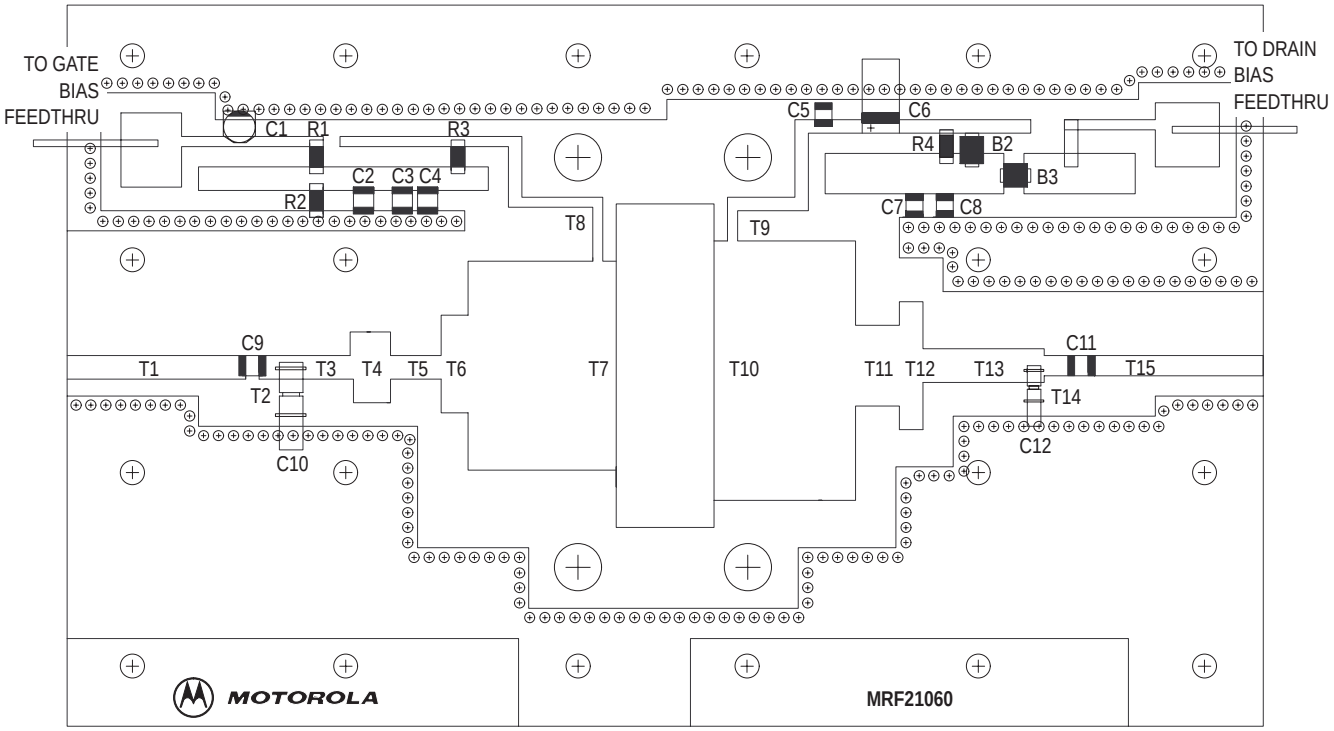


Figure 9. MRF21060 Populated PC Board Layout Diagram

The RF Line
NPN Silicon RF Power Transistor

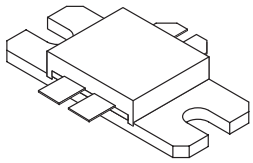
TPV8100B

150 W, 470 – 860 MHz
NPN SILICON
RF POWER TRANSISTOR

The TPV8100B is designed for output stages in band IV and V TV transmitter amplifiers. It incorporates high value emitter ballast resistors, gold metallizations and offers a high degree of reliability and ruggedness.

Including double input and output matching networks, the TPV8100B features high impedances. It can easily operate in a full 470 MHz to 860 MHz bandwidth in a single and simple circuit.

- To be used class AB for TV band IV and V.
- Specified 28 Volts, 860 MHz Characteristics
  Output Power = 125 Watts (peak sync.)
  Output Power = 100 Watts (CW)
  Minimum Gain = 8.5 dB
- Specified 32 Volts, 860 MHz Characteristics
  Output Power = 150 Watts (peak sync.)
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



CASE 398–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CER}	40	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Collector–Current — Continuous	I_C	12	Adc
Total Device Dissipation @ 25°C Case Derate above 25°C	P_D	215 1.25	Watts W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1)	$R_{\theta JC}$	0.8	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 10 mA, R_{be} = 75 Ω)	$V_{(BR)CER}$	30	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 10 mAdc)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector–Base Breakdown Voltage (I_E = 20 mAdc)	$V_{(BR)CBO}$	65	—	—	Vdc
Collector–Emitter Leakage (V_{CE} = 28 V, R_{be} = 75 Ω)	I_{CER}	—	—	10	mA

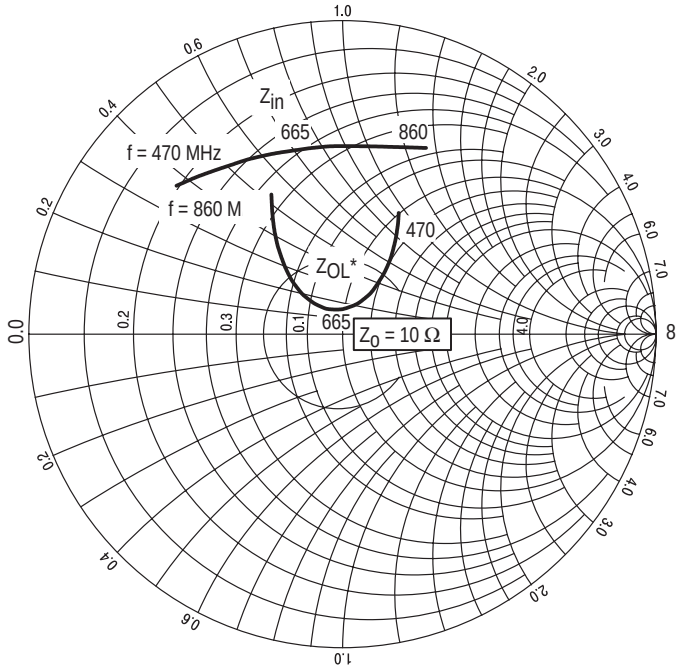
NOTE:
1. Thermal resistance is determined under specified RF operating condition.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 2 Adc, V_{CE} = 10 Vdc)	h_{FE}	30	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (each side) (2) (V_{CB} = 28 V, I_E = 0, f = 1 MHz)	C_{ob}	—	44	—	pF
FUNCTIONAL TESTS IN CW (SOUND)					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 V, P_{out} = 100 W, I_{CQ} = 2 x 50 mA, f = 860 MHz)	G_p	8.5	9.5	—	dB
Collector Efficiency (V_{CC} = 28 V, P_{out} = 100 W, I_Q = 2 x 50 mA, f = 860 MHz)	η	55	58	—	%
Output Power @ 1 dB Compression (P_{ref} = 25 W) (V_{CC} = 28 V, I_{CQ} = 2 x 50 mA, f = 860 MHz)	P_{out}	100	110	—	W
FUNCTIONAL TESTS IN VIDEO (STANDARD BLACK LEVEL)					
Peak Output Power (synch.) (V_{CC} = 28 V, I_{CQ} = 2 x 50 mA, f = 860 MHz)	P_{out}	125	135	—	W
Peak Output Power (synch.) (V_{CC} = 32 V, I_{CQ} = 2 x 25 mA, f = 860 MHz)	P_{out}	150	160	—	W
Recommended Quiescent Current	I_{CQ}	—	—	2 x 0.3	A

NOTE:
2. Value of "C_{ob}" is that of die only. It is not measurable in TPV8100B because of internal matching network.



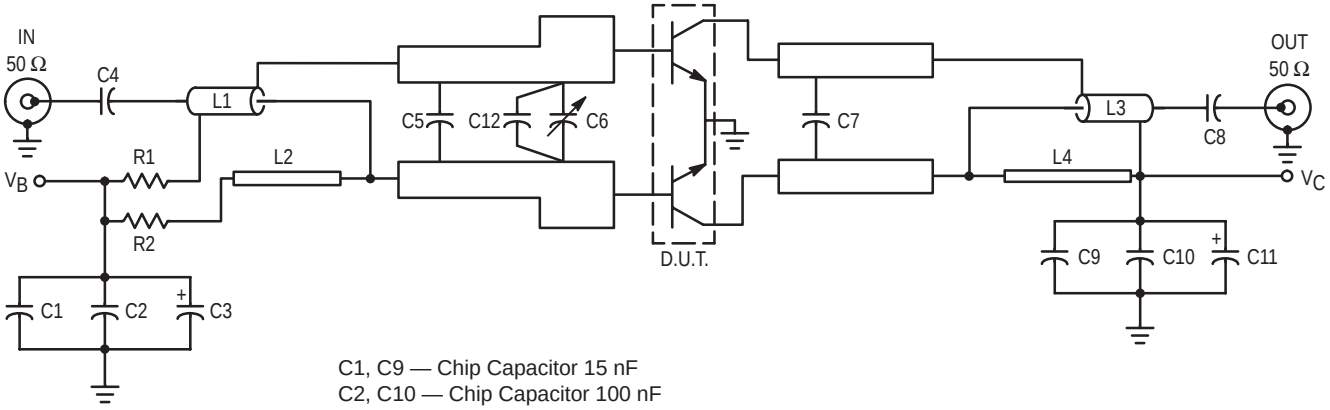
f (MHz)	Z_{in} (Ohms)	Z_{OL}* (Ohms)
470	1.95 + j3.67	10.0 + j9.50
665	3.65 + j6.82	9.23 + j1.30
860	6.66 + j13.8	4.45 + j5.22

Z_{OL}* = Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

NOTE: Z_{in} & Z_{OL}* are given from base–to–base and collector–to–collector respectively.

Input and Output impedances with circuit tuned for maximum linearity @ V_{CC} = 28 V / I_{CQ} = 2 x 50 mA / P_{out} = 100 W

Figure 1. Series Equivalent Input/Output Impedances



C1, C9 — Chip Capacitor 15 nF
C2, C10 — Chip Capacitor 100 nF
C3, C11 — Chip Capacitor 100 μF/40 V
C4 — Chip Capacitor 15 pF ATC 100A
C5 — Chip Capacitor 5.6 pF ATC 100A
C6 — Trimmer Capacitor 1–4 pF
C7 — Chip Capacitor 12 pF ATC 100B
C8 — Chip Capacitor 15 pF ATC 100A
C12 — Chip Capacitor 12 pF ATC 100A
L1, L3 — Coaxial Wire 25 Ω/85 Mils/40 mm
L2, L4 — Printed Board Inductance
R1, R2 — Chip Resistor 1 Ω 0805 5%

Figure 2. Test Circuit

TYPICAL CHARACTERISTICS

CW — WIDEBAND

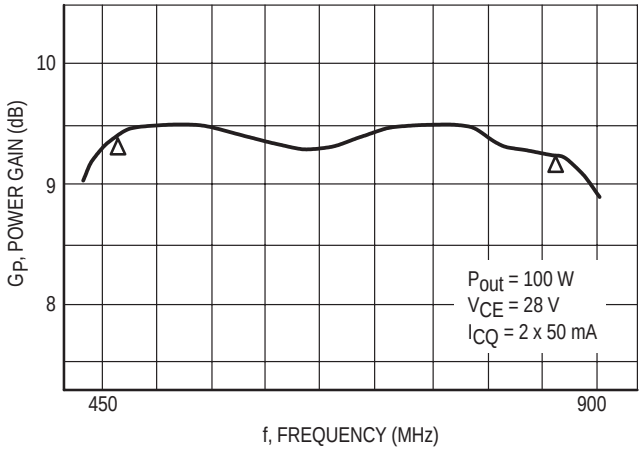


Figure 3. Power Gain versus Frequency

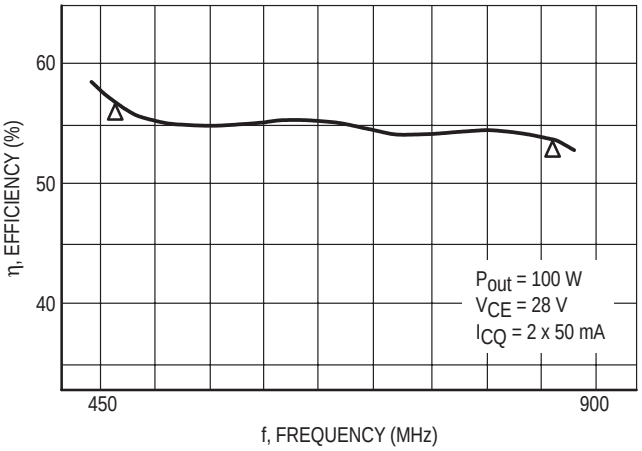


Figure 4. Collector Efficiency versus Frequency

TYPICAL VIDEO CHARACTERISTICS @ f = 800 MHz
V_{CE} = 28 V

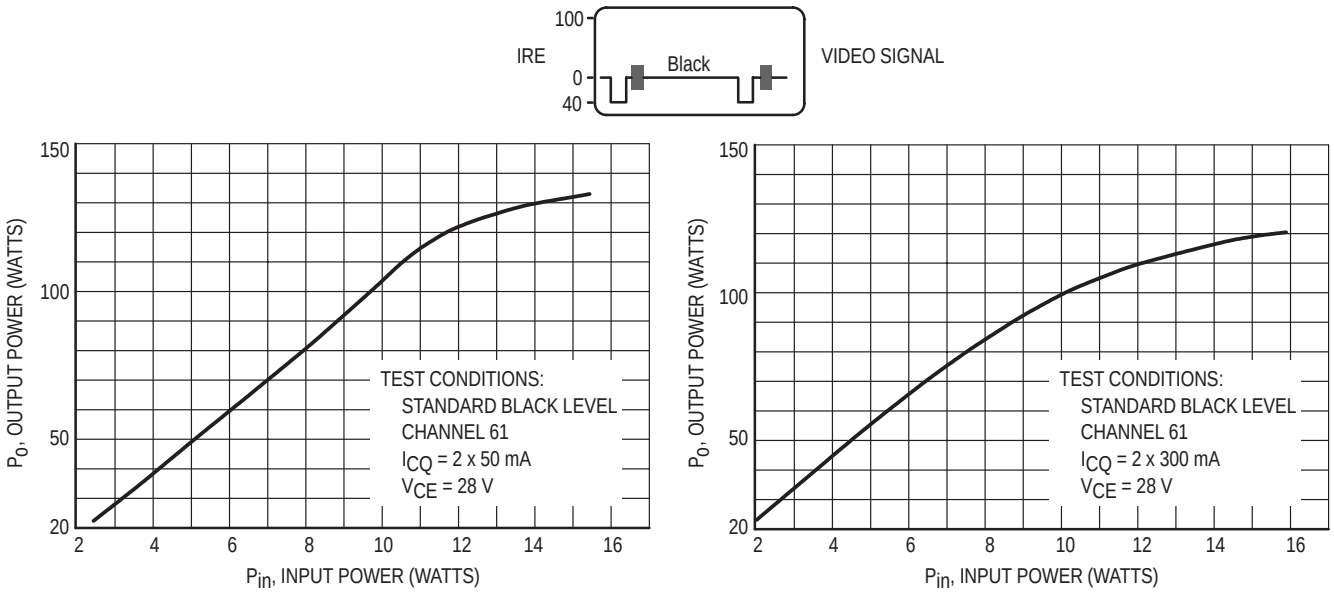


Figure 5. Peak Output Power versus Peak Input Power

Figure 6. Peak Output Power versus Peak Input Power

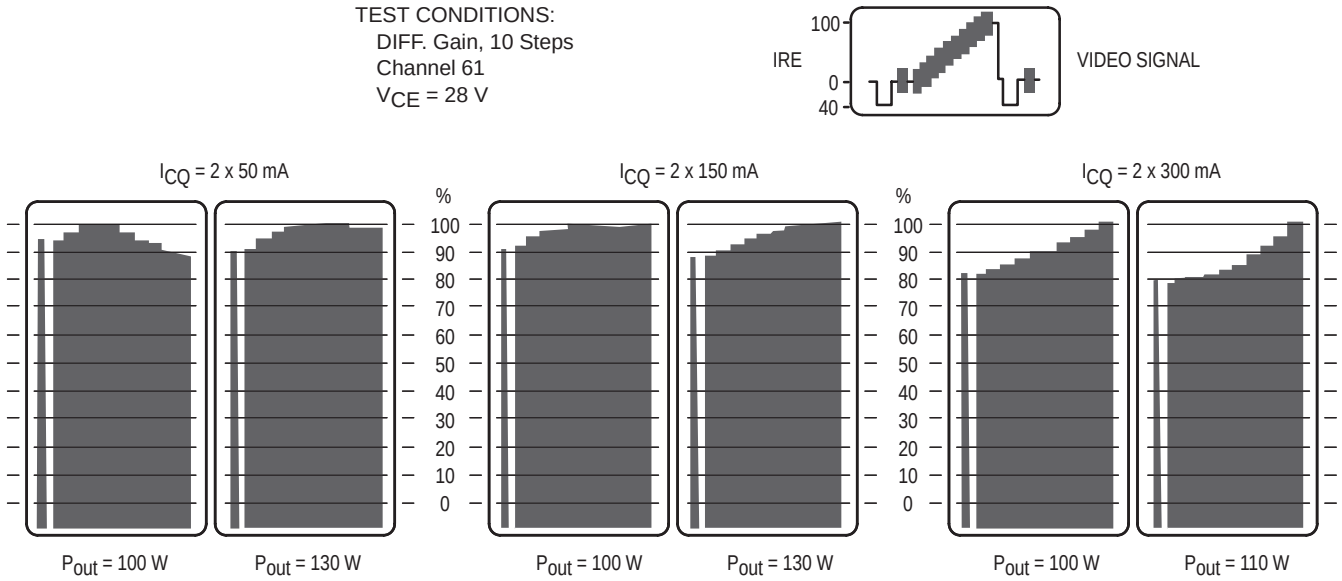
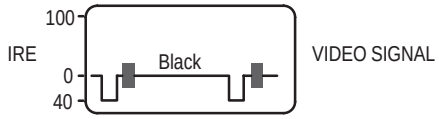
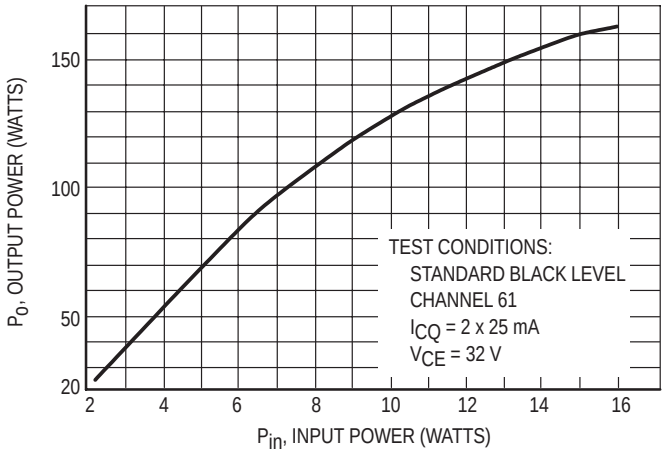


Figure 7. Gain versus Output Power

TYPICAL VIDEO CHARACTERISTICS @ f = 800 MHz
V_{CE} = 32 V





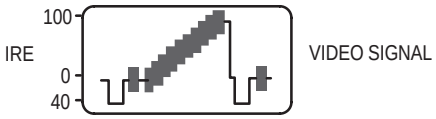
V_{CE} = 32 V, I_{CQ} = 2 x 25 mA

P_{out}	Gain
25 W	10.6 dB
50 W	11.1 dB
100 W	11.3 dB
120 W	11.1 dB
130 W	11.0 dB
140 W	10.7 dB
150 W	10.5 dB
160 W	10.2 dB

(see curve on left)

Figure 8. Peak Output Power versus Peak Input Power

TEST CONDITIONS:
DIFF. Gain, 10 Steps
Channel 61
V_{CE} = 32 V
I_{CQ} = 2 x 25 mA



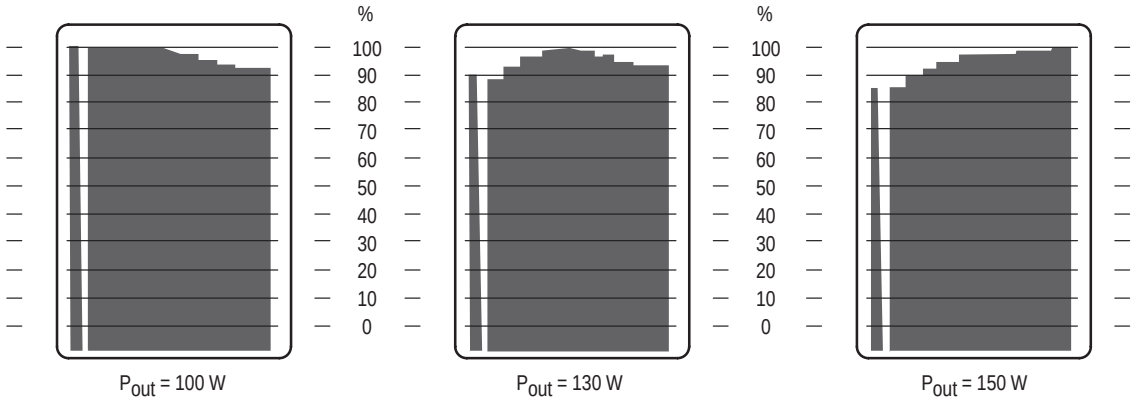


Figure 9. Differential Gain

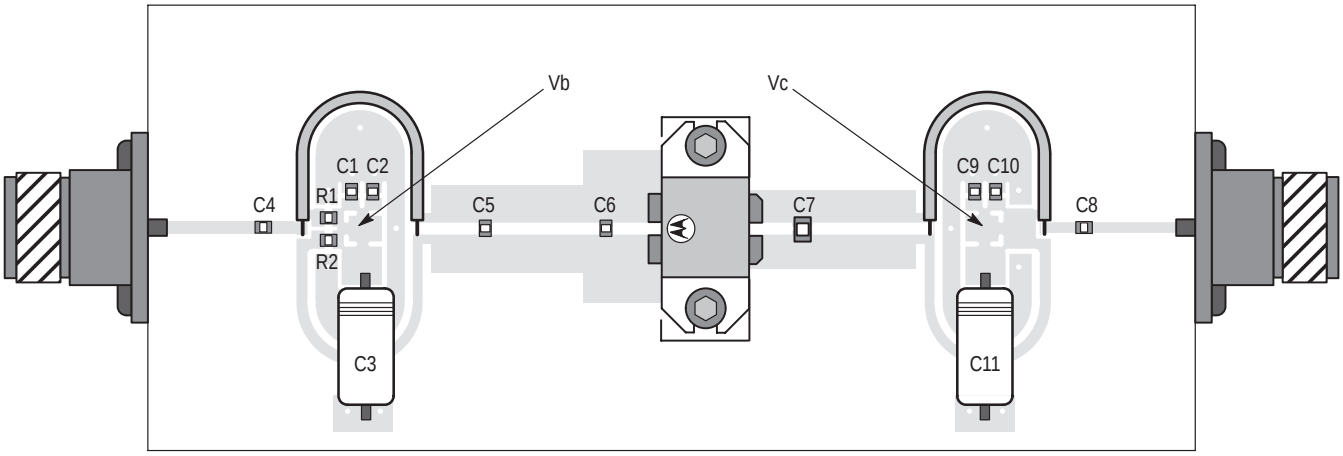


Figure 10. Components View

Chapter Six
RF Amplifier Modules

Section One 6.1–0
RF Amplifier Modules – Selector Guide

Section Two 6.2–0
RF Amplifier Modules – Data Sheets

Section One
Selector Guide

Motorola RF Amplifier Modules

Motorola's RF portfolio includes many hybrid designs optimized to perform either in narrowband base station transmitter applications, or in broadband linear amplifiers. Motorola modules feature two or more active transistors (LDMOS, GaAs, or Bipolar die technology) and their associated 50 ohm matching networks. Circuit substrate and metallization have been selected for optimum performance and reliability. For PA designers, hybrid modules offer the benefits of small and less complex system designs, in less time and at a lower overall cost.

Table of Contents

	Page
RF Amplifier Modules	6.1–1
Base Stations	6.1–2
Wideband Linear Amplifiers	6.1–3
Packages	6.1–4

Motorola RF Amplifier Modules/ICs

Complete amplifiers with 50 ohm input and output impedances are available for all popular base station transmitter systems, including GSM and CDMA, covering frequencies from 800 MHz up to 2.2 GHz.

Base Stations

Designed for applications such as macrocell drivers and microcell output stage, these class AB amplifiers are ideal for GSM base station systems at 900, 1800 and 1900 MHz, with power requirements up to 16 watts.

Table 1. Base Stations

Device	Frequency MHz	P_{out} Watts	Gain (Min) dB	Supply Voltage Volts	Class	System Application	Die Technology	Package/Style
MHVIC910L(46b)	921–960	10	22	26	AB	GSM900	LDMOS–IC	978/–
MHW1810–1	1805–1880	10	24	26	AB	GSM1800	LDMOS	301AW/1
MHW1810–2	1805–1880	10	32	26	AB	GSM1800	LDMOS	301AW/1
MHW1815	1805–1880	15	30	26	AB	GSM1800	Silicon Bipolar	301AK/1
MHW1910–1	1930–1990	10	24	26	AB	GSM1900	LDMOS	301AW/1
MHW1915	1930–1990	15	29	26	AB	GSM1900	Silicon Bipolar	301AK/1

Table 2. Base Station Drivers

These 50 ohm amplifiers are recommended for modern multi–tone CDMA, TDMA and UMTS base station pre–driver applications. Their high third–order intercept point, tight phase and gain control, and excellent group delay characteristics make these devices ideal for use in high–power feedforward loops.

Ultra–Linear (for CDMA, W–CDMA, TDMA, Analog) – Class A (Silicon Bipolar Die)

Device	Frequency Band MHz	V_{CC} (Nom.) Volts	I_{CC} (Nom.) mA	Gain (Nom.) dB	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept (Typ) dBm	NF (Typ) dB	Case/ Style
MHL9128	800–960	28	400	20	0.5	31	43	7.5	448/1

Ultra–Linear (for CDMA, W–CDMA, TDMA, Analog) – Class A (LDMOS Die) – Lateral MOSFETs

Device	Frequency Band MHz	V_{DD} (Nom.) Volts	I_{DD} (Nom.) mA	Gain (Nom.) dB	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept (Typ) dBm	NF (Typ) dB	Case/ Style
MHL9838★	800–925	28	770	31	.1	39	50	3.7	301AP/1
MHL9236	800–960	26	550	30.5	.1	34	47	3.5	301AP/1
MHL9236M	800–960	26	550	30.5	.1	34	47	3.5	301AP/2
MHL9318★	860–900	28	500	17.5	.1	35.5	49	3.0	301AS/1
MHL19338★	1900–2000	28	500	30	.1	36	46	4.2	301AP/1
MHL19936(46b)	1900–2000	28	1400	30	.2	41	51	4.2	301AY/1
MHL21336(46a)	2100–2200	26	500	30	.15	35	45	4.5	301AP/1

Ultra–Linear (for CDMA, W–CDMA, TDMA, Analog) – Class A – GaAs FET

MHL9025(46b)	790–920	15	330	21.5	.25	31.5	48	2.5	438F/1

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

★New Product

Wideband Linear Amplifiers

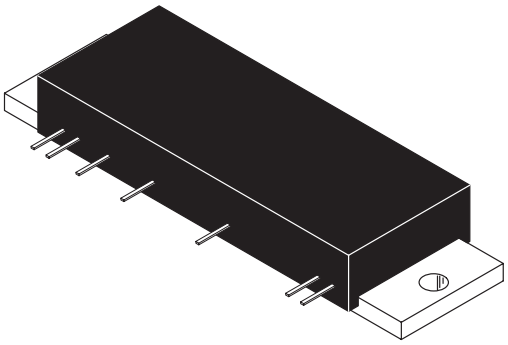
Table 1. Standard 50 Ohm Linear Hybrid

This series of RF linear hybrid amplifier has been optimized for wideband, 50 ohm applications. These amplifiers were designed for multi–purpose RF applications where linearity, dynamic range and wide bandwidth are of primary concern. The MHL series utilizes a new case style that provides microstrip input and output connections.

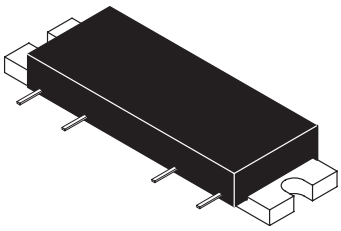
Device	Frequency Band MHz	V_{CC} (Nom.) Volts	I_{CC} (Nom.) mA	Gain/Freq. (Typ) dB/MHz	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept Point/Freq. (Typ) dBm/MHz	NF/Freq. (Typ) dB/MHz	Case/ Style
MHL8115	40–1000	15	700	17.5/900	1	30	41.5/1000	8.5/1000	448/2
MHL8118	40–1000	28	400	17.5/900	1	30	41.5/1000	8.5/1000	448/1

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

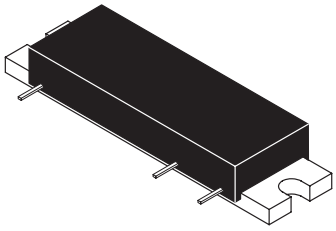
RF Amplifier Modules Packages



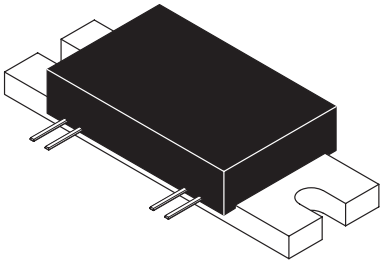
CASE 301AK
STYLE 1



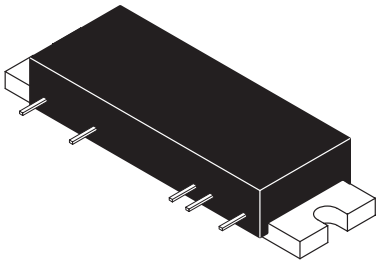
CASE 301AP
STYLE 1, 2



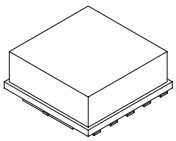
CASE 301AS
STYLE 1



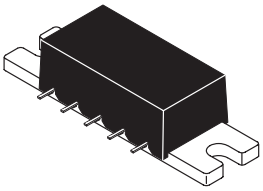
CASE 301AW
STYLE 1



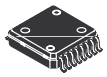
CASE 301AY
STYLE 1



CASE 438F
STYLE 1



CASE 448
STYLE 1, 2



CASE 978

Section Two

Motorola RF Amplifier Modules – Data Sheets

Device Number	Page Number
MHL8115	6.2–3
MHL8118	6.2–5
MHL9128	6.2–7
MHL9236	6.2–9
MHL9236M	6.2–9
MHL9318	6.2–12
MHL9838	6.2–15
MHL19338	6.2–18
MHW1810–1	6.2–19
MHW1810–2	6.2–19
MHW1815	6.2–25
MHW1910–1	6.2–27
MHW1915	6.2–31

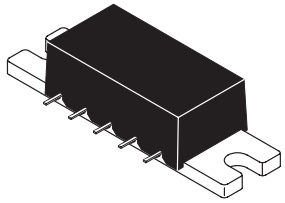
MHL8115

The RF Line
UHF Linear Amplifier

Designed for linear amplifier applications in 50 Ohm systems requiring wide bandwidth, low noise, and low distortion. Internal DC blocking on RF ports reduces external component count and related circuit area. This hybrid utilizes push–pull circuit design.

- Supply Voltage: 15 Vdc
- Third Order Intercept: 41.5 dBm Typ
- Power Gain: 17.5 dB Typ (@ 900 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- 50 Ohm Input/Output Impedances

1 W, 17.5 dB
50 – 1000 MHz
LINEAR AMPLIFIERS



CASE 448–02, STYLE 2

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	18	Vdc
RF Input Power	P_{in}	+20	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = +25°C; V_{CC} = 15 Vdc; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DC}	—	700	760	mA
Power Gain	(f = 900 MHz)	P_G	16.5	17.5	—	dB
Gain Flatness	(f = 50 – 1000 MHz)	FL	—	1.0	2.0	dB
Power Output @ 1 dB Comp.	(f = 900 MHz)	P_{out} 1 dB	29	30	—	dBm
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)		ITO	40.5	41.5	—	dBm
Input/Output VSWR	(f = 50 – 900 MHz) (f = 900 – 1000 MHz)	VSWR	— —	— —	2.0:1 2.6:1	
Noise Figure, Broadband	(f = 500 MHz) (f = 1000 MHz)	NF	— —	7.5 8.5	8.5 9.5	dB
Second Harmonic Distortion (P_o = 100 mW, f_{2H} = 1000 MHz)		dso	—	–55	–45	dB
Second Order Intermodulation Distortion (P_o = 2.75 dBm, f_1 = 373 MHz, f_2 = 450 MHz)		IM2	—	–65	–60	dB
Intermodulation Distortion, 3 Tone (f = 860 MHz, P_{sync} = 200 mW)		IM3	—	–60	—	dB

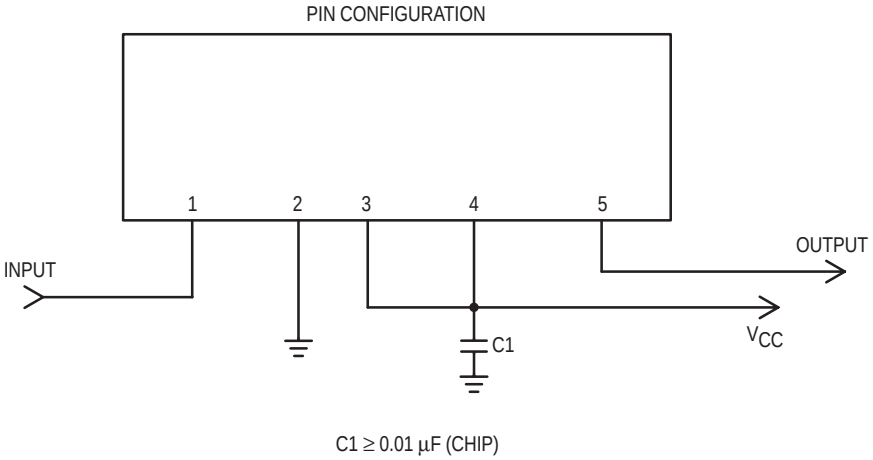


Figure 1. MHL8115 External Connections

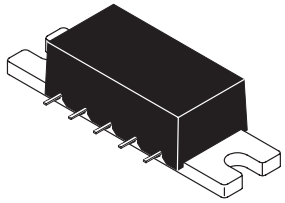
MHL8118

The RF Line
UHF Linear Amplifier

Designed for linear amplifier applications in 50 Ohm systems requiring wide bandwidth, low noise, and low distortion. Internal DC blocking on RF ports reduces external component count and related circuit area. This hybrid utilizes push–pull circuit design.

- Supply Voltage: 28 Vdc
- Third Order Intercept: 41.5 dBm Typ
- Power Gain: 17.5 dB Typ (@ 900 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- 50 Ohm Input/Output Impedances

1 W, 17.5 dB
50 – 1000 MHz
LINEAR AMPLIFIERS



CASE 448–02, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	32	Vdc
RF Input Power	P_{in}	+20	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = +25°C; V_{CC} = 28 Vdc; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DC}	—	400	440	mA
Power Gain	(f = 900 MHz)	P_G	16.5	17.5	—	dB
Gain Flatness	(f = 50 – 1000 MHz)	FL	—	1.0	2.0	dB
Power Output @ 1 dB Comp.	(f = 900 MHz)	P_{out} 1 dB	29	30	—	dBm
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)		ITO	40.5	41.5	—	dBm
Input/Output VSWR	(f = 50 – 900 MHz) (f = 900 – 1000 MHz)	VSWR	— —	— —	2.0:1 2.6:1	
Noise Figure, Broadband	(f = 500 MHz) (f = 1000 MHz)	NF	— —	7.5 8.5	8.5 9.5	dB
Second Harmonic Distortion (P_o = 100 mW, f_{2H} = 1000 MHz)		dso	—	–55	–45	dB
Second Order Intermodulation Distortion (P_o = 2.75 dBm, f_1 = 373 MHz, f_2 = 450 MHz)		IM2	—	–65	–60	dB
Intermodulation Distortion, 3 Tone (f = 860 MHz, P_{sync} = 200 mW)		IM3	—	–60	—	dB

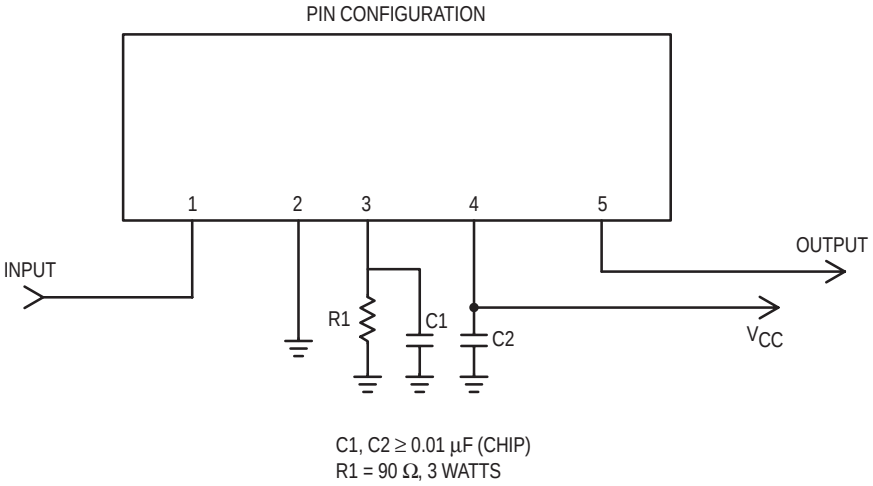


Figure 1. MHL8118 External Connections

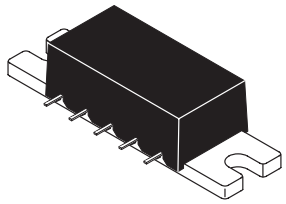
MHL9128

The RF Line
UHF Linear Amplifier

Designed specifically for linear amplifier applications in the cellular frequency band. Internal DC blocking on RF ports reduces external component count and related circuit area. This device can be easily combined for higher power applications.

- Supply Voltage: 28 Vdc
- Third Order Intercept: 43 dBm Typ
- Power Gain: 20 dB Typ (@ f = 900 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- 50 Ohm Input/Output Impedances

1.3 W, 20 dB
800–960 MHz
LINEAR AMPLIFIER



CASE 448–02, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise stated)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	32	Vdc
RF Input Power	P_{in}	+20	dBm
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 28 Vdc, T_C = 25°C; 50 Ω System, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DC}	400	—	440	mA
Power Gain (1)	(f = 900 MHz)	P_G	19	20	21	dB
Absolute Phase Variation (1)	(f = 900 MHz)	$\Delta\phi$		±8	±18	Deg.
Gain Flatness	(f = 800–960 MHz)	G_F	—	0.5	0.75	dB
Power Output @ 1 dB Comp.	(f = 900 MHz)	P_{out} 1 dB	30	31	—	dBm
Input VSWR	(f = 800–920 MHz) (f = 920–960 MHz)	$VSWR_{in}$	— —	1.25:1 1.50:1	1.5:1 1.9:1	
Output VSWR	(f = 800–960 MHz)	$VSWR_{out}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)		ITO	42	43	—	dBm
Noise Figure	(f = 960 MHz)	NF	—	7.5	9.5	dB

(1) Consult factory for tighter gain and/or phase windows.

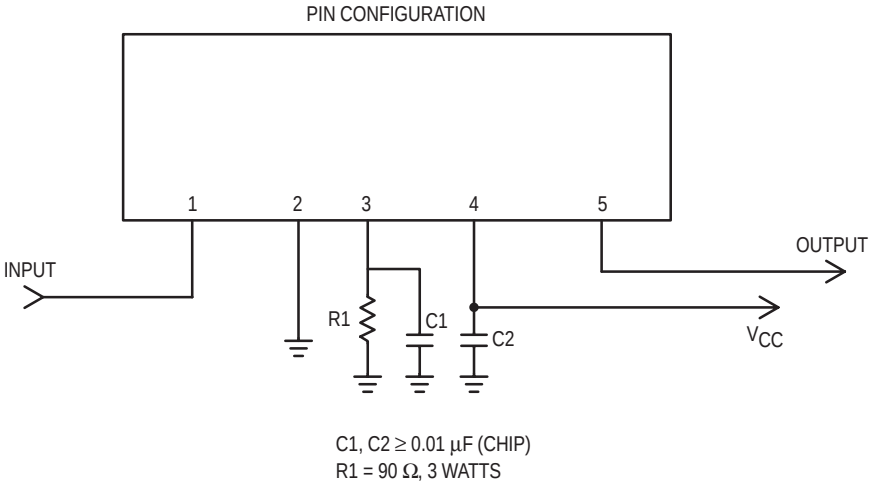


Figure 1. MHL9128 External Connections (Case 448–02, Style 1)

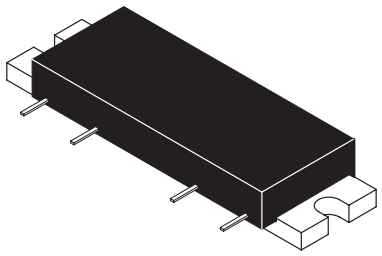
MHL9236
MHL9236M

The RF Line
Cellular Band Linear Amplifiers

Designed for ultra–linear amplifier applications in 50 ohm systems operating in the cellular frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for the most demanding analog or digital modulation systems, such as TDMA, CDMA or QPSK.

- Third Order Intercept: 47 dBm Typ
- Power Gain: 30.5 dB Typ (@ f = 880 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications
- For Use in TDMA, CDMA, QPSK or Analog Systems

2.5 W, 30.5 dB
800 – 960 MHz
LINEAR AMPLIFIERS



CASE 301AP–01 STYLE 1, 2

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+10	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 26 Vdc, T_C = 25°C; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	550	620	mA
Power Gain	(f = 880 MHz)	P_G	29.5	30.5	31.5	dB
Gain Flatness	(f = 800 – 960 MHz)	G_F	—	0.1	0.3	dB
Power Output @ 1 dB Comp.	(f = 880 MHz)	P_{out} 1 dB	33.0	34.0	—	dBm
Input VSWR	(f = 800 – 960 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Output VSWR	(f = 800 – 960 MHz)	$VSWR_{out}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)		ITO	46.0	47.0	—	dBm
Noise Figure	(f = 800–960 MHz)	NF	—	3.5	4.5	dB

TYPICAL CHARACTERISTICS

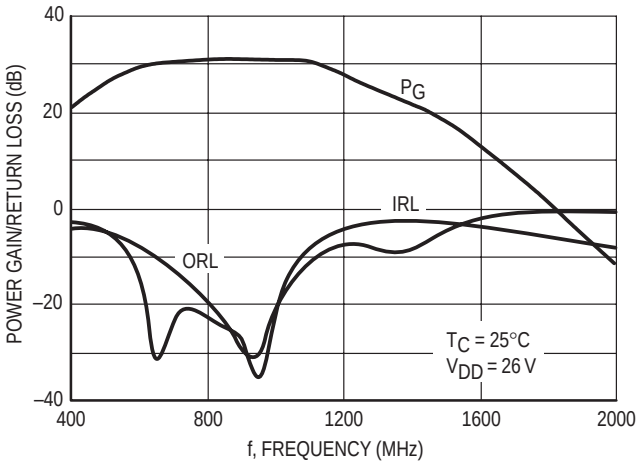


Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency

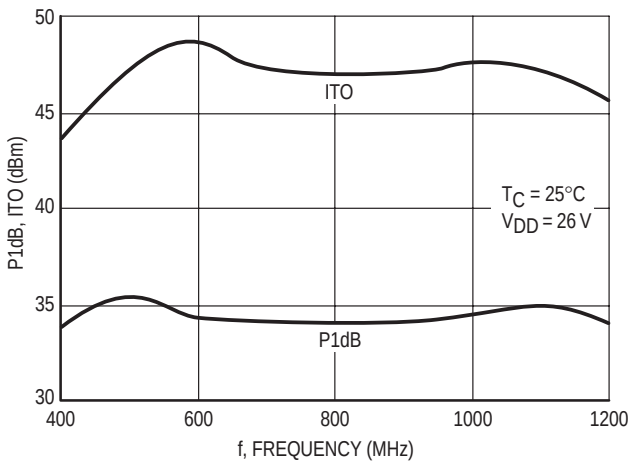


Figure 2. P1dB, ITO versus Frequency

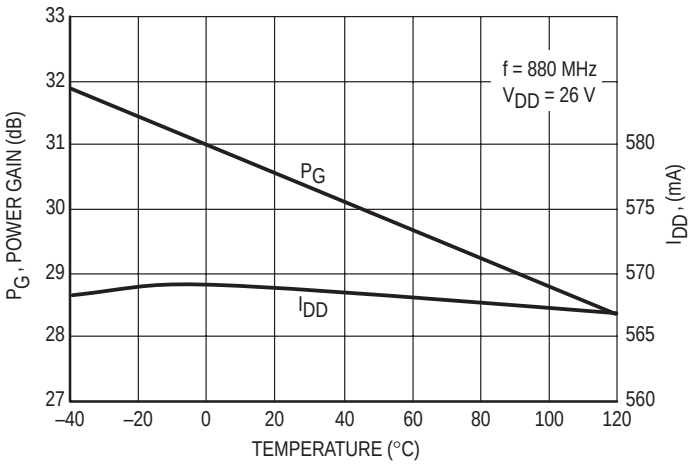


Figure 3. Power Gain, I_{DD} versus Temperature

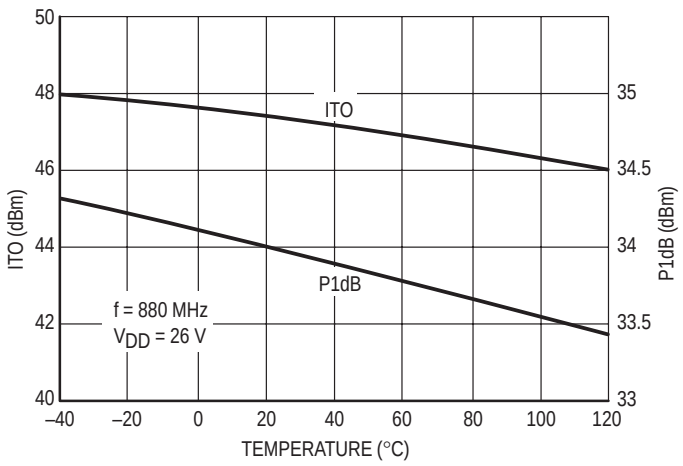


Figure 4. ITO, P1dB versus Temperature

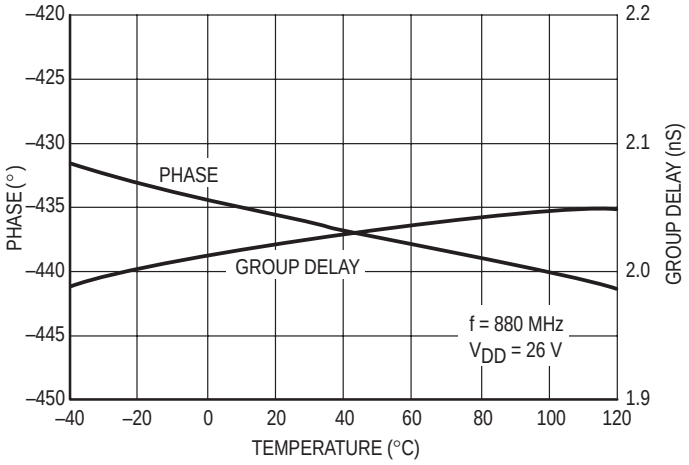


Figure 5. Phase(1), Group Delay(1) versus Temperature

(1)In Production Test Fixture

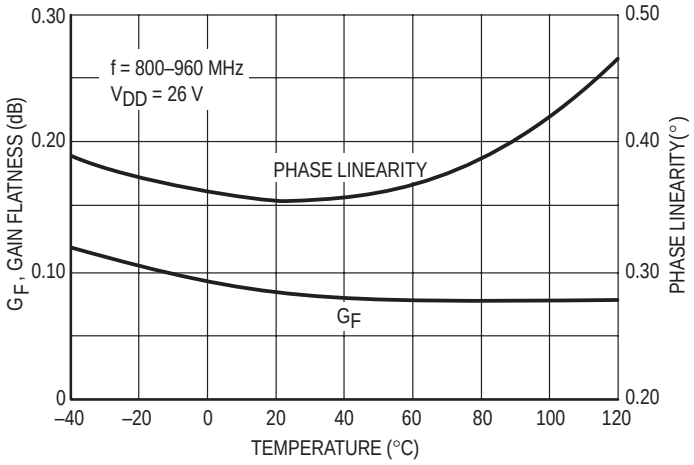


Figure 6. Gain Flatness, Phase Linearity versus Temperature

TYPICAL CHARACTERISTICS

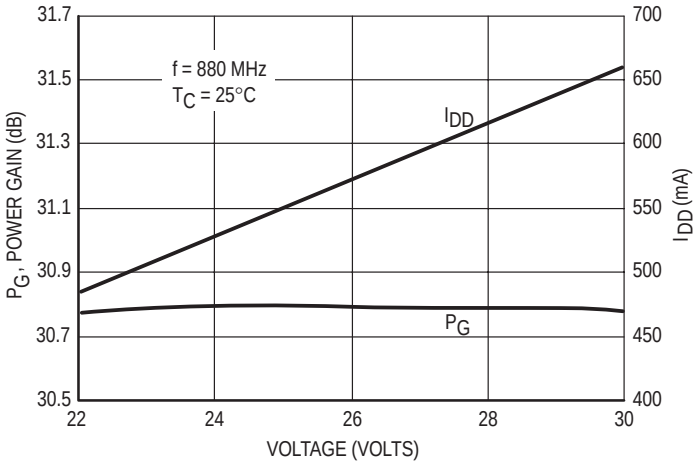


Figure 7. Power Gain, I_{DD} versus Voltage

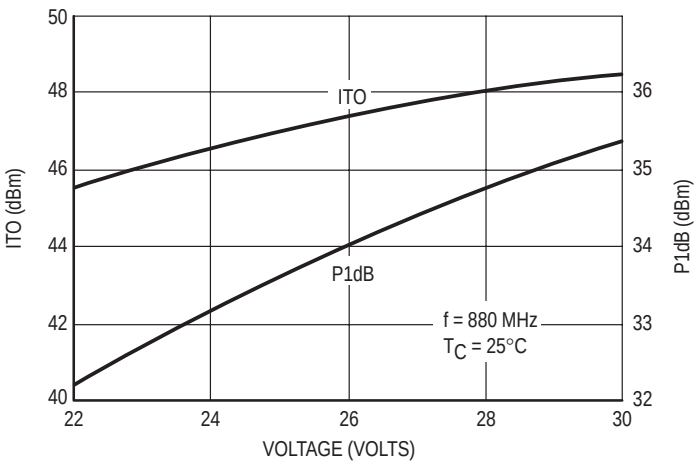


Figure 8. ITO, P1dB versus Voltage

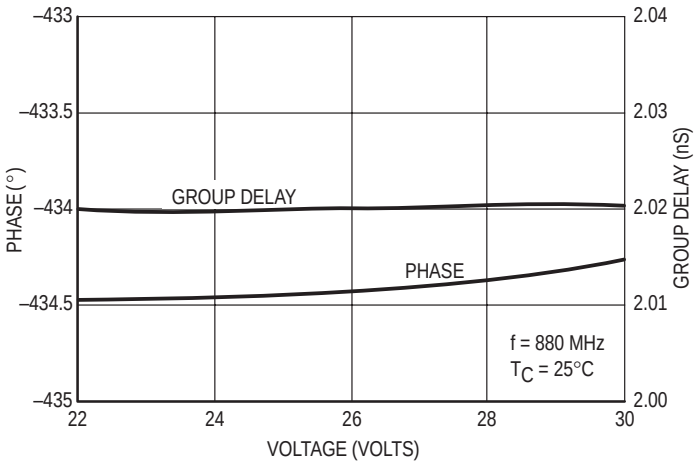


Figure 9. Phase(1), Group Delay(1) versus Voltage

(1)In Production Test Fixture

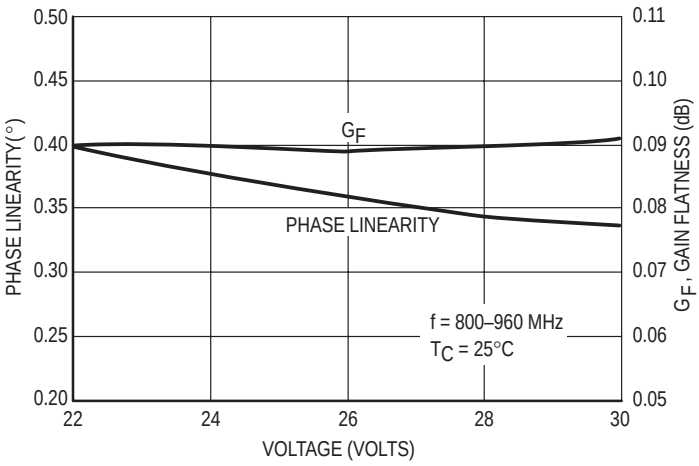


Figure 10. Phase Linearity, Gain Flatness versus Voltage

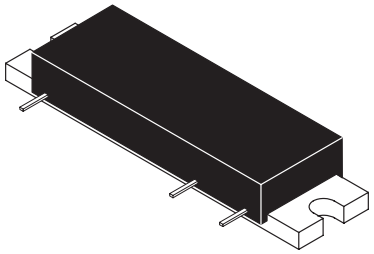
MHL9318

The RF Line
Cellular Band Linear Amplifier

3.0 W, 17.5 dB
860 – 900 MHz
LINEAR AMPLIFIER

Designed for ultra–linear amplifier applications in 50 ohm systems operating in the cellular frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for the most demanding analog or digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 49 dBm Typ
- Power Gain: 17.5 dB Typ (@ f = 880 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications
- For Use in TDMA and CDMA Multi–Carrier Applications



CASE 301AS–01, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+20	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 28 Vdc, T_C = 25°C; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	500	560	mA
Power Gain	(f = 880 MHz)	P_G	17	17.5	18.5	dB
Gain Flatness	(f = 860 – 900 MHz)	G_F	—	0.1	0.2	dB
Power Output @ 1 dB Comp.	(f = 880 MHz)	P_{out} 1 dB	—	35.5	—	dBm
Input VSWR	(f = 860 – 900 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Output VSWR	(f = 860 – 900 MHz)	$VSWR_{out}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)		ITO	47	49	—	dBm
Noise Figure	(f = 960 MHz)	NF	—	3	4.5	dB

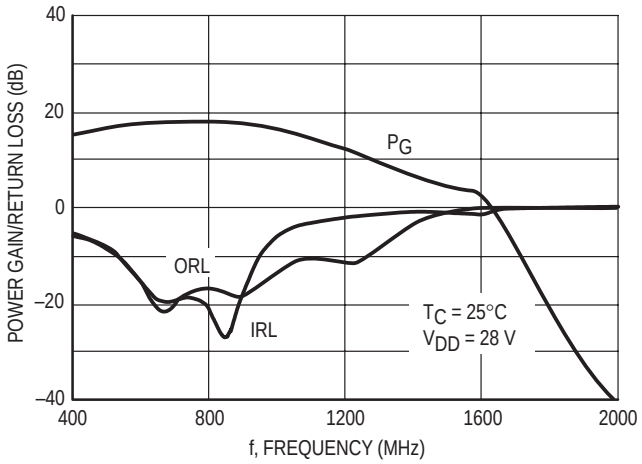


Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency

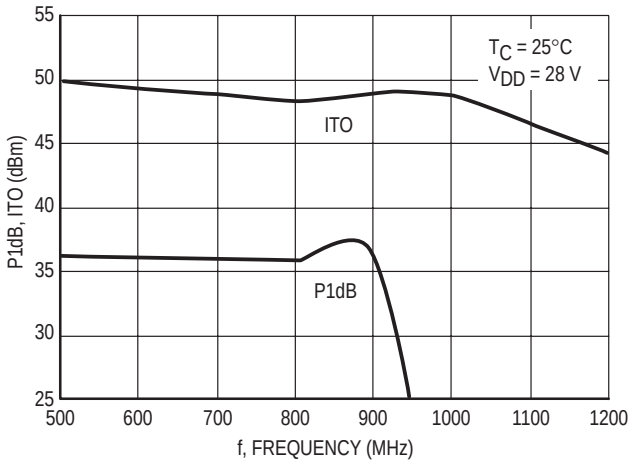


Figure 2. P1dB, ITO versus Frequency

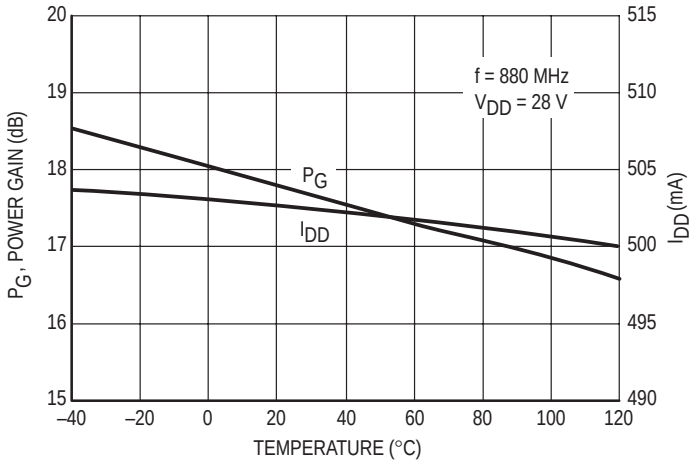


Figure 3. Power Gain, I_{DD} versus Temperature

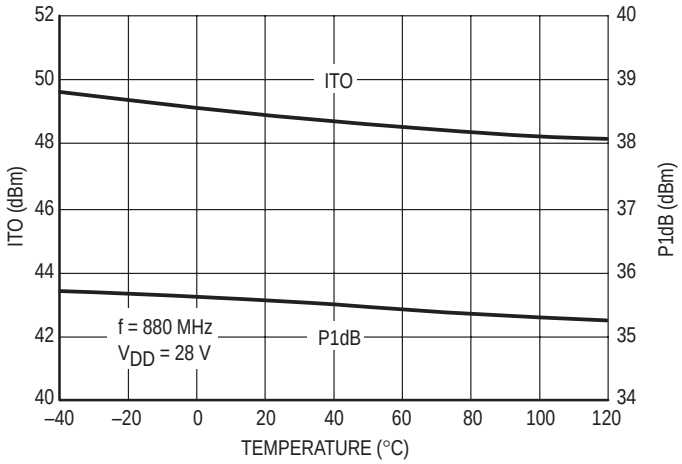


Figure 4. ITO, P1dB versus Temperature

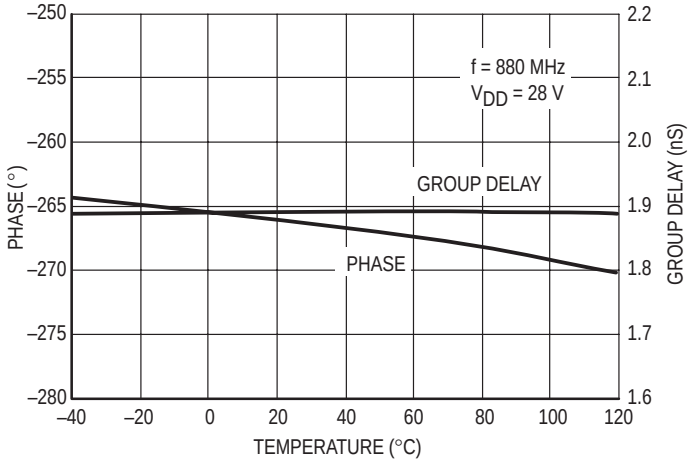


Figure 5. Phase(1), Group Delay(1) versus Temperature

(1)In Production Test Fixture

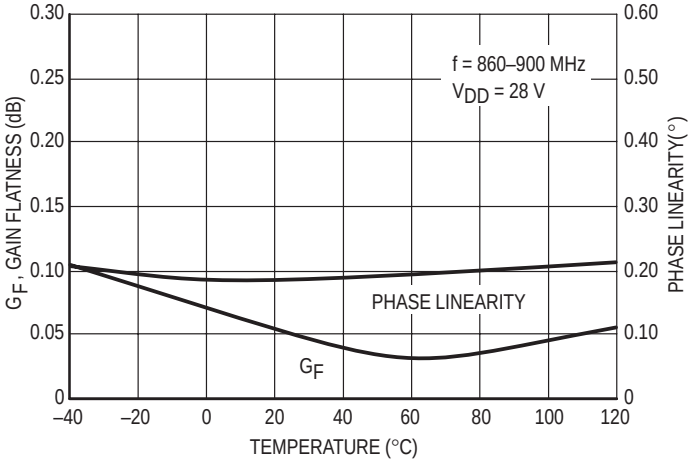


Figure 6. Gain Flatness, Phase Linearity versus Temperature

TYPICAL CHARACTERISTICS

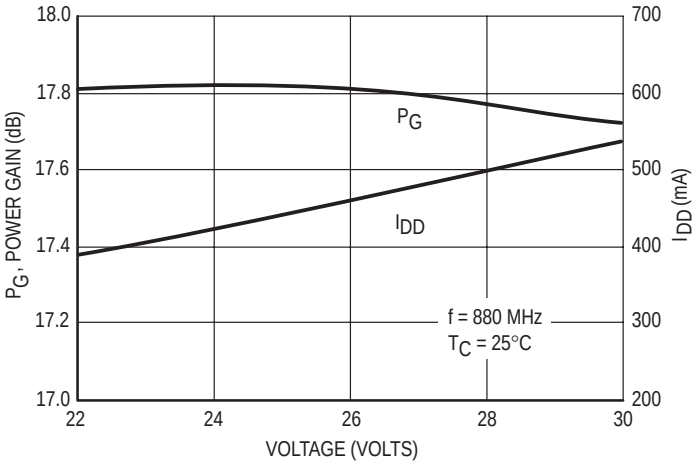


Figure 7. Power Gain, I_{DD} versus Voltage

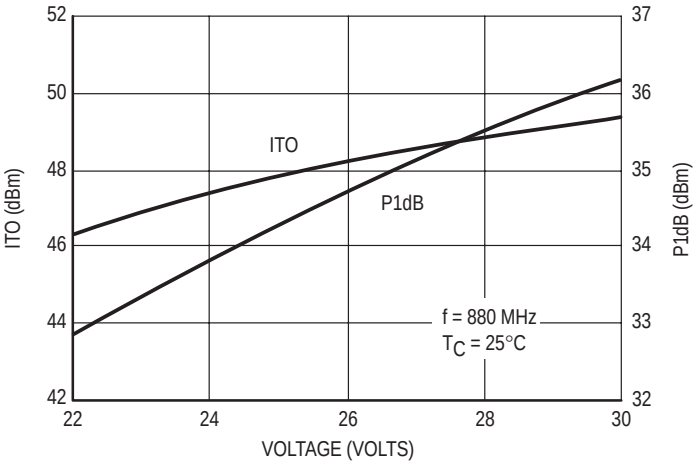


Figure 8. ITO, P1dB versus Voltage

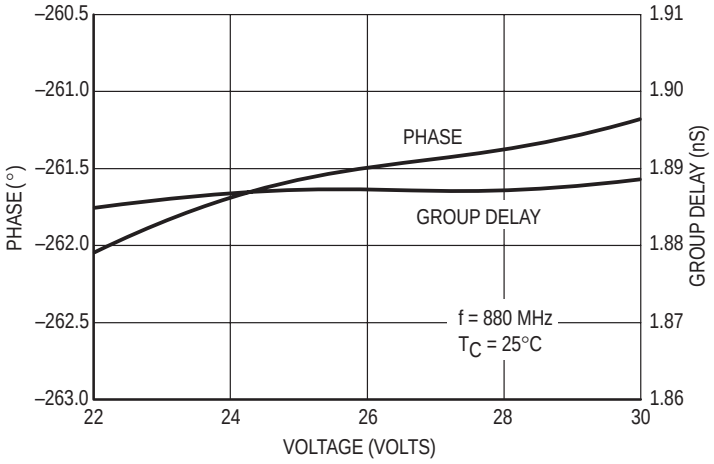


Figure 9. Phase(1), Group Delay(1) versus Voltage
(1)In Production Test Fixture

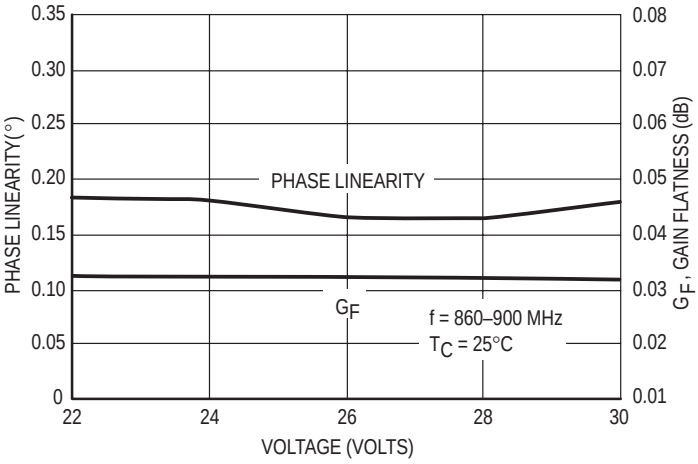


Figure 10. Phase Linearity, Gain Flatness versus Voltage

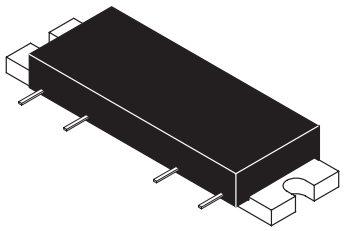
MHL9838

The RF Line
Cellular Band Linear Amplifier

8.0 W, 31 dB
800–925 MHz
LINEAR AMPLIFIER

Designed for ultra–linear amplifier applications in 50 ohm systems operating in the cellular frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for the most demanding analog or digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 50 dBm Typ
- Power Gain: 31 dB Typ (@ f = 880 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications
- For Use in TDMA and CDMA Multi–Carrier Applications



CASE 301AP–01, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+6	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 28 Vdc, T_C = 25°C; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	770	800	mA
Power Gain	(f = 880 MHz)	P_G	30	31	32	dB
Gain Flatness	(f = 800–925 MHz)	G_F	—	0.1	0.3	dB
Power Output @ 1 dB Comp.	(f = 880 MHz)	P_{out} 1 dB	—	39	—	dBm
Input VSWR	(f = 800–925 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Output VSWR	(f = 800–925 MHz)	$VSWR_{out}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)		ITO	49	50	—	dBm
Noise Figure	(f = 925 MHz)	NF	—	3.7	4.5	dB

TYPICAL CHARACTERISTICS

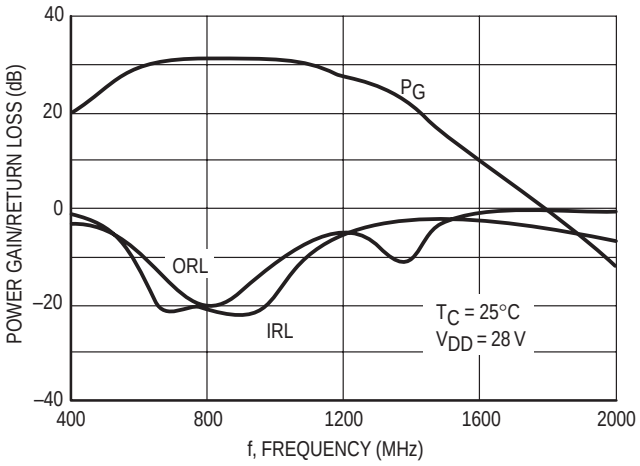


Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency

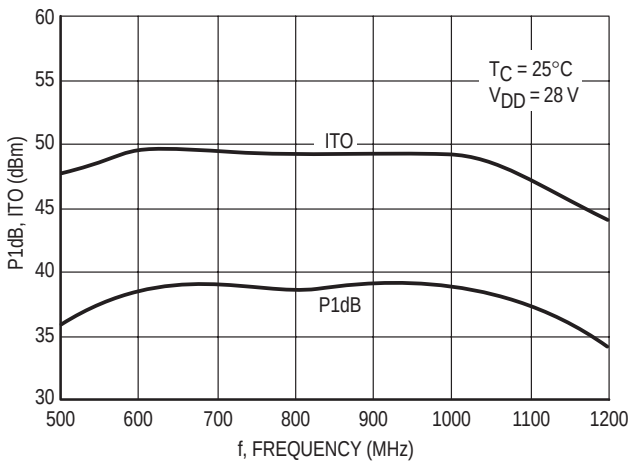


Figure 2. P1dB, ITO versus Frequency

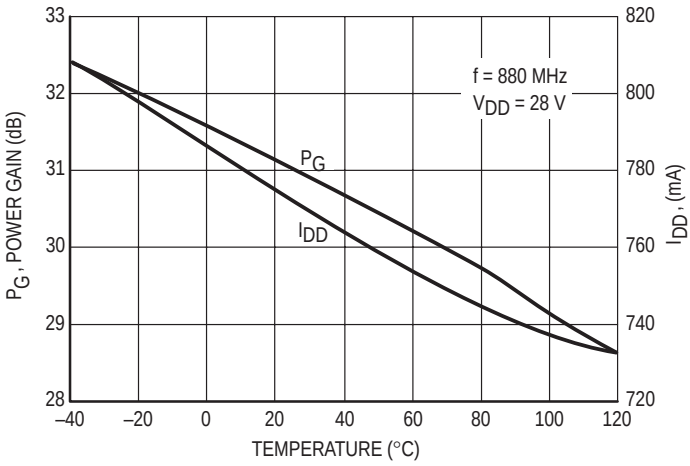


Figure 3. Power Gain, I_{DD} versus Temperature

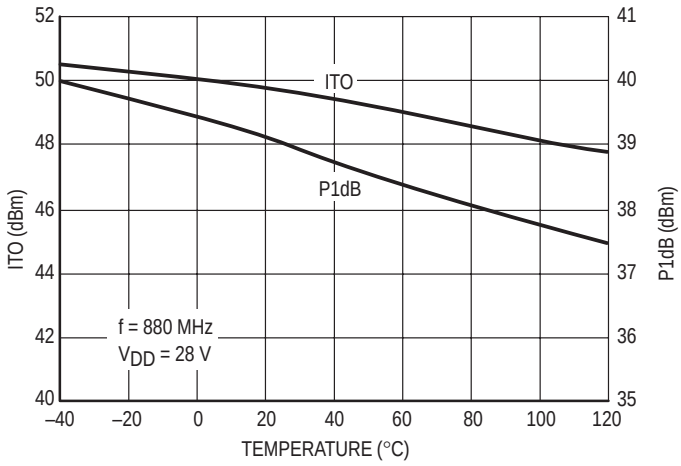


Figure 4. ITO, P1dB versus Temperature

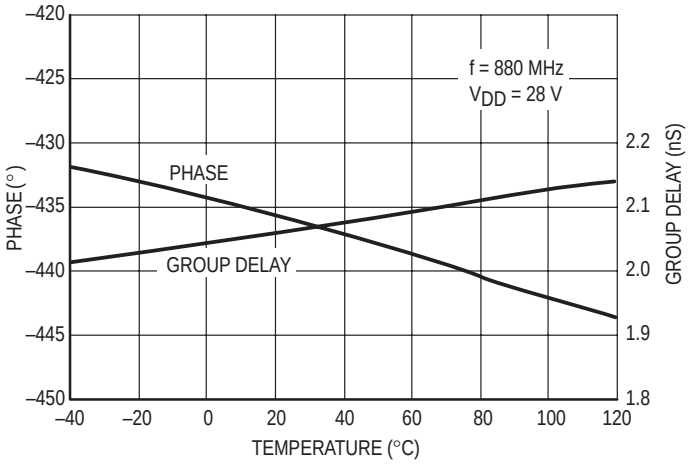


Figure 5. Phase(1), Group Delay(1) versus Temperature

(1)In Production Test Fixture

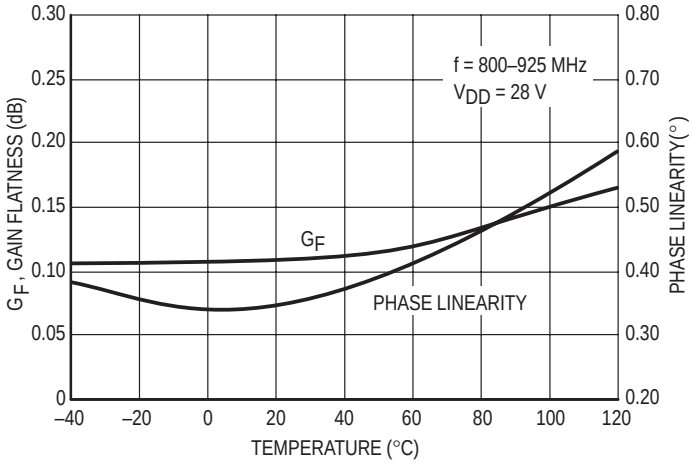


Figure 6. Gain Flatness, Phase Linearity versus Temperature

TYPICAL CHARACTERISTICS

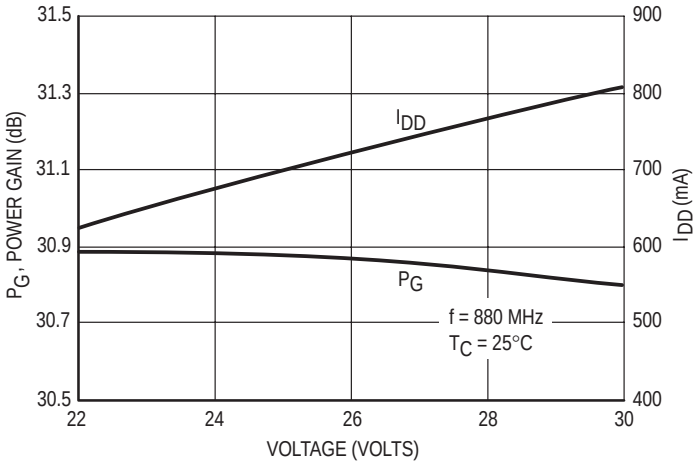


Figure 7. Power Gain, I_{DD} versus Voltage

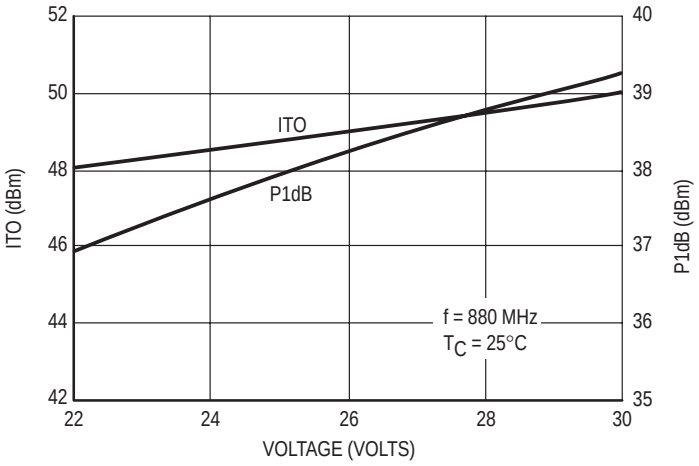


Figure 8. ITO, P1dB versus Voltage

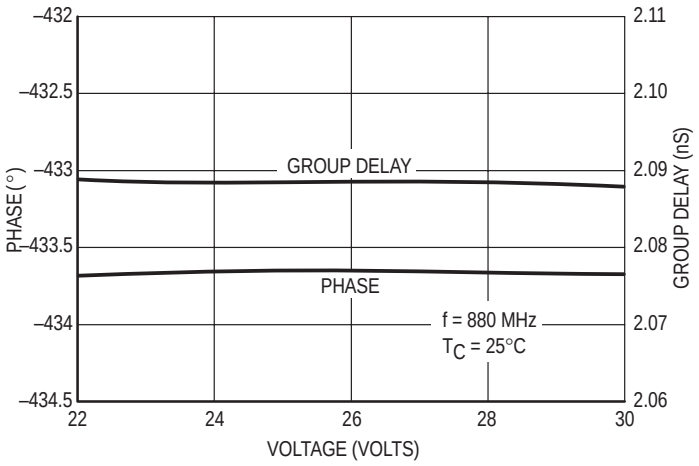


Figure 9. Phase(1), Group Delay(1) versus Voltage

(1)In Production Test Fixture

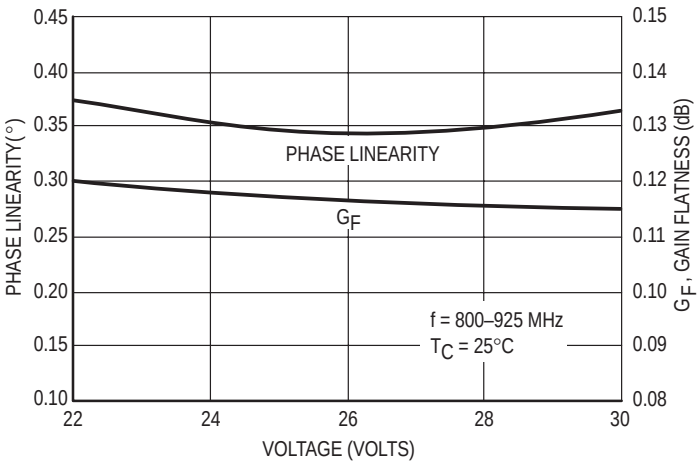


Figure 10. Phase Linearity, Gain Flatness versus Voltage

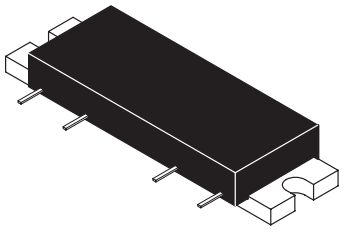
MHL19338

The RF Line
PCS Band Linear Amplifier

Designed for ultra–linear amplifier applications in 50 ohm systems operating in the PCS frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 46 dBm Typ
- Power Gain: 30 dB Typ (@ f = 1960 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications

4.0 W, 30 dB
1900–2000 MHz
LINEAR AMPLIFIER



CASE 301AP–01 STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+10	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 28 Vdc, T_C = 25°C; 50 Ω System)

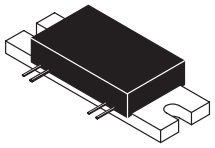
Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	500	525	mA
Power Gain	(f = 1960 MHz)	P_G	29	30	31	dB
Gain Flatness	(f = 1900 – 2000 MHz)	G_F	—	0.1	0.4	dB
Power Output @ 1 dB Comp.	(f = 1950 MHz)	P_{out} 1 dB	35	36	—	dBm
Input VSWR	(f = 1900 – 2000 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 1950 MHz, f2 = 1955 MHz)		ITO	45	46	—	dBm
Noise Figure	(f = 2000 MHz)	NF	—	4.2	4.5	dB

The RF MOSFET Line
RF Power Field Effect Amplifiers
N–Channel Enhancement–Mode Lateral MOSFETs

MHW1810-1
MHW1810-2

- Specified 26 Volts, 1805–1880 MHz, Class AB Characteristics
  Output Power = 16 Watts CW Typ
  Power Gain = 26 dB Typ @ 10 Watts (MHW1810–1)
  Power Gain = 34 dB Typ @ 10 Watts (MHW1810–2)
  Efficiency = 34% Min @ 10 Watts
- 50 Ω Input/Output System
- Designed for GSM Linearity Requirements

10 W, 1805 – 1880 MHz
RF POWER AMPLIFIER



CASE 301AW–02, STYLE 1

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
DC Supply Voltage		V_S	28	Vdc
DC Bias Voltage		V_{bias}	28	Vdc
RF Input Power	MHW1810–1 MHW1810–2	P_{in}	21 16	dBm
RF Output Power		P_{out}	20	W
Operating Case Temperature Range		T_C	– 10 to +90	°C
Storage Temperature Range		T_{stg}	– 30 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = +25°C, V_S = 26 Vdc; V_{bias} = 5 Vdc; 50 Ω system, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	1805	—	1880	MHz
Quiescent Current (P_{in} = 0 mW)		I_{DQ}	100	—	150	mA
Bias Current		I_{bias}	—	—	2	mA
Output Power at 1 dB Compression		P_{1dB}	10	14	—	W
Power Gain (P_{out} = 10 W) (P_{out} = 10 W)	MHW1810–1 MHW1810–2	G_P	24 32	26 34	28 36	dB
Efficiency (P_{out} = 10 W)		η	34	—	—	%
Input VSWR (P_{out} = 10 W)		$VSWR_{in}$	—	—	1.8:1	—
Harmonics at $2f_o$ (P_{out} = 10 W)		H_2	—	—	– 35	dBc
Harmonics at $3f_o$ (P_{out} = 10 W)		H_3	—	—	– 45	dBc
Reverse IMD; P_{out} = 10 W; Preverse = –40 dBc (F1 = F0 ±200 kHz @ –40 dBc)		IMD_r	—	—	– 50	dBc
Load Mismatch Stress Load VSWR = 5:1, All Phase Angles		ψ	No Degradation in Output Power			
Stability (P_{out} = 10 mW to 10 W, $V_S \leq$ 26 Vdc) Load VSWR = 5:1, All Phase Angles		—	All Spurious Outputs More Than 60 dB Below Desired Signal			

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

EXTREME CASE ELECTRICAL CHARACTERISTICS (T_C = –10 to +85°C, V_S = 23.5 to 26 Vdc, V_{bias} = 3 to 26 Vdc, 50 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1805	—	1880	MHz
Quiescent Current (P_{in} = 0 mW)	I_{DQ}	100	—	160	mA
Bias Current	I_{bias}	—	—	2	mA
Output Power at 1 dB Compression	P_{1dB}	8	—	—	W
Power Gain Variation for a Given Part (P_{out} = 10 W)	G_P	—	5	6.5	dB
Efficiency (P_{out} = 10 W)	η	32	—	—	%
Input VSWR	$VSWR_{in}$	—	—	2:1	—
Harmonics at $2f_o$	H_2	—	—	– 35	dBc
Harmonics at $3f_o$	H_3	—	—	– 45	dBc
Reverse IMD; P_{out} = 10 W; Preverse = –40 dBc (F1 = F0 ±200 kHz @ –40 dBc)	IMD_r	—	—	– 50	dBc
Load Mismatch Stress Load VSWR = 5:1, All Phase Angles	ψ	No Degradation in Output Power			
Stability (P_{out} = 10 mW to 10 W, $V_S \leq$ 26 Vdc) Load VSWR = 5:1, All Phase Angles	—	All Spurious Outputs More Than 60 dB Below Desired Signal			

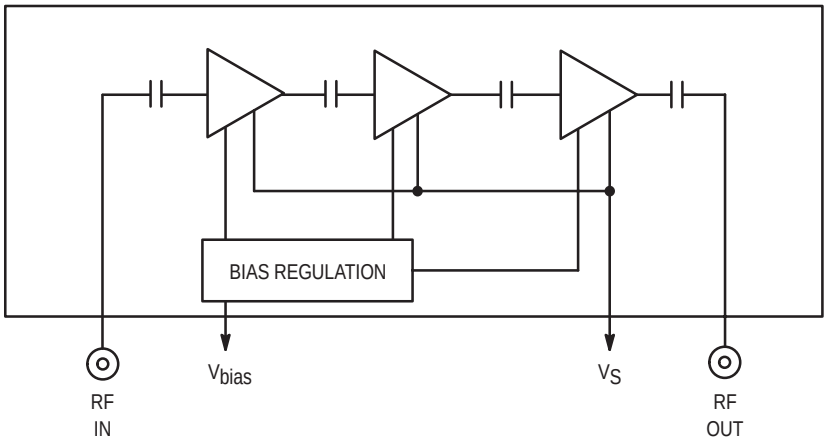


Figure 1. Internal Diagram

TYPICAL CHARACTERISTICS
MHW1810–1

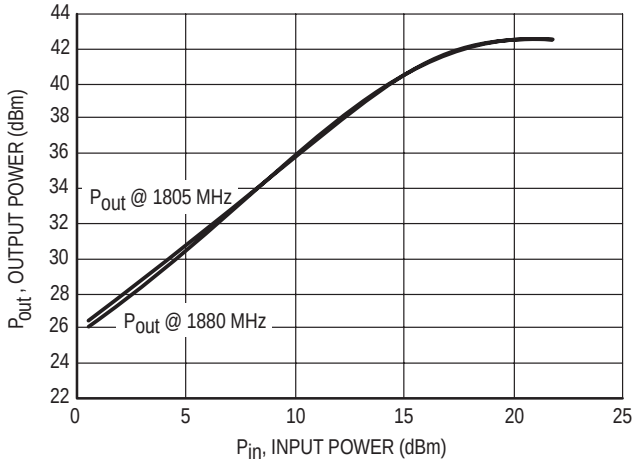


Figure 2. Output Power versus Input Power

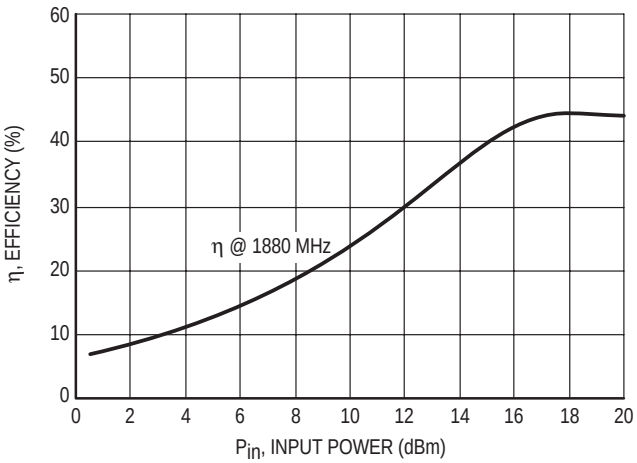


Figure 3. Efficiency versus Input Power

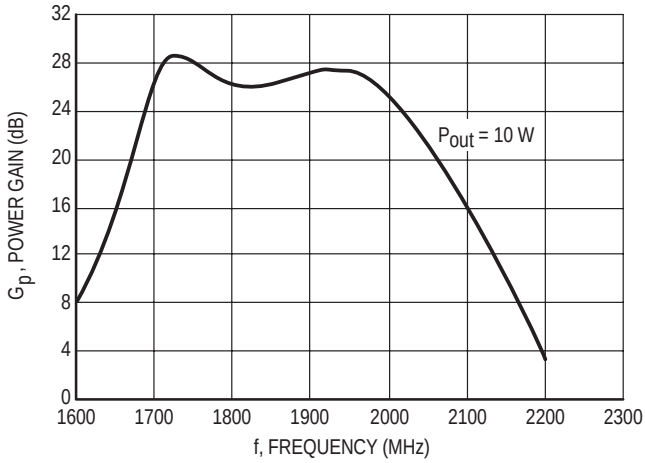


Figure 4. Power Gain versus Frequency

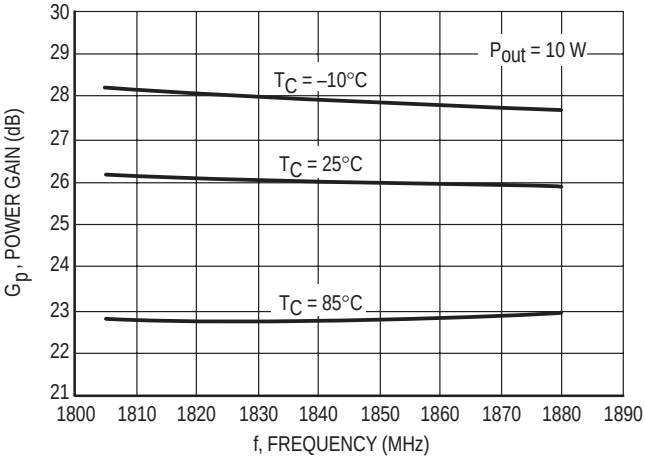


Figure 5. Gain versus Frequency

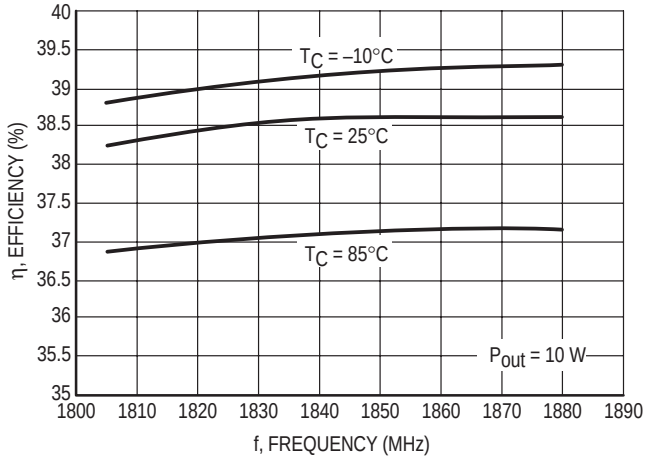


Figure 6. Efficiency versus Frequency

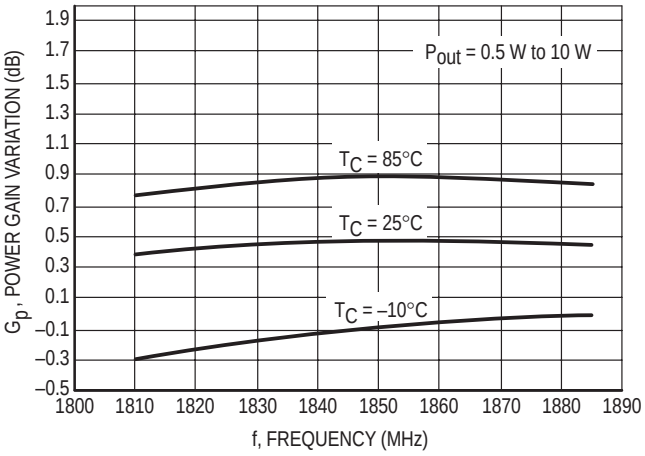


Figure 7. Power Gain Variation versus Frequency

TYPICAL CHARACTERISTICS
MHW1810–1

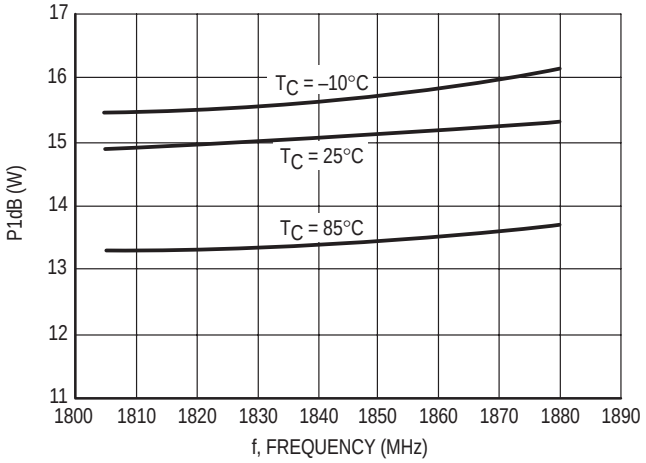


Figure 8. P1dB versus Frequency

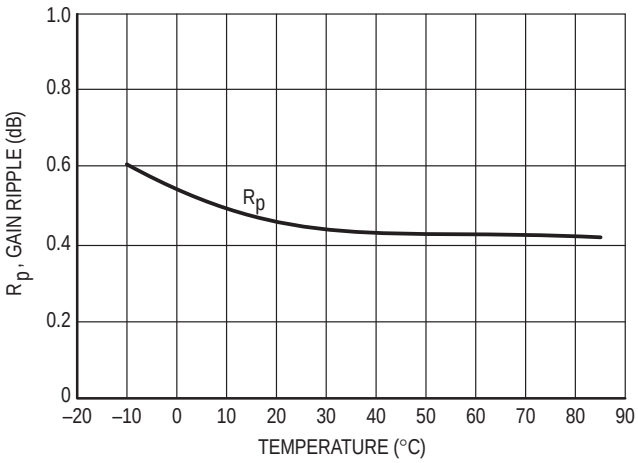


Figure 9. Gain Ripple versus Temperature

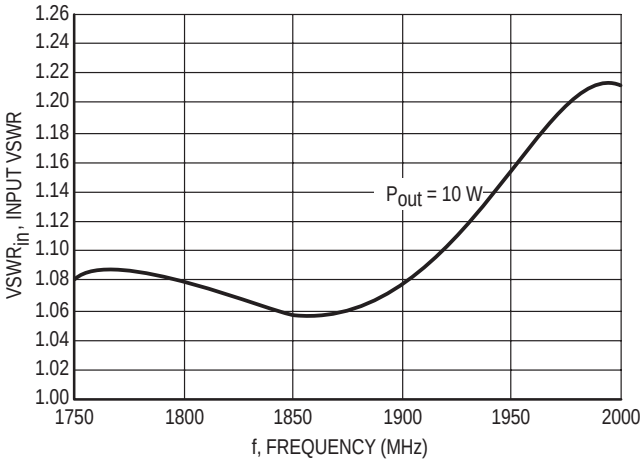


Figure 10. Input VSWR

TYPICAL CHARACTERISTICS
MHW1810–2

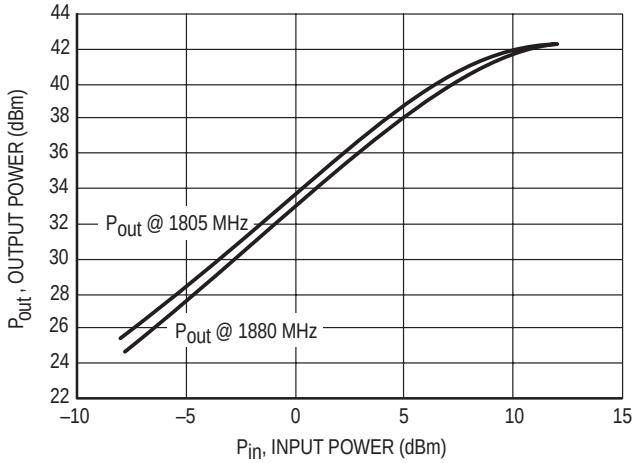


Figure 11. Output Power versus Input Power

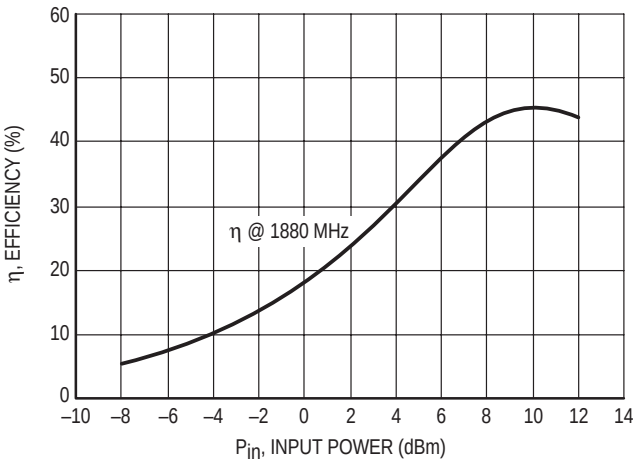


Figure 12. Efficiency versus Input Power

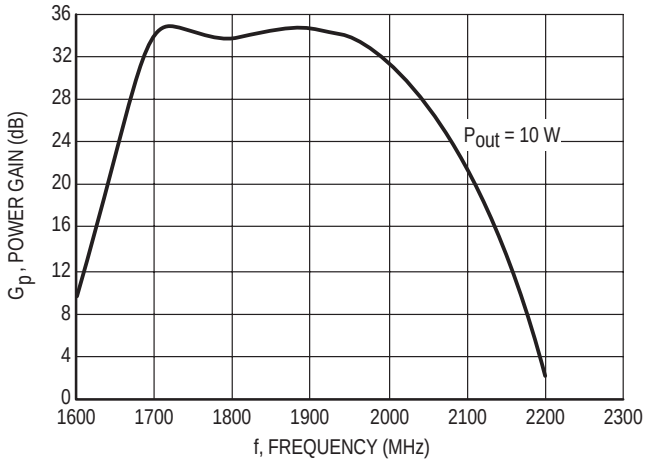


Figure 13. Power Gain versus Frequency

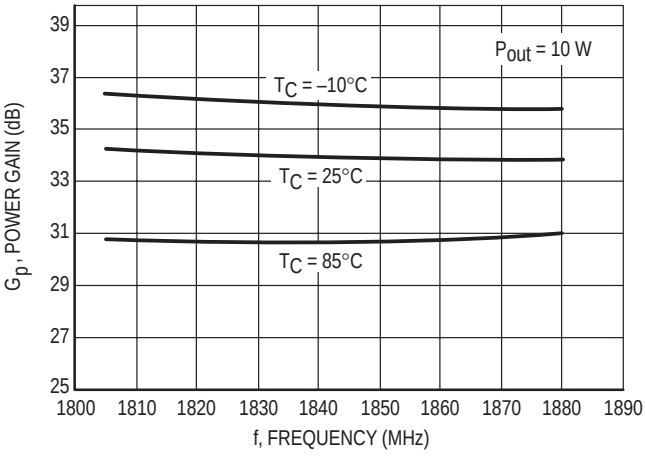


Figure 14. Gain versus Frequency

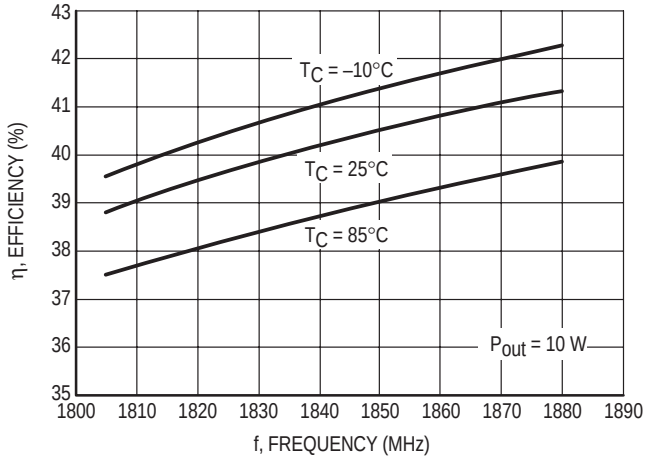


Figure 15. Efficiency versus Frequency

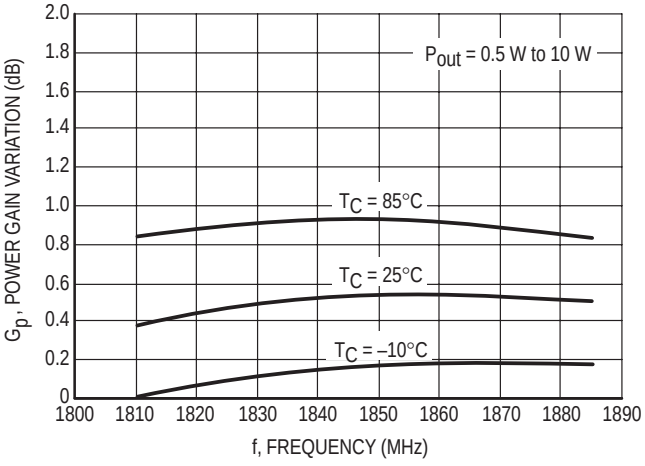


Figure 16. Power Gain Variation versus Frequency

TYPICAL CHARACTERISTICS
MHW1810–2

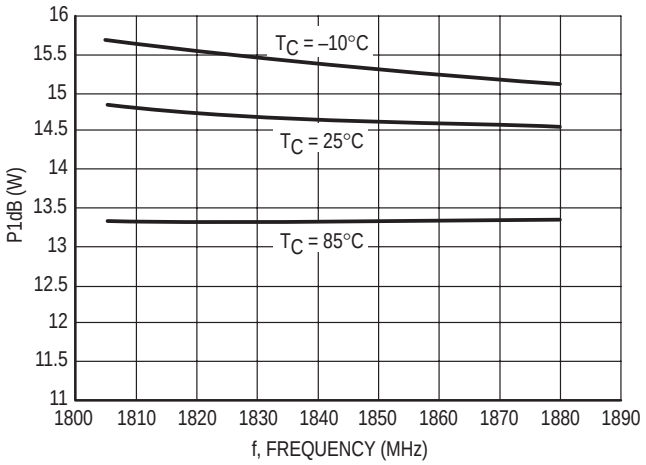


Figure 17. P1dB versus Frequency

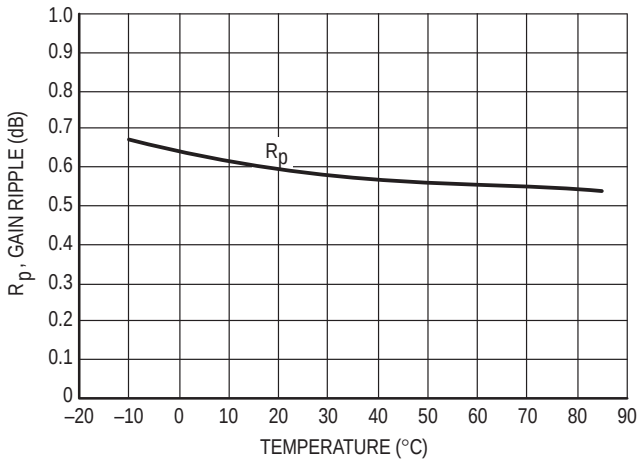


Figure 18. Gain Ripple versus Temperature

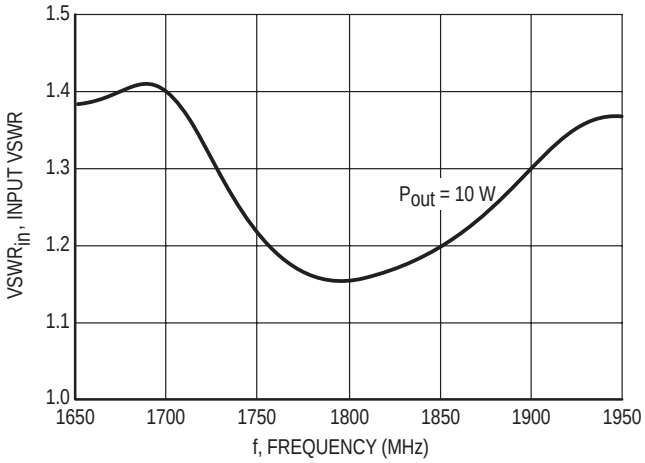


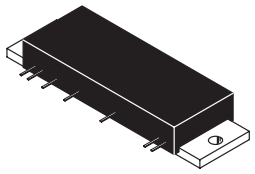
Figure 19. Input VSWR

The RF Line
Microwave Bipolar Power Amplifier

- Specified 26 Volt Characteristics:
  RF Output Power: 15 Watts
  RF Power Gain: 32 dB Typ
  Efficiency: 25% Min
- 50 Ohm Input/Output System

MHW1815

15 W
1805–1880 MHz
RF POWER AMPLIFIER



CASE 301AK–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_S	28	Vdc
DC Bias Voltage	V_B	5.5	Vdc
RF Input Power	P_{in}	17	dBm
RF Output Power	P_{out}	23	W
Operating Case Temperature Range	T_C	–30 to +85	°C
Storage Temperature Range	T_{stg}	–30 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C; V_S = 26 Vdc; V_{BIAS} = 5 Vdc; 50 Ω system)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1805	—	1880	MHz
Total Quiescent Current (P_{in} = 0 mW)	I_q	—	300	—	mA
Power Gain (P_{out} = 15 W) (1)	G_p	30	32	—	dB
Output Power at 1 dB Compression	P1dB	15	—	—	Watts
Efficiency (1 dB Compression Power)	η	25	—	—	%
Input VSWR (P_{out} = 15 W)	$VSWR_{IN}$	—	—	2:1	—
Ripple (P_{out} = 15 W)	Rp	—	1	—	dB
Load Mismatch Stress (P_{out} = 15 W; Load VSWR = 3:1; at All Phase Angles)	ψ	No Degradation in Output Power			
Stability (P_{out} = 1 mW – 15 W; Load VSWR = 2:1; at All Phase Angles except Harmonics)	—	All Spurious Outputs More than 60 dB Below Desired Signal			
Stability (P_{out} = 1 mW – 15 W; Load VSWR = 2:1; f = 1805 – 1880 MHz; at All Phase Angles)	—	All Spurious Typically Lower than –36 dBm			

(1) Adjust P_{in} for specified P_{out}.

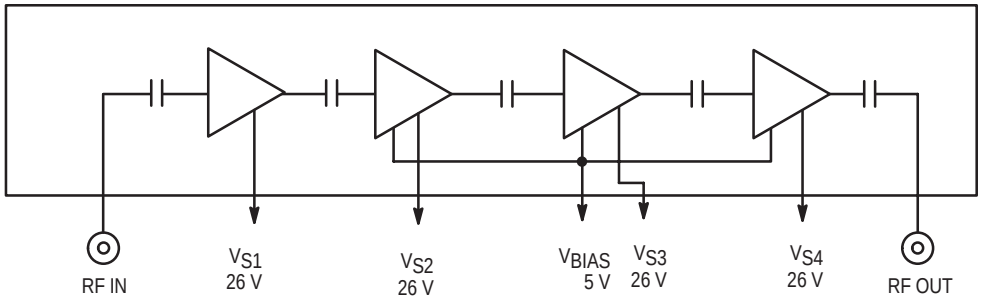


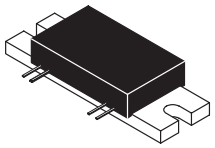
Figure 1. Internal Diagram

The RF MOSFET Line
RF Power Field Effect Amplifier
N–Channel Enhancement–Mode Lateral MOSFET

MHW1910-1

- Specified 26 Volts, 1930–1990 MHz, Class AB Characteristics
  Output Power = 14 Watts CW Typ
  Power Gain = 26 dB Typ @ 10 Watts
  Efficiency = 34% Min @ 10 Watts
- 50 Ω Input/Output System
- Designed for GSM Linearity Requirements

10 W, 1930 – 1990 MHz
RF POWER AMPLIFIER



CASE 301AW–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_S	28	Vdc
DC Bias Voltage	V_{bias}	28	Vdc
RF Input Power	P_{in}	21	dBm
RF Output Power	P_{out}	20	W
Operating Case Temperature Range	T_C	– 10 to +90	°C
Storage Temperature Range	T_{stg}	– 30 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = +25°C, V_S = 26 Vdc; V_{bias} = 5 Vdc; 50 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1930	—	1990	MHz
Quiescent Current (P_{in} = 0 mW)	I_{DQ}	100	—	150	mA
Bias Current	I_{bias}	—	—	2	mA
Output Power at 1 dB Compression	P_{1dB}	10	14	—	W
Power Gain (P_{out} = 10 W)	G_P	24	26	28	dB
Efficiency (P_{out} = 10 W)	η	34	—	—	%
Input VSWR	$VSWR_{in}$	—	—	1.8:1	—
Harmonics at $2f_o$	H_2	—	—	– 35	dBc
Harmonics at $3f_o$	H_3	—	—	– 45	dBc
Reverse IMD; P_{out} = 10 W; Preverse = –40 dBc (F1 = F0 ±200 kHz @ –40 dBc)	IMD_r	—	—	– 50	dBc
Load Mismatch Stress Load VSWR = 5:1, All Phase Angles	ψ	No Degradation in Output Power			
Stability (P_{out} = 10 mW to 10 W, $V_S \leq$ 26 Vdc) Load VSWR = 5:1, All Phase Angles	—	All Spurious Outputs More Than 60 dB Below Desired Signal			

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

EXTREME CASE ELECTRICAL CHARACTERISTICS (T_C = –10 to +85°C, V_S = 23.5 to 26 Vdc, V_{bias} = 3 to 26 Vdc, 50 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1930	—	1990	MHz
Quiescent Current (P_{in} = 0 mW)	I_{DQ}	100	—	160	mA
Bias Current	I_{bias}	—	—	2	mA
Output Power at 1 dB Compression	P_{1dB}	8	—	—	W
Power Gain Variation for a Given Part (P_{out} = 10 W)	G_P	—	5	6.5	dB
Efficiency (P_{out} = 10 W)	η	32	—	—	%
Input VSWR	$VSWR_{in}$	—	—	2:1	—
Harmonics at $2f_o$	H_2	—	—	– 35	dBc
Harmonics at $3f_o$	H_3	—	—	– 45	dBc
Reverse IMD; P_{out} = 10 W; Preverse = –40 dBc (F1 = F0 ±200 kHz @ –40 dBc)	IMD_r	—	—	– 46	dBc
Load Mismatch Stress Load VSWR = 5:1, All Phase Angles	ψ	No Degradation in Output Power			
Stability (P_{out} = 10 mW to 10 W, $V_S \leq$ 26 Vdc) Load VSWR = 5:1, All Phase Angles	—	All Spurious Outputs More Than 60 dB Below Desired Signal			

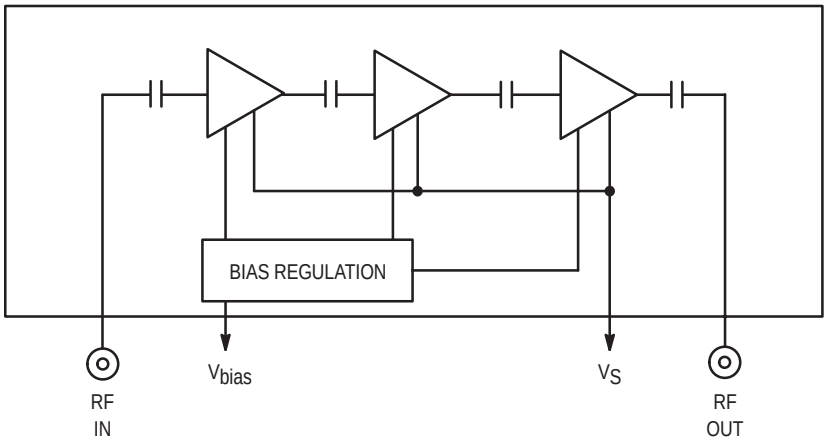


Figure 1. Internal Diagram

TYPICAL CHARACTERISTICS

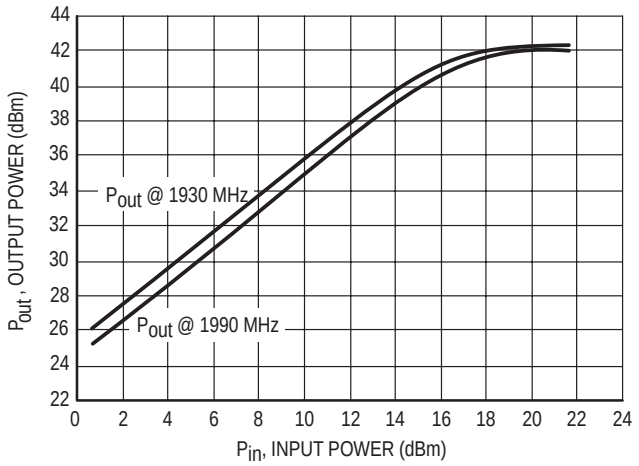


Figure 2. Output Power versus Input Power

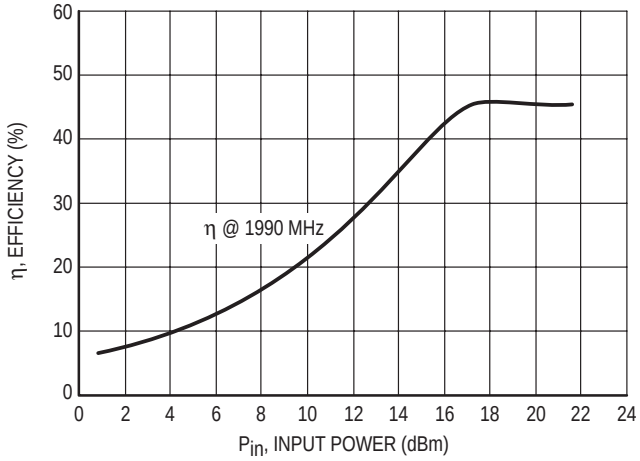


Figure 3. Efficiency versus Input Power

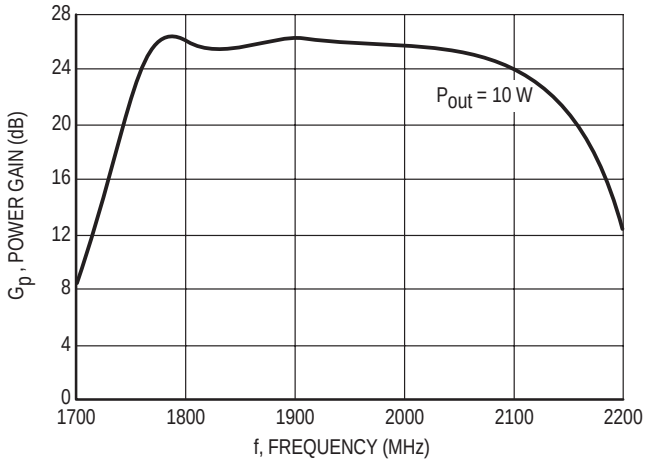


Figure 4. Power Gain versus Frequency

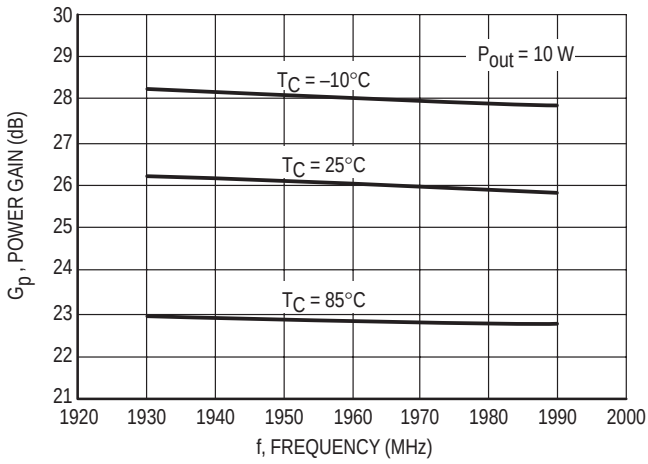


Figure 5. Gain versus Frequency

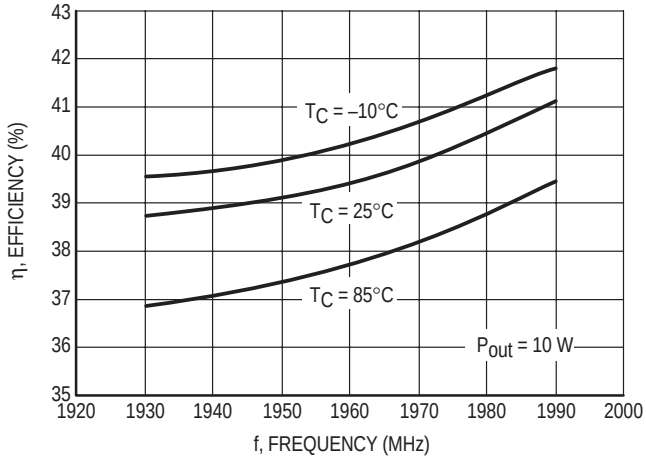


Figure 6. Efficiency versus Frequency

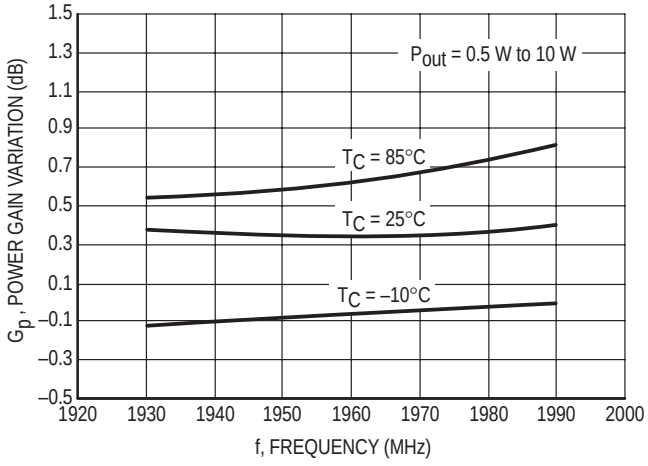


Figure 7. Power Gain Variation versus Frequency

TYPICAL CHARACTERISTICS

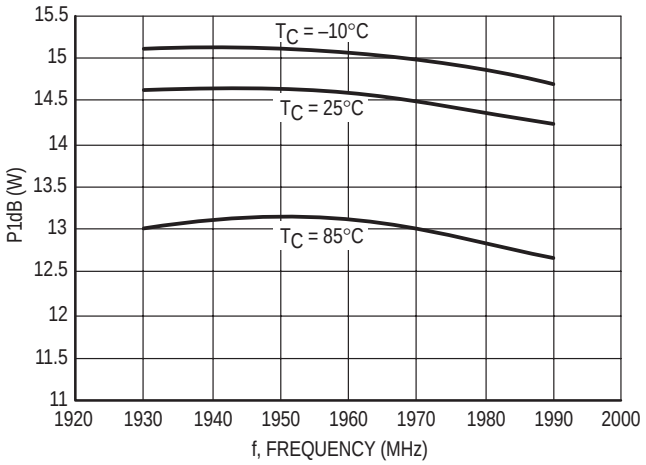


Figure 8. P1dB versus Frequency

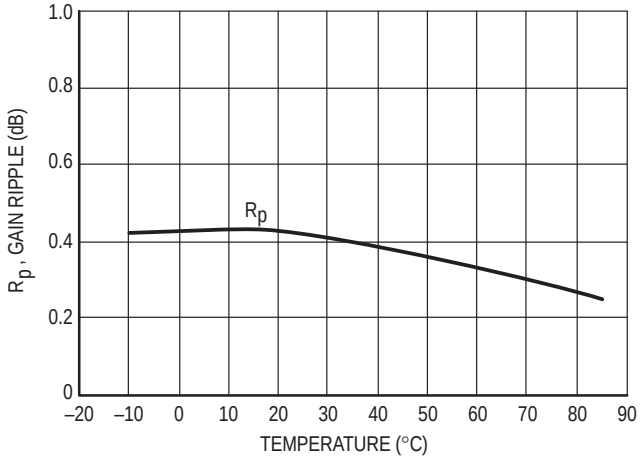


Figure 9. Gain Ripple versus Temperature

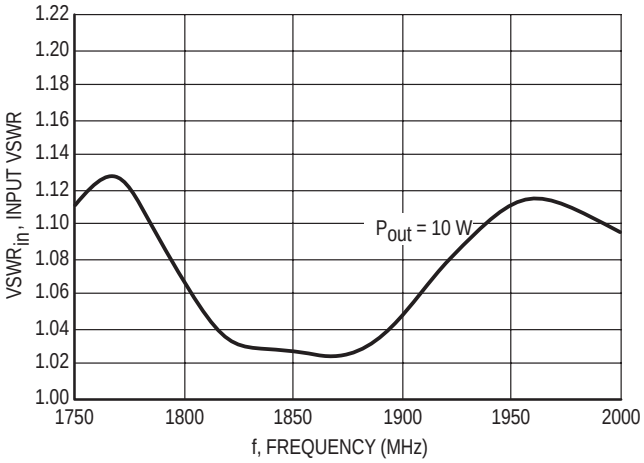


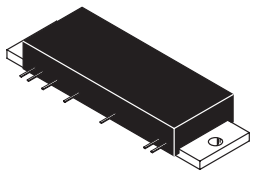
Figure 10. Input VSWR

The RF Line
Microwave Bipolar Power Amplifier

- Specified 26 Volt Characteristics:
  RF Output Power: 15 Watts
  RF Power Gain: 31 dB Typ
  Efficiency: 25% Min
- 50 Ohm Input/Output System

MHW1915

15 W
1930 – 1990 MHz
RF POWER AMPLIFIER



CASE 301AK–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_S	28	Vdc
DC Bias Voltage	V_B	5.5	Vdc
RF Input Power	P_{in}	17	dBm
RF Output Power	P_{out}	23	W
Operating Case Temperature Range	T_C	–30 to +85	°C
Storage Temperature Range	T_{stg}	–30 to +100	°C

ELECTRICAL CHARACTERISTICS (V_S = 26 Vdc; V_{BIAS} = 5 Vdc; T_C = +25°C; 50 Ω system)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1930	—	1990	MHz
Total Quiescent Current (P_{in} = 0 mW)	I_q	—	300	—	mA
Power Gain (P_{out} = 15 W) (1)	G_p	29	31	—	dB
Output Power at 1 dB Compression	P1dB	15	—	—	Watts
Efficiency (1 dB Compression Power)	η	25	—	—	%
Input VSWR (P_{out} = 15 W)	$VSWR_{IN}$	—	—	2:1	—
Ripple (P_{out} = 15 W)	Rp	—	1	—	dB
Load Mismatch Stress (P_{out} = 15 W; Load VSWR = 2:1; at All Phase Angles)	ψ	No Degradation in Output Power			
Stability (P_{out} = 1 mW – 15 W; Load VSWR = 2:1; at All Phase Angles except Harmonics)	—	All Spurious Outputs More than 60 dB Below Desired Signal			
Stability (P_{out} = 1 mW – 15 W; Load VSWR = 2:1; f = 1930 – 1990 MHz; at All Phase Angles)	—	All Spurious Outputs Typically Lower than –36 dBm			

(1) Adjust P_{in} for specified P_{out}.

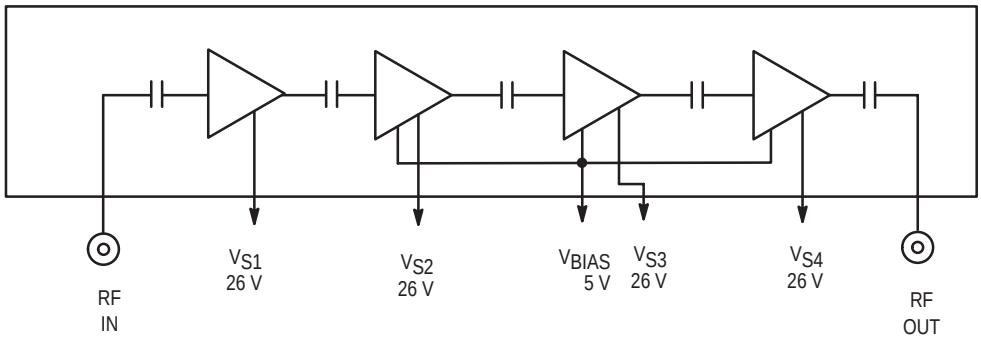


Figure 1. Internal Diagram

Chapter Seven
RF CATV Distribution Amplifiers

Section One 7.1–0
RF CATV Distribution Amplifiers – Selector Guide

Section Two 7.2–0
RF CATV Distribution Amplifiers – Data Sheets

Section One
Selector Guide

Motorola RF CATV Distribution Amplifiers

Motorola Hybrids are manufactured using the latest generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels.

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RF CATV Distribution Amplifiers	7.1–1
Forward Amplifiers	7.1–2
Reverse Amplifiers	7.1–4
Packages	7.1–6

Motorola RF CATV Distribution Amplifiers

Motorola Hybrids are manufactured using the latest generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels.

Forward Amplifiers

40–1000 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 1000 MHz dB Max	Package/ Style
			Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 152 CH	Cross Modulation dB 152 CH		
MHW9182B★	18.5	152	+38	–63(40)	–61	–61	7.5	714Y/1
MHW9242A★	24	152	+38	–61(40)	–61	–59	8.0	714Y/1

40–860 MHz Hybrids

Device	Gain dB Typ @ 50 MHz	Frequency MHz	V_{CC} Volts	2nd Order IMD @ V_{out} = 50 dBmV/ch Max	DIN45004B @ f=860 MHz dBμV Min	Noise Figure @ 860 MHz dB Max	Package/ Style
CA901	17	40 – 860	24	–60	120	8.0	714P/2
CA901A	17	40 – 860	24	–64	120	8.0	714P/2
Power Doubling Hybrids							
CA922	17	40 – 860	24	–63	123	9.5	714P/2
CA922A	17	40 – 860	24	–67	123	9.5	714P/2

40–860 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 860 MHz dB Max	Package/ Style
			Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 128 CH	Cross Modulation FM = 55.25 MHz dB 128 CH		
MHW8182B	18.5	128	+38	–64(40)	– 66	– 65	7.5	714Y/1
MHW8222B(46b)	21.9	128	+38	–59(40)	– 64	– 63	7.0	1302/1
MHW8242B★	24	128	+38	–62(40)	– 64	– 60	7.5	714Y/1
MHW8272A	27.2	128	+38	–64(40)	– 64	– 62	7.0	714Y/1
MHW8292	29	128	+38	–56(40)	– 60	– 60	7.0	714Y/1

(40)Composite 2nd Order; V_{out} = +38 dBmV/ch

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

★New Product

CATV Distribution: Forward Amplifiers (continued)

40 – 860 MHz Hybrids, V_{CC} = 24 Vdc, Class A (continued)

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 128 CH	Cross Modulation FM = 55.25 MHz dB 128 CH	Noise Figure @ 860 MHz dB Max	Package/ Style
Power Doubling Hybrids								
MHW8185L(21)	18.5	128	+40	–62(39)	– 63	– 64	8.5*	714Y/1
MHW8185LR(28)	18.5	128	+40	–62(39)	– 63	– 64	8.5*	714Y/2
MHW8185	18.8	128	+40	–62(39)	– 64	– 64	8.0	714Y/1
MHW8185R(14)	18.8	128	+40	–62(39)	– 64	– 64	8.0	714Y/2
MHW8205L(22)	19.5	128	+40	–60(39)	– 63	– 64	8.5*	714Y/1
MHW8205	19.8	128	+40	–60(39)	– 63	– 64	8.0	714Y/1
MHW8205R(24)	19.8	128	+40	–60(39)	– 63	– 64	8.0	714Y/2
MHW8205LR(29,46b)	19.8	128	+40	–60(39)	– 63	– 64	8.5*	714Y/2

*@ 870 MHz

40 – 750 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 110 CH	Cross Modulation FM = 55.25 MHz dB 110 CH	Noise Figure @ 750 MHz dB Max	Package/ Style
MHW7182B	18.5	110	+40	–63(39)	– 66	– 64	6.5	714Y/1
MHW7222A	21.5	110	+40	–57(39)	– 60	– 60	7.0	714Y/1
MHW7222B(46b)	21.9	110	+40	–60(39)	– 61	– 60	6.5	1302/1
MHW7242B★	24	110	+40	–62(39)	– 63	– 58	7.0	714Y/1
MHW7272A	27.2	110	+40	–64(39)	– 64	– 60	6.5	714Y/1
MHW7292	29	110	+40	–60(39)	– 60	– 60	6.5	714Y/1
Power Doubling Hybrids								
MHW7185CL(23)	18.5	110	+44	–64(36)	–61	–63	7.5	714Y/1
MHW7185C	18.8	110	+44	–64(36)	–62	–63	7.5	714Y/1
MHW7205CL(27)	19.5	110	+44	–63(36)	–61	–62	7.5	714Y/1
MHW7205C	19.8	110	+44	–63(36)	–61	–62	7.5	714Y/1

(14)Mirror Amplifier Version of MHW8185

(21)Low DC Current Version of MHW8185; Typical I_{CC} @ Vdc = 24 V is 365 mA.

(22)Low DC Current Version of MHW8205; Typical I_{CC} @ Vdc = 24 V is 365 mA.

(23)Low I_{CC} Version of MHW7185C; Typical I_{CC} @ Vdc = 24 V is 365 mA.

(24)Mirror Amplifier Version of MHW8205

(27)Low I_{CC} Version of MHW7205C; Typical I_{CC} @ Vdc = 24 V is 365 mA.

(28)Mirror Amplifier Version of MHW8185L

(29)Mirror Amplifier Version of MHW8205L

(36)Composite 2nd order; V_{out} = +44 dBmV/ch

(39)Composite 2nd order; V_{out} = +40 dBmV/ch

(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

★New Product

CATV Distribution: Forward Amplifiers (continued)

40–550 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 550 MHz dB Max	Package/ Style
			Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 77 CH	Cross Modulation dB 77 CH		
MHW6182T(46b)	18.2	77	+44	–72(35)	–58	–57	7.0	1302/1
MHW6222T(46b)	22	77	+44	–66(35)	–57	–57	6.0	1302/1
MHW6272T(46b)	27	77	+44	–64(35)	–57	–57	6.5	1302/1
MHW6342T	34.5	77	+44	–64(35)	–57	–57	6.5	1302/1
Power Doubling Hybrids								
MHW6185T(46b)	18.5	77	+44	–65(36)	–65	–68	7.5	1302/1

Reverse Amplifiers

5–200 MHz Hybrids, V_{CC} = 24 Vdc, Class A – 22 CH, 26 CH

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications						Noise Figure @ 175 MHz dB Max	Package/ Style
			Output Level dBmV	2nd Order Test(30) dB	Composite Triple Beat dB		Cross Modulation dB			
					22 CH	26 CH	22 CH	26 CH		
MHW1224	22	22	+50	–72	–69	–68.5(19)	–62	–62(19)	5.5	714Y/1
MHW1244	24	22	+50	–72	–68	–67.5(19)	–61	–61(19)	5.0	714Y/1

5–200 MHz Hybrids, V_{CC} = 24 Vdc, Class A – 6 CH, 10 CH

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications							Noise Figure @ 200 MHz dB Max	Package/ Style
			Output Level dBmV	2nd Order Test dB		Composite Triple Beat dB		Cross Modulation dB			
				6 CH	10 CH	6 CH	10 CH	6 CH	10 CH		
MHW1224LA(34,46b)	22	6,10	50	TBD	TBD	–74	TBD	–64	TBD	4.9	1302/1
MHW1254LA(34,46b)	25	6,10	50	TBD	TBD	–75	TBD	–65	TBD	6.1	1302/1
MHW1304LA(34,46b)	30	6,10	50	TBD	TBD	–74	TBD	–64	TBD	4.9	1302/1
MHW1354LA(34,46b)	35	6,10	50	TBD	TBD	–73	TBD	–63	TBD	5.8	1302/1

(19)Typical
(30)Channels 2 and A @ 7
(34)Specifications are preliminary.
(35)Channels 2 and M30 @ M39
(36)Composite 2nd order; V_{out} = +44 dBmV/ch
(46)To be introduced: a) 1Q00; b) 2Q00; c) 3Q00

CATV Distribution: Reverse Amplifiers (continued)

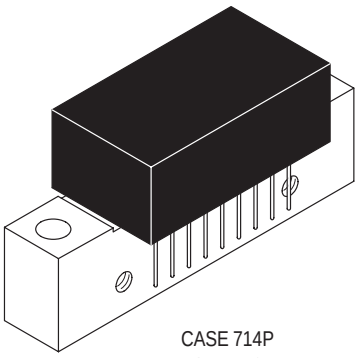
Low Current Amplifiers — 5–50 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	I_{DC} mA Max	Maximum Distortion Specifications				Noise Figure @ 50 MHz dB Max	Package/ Style
				Output Level dBmV	2nd Order Test(30) dB	Composite Triple Beat dB 4 CH	Cross Modulation dB 4 CH		
MHW1254L	25	4	135	+50	–70	–70	–62	4.5	714Y/1
MHW1304L	30	4	135	+50	–70	–66	–57	4.5	714Y/1

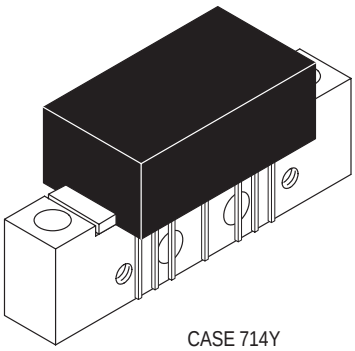
(19)Typical

(30)Channels 2 and A @ 7

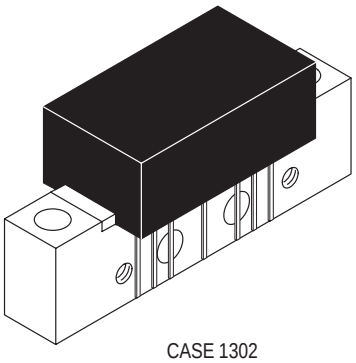
RF CATV Distribution Amplifiers Packages



CASE 714P
STYLE 2



CASE 714Y
STYLE 1, 2



CASE 1302
STYLE 1

Section Two

Motorola RF CATV Distribution Amplifiers – Data Sheets

Device Number	Page Number
CA901	7.2–3
CA901A	7.2–3
CA922	7.2–5
CA922A	7.2–5
MHW1224	7.2–7
MHW1244	7.2–7
MHW1254L	7.2–9
MHW1304L	7.2–10
MHW6182	7.2–11
MHW6185B	7.2–12
MHW6222	7.2–13
MHW6272	7.2–14
MHW6342T	7.2–15
MHW7182B	7.2–17
MHW7185C	7.2–18
MHW7185CL	7.2–19
MHW7205C	7.2–20
MHW7205CL	7.2–21
MHW7222A	7.2–22
MHW7242B	7.2–24
MHW7272A	7.2–25
MHW7292	7.2–26
MHW8182B	7.2–27
MHW8185	7.2–28
MHW8185L	7.2–29
MHW8185LR	7.2–30
MHW8185R	7.2–31
MHW8205	7.2–32
MHW8205L	7.2–33
MHW8205R	7.2–34
MHW8222	7.2–35
MHW8242B	7.2–36
MHW8272A	7.2–37
MHW8292	7.2–38
MHW9182B	7.2–39
MHW9242A	7.2–40

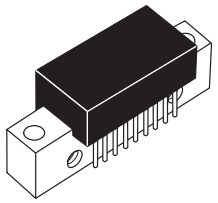
The RF Line
VHF/UHF CATV Amplifiers

. . . designed for broadband applications requiring low–distortion amplification. Specifically intended for CATV/MATV market requirements. These amplifiers feature ion–implanted arsenic emitter transistors and an all gold metal system.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  Frequency Range — 40 to 860 MHz
  Power Gain — 17 dB Typ @ f = 40 MHz
  Noise Figure — 6.5 dB Typ @ f = 500 MHz
  120 dBμV DIN45004B @ 860 MHz
- All Gold Metallization for Improved Reliability
- Superior Gain, Return Loss and DC Current Stability with Temperature

CA901
CA901A

17 dB
40 – 860 MHz
VHF/UHF
CATV/MATV
AMPLIFIERS



CASE 714P–03, STYLE 2
(CA)

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+14	dBm
Supply Voltage	V_{CC}	26	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain (f = 40 MHz)		P_G	16.5	17	17.5	dB
Slope (40 – 860 MHz)		S	0.2	0.8	1.5	dB
Gain Flatness		—	—	—	0.6	dB
Input/Output Return Loss f = 40 – 100 MHz f = 100 – 800 MHz f = 800 – 860 MHz		IRL/ORL	20 15 10/15	— 17 12/18	— — —	dB
Second Order Intermodulation Distortion (V_{out} = +50 dBmV per ch.)	CA901 CA901A	IMD_2	— —	— —	–60 –64	dB
DIN45004B (See Figure 1) f = 40 – 400 MHz f = 400 – 860 MHz		DIN	121 120	— —	— —	dBμV
Noise Figure f = 500 MHz f = 860 MHz		NF	— —	6.5 7.0	7.5 8.0	dB
Supply Current		I_{DC}	—	235	255	mA

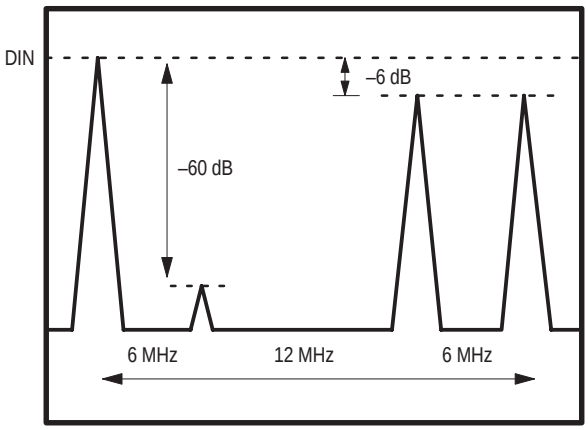


Figure 1. DIN45004B Test

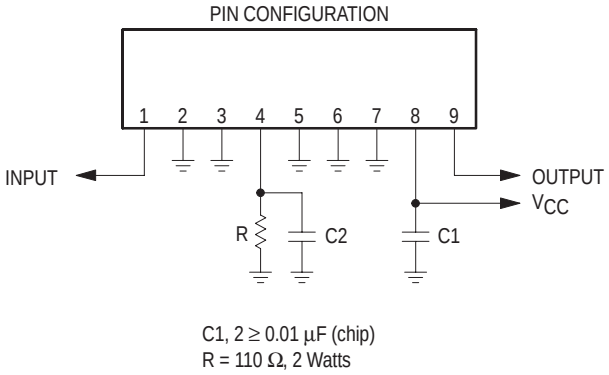


Figure 2. External Connections

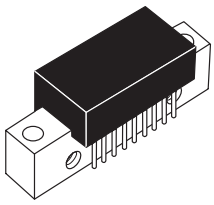
The RF Line
VHF/UHF CATV Amplifiers

CA922
CA922A

Designed for broadband applications requiring low–distortion and high output capability. Specifically intended for CATV/MATV market requirements. These amplifiers feature ion–implanted arsenic emitter transistors and an all gold metal system.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C
  - Frequency Range — 40 to 860 MHz
  - Power Gain — 17 dB Typ @ f = 40 MHz
  - Noise Figure — 7.0 dB Typ @ f = 500 Mhz
  - 123 dBμV DIN45004B @ 860 MHz
- All Gold Metalization for Improved Reliability
- Superior Gain, Return Loss and DC Current Stability with Temperature
- Improved 2nd Order IMD Available (CA922A)

17 dB
40 – 860 MHz
VHF/UHF
CATV/MATV
AMPLIFIERS



CASE 714P–03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	26	V
RF Input Power Per Tone	P_{in}	+16	dBm
Storage Temperature	T_{stg}	– 40 to +100	°C
Operating Case Temperature Range	T_C	– 20 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 75 Ohm System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		Idc	—	400	440	mA
Power Gain (f = 40 MHz)		PG	16.5	17	17.5	dB
Bandwidth		BW	40	—	860	MHz
Slope (40 – 860 MHz)		S	0.2	0.8	1.5	dB
Gain Flatness		FL	—	—	1.0	dB
Input/Output Return Loss	f = 40 – 100 MHz f = 100 – 800 MHz f = 800 – 860 MHz	IRL/ORL	20 15 10/13	— 17 12/15	— — —	dB
Second Order Intermodulation Distortion (V_O = +50 dBmV/ch.)	CA922 CA922A	IMD_2	— —	— —	– 63 – 67	dB dB
DIN45004B (See Figure 1)	f = 40 – 400 MHz f = 400 – 860 MHz	DIN	124 123	— —	— —	dBμV
Noise Figure	f = 500 MHz f = 860 MHz	NF	— —	7.0 8.0	8.5 9.5	dB

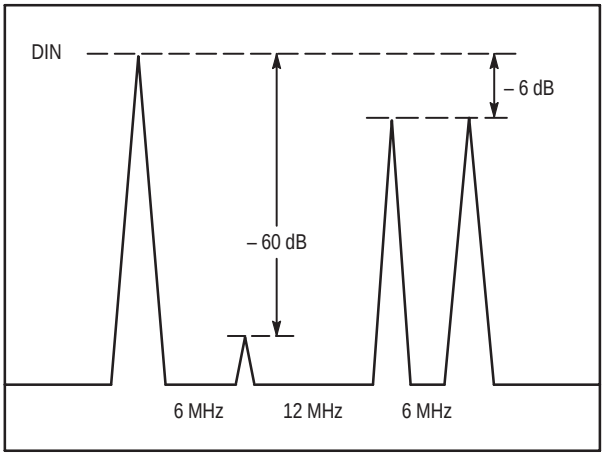


Figure 1. DIN45004B Test

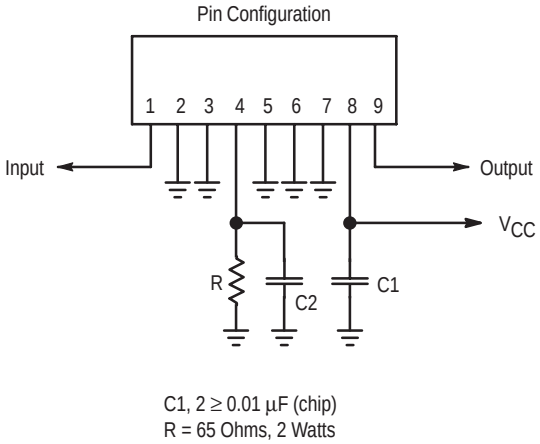


Figure 2. External Connections

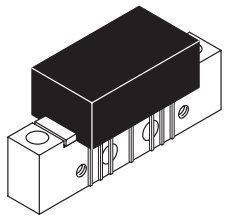
The RF Line
Low Distortion Wideband Amplifiers

MHW1224
MHW1244

Designed specifically for broadband applications requiring low distortion characteristics. Specified for use as return amplifiers for mid–split and high–split 2–way cable TV systems. Features all gold metallization system.

- Guaranteed Broadband Power Gain @ f = 5.0–200 MHz
- Guaranteed Broadband Noise Figure @ f = 5.0–175 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- All Ion–Implanted Arsenic Emitter Transistor Chips with 6.0 GHz f_T's
- Circuit Design Optimized for Good RF Stability Under High VSWR Load Conditions
- Transformers Designed to Insure Good Low Frequency Gain Stability versus Temperature

22.0 dB
24.0 dB
5.0–200 MHz
CATV HIGH–SPLIT
REVERSE AMPLIFIERS



CASE 714Y–03, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+65	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system)

Characteristic	Symbol	MHW1224	MHW1244	Units
Power Gain @ 10 MHz	G_P	22.0 ± 0.5	24.0 ± 0.5	dB
Frequency Range (Response/Return Loss) Note 1	BW	5.0–200		MHz
Cable Slope Equivalent (5.0–200 MHz)	S	–0.2 Min/+0.8 Max		dB
Gain Flatness (5.0–200 MHz)	F	±0.2 Max		dB
Input/Output Return Loss (5.0–200 MHz) Note 1	IRL/ORL	18.0 Min		dB
Cross Modulation Distortion @ +50 dBmV per ch.				
12–Channel FLAT (5.0–120 MHz)	XM_{12}	–67 Typ	–66 Typ	dB
22–Channel FLAT (5.0–175 MHz) (2) (3)	XM_{22}	–62 Max	–61 Max	dB
26–Channel FLAT (5.0–200 MHz)	XM_{26}	–62 Typ	–61 Typ	dB

NOTES:
1. Response and return loss characteristics are tested and guaranteed for the full 5.0–200 MHz frequency range.
2. Motorola 100% distortion and noise figure testing is performed over the 5.0–175 MHz frequency range. Cross modulation and composite triple beat testing are with 22–channel loading; Video carriers used are:

T7–T13	7.0–43.0 MHz	7–Channels
2–6	55.25–83.25 MHz	5–Channels
A–7	121.25–175.25 MHz	10–Channels

3. Video carriers used for 12–Channel typical performances are T7–6; For 26–Channel typical performance, Channels 8, 9, 10 and 11 are added to the 22–Channel carriers listed above.

ELECTRICAL CHARACTERISTICS — continued (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system)

Characteristic	Symbol	MHW1224	MHW1244	Units
Composite Triple Beat Distortion @ +50 dBmV per ch. 22–Channel FLAT (5.0–175 MHz) 26–Channel FLAT (5.0–200 MHz) Notes 2 and 3	 CTB_{22} CTB_{26}	 –69 Max –68.5 Typ	 –68 Max –67.5 Typ	 dB dB
Individual Triple Beat Distortion @ +50 dBmV per ch. Mid–Split (5.0–120 MHz) T11, T12 and CH2 @ 123.25 MHz High–Split (5.0–175 MHz) T13, CH2 and CH5 @ 175.5 MHz	 TB_3 TB_3	 –88 Typ –85 Typ	 –87 Typ –84 Typ	 dB dB
Second Order Distortion @ +50 dBmV per ch. High–Split (5.0–175 MHz) CH2, CHA @ 176.5 MHz	IMD	–72 Max	–72 Max	dB
Noise Figure High–Split (5.0–175 MHz) Note 2	NF	5.5 Max	5.0 Max	dB
DC Current	I_{DC}	210 Typ/240 Max		mAdc

NOTES:

1. Response and return loss characteristics are tested and guaranteed for the full 5.0–200 MHz frequency range.
2. Motorola 100% distortion and noise figure testing is performed over the 5.0–175 MHz frequency range. Cross modulation and composite triple beat testing are with 22–channel loading; Video carriers used are:

T7–T13	7.0–43.0 MHz	7–Channels
2–6	55.25–83.25 MHz	5–Channels
A–7	121.25–175.25 MHz	10–Channels

3. Video carriers used for 12–Channel typical performances are T7–6; For 26–Channel typical performance, Channels 8, 9, 10 and 11 are added to the 22–Channel carriers listed above.

The RF Line

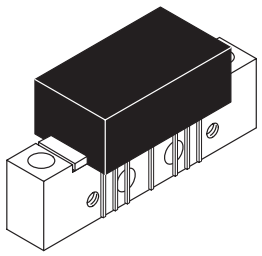
Low Distortion Wideband Reverse Amplifier Module

MHW1254L

24 Vdc, 50 MHz, 25 dB
CATV LOW CURRENT AMPLIFIER

Designed specifically for broadband applications requiring low distortion characteristics. Specified for use as return amplifiers for low–split, 2–way cable TV systems. Features all gold metallization system.

- Guaranteed Broadband Power Gain
- Guaranteed Broadband Noise Figure
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- Circuit Design Optimized for Good RF Stability Under High VSWR Load Conditions
- Transformers Designed to Insure Good Low Frequency Gain Stability versus Temperature



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{IN}	+70	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = 30°C, 75 ohm system, unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Bandwidth		BW	5.0	50	MHz
Power Gain	(f = 5.0 MHz)	Gp	24.3	25.8	dB
Return Loss	(@ f = 5.0–50 MHz)	RL	20	—	dB
Second Order Distortion	(V_{out} = +50 dBmV/ch)	IMD	—	–70	dBc
Cross Modulation	(V_{out} = +50 dBmV/ch)	XMD_4	—	–62	dBc
Triple Beat Distortion	(V_{out} = +50 dBmV/ch)	TB_3	—	–70	dBc
Noise Figure	(f = 50 MHz)	NF	—	4.5	dB
DC Current		IDC	100	135	mA

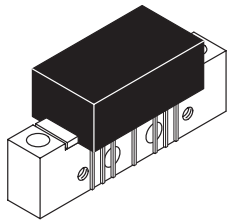
The RF Line
Low Distortion Wideband Reverse Amplifier Modules

Designed specifically for broadband applications requiring low distortion characteristics. Specified for use as return amplifiers for low–split 2–way cable TV systems. Features all gold metallization system.

- Guaranteed Broadband Power Gain
- Guaranteed Broadband Noise Figure
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- Circuit Design Optimized for Good RF Stability Under High VSWR Load Conditions
- Transformers Designed to Insure Good Low Frequency Gain Stability versus Temperature

MHW1304L

24 Vdc
50 MHz
30 dB
CATV LOW CURRENT AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{IN}	+70	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = 30°C, 75 ohm system, unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Bandwidth	All	BW	5.0	50	MHz
Power Gain	(f = 5.0 MHz)	Gp	29.2	30.8	dB
Return Loss	(@ f = 5.0–50 MHz)	RL	18	—	dB
Second Order Distortion	(V_{out} = +50 dBmV/ch)	IMD	—	–70	dBc
Cross Modulation	(V_{out} = +50 dBmV/ch)	XMD_4	—	–57	dBc
Triple Beat Distortion	(V_{out} = +50 dBmV/ch)	TB_3	—	–66	dBc
Noise Figure	(f = 50 MHz)	NF	—	4.5	dB
DC Current		I_{DC}	100	135	mA

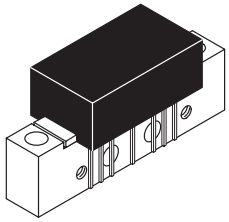
The RF Line
550 MHz CATV Amplifier

MHW6182

. . . designed specifically for 550 MHz CATV applications. Features ion–implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 77 Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 18.2 dB (Typ) @ 50 MHz
  18.8 dB (Min) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 7.0 dB (Max)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion–Implanted Transistors

18 dB GAIN
550 MHz
77–CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIER



CASE 714Y–03, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain — 50 MHz		G_p	17.7	18.2	18.7	dB
Power Gain — 550 MHz		G_p	18.8	19.2	20	dB
Slope		S	0.5	—	2.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.5	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	–85	—	
(V_{out} = +44 dBmV per ch., Ch 2, M30, M39)			—	–80	–72	
Cross Modulation Distortion						dB
(V_{out} = +46 dBmV per ch.)	60–Channel FLAT	XMD_{60}	—	–61	—	
(V_{out} = +44 dBmV per ch.)	77–Channel FLAT	XMD_{77}	—	–64	–62	
Composite Triple Beat						dB
(V_{out} = +46 dBmV per ch.)	60–Channel FLAT	CTB_{60}	—	–62	—	
(V_{out} = +44 dBmV per ch.)	77–Channel FLAT	CTB_{77}	—	–60	–58	
Noise Figure (f = 550 MHz)		NF	—	—	7.0	dB
DC Current		I_{DC}	—	210	240	mA

Product Is on Lifetime Buy.
The next generation of higher performance products are in development. Visit our online Selector Guides (http://mot–sps.com/rf/sg/sg.html) for scheduled introduction dates.

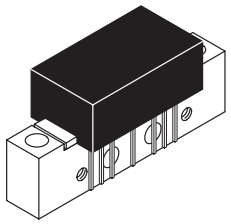
MHW6185B

The RF Line
High Output Doubler 550 MHz CATV Amplifier Module

18 dB GAIN
550 MHz
77–CHANNEL
CATV AMPLIFIER

The MHW6185B is designed specifically for 550 MHz CATV applications. Features ion–implanted arsenic emitter transistors and an all gold metallization system.

- 5th Generation Die Technology
- Specified for 77–Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 18.5 dB Typ @ 50 MHz
  19.5 dB Typ @ 550 MHz
- Broadband Noise Figure
  NF = 4.5 dB Typ @ 50 MHz
- Improvement in Distortion Over Conventional Hybrids
- Allows Higher Output Level Operation



CASE 714Y–03, STYLE 1

LIFETIME BUY

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain	50 MHz 550 MHz	G_p	18 18.8	18.5 19.5	19 20.5	dB
Slope	40–550 MHz	S	0.3	—	2.0	dB
Gain Flatness (Peak To Valley)		—	—	—	0.5	dB
Return Loss — Input/Output (Z_0 = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	dB
Composite Second Order 77 ch, (V_{out} = +44 dBmV)		CSO_{77}	—	–68	–65	dB
Cross Modulation Distortion (77 ch, V_{out} = +44 dBmV @ Fm = 55 MHz		XMD_{77}	—	–78	–68	dB
Signal–to–Triple Beat Noise (77 ch, V_{out} = +44 dBmV)		CTB_{77}	—	–66	–65	dB
Noise Figure	550 MHz	NF	—	6.0	7.5	dB
DC Current (V_{DC} = 24 Vdc, T_C = 30°C)		I_{DC}	380	415	440	mA

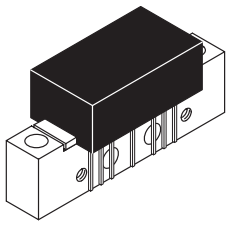
The RF Line
550 MHz CATV Amplifier

. . . designed specifically for 550 MHz CATV applications. Features ion–implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 77–Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 22 dB (Typ) @ 50 MHz
  22 dB (Min) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 6.0 dB (Max)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion–Implanted Transistors

MHW6222

22 dB GAIN
550 MHz
77–CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIER



CASE 714Y–03, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+60	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain — 50 MHz		G_p	21.4	22	22.6	dB
Power Gain — 550 MHz		G_p	22	—	—	dB
Slope		S	0.2	—	1.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	–80	—	
(V_{out} = +44 dBmV per ch., Ch 2, M30, M39)			—	–72	–66	
Cross Modulation Distortion						dB
(V_{out} = +46 dBmV per ch.)	60–Channel FLAT	XMD_{60}	—	–60	—	
(V_{out} = +44 dBmV per ch.)	77–Channel FLAT	XMD_{77}	—	–60	–57	
Composite Triple Beat						dB
(V_{out} = +46 dBmV per ch.)	60–Channel FLAT	CTB_{60}	—	–61	—	
(V_{out} = +44 dBmV per ch.)	77–Channel FLAT	CTB_{77}	—	–59	–57	
Noise Figure (f = 550 MHz)		NF	—	5.0	6.0	dB
DC Current		I_{DC}	—	210	240	mA

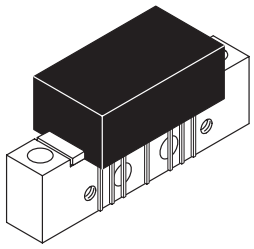
The RF Line

77-Channel (550 MHz) CATV Line Extender Amplifier

MHW6272

- Specified for 60– and 77–Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 27 dB (Typ)
- Broadband Noise Figure
  NF = 6 dB (Typ) @ 550 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

27 dB GAIN
550 MHz
77–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain	50 MHz 550 MHz	G_p	26.2 27	27 —	27.8 29.2	dB
Slope		S	0	1	2	dB
Gain Flatness (Peak To Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz 450–550 MHz	IRL/ORL	18 16	— —	— —	dB
Second Order Intermodulation Distortion (V_{out} = +48 dBmV per ch., Ch 2, 13, R) (V_{out} = +46 dBmV per ch., Ch 2, M6, M15) (V_{out} = +46 dBmV per ch., Ch 2, M13, M22) (V_{out} = +44 dBmV per ch., Ch 2, M30, M39)		IMD	 — — — —	 –80 –78 –76 –69	 — — — –64	dB
Cross Modulation Distortion @ Ch 2 (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.) 	 53–Channel FLAT 60–Channel FLAT 70–Channel FLAT 77–Channel FLAT	 XMD_{53} XMD_{60} XMD_{70} XMD_{77}	 — — — —	 –63 –62 –61 –59	 — — — –57	dB
Composite Triple Beat (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.) 	 53–Channel FLAT 60–Channel FLAT 70–Channel FLAT 77–Channel FLAT	 TB_{53} TB_{60} TB_{70} TB_{77}	 — — — —	 –63 –62 –61 –59	 — — — –57	dB
Noise Figure	550 MHz	NF	—	6.0	6.5	dB
DC Current		I_{DC}	—	310	340	mA

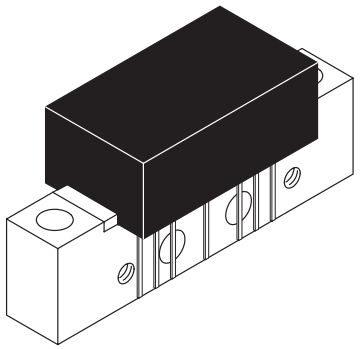
The RF Line
77-Channel (550 MHz) CATV Amplifier

The MHW6342T is designed specifically for 550 MHz CATV applications. Features ion–implanted arsenic emitter transistors with 7 GHz f_T and an all gold metallization system.

- Specified for 77–Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 34.5 dB (Typ) @ 50 MHz
  35.2 dB (Typ) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 5.5 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz Ion–Implanted Transistors

MHW6342T

34 dB GAIN
550 MHz
77–CHANNEL
CATV AMPLIFIER



CASE 1302–01, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain	50 MHz	G_p	33.5	34.5	35.5	dB
Power Gain	550 MHz	G_p	34.5	35.2	—	dB
Slope		S	0	0.7	2	dB
Gain Flatness (Peak To Valley)		—	—	0.3	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz 450–550 MHz	IRL/ORL	18 16	— —	— —	dB
Second Order Intermodulation Distortion (V_{out} = +46 dBmV per ch., Ch 2, M13, M22) (V_{out} = +44 dBmV per ch., Ch 2, M30, M39)		IMD	 — —	 –80 –74	 — —	dB
Cross Modulation Distortion (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 60–Channel FLAT 77–Channel FLAT	 XMD_{60} XMD_{77}	 — —	 –62 –63	 — –57	dB

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

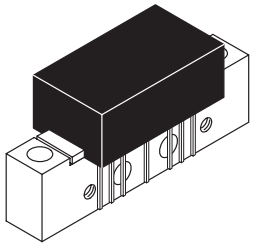
Composite Triple Beat (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 60–Channel FLAT 77–Channel FLAT	 CTB_{60} CTB_{77}	 — —	 –64 –63	 — –57	dB
Composite Second Order (V_{out} = +46 dBmV/ch, 60–Channel FLAT) (V_{out} = +44 dBmV/ch, 77–Channel FLAT)		 CSO_{60} CSO_{77}	 — —	 –70 –65	 — –57	dB
Noise Figure	550 MHz	NF	—	5.5	6.5	dB
DC Current		I_{DC}	—	310	340	mA

The RF Line
110-Channel 750 MHz CATV Amplifier

MHW7182B

- Specified for 77 and 110–Channel Performance
- Broadband Power Gain — @ f = 750 MHz
  G_p = 19 dB (Typ)
- Broadband Noise Figure
  NF = 5.0 dB (Typ) @ 750 MHz
- All Gold Metallization
- Improved Distortion Performance

18 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	18 18.2	18.5 19	19 20	dB
Slope	40–750 MHz	S	0	0.4	1	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 20 —	 — —	 — 0.005	 dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CSO_{110} CSO_{77}	 — —	 –70 –70	 –63 –64	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 110–Channel FLAT 77–Channel FLAT	 XMD_{110} XMD_{77}	 — —	 –66 –61	 –64 –59	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CTB_{110} CTB_{77}	 — —	 –68 –66	 –66 –64	dBc
Noise Figure	50 MHz 550 MHz 750 MHz	NF	— — —	4.0 4.5 5.0	5.0 — 6.5	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	180	220	240	mA

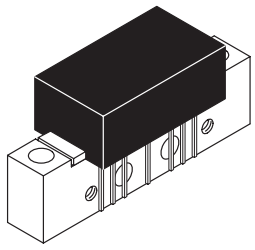
The RF Line

High Output Power Doubler 750 MHz CATV Amplifier

MHW7185C

- Specified for 77 and 110–Channel Performance
- Broadband Power Gain — @ f = 40–750 MHz
  G_p = 19.4 dB (Typ)
- Broadband Noise Figure
  NF = 6.2 dB (Typ) @ 750 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

19.4 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

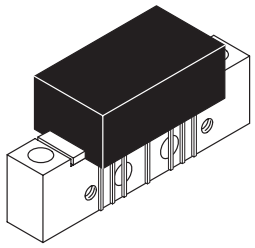
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	18.3 19	18.8 19.4	19.3 20	dB
Slope	40–750 MHz	S	0	0.4	1.0	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 19 —	 — —	 — 0.006	 dB dB/MHz
Composite Second Order (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CSO_{110} CSO_{77}	 — —	 –72 –80	 –64 –68	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 110–Channel FLAT 77–Channel FLAT	 XMD_{110} XMD_{77}	 — —	 –66 –70	 –63 –68	dBc
Composite Triple Beat (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CTB_{110} CTB_{77}	 — —	 –64 –71	 –62 –69	dBc
Noise Figure	50 MHz 550 MHz 750 MHz	NF	— — —	5.0 5.8 6.2	6.0 — 7.5	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	365	400	435	mA

The RF Line
High Output Power Doubler 750 MHz CATV Amplifier

MHW7185CL

- Specified for 77 and 110–Channel Performance
- Broadband Power Gain — @ f = 750 MHz
  G_p = 19.2 dB (Typ)
- Broadband Noise Figure
  NF = 6.5 dB (Typ) @ 750 MHz
- All Gold Metallization
- Lower DC Current Consumption
- Superior DC Current Stability with Temperature

19.2 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

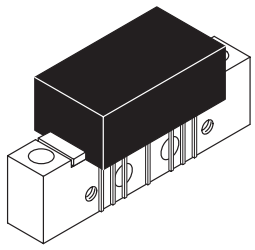
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	18 18.7	18.5 19.2	19 19.7	dB
Slope	40–750 MHz	S	0.3	0.6	1.3	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 20 —	 — —	 — 0.007	 dB dB/MHz
Composite Second Order (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CSO_{110} CSO_{77}	 — —	 –70 –83	 –64 –68	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 110–Channel FLAT 77–Channel FLAT	 XMD_{110} XMD_{77}	 — —	 –66 –69	 –63 –67	dBc
Composite Triple Beat (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CTB_{110} CTB_{77}	 — —	 –63.5 –70	 –61 –68	dBc
Noise Figure	50 MHz 550 MHz 750 MHz	NF	— — —	5.3 5.8 6.5	6.2 — 7.5	dB
DC Current (V_{DC} = 24 V, T_C = –20 to +100°C)		I_{DC}	345	370	385	mA

The RF Line
High Output Power Doubler 750 MHz CATV Amplifier

MHW7205C

- Specified for 77 and 110–Channel Performance
- Broadband Power Gain — @ f = 40–750 MHz
  G_p = 20.2 dB (Typ)
- Broadband Noise Figure
  NF = 6.2 dB (Typ) @ 750 MHz
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors
- Composite Triple Beat — @ 110–Channel Loading
  CTB = –63 dB (Typ)

20.2 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

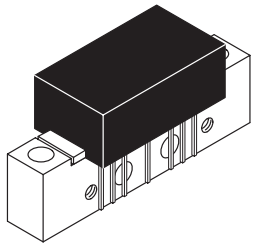
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	19.3 20	19.8 20.2	20.3 21	dB
Slope	40–750 MHz	S	0	0.4	1.0	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_0 = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 19 —	 — —	 — 0.006	 dB dB/MHz
Composite Second Order (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CSO_{110} CSO_{77}	 — —	 –70 –80	 –63 –68	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 110–Channel FLAT 77–Channel FLAT	 XMD_{110} XMD_{77}	 — —	 –67 –70	 –62 –68	dBc
Composite Triple Beat (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CTB_{110} CTB_{77}	 — —	 –63 –71	 –61 –69	dBc
Noise Figure	50 MHz 550 MHz 750 MHz	NF	— — —	5.0 5.8 6.2	6.0 — 7.5	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	365	400	435	mA

The RF Line
High Output Power Doubler 750 MHz CATV Amplifier

MHW7205CL

- Specified for 77 and 110–Channel Performance
- Broadband Power Gain — @ f = 750 MHz
  G_p = 20 dB (Typ)
- Broadband Noise Figure
  NF = 6.2 dB (Typ) @ 750 MHz
- Composite Triple Beat — @ 110–Channel Loading
  CTB = –63 dB (Typ)
- Lower DC Current Consumption and Superior DC Stability with Temperature

20 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	19 19.7	19.5 20	20 21.2	dB
Slope	40–750 MHz	S	0.2	0.5	1.7	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.3	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 20 —	 — —	 — 0.007	 dB dB/MHz
Composite Second Order (V_{out} = +44 dBmV/ch., Worst Case) 110–Channel FLAT 77–Channel FLAT		 CSO_{110} CSO_{77}	 — —	 –69 –80	 –63 –67	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +44 dBmV/ch., FM = 55 MHz) 110–Channel FLAT 77–Channel FLAT		 XMD_{110} XMD_{77}	 — —	 –65 –69	 –62 –66	dBc
Composite Triple Beat (V_{out} = +44 dBmV/ch., Worst Case) 110–Channel FLAT 77–Channel FLAT		 CTB_{110} CTB_{77}	 — —	 –63 –70	 –61 –68	dBc
Noise Figure	50 MHz 550 MHz 750 MHz	NF	— — —	5.0 5.8 6.2	6.2 — 7.5	dB
DC Current (V_{DC} = 24 V, T_C = –20 to +100°C)		I_{DC}	345	365	385	mA

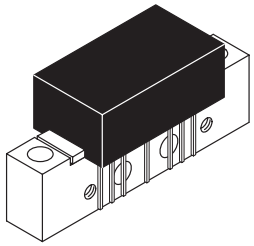
The RF Line
110-Channel (750 MHz) CATV Amplifier

MHW7222A

The MHW7222A is designed specifically for up to 750 MHz CATV systems as amplifiers in trunk and line extender applications. This amplifier features ion–implanted, arsenic emitter transistors, an all gold metallization system and offers improved ruggedness and distortion performance.

- Specified for 110–Channel Performance
- Broadband Power Gain — @ f = 40–750 MHz
  G_p = 22.3 dB Typ @ 750 MHz
- Broadband Noise Figure
  NF = 5.5 dB Typ
- All Gold Metallization

22 dB GAIN
750 MHz
110 CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+70	dBmV
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	f = 50 MHz f = 750 MH	G_p	20.8 22	21.5 22.3	22.2 24	dB
Slope (f = 40–750 MHz)		S	0	1	2	—
Gain Flatness (Peak To Valley)	(f = 40–750 MHz)	G_f	—	0.4	0.6	—
Input/Output Return Loss @ f = 40 MHz		IRL/ORL	20	24	—	dB
Derate Return Loss @ f > 40 MHz		RLD	—	—	0.008	dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch; 110 Channels) (V_{out} = +44 dBmV/ch; 77 Channels)		 CSO_{110} CSO_{77}	 — —	 –65 –65	 –57 —	dB

(continued)

ELECTRICAL CHARACTERISTICS — continued

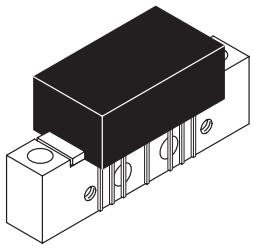
Characteristic		Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion (V_{out} = +40 dBmV/ch, 110–Channel @ Fm = 55.25 MHz) (V_{out} = +44 dBmV/ch, 77–Channel @ Fm = 55.25 MHz)		 XMD_{110} XMD_{77}	 — —	 –64 –60	 –60 —	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch, 110–Channels, Worst Case) (V_{out} = +44 dBmV/ch, 77–Channels, Worst Case)		 CTB_{110} CTB_{77}	 — —	 –63 –62	 –60 —	dBc
Noise Figure	f = 50 MHz f = 750 MHz	NF	— —	3.6 5.5	5 7	dB
DC Current		I_{DC}	180	220	240	mA

The RF Line
110-Channel (750 MHz) CATV Line Extender Amplifier

MHW7242B

- Specified for 110–Channel Performance
- Broadband Power Gain — @ f = 40–750 MHz
  G_p = 24.7 dB (Typ)
- Broadband Noise Figure
  NF = 7 dB (Max) @ 750 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

24 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

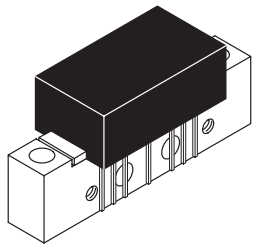
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	23.2 24	24.0 24.7	24.8 25.5	dB
Slope	40–750 MHz	S	0	0.7	1.5	dB
Gain Flatness (40–750 MHz, Peak To Valley)		—	—	0.3	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CSO_{110} CSO_{77}	 — —	 –68 –73	 –62 –62	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 110–Channel FLAT 77–Channel FLAT	 XMD_{110} XMD_{77}	 — —	 –60 –55	 –58 –53	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CTB_{110} CTB_{77}	 — —	 –66 –63	 –63 –61	dBc
Noise Figure	50 MHz 750 MHz	NF	— —	4.8 5.5	5.5 7	dB
DC Current		I_{DC}	280	316	350	mA

The RF Line
110-Channel (750 MHz) CATV Line Extender Amplifier

MHW7272A

- 24 V Supply Voltage
- Specified for 110–Channel Performance
- Typical Noise Figure
  NF = 5.5 dB @ 750 MHz
- All Gold Metallization
- Improved CTB Performance over Previous Versions

27 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	26.2 27	27.2 27.7	27.8 29	dB
Slope	40–750 MHz	S	0	0.7	1.5	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CSO_{110}	—	–70	–64	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–63	–60	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–68	–64	dBc
Noise Figure	50 MHz 750 MHz	NF	— —	— 5.5	5.5 6.5	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	280	310	350	mA

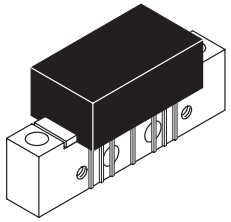
The RF Line

110-Channel (750 MHz) CATV Line Extender Amplifier

MHW7292

- 24 V Supply Voltage
- Specified for 110–Channel Performance
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

29 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

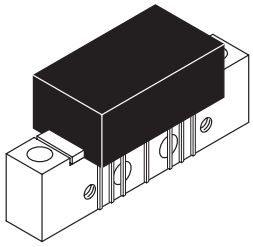
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	28.2 29	29 29.8	29.8 31	dB
Slope	40–750 MHz	S	0	0.7	2	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_0 = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CSO_{110}	—	–70	–60	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–62	–60	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–62	–60	dBc
Noise Figure	50 MHz 750 MHz	NF	— —	— 5.5	5.5 6.5	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	280	310	350	mA

The RF Line
128-Channel 860 MHz CATV Amplifier

MHW8182B

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 860 MHz
  G_p = 19.1 dB (Typ)
- Broadband Noise Figure
  NF = 5.5 dB (Typ) @ 860 MHz
- All Gold Metallization
- Improved CTB Distortion Performance

18 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	18 18.2	18.5 19.1	19 20.5	dB
Slope	40–860 MHz	S	0	0.7	2.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 20 —	 — —	 — 0.005	 dB dB/MHz
Composite Second Order (V_{out} = +38 dBmV/ch., Worst Case) (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CSO_{128} CSO_{110} CSO_{77}	 — — —	 –71 –70 –70	 –64 –63 –64	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +38 dBmV/ch., FM = 55 MHz) (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 XMD_{128} XMD_{110} XMD_{77}	 — — —	 –68 –66 –61	 –65 –64 –59	dBc
Composite Triple Beat (V_{out} = +38 dBmV/ch., Worst Case) (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CTB_{128} CTB_{110} CTB_{77}	 — — —	 –69 –68 –66	 –66 –66 –64	dBc
Noise Figure	50 MHz 550 MHz 750 MHz 860 MHz	NF	— — — —	4.0 4.5 5.0 5.5	5.0 — 6.5 7.5	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	180	220	240	mA

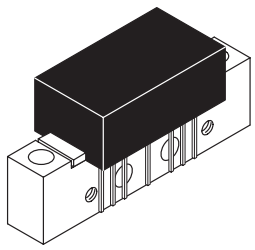
The RF Line

High Output Power Doubler 860 MHz CATV Amplifier

MHW8185

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 19.4 dB (Typ)
- Broadband Noise Figure
  NF = 7 dB (Typ) @ 860 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

19.4 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

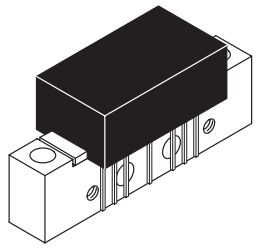
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	18.3 19	18.8 19.4	19.3 20.5	dB
Slope	40–860 MHz	S	0	.5	1.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.3	1.0	dB
Return Loss — Input/Output (Z_0 = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 19 —	 — —	 — 0.006	 dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CSO_{128} CSO_{110} CSO_{77}	 — — —	 –70 –72 –80	 –62 –64 –68	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 XMD_{128} XMD_{110} XMD_{77}	 — — —	 –72 –67 –70	 –64 –63 –68	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CTB_{128} CTB_{110} CTB_{77}	 — — —	 –67 –64 –71	 –64 –62 –69	dBc
Noise Figure	50 MHz 550 MHz 750 MHz 860 MHz	NF	— — — —	5.0 5.8 6.2 7.0	6.0 — — 8.0	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	365	400	435	mA

The RF Line
High Output Power Doubler 870 MHz CATV Amplifier

MHW8185L

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 40–870 MHz
  G_p = 19.4 dB (Typ)
- Lower DC Current Consumption
- Superior DC Current Stability with Temperature

19.4 dB GAIN
870 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

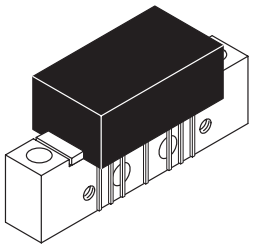
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	870	MHz
Power Gain	50 MHz 870 MHz	G_p	18 19	18.5 19.4	19 20.5	dB
Slope	40–870 MHz	S	0.4	0.9	1.4	dB
Gain Flatness (40–870 MHz, Peak–to–Valley)		—	—	0.3	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 20 —	 — —	 — 0.007	 dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CSO_{128} CSO_{110} CSO_{77}	 — — —	 –69 –70 –85	 –62 –64 –68	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 XMD_{128} XMD_{110} XMD_{77}	 — — —	 –72 –66 –69	 –64 –63 –67	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CTB_{128} CTB_{110} CTB_{77}	 — — —	 –66 –63 –70	 –63 –61 –68	dBc
Noise Figure	50 MHz 550 MHz 750 MHz 870 MHz	NF	— — — —	5.3 5.8 6.6 7.8	6.2 — — 8.5	dB
DC Current (V_{DC} = 24 V, T_C = –20 to +100°C)		I_{DC}	345	365	385	mA

The RF Line
High Output Power Doubler 870 MHz CATV Amplifier

MHW8185LR

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 40–870 MHz
  G_p = 19.4 dB (Typ)
- Lower DC Current Consumption
- Superior DC Current Stability with Temperature

19.4 dB GAIN
870 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	870	MHz
Power Gain	50 MHz 870 MHz	G_p	18 19	18.5 19.4	19 20.5	dB
Slope	40–870 MHz	S	0.4	0.9	1.4	dB
Gain Flatness (40–870 MHz, Peak–to–Valley)		—	—	0.3	0.8	dB
Return Loss — Input/Output (Z_0 = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 20 —	 — —	 — 0.007	 dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CSO_{128} CSO_{110} CSO_{77}	 — — —	 –69 –70 –85	 –62 –64 –68	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 XMD_{128} XMD_{110} XMD_{77}	 — — —	 –72 –66 –69	 –64 –63 –67	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CTB_{128} CTB_{110} CTB_{77}	 — — —	 –66 –63 –70	 –63 –61 –68	dBc
Noise Figure	50 MHz 550 MHz 750 MHz 870 MHz	NF	— — — —	5.3 5.8 6.6 7.8	6.2 — — 8.5	dB
DC Current (V_{DC} = 24 V, T_C = –20 to +100°C)		I_{DC}	345	365	385	mA

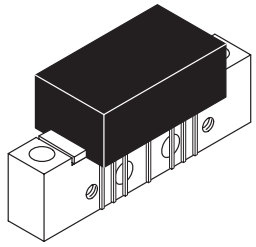
The RF Line

High Output Mirror Power Doubler 860 MHz CATV Amplifier

MHW8185R

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 860 MHz
  G_p = 19.4 dB (Typ)
- Broadband Noise Figure
  NF = 7 dB (Typ) @ 860 MHz
- Pin Configuration Mirrors that of MHW8185
- Typical CTB @ 860 MHz under 128–Channel FLAT Loading = –67 dBc
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

19.4 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	18.3 19	18.8 19.4	19.3 20.5	dB
Slope	40–860 MHz	S	0	.5	1.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.3	1.0	dB
Return Loss — Input/Output (Z_o = 75 Ohms)		IRL/ORL				
	@ 40 MHz		19	—	—	dB
	@ f > 40 MHz (Derate)		—	—	0.006	dB/MHz
Composite Second Order						dBc
(V_{out} = +40 dBmV/ch., Worst Case)	128–Channel FLAT	CSO_{128}	—	–70	–62	
(V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT	CSO_{110}	—	–72	–64	
	77–Channel FLAT	CSO_{77}	—	–80	–68	
Cross Modulation Distortion @ Ch 2						dBc
(V_{out} = +40 dBmV/ch., FM = 55 MHz)	128–Channel FLAT	XMD_{128}	—	–72	–64	
(V_{out} = +44 dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–67	–63	
	77–Channel FLAT	XMD_{77}	—	–70	–68	
Composite Triple Beat						dBc
(V_{out} = +40 dBmV/ch., Worst Case)	128–Channel FLAT	CTB_{128}	—	–67	–64	
(V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–64	–62	
	77–Channel FLAT	CTB_{77}	—	–71	–69	
Noise Figure	50 MHz	NF	—	5.0	6.0	dB
	550 MHz		—	5.8	—	
	750 MHz		—	6.2	—	
	860 MHz		—	7.0	8.0	
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	365	400	435	mA

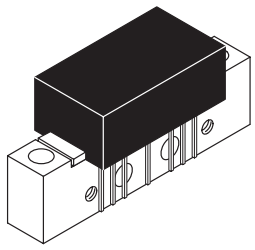
The RF Line

High Output Power Doubler 860 MHz CATV Amplifier

MHW8205

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 20.2 dB (Typ)
- Broadband Noise Figure
  NF = 7 dB (Typ) @ 860 MHz
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors
- Composite Triple Beat — @ 128–Channel Loading
  CTB = –66 dB (Typ)

20.2 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

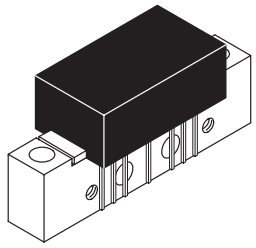
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	19.3 20	19.8 20.2	20.3 21.5	dB
Slope	40–860 MHz	S	0	.4	1.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.3	1.0	dB
Return Loss — Input/Output (Z_0 = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 19 —	 — —	 — 0.006	 dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CSO_{128} CSO_{110} CSO_{77}	 — — —	 –69 –70 –80	 –60 –63 –68	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 XMD_{128} XMD_{110} XMD_{77}	 — — —	 –72 –67 –71	 –64 –62 –68	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CTB_{128} CTB_{110} CTB_{77}	 — — —	 –66 –63 –71	 –63 –61 –69	dBc
Noise Figure	50 MHz 550 MHz 750 MHz 860 MHz	NF	— — — —	5.0 5.8 6.2 7.0	6.0 — — 8.0	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	365	400	435	mA

The RF Line
High Output Power Doubler 870 MHz CATV Amplifier

MHW8205L

20.4 dB GAIN
870 MHz
128–CHANNEL
CATV AMPLIFIER

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 870 MHz
  G_p = 20.4 dB (Typ)
- Broadband Noise Figure
  NF = 7.7 dB (Typ) @ 870 MHz
- 7 GHz f_T Ion–Implanted Transistors
- Composite Triple Beat — @ 128–Channel Loading
  CTB = –66 dB (Typ)
- Lower DC Current Consumption and Superior DC Stability with Temperature



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	870	MHz
Power Gain	50 MHz 870 MHz	G_p	19 19.8	19.5 20.4	20 21.3	dB
Slope	40–870 MHz	S	0.2	0.8	1.7	dB
Gain Flatness (40–870 MHz, Peak to Valley)		—	—	0.5	1.0	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 20 —	 — —	 — 0.007	 dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CSO_{128} CSO_{110} CSO_{77}	 — — —	 –69 –70 –80	 –60 –63 –67	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 XMD_{128} XMD_{110} XMD_{77}	 — — —	 –72 –65 –69	 –64 –62 –66	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CTB_{128} CTB_{110} CTB_{77}	 — — —	 –66 –63 –70	 –63 –61 –68	dBc
Noise Figure	50 MHz 550 MHz 750 MHz 870 MHz	NF	— — — —	5.0 5.8 6.2 7.7	6.2 — — 8.5	dB
DC Current (V_{DC} = 24 V, T_C = –20°C to +100°C)		I_{DC}	345	365	385	mA

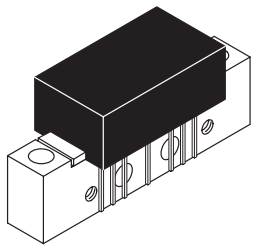
The RF Line

High Output Mirror Power Doubler 860 MHz CATV Amplifier

MHW8205R

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 20.2 dB (Typ)
- Broadband Noise Figure
  NF = 7 dB (Typ) @ 860 MHz
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors
- Composite Triple Beat — @ 128–Channel Loading
  CTB = –66 dB (Typ)

20.2 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	19.3 20	19.8 20.2	20.3 21.5	dB
Slope	40–860 MHz	S	0	.4	1.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.3	1.0	dB
Return Loss — Input/Output (Z_0 = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 19 —	 — —	 — 0.006	 dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CSO_{128} CSO_{110} CSO_{77}	 — — —	 –69 –70 –80	 –60 –63 –68	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 XMD_{128} XMD_{110} XMD_{77}	 — — —	 –72 –67 –71	 –64 –62 –68	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CTB_{128} CTB_{110} CTB_{77}	 — — —	 –66 –63 –71	 –63 –61 –69	dBc
Noise Figure	50 MHz 550 MHz 750 MHz 860 MHz	NF	— — — —	5.0 5.8 6.2 7.0	6.0 — — 8.0	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	365	400	435	mA

Product Is on Lifetime Buy.
The next generation of higher performance products are in development. Visit our online Selector Guides (http://mot–sps.com/rf/sg/sg.html) for scheduled introduction dates.

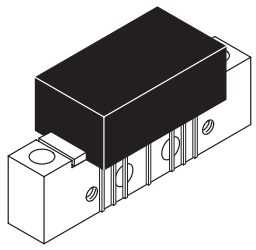
MHW8222

The RF Line
128-Channel (860 MHz) CATV Amplifier

22 dB GAIN
860 MHz
128 CHANNEL
CATV AMPLIFIER

The MHW8222 is designed specifically for up to 860 MHz CATV systems as amplifiers in trunk and line extender applications. These amplifiers feature ion–implanted, arsenic emitter transistors and an all gold metallization system.

- Specified for 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 22.3 dB Typ @ 860 MHz
- Broadband Noise Figure
  NF = 6.4 dB Typ
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization



CASE 714Y–03, STYLE 1

LIFETIME BUY

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+70	dBmV
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	f = 50 MHz f = 860 MHz	G_p	20.8 21.8	21.5 22.3	22.2 24	dB
Slope (f = 40–860 MHz)		S	0	1	2	—
Gain Flatness (Peak To Valley)	(f = 40–860 MHz)	—	—	—	0.4	0.8	—
Input/Output Return Loss @ f = 40 MHz		IRL/ORL	20	24	—	dB
Derate Return Loss @ f > 40 MHz		RLD	—	—	0.009	dB/MHz
Composite Second Order (V_{out} = +38 dBmV/ch; 128 Channels)		CSO_{128}	—	–63	–56	dB
Cross Modulation Distortion (V_{out} = +38 dBmV/ch, 128–Channel @ Fm = 55.25 MHz)		XMD_{128}	—	–68	–60	dBc
Composite Triple Beat (V_{out} = +38 dBmV/ch, 128–Channels, Worst Case)		CTB_{128}	—	–62	–60	dBc
Noise Figure	f = 50 MHz f = 860 MHz	NF	— —	3.6 6.4	5 7.5	dB
DC Current		I_{DC}	180	220	240	mA

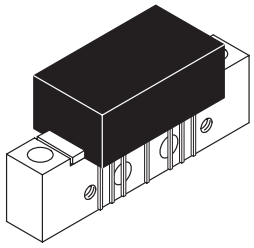
The RF Line

128-Channel (860 MHz) CATV Line Extender Amplifier

MHW8242B

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 24.8 dB (Typ)
- Broadband Noise Figure
  NF = 7.5 dB (Max) @ 860 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

24 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	23.2 24	24.0 24.8	24.8 25.5	dB
Slope	40–860 MHz	S	0	0.8	1.6	dB
Gain Flatness (40–860 MHz, Peak To Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order						dBc
(V_{out} = +38 dBmV/ch., Worst Case)	128–Channel FLAT	CSO_{128}	—	–69	–62	
(V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CSO_{110}	—	–68	–62	
(V_{out} = +44 dBmV/ch., Worst Case)	77–Channel FLAT	CSO_{77}	—	–73	–62	
Cross Modulation Distortion @ Ch 2						dBc
(V_{out} = +38 dBmV/ch., FM = 55 MHz)	128–Channel FLAT	XMD_{128}	—	–63	–60	
(V_{out} = +40 dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–60	–58	
(V_{out} = +44 dBmV/ch., FM = 55 MHz)	77–Channel FLAT	XMD_{77}	—	–55	–53	
Composite Triple Beat						dBc
(V_{out} = +38 dBmV/ch., Worst Case)	128–Channel FLAT	CTB_{128}	—	–68	–64	
(V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–66	–63	
(V_{out} = +44 dBmV/ch., Worst Case)	77–Channel FLAT	CTB_{77}	—	–63	–61	
Noise Figure	50 MHz 860 MHz	NF	— —	4.8 5.8	5.5 7.5	dB
DC Current		I_{DC}	280	316	350	mA

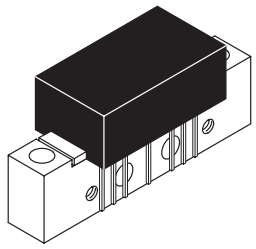
The RF Line

128-Channel (860 MHz) CATV Line Extender Amplifier

MHW8272A

- Specified for 128–Channel Performance
- Broadband Power Gain — @ f = 50 MHz
  G_p = 27.2 dB (Typ)
- Broadband Noise Figure
  NF = 6 dB (Typ) @ 860 MHz
- All Gold Metallization
- Improved CTB Performance over Previous Version

27 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

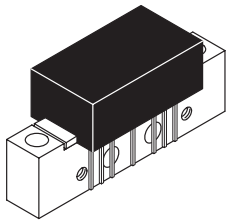
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	26.2 27	27.2 27.7	27.8 29.5	dB
Slope	40–860 MHz	S	0	0.6	2	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 20 —	 — —	 — 0.007	 dB dB/MHz
Composite Second Order (V_{out} = +38 dBmV/ch., Worst Case)	128–Channel FLAT	CSO_{128}	—	–69	–64	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +38 dBmV/ch., FM = 55 MHz)	128–Channel FLAT	XMD_{128}	—	–65	–62	dBc
Composite Triple Beat (V_{out} = +38 dBmV/ch., Worst Case)	128–Channel FLAT	CTB_{128}	—	–69	–64	dBc
Noise Figure	50 MHz 860 MHz	NF	— —	— 6.0	5.5 7.0	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	280	310	350	mA

The RF Line
128-Channel (860 MHz) CATV Line Extender Amplifier

MHW8292

- Specified for 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 29 dB (Typ)
- Broadband Noise Figure
  NF = 6 dB (Typ) @ 860 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

29 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

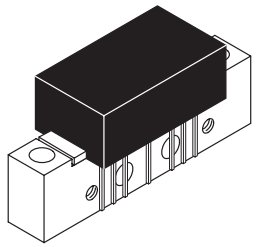
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	28.2 29	29 —	29.8 31.5	dB
Slope	40–860 MHz	S	0	1.0	2.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 20 —	 — —	 — 0.007	 dB dB/MHz
Composite Second Order (V_{out} = +38 dBmV/ch., Worst Case)	128–Channel FLAT	CSO_{128}	—	—	–56	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +38 dBmV/ch., FM = 55 MHz)	128–Channel FLAT	XMD_{128}	—	—	–60	dBc
Composite Triple Beat (V_{out} = +38 dBmV/ch., Worst Case)	128–Channel FLAT	CTB_{128}	—	—	–60	dBc
Noise Figure	50 MHz 860 MHz	NF	— —	— 6.0	5.5 7.0	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	280	310	350	mA

The RF Line
152-Channel 1000 MHz CATV Amplifier

MHW9182B

- Specified for 152–Channel Performance
- Broadband Power Gain — @ f = 1000 MHz
  G_p = 19.4 dB (Typ)
- Broadband Noise Figure
  NF = 6 dB (Typ) @ 1000 MHz
- All Gold Metallization
- Improved Ruggedness and Composite Second Order Distortion Performance

19.4 dB GAIN
1000 MHz
152–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

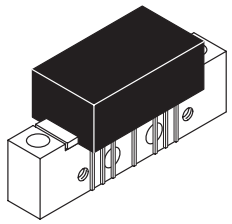
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	1000	MHz
Power Gain	50 MHz 1000 MHz	G_p	18 18.7	18.5 19.4	19 20.7	dB
Slope	40–1000 MHz	S	0.4	0.9	1.4	dB
Gain Flatness (40–1000 MHz, Peak to Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 20 —	 — —	 — 0.006	 dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +38 dBmV/ch., Worst Case)	 110–Channel FLAT 152–Channel FLAT	 CSO_{110} CSO_{152}	 — —	 70 –69	 –63 –63	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +38 dBmV/ch., FM = 55 MHz)	 110–Channel FLAT 152–Channel FLAT	 XMD_{110} XMD_{152}	 — —	 –66 –65	 –64 –61	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +38 dBmV/ch., Worst Case)	 110–Channel FLAT 152–Channel FLAT	 CTB_{110} CTB_{152}	 — —	 –68 –64	 –66 –61	dBc
Noise Figure	50 MHz 550 MHz 860 MHz 1000 MHz	NF	— — — —	4.0 4.5 5.5 6.0	5.0 — — 7.5	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	180	210	240	mA

The RF Line
152-Channel (1000 MHz) CATV Line Extender Amplifier

- Specified for 152–Channel Performance
- Broadband Power Gain — @ f = 40–1000 MHz
  G_p = 24 dB
- Broadband Noise Figure
  NF = 8 dB (Max) @ 1000 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

MHW9242A

24 dB GAIN
1000 MHz
152–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	1000	MHz
Power Gain	50 MHz 1000 MHz	G_p	23.2 24	— —	24.8 26	dB
Slope	40–1000 MHz	S	0	—	2.5	dB
Gain Flatness (40–1000 MHz, Peak–to–Valley)		—	—	—	1.0	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ f > 40 MHz (Derate)	@ 40 MHz	IRL/ORL	20 —	— —	— 0.01	dB dB/MHz
Composite Second Order						dBc
(V_{out} = +38 dBmV/ch; Worst Case)	152–Channel FLAT	CSO_{152}	—	–66	–61	
(V_{out} = +38 dBmV/ch; Worst Case)	128–Channel FLAT	CSO_{128}	—	–69	—	
(V_{out} = +40 dBmV/ch;Worst Case)	110–Channel FLAT	CSO_{110}	—	–69	—	
(V_{out} = +44 dBmV/ch; Worst Case)	77–Channel FLAT	CSO_{77}	—	–78	—	
Cross Modulation Distortion @ Ch 2						dBc
(V_{out} = +38 dBmV/ch., FM= 55 MHz)	152–Channel FLAT	XMD_{152}	—	–62	–59	
(V_{out} = +38 dBmV/ch, FM = 55.25 MHz)	128–Channel FLAT	XMD_{128}	—	–65	—	
(V_{out} = +40 dBmV/ch, FM = 55.25 MHz)	110–Channel FLAT	XMD_{110}	—	–63	—	
(V_{out} = +44 dBmV/ch, FM = 55.25 MHz)	77–Channel FLAT	XMD_{77}	—	–58	—	

ELECTRICAL CHARACTERISTICS — continued

Characteristic		Symbol	Min	Typ	Max	Unit
Composite Triple Beat						dBc
(V_{out} = +38 dBmV/ch., Worst Case)	152–Channel FLAT	CTB_{152}	—	–64	–61	
(V_{out} = +38 dBmV/ch, Worst Case)	128–Channel FLAT	CTB_{128}	—	–68	—	
(V_{out} = +40 dBmV/ch, Worst Case)	110–Channel FLAT	CTB_{110}	—	–67	—	
(V_{out} = +44 dBmV/ch, Worst Case)	77–Channel FLAT	CTB_{77}	—	–64	—	
Noise Figure	f = 50 MHz	NF	—	4.8	5.5	dB
	f = 750 MHz		—	5.5	7.0	
	f = 860 MHz		—	5.8	7.5	
	f = 1000 MHz		—	—	8.0	
DC Current		I_{DC}	280	318	350	mA

Chapter Eight
Tape and Reel Specifications

Motorola offers the convenience of Tape and Reel packaging for our growing family of standard integrated circuit products. Reels are available to support the requirements of both first and second generation pick–and–place equipment. The packaging fully conforms to the latest EIA–481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel–back cover tape.

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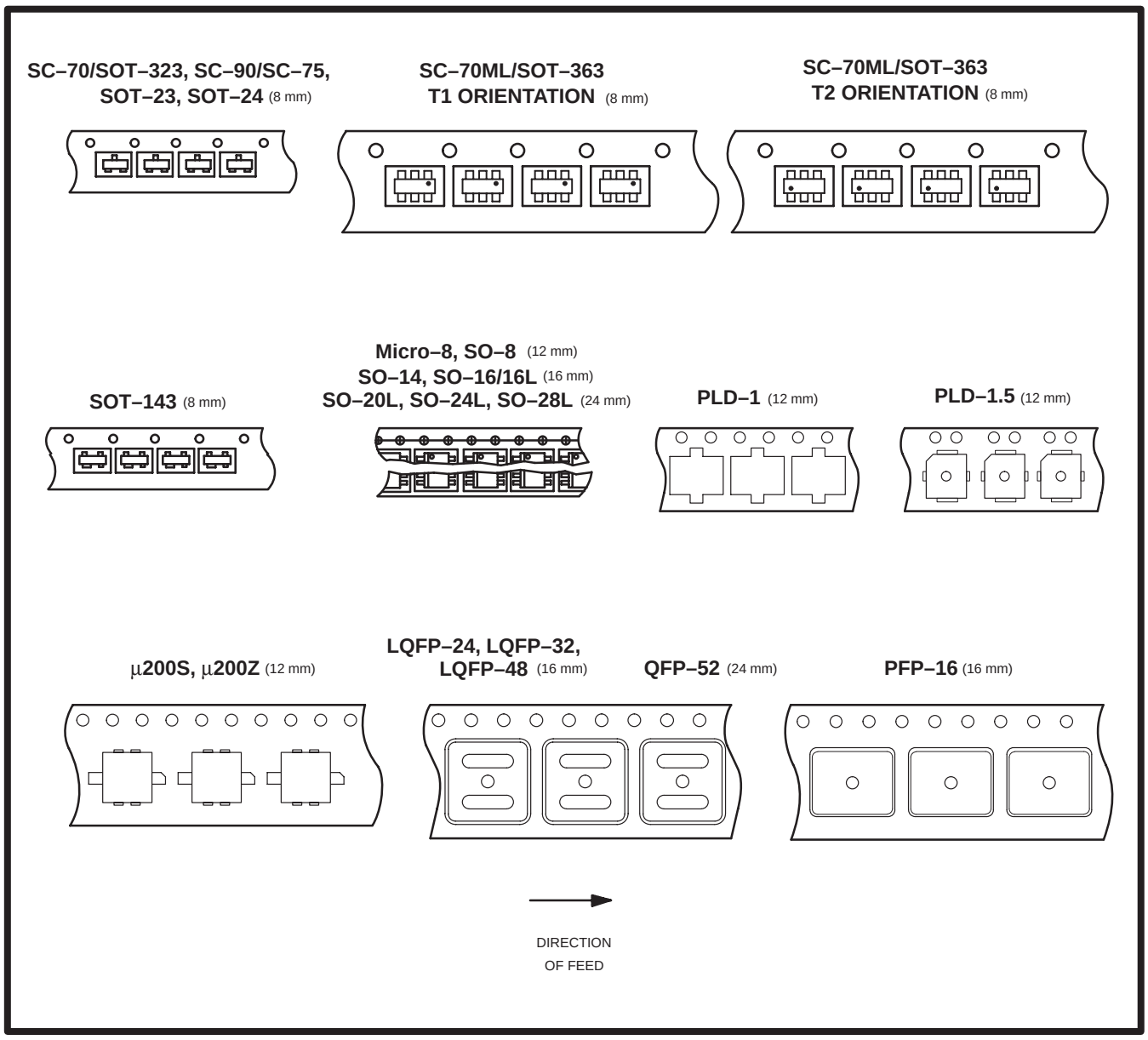
	Page
Tape and Reel Specifications	8.1–2
Embossed Tape and Reel Ordering Information	8.1–4
Embossed Tape and Reel Data for Discretes	8.1–5

RF and IF Tape and Reel Specifications

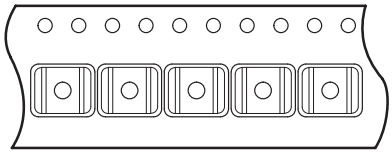
Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the “peel–back” cover tape.

- Two Reel Sizes Available (7″ and 13″)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, –1, –2
- SC–70/SOT–323, SC–70ML/SOT–363, SC–90/SC–75, SOT–23, SOT–24, SOT–143 in 8 mm Tape
- Micro–8, PLD–1, PLD–1.5, SO–8, µ200S, µ200Z in 12 mm Tape
- SO–14, SO–16/16L, LQFP24, LQFP–32, LQFP–48, TSSOP–16/16EP, TSSOP–20/20HS in 16 mm Tape
- QFP–52, SO–20L, SO–24L, SO–28L, µ250S in 24 mm Tape
- NI–600, µ400, µ400S in 32 mm Tape
- 465, 465A in 56 mm Tape

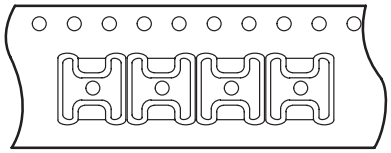
Use the standard device title and add the required suffix as listed in the option table on the following page. Note that the individual reels have a finite number of devices depending on the type of product contained in the tape. Also note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.



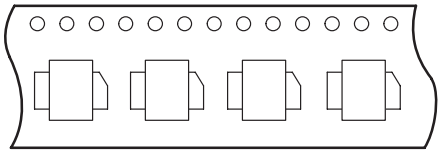
TSSOP–16/16EP (16 mm)



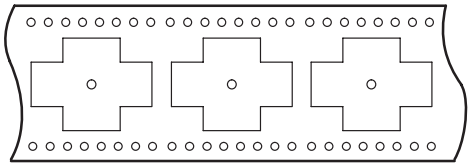
TSSOP–20/20HS (16 mm)



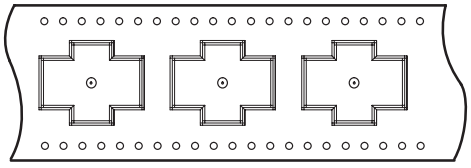
μ250S (24 mm)



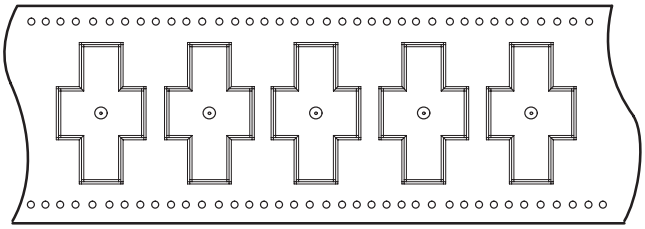
NI–600 (32 mm)



μ400, μ400S (32 mm)



465, 465A (56 mm)





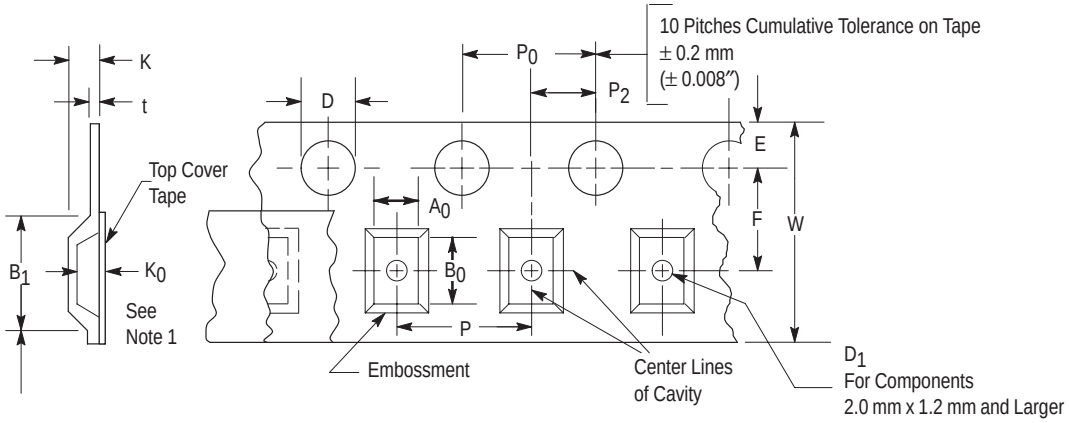
DIRECTION
OF FEED

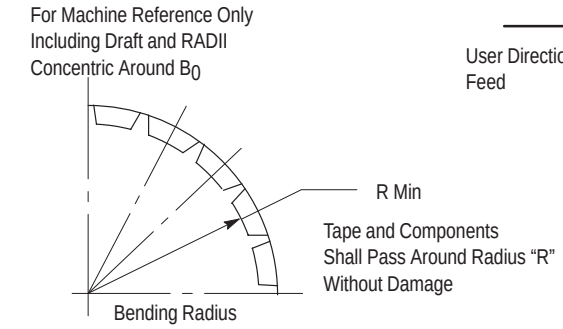
RF and IF EMBOSSED TAPE AND REEL ORDERING INFORMATION

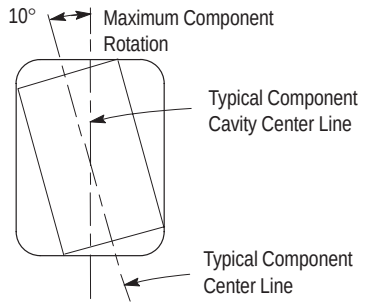
Package	Tape Width (mm)	Pitch mm (inch)	Reel Size mm (inch)	Devices Per Reel and Minimum Order Quantity	Device Suffix
SC–70/SOT–323	8 8	4.0 ± 0.1 (.157 ± .004)	178 (7) 330 (13)	3,000 10,000	T1 T3
SC–70ML/SOT–363	8	4.0 ± 0.1 (.157 ± .004)	178 (7)	3,000 3,000	T1 T2
SC–90/SC–75	8	4.0 ± 0.1 (.157 ± .004)	178 (7)	3,000	T1
Micro–8	12	8.0 ± 0.1 (.315 ± .003)	330 (13)	2,500	R2
PLD–1	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	1,000	T1
PLD–1.5	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	1,000	T1
PFP–16	16	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,500	R2
LQFP–24	16	12.0 ± 0.1 (.472 ± .004)	330 (13)	2,000	R2
LQFP–32	16	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,800	R2
LQFP–48	16	12.0 ± 0.1 (.472 ± .004)	330 (13)	2,000	R2
QFP–52	24	24.0 ± 0.1 (.945 ± .004)	330 (13)	1,500	R2
SO–8	12	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
SO–14	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
SO–16/16L	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
SO–20L	24	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,000	R2
SO–24L	24	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,000	R2
SO–28L	24	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,000	R2
SOT–23, SOT–24	8 8	4.0 ± 0.1 (.157 ± .004)	178 (7) 330 (13)	3,000 10,000	T1 T3
SOT–143	8 8	4.0 ± 0.1 (.157 ± .004)	178 (7) 330 (13)	3,000 10,000	T1 T3
TSSOP–16/16EP	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
TSSOP–20/20HS	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
µ200S (458)	12	12.0 ± 0.1 (.471 ± .004)	178 (7)	500	R1
µ200Z (458A)	12	12.0 ± 0.1 (.471 ± .004)	178 (7)	500	R1
µ250S (360C)	24	16.0 ± 0.1 (.631 ± .004)	330 (13)	500	R1
NI–600 (465D)	32	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
465, 465A	56	28.0 ± 0.1 (1.102 ± .004)	330 (13)	250	R3
µ400, µ400S	32	28.0 ± 0.1 (1.102 ± .004)	330 (13)	450	R2

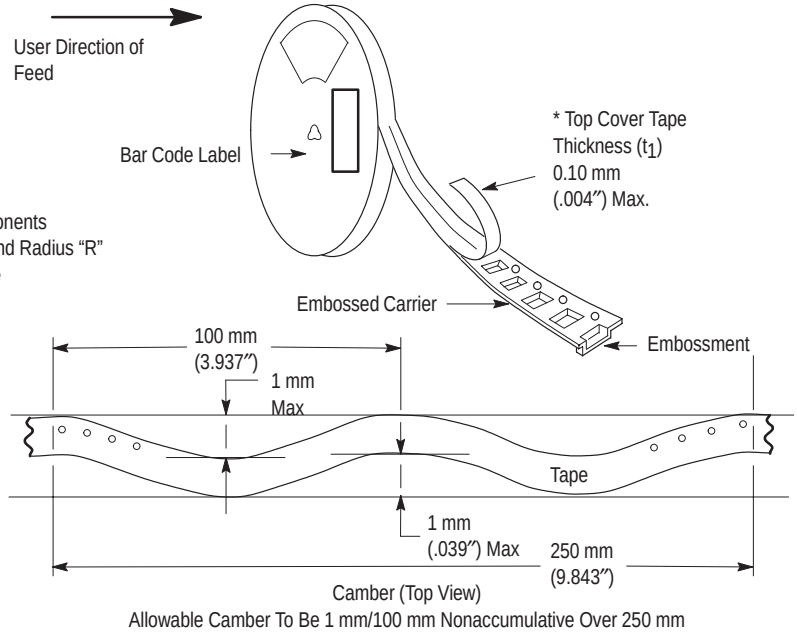
EMBOSSED TAPE AND REEL DATA FOR DISCRETES

CARRIER TAPE SPECIFICATIONS









DIMENSIONS

Tape Size	B_1 Max	D	D_1	E_1	F	K	P_0	P_2	R Min	T Max	W Max
8 mm	4.55 mm (.179″)	1.5 + 0.1 mm – 0.0 (.059 + .004″ – 0.0)	1.0 Min (.039″)	1.75 ± 0.1 mm (.069 ± .004″)	3.5 ± 0.05 mm (.138 ± .002″)	2.4 mm Max (.094″)	4.0 ± 0.1 mm (.157 ± .004″)	2.0 ± 0.1 mm (.079 ± .002″)	25 mm (.98″)	0.6 mm (.024″)	8.3 mm (.327″)
12 mm	8.2 mm (.323″)		1.5 mm Min (.060″)		5.5 ± 0.05 mm (.217 ± .002″)	6.4 mm Max (.252″)			30 mm (1.18″)		12 ± .30 mm (.470 ± .012″)
16 mm	12.1 mm (.476″)				7.5 ± 0.10 mm (.295 ± .004″)	7.9 mm Max (.311″)					16.3 mm (.642″)
24 mm	20.1 mm (.791″)				11.5 ± 0.1 mm (.453 ± .004″)	11.9 mm Max (.468″)					24.3 mm (.957″)
32 mm	23.0 mm (.906″)		1.5 mm Min (.059″)		14.2 ± 0.1 mm (.559 ± .004″)	—		2.0 ± 0.1 mm (.079 ± .004″)	50 mm (1.969″)		32.2 mm (1.272″)
56 mm	46.0 mm (1.811″)				26.2 ± 0.15 mm (1.031 ± .006″)	—		2.0 ± 0.15 mm (.079 ± .006″)	100 mm (3.397″)		56.3 mm (2.217″)

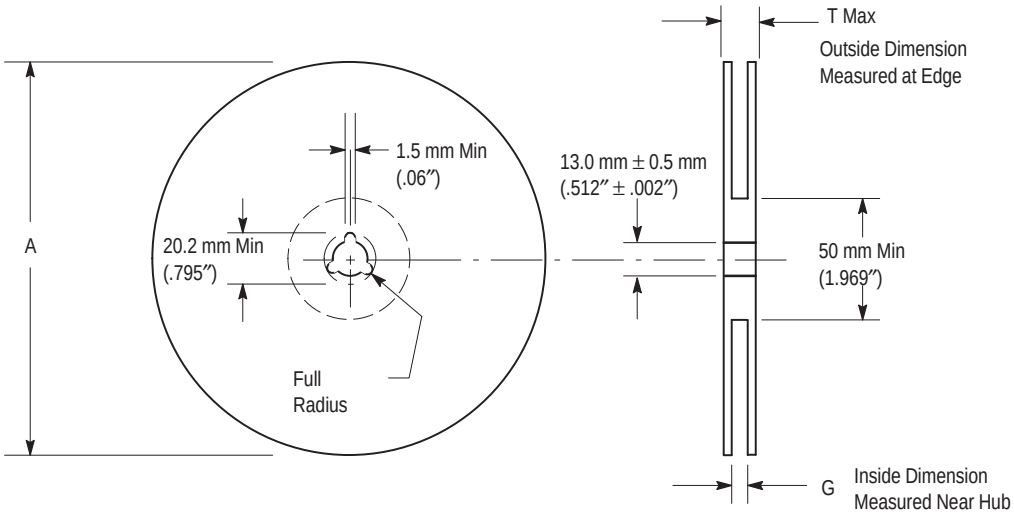
Metric dimensions govern — English are in parentheses for reference only.

NOTE 1: A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within .05 mm min. to .50 mm max., the component cannot rotate more than 10° within the determined cavity.

NOTE 2: If B_1 exceeds 4.2 mm (.165) for 8 mm embossed tape, the tape may not feed through all tape feeders.

NOTE 3: Pitch information is contained in the Embossed Tape and Reel Ordering Information on pg. 8.1–4.

EMBOSSED TAPE AND REEL DATA FOR DISCRETES



Size	A Max	G	T Max
8 mm	330 mm (12.992″)	8.4 mm + 1.5 mm, –0.0 (.33″ + .059″, –0.00)	14.4 mm (.56″)
12 mm	330 mm (12.992″)	12.4 mm + 2.0 mm, –0.0 (.49″ + .079″, –0.00)	18.4 mm (.72″)
16 mm	360 mm (14.173″)	16.4 mm + 2.0 mm, –0.0 (.646″ + .078″, –0.00)	22.4 mm (.882″)
24 mm	360 mm (14.173″)	24.4 mm + 2.0 mm, –0.0 (.961″ + .070″, –0.00)	30.4 mm (1.197″)
32 mm	360 mm (14.163″)	32.4 mm + 2.0 mm, –0.0 (1.276″+ 0.79″, –0.00)	0.6 mm (.024″)
56 mm	609 mm (23.976″)	56.4 mm + 2.0 mm, –0.0 (2.220” + 0.78″, –0.00)	0.6 mm (.024″)

Reel Dimensions

Metric Dimensions Govern — English are in parentheses for reference only

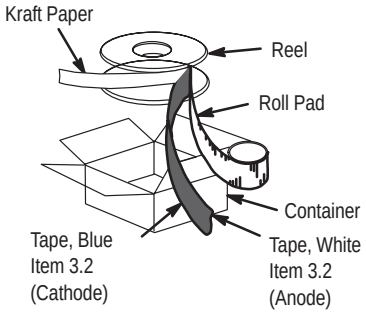


Figure 1. Reel Packing

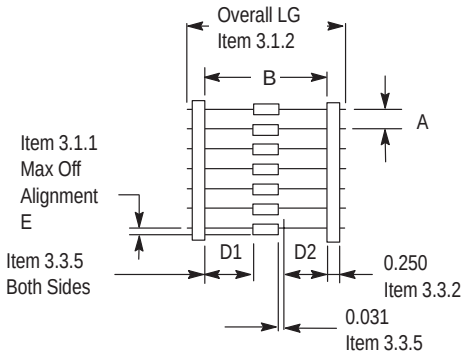


Figure 2. Component Spacing

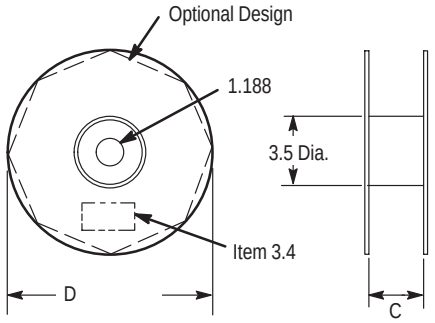


Figure 3. Reel Dimensions

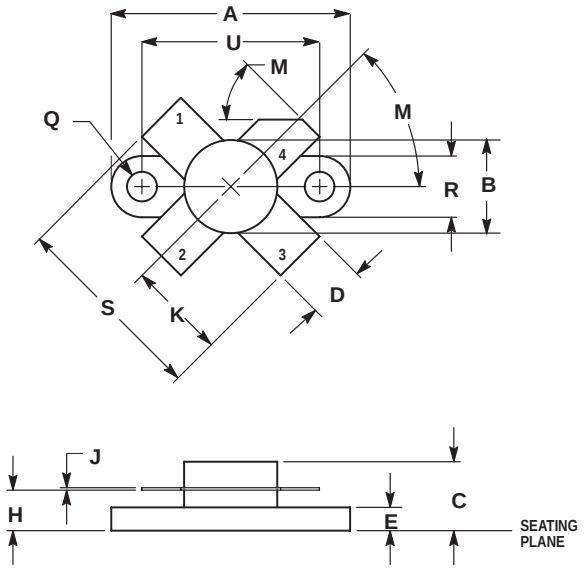
Chapter Nine
Packaging Information

The packaging availability for each device type is indicated on the individual data sheets and in the Selector Guide. All of the outline dimensions for the packages are given in this section.

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Case Dimensions

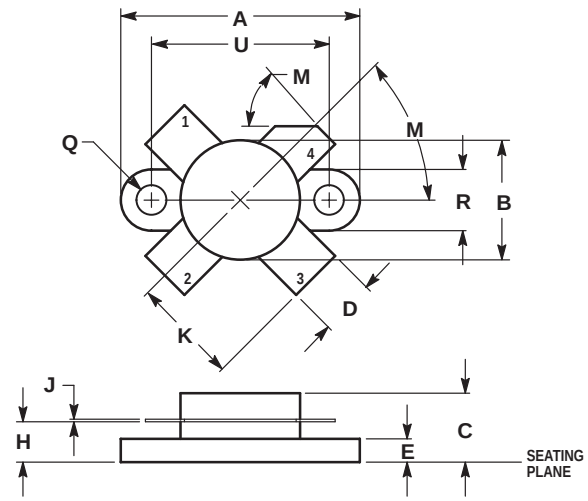


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.960	0.990	24.39	25.14
B	0.370	0.390	9.40	9.90
C	0.229	0.281	5.82	7.13
D	0.215	0.235	5.47	5.96
E	0.085	0.105	2.16	2.66
H	0.150	0.108	3.81	4.57
J	0.004	0.006	0.11	0.15
K	0.395	0.405	10.04	10.28
M	40°	50°	40°	50°
Q	0.113	0.130	2.88	3.30
R	0.245	0.255	6.23	6.47
S	0.790	0.810	20.07	20.57
U	0.720	0.730	18.29	18.54

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

CASE 211–07
ISSUE N
(.380″ FLANGE)

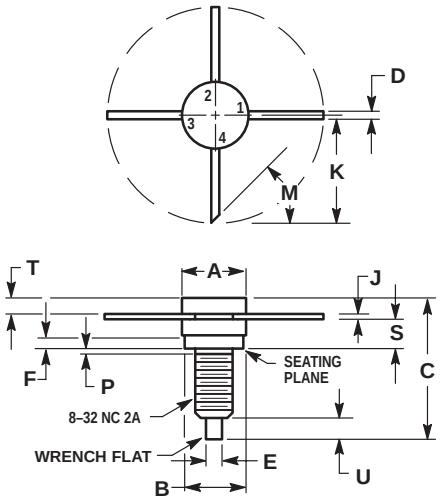


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.960	0.990	24.39	25.14
B	0.465	0.510	11.82	12.95
C	0.229	0.275	5.82	6.98
D	0.216	0.235	5.49	5.96
E	0.084	0.110	2.14	2.79
H	0.144	0.178	3.66	4.52
J	0.003	0.007	0.08	0.17
K	0.435	—	11.05	—
M	45°NOM		45°NOM	
Q	0.115	0.130	2.93	3.30
R	0.246	0.255	6.25	6.47
U	0.720	0.730	18.29	18.54

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

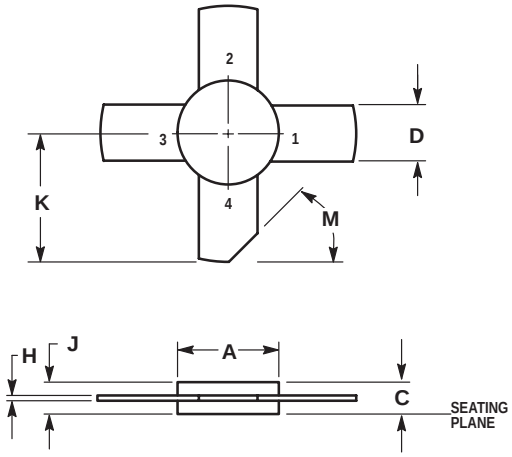
CASE 211–11
ISSUE N
(.500″ FLANGE)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	15.24	16.51	0.600	0.650
D	0.66	0.86	0.026	0.034
E	1.40	1.65	0.055	0.065
F	1.52	—	0.060	—
J	0.10	0.15	0.004	0.006
K	11.17	—	0.440	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
S	2.74	3.35	0.108	0.132
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

CASE 244A–01
ISSUE A

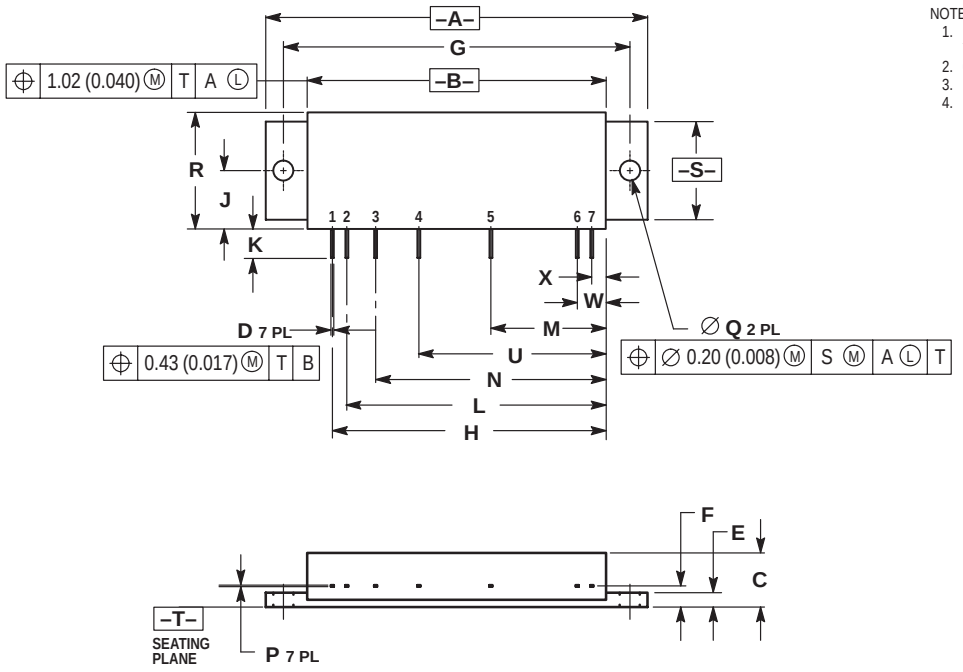


NOTES:
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. SEATING PLANE = GROUND AND IS CONNECTED TO PIN 1 AND 3.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.271	0.286	6.88	7.26
C	0.112	0.136	2.84	3.45
D	0.215	0.235	5.46	5.97
H	0.055	0.065	1.40	1.65
J	0.003	0.007	0.08	0.18
K	0.435	—	11.05	—
M	45° REF		45° REF	

STYLE 3:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

CASE 249–06
ISSUE H
(.280″ PILL)

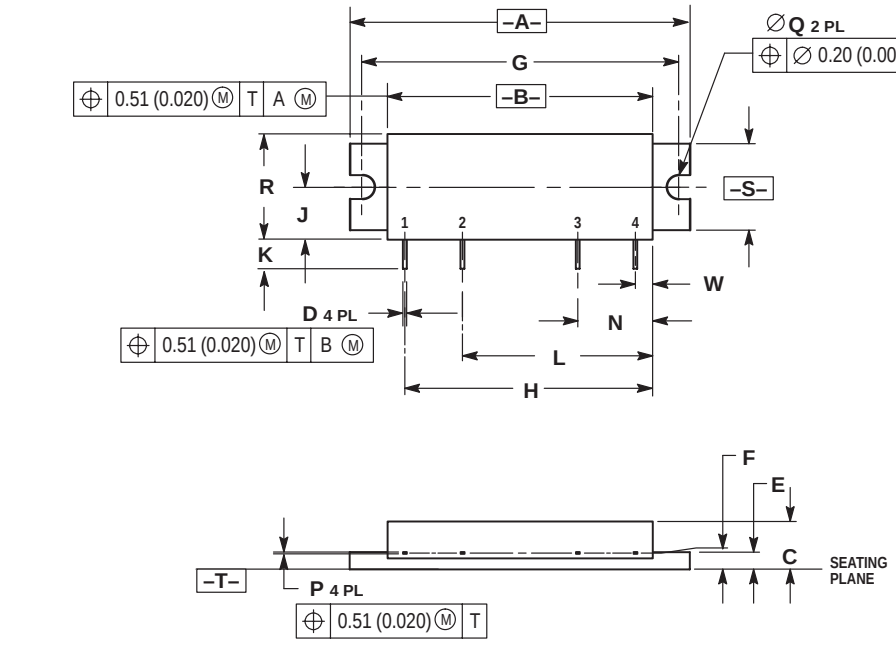


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.
4. REF INDICATES NON–CONTROLLED DIMENSION FOR REFERENCE USE ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	2.638	2.662	67.01	67.61
B	2.075 REF		52.71 REF	
C	—	0.375	—	9.53
D	0.017	0.023	0.43	0.58
E	0.098	0.114	2.49	2.90
F	0.134	0.156	3.40	3.96
G	2.405 BSC REF		61.09 BSC REF	
H	1.900 BSC		48.26 BSC	
J	0.390	0.430	9.91	10.92
K	0.175	0.217	4.45	5.51
L	1.800 BSC		45.72 BSC	
M	0.800 BSC		20.32 BSC	
N	1.600 BSC		40.64 BSC	
P	0.010 REF		0.25 REF	
Q	0.133	0.147	3.38	3.73
R	0.800	0.820	20.32	20.83
S	0.668	0.692	16.97	17.58
U	1.300 BSC		33.02 BSC	
W	0.200 BSC		5.08 BSC	
X	0.100 BSC		2.54 BSC	

STYLE 1:
PIN 1. RF INPUT
2. DC TERMINAL, Vs1
3. DC TERMINAL, Vs2
4. DC TERMINAL, Vb
5. DC TERMINAL, Vs3
6. DC TERMINAL, Vs4
7. RF OUTPUT

CASE 301AK–01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.

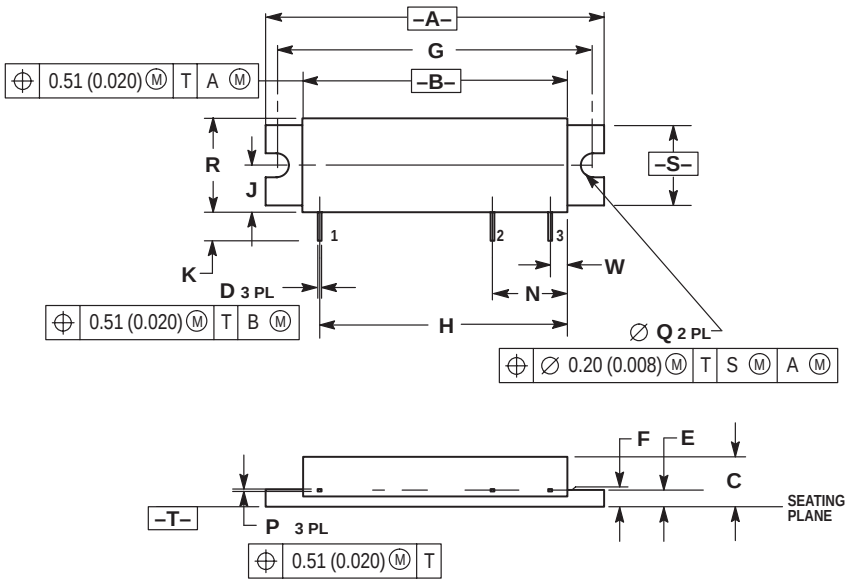
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.760	1.780	44.70	45.21
B	1.370	1.390	34.80	35.31
C	0.245	0.265	6.22	6.73
D	0.017	0.023	0.43	0.58
E	0.080	0.100	2.03	2.54
F	0.086 BSC		2.18 BSC	
G	1.650 BSC		41.91 BSC	
H	1.290 BSC		32.77 BSC	
J	0.266	0.280	6.76	7.11
K	0.125	0.165	3.18	4.19
L	0.990 BSC		25.15 BSC	
N	0.390 BSC		9.91 BSC	
P	0.008	0.013	0.20	0.33
Q	0.118	0.132	3.00	3.35
R	0.535	0.555	13.59	14.10
S	0.445	0.465	11.30	11.81
W	0.090 BSC		2.29 BSC	

STYLE 1:
PIN 1. RF INPUT
2. VDD1
3. VDD2
4. RF OUTPUT
CASE: GROUND

STYLE 2:
PIN 1. RF OUTPUT
2. VDD2
3. VDD1
4. RF INPUT
CASE: GROUND

CASE 301AP–01
ISSUE B

CASE DIMENSIONS (continued)



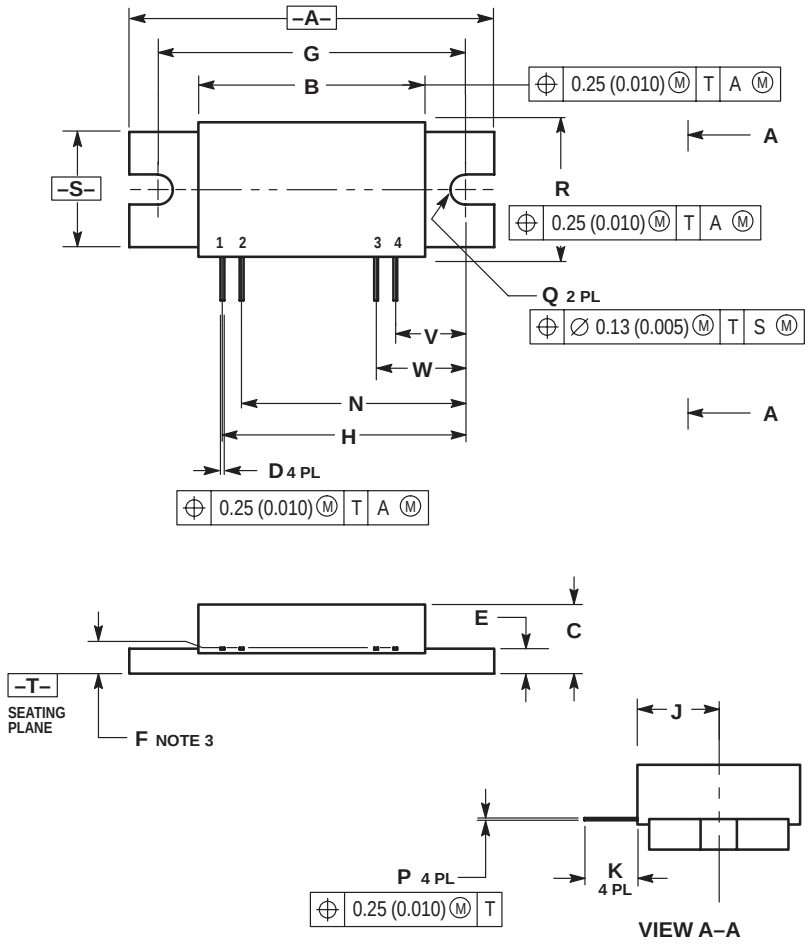
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.760	1.780	44.70	45.21
B	1.370	1.390	34.80	35.31
C	0.245	0.265	6.22	6.73
D	0.017	0.023	0.43	0.58
E	0.080	0.100	2.03	2.54
F	0.086 BSC		2.18 BSC	
G	1.650 BSC		41.91 BSC	
H	1.290 BSC		32.77 BSC	
J	0.266	0.280	6.76	7.11
K	0.125	0.165	3.18	4.19
N	0.390 BSC		9.91 BSC	
P	0.008	0.013	0.20	0.33
Q	0.118	0.132	3.00	3.35
R	0.535	0.555	13.59	14.10
S	0.445	0.465	11.30	11.81
W	0.090 BSC		2.29 BSC	

STYLE 1:
PIN 1. RF INPUT
2. VDD
3. RF OUTPUT
CASE: GROUND

CASE 301AS–01
ISSUE A

CASE DIMENSIONS (continued)

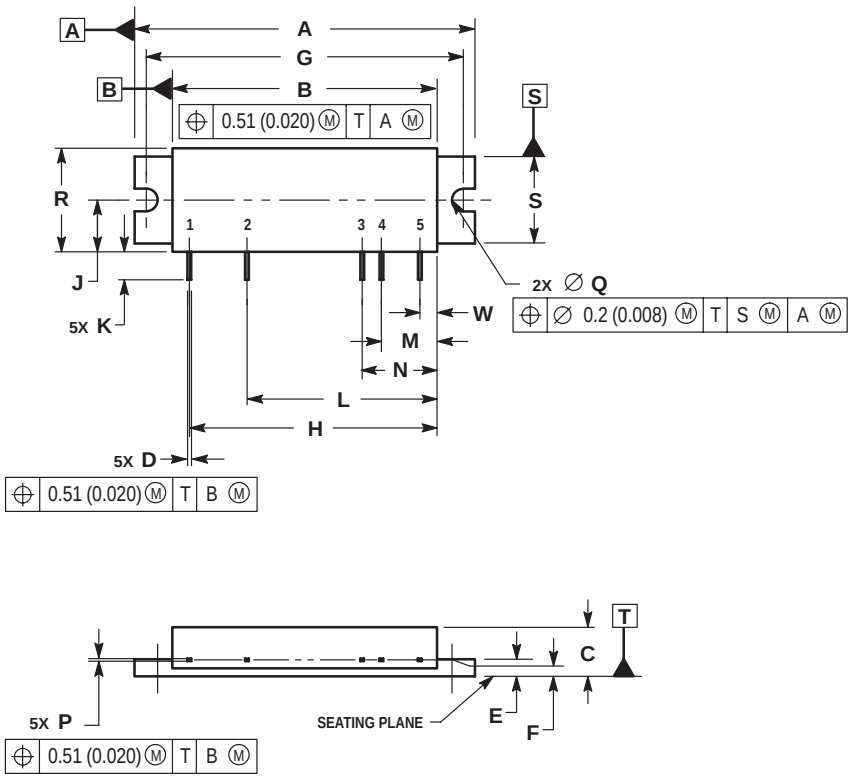


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F IS FROM THE BOTTOM OF HEATSINK TO THE TOP OF THE LEAD.
4. DIMENSION P TO BE MEASURED AS LEAD EXITS COVER.
5. FLANGE FLATNESS 0.038 (0.0015) MAXIMUM CONVEX, 0.063 (0.0025) MAXIMUM CONCAVE.
6. ADHESIVE MATERIAL SHALL BE INCLUDED IN THE DIMENSIONS LISTED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.890	1.910	48.01	48.51
B	1.170	1.190	29.72	30.22
C	0.350	0.376	8.89	9.55
D	0.018	0.022	0.46	0.55
E	0.115	0.135	2.92	3.42
F	0.170 BSC		4.31 BSC	
G	1.600 BSC		40.64 BSC	
H	1.265 BSC		32.13 BSC	
J	0.325	0.375	8.25	9.52
K	0.225	—	5.72	—
N	1.165 BSC		29.59 BSC	
P	0.010 REF		0.25 REF	
Q	0.150	0.160	3.81	4.06
R	0.685	0.705	17.40	17.90
S	0.598	0.612	15.18	15.54
V	0.365 BSC		9.27 BSC	
W	0.465 BSC		11.81 BSC	

STYLE 1:
PIN 1. RF IN
2. V BIAS
3. V SUPPLY
4. RF OUT

CASE 301AW–02
ISSUE B

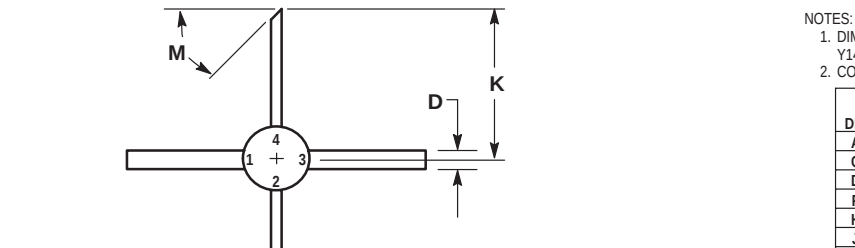


NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
3. DIMENSION F TO CENTER LINE OF LEADS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	44.7	45.21	1.760	1.780
B	34.8	35.31	1.370	1.390
C	6.22	6.73	0.245	0.265
D	0.43	0.58	0.017	0.023
E	2.03	2.54	0.080	0.100
F	2.18 BSC		0.086 BSC	
G	41.91 BSC		1.650 BSC	
H	32.77 BSC		1.290 BSC	
J	6.76	7.11	0.266	0.280
K	3.18	4.19	0.125	0.165
L	25.15 BSC		0.990 BSC	
M	7.37 BSC		0.290 BSC	
N	9.91 BSC		0.390 BSC	
P	0.2	0.33	0.008	0.013
Q	3	3.35	0.118	0.132
R	13.59	14.1	0.535	0.555
S	11.3	11.81	0.445	0.465
W	2.29 BSC		0.090 BSC	

STYLE 1:
PIN 5. RF INPUT
6. VDD1
7. VDD2
8. VDD3
9. RF OUTPUT
CASE: GROUND

CASE 301AY–01
ISSUE O

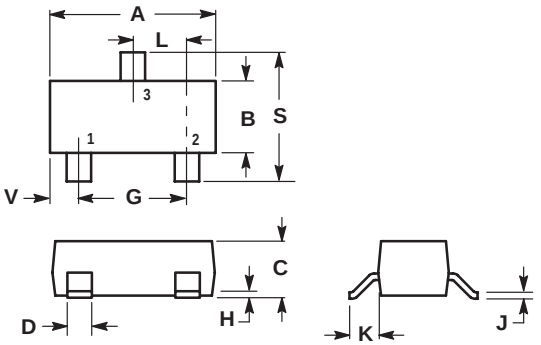


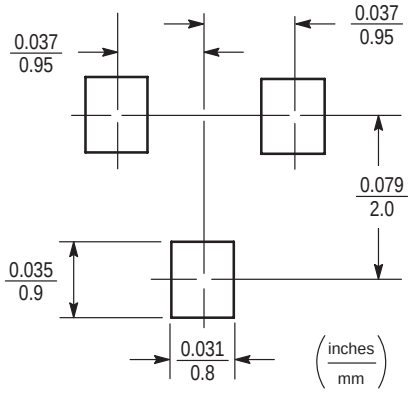
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.200	0.220	5.08	5.59
C	0.095	0.130	2.41	3.30
D	0.055	0.065	1.40	1.65
F	0.025	0.035	0.64	0.89
H	0.040	0.050	1.02	1.27
J	0.003	0.007	0.08	0.18
K	0.435	—	11.05	—
M	45 °REF		45 °REF	

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

CASE 305A–01
ISSUE A
(.204” PILL)





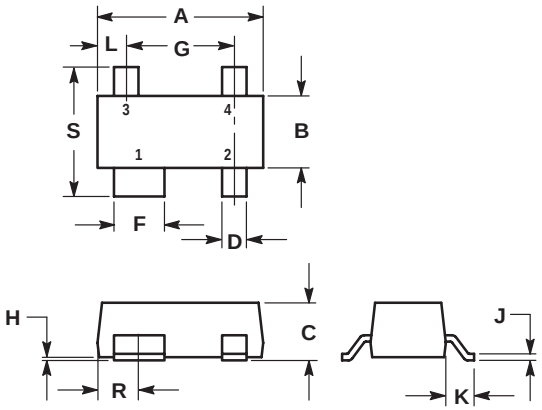
SOT–23
FOOTPRINT

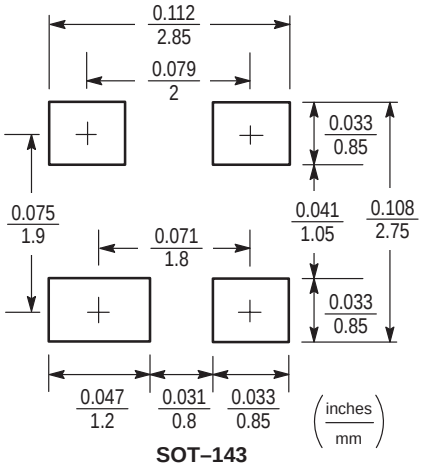
STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

CASE 318–08
ISSUE AF
(TO–236AB)





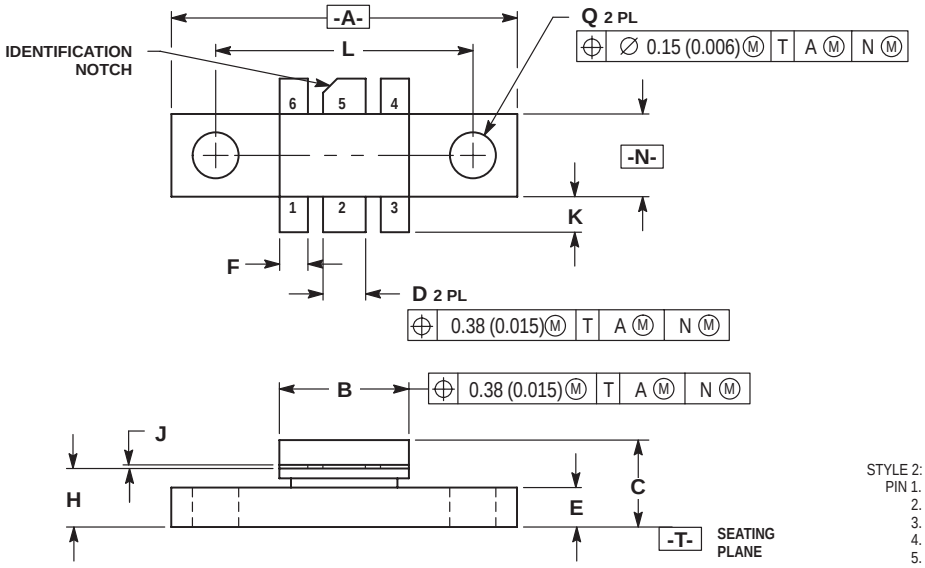
SOT–143
FOOTPRINT

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. EMITTER
4. BASE

NOTES:
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.80	3.04	0.110	0.120
B	1.20	1.39	0.047	0.055
C	0.84	1.14	0.033	0.045
D	0.39	0.50	0.015	0.020
F	0.79	0.93	0.031	0.037
G	1.78	2.03	0.070	0.080
H	0.013	0.10	0.0005	0.004
J	0.08	0.15	0.003	0.006
K	0.46	0.60	0.018	0.024
L	0.445	0.60	0.0175	0.024
R	0.72	0.83	0.028	0.033
S	2.11	2.48	0.083	0.098

CASE 318A–05
ISSUE R



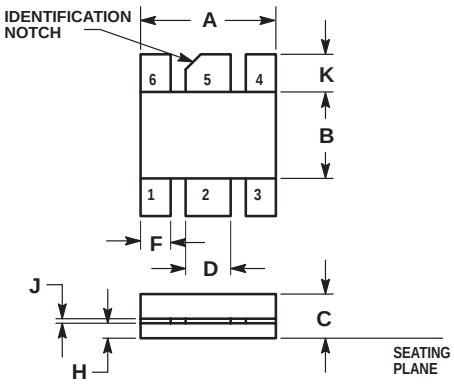
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETER	
DIM	MIN	MAX	MIN	MAX
A	0.965	0.985	24.52	25.01
B	0.355	0.375	9.02	9.52
C	0.230	0.260	5.85	6.60
D	0.115	0.125	2.93	3.17
E	0.102	0.114	2.59	2.90
F	0.075	0.085	1.91	2.15
H	0.160	0.170	4.07	4.31
J	0.004	0.006	0.11	0.15
K	0.090	0.110	2.29	2.79
L	0.725 BSC		18.42 BSC	
N	0.225	0.241	5.72	6.12
Q	0.125	0.135	3.18	3.42

STYLE 2:
PIN 1. EMITTER (COMMON)
2. BASE (INPUT)
3. EMITTER (COMMON)
4. EMITTER (COMMON)
5. COLLECTOR (OUTPUT)
6. EMITTER (COMMON)

STYLE 3:
PIN 1. SOURCE (COMMON)
2. GATE (INPUT)
3. SOURCE (COMMON)
4. SOURCE (COMMON)
5. DRAIN (OUTPUT)
6. SOURCE (COMMON)

CASE 319–07
ISSUE M
(CS–12)

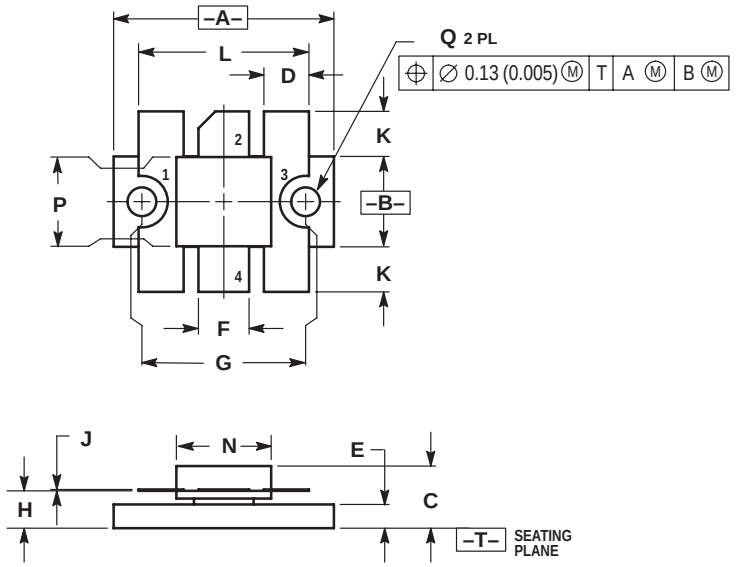


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.355	0.365	9.02	9.27
B	0.225	0.235	5.72	5.96
C	0.110	0.125	2.80	3.17
D	0.115	0.125	2.93	3.17
F	0.075	0.085	1.91	2.15
H	0.035	0.045	0.89	1.14
J	0.004	0.006	0.11	0.15
K	0.090	0.110	2.29	2.79

STYLE 2:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. EMITTER
5. COLLECTOR
6. EMITTER

CASE 319A–02
ISSUE B

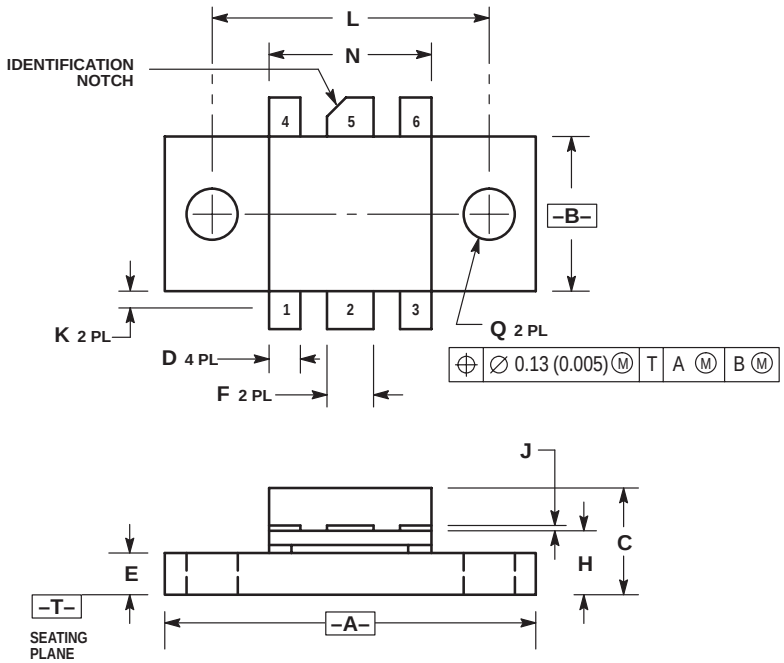


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.965	0.985	24.51	25.02
B	0.390	0.410	9.91	10.41
C	0.250	0.290	6.73	7.36
D	0.190	0.210	4.83	5.33
E	0.095	0.115	2.42	2.92
F	0.215	0.235	5.47	5.96
G	0.725 BSC		18.42 BSC	
H	0.155	0.175	3.94	4.44
J	0.004	0.006	0.10	0.15
K	0.195	0.205	4.95	5.21
L	0.740	0.770	18.80	19.55
N	0.415	0.425	10.54	10.80
P	0.390	0.400	9.91	10.16
Q	0.120	0.135	3.05	3.42

STYLE 2:
PIN 1. SOURCE
2. DRAIN
3. SOURCE
4. GATE

CASE 333–04
ISSUE E



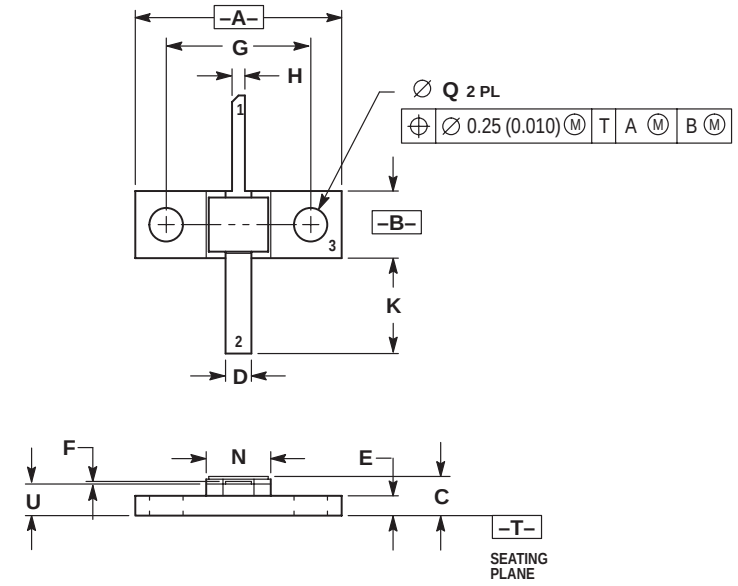
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.965	0.985	24.52	25.01
B	0.390	0.410	9.91	10.41
C	0.250	0.290	6.35	7.36
D	0.075	0.090	1.91	2.28
E	0.095	0.115	2.42	2.92
F	0.110	0.130	2.80	3.30
H	0.155	0.175	3.94	4.44
J	0.004	0.006	0.11	0.15
K	0.090	0.116	2.29	2.94
L	0.725 BSC		18.41 BSC	
N	0.415	0.435	10.55	11.04
Q	0.120	0.135	3.05	3.42

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. BASE
5. COLLECTOR
6. BASE

STYLE 2:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. EMITTER
5. COLLECTOR
6. EMITTER

CASE 333A–02
ISSUE C
(MAAC PAC)

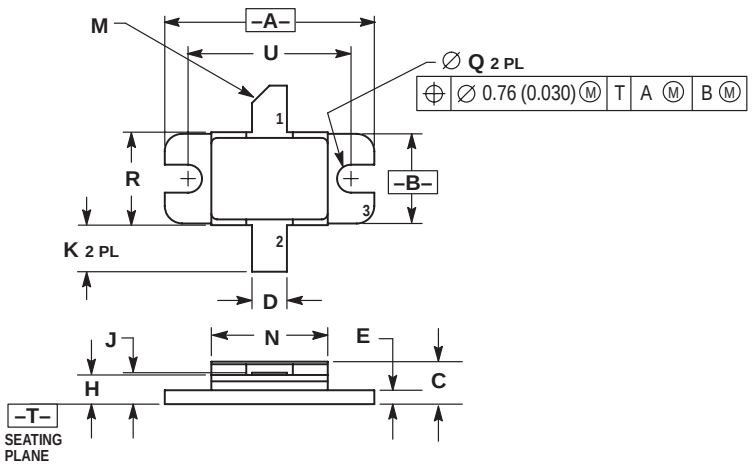


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.790	0.810	20.07	20.57
B	0.253	0.267	6.43	6.78
C	0.144	0.160	3.66	4.06
D	0.093	0.107	2.37	2.71
E	0.074	0.080	1.88	2.03
F	0.002	0.006	0.06	0.15
G	0.560 BSC		14.22 BSC	
H	0.043	0.057	1.10	1.44
K	0.346	0.394	8.79	10.10
N	0.243	0.257	6.18	6.52
Q	0.125	0.135	3.18	3.42
U	0.117	0.128	2.98	3.25

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 336E–02
ISSUE B

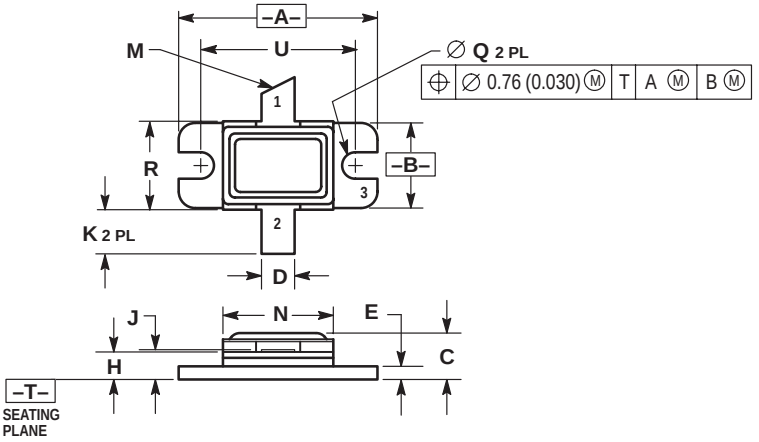


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.890	0.910	22.61	23.11
B	0.375	0.395	9.53	10.03
C	0.150	0.165	3.81	4.19
D	0.145	0.155	3.69	3.93
E	0.055	0.065	1.40	1.65
H	0.120	0.130	3.05	3.30
J	0.003	0.006	0.08	0.15
K	0.185	0.215	4.70	5.46
M	45° REF		45° REF	
N	0.490	0.510	12.45	12.95
Q	0.115	0.125	2.93	3.17
R	0.395	0.405	10.04	10.28
U	0.700 BSC		17.78 BSC	

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 355C–02
ISSUE C

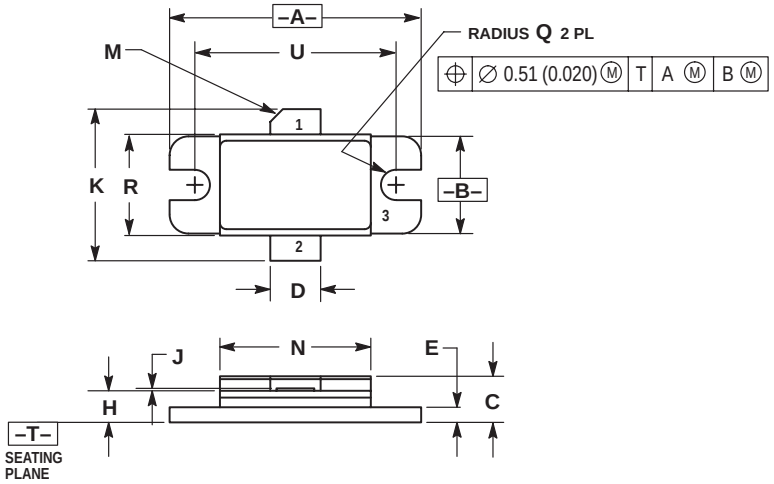


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.890	0.910	22.61	23.11
B	0.375	0.395	9.53	10.03
C	0.190	0.210	4.83	5.33
D	0.145	0.155	3.69	3.93
E	0.055	0.065	1.40	1.65
H	0.120	0.130	3.05	3.30
J	0.003	0.006	0.08	0.15
K	0.185	0.215	4.70	5.46
M	45 ° REF		45 ° REF	
N	0.490	0.510	12.45	12.95
Q	0.115	0.125	2.93	3.17
R	0.395	0.405	10.04	10.28
U	0.700 BSC		17.78 BSC	

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 355E–01
ISSUE B

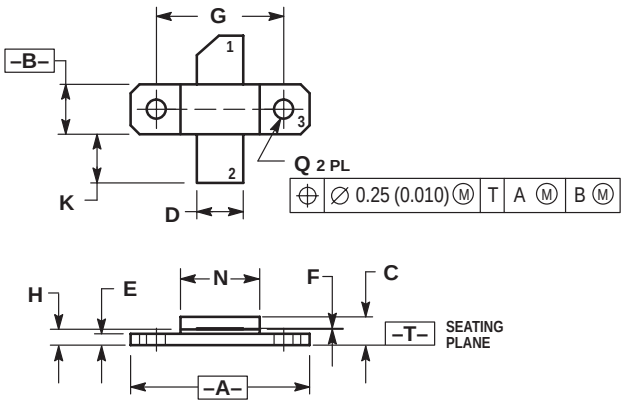


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.990	1.010	25.15	25.65
B	0.375	0.395	9.53	10.03
C	0.145	0.175	3.68	4.45
D	0.195	0.205	4.95	5.21
E	0.055	0.065	1.40	1.65
H	0.117	0.133	2.97	3.38
J	0.003	0.006	0.08	0.15
K	0.580	0.620	14.73	15.75
M	45 ° REF		45 ° REF	
N	0.590	0.610	14.99	15.49
Q	0.055	0.065	1.40	1.65
R	0.395	0.405	10.03	10.29
U	0.800 BSC		20.32 BSC	

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 355J–02
ISSUE A

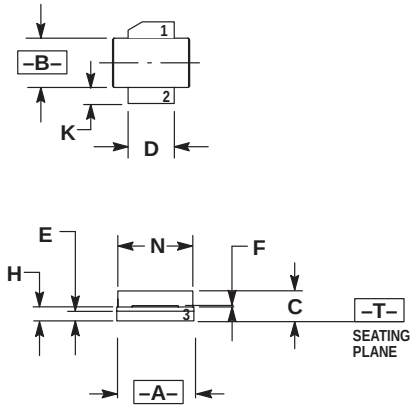


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM EDGE OF FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.790	0.810	20.07	20.57
B	0.220	0.240	5.59	6.09
C	0.125	0.175	3.18	4.45
D	0.205	0.225	5.21	5.71
E	0.050	0.070	1.27	1.77
F	0.004	0.006	0.11	0.15
G	0.562 BSC		14.27 BSC	
H	0.077	0.087	1.96	2.21
K	0.215	0.255	5.47	6.47
N	0.350	0.370	8.89	9.39
Q	0.120	0.140	3.05	3.55

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 360B–03
ISSUE D

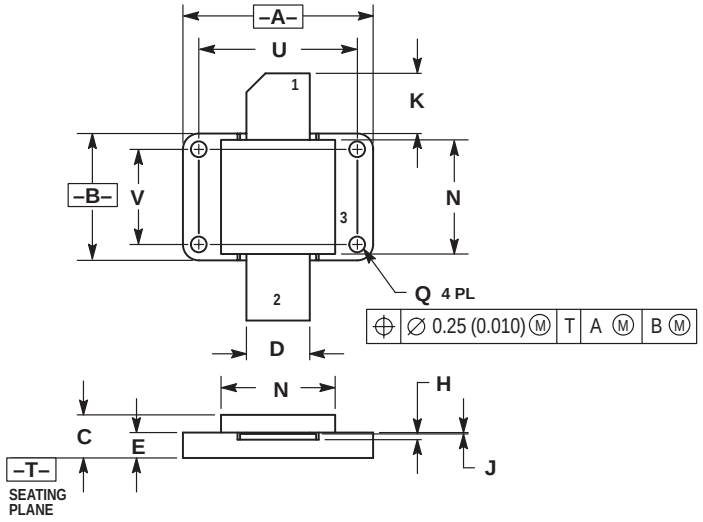


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.370	0.390	9.40	9.91
B	0.220	0.240	5.59	6.09
C	0.105	0.155	2.67	3.94
D	0.205	0.225	5.21	5.71
E	0.035	0.045	0.89	1.14
F	0.004	0.006	0.11	0.15
H	0.057	0.067	1.45	1.70
K	0.085	0.115	2.16	2.92
N	0.350	0.370	8.89	9.39

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 360C–03
ISSUE B

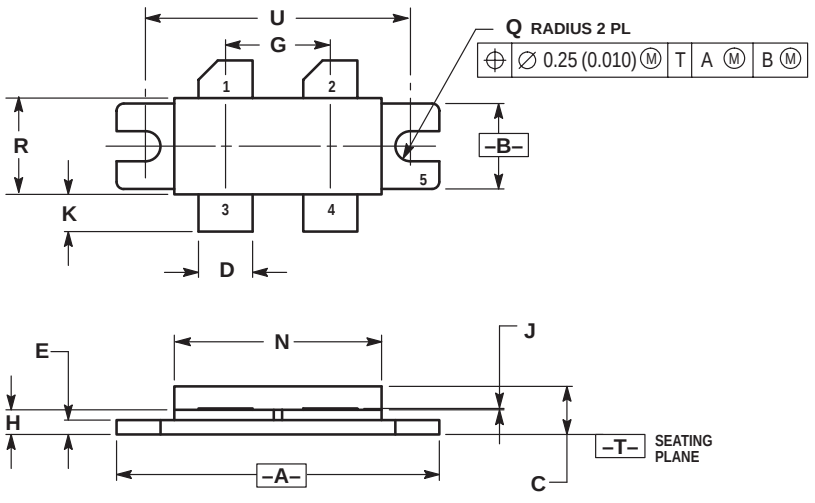


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.490	1.510	37.85	38.35
B	0.990	1.010	25.15	25.65
C	0.330	0.365	8.38	9.27
D	0.490	0.510	12.45	12.95
E	0.195	0.205	4.95	5.21
H	0.045	0.055	1.14	1.39
J	0.004	0.006	0.10	0.15
K	0.425	0.500	10.80	12.70
N	0.890	0.910	22.87	23.11
Q	0.120	0.130	3.05	3.30
U	1.250 BSC		31.75 BSC	
V	0.750 BSC		19.05 BSC	

STYLE 2:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 368–03
ISSUE C
(HOG PAC)

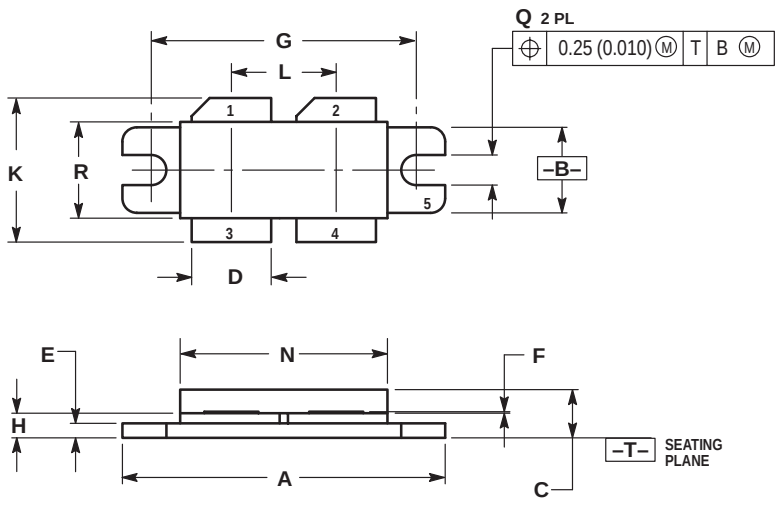


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.330	1.350	33.79	34.29
B	0.370	0.410	9.40	10.41
C	0.190	0.230	4.83	5.84
D	0.215	0.235	5.47	5.96
E	0.050	0.070	1.27	1.77
G	0.430	0.440	10.92	11.18
H	0.102	0.112	2.59	2.84
J	0.004	0.006	0.11	0.15
K	0.185	0.215	4.83	5.33
N	0.845	0.875	21.46	22.23
Q	0.060	0.070	1.52	1.78
R	0.390	0.410	9.91	10.41
U	1.100 BSC		27.94 BSC	

STYLE 2:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375–04
ISSUE D

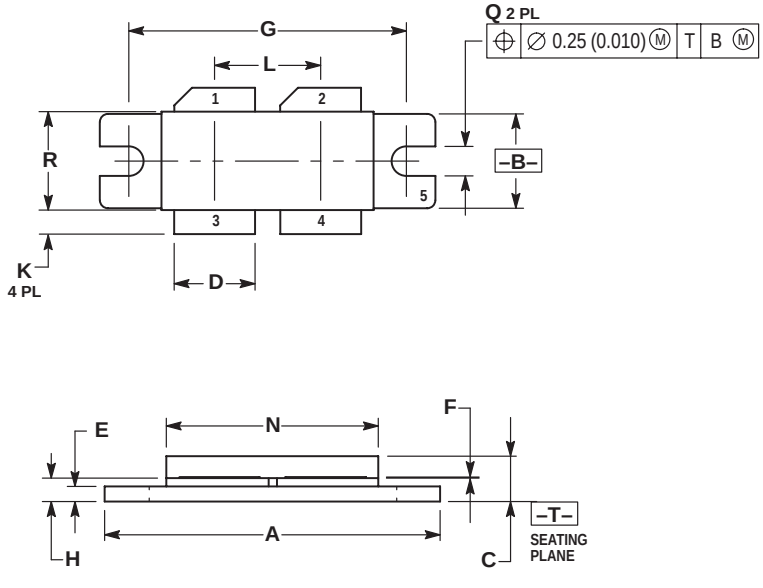


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.330	1.350	33.79	34.29
B	0.375	0.395	9.52	10.03
C	0.180	0.205	4.57	5.21
D	0.320	0.340	8.13	8.64
E	0.060	0.070	1.52	1.77
F	0.004	0.006	0.11	0.15
G	1.100 BSC		27.94 BSC	
H	0.082	0.097	2.08	2.46
K	0.580	0.620	14.73	15.75
L	0.435 BSC		11.05 BSC	
N	0.845	0.875	21.46	22.23
Q	0.118	0.130	3.00	3.30
R	0.390	0.410	9.91	10.41

STYLE 1:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. BASE
5. EMITTER

CASE 375A–01
ISSUE O

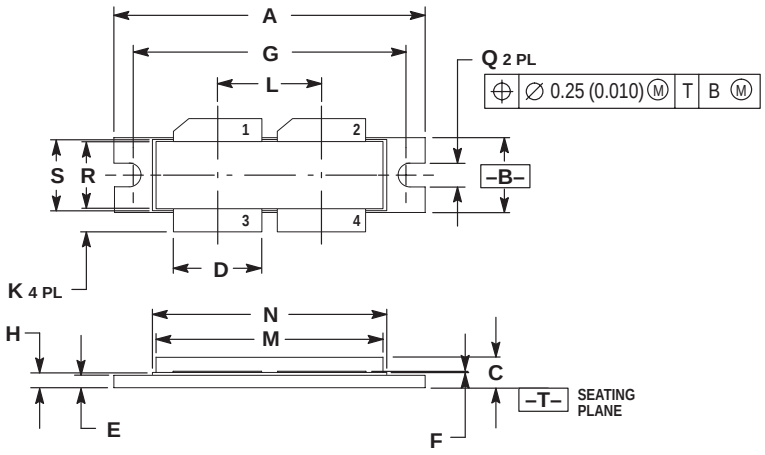


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.330	1.350	33.79	34.29
B	0.375	0.395	9.52	10.03
C	0.180	0.210	4.57	5.33
D	0.320	0.340	8.13	8.64
E	0.060	0.070	1.52	1.77
F	0.004	0.006	0.11	0.15
G	1.100 BSC		27.94 BSC	
H	0.093	0.108	2.36	2.74
K	0.085	0.115	2.16	2.92
L	0.425 BSC		10.80 BSC	
N	0.845	0.875	21.46	22.23
Q	0.118	0.130	3.00	3.30
R	0.390	0.410	9.91	10.41

STYLE 2:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375B–02
ISSUE A

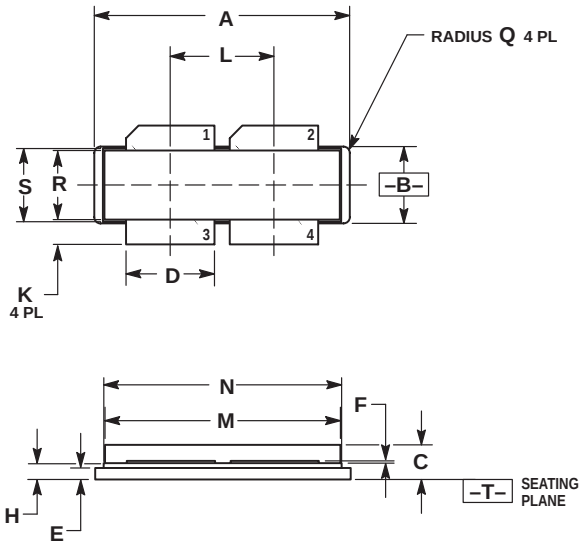


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.610	1.630	40.89	41.40
B	0.390	0.410	9.91	10.41
C	0.150	0.180	3.81	4.57
D	0.450	0.470	11.43	11.94
E	0.060	0.068	1.52	1.73
F	0.003	0.006	0.08	0.15
G	1.400 BSC		35.56 BSC	
H	0.079	0.089	2.01	2.26
K	0.117	0.137	2.97	3.48
L	0.540 BSC		13.72 BSC	
M	1.225	1.235	31.12	31.37
N	1.219	1.241	30.96	31.52
Q	0.120	0.130	3.05	3.30
R	0.350	0.370	8.89	9.40
S	0.360	0.380	9.14	9.65

STYLE 2:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375D–01
ISSUE O

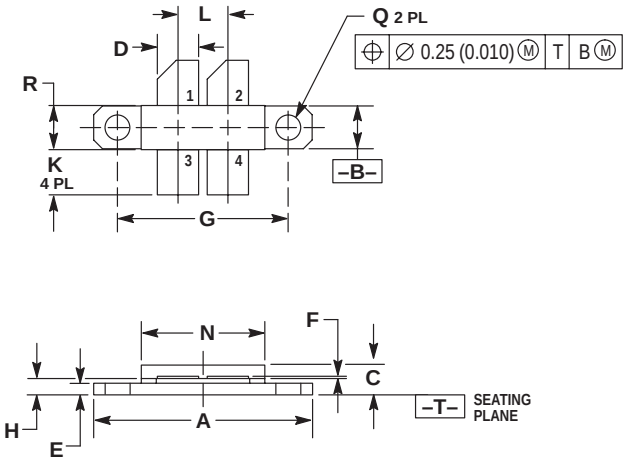


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.325	1.335	33.66	33.91
B	0.390	0.410	9.91	10.41
C	0.150	0.180	3.81	4.57
D	0.450	0.470	11.43	11.94
E	0.060	0.068	1.52	1.73
F	0.003	0.006	0.08	0.15
H	0.079	0.089	2.01	2.26
K	0.117	0.137	2.97	3.48
L	0.540 BSC		13.72 BSC	
M	1.225	1.235	31.12	31.37
N	1.219	1.241	30.96	31.52
Q	0.030 BSC		0.76 BSC	
R	0.350	0.370	8.89	9.40
S	0.360	0.380	9.14	9.65

STYLE 2:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375E–01
ISSUE O

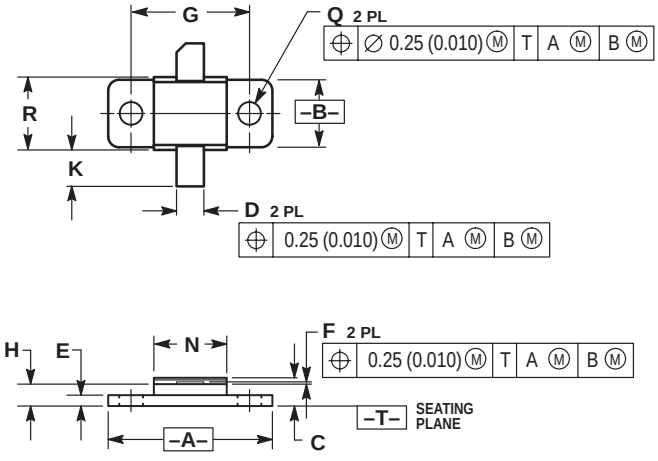


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.135	1.145	28.80	29.10
B	0.225	0.235	5.72	5.97
C	0.148	0.178	3.76	4.52
D	0.210	0.220	5.33	5.59
E	0.055	0.065	1.40	1.65
F	0.004	0.006	0.110	0.150
G	0.900 BSC		22.86 BSC	
H	0.076	0.086	1.93	2.18
K	0.215	0.255	5.46	6.28
L	0.260 BSC		6.60 BSC	
N	0.638	0.650	16.20	16.50
Q	∅ 0.130 BSC		∅ 3.30 BSC	
R	0.225	0.235	5.72	5.97

STYLE 2:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375F–02
ISSUE A

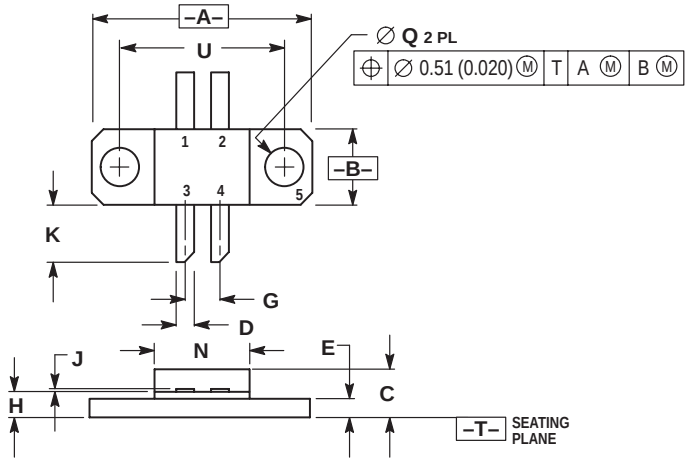


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.890	0.910	22.61	23.11
B	0.370	0.400	9.40	10.16
C	0.145	0.160	3.69	4.06
D	0.140	0.160	3.56	4.06
E	0.055	0.065	1.40	1.65
F	0.003	0.006	0.08	0.15
G	0.650 BSC		16.51 BSC	
H	0.110	0.130	2.80	3.30
K	0.180	0.220	4.57	5.59
N	0.390	0.410	9.91	10.41
Q	0.115	0.135	2.93	3.42
R	0.390	0.140	9.91	10.41

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 376B–02
ISSUE B

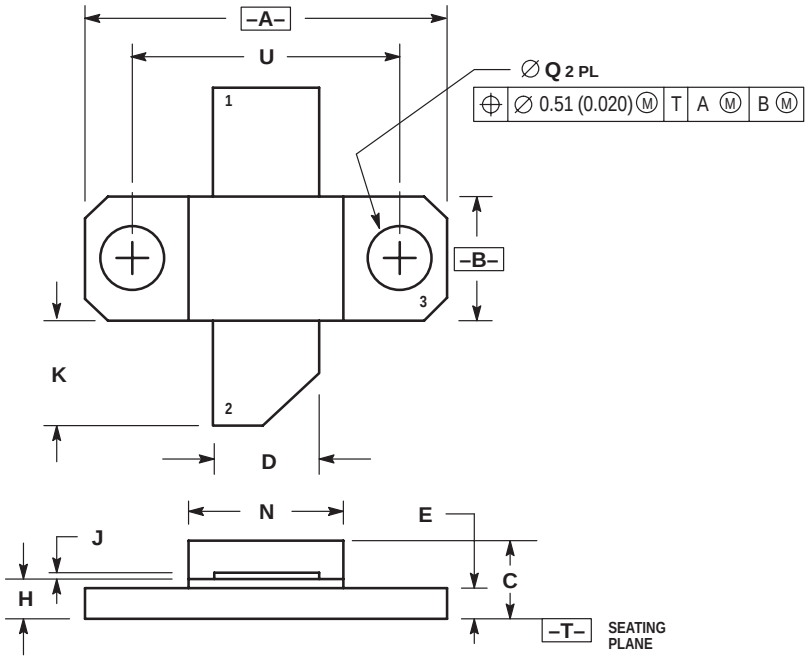


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.739	0.750	18.77	19.05
B	0.240	0.260	6.10	6.60
C	0.165	0.198	4.19	5.03
D	0.055	0.065	1.40	1.65
E	0.055	0.070	1.40	1.78
G	0.110	0.130	2.79	3.30
H	0.079	0.091	2.01	2.31
J	0.003	0.005	0.08	0.13
K	0.180	0.220	4.57	5.59
N	0.315	0.330	8.00	8.38
Q	0.125	0.135	3.18	3.42
U	0.560 BSC		14.22 BSC	

STYLE 1:
PIN 1. BASE
2. BASE
3. COLLECTOR
4. COLLECTOR
5. EMITTER

CASE 395B–01
ISSUE A



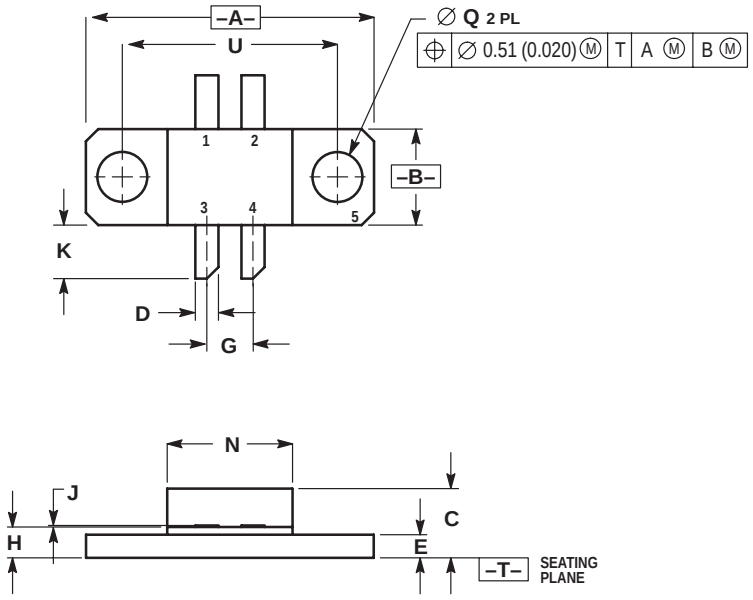
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.739	0.750	18.77	19.05
B	0.240	0.260	6.10	6.60
C	0.165	0.198	4.19	5.03
D	0.215	0.225	5.46	5.72
E	0.055	0.070	1.40	1.78
H	0.079	0.091	2.01	2.31
J	0.004	0.006	0.10	0.15
K	0.210	0.240	5.33	6.10
N	0.315	0.330	8.00	8.38
Q	0.125	0.135	3.18	3.42
U	0.560 BSC		14.23 BSC	

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

CASE 395C–01
ISSUE A

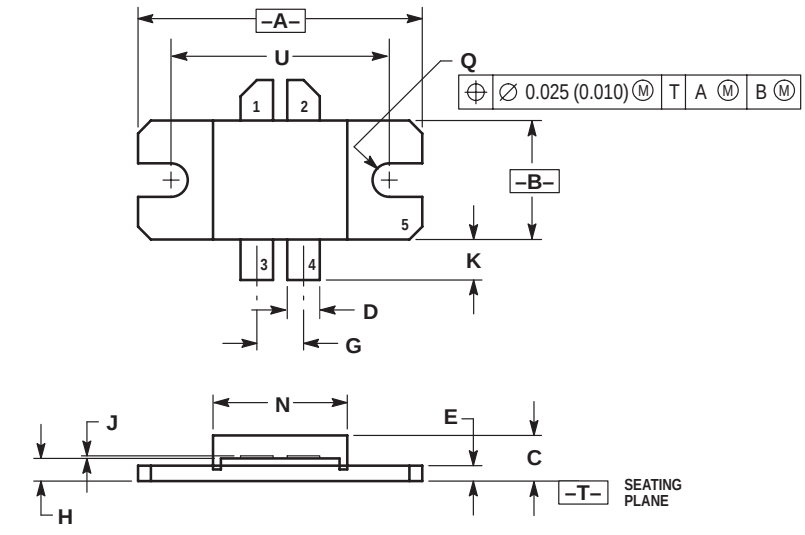


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.739	0.750	18.77	19.05
B	0.240	0.260	6.10	6.60
C	0.165	0.198	4.19	5.03
D	0.055	0.065	1.40	1.65
E	0.055	0.070	1.40	1.78
G	0.110	0.130	2.79	3.30
H	0.079	0.091	2.01	2.31
J	0.003	0.005	0.08	0.13
K	0.120	0.150	3.05	3.81
N	0.315	0.330	8.00	8.38
Q	0.125	0.135	3.18	3.42
U	0.560 BSC		14.23 BSC	

STYLE 1:
PIN 1. BASE
2. BASE
3. COLLECTOR
4. COLLECTOR
5. EMITTER

CASE 395E–01
ISSUE O

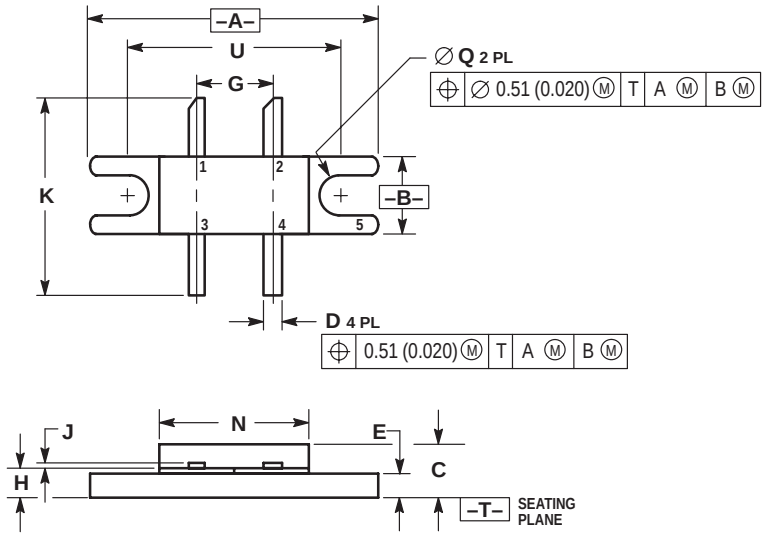


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.094	1.110	27.79	28.19
B	0.457	0.465	11.61	11.81
C	0.165	0.182	4.25	4.62
D	0.121	0.131	3.08	3.32
E	0.055	0.065	1.40	1.65
G	0.177	0.185	4.50	4.69
H	0.081	0.091	2.06	2.31
J	0.002	0.004	0.06	0.10
K	0.142	0.163	3.60	4.14
N	0.510	0.520	12.95	13.21
Q	0.125	0.135	3.18	3.42
U	0.844 BSC		21.44 BSC	

STYLE 1:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. BASE
5. EMITTER

CASE 398–03
ISSUE C

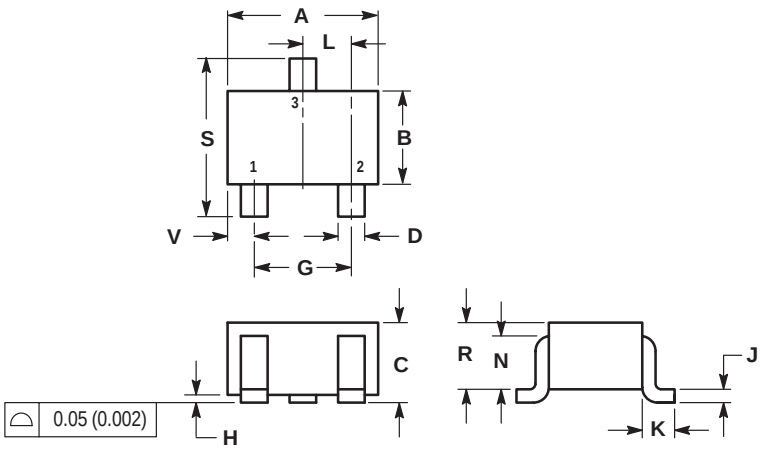


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.965	0.985	24.52	25.01
B	0.245	0.265	6.23	6.73
C	0.165	0.185	4.20	4.69
D	0.050	0.070	1.27	1.77
E	0.070	0.080	1.78	2.03
G	0.254 BSC		6.45 BSC	
H	0.095	0.105	2.42	2.66
J	0.003	0.006	0.08	0.15
K	0.625	0.675	15.88	17.14
N	0.495	0.520	12.58	13.20
Q	0.120	0.140	3.05	3.55
U	0.725 BSC		18.42 BSC	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 412–01
ISSUE O

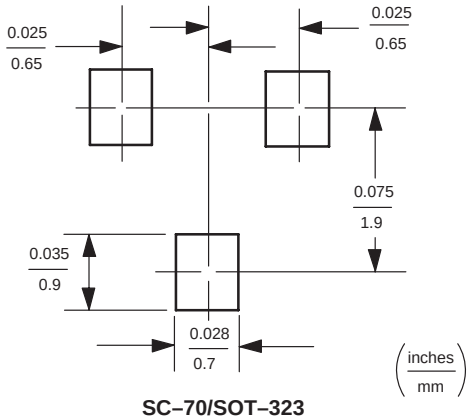


STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

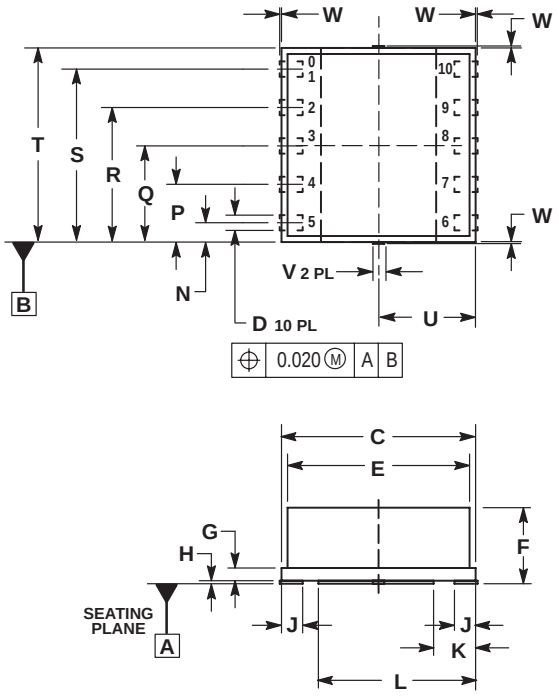
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.035	0.049	0.90	1.25
D	0.012	0.016	0.30	0.40
G	0.047	0.055	1.20	1.40
H	0.000	0.004	0.00	0.10
J	0.004	0.010	0.10	0.25
K	0.017 REF		0.425 REF	
L	0.026 BSC		0.650 BSC	
N	0.028 REF		0.700 REF	
R	0.031	0.039	0.80	1.00
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

CASE 419–02
ISSUE J



SC–70/SOT–323
FOOTPRINT

CASE DIMENSIONS (continued)

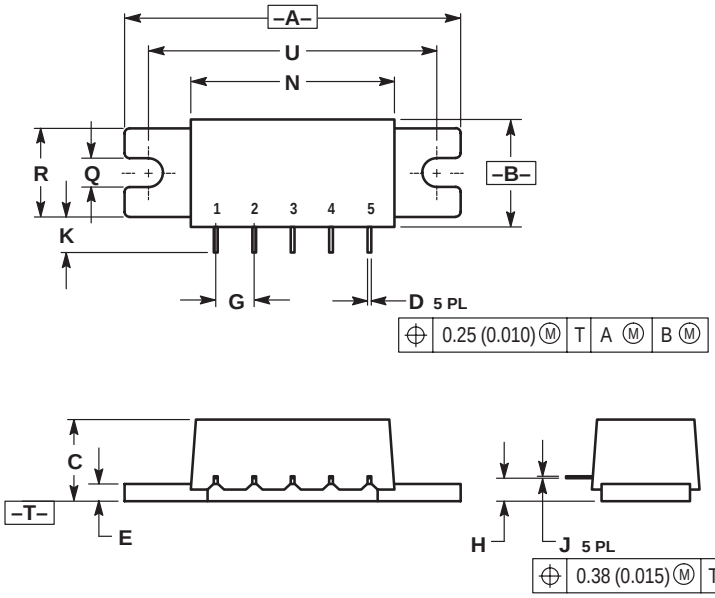


NOTES:
1. DIMENSIONS ARE IN INCHES.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994.

DIM	INCHES MIN	INCHES MAX
C	0.495	0.505
D	0.035	0.045
E	0.474 REF	
F	0.186	0.196
G	0.033 REF	
H	0.008 REF	
J	0.050	0.060
K	0.100 REF	
L	0.400 REF	
N	0.050 REF	
P	0.150 REF	
Q	0.250 REF	
R	0.350 REF	
S	0.450 REF	
T	0.495	0.505
U	0.250 REF	
V	0.025	0.035
W	—	0.005

STYLE 1:
PIN 1. GROUND
2. GROUND
3. R.F. IN
4. GROUND
5. GROUND
6. GROUND
7. GROUND
8. R.F. OUT
9. GROUND
10. +VDC

CASE 438F–01
ISSUE O



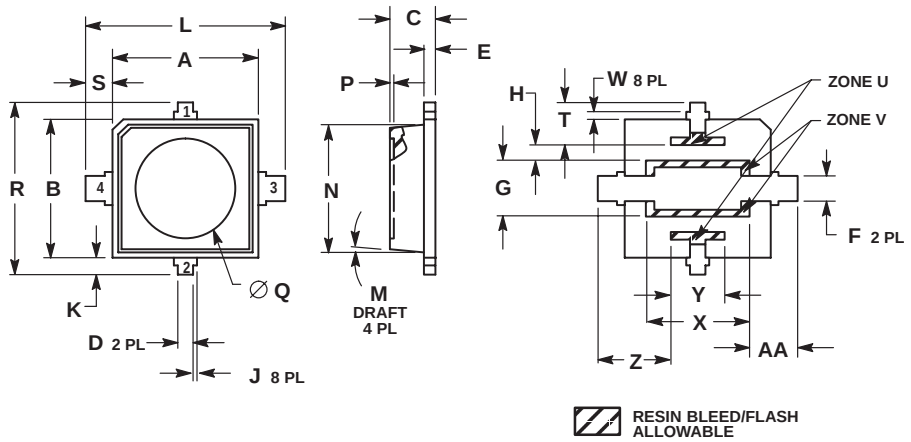
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.740	1.760	44.20	44.70
B	0.550	0.570	13.97	14.49
C	0.405	0.445	10.29	11.30
D	0.018	0.022	0.46	0.55
E	0.085	0.095	2.16	2.41
G	0.200 BSC		5.08 BSC	
H	0.120 BSC		3.05 BSC	
J	0.009	0.011	0.23	0.28
K	0.180	0.220	4.57	5.59
N	1.045	1.075	26.54	27.30
Q	0.145	0.155	3.68	3.94
R	0.455	0.465	11.56	11.81
U	1.490	1.510	37.85	38.35

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. RESISTOR–GROUND
4. VCC
5. RF OUTPUT

STYLE 2:
PIN 1. RF INPUT
2. GROUND
3. VCC1
4. VCC2
5. RF OUTPUT

CASE 448–02
ISSUE B

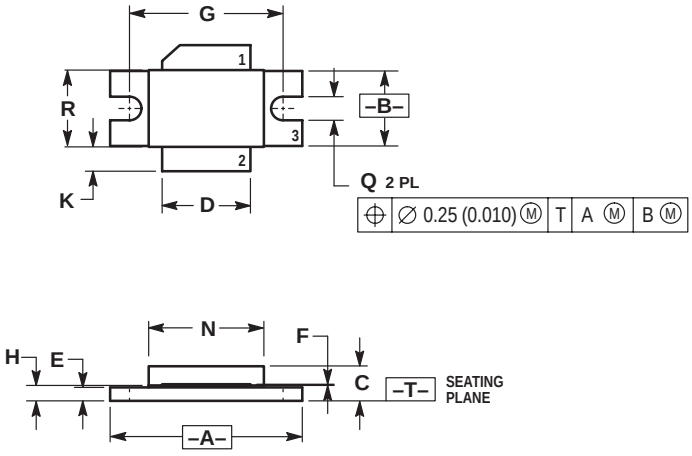


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.185	0.195	4.70	4.95
B	0.175	0.185	4.44	4.70
C	0.058	0.064	1.47	1.63
D	0.017	0.023	0.43	0.58
E	0.014	0.017	0.36	0.43
F	0.027	0.033	0.69	0.84
G	0.071	0.077	1.80	1.96
H	0.017	0.023	0.43	0.58
J	0.000	0.007	0.00	0.18
K	0.018	0.026	0.46	0.66
L	0.253	0.263	6.43	6.68
M	5 °REF		5 °REF	
N	1.75 REF		4.44 REF	
P	0.000	0.006	0.00	0.15
Q	0.120	0.130	3.05	3.30
R	0.220	0.230	5.59	5.84
S	0.030	0.038	0.76	0.97
T	0.050	0.060	1.27	1.52
U	0.000	0.018	0.00	0.46
V	0.000	0.014	0.00	0.36
W	0.004	0.016	0.10	0.41
X	0.131	0.141	3.33	3.58
Y	0.065	0.075	1.65	1.90
Z	0.089	0.099	2.26	2.51
AA	0.056	0.066	1.42	1.67

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. SOURCE

CASE 449–02
ISSUE A

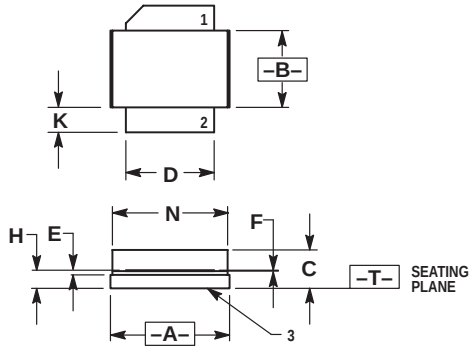


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.995	1.005	25.27	25.53
B	0.380	0.390	9.65	9.91
C	0.156	0.191	3.96	4.85
D	0.455	0.465	11.56	11.81
E	0.060	0.075	1.52	1.91
F	0.004	0.006	0.10	0.15
G	0.800 BSC		20.32 BSC	
H	0.078	0.090	1.98	2.29
K	0.117	0.137	2.97	3.48
N	0.595	0.605	15.11	15.37
Q	0.120	0.130	3.05	3.30
R	0.395	0.410	10.03	10.41

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

CASE 451–06
ISSUE F

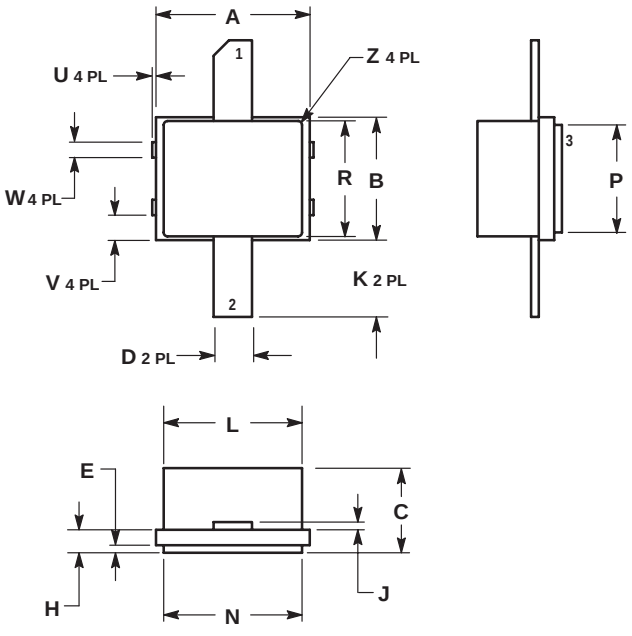


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.615	0.625	15.62	15.88
B	0.395	0.410	10.03	10.41
C	0.156	0.191	3.96	4.85
D	0.455	0.465	11.56	11.81
E	0.060	0.075	1.52	1.91
F	0.004	0.006	0.10	0.15
H	0.078	0.090	1.98	2.29
K	0.117	0.137	2.97	3.48
N	0.595	0.605	15.11	15.37

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

CASE 451A–03
ISSUE B

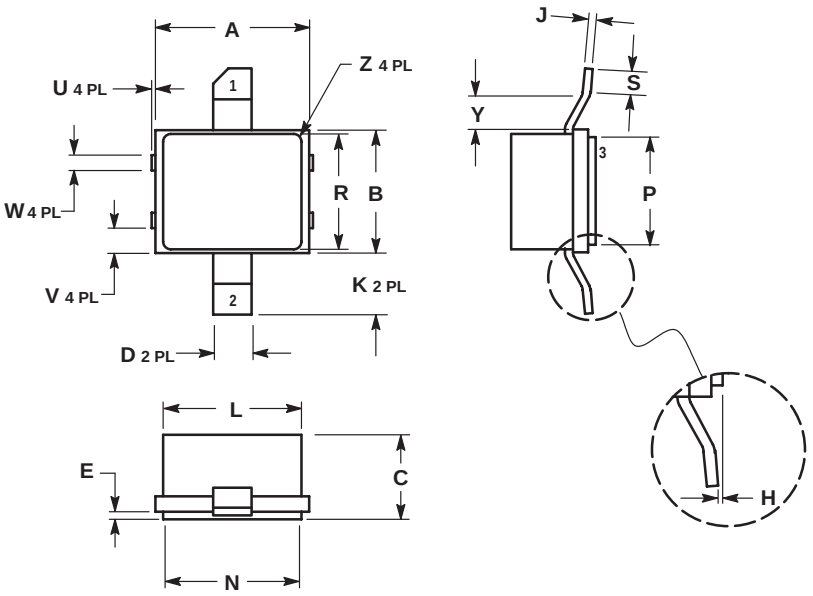


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM THE BODY OF THE PACKAGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.197	0.203	5.00	5.16
B	0.157	0.163	3.99	4.14
C	0.085	0.110	2.16	2.79
D	0.047	0.053	1.19	1.35
E	0.006	0.010	0.15	0.25
H	0.025	0.031	0.64	0.79
J	0.006	0.010	0.15	0.25
K	0.060	0.100	1.52	2.54
L	0.177	0.183	4.50	4.65
N	0.175	0.183	4.45	4.65
P	0.135	0.143	3.43	3.63
R	0.147	0.153	3.73	3.89
U	0.000	0.005	0.00	0.13
V	0.030	0.040	0.76	1.02
W	0.017	0.023	0.43	0.58
Z	—	0.020	—	0.508

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 458–05
ISSUE E

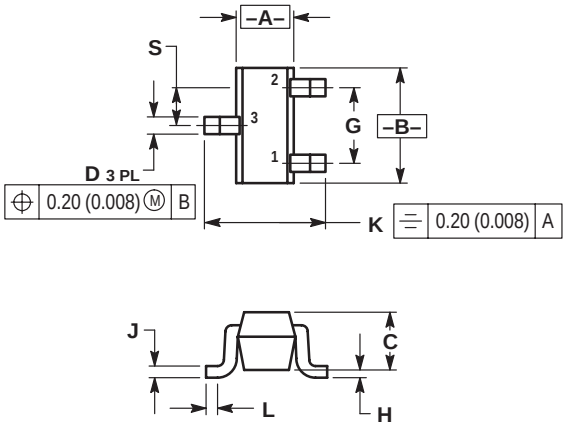


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION –H– (PACKAGE COPLANARITY): THE BOTTOM OF THE LEADS AND REFERENCE PLANE –T– MUST BE COPLANAR WITHIN DIMENSION –H–.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.197	0.203	5.00	5.16
B	0.157	0.163	3.99	4.14
C	0.085	0.110	2.16	2.79
D	0.047	0.053	1.19	1.35
E	0.006	0.010	0.15	0.25
H	0.000	0.004	0.00	0.10
J	0.006	0.010	0.15	0.25
K	0.050	0.080	1.27	2.03
L	0.177	0.183	4.50	4.65
N	0.175	0.183	4.45	4.65
P	0.135	0.143	3.43	3.63
R	0.147	0.153	3.73	3.89
S	0.020	0.040	0.51	1.02
U	0.000	0.005	0.00	0.13
V	0.030	0.040	0.76	1.02
W	0.017	0.023	0.43	0.58
Y	0.030	0.040	0.76	1.02
Z	—	0.020	—	0.508

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 458A–02
ISSUE A

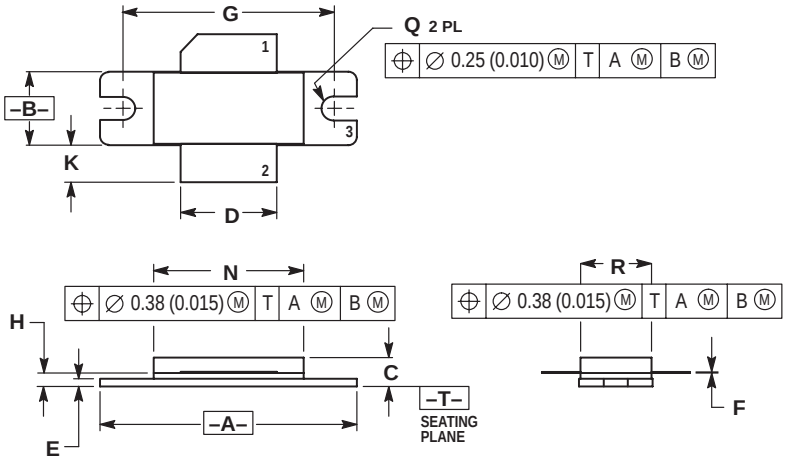


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	0.70	0.80	0.028	0.031
B	1.40	1.80	0.055	0.071
C	0.60	0.90	0.024	0.035
D	0.15	0.30	0.006	0.012
G	1.00 BSC		0.039 BSC	
H	—	0.10	—	0.004
J	0.10	0.25	0.004	0.010
K	1.45	1.75	0.057	0.069
L	0.10	0.20	0.004	0.008
S	0.50 BSC		0.020 BSC	

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

CASE 463–01
ISSUE A
(SC–90/SC–75)

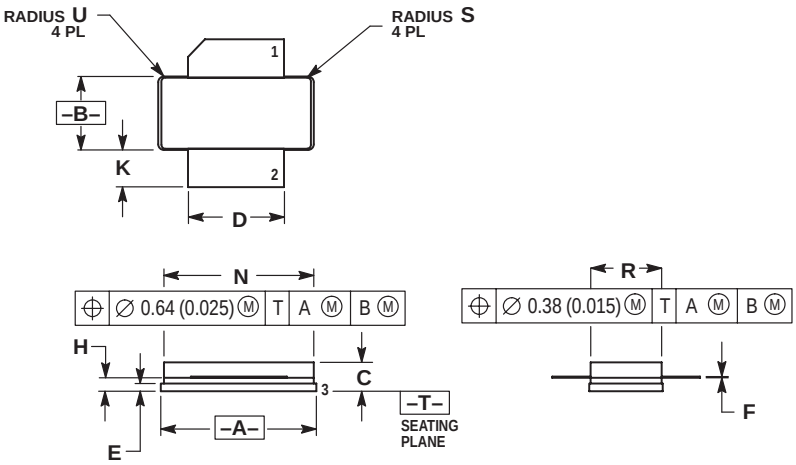


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.055	0.065	1.40	1.65
K	0.170	0.210	4.32	5.33
N	0.772	0.788	19.60	20.00
Q	0.118	0.138	3.00	3.51
R	0.365	0.375	9.27	9.53

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465–04
ISSUE D

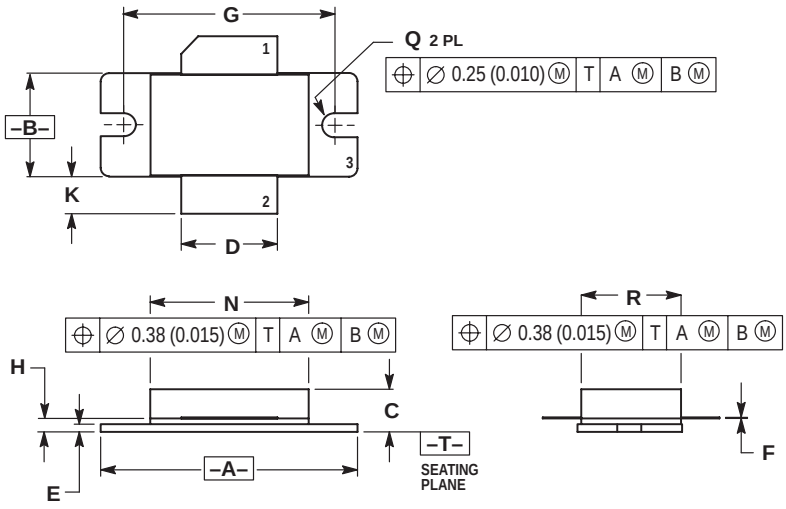


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.055	0.065	1.40	1.65
K	0.170	0.210	4.32	5.33
N	0.775	0.785	19.69	19.94
R	0.365	0.375	9.27	9.53
S	0.020 REF		0.51 REF	
U	0.030 REF		0.76 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
4. SOURCE

CASE 465A–04
ISSUE D

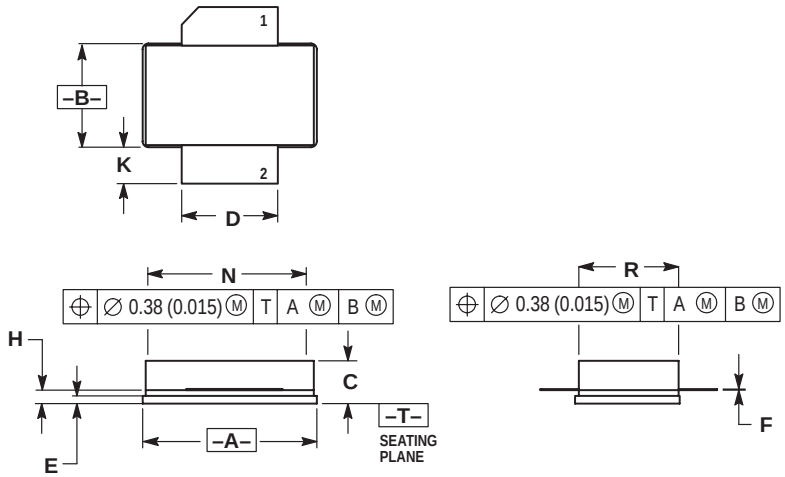


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.535	0.545	13.6	13.8
C	0.155	0.200	3.94	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
N	0.871	0.889	19.30	22.60
Q	0.118	0.138	3.00	3.51
R	0.515	0.525	13.10	13.30

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465B–02
ISSUE A

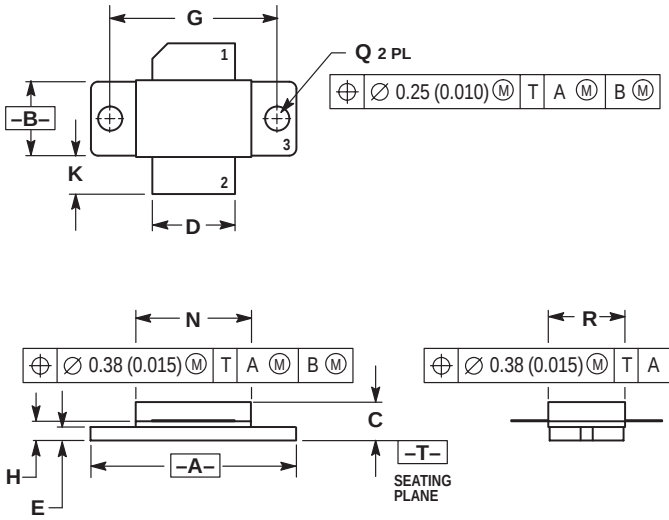


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.6	13.8
C	0.155	0.200	3.94	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465C–01
ISSUE O

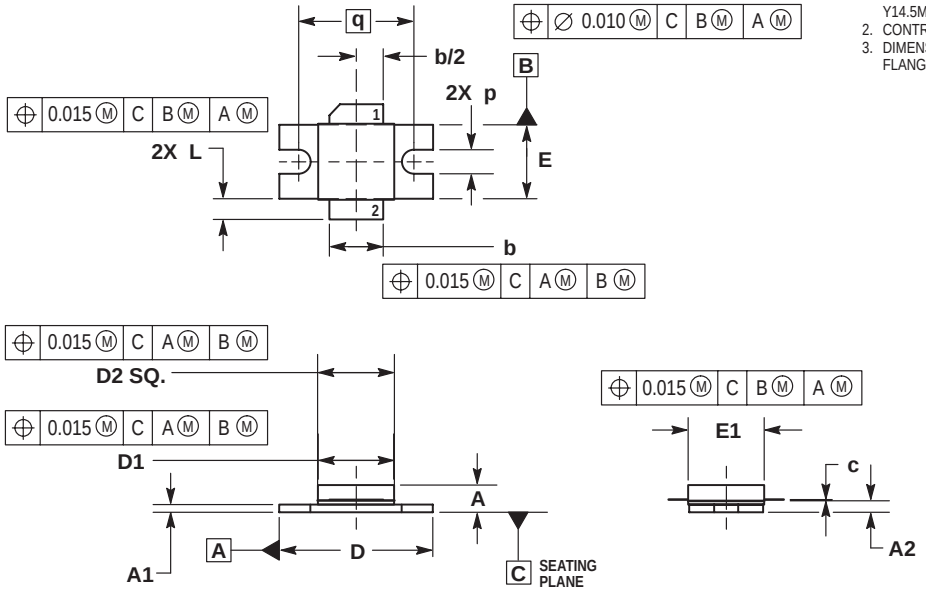


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.065	1.075	27.05	27.31
B	0.380	0.390	9.65	9.91
C	0.160	0.205	4.06	5.21
D	0.425	0.435	10.80	11.05
E	0.060	0.070	1.52	1.78
F	0.004	0.006	0.10	0.15
G	0.870 BSC		22.10 BSC	
H	0.096	0.106	2.44	2.70
K	0.185	0.215	4.70	5.46
N	0.591	0.601	15.01	15.27
Q	0.124	0.130	3.15	3.30
R	0.392	0.404	9.96	10.26

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465D–02
ISSUE A



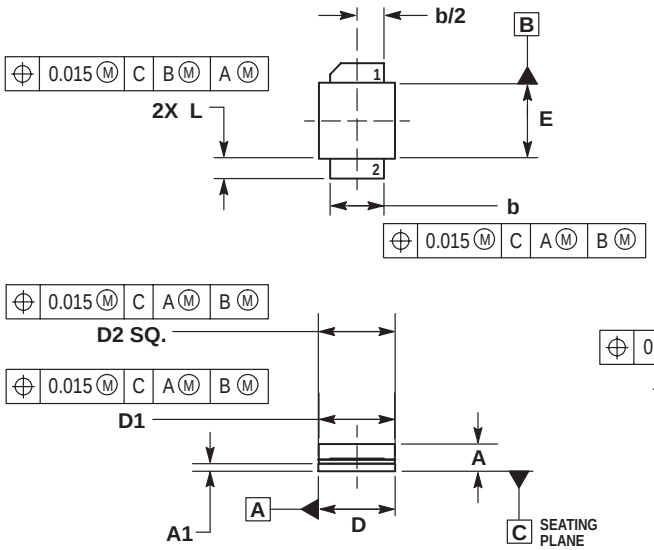
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A2 IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES	
DIM	MIN	MAX
A	0.125	0.160
A1	0.035	0.045
A2	0.057	0.067
b	0.275	0.285
c	0.003	0.006
D	0.795	0.805
D1	0.392	0.400
D2	0.395	0.405
E	0.380	0.390
E1	0.392	0.400
L	0.092	0.122
p	0.118	0.138
q	0.600 BSC	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465E–01
ISSUE A

CASE DIMENSIONS (continued)



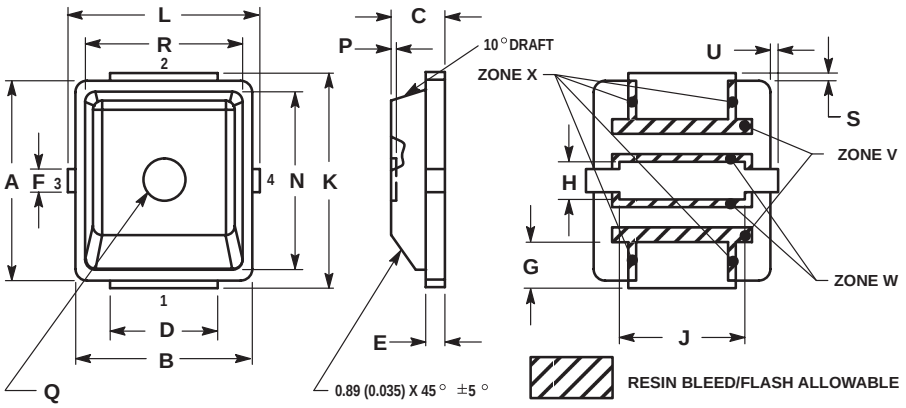
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A2 IS MEASURED 0.030" AWAY FROM FLANGE.

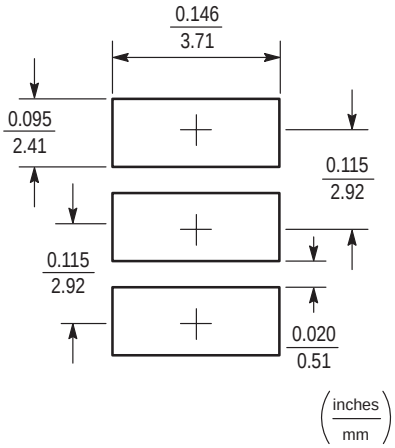
	INCHES	
DIM	MIN	MAX
A	0.125	0.160
A1	0.035	0.045
A2	0.057	0.067
b	0.275	0.285
c	0.003	0.006
D	0.395	0.405
D1	0.392	0.400
D2	0.395	0.405
E	0.395	0.405
E1	0.392	0.400
L	0.092	0.122

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465F–01
ISSUE O

CASE DIMENSIONS (continued)





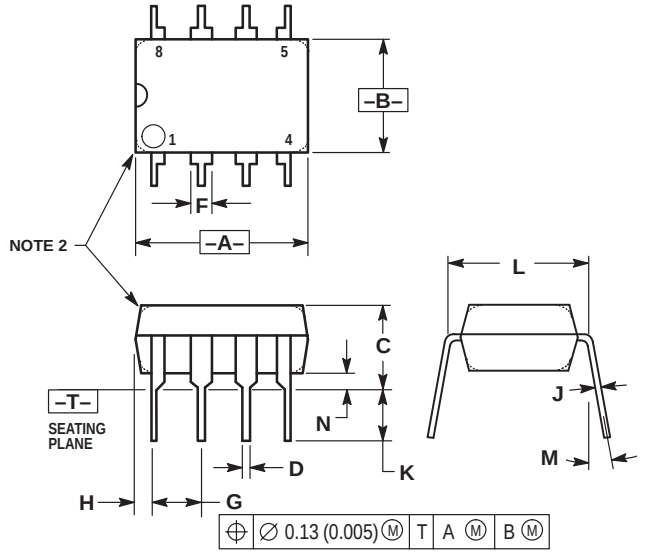
SOLDER FOOTPRINT

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.255	0.265	6.48	6.73
B	0.225	0.235	5.72	5.97
C	0.065	0.072	1.65	1.83
D	0.130	0.150	3.30	3.81
E	0.021	0.026	0.53	0.66
F	0.026	0.044	0.66	1.12
G	0.050	0.070	1.27	1.78
H	0.045	0.063	1.14	1.60
J	0.160	0.180	4.06	4.57
K	0.273	0.285	6.93	7.24
L	0.245	0.255	6.22	6.48
N	0.230	0.240	5.84	6.10
P	0.000	0.008	0.00	0.20
Q	0.055	0.063	1.40	1.60
R	0.200	0.210	5.08	5.33
S	0.006	0.012	0.15	0.31
U	0.006	0.012	0.15	0.31
ZONE V	0.000	0.021	0.00	0.53
ZONE W	0.000	0.010	0.00	0.25
ZONE X	0.000	0.010	0.00	0.25

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. SOURCE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. RESIN BLEED/FLASH ALLOWABLE IN ZONE V, W, AND X.

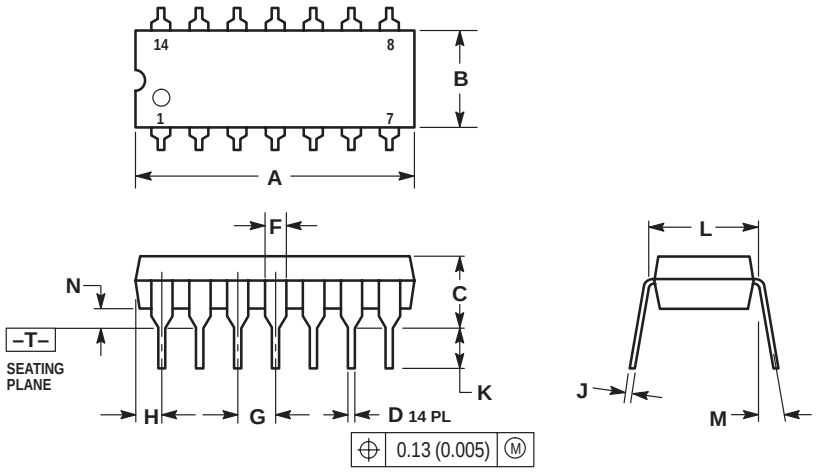
CASE 466–02
ISSUE B
(PLD–1.5)



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

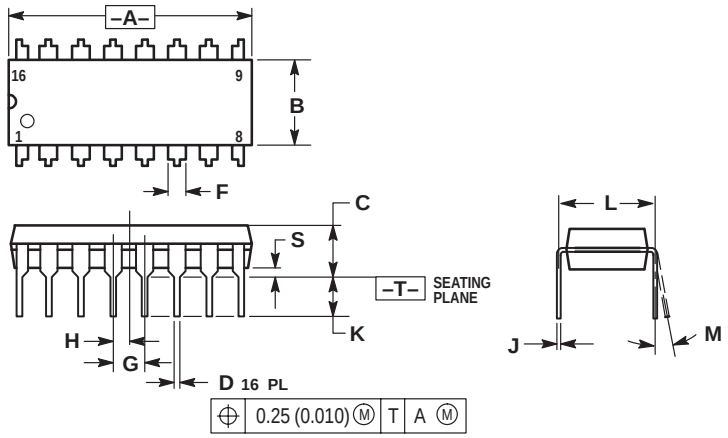
CASE 626–05
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	—	10°	—	10°
N	0.015	0.039	0.38	1.01

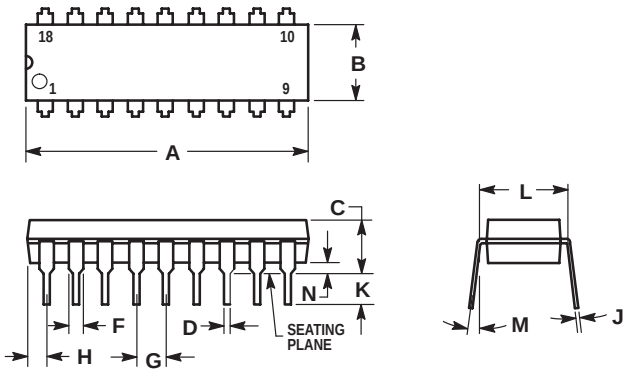
CASE 646–06
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

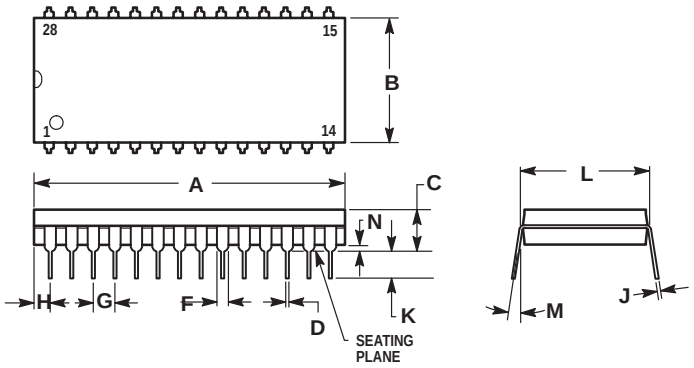
CASE 648–08
ISSUE R



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

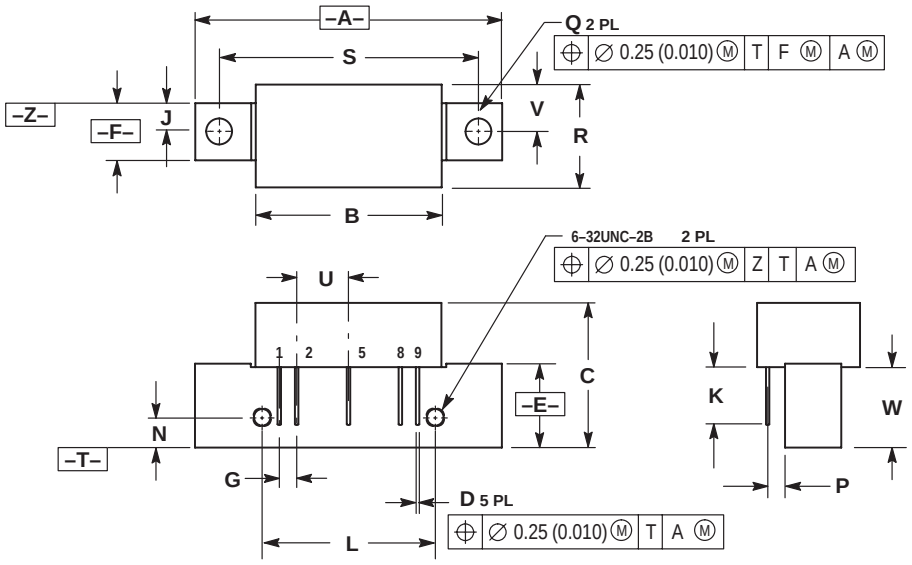
CASE 707–02
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 710–02
ISSUE B



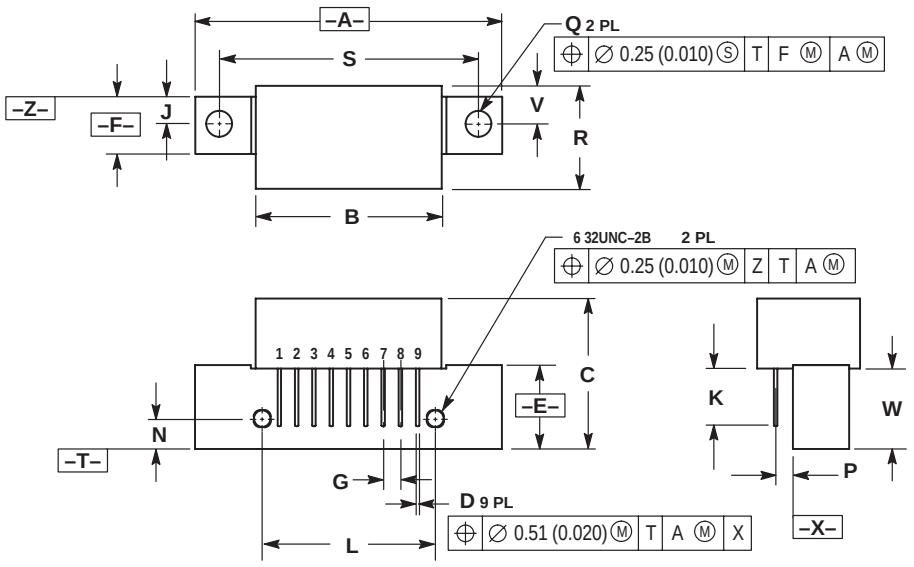
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	——	1.775	——	45.08
B	——	1.085	——	27.56
C	——	0.840	——	21.34
D	0.018	0.022	0.46	0.56
E	0.465	0.510	11.81	12.95
F	0.300	0.325	7.62	8.25
G	0.100 BSC		2.54 BSC	
J	0.156 BSC		3.96 BSC	
K	0.315	0.355	7.62	8.50
L	1.000 BSC		25.40 BSC	
N	0.165 BSC		4.19 BSC	
P	0.100 BSC		2.54 BSC	
Q	0.148	0.168	3.76	4.27
R	——	0.595	——	15.11
S	1.500 BSC		38.10 BSC	
U	0.300 BSC		7.62 BSC	
V	0.280 BSC		7.11 BSC	
W	0.435	0.450	11.05	11.43

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. DELETED
4. DELETED
5. VDC
6. DELETED
7. DELETED
8. GROUND
9. RF OUTPUT

CASE 714AA–01
ISSUE O

CASE DIMENSIONS (continued)

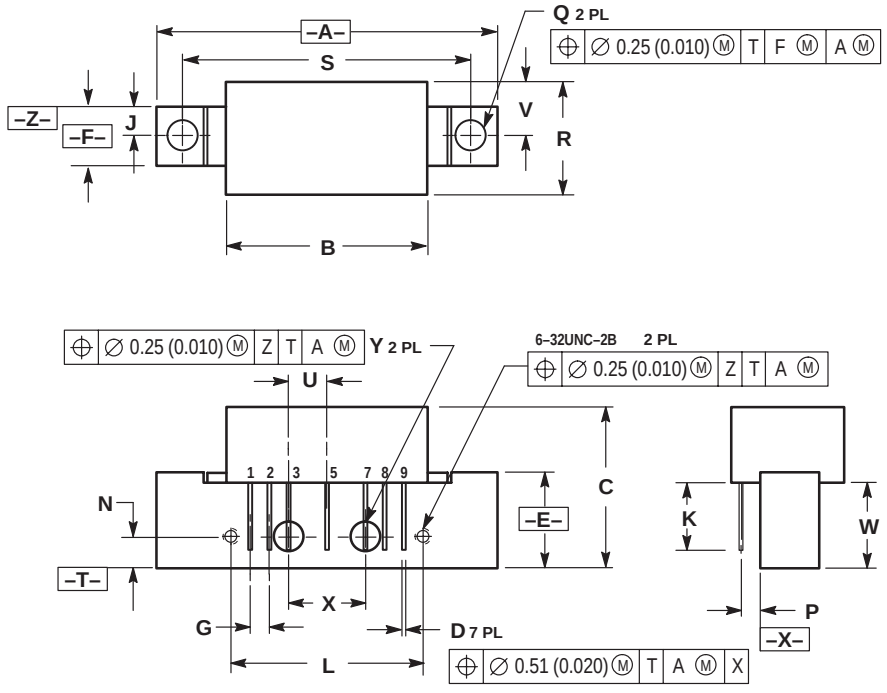


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	——	1.775	——	45.08
B	——	1.085	——	27.56
C	——	0.870	——	22.10
D	0.018	0.022	0.46	0.56
E	0.465	0.510	11.81	12.95
F	0.300	0.325	7.62	8.25
G	0.100 BSC		2.54 BSC	
J	0.156 BSC		3.96 BSC	
K	0.330	0.370	8.38	9.40
L	1.000 BSC		25.40 BSC	
N	0.165 BSC		4.19 BSC	
P	0.100 BSC		2.54 BSC	
Q	0.148	0.168	3.76	4.27
R	——	0.595	——	15.11
S	1.500 BSC		38.10 BSC	
V	0.209	0.239	5.31	6.07
W	0.425	——	10.80	——

STYLE 2:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. RESISTOR-GROUND
5. GROUND
6. GROUND
7. GROUND
8. V_{CC} 1
9. RF OUTPUT

CASE 714P–03
ISSUE B



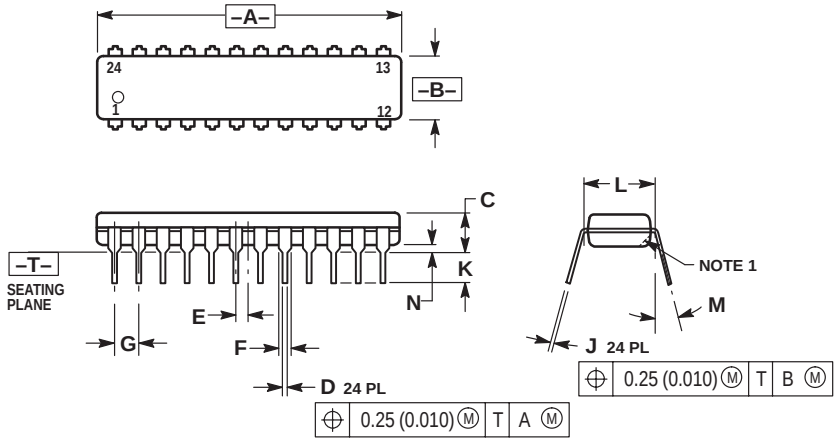
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	——	1.775	——	45.08
B	——	1.085	——	27.56
C	——	0.840	——	21.34
D	0.018	0.022	0.46	0.56
E	0.465	0.510	11.81	12.95
F	0.300	0.325	7.62	8.25
G	0.100 BSC		2.54 BSC	
J	0.156 BSC		3.96 BSC	
K	0.315	0.355	8.00	8.50
L	1.00 BSC		25.40 BSC	
N	0.165 BSC		4.19 BSC	
P	0.100 BSC		2.54 BSC	
Q	0.148	0.168	3.76	4.27
R	——	0.600	——	15.24
S	1.500 BSC		38.10 BSC	
U	0.200 BSC		5.08 BSC	
V	——	0.250	——	6.35
W	0.435	0.450	11.05	11.43
X	0.400 BSC		10.16 BSC	
Y	0.152	0.163	3.85	4.15

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

STYLE 2:
PIN 1. RF OUTPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF INPUT

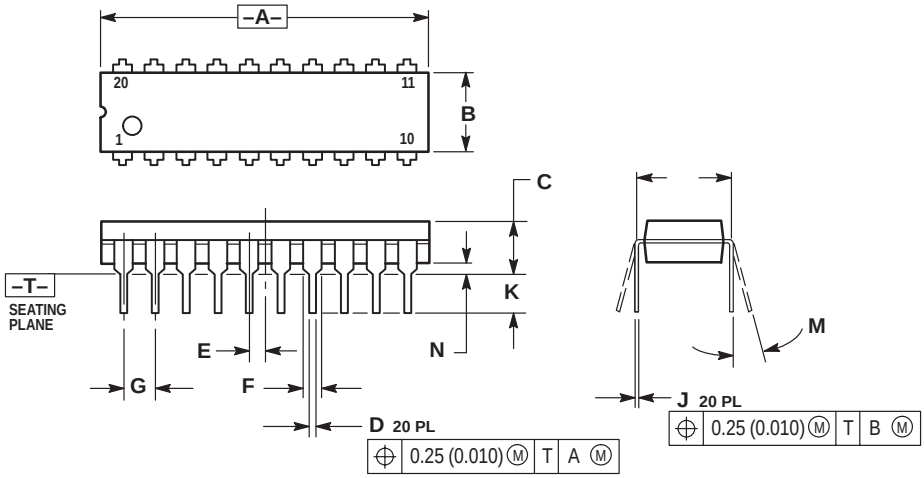
CASE 714Y–03
ISSUE D



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

CASE 724–03
ISSUE D

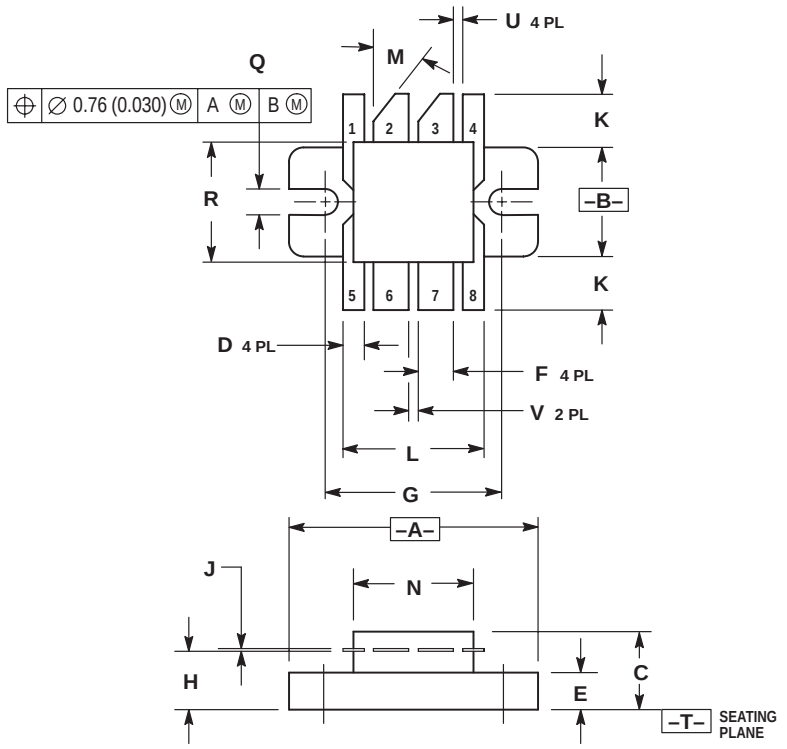


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

CASE 738–03
ISSUE E

CASE DIMENSIONS (continued)



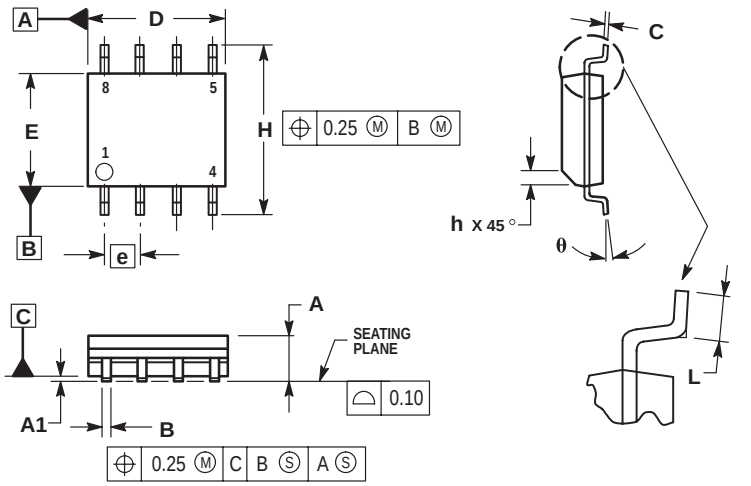
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

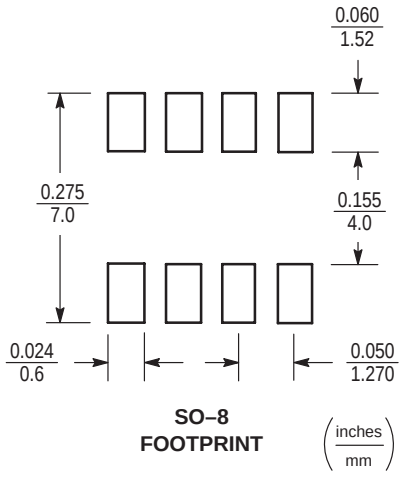
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.60	23.11	0.890	0.910
B	9.52	10.03	0.375	0.395
C	6.65	7.16	0.262	0.282
D	1.60	1.95	0.063	0.077
E	2.94	3.40	0.116	0.134
F	2.87	3.22	0.113	0.127
G	16.51 BSC		0.650 BSC	
H	4.01	4.36	0.158	0.172
J	0.07	0.15	0.003	0.006
K	4.34	4.90	0.171	0.193
L	12.45	12.95	0.490	0.510
M	45° NOM		45° NOM	
N	1.051	11.02	0.414	0.434
Q	3.04	3.35	0.120	0.132
R	9.90	10.41	0.390	0.410
U	1.02	1.27	0.040	0.050
V	0.64	0.89	0.025	0.035

STYLE 1:
PIN 1. EMITTER (COMMON)
2. COLLECTOR
3. COLLECTOR
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE
7. BASE
8. EMITTER (COMMON)

STYLE 2:
PIN 1. SOURCE (COMMON)
2. DRAIN
3. DRAIN
4. SOURCE (COMMON)
5. SOURCE (COMMON)
6. GATE
7. GATE
8. SOURCE (COMMON)

CASE 744A–01
ISSUE C





SO–8
FOOTPRINT

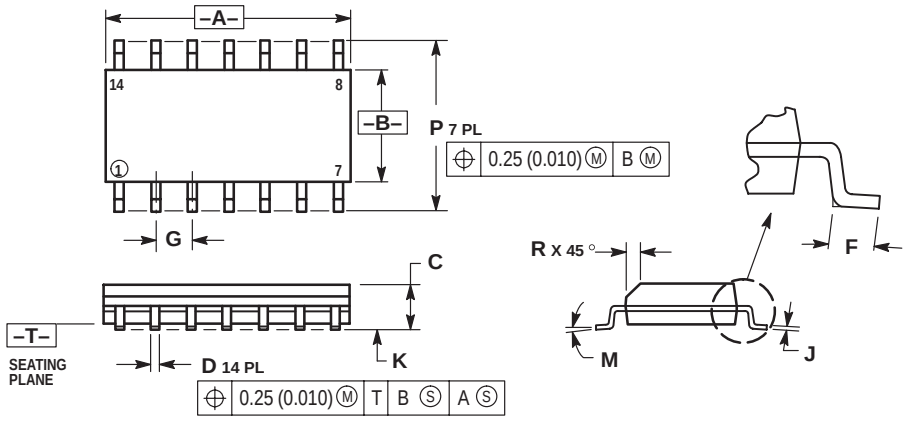
STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

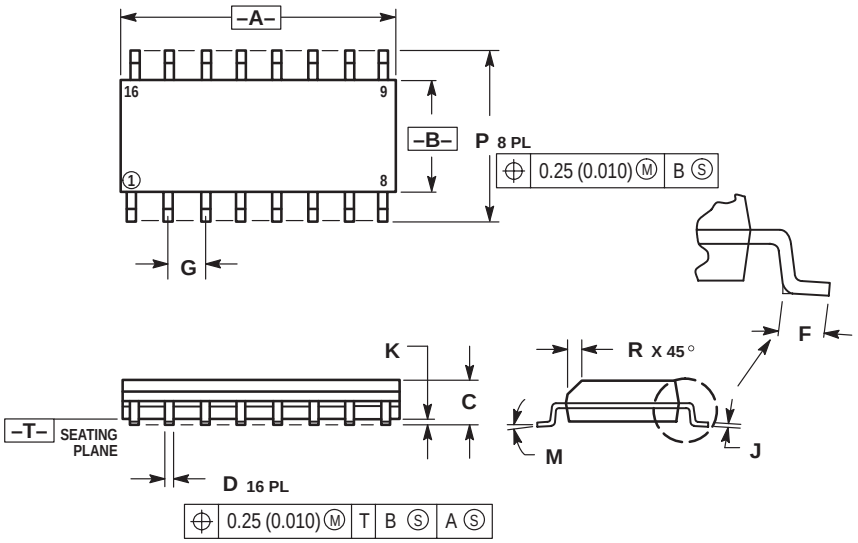
CASE 751–06
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

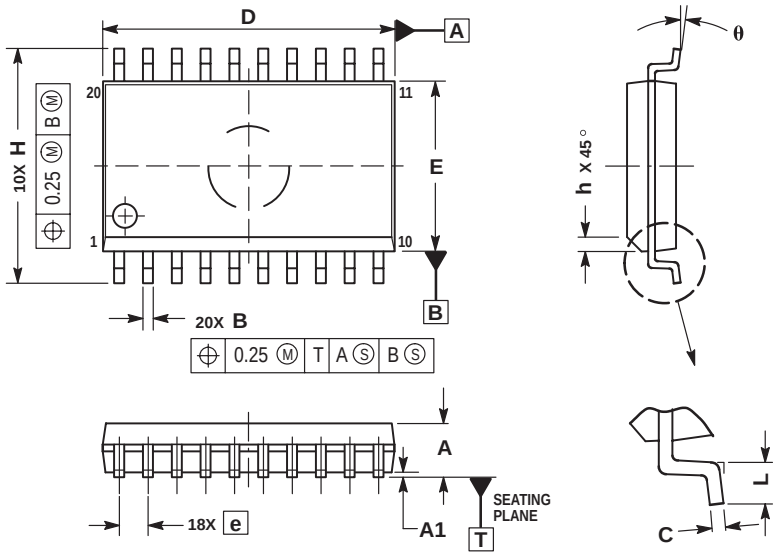
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

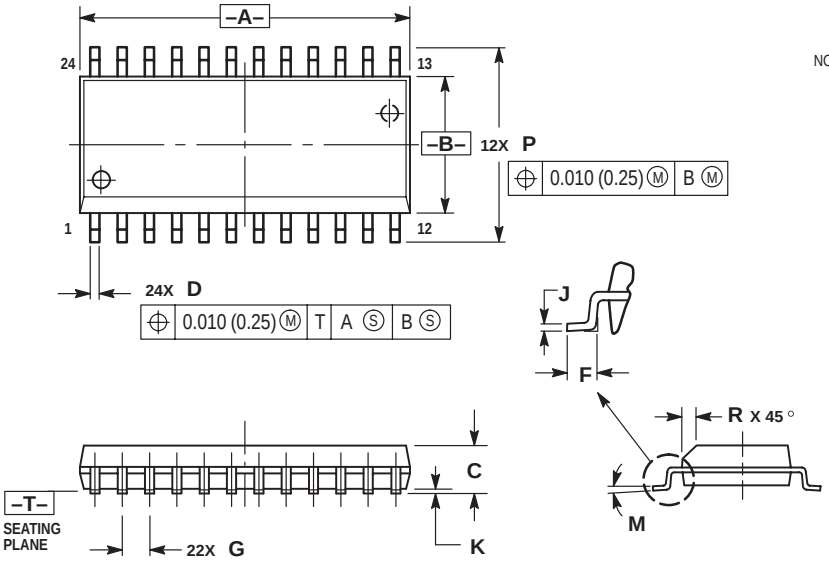
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

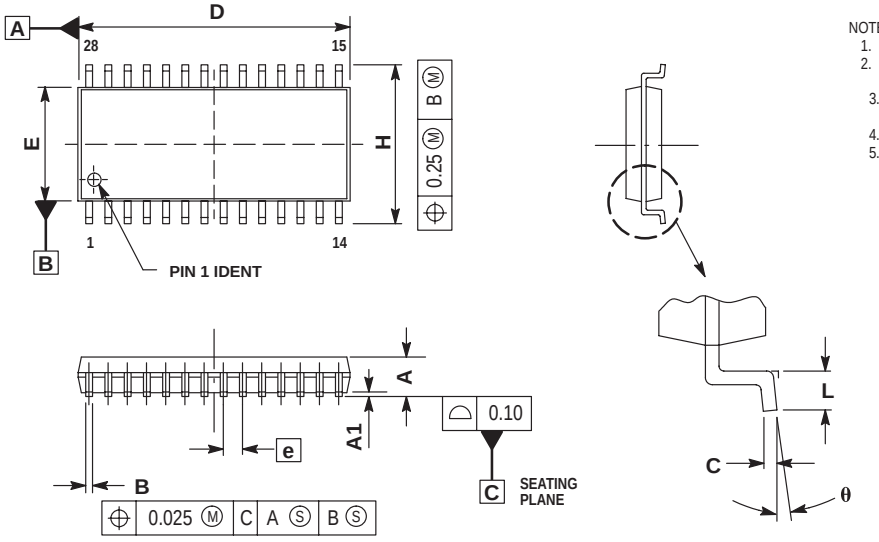
CASE 751D–05
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

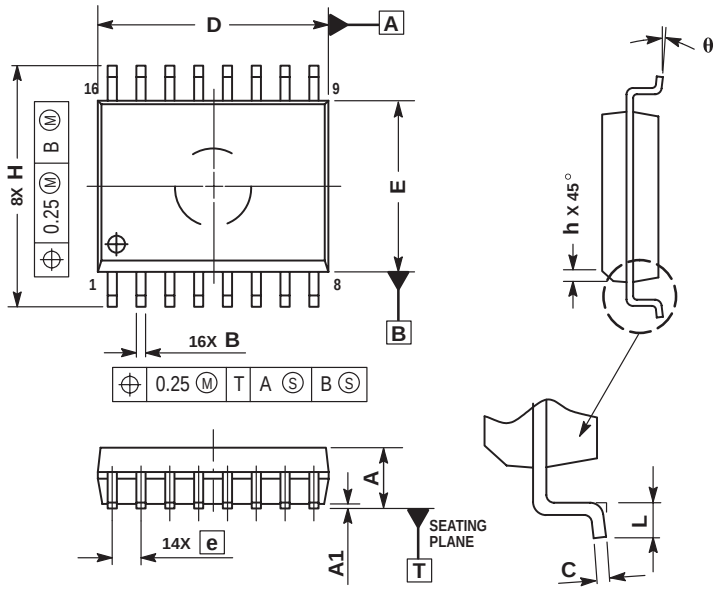
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
4. MAXIMUM MOLD PROTRUSION 0.015 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
θ	0 °	8 °

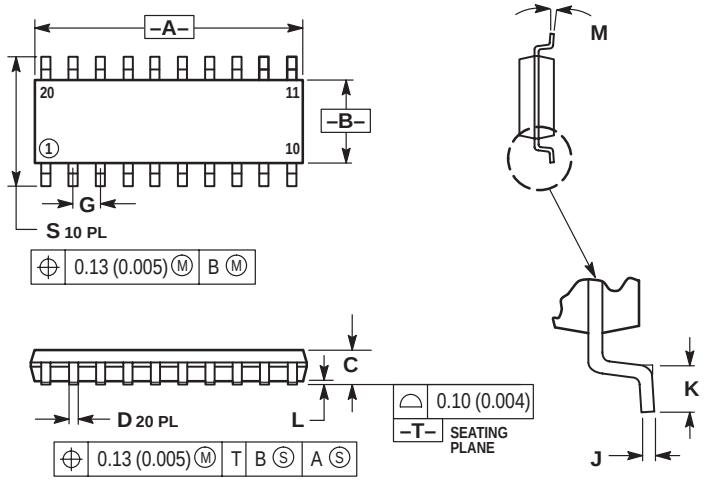
CASE 751F–05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

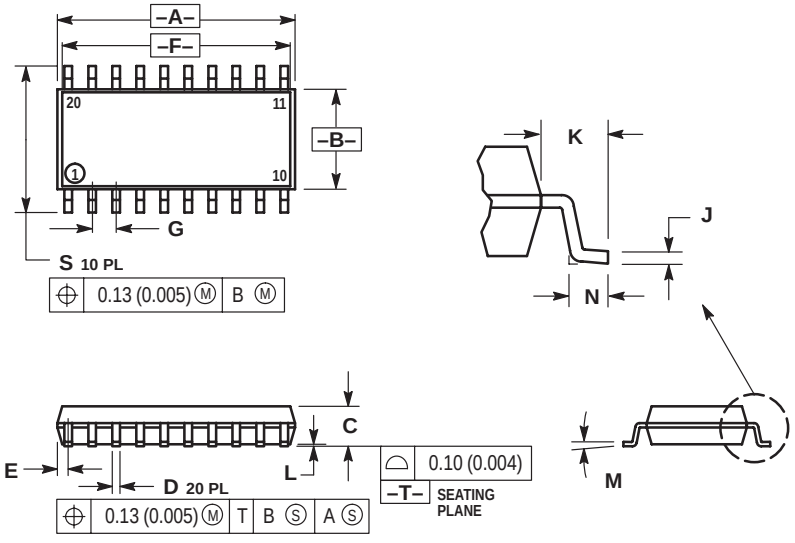
CASE 751G–03
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.12 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.55	12.80	0.494	0.504
B	5.10	5.40	0.201	0.213
C	—	2.00	—	0.079
D	0.35	0.45	0.014	0.018
G	1.27 BSC		0.050 BSC	
J	0.18	0.23	0.007	0.009
K	0.55	0.85	0.022	0.033
L	0.05	0.20	0.002	0.008
M	0 °	7 °	0 °	7 °
S	7.40	8.20	0.291	0.323

CASE 751J–02
ISSUE A



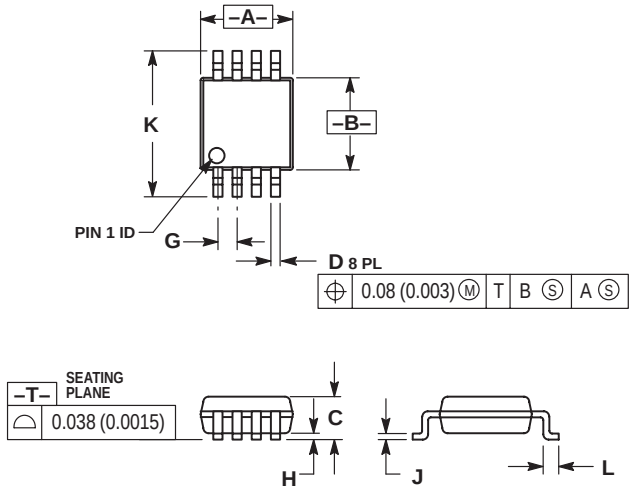
NOTES:
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: MILLIMETER.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
6. MAXIMUM MOLD PROTRUSION 0.15 (0.008) PER SIDE.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.006) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.35	12.80	0.486	0.504
B	5.10	5.45	0.201	0.215
C	1.95	2.05	0.077	0.081
D	0.35	0.50	0.014	0.020
E	—	0.81	—	0.032
F	12.40*		0.488*	
G	1.15	1.39	0.045	0.055
H	0.59	0.81	0.023	0.032
J	0.18	0.27	0.007	0.011
K	1.10	1.50	0.043	0.059
L	0.05	0.20	0.001	0.008
M	0 °	10 °	0 °	10 °
N	0.50	0.85	0.020	0.033
S	7.40	8.20	0.291	0.323

*APPROXIMATE

CASE 803C–01
PRELIMINARY

CASE DIMENSIONS (continued)

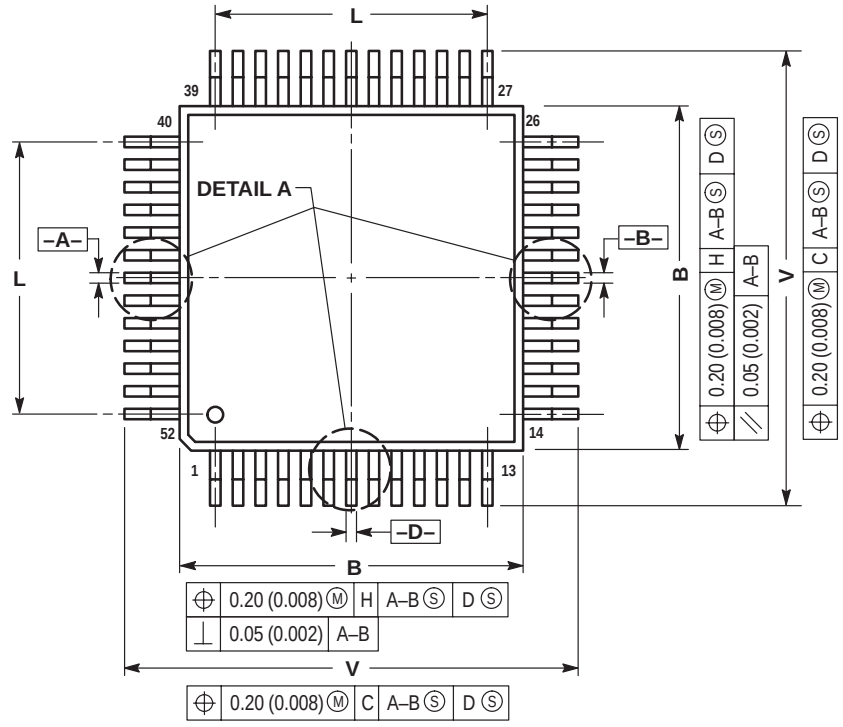


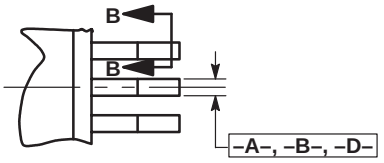
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	—	1.10	—	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

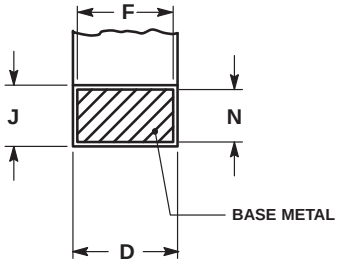
CASE 846A–02
ISSUE D
(Micro–8)

CASE DIMENSIONS (continued)



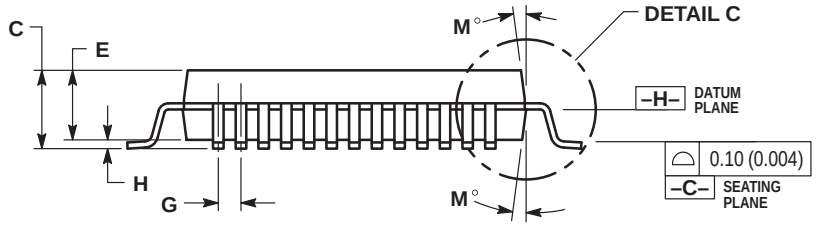


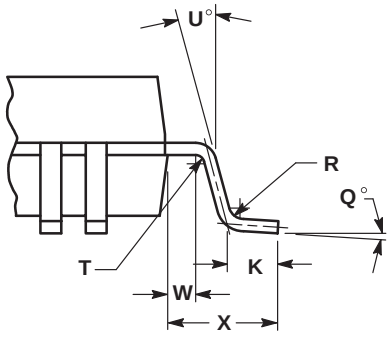
DETAIL A



0.02 (0.008) M C A–B S D S

SECTION B–B



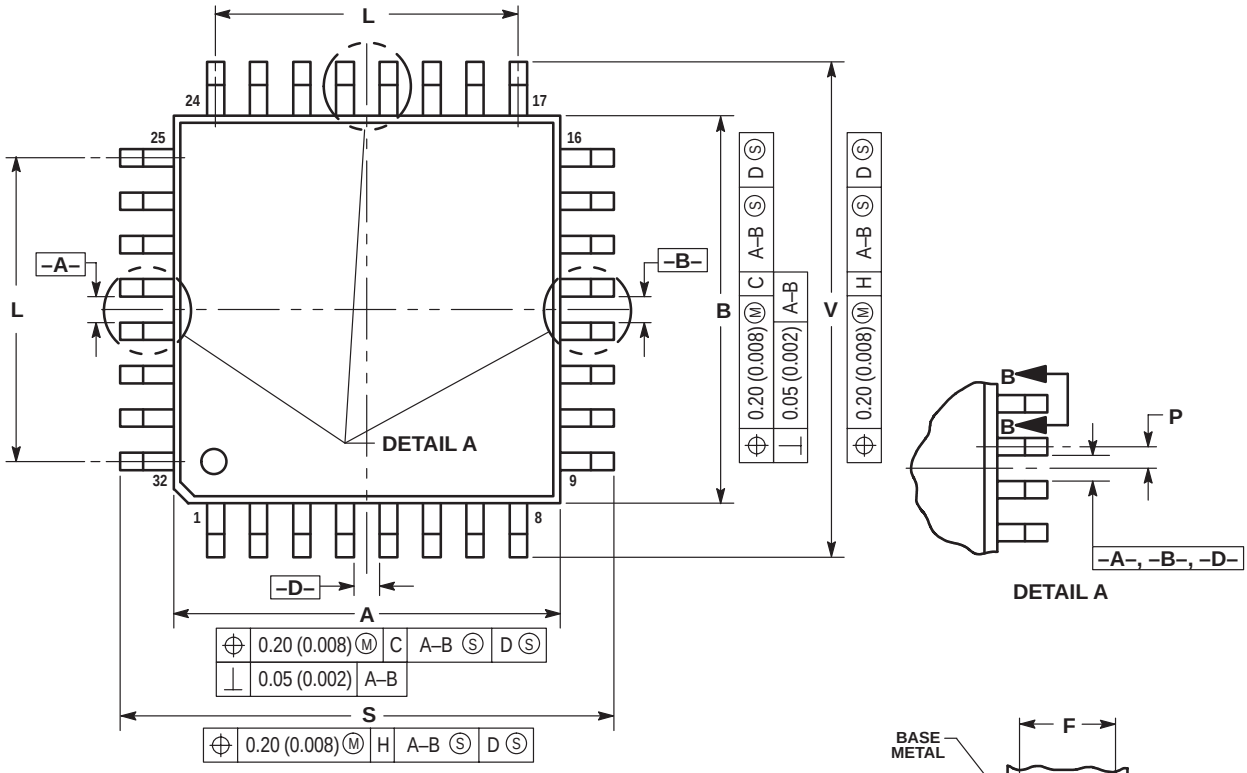


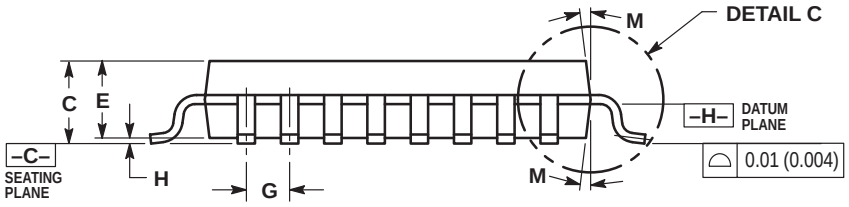
DETAIL C

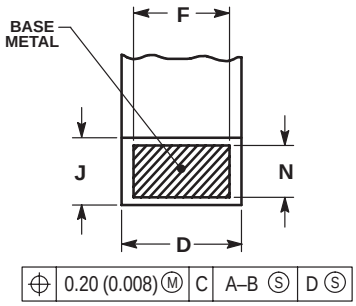
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.10	0.079	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	7.80 REF		0.307 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0°	—	0°	—
V	12.95	13.45	0.510	0.530
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.063 REF	

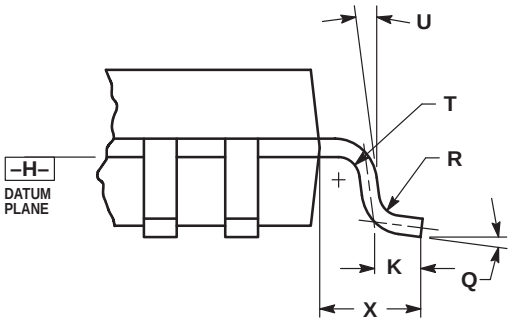
CASE 848B–04
ISSUE C







SECTION B–B
VIEW ROTATED 90 ° CLOCKWISE

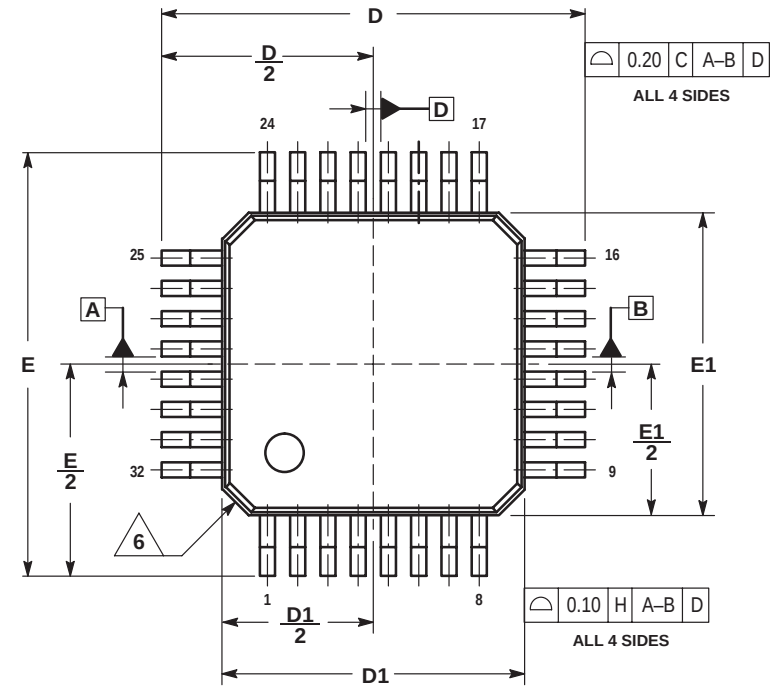


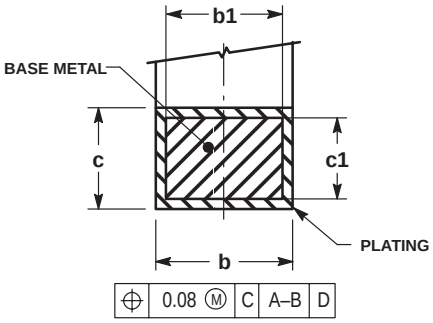
DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

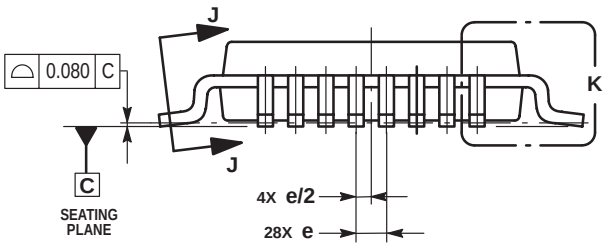
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC		0.031 BSC	
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6 °	8 °	6 °	8 °
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5 °	10°	5 °	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5 °	11°	5 °	11°
V	8.85	9.15	0.348	0.360
X	1.00 REF		0.039 REF	

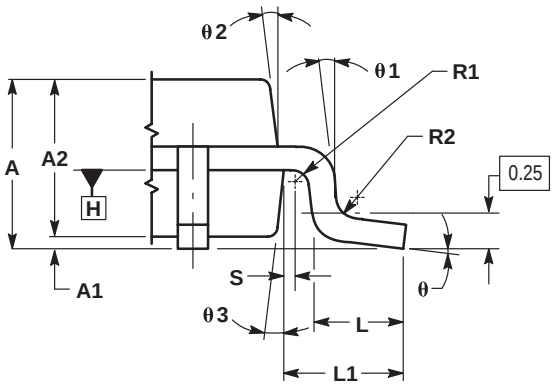
CASE 873–01
ISSUE A





SECTION J–J



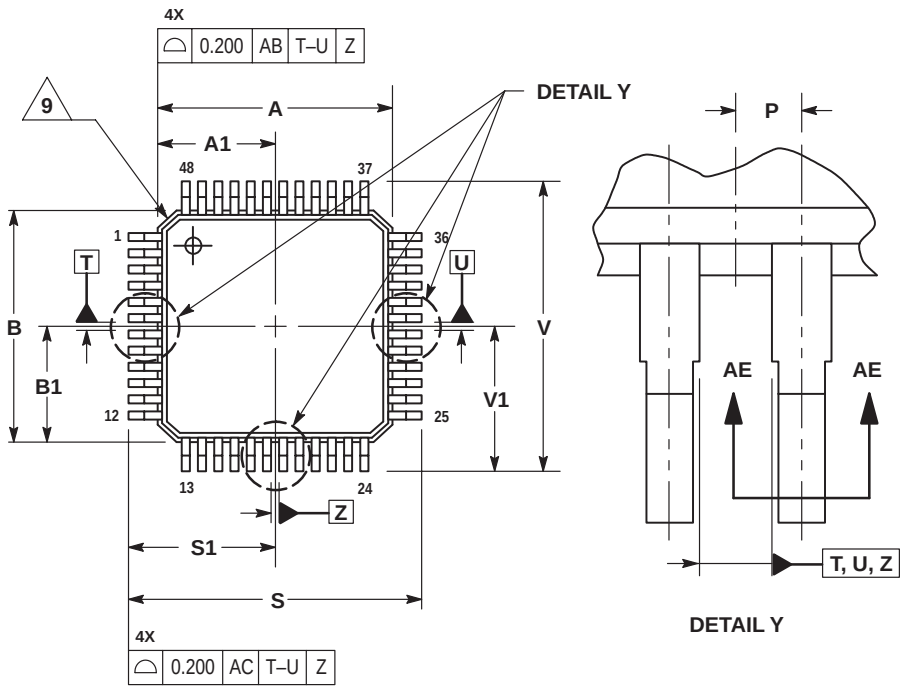


DETAIL K

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED WHERE THE LEADS EXIT THE PLASTIC BODY AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN A PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.
6. EXACT SHAPE OF CORNERS MAY VARY.

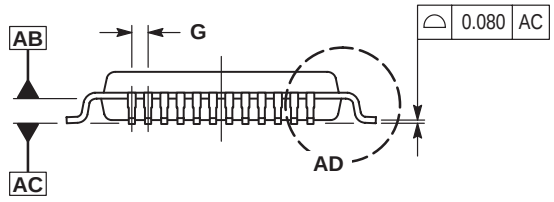
	MILLIMETERS	
DIM	MIN	MAX
A	—	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.18	0.27
b1	0.17	0.23
c	0.10	0.20
c1	0.09	0.16
D	7.00 BSC	
D1	5.00 BSC	
E	7.00 BSC	
E1	5.00 BSC	
e	0.50 BSC	
L	0.45	0.75
L1	1.00 REF	
R1	0.08	—
R2	0.08	0.20
S	0.20	—
θ	0°	7°
θ1	0°	—
θ2	11°	13°
θ3	11°	13°

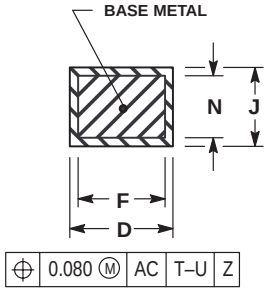
CASE 873C–01
ISSUE A



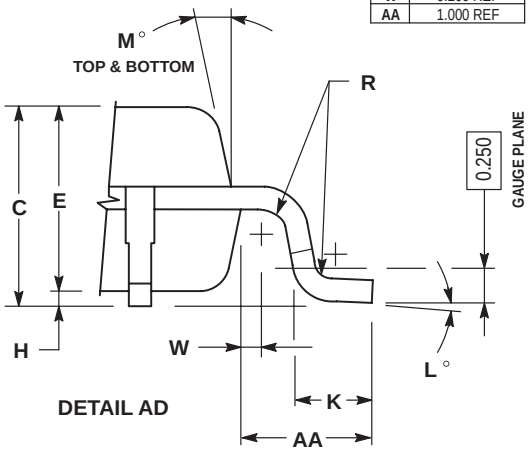
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	1°	5°
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	





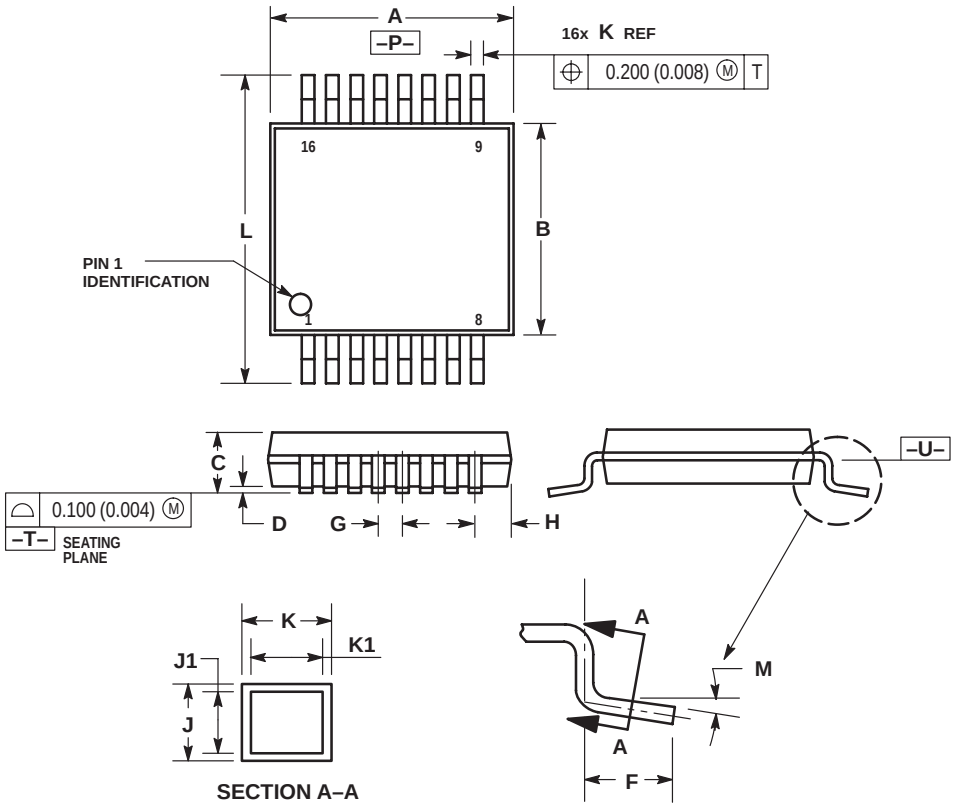
SECTION AE–AE



DETAIL AD

CASE 932–02
ISSUE E
(TQFP–48)

CASE DIMENSIONS (continued)

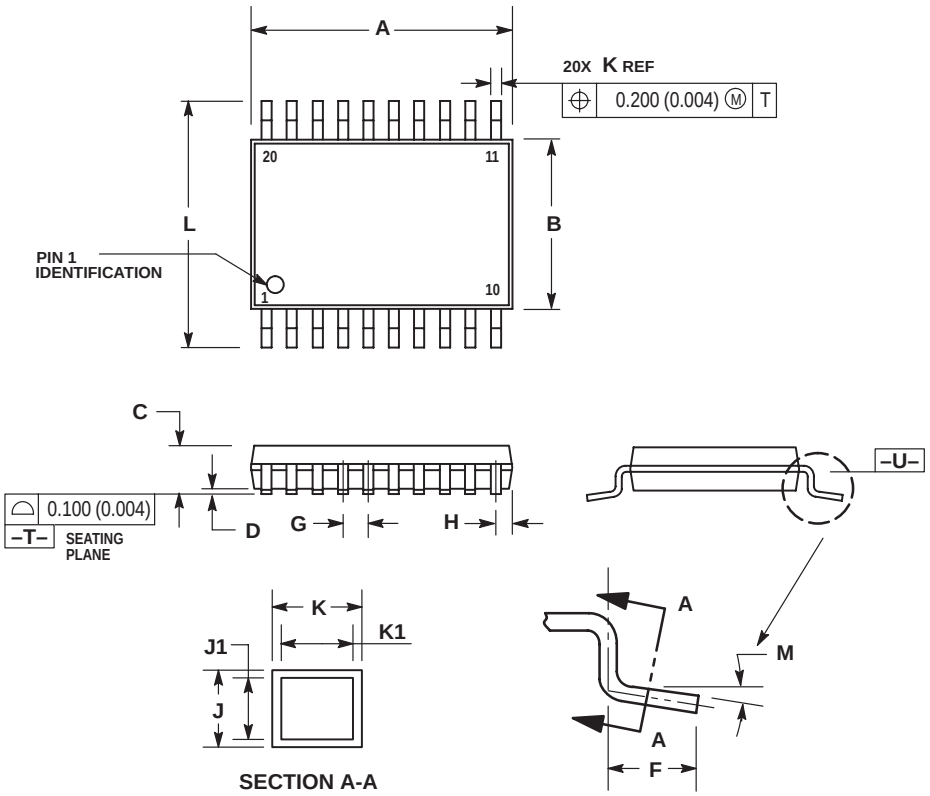


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –U–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	5.10	—	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0047
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC		0.026 BSC	
H	0.22	0.23	0.009	0.010
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	0°	10°	0°	10°

CASE 948C–03
ISSUE B
(TSSOP–16)

CASE DIMENSIONS (continued)

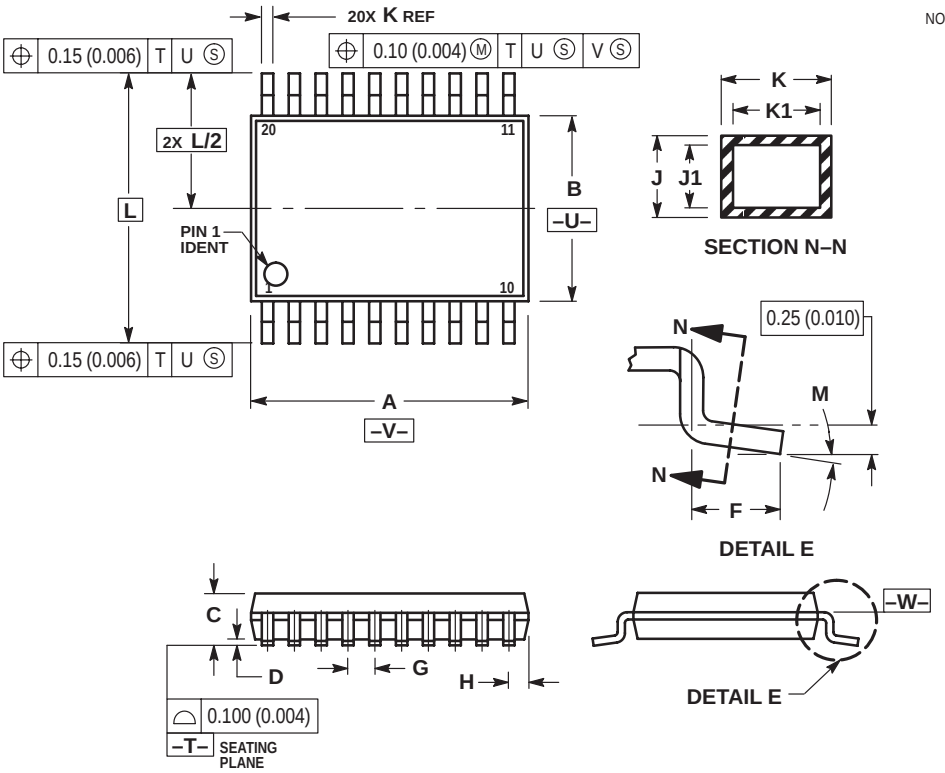


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –U–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	——	6.60	——	0.260
B	4.30	4.50	0.169	0.177
C	——	1.20	——	0.047
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC		0.026 BSC	
H	0.275	0.375	0.011	0.015
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	0°	10°	0°	10°

CASE 948D–03
ISSUE B
(TSSOP–20)

CASE DIMENSIONS (continued)

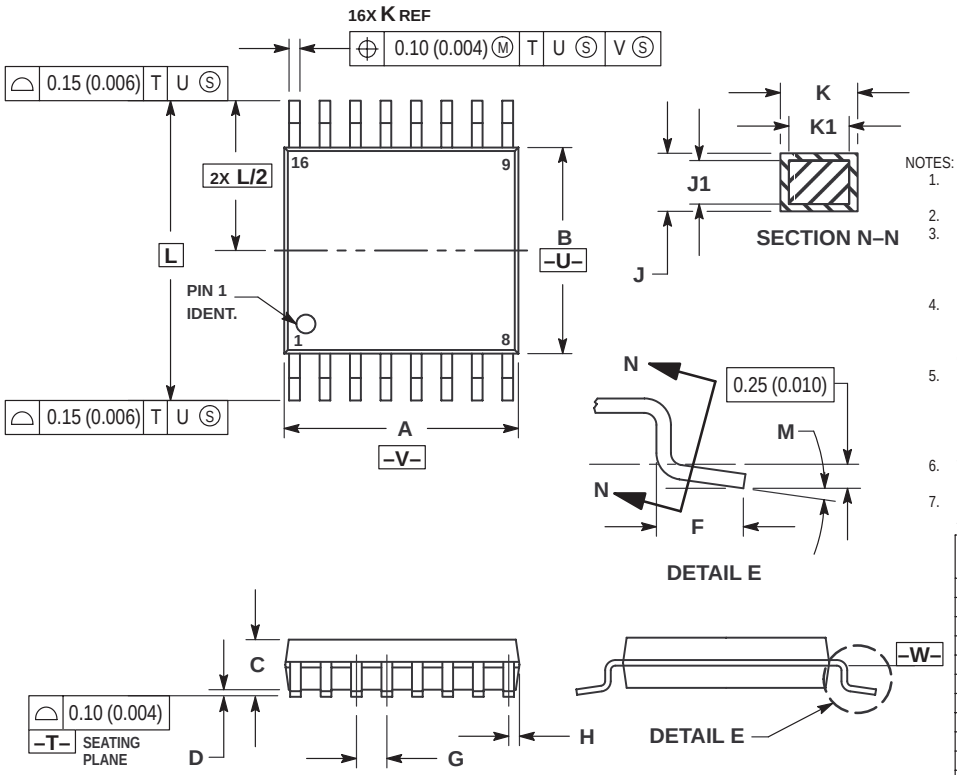


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

CASE 948E–02
ISSUE A
(TSSOP–20HS)

CASE DIMENSIONS (continued)

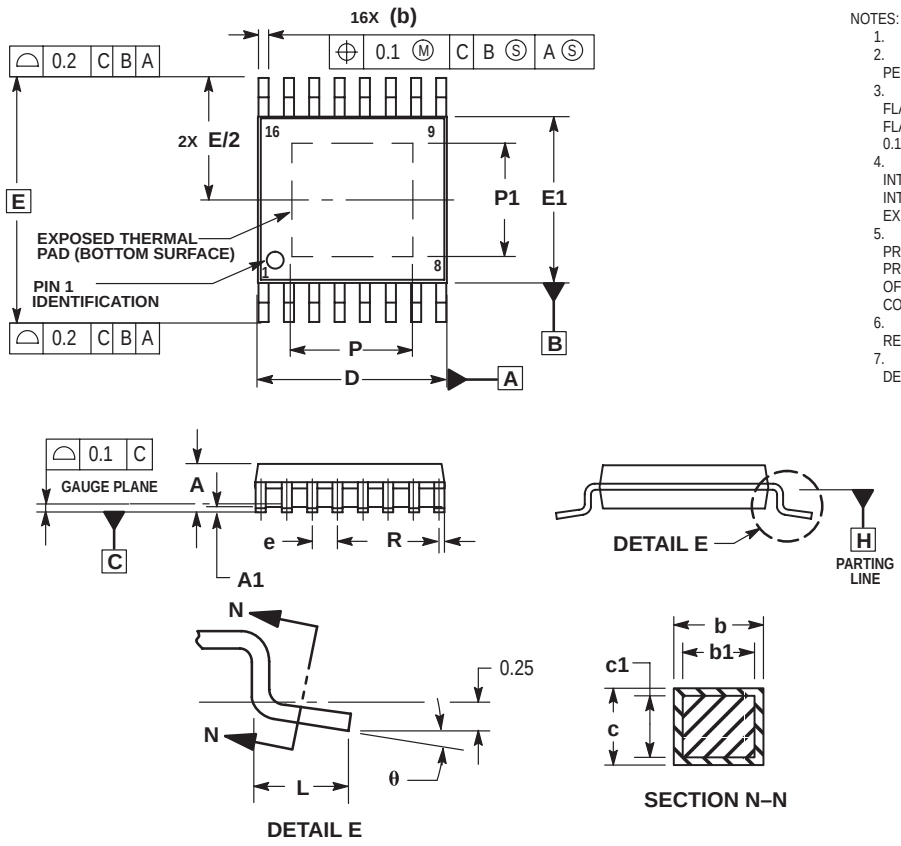


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

CASE 948F–01
ISSUE O

CASE DIMENSIONS (continued)

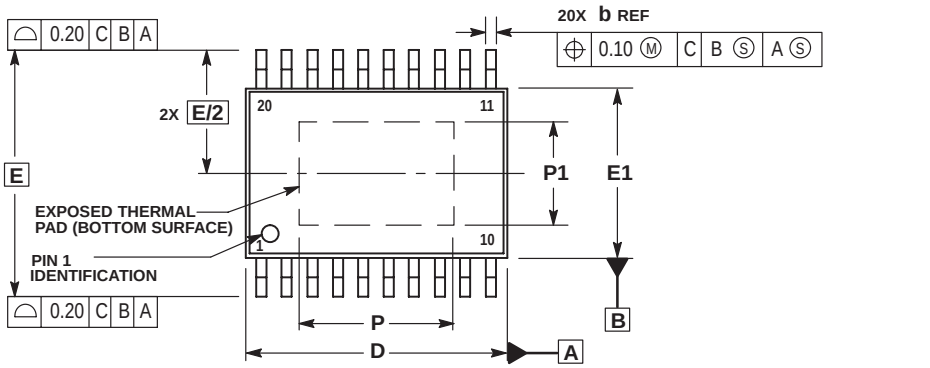


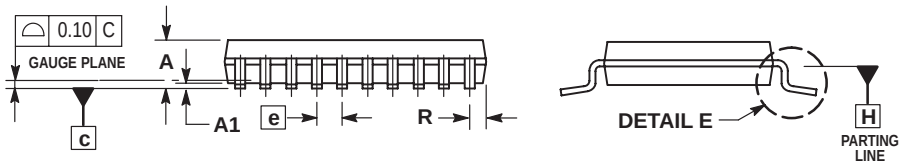
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE H.

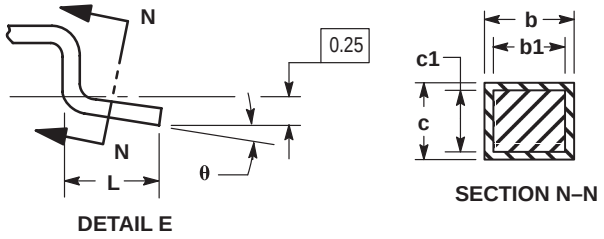
	MILLIMETERS	
DIM	MIN	MAX
A	—	1.2
A1	0	0.15
b	0.19	0.3
b1	0.19	0.25
c	0.09	0.2
c1	0.09	0.16
D	4.9	5.1
E	6.40 BSC	
E1	4.3	4.5
e	0.65 BSC	
L	0.5	0.75
P	—	3.9
P1	—	3
R	0.18	0.28
θ	0°	8°

CASE 948L–01
ISSUE A

CASE DIMENSIONS (continued)





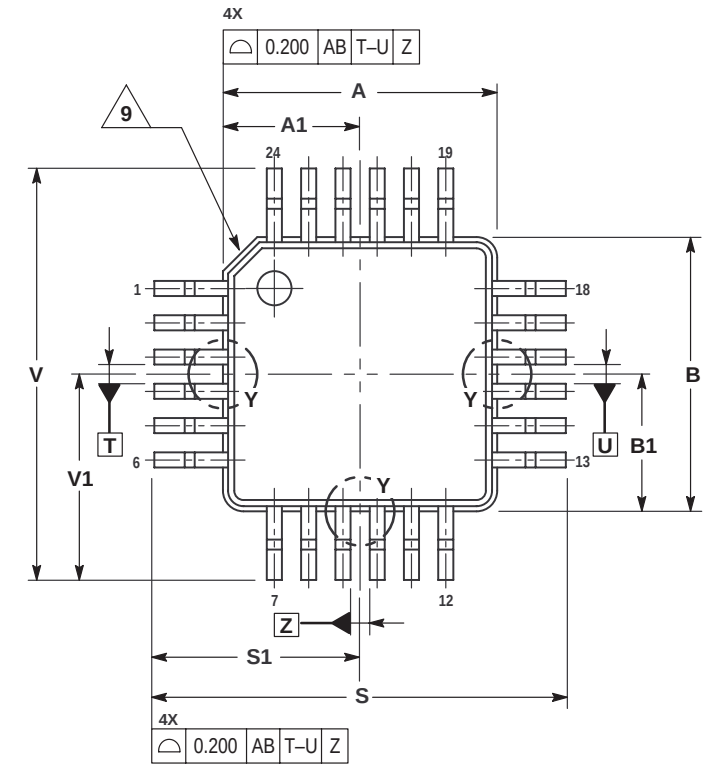


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	—	1.20
A1	0.00	0.10
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	6.40	6.60
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.50	0.75
P	—	4.80
P1	—	3.00
R	0.27	0.37
θ	0 °	8 °

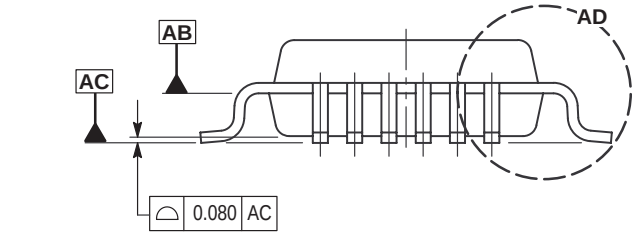
CASE 948M–01
ISSUE O

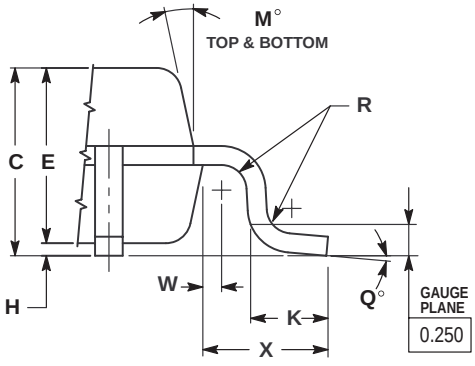
CASE DIMENSIONS (continued)



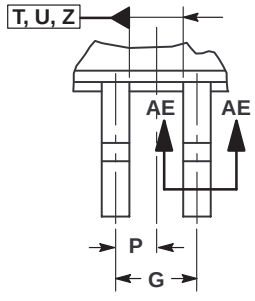
NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT DATUM PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	4.000 BSC	
A1	2.000 BSC	
B	4.000 BSC	
B1	2.000 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
Q	0°	7°
R	0.150	0.250
S	6.000 BSC	
S1	3.000 BSC	
V	6.000 BSC	
V1	3.000 BSC	
W	0.200 REF	
X	1.000 REF	

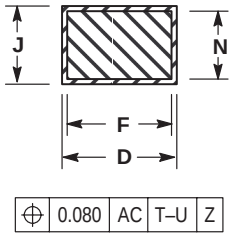




DETAIL AD



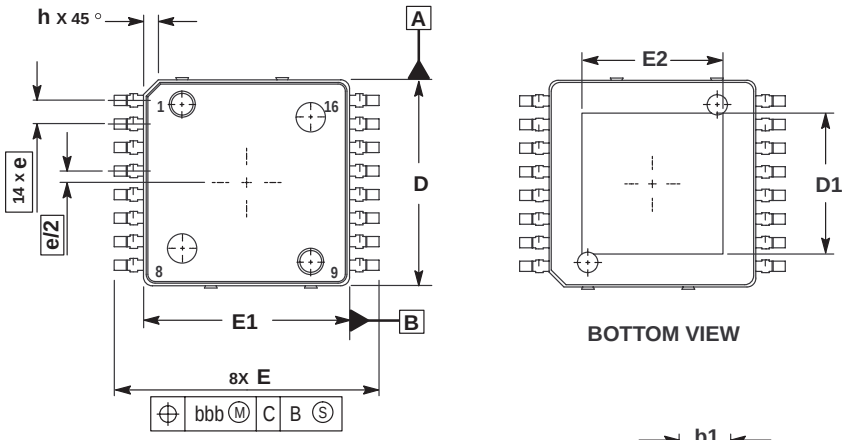
DETAIL Y



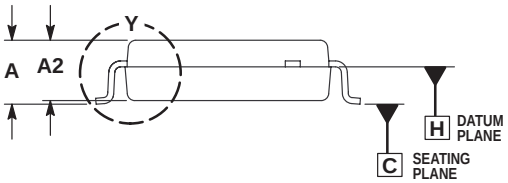
SECTION AE–AE

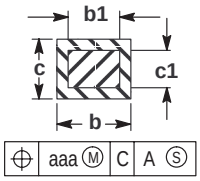
CASE 977–02
ISSUE A

CASE DIMENSIONS (continued)

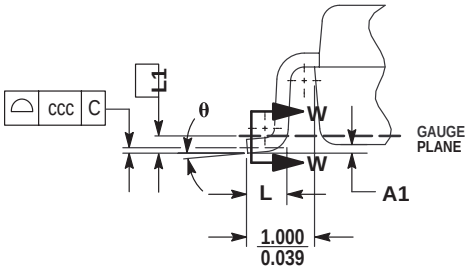


BOTTOM VIEW





SECT W–W

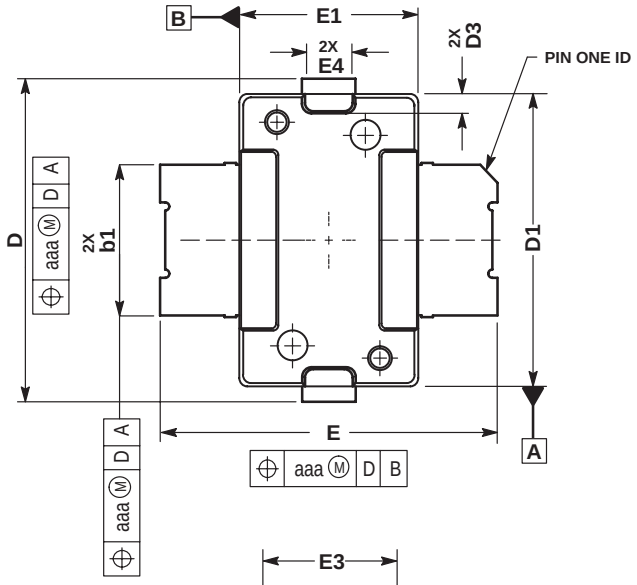


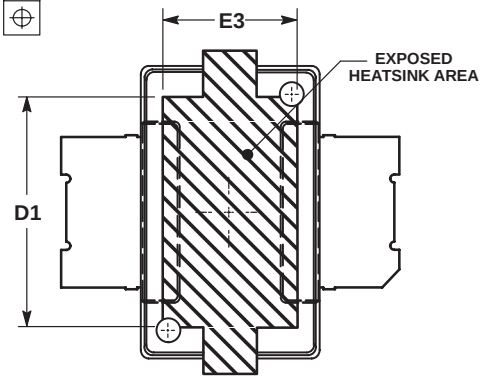
DETAIL Y

NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

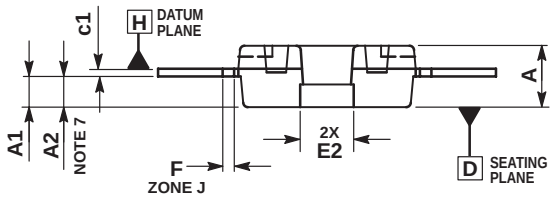
	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.300
A1	0.025	0.100
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	—	0.600
θ	0 °	7 °
aaa	0.200	
bbb	0.200	
ccc	0.100	

CASE 978–03
ISSUE B
(PFP–16)





BOTTOM VIEW

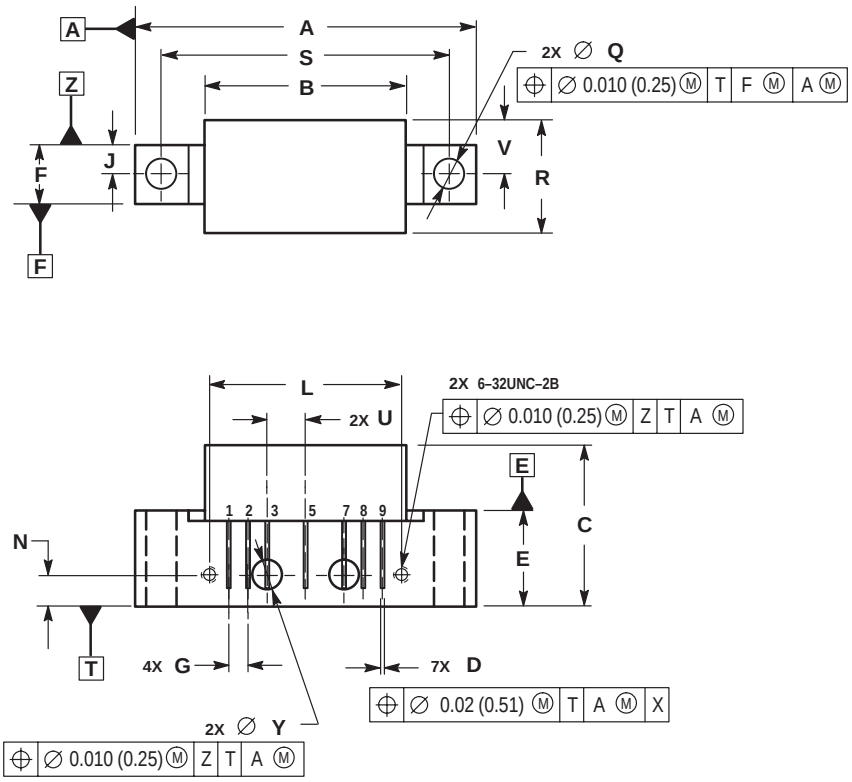


NOTES:
1. CONTROLLING DIMENSION: INCH.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.006 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.005 TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

	INCHES	
DIM	MIN	MAX
A	0.076	0.084
A1	0.038	0.044
A2	0.040	0.042
D	0.416	0.424
D1	0.376	0.384
D2	0.290	0.320
D3	0.016	0.024
E	0.436	0.444
E1	0.236	0.244
E2	0.066	0.074
E3	0.150	0.180
E4	0.058	0.066
F	0.025 BSC	
b1	0.193	0.199
c1	0.007	0.011
aaa	0.004	

CASE 1265–04
ISSUE C
(TO–270)

CASE DIMENSIONS (continued)



NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	——	1.775	——	45.08
B	——	1.085	——	27.56
C	——	0.840	——	21.34
D	0.015	0.021	0.38	0.53
E	0.465	0.510	11.81	12.95
F	0.300	0.325	7.62	8.25
G	0.100 BSC		2.54 BSC	
J	0.156 BSC		3.96 BSC	
K	0.315	0.355	8.00	8.50
L	1.00 BSC		25.40 BSC	
N	0.165 BSC		4.19 BSC	
P	0.100 BSC		2.54 BSC	
Q	0.148	0.168	3.76	4.27
R	——	0.600	——	15.24
S	1.500 BSC		38.10 BSC	
U	0.200 BSC		5.08 BSC	
V	——	0.250	——	6.35
W	0.435	0.450	11.05	11.43
X	0.400 BSC		10.16 BSC	
Y	0.152	0.163	3.85	4.15
Z	0.009	0.011	0.23	0.28

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

CASE 1302–01
ISSUE O

Chapter Ten
Applications and Product Literature

Motorola's Applications Literature provides guidance to the effective use of its semiconductor families across a broad range of practical applications. Many different topics are discussed in a way that is not possible in a device data sheet, from detailed circuit designs complete with PCB layouts, through matters to consider when embarking on a design, to complete overviews of product families and their design philosophies.

Information is presented in the form of Application Notes, Article Reprints and detailed Engineering Bulletins.

Table of Contents

	Page
Applications Literature	10.1–2
Product Literature	10.1–3

Literature

Application Notes, Engineering Bulletins and Article Reprints of special interest to designers of RF and RF/IF equipment are listed below. This technical documentation is available on the Motorola Semiconductor Product Sector Web site or is available through the Motorola Literature Distribution Center. Phone and fax numbers for ordering literature are listed on the back cover of this book and in our Accessing Data On–line section.

Application Notes

AN139A Understanding Transistor Response Parameters
AN211A Field Effect Transistors in Theory and Practice
AN215A RF Small–Signal Design Using Two–Port Parameters
AN238 Transistor Mixer Design Using 2–Port Parameters
AN267 Matching Network Designs with Computer Solutions
AN282A Systemizing RF Power Amplifier Design
AN419 UHF Amplifier Design Using Data Sheet Design Curves
AN423 Field Effect Transistor RF Amplifier Design Techniques
AN535 Phase–Locked–Loop Design Fundamentals
AN548A Microstrip Design Techniques for UHF Amplifiers
AN555 Mounting Stripline–Opposed–Emitter (SOE) Transistors
AN593 Broadband Linear Power Amplifiers Using Push–Pull Transistors
AN721 Impedance Matching Networks Applied to RF Power Transistors
AN749 Broadband Transformers and Power Combining Techniques for RF
AN758 A Two–Stage 1 kW Solid–State Linear Amplifier
AN762 Linear Amplifiers for Mobile Operation
AN779 Low–Distortion 1.6 to 30 MHz SSB Driver Designs
AN790 Thermal Rating of RF Power Transistors
AN791 A Simplified Approach to VHF Power Amplifier Design
AN827 The Technique of Direct Programming by Using a Two–Modulus Prescaler
AN860 Power MOSFETs versus Bipolar Transistors
AN878 VHF MOS Power Applications
AN923 800 MHz Test Fixture Design
AN955 A Cost Effective VHF Amplifier for Land Mobile Radios
AN1022 Mechanical and Thermal Considerations in Using RF Linear Hybrid Amplifiers
AN1024 RF Linear Hybrid Amplifiers
AN1025 Reliability Considerations in Design and Use of RF Integrated Circuits
AN1026 Extending the Range of an Intermodulation Distortion Test
AN1027 Reliability/Performance Aspects of CATV Amplifier Design
AN1028 35/50 Watt Broadband (160 – 240 MHz) Push–Pull TV Amplifier Band III
AN1029 TV Transposers Band IV and VP_O = 0.5 W/1.0 W
AN1030 1 W/2 W Broadband TV Amplifier Band IV and V
AN1032 How Load VSWR Affects Non–Linear Circuits
AN1033 Match Impedances in Microwave Amplifiers
AN1034 Three Balun Designs for Push–Pull Amplifiers
AN1037 Solid–State Power Amplifier — 300 Watt FM, 88–108 MHz
AN1038 1.2 V, 40 – 900 MHz Broadband Amplifier with the TP3400 Transistor
AN1039 470 – 860 MHz — Broadband Amplifier – 5 W
AN1040 Mounting Considerations for Power Semiconductors
AN1041 Mounting Procedures for Very High Power RF Transistors
AN1107 Understanding RF Data Sheet Parameters
AN1207 The MC145170 in Basic HF and VHF Oscillators
AN1253 An Improved PLL Design Method Without ϖn and ζ
AN1277 Offset Reference PLLs for Fine Resolution or Fast Hopping
AN1526 RF Power Device Impedances: Practical Considerations
AN1528 Packaging Considerations for RF Transistors
AN1529 RF Power Circuit Concepts Using FETs and BJTs
AN1530 Motorola Advanced Amplifier Concept Package
AN1531 Parameter Extraction Techniques for RF Power Transistors Models
AN1539 An IF Communication Circuit Tutorial
AN1575 Worldwide Cordless Telephone Frequencies
AN1580 Mounting and Soldering Recommendations for the Motorola Power Flat Pack Package
AN1599 Power Control with the MRFIC0913 GaAs Integrated Power Amplifier and MC33169 Support IC
AN1602 3.6 V and 4.8 V GSM/DCS1800 Dual Band PA Application with DECT Capability Using Standard Motorola RFIC's
AN1610 Using Motorola's MRFIC1502 in Global Positioning System Receivers
AN1617 Mounting Recommendations for Copper Tungsten Flanged Transistors
AN1639 Phase Noise Measurement Using the Phase Lock Technique
AN1643 RF LDMOS Power Modules for GSM Base Station Application: Optimum Biasing Circuit
AN1658 Converting MC13110/13111 Based Designs to the MC13110A,B/13111A,B
AN1670 60 Watts, GSM 900 MHz, LDMOS Two–Stage Amplifier

Literature (continued)

AN1671 MC145170 PSpice Modeling Kit
AN1673 Solder Reflow Mounting Method for the MRF286 and Similar Packages
AN1674 Mounting Method with Mechanical Fasteners for the MRF286 and Similar Packages
AN1675 A Low Noise Amplifier with High IP3 for the 900 MHz Band Using the MRF1057T1 Low Noise Transistor
AN1676 A Cascade 2 Stage Low Noise Amplifier Using the MRF1047T1 Low Noise Transistor
AN1687 A Full–Featured Wireless Interface for RS–232 Communications
AN1691 Practical Solutions for Medium Data Rate Wireless Communications
AN1696 Broadband Intermodulation Performance Development Using the Rohde & Schwarz Vector Network Analyzer ZVR
AN4005 Thermal Management and Mounting Method for the PLD 1.5 RF Power Surface Mount Package

Article Reprints

AR141 Applying Power MOSFETs in Class D/E RF Power Amplifier Design
AR164 Good RF Construction Practices and Techniques
AR165S RF Power MOSFETs
AR176 New MOSFETs Simplify High Power RF Amplifier Design
AR254 Phase–Locked Loop Design Articles
AR305 Building Push–Pull, Multioctave, VHF Power Amplifiers
AR313 Wideband RF Power Amplifier
AR346 RF Power FETs – Their Characteristics and Applications, Parts 1 & 2
AR347 A Compact 1–kW 2–50 MHz Solid State Linear Amplifier
AR510 VSWR Protection of Solid State RF Power Amplifiers
AR511 Biasing Solid State Amplifiers to Linear Operation
AR571 Silicon MOSFET Technology for Wireless Communications
AR573 Modeling a New Generation for RF Devices: MOSFETs of L–Band Applications
AR579 CAD of a Broadband, Class–C 65 Watt UHF Power Amplifier
AR580 MOSFET RF Power: An Update — Parts 1 and 2
AR581 Procedure Performs Thermal Measurements on Pulsed Devices
AR582 MIMP Analyzes Impedance Matching Networks
AR583 Power MOSFETs Handle Bipolar Amp Applications
AR586 Power MOSFETs versus Bipolar Transistors
AR589 QSPLOT Utility Displays S–Parameter Data
AR594 GaAs RF ICs Target 2.4–GHz Frequency Band
AR596 Design and Performance of a Low Voltage, Low Noise 900 MHz Amplifier
AR606 PCS and RF Components
AR612 Plastic Packages Hold Power RF MOSFETs
AR614 Advantages of LDMOS in High Power Linear Amplification
AR624 Aluminum–Based Metallization Enhances Device Reliability
AR628 Impedance Measurements for High Power RF Transistors Using the TRL Method
AR629 Digital Predistortion Techniques for RF Power Amplifiers with CDMA Applications

Engineering Bulletins

EB19 Controlled – Q RF Technology — What It Means, How It's Done
EB27A Get 300 Watts PEP Linear Across 2 to 30 MHz from This Push–Pull Amplifier
EB38 Measuring the Intermodulation Distortion of Linear Amplifiers
EB63 140 W (PEP) Amateur Radio Linear Amplifier 2 – 30 MHz
EB74 A 10 Watt, 225 – 400 MHz Amplifier — MRF331
EB77 A 60–Watt, 225 – 400 MHz Amplifier — 2N6439
EB89 A 1–Watt, 2.3 GHz Amplifier
EB104 Get 600 Watts RF from Four Power FETs
EB105 A 30 Watt, 800 MHz Amplifier Design
EB107 Mounting Considerations for Motorola RF Power Modules
EB202 RF Transistor Design
EB209 Mounting Method for RF Power Leadless Surface Mount Transistors
EB211 Thermal Management and Solder Mounting Method for the MRF286, 60 Watt Power Device in a CuW (Copper Tungsten) Base Package

Product Literature

SG46/D Wireless Semiconductor Solutions RF and IF Selector Guide
CD301/D Wireless Semiconductor Solutions RF and IF CD–ROM
CD303/D RF LDMOS Technology CD–ROM
BR1502/D Wireless Infrastructure Solutions
BR1504/D RF Power Solutions
BR3031/D Wireless Infrastructure DSP Solutions
SG382/D Motorola RF CATV Distribution Amplifier Selector Guide
SG384/D Motorola LDMOS Product Family Selector Guide

Chapter Eleven

Motorola Distributor & Worldwide Sales Offices

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- Newark 1–800–4NEWARK

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